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# NASA TECH BRIEF



## Failure Rates for Accelerated Acceptance Testing of Silicon Transistors

Extrapolation tables for the control of silicon transistor product reliability have been compiled in a *Handbook of Extrapolated Lambda Sampling Plans for Silicon Transistors.* The tables are based on a version of the Arrhenius statistical relation and are intended to be used for low- and medium-power silicon transistors as an extension of the lambda sampling plans contained in MIL-S-19500 (Table C-I). The purpose of the extrapolating tables is twofold: first, to bridge the gap between the life-test failure-rate lambda value selected at maximum rated test conditions and that expected at derated operating levels; and second, to provide a guideline for estimating economic sample sizes.

The Arrhenius relation was chosen as the means of extrapolating because of theoretical consideration related to the physical–chemical reactions of silicon transistor materials under conditions of varying temperature and because it is the most widely published and accepted extrapolation procedure in the semiconductor industry. The acceleration factor of $7.5 \times 10^3$°K used in the construction of the extrapolation tables is a conservative estimate; the value was derived on the basis of a literature search.

The extrapolation tables become meaningful provided that the units which comprise the test sample pass the appropriate sampling plan and are selected from a population that has been 100% screened for latent and potential failures attributable to processing and/or workmanship discrepancies.

There is an extrapolation table corresponding to each sampling plan in Table C- I of the MIL-S-19500. The tables are indexed according to the sampling plan lambda value arranged in descending order, the sample size, and the number of failures permitted (acceptance number).

The temperature range of the tables is from 200° to 25°C in decrements of 5°. The high temperature of 200°C is perhaps the most common temperature at which low- and medium-power silicon transistors are life-tested and at which there exists a relation to operating life tests. Operating derating curves between maximum rated dissipation and 200°C are usually available from semiconductor manufacturers.

The tables contain failure rate values (%/100 hours) for confidence limits of 10, 60, 70, 80 and 90%. The 60% and 90% values are the ones most commonly referred to; the 10% value is presented for information purposes only.

The tables can be used in either of two ways. First, having selected a lambda value at maximum thermal test conditions, one can obtain the maximum expected failure rate (%/1000 hours) at "in-use" conditions by matching the derated "in-use" temperature (°C) with the desired level of confidence (%). Second, the tables may be used in an inverse fashion. For example, knowing the failure rate required for a derated "in-use" condition, one can obtain an appropriate sampling plan that would give the necessary assurance at maximum rating. If there were a large range of failure rates required, more than one sampling plan might be acceptable. In that case, cost considerations would be the determining factor in selecting the most satisfactory plan.

**Note:**

Copies of the Handbook are available from:
Clearinghouse for Federal Scientific and Technical Information
Springfield, Virginia 22151
Price $3.00
Reference: TSP68-10541

**Patent status:**

No patent action is contemplated by NASA.

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