

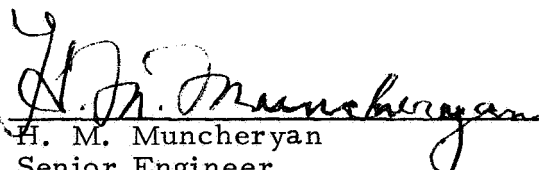
STUDY OF FAILURE AND RELIABILITY IN
MICROELECTRONIC DEVICES
8th QUARTERLY SUMMARY REPORT

16 October 1967

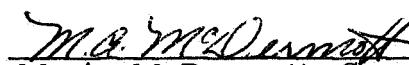
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NATIONAL AERONAUTICS AND SPACE ADMINISTRATION
ELECTRONIC RESEARCH CENTER

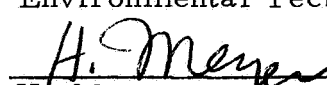
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ABSTRACT

Four groups of integrated microcircuits produced by various manufacturers were subjected to thermal cycling, step-stress tests, and operating life tests in excess of 10,000 hours. These tests variously resulted in the electrical failure modes characterized by I_{CEX} , I_R , I_{EBO} , I_{CBO} , $V_{BE(Sat)}$, h_{FE} , BV_{CEO} , and BV_{CBO} . These failure modes were verified metallographically by direct observation from the uncapped devices and by indirect failure derivations.

The combined data from environmental and operating life tests provided considerable knowledge and information for determining the failure mechanisms of the failure modes encountered during this investigation. The major mechanisms identified were inhomogeneous aluminum metallization, faulty contact deposition, bubbles and pinholes in the pyrolytic passivation film, with randomly occurring cracks or surface pits in the silicon pellet. Other discrepancies were also observed which were attributed to surface reactions, such as inversion layer formation, ionic migration at the silicon dioxide surface, ionic entrapment at oxide defects, and metallization changes. Bond separation in two of the specimens was caused by the formation of a brittle inter-metallic compound (purple plague) at the gold-to-aluminum bond interface. A short in a gate diode was conducive to a microcrack initiated in the P-N junction during bonding operation and subsequent diffusion of aluminum metallization into the crack during life tests. Frequently observed misaligned bonds had caused in at least one instance a short in the output pin.

Through these failure evaluations and analyzed data, all failure modes encountered in this program could be reduced to three fundamental failure indicators, namely, leakage current (I_R), breakdown voltage (BV), and output saturation voltage (V_{SAT}), all other failure indicators being derivations of the respective failure types, which are verifiable metallographically. The continuing tests and studies under the extended physics of failure contract will utilize these failure indicating parameters as the building blocks in the evaluation testing and the development of effective device screening methods for achieving high device reliability and long service life.

STUDY OF FAILURE AND RELIABILITY IN MICROELECTRONIC DEVICES

1.0 INTRODUCTION

1.1 General

This report summarizes the highlights of the study and evaluation of failure mechanisms in microelectronic devices conducted under a NASA/ERC Contract No. NAS 12-72, during the past several years at Librascope. Particular consideration is given to the information and knowledge derived from the environmental and life tests conducted that may contribute toward the establishment of device screening and selection criteria. Electrical failure modes that were encountered either in environmental or life tests are discussed in relation to their microscopic verification and possible process corrective measures. It will be evident that some progress was made in this direction whereby the resulting finding could be utilized in future and more advanced studies of the failure phenomena and mechanisms involving the cause and effect of such phenomena.

The extension of this program to further and more detailed investigation of the failure mechanisms in microelectronic devices through the extended Contract No. NAS 12-72 is anticipated to be particularly productive in producing results to validate certain of the test methods as forming the basis for the selection of the ultimate screening criteria for the devices. It has already been proved during the past investigation program that a definite relation exists between electrical failure modes and device fabrication process discrepancies, which in majority may be considered to arise from elements of human error. It is certainly the anticipated objective of this program to explore and determine means and expedience to reduce such elements to a minimum or nil. This end may be achieved through obtaining and evaluating data relative to the effectiveness of the various device screening tests to establish criteria correlative between electrical failure modes and the associated device fabrication deficiencies. Some valuable data have already been derived from the preceding investigations which reflect such an achievement to reside within the capability of the present course of endeavor. The ultimate goal of the present study and evaluation then will include the determination of reliability indicating electrical parameters that would enable the prediction of relative service life of microelectronic semiconductor devices.

1.2 Objectives

The objectives of the program were:

- (a) To explore and detect failure modes in semiconductor devices through accelerated testing and to develop techniques to determine their failure mechanisms.
- (b). To isolate predominant failure mechanism through testing as a function of stress level and process control, and to identify the processes that require additional controls to achieve high reliability.

1.2 Objectives (Cont.)

(c) To develop screening techniques through identification and verification of failure mechanisms in an effort to establish criteria for selecting high-reliability devices.

These objectives have been partially achieved in the preceding investigation program and will be complemented by the continuing test and evaluation program. The recently extended test program will lead to the determination and development of an effective screening method through comparative study of failure and cause and defining of valid reliability-indicating parameters. The achievement of the ultimate goal will be further prevailed by the selection and use of a single-type device for the entire test program.

1.3 Summary of Work Accomplished

This program was initiated 2-1/2 years ago at Librascope under the sponsorship of NASA/ERC as a physics of failure study and evaluation program of microelectronic circuits. The investigation generally included temperature cycling, thermal step-stress tests, and operating life tests. The failure analysis consisted of a preliminary failure analysis and a detailed failure analysis. The preliminary failure analysis was instituted on all degradation failures and consisted of repeating the initial measurements in an effort to locate and identify the circuit element causing an out-of-tolerance drift. The detailed failure analysis was performed subsequent to the preliminary analysis to determine the failure mechanism or other physical phenomena which induced the particular failure. The failure degradative criteria were based on the maximum allowable tolerance limits shown in Table 1. The test and evaluation proceeded in accordance with the sequential scheme shown in the flow chart of Figure 1.

One hundred fifteen devices from each of the four vendor lots were tested, first environmentally and later by operating life tests. Following each step of testing, electrical parameter measurements were taken. If catastrophic failures occurred, selected representative specimens, when applicable, were uncapped and examined microscopically. The latter examination was extended to the removal of the aluminum metallization by means of HCl, and the SiO₂ by means of HF for diagnosis of the degraded active junctions thereunder. This procedure further permitted the measurement of thickness to be made on both the metallization and SiO₂ layers. The evidence proved that in most cases inadequate control was employed over oxidations and metallization processes. The temperature step-stress test revealed improper mask alignment in certain cases, causing excessive leakage conditions. Presence of intermetallic complex (Au-Al) at gold-to-aluminum bond interface was predominant after thermal step stress, which condition gave rise to an increase in output transistor saturation voltage, causing open bonds in some of the devices. Fairchild devices yielded the greatest failure rates, while Signetics devices showed the smallest failure rate per 1000 hour of operating conditions. These findings uncovered the various existing fabrication and process problems in the devices tested, the findings also established a basis for the use of further and more advanced techniques of testing and

Figure 1. Flow Chart of Physics of Failure Program

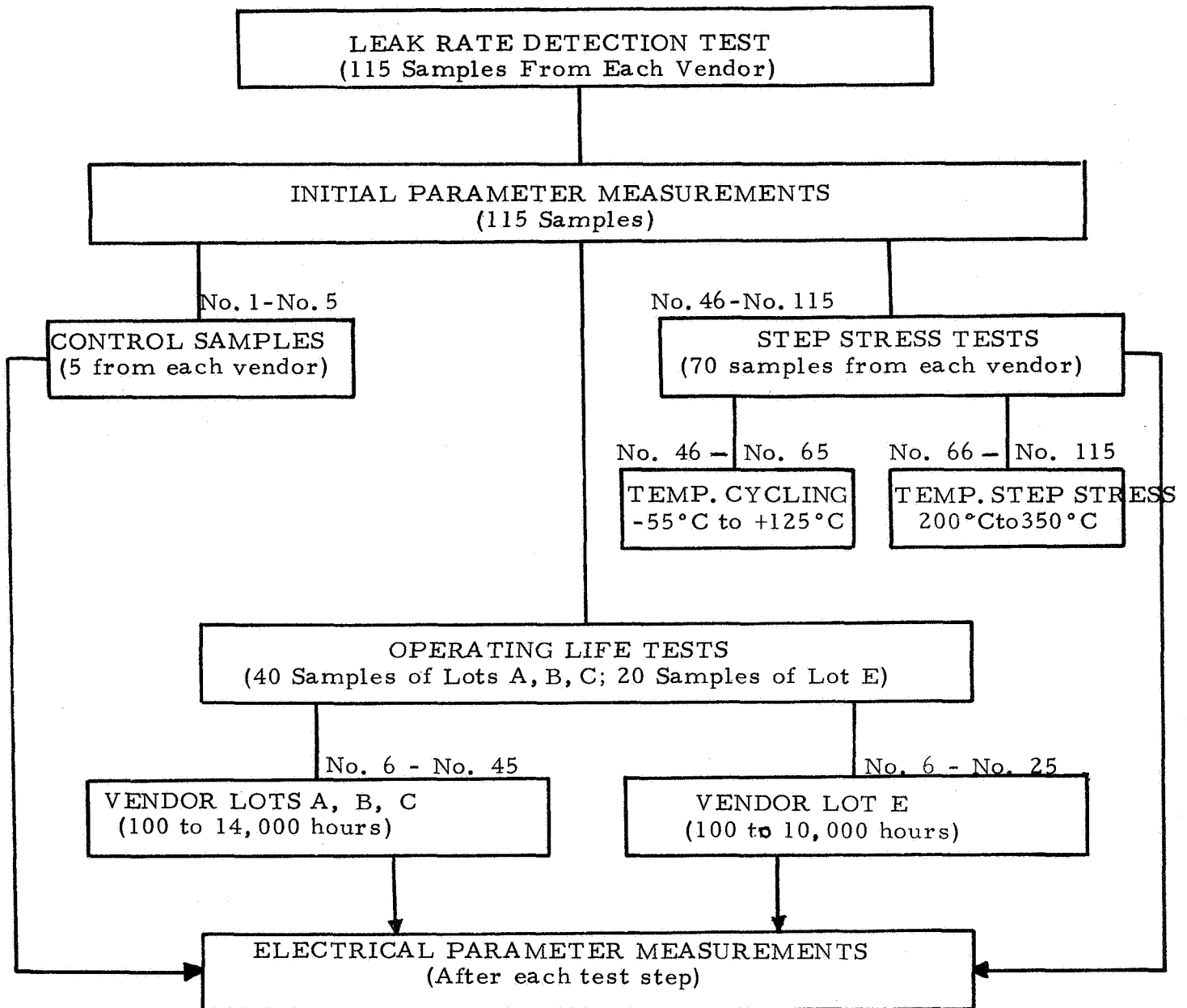


TABLE 1 - Failure Criteria

Parameter Type	Change
Reverse Junction Current I_R , I_{CBO} , I_{CRO}	Initial X 10 but greater than 10 n amp
Output Saturation Voltage $V_{CE(SAT)}$	$\pm 10\%$ of initial value but greater than ± 10 mv
Effective Gain h_{FE}	$\pm 20\%$ of initial value
Resistance	$\pm 10\%$ of initial value
Junction Breakdown Voltages BV_R , BV_{CBO} , BV_{CEO}	$\pm 25\%$ of initial value -20%

1.3 Summary of Work Accomplished (Cont.)

evaluation whereby an effective and valid device-screening method could be emanated as the ultimate goal of this failure analysis program.

2.0 INVESTIGATION

2.1 Operating Life Tests

2.1.1 Types of Devices Tested

The test specimens employed in this study and evaluation program were generally NAND/NOR gate type microcircuits procured from three different manufacturers direct. The manufacturers were: Fairchild, whose devices were referred to as Vendor Lot A in the prior reports and in some tables for sake of convenience; Motorola, whose devices were designated Vendor Lot B; and, Signetics, whose devices were designated Vendor Lot C. Since Motorola supplied two types of microcircuits, the second type was referred to as Vendor Lot E devices. Motorola (Lot E) devices differed from Motorola (Lot B) devices in that the Motorola (Lot E) devices had aluminum leads bonded to aluminum pads and were packaged in flat packs. The devices of all other vendors, including Motorola Lot B, had gold leads bonded to aluminum pads and were packaged in modified TO-5 cans. The types and part numbers of the various vendor devices used in this program are given in Table 2.

Each of the device manufacturers was given a briefing of the application of his devices and the objectives of the tests to which the devices would be subjected. The manufacturers further were given the opportunity of making suggestions and comments when applicable.

2.1.2 Operating Life Test Conditions

The specimens were subjected to an ambient temperature of $125^{\circ} \pm 3^{\circ} \text{C}$. During testing, the specimens were switched parallel from "0" to "1" state at a 1-megacycle pulse repetition rate. Each gate was loaded with a resistor-capacitance network to simulate maximum fan-out. The unused diodes were tied to the V_{CC} supply. The life tests were interrupted and post environmental measurements were performed at intervals of 100, 250, 500, 1000 hours and every 1000 hour duration thereafter. The Fairchild, Motorola (Lot B) and Signetics devices received 14,000 hours of life test, and Motorola (Lot E) devices received 10,000 hours of life test because the Motorola (Lot E) device tests were started later than the other lots.

TABLE 2. Device Identification List (Life Tests)

Manufacturer	Reference Code	Part Number	Part Description	Quantity Tested	
				Control	Tested
Fairchild	A	SL-1519	DTL Dual Gate	1-5	6-45
Motorola	B	SC-736	DTL NAND/NOR Gates	1-5	6-45
Signetics	C	SE-102K	DTL NAND/NOR Gates	1-5	6-45
Motorola	E	MC-930	Dual NAND/NOR Gates	1-5	6-25

The circuit diagrams of the devices are given in Figures 2, 3 and 4.

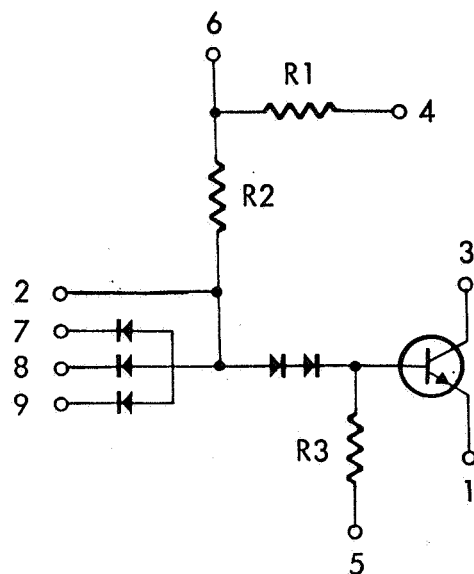


FIGURE 2. Motorola and Signetics Gate Circuit

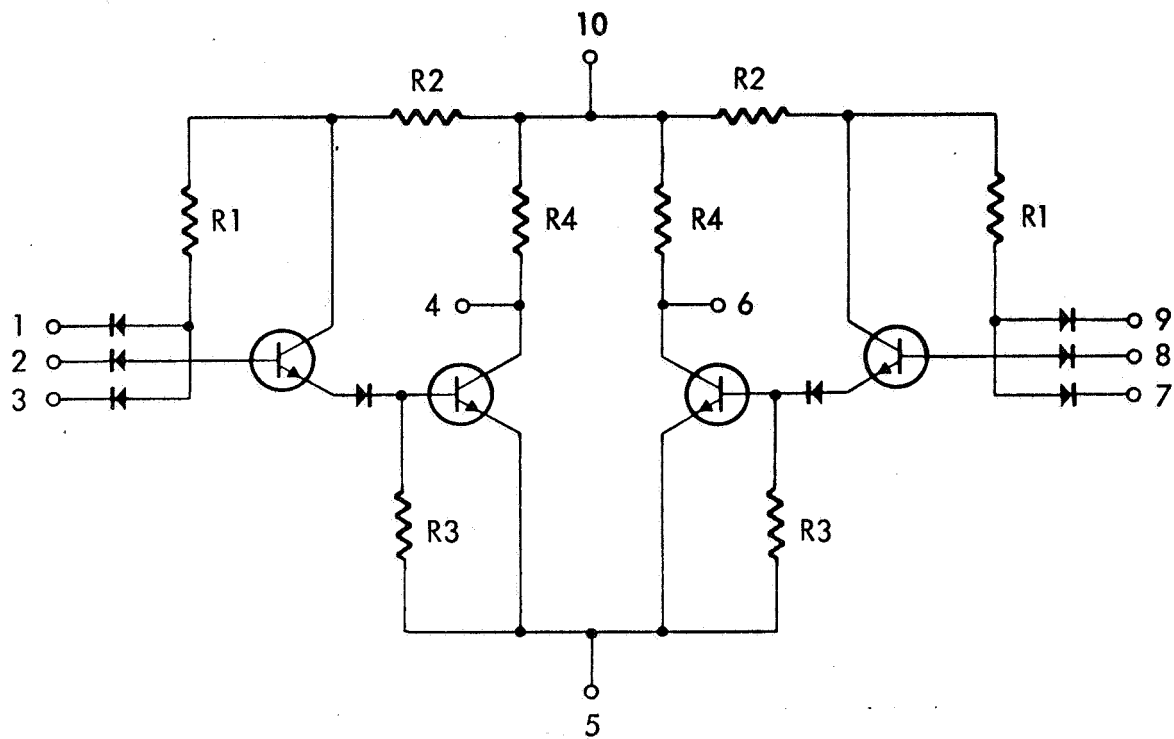


FIGURE 3. Fairchild Gate Circuit

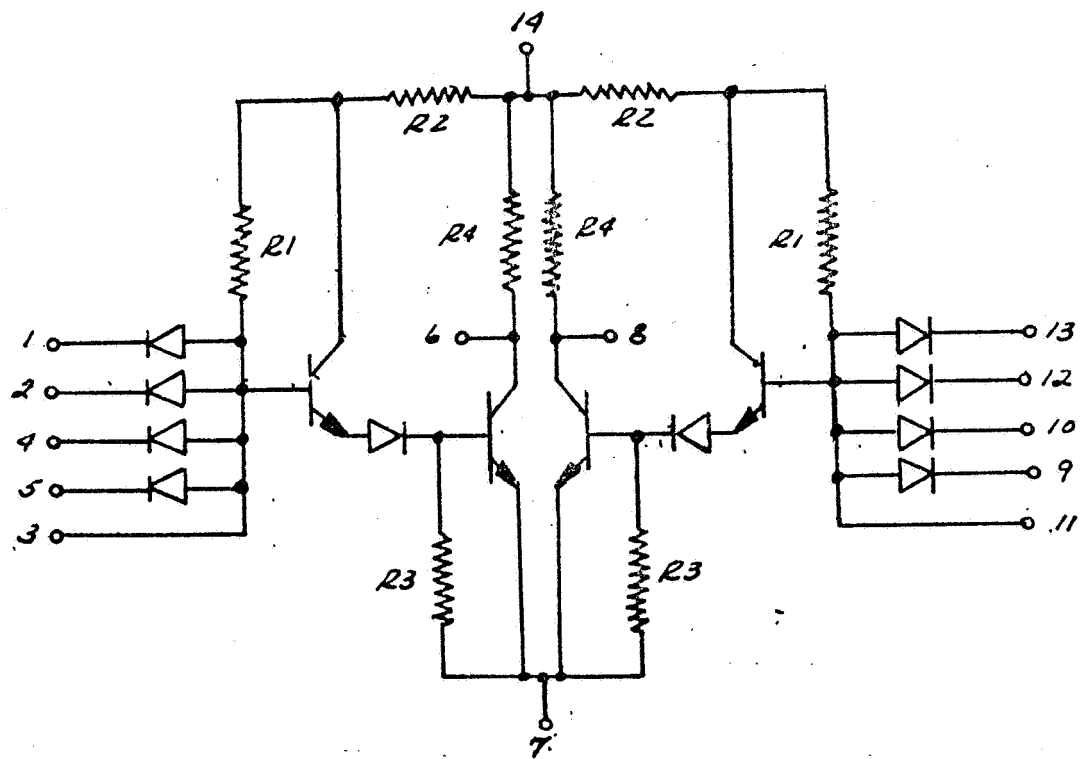


FIGURE 4. Motorola Flat Pack Gate Circuit

2.1.3 Vibration Tests

Subsequent to 12,000 hour life test of the Fairchild, Motorola (Lot B) and Signetics devices and after 8000 hour life test of Motorola (Lot E) devices, specimens were randomly selected from these vendor lots and subjected to a vibration test in a plane perpendicular to the device active surface. The devices were vibrated 15 minutes. Each cycle consisted of vibrating the devices from 10 cps to 55 cps and back to 10 cps in one minute. No failure occurred in Fairchild and Signetics devices. Two specimens each from Motorola (Lot B) and (Lot E) devices failed during vibration. The failure modes occurred by increases in I_{CEX} , $V_{(Sat)}$, I_{T2} , and a decrease in BV, indicating a short at the respective pin.

2.2 Investigation of Failure Modes

2.2.1 Experimental Procedure

Selected devices from parametrically failed categories were carefully uncapped to preserve the contents of each package intact. The uncapped devices were viewed with a microscope at varying magnifications to study the effect produced on the device structure by various environmental tests and later by life tests. The top views of the devices revealed the following discrepant conditions: growth of intermetallic compound ($AuAl_2$, possibly with Au-AlSi complex) at the bond interface of those specimens having gold-to-aluminum lead connections; this condition shown in Figure 5, was electrically determined as output transistor saturation ($V_{CE(Sat)}$). In some failed devices, the thin-film aluminum metallization was porous and appeared crazed, as exemplified in Figure 5. Surface contamination was prominent in random devices of each vendor lot; examples are given in Figures 6 and 7. Figure 7 further presents excessive pinhole and porosity, and misaligned bonds on metallization pads, which condition gave rise to breakdown voltage (BV) discrepancy in the device.

Misalignment of bonds was quite frequent, particularly in Motorola (Lot B), as will be noted from Figure 8. When the bond is so misaligned that it partially extends over the active region of a poorly silicon-dioxide-isolated diode or transistor, the condition may cause a short at the P-N junction either by direct contact of the bond with the P-N regions or by metallic diffusion into the degraded region and bridging the two active regions. Examples of electrical shorts occurring in the latter manner are shown in Figures 9 and 10.

Degradation in the aluminum metallization was infrequently encountered, together with excessive porosity, as shown in Figures 11 and 12. This could have been due to the softening of the metallization during various thermal cycles and step-stress tests. Since in some devices this condition was observed to be associated with a poor passivation film, the aluminum metallization was removed with HNO_3 -2HCl from several representative specimens, after the removal of the passivation film. In Figure 10, a portion of the metallization of diode No. 9 is shown as having been removed. It is evident from the photomicrograph that both the anode and the cathode epitaxies were degraded, forming a narrow path there-between during initial processing. Consequently, the aluminum metallization had partially diffused into the path, bridging the electrode elements

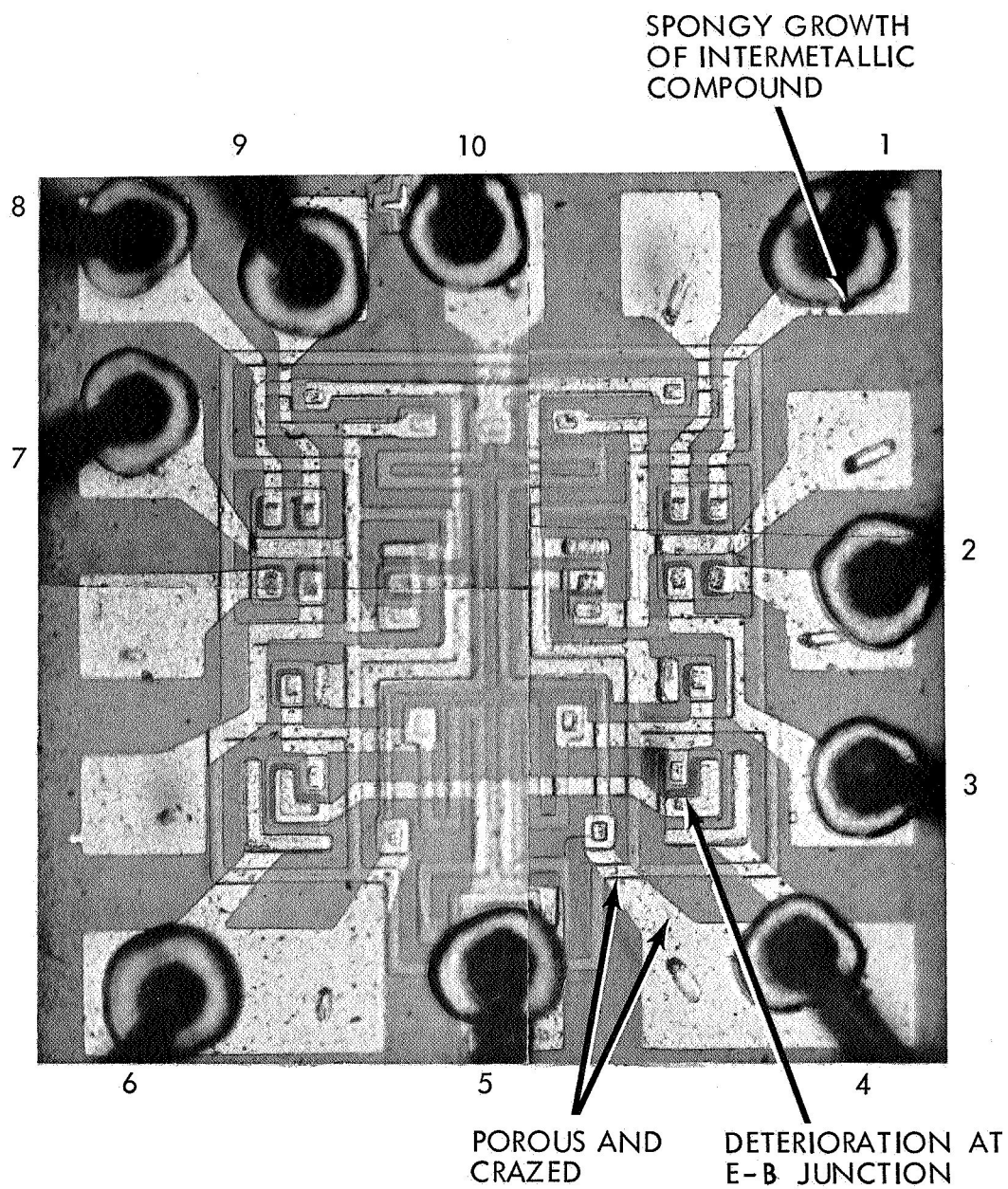


Figure 5. Macrograph Showing Areas Affected by $V_{(SAT)}$
Type Failure (Fairchild, No. 42)

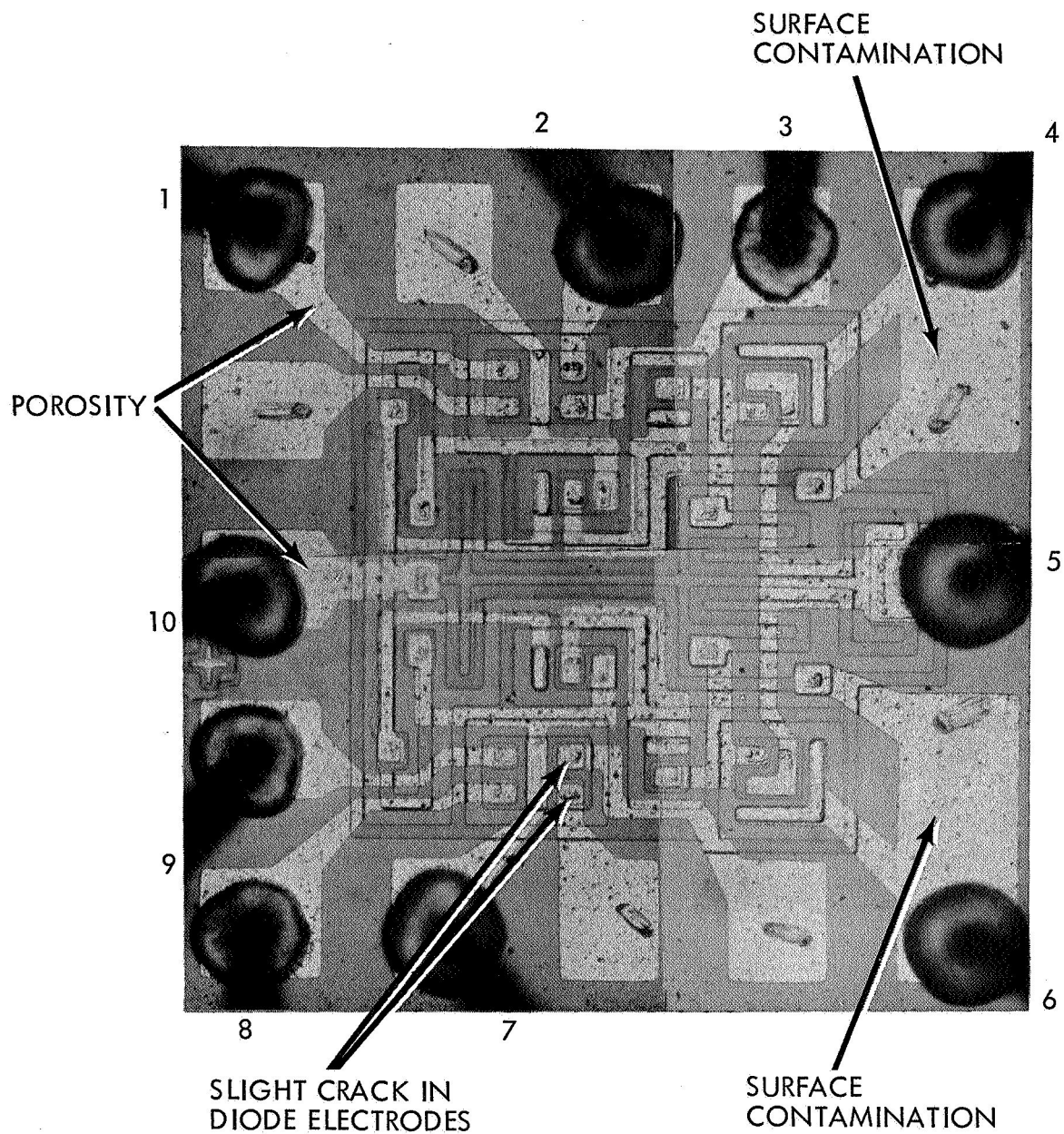


Figure 6. Fairchild Device With BV-Type Failure

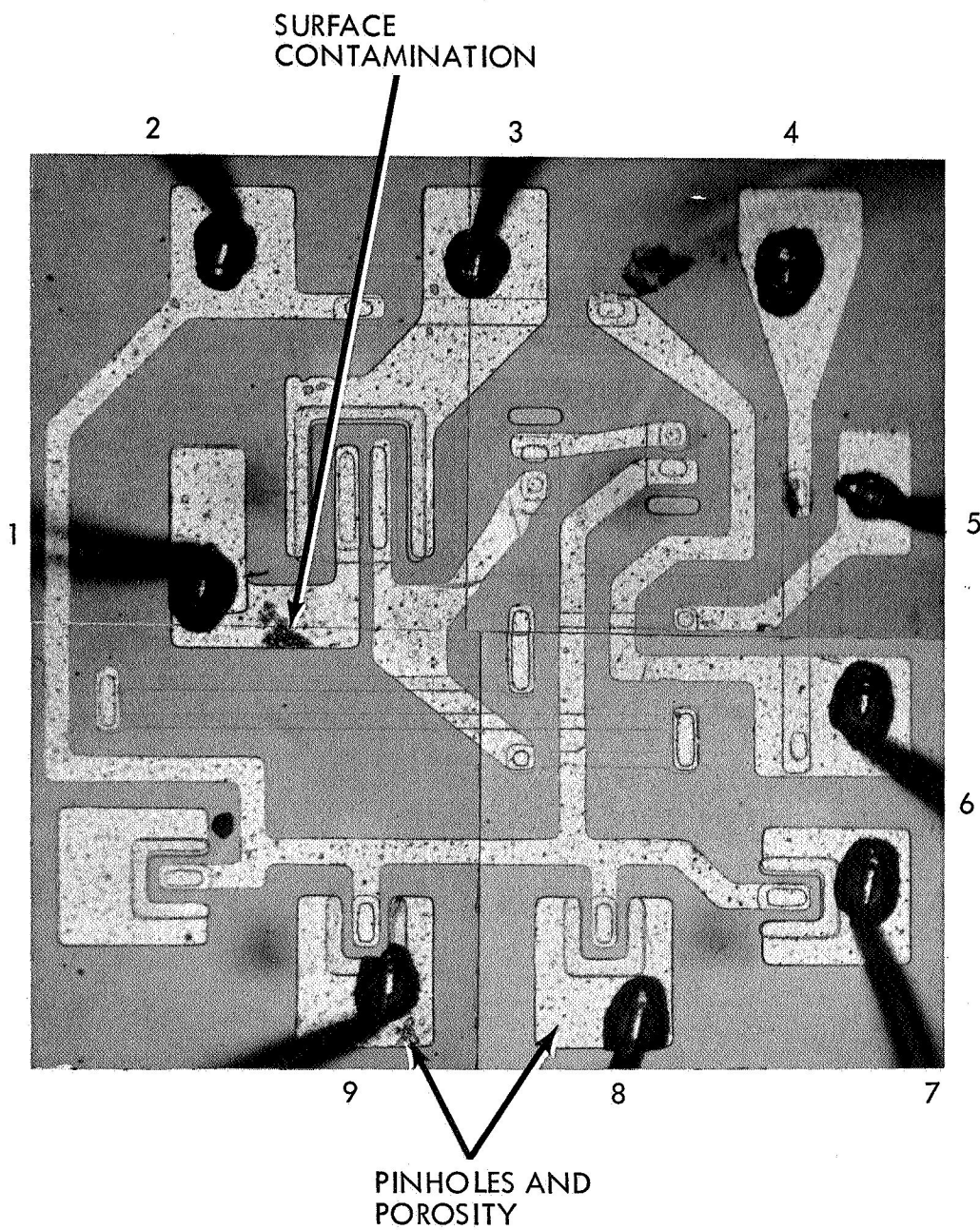


Figure 7. Motorola (Lot B) Device With BV_8 and BV_9 Failures

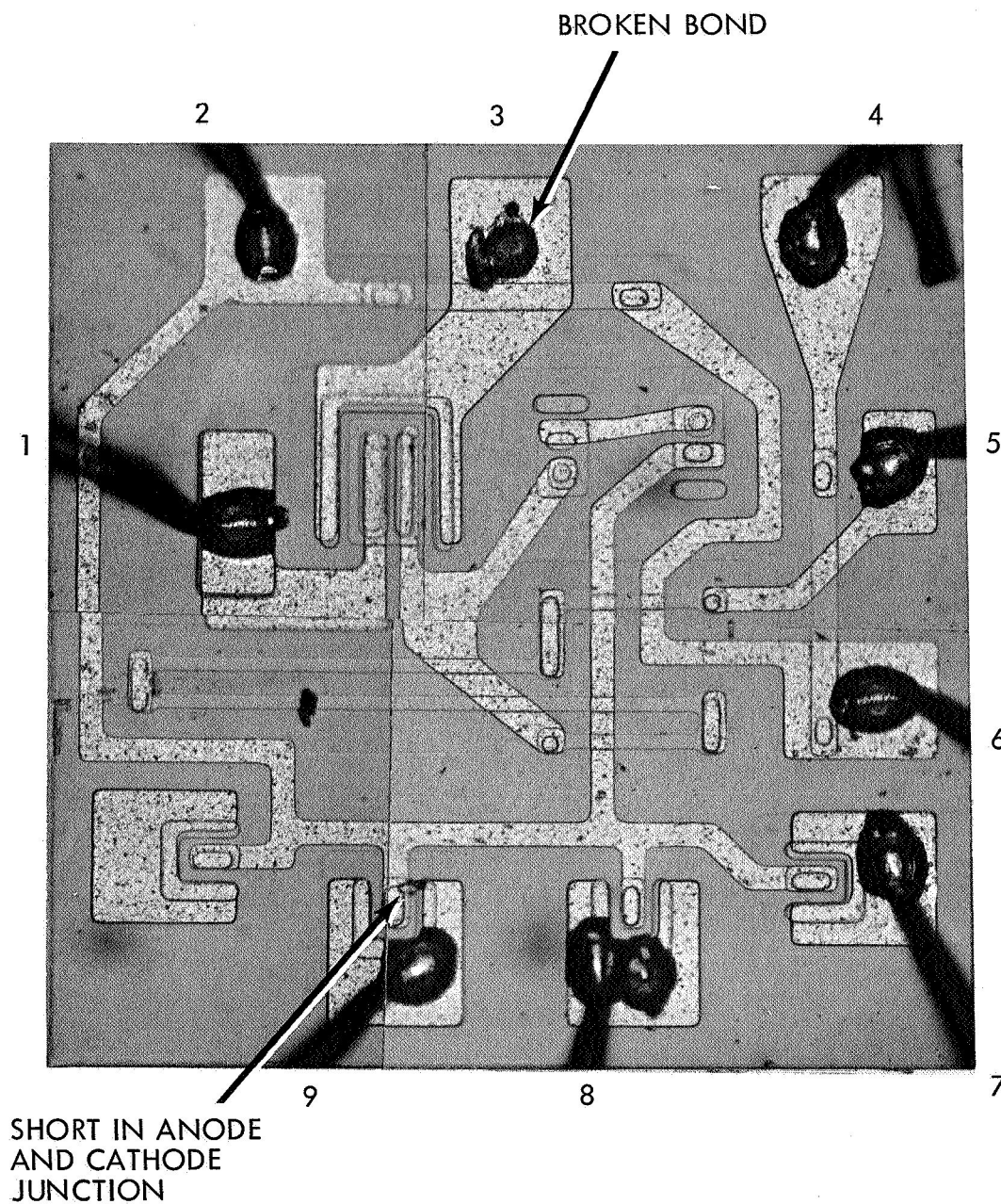


Figure 8. Motorola (Lot B) with BV-Type Failure

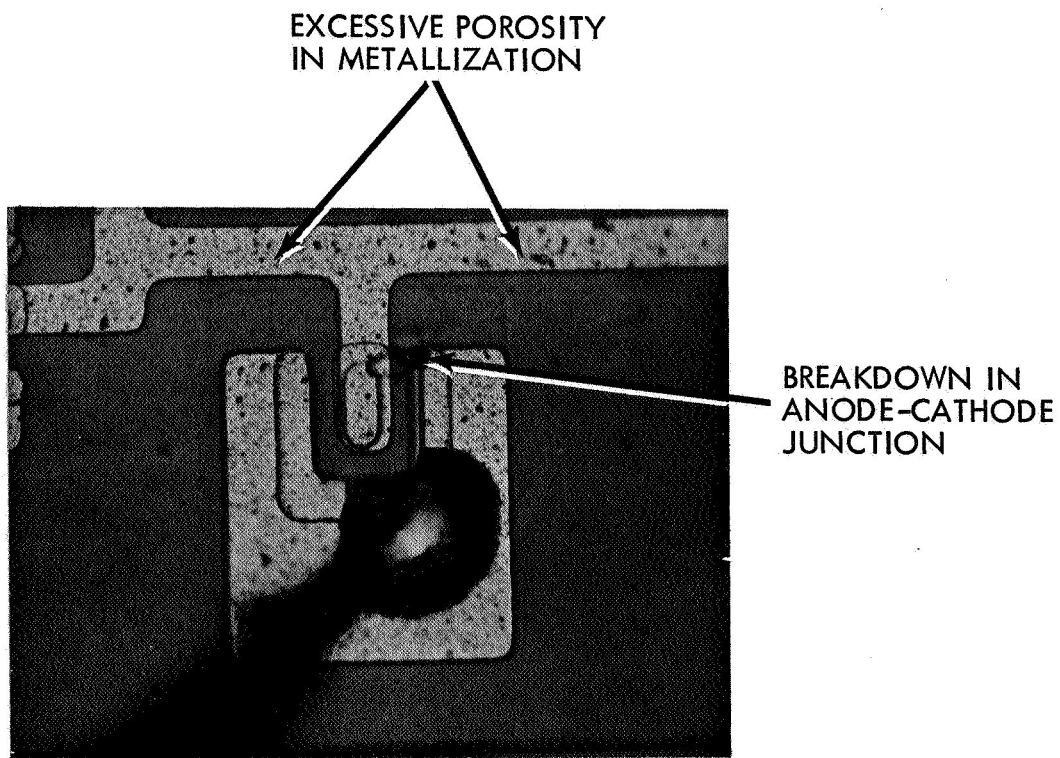


Figure 9. Shorted Diode 9 of Specimen 30

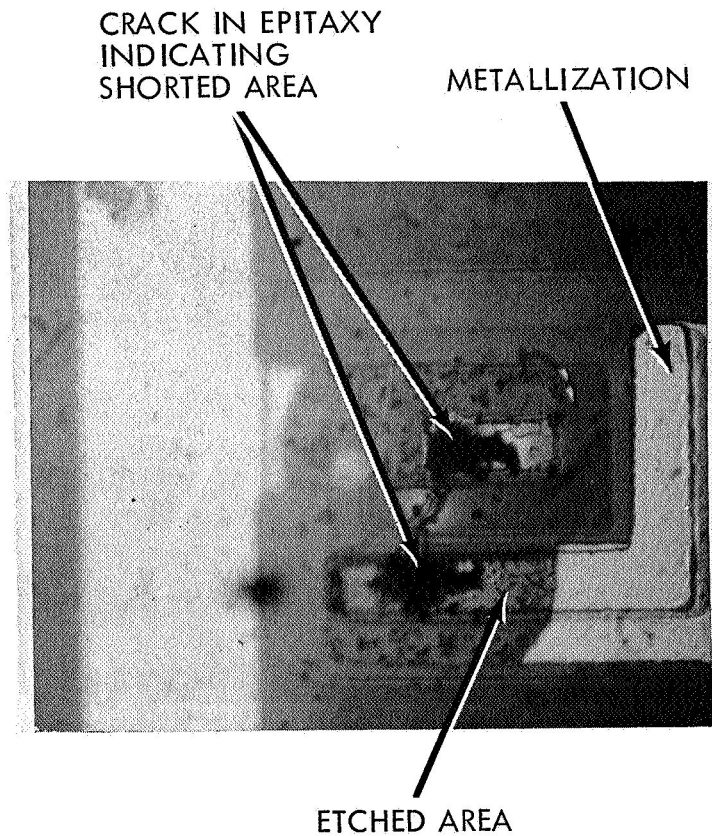


Figure 10. Diode 9 of Specimen 13 Showing the Shorted
Area Between Anode and Cathode
(Metallization Partially Removed By HNO_3 -2HCl Etch)

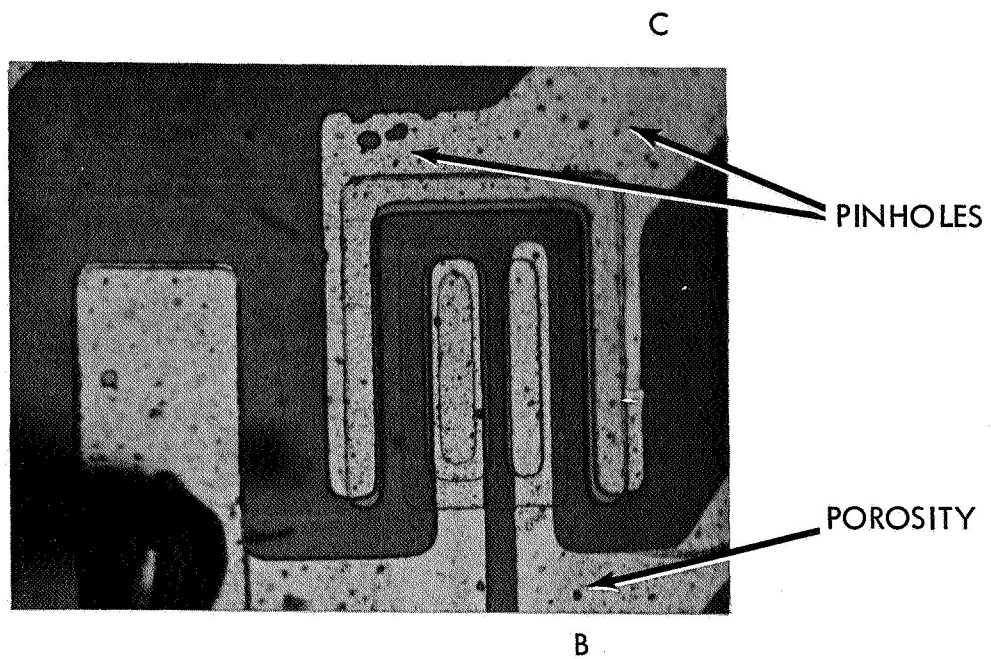


Figure 11. Output Transistor With Excessive Porosity

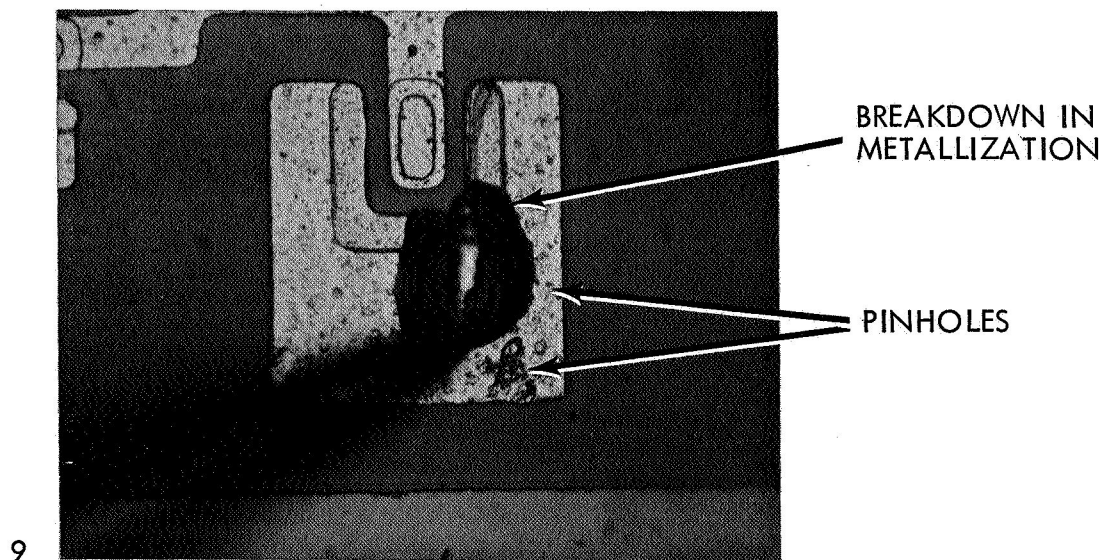


Figure 12. Diode 9 of Specimen 19 (Motorola, Lot B)

2.2.1 Experimental Procedure (Cont.)

and giving rise to a short in that region.

Open diode or transistor was characterized by the top views of the specimen shown in Figures 13 and 14; the Figure 14 is a magnified view of the open transistor with $V_{(Sat)}$ failure indicator shown in Figure 13. The transistor output voltage had increased from the initial 0.256 to 20.36 volts.

Device structural element degradation due to temperature cycling and life test, burnt and eroded areas resulting from transient voltage surges, and shorts or opens could be readily observed from the top view (Figures 6 through 14) without further cross-sectioning the device, although cross-sectional view of the device contributes valuable information not obtainable by surface examination.

Some of the failed devices were studied by treating them with concentrated HCl for definite intervals of time and finally removing the aluminum metallization completely from the die surface, as shown in Figure 15. This action permitted the observation of any defect in the pyrolytic glass dielectric in the N, N+ and P regions by change of birefringent colors. Subsequent to these observations, the dielectric film was etched in stepwise manner using a 5 percent solution of HF. It was thus possible to study the various active regions at desired depths to determine their physical characteristics as well as certain changes that may have occurred during thermal and electrical test prevailing over the tendency for degradation, inversion, or fouling of the doped regions.

2.2.2 Failure Modes Encountered

The types of failure modes encountered during the life span of this program were: open circuit, short circuit, decreased breakdown voltage, high input diode leakage current, increased output saturation voltage, collector-base leakage current, input diode forward current degradation, output transistor leakage current, input transistor leakage current, and d-c current gain. These failure modes manifested themselves in the change of failure mode indicators I_R , I_{CBO} , I_{CEX} , $V_{CE(Sat)}$, I_{CRO} , h_{FE} , BV_{CBO} , I_F , and I_T . These electrical failure indicators, in turn, identified themselves in the structural changes of the device elements, as observed metallographically in Figures 5 through 15.

The metallographic indications were: open bond, internal lead degradation, porous and degraded metallization, faulty contact deposition, contaminated pellet surface, crazed aluminum metallization, passivation film inhomogeneity, random cracks or pits in the silicon pellet, intermetallic growth at gold-aluminum bond interface, aluminum diffusion in a flaw bridging the P-N junction, and misalignment of aluminum metallization with respect to active areas in

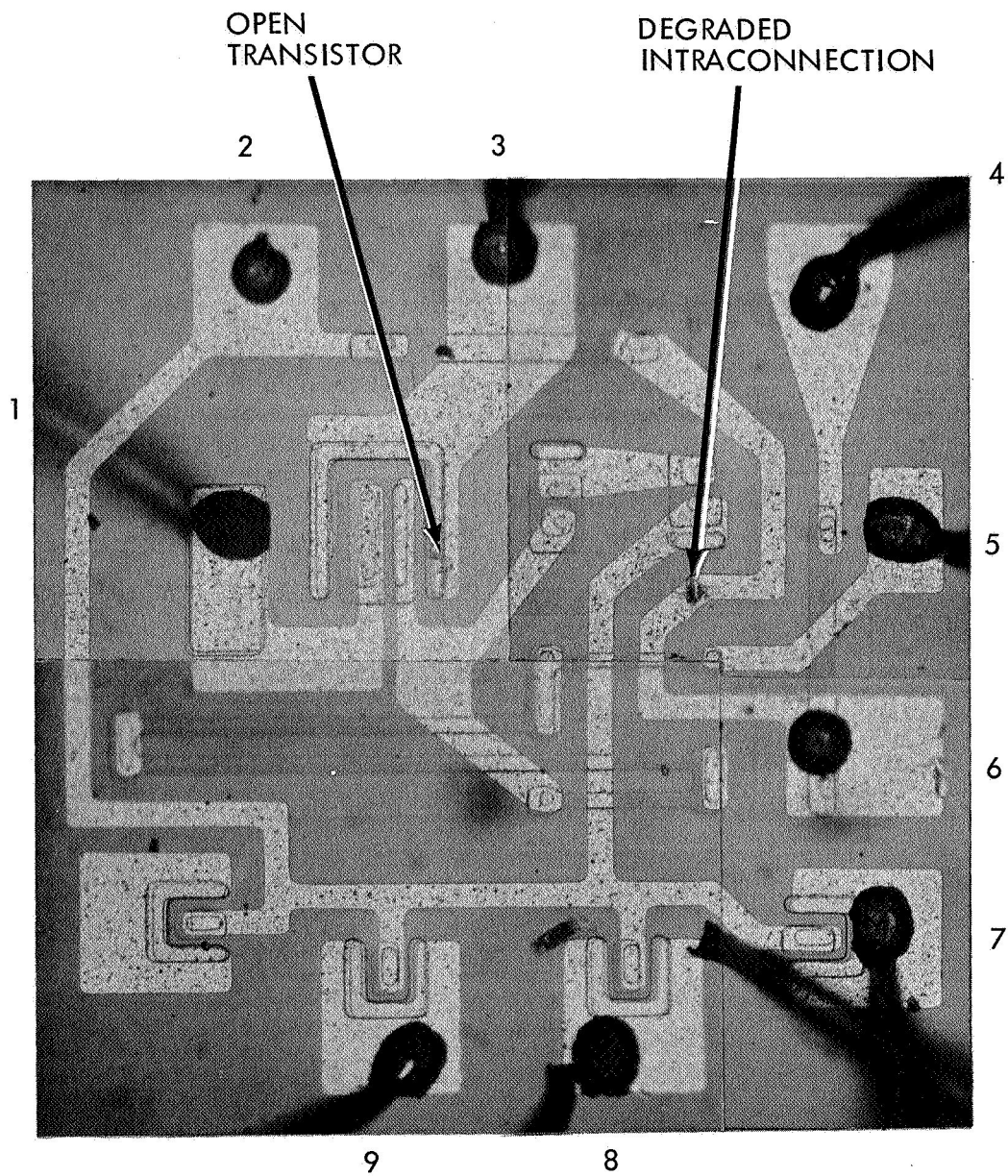


Figure 13. Motorola (Lot B) Device With V_{SAT} Failure

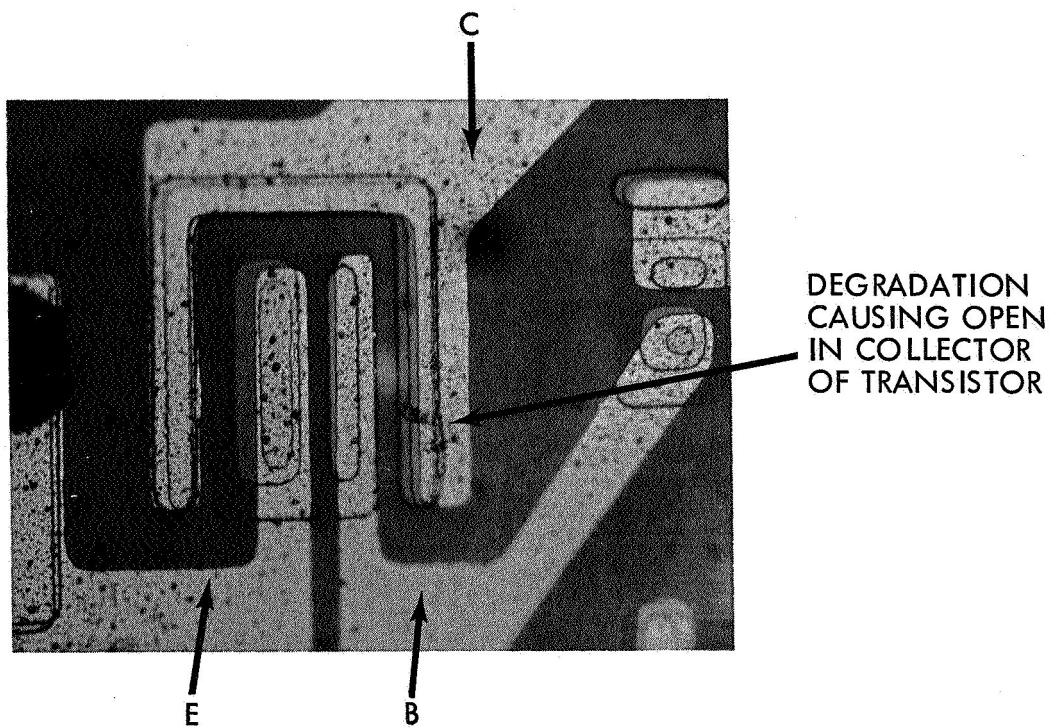
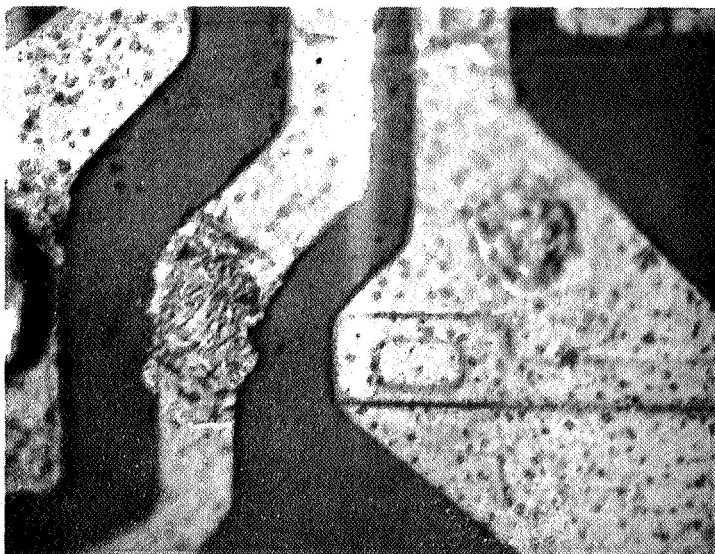
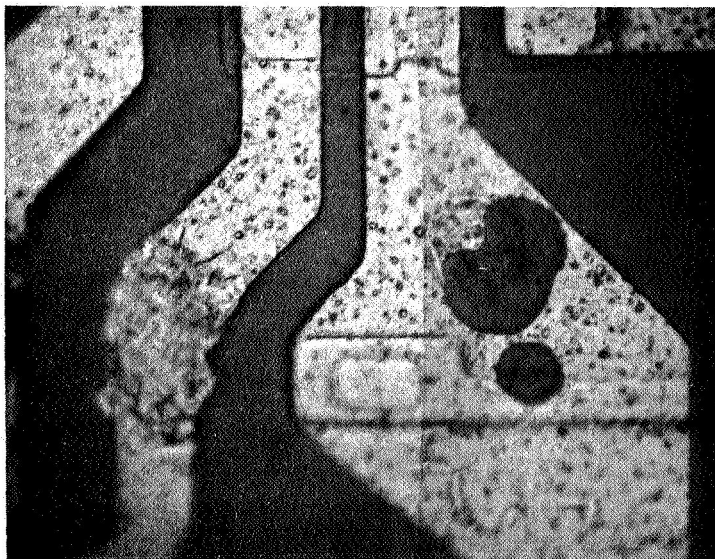


Figure 14. Output Transistor of Specimen 9 (Motorola)



(a)
BEFORE
Aluminum Removal



(b)
DURING
(1.5 minutes of hydrochloric
acid treatment)



(c)
AFTER
Aluminum Removal

Figure 15. Passivating Film of a Motorola (Lot E) Device
(Sequence of Dissolution of Aluminum Below the Glass)

2.2.2 Failure Modes Encountered (Cont.)

several specimens examined. It is thus seen that an accurate and valid correlation between the electrical failure modes (represented by the respective failure indicators) and the metallographic findings would be the principal basis in the establishment of screening criteria by the use of the minimum number of failure indicators and preferably at low cost. Future investigations in the continuing program will concentrate on this concept for the ultimate assurance of reliability of the microelectronic (semiconductor) devices.

2.2.3 Study of Failure Modes

The failure modes were studied with the view of relating their effects on the device elemental structures to the determination of the mechanisms causing the elemental failures. It was found that differences occur in elemental failures in different Vendor devices. These differences were generally due to the type of the internal lead material and its bonding characteristics, differences in metallization homogeneity, dissimilarities in passivation layers, misalignments of bonds on the pads and of metallization with respect to the active areas, general workmanship and package design, and control over the fabrication and processing requirements. Both Fairchild and Signetics were found to be inert to catastrophic failure by intermetallic formation at temperatures in the vicinity of 250°C, at which ambient the Motorola (Lot B) devices, for instance, showed increased saturation voltage (V_{Sat}), meaning the formation of Au-Al-Si at the bond interface on the die. This relation could be attributable to the possible interaction of aluminum with the dielectric passivation at this low temperature. At a higher temperature (325° to 350°C), both Fairchild and Signetics devices revealed inter-metallic formation.

In comparing the findings in the dielectric properties of Fairchild, Motorola (Lot B), and Signetics, variations existed in the oxide thicknesses between the Fairchild devices and the Motorola (Lot B) and Signetics devices, as will be noted in Table 3. Considerable differences were prevalent in the oxide thicknesses of the individual samples of Fairchild, while the Motorola (Lot B) and Signetics devices exhibited more constancy in the uniformity at the N, P, and N+ active regions. Motorola (Lot E) dielectric was similar to that of Motorola (Lot B), and both dielectrics were extremely unreactive to the effect of etching with HF.

The rate of removal of aluminum metallization varied within the individual specimens of Fairchild lot as well as with respect to the other lot devices, as indicated in Table 3. It will be observed from Table 4 that the shelf-life device exhibited high reactivity compared with other devices. During treating the Fairchild and Motorola (Lot E) aluminum-interconnection metallization with HCl it was observed that certain interconnects that had not been exposed to high current densities were less reactive with HCl. It could thus be concluded that further study of the characteristics of aluminum-metallization would be necessary.

TABLE 3
GENERAL PHYSICAL CHARACTERISTICS OF
VENDOR LOTS TESTED

Vendor Lot	Type of Package	Type of Circuit	Chip Dimensions (In Mils)	Number of Bonds	Number of Pads	Type of Bond	Conductor Density*	General Appearance of Al	Thickness of SiO ₂	Presence of Glass Passivation Layer
A	TO-5 Can	Dual Input Gate	40x40	10	14	Au-Al	2X	Uneven; only vendor in which Al exhibits the "cracked oil-painting" effect.	7200A	No
B	TO-5 Can	Single Input Gate	40x40	9	10	Au-Al	1X	Smooth and quite granular in appearance, i.e., more porous than Al in Fairchild devices	10,000 A	No
C	TO-5 Can	Single Input Gate	50x40	9	10	Au-Al	1X	Very smooth and few if any pores evident.	7200A	No
E	Flat - Pack	Dual Input Gate	40x40	14	14	Al-Al	2X	Similar to Al in Motorola (Lot B) except for presence of a passivation layer which covers the entire device except the pad regions	10,000A	Yes

*The ratio of thin-film aluminum surface area to the total surface area of the chip.

TABLE 4

SUMMARY OF THIN-FILM ALUMINUM CHARACTERISTICS

Device Number and History	Initial Appearance of Al	Relative Rate of Removal of Al*	Degree of Al-Dielectric Interaction
ASL-1 (Shelf-Life)	Uneven; appears thicker in certain areas than in others. Somewhat granular in appearance. Under high power Al appears somewhat porous and like a cracked-oil painting.	20X	Some interaction
16A, 20A (Life Test)	Similar to ASL-1	1X	Somewhat more than in ASL-1
54A (150 cycles)	Much more granular in appearance than in ASL-1. The "cracked-oil painting" effect more strongly evident.	6X	Similar to 20A
59A (150 cycles)	Similar to 54A	6X	Extensive interaction of Al with surface dielectric
66A, 85A (Hi-Temp) 350°C	"Cracked-oil painting" effect still more pronounced, Resulting in uneven Al surface.	2X	Almost no interaction visible, except for purple plague around bonds.
113A (Hi Temp) 350°C	"Cracked-oil painting" effect is manifested to a large extent. Channeling of certain Al electrodes is quite pronounced.	6X	Similar to ASL-1.
BSL-1 (Shelf-life)	Very granular in appearance, but surface is much smoother and more even than Al surface in Fairchild devices.	2X	Not to any significant degree
8B(Life Test)	Granular Appearing, similar to BSL-1	2X	None

TABLE 4 (Cont.)
SUMMARY OF THIN-FILM ALUMINUM CHARACTERISTICS

<u>Device Number and History</u>	<u>Initial Appearance of Al</u>	<u>Relative Rate of Removal of Al*</u>	<u>Degree of Al-Dielectric Interaction</u>
8B (life test)	Granular Appearing, similar to BSL-1	2X	None
CSL-1 (Shelf-Life)	Very smooth and even; relatively few "pores" in comparison to ASL-1	4X	Little if any interaction
68C, 107C (Hi Temp) 350°C	Smooth and even where it has not been eroded to form discontinuities	5X	Quite extensive interaction
ESL-1 (Shelf-Life)	Similar to Motorola Lot B except for a pinkish tint or hue (implying a clear covering layer)	Does not apply because of presence of passivation layer.	None

*The rate of removal of Al in device 16A was used as the standard rate (1X). The aluminum thicknesses are unknown. Thus rates represent the time for total removal of aluminum.

3. ANALYSIS OF TEST RESULTS

During the life tests, there were more failures in Fairchild devices than in those of any of the other three lots. Referring to Tables 5 and 6, it will be noted that there were 13 device failures from Fairchild lot, 7 from Motorola Lot B, 4 from Signetics lot, and 4 from Motorola Lot E. Failure modes experienced by all the devices were electrical shorts, degradation-caused current leakage or (I_R), increase in $V_{(Sat)}$, and decrease in breakdown voltage.

3.1 Fairchild DTL Dual Gates

Of the 13 specimens that failed from Fairchild lot, 5 specimens failed by high current leakage (I_R) during the first 5000 hour life test; 5 specimens failed due to low output transistor breakdown voltage (BV) in the 6000-hour life test; and, 2 specimens failed as a result of increased saturation voltage (V_{Sat}) in 7000- and 10,000 hour life tests, respectively, and 1 specimen failed with greatly decreased voltage breakdown (BV) in 10,000-hour life test. No other failures occurred during the life test up to the final 14,000 hours.

At the completion of 12,000-hour life test, seven specimens were removed from the test lot and subjected to a vibration test described in paragraph 2.1.3. Subsequently, the specimens were functionally tested. No failure was experienced by any of the specimens. Therefore, no post-mortem examination was performed on the devices, which were then placed back in the following 13,000-hour test.

3.2 Motorola DTL NAND/NOR Gates

Seven devices had failed during life test up to 14,000-hours. Of these, 1 specimen failed in the 7000-hour life test as a result of increased saturation voltage (V_{SAT}); 3 specimens failed (1 at 8000 and 1 at 14,000 hour) because of low output transistor breakdown voltage (BV) and a short in the input diode at pin 9; 1 specimen failed with increased $V_{(Sat)}$ and open collector at 9000-hour point; and 2 specimens failed at 12,000 hour point, one with increased $V_{(Sat)}$ and the other with high leakage current (I_R) and low output transistor breakdown voltage (BV), which further indicated a short in diode at pin 9.

Subsequent to the 12,000-hour life test, six specimens from Motorola Lot B were subjected to a vibration test described in paragraph 2.1.3. One specimen failed in the vibration test. The failure was due to increased leakage current (I_R) and low output transistor breakdown voltage (BV), indicating a short at pin 9. (See representative sample in Figure 7).

TABLE 5. SUMMARY OF FAILURES OF ALL VENDOR DEVICES

DATA POINT	DURING OPERATING LIFE TESTS										Hours
	FAIRCHILD		MOTOROLA (LOT B)		SIGNETICS		MOTOROLA (LOT E)				
	Total		Total		Total		Total				
	Samples	Failures	Samples	Failures	Samples	Failures	Samples	Failures	Samples	Failures	
100 Hours	40	0	40	0	40	0	20	0			100
250 Hours	40	0	40	0	40	0	20	1			250
500 Hours	40	0	40	0	40	0	19	0			500
1000 Hours	40	1	40	0	40	1	19	0			1000
2000 Hours	39	0	40	0	39	0	19	0			2000
3000 Hours	39	0	40	1*	39	0	19	0			3000
4000 Hours	39	2	40	0	39	0	19	0			4000
5000 Hours	37	2	40	0	39	0	19	0			5000
6000 Hours	35	5	40	1*	39	1*	19	0			6000
7000 Hours	30	1	40	1	39	0	19	0			7000
8000 Hours	29	0	39	2	39	1	19**	0			8000
9000 Hours	29	0	37	1	38	1	16	2			9000
10,000 Hours	29	2	36	0	37	1	15	1			10,000
11,000 Hours	27	0	36	0	37	0					
12,000 Hours	27***	0	34	2	37	0					
13,000 Hours	27	0	30	0	31	0					
14,000 Hours	27	0	29	1	31	0					

*Device returned to test.

**Three devices were removed after 8000-hour test and subjected to vibration tests; two failed to pass functional tests, and the third one was placed back in 10,000-hour test.

***After 12,000-hour point, seven devices were removed, vibrated, and all 27 devices were functionally tested, found good, and placed back in 13,000-hour test.

Four vibrated specimens were not put back into test.

NOTE: See Appendix B for details of individual device failures.

3.2 Motorola DTL NAND/NOR Gates (Cont.)

Two specimens, one from those that failed in functional tests after 12,000-hour life test, and the second one that failed in vibration test (described above), were uncapped and examined under a microscope at various magnifications. The specimen that was subjected to vibration revealed a disrupted bond, and porous and misaligned metallization at the pads, (Similar to that shown in Figure 8). The second specimen revealed several badly misaligned bonds on the pads; the bonds indicated partial diffusion into the respective pads and interconnection strips. The aluminum interconnection film at pin 9 was degraded; the functional tests had shown an open between the pin 5 and the pins 2, 7, 8 and 9. Although these findings (functional tests) verified the failure conditions, further studies of the cross sectional views of the device would have revealed additional relevant information.

3.3 Signetics DTL NAND/NOR Gates

Four devices failed from Signetics lot during life test. One device failed at 1000-hour point as a result of high leakage current (I_R); another failed at 6000-hour life test from a slight decrease in $V_{(Sat)}$ but was returned to test; and, the other two specimens failed by low output transistor breakdown voltage (BV) after 8000- and 10,000-hour tests, respectively. No other failures were experienced to the end of 14,000-hour life test.

At the completion of 12,000-hour life tests, six specimens were randomly selected and subjected to vibration tests. No failures occurred. No post-mortem examination was performed on Signetics specimens.

3.4 Motorola Dual NAND/NOR Gates

Motorola (Lot E) devices received only 10,000-hour life test because the test was started later than those of other Vendor lots. Four devices failed during this test period. One device failed in 250-hour life test, suffering from increased output transistor leakage current (I_{CEX}); a second specimen failed in I_{CEX_1} and I_{CEX_2} by increased leakage after 8000 hours of life test; the third specimen failed in BV_{12} by a short in pin 12, and further failed by a decrease of forward blocking voltage (V_F) during 9000-hour life test; and, the fourth specimen failed in 10,000-hour test by $V_{(Sat)_1}$ and $V_{(Sat)_2}$.

Three specimens from this lot were subjected to vibration test after the completion of 8000-hour life test. One of the three specimens failed; this specimen, together with a second specimen which showed a failure in functional tests after 9000-hour life test (mentioned above), was uncapped and metallographically examined with the following results.

3.4 Motorola Dual NAND/NOR Gates (Cont.)

The device that was subjected to vibration after 8000-hour life test and had failed in the output transistor leakage currents I_{CEX_1} and I_{CEX_2} had aluminum-to-aluminum lead connection at the metallized pads and aluminum-to-gold connection at the external lead sites (posts). At the interface of the tripple-stitched aluminum-to-gold bond at the posts, aluminum had diffused into the gold plating of the posts at the peripheries of the stitch bonds. The stitches of the several bonds were disrupted from the gold plating, indicating a degradation at the bond interface by interaction of gold and aluminum. Since the terminal second and third stitch interfaces as well as the first stitch bond interface were degraded and ruptured, the intent of the additional two terminal stitches was defeated.

In stitch bonding, the principal factor conducive to bond strength is dependent on the cross-sectional area of the first stitch. If this area is excessively reduced by pressure during stitch bonding, then the presence of the terminal two stitches would seem to serve no practical purpose, unless they are intended for support during removal of tails. The validity of this contention was well confirmed with the findings in this and the second specimen discussed below.

The second specimen had failed to pass the functional test following the 9000-hour life test. The failure was indicated in BV, with a short at diode pin 12, and by a decrease in V_F . The lid of the package (flat pack) was opened and the top view of the device was examined with a microscope. All the aluminum-to-aluminum bonds were intact; however, the terminal one or two stitch bonds at the bond sites (posts) were disrupted. Since bluish dark diffusion areas were noted surrounding the bond areas, the condition could be attributed to the formation of a brittle intermetallic at the bond interface. Randomly chipped off aluminization at the intra-connections was also visible. At random sites, the metallization was misaligned with respect to the active regions. The latter condition could cause metal diffusion into degraded epitaxy or active junction, causing a short, as incurred by the diode adjacent pin 12. (See Specimen 15, Table 4).*

4.0 COROLLARY INFORMATION

4.1 Failure Cause and Effect

Recapitulating the preceding studies and findings from the different manufacturer's devices, it can be asserted that a principal similarity of the various devices resided in the types of failures arising from ineffective process controls over the fabrication and packaging operations. These findings generally indicated that the majority of the failures were due to poor metallization, with misaligned bonds and associated contacts with the active areas of the device trailing the principal discrepancy. Metal-to-metal diffusion and metal-to-semiconductor

*Appendix B

4.0 COROLLARY INFORMATION (Cont.)

4.1 Failure Cause and Effect (Cont.)

diffusion were also prominent in causing failures, especially at elevated temperatures such as those encountered in this program. Random occurrences of flaws in the pyrolytic passivation film and microcracks in the epitaxy of the device also played, although not often serious, dominant part in producing electrical parameter failures. In the earlier part of the investigation, failure was also contributed to the incomplete removal of the photoresist from the dielectric windows of the die.

As will be noted from the preceding discussions, the Fairchild devices had the greatest number of failures, namely 13; 6 failures were by breakdown voltage (BV), 5 in leakage current (I_R), and 2 in saturation voltage (V_{SAT}). Motorola Lot B had 7 failures: 3 in (V_{SAT}), 3 in (BV), and 1 in (I_L) or (I_R). Signetics lot had 2 breakdown voltage discrepancies (BV), and 1 increased reverse current leakage (I_R). Motorola Lot E experienced 2 failures by leakage current (I_L or I_{CEX}), 1 failure by BV and V_F , and 1 failure by $V_{(Sat)}$. It is thus seen that the failures encountered in this program can be reduced to three basic failure mode indicators, i.e., BV, I_R , and $V_{(Sat)}$. These include the more definitive failure indicators BV_R , BV_{CBO} , BV_{CEO} , $V_{CE(Sat)}$, I_R or I_{CEX} , I_{CBO} and I_{CEO} . When the device was uncapped and the collector metallization was opened, then I_{BEO} could be measured, and from this and I_{CEO} , the value of h_{FE} could be extrapolated.

In terms of device elemental discrepancies, these failure mode indicators would be conducive to the characterization of the failure cause in the device structure. For instance, referring to the 6th Quarterly Report (February 1967), the specimen No. 19 of Motorola Lot B indicated, during functional tests, that decreases in the breakdown voltages (BV) were incurred by the diodes 8 and 9, (Figure 7). The devices were uncapped and examined metallographically. The examination revealed surface contamination and pinholes in the aluminum metallization of diode 8, and badly misaligned bond and pinholes in excess were present on the cathode metallization of diode 9. In another case, specimen No. 42 of Fairchild device, shown in Figure 5, had failed in V_{SAT} and BV after 10,000-hour life test.

Metallographic examination of the top view of the device circuit revealed a slight intermetallic growth at the bond interface (V_{SAT}), and crazed aluminization and slight deterioration of the emitter-base junction of transistor at pin 4 verified the failure condition BV. These examples can be extended to many other failure modes and their respective metallographic verifications. Consequently, it can be asserted that definite correlation between electrical failure mode indicators and microscopic

4.1 Failure Cause and Effect (Cont.)

findings of the device circuit elements could be made, as presented with illustrations in paragraph 2.2 of this report.

4.2 Comparison of Vendor Lot Failures

A comparison of the four vendor lot failures encountered in the study program is given in Table 6. This table presents a qualitative analysis as characterized by the device failures during the operating life test.

Table 6. Comparison of Vendor Lot Failures

VENDOR	DISCREPANCY	NUMBER OF DISCREPANCIES
A	BV	6
	I_R	5
	V_{Sat}	2
B	V_{Sat}	3
	BV	3
	I_R	1
C	BV	2
	I_R	1
E	I_R	2
	BV	1
	V_{Sat}	1

It will be noted that the greatest number of failures in BV were incurred by Fairchild lot and the smallest by Signetics lot; these failures indicate the need for elimination of oxide contamination, inter-junction metallic diffusion, surface charge, microcrack, and misalignment of bonds, by use of adequate process controls. Increased leakage current (I_R) also occurred most frequently in Fairchild devices and least frequently in Motorola lots B and E; this condition could be caused by any one or more of the following discrepancies: poor lead bond placement, hermetic seal failure, contamination within the silicon pellet, crack in silicon die, gold sintered into P-N junction, fusion of electrical paths, etc. The discrepancy V_{SAT} occurred in Fairchild lot and Motorola Lots B and E: two in Fairchild lot and three in Motorola lots, which latter vendor reduced the occurrence of V_{SAT} in Motorola Lot E by use of aluminum-to-aluminum bonds at the metallization pads; however, there occurred one $V_{(Sat)}$ condition at a gold-plated post. No significant effect of V_{Sat} was noted in Signetics lot. The discrepancy V_{Sat} is indication

4.2 Comparison of Vendor Lot Failures (Cont.)

of crack in PN junction, Au-Al-Si complex growth at bond interface, emitter and base softening, back contact degradation, spike, etc.

It is apparent from Table 6 that the Signetics devices had the fewest failures among the gold-to-aluminum-pad bonded vendor lots. Motorola Lot E had the next fewest failures next to those of Signetics, but the Motorola Lot E had undergone only 10,000 hours of life test as versus 14,000 hours of life test undergone by the other lot devices, including Signetics devices. Thus, Signetics devices may be considered superior to the other vendor devices tested.

4.3 Development of a Needed Screening Test

From the findings of this test program and instigated by the trend of high incidence of semiconductor failure of devices during use, it is immediately apparent that the development of an effective device screening method is an urgent prerequisite to the procurement of semiconductor microcircuits for use on critical aerospace systems and associated equipment. Determination of reliability indicating parameters and the sequence of tests necessary for obtaining such parametric data must be accomplished. The vast amount of qualitative data obtained in the already completed test program suggest that an effective device screening test method would be one which focuses consideration on the minimum number of failure mode indicators capable of providing the necessary reliability information at low cost.

It has been already pointed out that drastic measures would be required on the part of the manufacturer in the control of fabrication techniques, process methods, and general workmanship of the device. Transcending these controls, the requirement for the training of technicians and operators engaged in the bonding and packaging of the devices would seem a most important supplier responsibility. In this connection, the electrical parameters chosen should be in accord with the conventional inspection facility available at the procuring agency. The extended program of physics of failure analysis then should be predicated on a carefully planned, organized, and executed test program that has a primary consideration for the reliable inspection and screening of microcircuits with equipment of relatively routine applications. Complementing the establishment of checking and screening methods, applicable specifications prescribing the test procedures to be implemented would be a part of the test program.

5.0 CONCLUSIONS

5.1 The findings in the life test indicate that the Fairchild and Motorola (Lot B) devices require more stringent process control over the metallization process than those of Signetics and Motorola (Lot E).

5.2 Misaligned lead bonds on pads and associated contact regions and paths are due to initial process deficiencies.

5.3 Partial diffusion of the gold bond into the pad area and contiguous metallization had resulted from misaligned and overlapping bond conditions.

5.4 Passivation film in some of the specimens was nonuniform and pitted in regions that could cause current leakage to undesired points.

5.5 Infrequently seen cracked condition in the P-N junction could be attributable to the inadequate lead bonding process technique.

5.6 Contaminated pellet surface noted could be eliminated by proper cleaning of the die before bonding and by eliminating contaminants through control of package seal integrity.

5.7 The presence of Au-Al intermetallic growth at the gold-aluminum bond interface in all except Signetics specimens suggests that this discrepancy could be controlled by adequate bonding temperature, pressure, and time at the time of fabrication of the device.

5.8 Ionic migration from one doped region to another in the die was determined to be due to the degraded silicon dioxide isolation and the silicon underneath.

6.0 RECOMMENDATIONS

6.1 Further and intensified effort is recommended toward conducting of a systematic and properly sequenced environmental and stress tests, using one type of a selected microcircuit that is typical of a device for the intended system application.

6.2 The post-mortem investigation should be emphasized on all catastrophically failed specimens as well as on representative control samples.

6.3 From the investigation to be carried out in the extended physics of failure program, a valid, rapid, and effective microcircuit screening technique should be evolved which will enable the inspection activity to weed out defective devices prior to their installation in systems.

6.4 The screening tests should be arranged in a sequential order so that the effect of a previous test should not reflect in the failure of the device in the succeeding test.

6.5 The testing effort should be directed toward reducing the number of electrical parameter failure indicators to a minimum and to include only the reliability-indicating parameters, which should be identified during the extended testing program.

6.6 The work in the new program to be started should be concentrated on the evaluation and defining of the already suggested three basic failure indicators, namely, I_R , BV, and V_{Sat} as the reliability-indicating parameter aids in the establishment of the projected goal of device screening.

6.7 Factual data should be obtained through environmental and thermal stress tests to be conducted to verify the effectiveness of the screening techniques derived from the investigation.

6.8 On the basis of the operating life test effort supplemented by applicable data from the previous tests, Signetics devices appear to be superior for applications at elevated temperature conditions; however, this statement should be taken with some reservation for the fact that it relies upon the comparative findings from a limited course of physics of failure effort.

6.9 It appears that the interaction of aluminum with silicon dioxide presents a problem which cannot be overlooked. Further studies are necessary to determine the underlying cause, especially under environmental conditions.

6.10 Some effort should also be devoted to the possible establishment of criteria for determining external workmanship quality in relation to device performance and service life.

APPENDIX A

Correlation of Failure Modes with Probable Production Faults

APPENDIX A

RELATION OF FAILURE MODE TO PROBABLE PRODUCTION FAULT

Device Number	History of Device	Type of Electronic Failure Reported	Visible Defects Seen	
			In Al	In Dielectric
16A*	5000 hours operating life	I ₃ leakage current increased (from 16.2 na to 27000 na); degradation of the input diode leakage current (lead No. 3).	None	Scratch in Silicon, near input diode of pin No. 3. Char near window of resistor, R1.
20A	6000 hours operating life	Short at input diode 9. BV ₉ decreased from 5.657 to 0.182V.	None	None
54A	Post 150 cycles (-65°C to +125°C)	Increase in Vsat ₄ : 67% (from 0.210V to 0.351V). Increase in Vsat ₆ : 22% (from 0.210V to 0.256V).	None	None
59A	Post 150 cycles (-65°C to +125°C)	Vsat ₄ increased 70% (from 0.270V to 0.459V) Vsat ₆ increased 22% (from 0.270V to 0.329V)	None	Superficial scratch in Al electrode that leads to emitter of transistor of pin No. 6.
66A	Post 350°C	Vsat ₄ increased 27% (from 0.223V to 0.283V)	None	Scratch in dielectric across portion of transistor region of pin No. 4.
		Vsat ₆ increased 18% (from 0.223V to 0.263V)	Al exhibits a black spot. Looks like a burn out. This Al is in contact with the window to the base of the transistor of pin No. 4.	None
			Purple plague around bonds.	None
			Superficial scratch.	None

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*Letter stands for Vendor Lot type.

APPENDIX A

Device Number	History of Device	Type of Electronic Failure Reported	Visible Defects Seen	
			In Al	In Dielectric
85A	Post 350°C	Catastrophic failure on V_{sat} measurement.	None, except for the purple plague around the bonds.	None
113A	Post 350°C	BV_9 open circuit at 340°C.		Deep cavity in silicon where pin No. 9 had once been bonded.
		R_1 and R_2 open.		Black char residue (deposit) strongly adhering to silicon in resistor region of R_1 and R_2 .
		Severe degradation of input leakage current.	Purple plague	An apparent short across the dielectric between diode of pin No. 3 and expander.
8B	7000 hour operating life	Output transistor saturation voltage increased 8x (from 0.239V to 1.87V).	None	A depression in the dielectric covering region of a transistor whose collector was shorted thus transforming it into a diode.
68C	Post 350°C	Output transistor open (open indicated on the V_{sat_3} measurement).	Extensive discontinuities in the Al, around perimeter of purple plague.	Cavitation down into silicon near window to which Al electrode of pin No. 5 leads.
107C	Post 350°C	Same as in 68C.	Extensive discontinuities in the Al around perimeter of purple plague.	None
51E	Post 200°C	BV_{13} indicates a shorted diode.	Misalignment of aluminum and diode diffusion mask in devices of Vendor E.	A short across the dielectric is seen as a charred streak between expander and diode of pin No. 13.
	Post 250°C	BV_1 indicates a shorted diode.	Some minor imperfections are visible in several interconnections.	Similar to short above but seen between expander and diode of pin No. 1.

APPENDIX A

Device Number	History of Device	Type of Electronic Failure Reported	Visible Defects Seen	
			In Al	In Dielectric
58E	Post 200°C	BV ₁₂ indicates a shorted diode.		Similar to shorts in 51E, but between expander and diode of pin No. 12.
49E	Post 250°C	BV ₁₂ indicates a shorted diode		Similar to 51E but between expander and diode of pin No. 2.
	Post 325°C	Input diode leakage current It ₁ increased three orders of magnitude (from 2.96 na to 1440 na).		None
		It ₂ increased two orders of magnitude (from 3.97 na to 216.9 na). About 20x.		
			A few superficial scratches in the Al.	
50E	Post 325°C	Input diode leakage current It ₁ increased two orders of magnitude (from 3.87 na to 429.7 na).		None
		It ₂ increased from 8.48 na to 197.0 na).		None
		Output transistor threshold voltage, thres 2, increased from .1336V to .1885V for 41% increase.		None
54E	Post 325°C	Catastrophic failure on threshold and leakage current.		None
64E	Post 325°C	Both input diode leakage currents increased two orders of magnitude It ₁ : (from 3.50 na to 437.9 na).		Looks very similar to the shorts visible in 51E and 58E.
				None

APPENDIX A

Device Number	History of Device	Type of Electronic Failure Reported	Visible Defects Seen	
			In Al	In Dielectric
64E (Cont).		It ₂ (from 4.39 na to 135.9 na)		None
		Threshold voltage was a catastrophic Failure.		None
		Both input diode leakage currents increased two orders of magnitude, It ₁ from 2.77 na to 282.6 na;		None
69E	Post 325°C	It ₂ from 1.52 na to 346.9 na		None
		Threshold voltage (thres 1) increased to 0.1751 volts for an increase of 12%.		None

APPENDIX B

Summary of Specimen Failures During Life Tests

APPENDIX B

TABLE 1. SUMMARY OF FAILURES OF FAIRCHILD DEVICES
LIFE TEST

DATA POINT	Total Number of Samples	Number of Failures	Device Number	Remarks
1000 Hour Life	40	1	43	I _g increased from 157.0 na to 2.19 ua.
4000 Hour Life	39	2	21	I ₃ increased from 11.00 na to 61.96 ma.
			27	I ₃ increased from 13.20 na to 15.94 ua.
5000 Hour Life	37	2	9	I ₂ increased from 29.10 na to 434.4 na.
			16	I ₃ leakage increased from 16.2 na to 27.00 ua.
6000 Hour Life	35	5	20	BV ₉ decreased from 5.657 volts to .182 volt.
			22	BV ₉ decreased from 5.649 to 2.786 volts.
			30	BV ₈ decreased from 5.416 volts to .002 volt. I _g reading of .5764 ma.
			38	BV ₉ decreased from 5.737 volts to 2.200 volts. V _{SAT} increased 69%.
			39	BV ₉ decreased from 5.830 volts to 3.388 volts.

APPENDIX B

TABLE 1. SUMMARY OF FAILURES OF FAIRCHILD DEVICES
LIFE TEST (Cont'd.)

DATA POINT	Total Number of Samples	Number of Failures	Device Number	Remarks
7000 Hour Life	30	1	-	V _{SAT} increased from .255 volt to .376 volt (47%).
8000 Hour Life	29	0	-	
9000 Hour Life	29	0	-	
10,000 Hour Life	27	2	42	V _{SAT} (V ₆) increased from .305 volt to 1.08 volts. Slight intermetallic compound growth at bond interface; metallization is porous and crazed.
11,000 Hour Life	27	0	45	BV ₉ decreased from 5.85 volts to .451 volt. Small crack in die; indicates contact degradation with resultant discontinuity effect.
12,000 Hour Life	27	0	-	Seven specimens were removed from test for vibration testing. See Page 4, 7th Quarterly Report, 1 June 1967.
13,000 Hour Life	27	0	-	
14,000 Hour Life	27	0	-	

APPENDIX B

TABLE 2. SUMMARY OF FAILURES OF MOTOROLA LOT B

LIFE TESTS

DATA POINT	Total Number of Samples	Number of Failures	Device Number	Remarks
3000 Hour Life	40	1	19	I ₃ increased from 4.80 na to 492.6 na. Device annealed and returned to test.
6000 Hour Life	40	1	30	BV ₉ decreased from 31.30 volts to 13.59 volts. No failure analysis per- formed. Device returned to test.
7000 Hour Life	40	1	8	VSA _T increased from .239 volt to 1.87 volts.
8000 Hour Life	39	2	19	BV ₈ decreased from 27.10 volts to 16.24 volts; surface contamination; pinholes in metallization.
				BV ₉ decreased from 28.30 volts to 15.24 volts; transistor emitter lead degraded; breakdown in diode No. 9.
			30	BV ₉ decreased from 31.30 volts to 14.19 volts; bond broken at transistor collector; diode No. 9 shorted.

APPENDIX B

TABLE 2 SUMMARY OF FAILURES OF MOTOROLA LOT B
LIFE TESTS (Cont'd.)

DATA POINT	Total Number of Samples	Number of Failures	Device Number	Remarks
9000 Hour Life	37	1	9	V _{SAT} increased from .256 volt to 20.36 volts; collector was found to be open.
10,000 Hour Life	36	0	-	
11,000 Hour Life	36	0	-	
12,000 Hour Life	36	0	-	Six specimens were removed from test for vibration testing.
	34	2	28	Leakage current increased from 6.9 na to 64 na, after vibration test following 12,000-hour life test.
				BV ₉ decreased from 30 volts to 0.282 volt, indicating a short at pin 9.
			32	V _(sat) increased from 0.25 volt to 8.7 volts.
13,000 Hour Life	30	0	-	
14,000 Hour	29		10	VB decreased from 29.9 volts to 5.3 volts. I _T increased from 6.4 mA to 41 mA.

*Four of the vibrated specimens were not returned to test.

APPENDIX B

TABLE 3. SUMMARY OF FAILURES OF SIGNETICS DEVICES LIFE TESTS

DATA POINT	Total Number of Samples	Number of Failures	Device Number	Remarks
1000 Hour Life	40	1	31	I ₇ increased from 2.7 na to 109.5 ua.
6000 Hour Life	39	1	24	V _{SAT} decreased from .265 volt to .2354 volt. Device returned to test.
7000 Hour Life	39	0	-	
8000 Hour Life	39	1	43	BV ₇ decreased from 18.80 volts to .720 volt.
9000 Hour Life	38	0	-	
10,000 Hour Life	38	1	13	BV ₉ decreased from 19.10 volts to .195 volt.
11,000 Hour Life	37	0	-	
12,000 Hour Life	37	0	-	Six specimens were removed from test for vibration testing. No failures occurred.
13,000 Hour Life	31	0	-	
14,000 Hour Life	31	0	-	

APPENDIX B

TABLE 4. SUMMARY OF FAILURES OF MOTOROLA LOT E
LIFE TESTS

DATA POINT	Total Number of Samples	Number of Failures	Device Number	Remarks
250 Hour Life	20	1	24	Output transistor leakage current increased from 750-800 na to 2 ma.
500 Hour Life	19	0		
1000 Hour Life	19	0		
2000 Hour Life	19	0		
3000 Hour Life	19	0		
4000 Hour Life	19	0		
5000 Hour Life	19	0		
6000 Hour Life	19	0		
7000 Hour Life	19	0		
8000 Hour Life	19	1	21	Three specimens were removed from test for vibration testing, after 8000-hour life test after vibration. Specimen 21 failed functional tests; I_{CEX} and I_{CEX2} increased excessively.
9000 Hour Life	16	1	15	BV_{12} was shorted (pin 12); V_F decreased from initial 0.69% volt to 0.150 volt.
10,000 Hour Life	15	1	7	V_{Sat1} increased from 0.12 volt to 21 volts. V_{Sat2} increased from 0.12 volt to 21 volts.

APPENDIX C

Basic Circuits Used In Microcircuit Testing

APPENDIX C

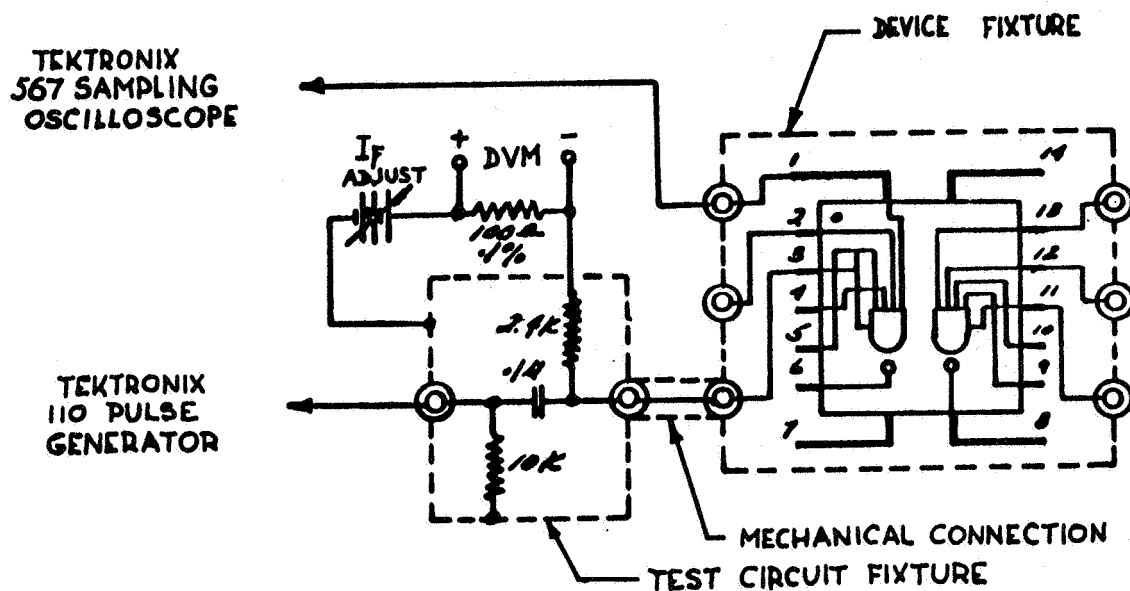


FIGURE 1. Basic Reverse Recovery Time Test Setup

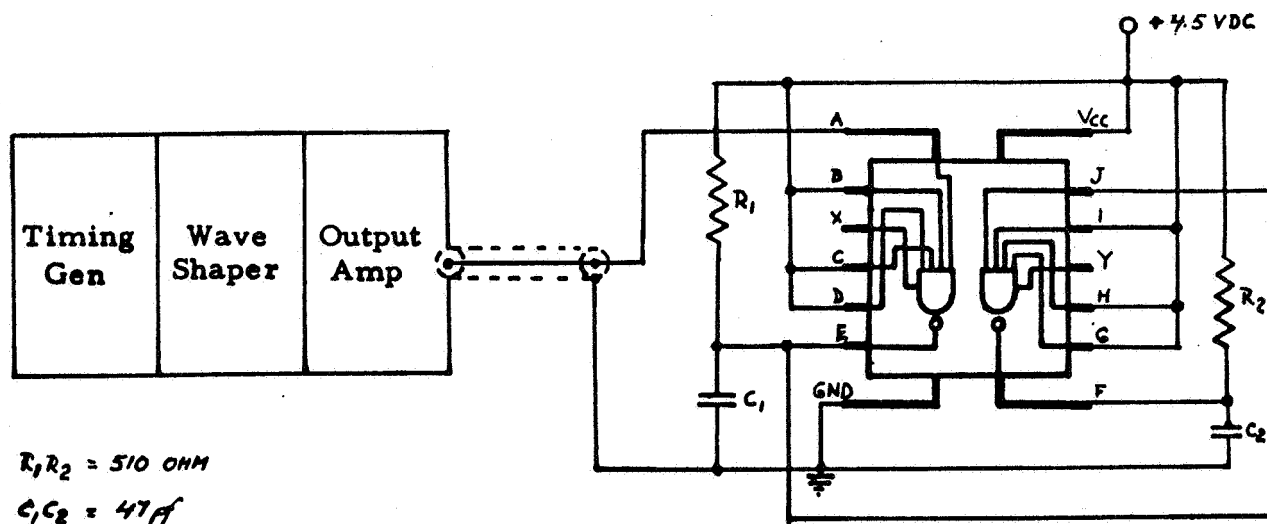


FIGURE 2. Basic Operating Life Test

APPENDIX C

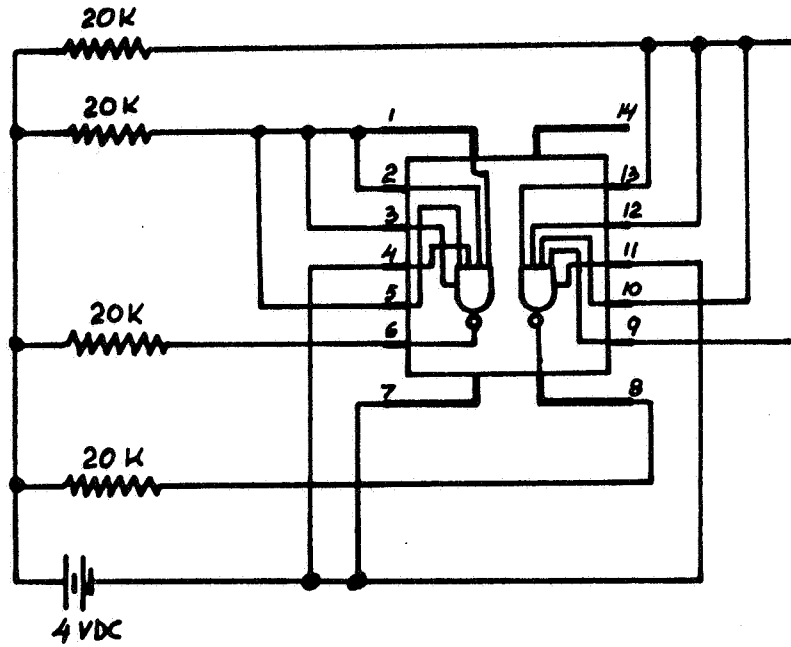


FIGURE 3. Reverse Bias Connections for Temperature Cycle

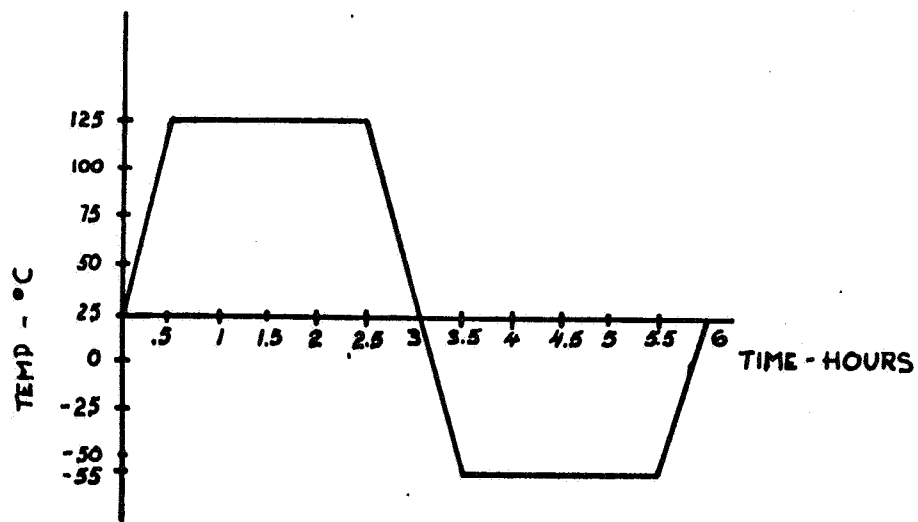


FIGURE 4. One Cycle of Temperature Cycle