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NASCOM ON-LINE DATA-SWITCHING SYSTEM

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GODDARD SPACE FLIGHT CENTER
Greenbelt, Maryland

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ABSTRACT

This document describes NASCOM high-speed data switching from an integrated hardware-software standpoint in general with emphasis on software structuring, reliability, and error control.

CONTENTS

ILLUSTRATIONS

NASCOM ON-LINE

DATA-SWITCHING SYSTEM

INTRODUCTION

The National Aeronautics and Space Administration Communications Network (NASCOM) is a worldwide voice, data, and teletype facility which supports NASA's space flight projects and missions. These missions have progressed from comparatively simple satellites to complex manned and unmanned spacecraft requiring real-time monitoring and control of the spacecraft from centralized mission and project control centers. The complexity and size of NASCOM has increased correspondingly. As a result, the network is now one of the world's largest real-time communications systems, interconnecting 90 major tracking stations, project and mission control centers, and launch facilities with over 800,000 circuit miles.

This document reviews the approach used in the design of an Automatic Data-Switching System (ADSS) and the results of the design effort. This section describes the present teletype message-switching system and the expanded requirements placed on the network for support of future missions. The remaining sections describe the hardware and software of the ADSS.

The network is configured with all overseas circuits and a majority of the U.S. circuits concentrated at the primary switching center at the Goddard Space Flight Center (GSFC), Greenbelt, Maryland. Overseas switching centers are located at London, England; Honolulu, Hawaii; and Canberra, Australia; with new centers under construction at Guam and Madrid. The first three figures illustrate the present NASCOM transmission network. Figure 1 shows the American sector of the network with trunks concentrated at the primary switching center at GSFC. Figure 2 shows the Western sector with switching centers located in Honolulu and Canberra. Figure 3 the Eastern sector with switching centers at London and Madrid.

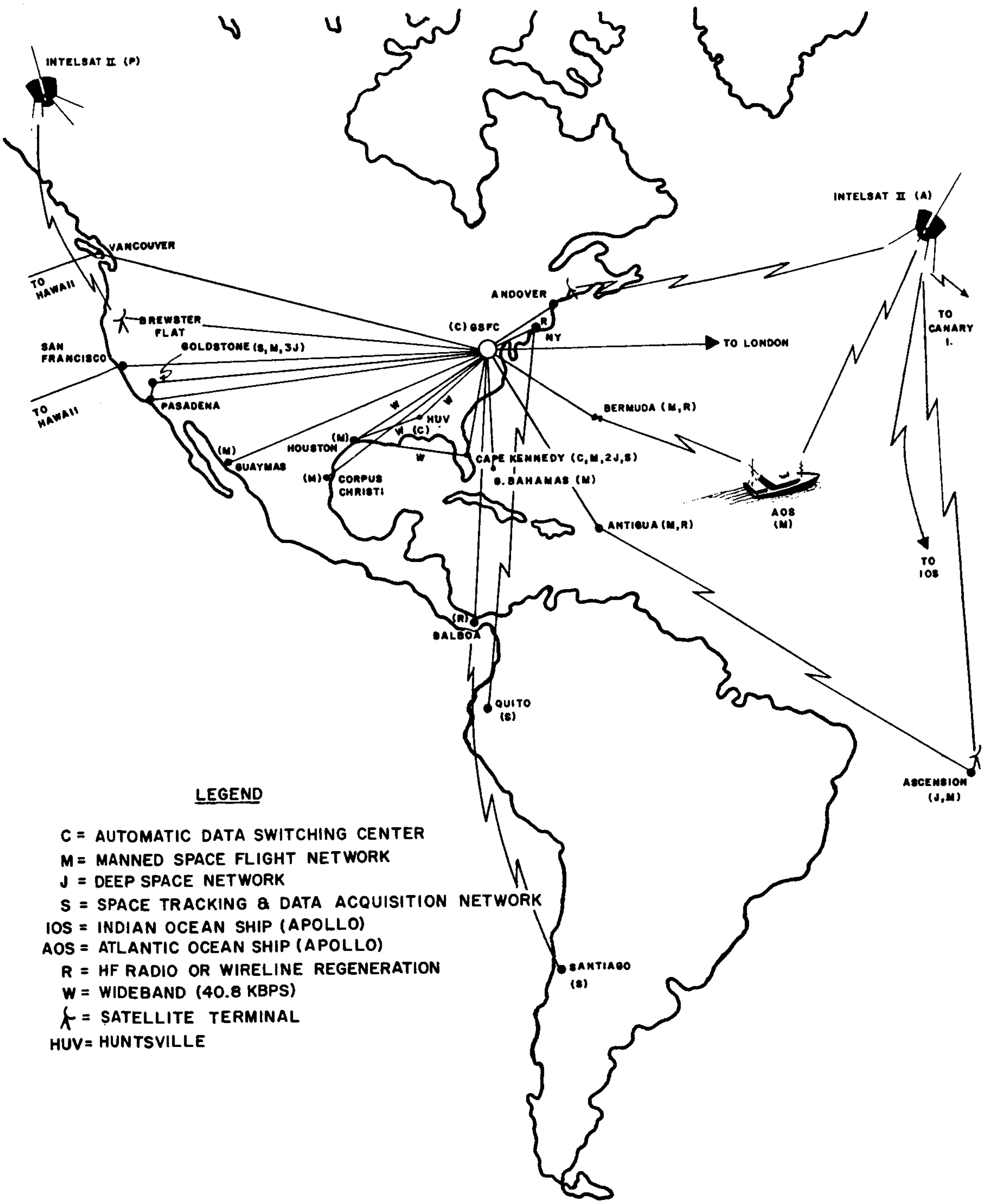
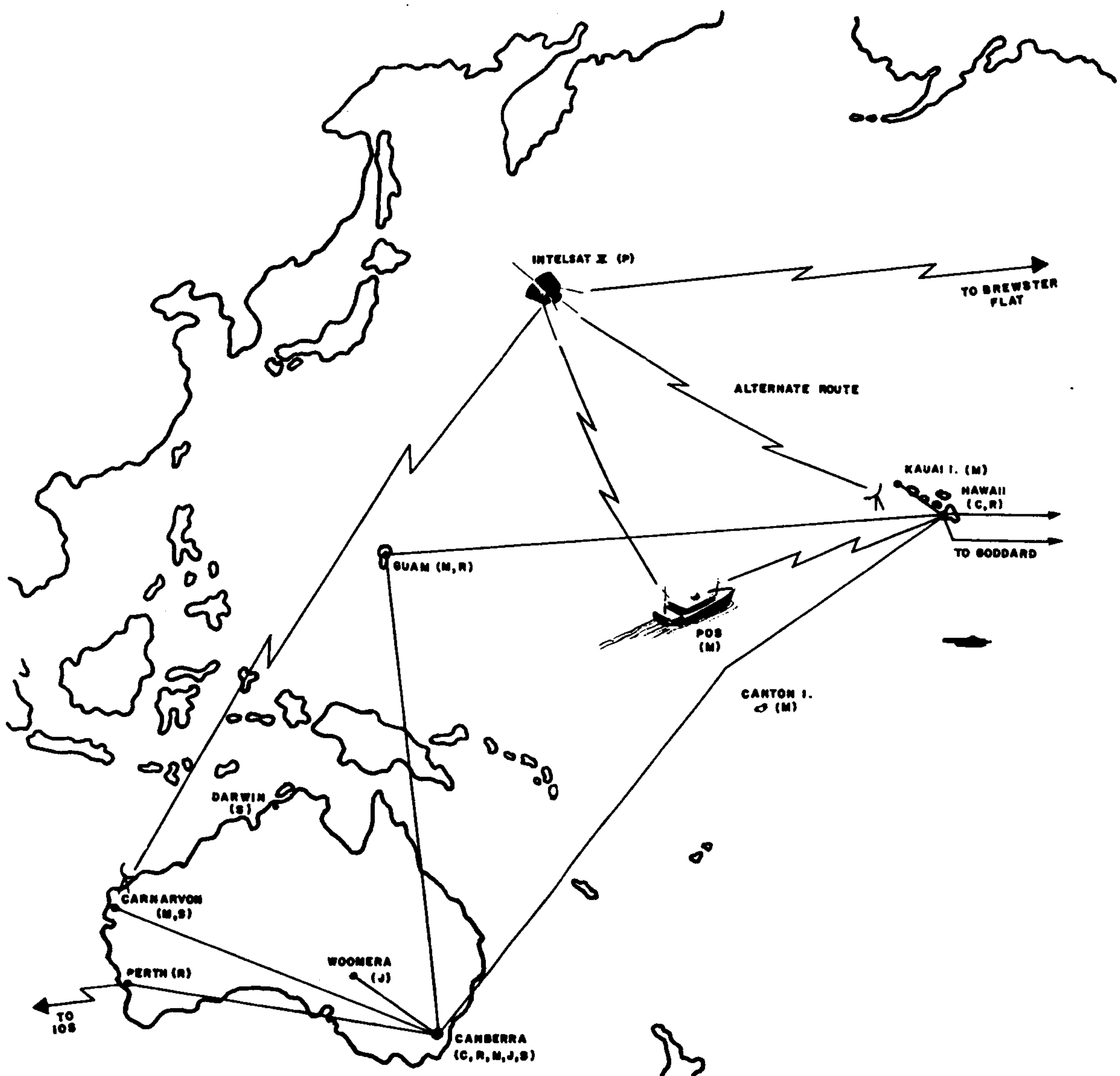


Figure 1. High-Speed Data Communications Network, North and South America



LEGEND

C = AUTOMATIC DATA SWITCHING CENTER
M = MANNED SPACE FLIGHT NETWORK
J = DEEP SPACE NETWORK
S = SPACE TRACKING & DATA ACQUISITION NETWORK
IOS = INDIAN OCEAN SHIP (APOLLO)
POS = PACIFIC OCEAN SHIP (APOLLO)
R = HF RADIO OR WIRELINE REGENERATION
W = WIDEBAND (40.8 KBPS)
⅄ = SATELLITE TERMINAL

Figure 2. High-Speed Data Communications Network, Pacific Area and Australia

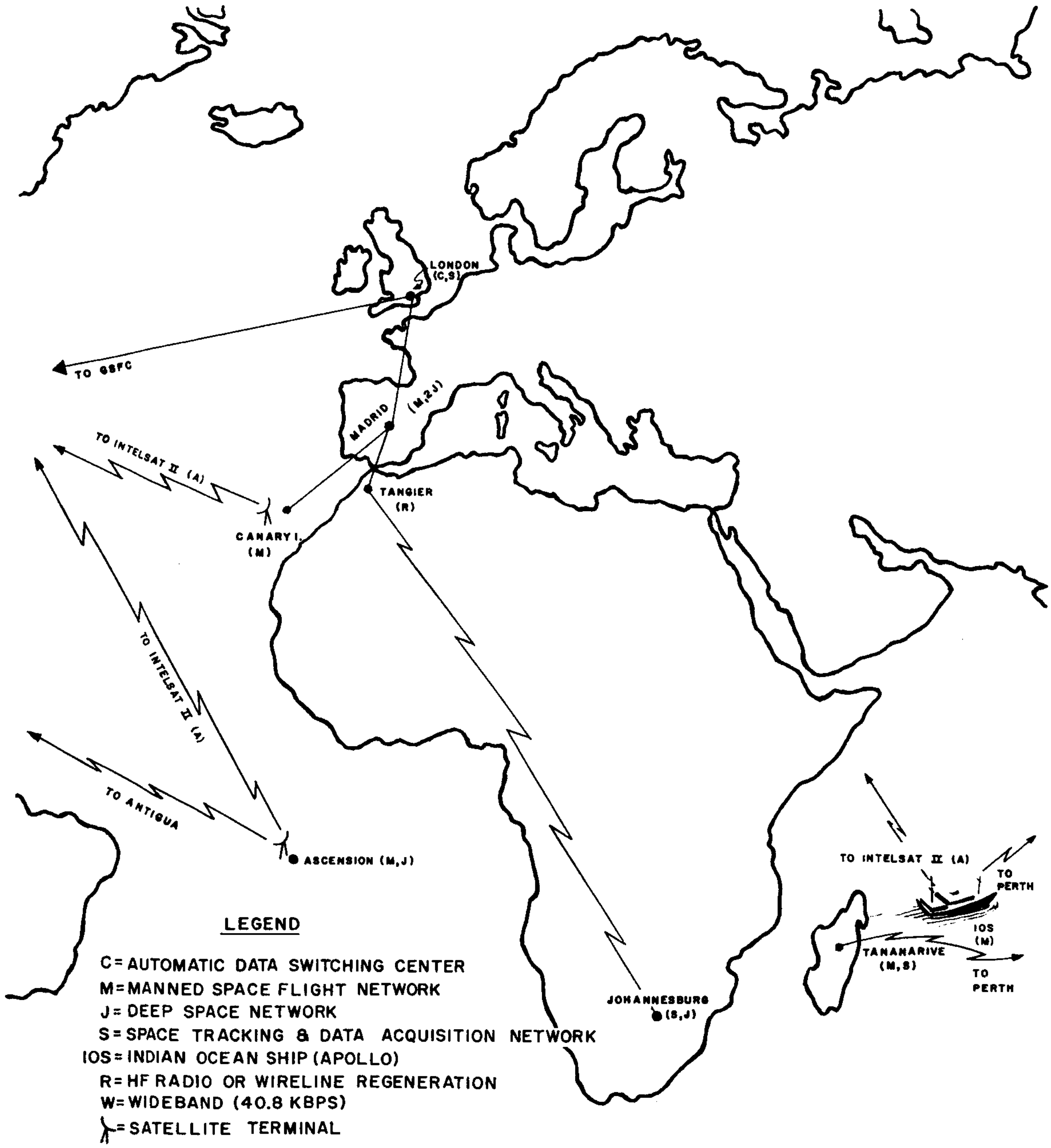


Figure 3. High-Speed Data Communications Network, European and African Area

To provide real-time teletype service to all mission and project control centers, communications processors (CP's) at GSFC, London, and Canberra are used for message switching. Teletype CP's at the overseas switching centers and at GSFC receive teletype messages from the tracking sites over 45-, 50-, or 75-baud teletype circuits. Two diversely routed high-speed data circuits operating at 1200 and 2400 bits per second link each of the overseas CP's to the primary switching center at GSFC. At GSFC, the teletype messages are transmitted to the specific project and mission control centers over teletype circuits of sufficient capacity to handle the peak mission traffic load. For example, a teletype message originating at Carnarvon, Australia, and destined for Houston, Texas, is sent to the NASCOM switching center at Canberra where it is interleaved with other messages over the high-speed data circuits to GSFC. At GSFC the message address is read by the GSFC-CP and retransmitted over a teletype circuit to the Mission Control Center at Houston, Texas.

Voice circuits are now switched manually by means of a special four-wire switchboard at GSFC called the Switching, Conference, and Monitoring Arrangements (SCAMA). Through the use of pushbuttons, an operator at GSFC can interconnect voice circuits from tracking sites with those to project and mission control centers. Special four-wire switchborads are also operational at the London, Canberra, and Honolulu centers.

High-speed digital (600 to 128,000 bits per second) is presently switched either on an alternate basis with the voice network or by manual patching at a technical control point.

With an increase in the number of manned and unmanned missions, it became apparent that the volume of high-speed data to be handled would introduce additional switching problems. The cost to provide each user with separate communication facilities from a given tracking station directly into specific project or mission control areas would be prohibitive. Severe operational problems would be encountered if user requirements for high-speed data were implemented using manual circuit switching. For example, a voice-band data message originating at Carnarvon, Australia, would depend upon the coordinated efforts of seven operators to establish a data grade circuit ultimately terminating in the Mission Control Center at Houston, Texas. Thus, to meet the reliability objectives of future programs, the ADSS was designed to perform automatic switching of high-speed data messages at the network switching centers.

The ADSS is a computer-controlled switching system which uses CP's at the existing NASCOM switching centers to perform message switching on 1200-2400 bit per second data circuits. Each data block is prefixed by a header to provide routing and accounting information similar to the teletype header.

High-speed data blocks are received from the tracking stations at the overseas automatic data-switching centers and forwarded to GSFC on trunks at data rates up to 9600 bits per second over specially equalized voice-frequency bandwidth circuits.

Data blocks are then forwarded to mission and project control centers. A high-speed data message originating at the manned flight site at Carnarvon, for example, will be transmitted to the CP at Canberra and forwarded to GSFC. At GSFC, the high-speed data messages are sent to the Mission Control Center at Houston, Texas, over two diversely routed 40.8 kbps data circuits. Figure 4 is a schematic representation of the planned ADSS configuration within the NASCOM network.

SYSTEM HARDWARE

The CP's now in operation at GSFC (Univac 490A systems) for teletype message switching consist of a basic central processor and 1.2-million bits of random access ferrite core memory with a cycle time of 4.8 microseconds. The mass-storage device now in operation is a drum having a storage capacity of 23-million bits of information. Teletype message traffic queues and recent traffic are stored on this drum for recall up to 16 hours, depending on traffic loads. At London and Canberra, the CP's (Univac 418 systems) have an access time of 2 microseconds with 216 thousand bits of core storage. The mass-storage device at these centers is also a rotating drum unit with 4.7-million bits capacity.

The CP's (Univac 494 systems) to be installed at GSFC for the ADSS consist of a basic central processor and associated peripheral subsystems including over 2-million bits of random access core memory with a cycle time of 750 nanoseconds. The central processor maintains control over input-output, storage, and logical functions of the CP. The peripheral devices include the mass storage and the multiplexers and scanner which connect the switcher to the transmission network. A terminal device associated with each data circuit provides direct interface with the communications transmission media. The mass-storage device for the ADSS is also a drum with a total storage capacity of 46-million bits of information. Teletype traffic queues and recall storage will use the mass storage in a manner similar to the present system. Less frequently executed programs will also be stored in this area.

The CP's at the automatic data-switching centers at London, Canberra, and Honolulu consist of a central processor with 288-thousand bits of core storage with an access time of 2 microseconds. Two drum units each with 4.7 million bits each of storage capacity satisfy the mass-storage requirements at these centers.

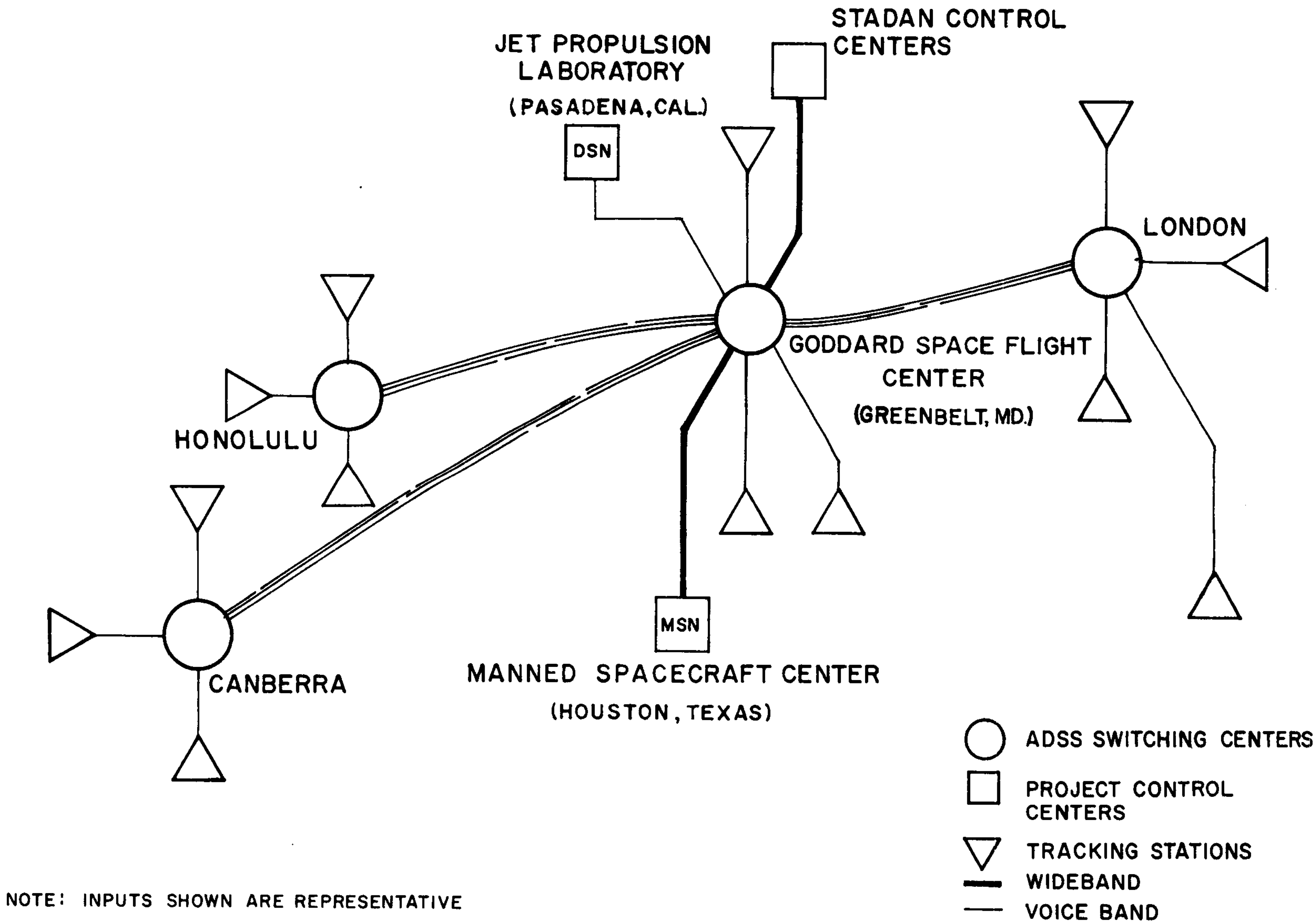


Figure 4. Basic Automatic Data-Switching System

The CP's at each of the switching centers are configured in a standby redundant configuration, (i.e., the off-line equipment is in constant readiness in case the on-line system fails). This equipment configuration provides assurance that the ADSS system will be available during periods of extended mission activity. Figure 5 shows a typical dual-equipment ADSS configuration. Dual standby redundancy produces a high value for mean time to first failure (MTTFF) of the system. The value for system availability of 0.998 is a design goal which in standby redundancy still permits conservative figures for repair rate and single-system failures.

ADSS processor interface with transmission channels in the NASCOM network is accomplished by the communication subsystem which is used to provide initial synchronization, buffering, serial to paralled conversion, multiplexing of input channels, and when required by the user, error control. The communication subsystems consist of a communication line terminal (CLT) which buffers the incoming serial input for parallel transfer to the processor or accepts parallel data from the processor for serial output to the transmission link, and a multiplexing device which connects the specific circuit to the central processor through an input-output channel on a time-shared basis. The CLT provides initial synchronization through detection of the synchronization word shown in Figure 6. The techniques for maintaining synchronization are discussed in the section on software.

When needed, the communication subsystem can provide error control capability by employing a special polynomial buffer terminal (PBT) which performs all the functions indicated for the CLT and which also provides encoding, decoding, and the addition of error status indicators. The PBT can provide reliable error detection through the use of an existing technique* which also provides message framing of the input data. The multiplexer associated with the PBT performs the same function as that associated with the CLT. In each instance, a single multiplexer can accommodate up to 16 high-speed circuits.

The use of error-detection techniques in the communications subsystem assures an undetected error rate which will not exceed 1×10^{-12} and less than a 15 percent loss in transmission efficiency, with line error rates exceeding 1×10^{-3}. Where real-time requirements are not restrictive, the error-detection technique is combined with automatic retransmission capability between CP's to increase the amount of valid data handled on the link.

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*Frey, A. H.: Message Framing and Error Control. IEE Transactions on Military Electronics. p. 143-147, April 1965

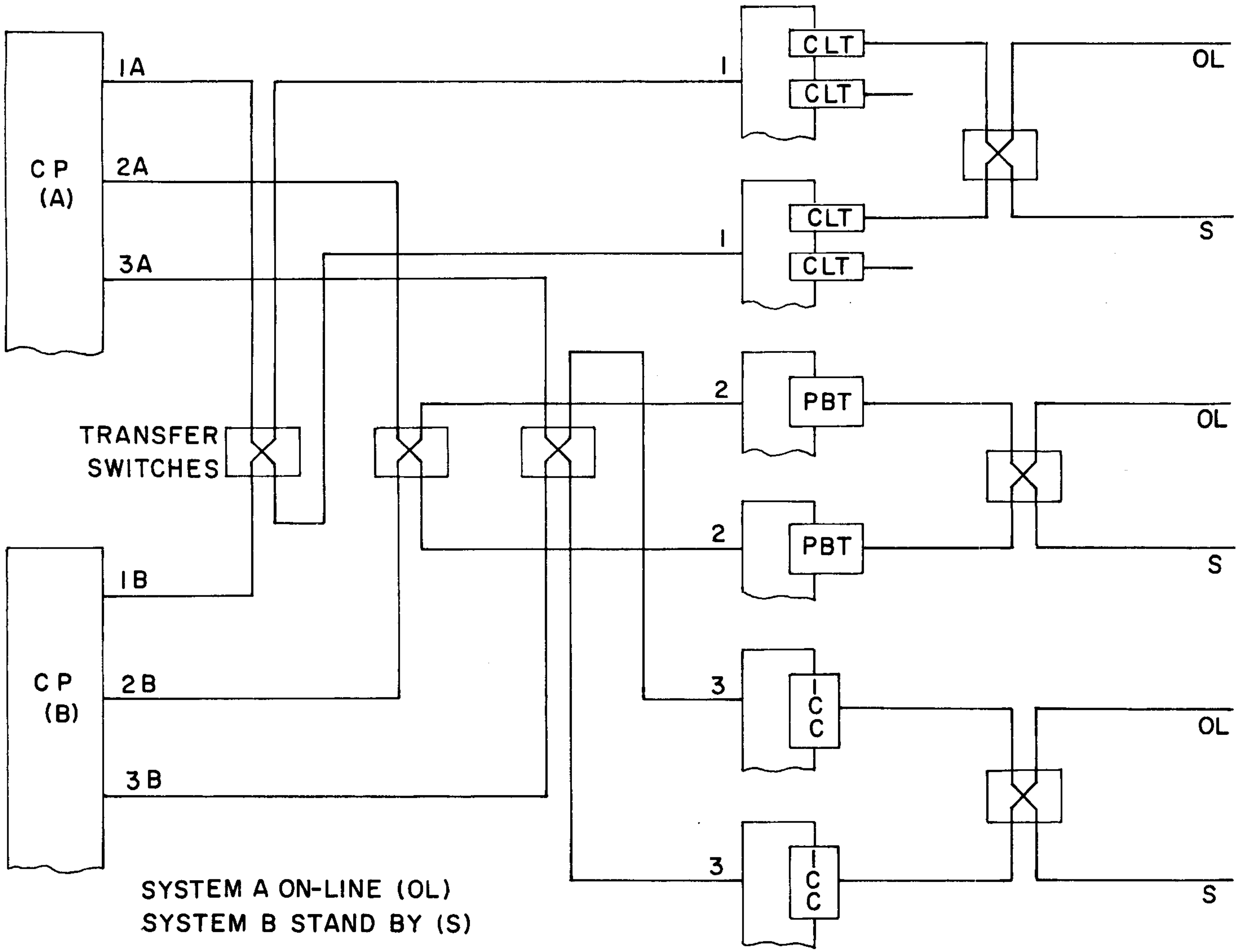

Figure 5. Dual-System Communications Processor

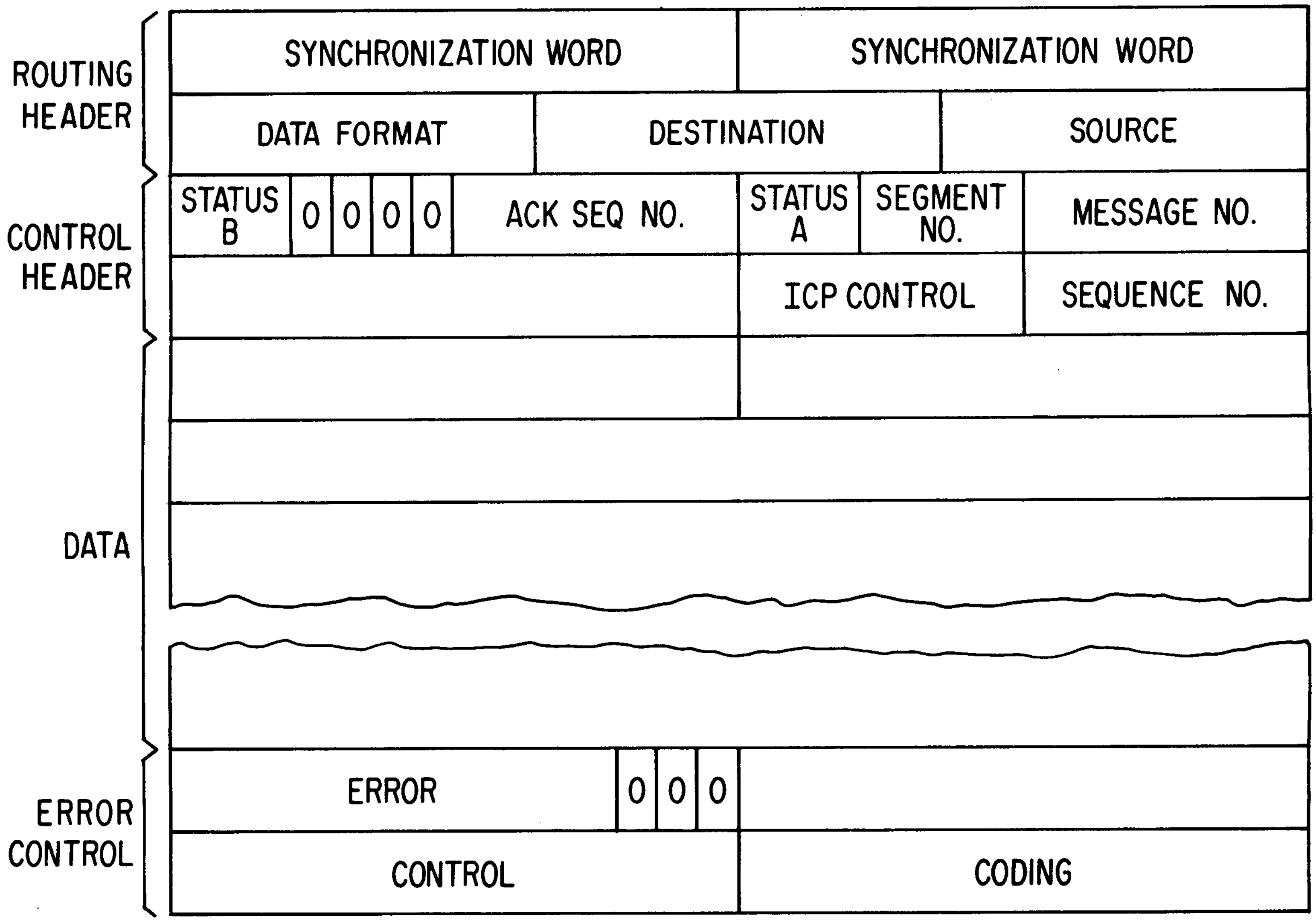

Figure 6. ADSS Transmission Format

In addition to the standard console capability for program monitoring and modification, the ADSS provides facilities for centrally monitoring the status of communication facilities at the switching centers and remote sites. A display program within the processor automatically updates stored displays with the required communications status information. By entering a coded numeric from the console to the processor, communication controllers can view on cathode-ray tubes at a communication console any of the stored displays. Preprogrammed limits on communications status conditions force specified displays for viewing, thus permitting necessary controller action. Hard copies of the stored displays are available through controller request by access to a high-speed printer. A map display providing processor controlled information of circuit availability and usage is planned for GSFC.

SYSTEM SOFTWARE

The ADSS implementation plan calls for an established procedure for routing data from the tracking stations to the control and computing centers. To perform effectively with a minimum amount of processing, the switching CP must know the source and destination of the data blocks as well as the type of data being handled. This information is placed at the beginning of each data block transmitted from the sites. Switching and routing procedures are based on this header information. The routing header is shown in Figure 6. When two CP's communicate (as between London, Canberra, or Honolulu) to GSFC, a control header is used in addition to the routing header to maintain accounting between CP's.

The ADSS software subsystem is divided into four levels which run from D, the lowest, to A, the highest. Level D processing monitors the input terminals, maintains buffer control over the data flowing through the system, and also controls rudimentary accounting of input and output messages. Level C consists of various analysis routines. These programs will determine what action that system shall take when changes on the inputs or equipment failures occur. The analysis routines also monitor the general performance of the system and inform operators of impending problem areas. The policy followed by the analysis routines is set by the system reconfiguration routines in level B. While these routines have limited policy-making ability, the ultimate control of system policy remains with the operator through interface at level A. Figure 7 illustrates the software subsystem structure.

Each processor is a set of routines designed to accomplish a specific task within the hierarchial structure. These processors are normally linked through program linkage tables. The structure of the transmission network is also stored at each source and the destinations are connected to each output. The following paragraphs briefly describe the operation of the four software structural levels.

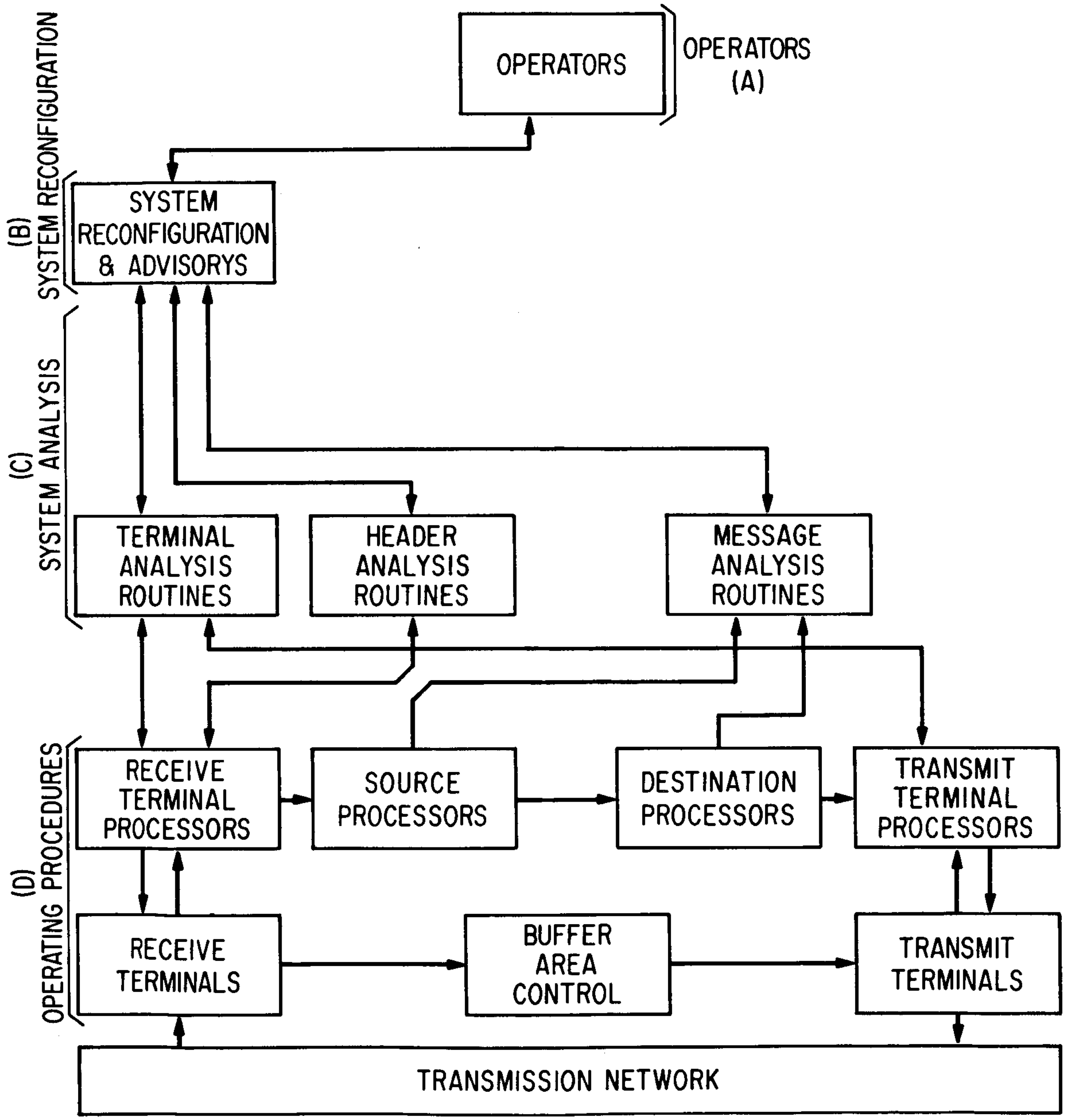

Figure 7. System Control Structure

Level D

The operating procedures level of the software subsystems is divided into four functional areas: the receive terminal, source, destination, and transmit terminal processors. These routines perform all basic switching and accounting functions within the CP. In addition to the basic functions, these programs also detect out-of-limit conditions that require further attention. The receive and transmit terminal processors control the specific data interface points and monitor the performance of these points based on the data format code appearing in the input header. The source and destination processors maintain accounting with the specific source or destination as defined by the appropriate code appearing in the data header.

The input terminal processor routines, with associated buffer-control routines, transfer data to the core memory of the computer and simply match the header on the data block with a header pattern stored in a small area of core set aside for each terminal. These "module" areas hold significant information concerning each terminal, including their recent history. If a perfect match occurs, past switching and buffering procedures are followed. If a perfect match is not detected, the appropriate analysis routine determines the cause of the mismatch. When a mismatch is caused by transmission errors, the history of the terminal is used to switch the input block. When the change in the input routine header is valid, new procedures are established and entered in the history area.

Following the input routines are the source processors; these routines are selected based on the source code residing in the input module area. There are two general source processors, one for message accounting and one for data being switched through the system without accounting. The next set of routines are destination processors selected by destination code also residing in the input module area. They generate accounting information for the distant processor, or if no accounting is required, pass control on to the last processor, the output terminal processor. These final routines control the output data interface and monitor the performance of the output terminal.

Level C

Level C is the analysis level. When the system experiences changes on its inputs, this level of processing analyzes these changes. To build the analysis routines, the following factors must be analyzed:

1. Transmission errors due to natural disturbance
2. Change in link requirements, i.e., a valid header change
3. Loss of frame synchronization
4. Faulty switching or transmission equipment in the field

All of these conditions can cause ambiguities or lack of confidence in the established switching linkage and must be considered. The ambiguous conditions are classified as terminal, header, or accounting ambiguities. Figure 7 illustrates level C and the interconnection with the normal level D.

When changes occur in terminal status, the terminal processors in level D alert the terminal analysis routines. These routines consider problems such as excessive invalid block transfers and loss of modem timing. The header analysis routines generally handle validation of the incoming data blocks. They search the structure of the network to determine the validity of input data and establish valid switching linkage procedures. For problems such as out-of-sequence message and segment numbers and failures in distant switching equipment, the source and destination processors alert the message analysis routines.

Level B

This level is intended to stabilize the operation of the lower level processors. This level controls areas such as change in network circuit usage and change in error tolerance so that the system can adapt to the total network environment.

The two routines presently planned for this level of processing are structural changes and operator interface. The network structural tables can be changed when the system, as configured, cannot satisfy the goals set down by the operators. For example, if one of the broadband circuits between GSFC and Houston should fail, this routine will determine the procedures to reassign circuits available to re-establish data transmission. The operator interface routines also receive orders from the operators for structural changes in network and generate display messages to inform the operator when his decisions are required.

Another area being considered for this level is accounting coordination between the two redundant computers to keep the processors in synchronization and to avoid excessive use of analysis processors by any specific terminal. The two redundant computers, to act in true parallel fashion, must be considered as two coupled or interacting subsystems. When this configuration is implemented, some of the integrity of the two subsystems is lost. This factor affects the operational availability and must be considered in overall availability calculations.

Level A

Level A is the operator-computer interface. It is at this level that the operator maintains system control. Through the use of display information and advisories, the operator may make determinations as to system status. He may also take action through various input devices available to make system reconfiguration to meet changing or emergency conditions.

By structuring the system hierarchy on these levels, the software subsystems can operate as a direct extension of the operator. The general adaptive nature of the structural tables and operating software permits changes in the system through the operator interface without making direct changes to system programming, thus permitting the software to reach a steady-state reliability.

CONCLUSIONS

Because of operational problems existing in any large-scale data-switching system where manual circuit switching is attempted, NASCOM selected a computer-oriented data-switching system. This approach allows the basic switching tasks to be handled by a general-purpose digital computer as well as considerable economic savings by using shared trunks.

Hardware-software boundaries were drawn so that error detection and correction could be most economically implemented in the data-transmission path requiring them. The hardware system adds to equipment now operating to provide whatever expansion is required, thus permitting system growth without destroying existing capability. The software system allots computer-processing time to circuits which require attention because of high transmission errors or other environmental disturbances and is designed to adapt to widely varying transmission-line error characteristics. Normal transfers require a small amount of the processor time.

Operator interface is designed to present problems for solution only when the system, as structured, cannot cope with these problems and to present problems at a rate not exceeding the operator's decision-making capability. The ADSS system will simplify the operational problems involved in high-speed data switching and minimize the number of comparatively expensive leased voice/data trunks between GSFC and the NASCOM network overseas switching centers.