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ADVANCED COMPUTER DORMANT RELIABILITY STUDY

By L. K. Davis, T. C. Schairer and G. A. Watson

14 OCTOBER 1967

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FOREWORD

This final report describes the work accomplished under NASA Contract NAS 12-536, "Advanced Computer Dormant Reliability Study." It was performed by Autonetics, a Division of the Aerospace and Systems Group of the North American Rockwell Corporation (formerly North American Aviation, Inc.), Anaheim, California. The work was administered under the direction of the National Aeronautics and Space Administration, Electronics Research Laboratories, Cambridge, Massachusetts.

The participants were:

G. A. Watson - Principal Investigator

L. K. Davis

T. G. Schairer

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ADVANCED COMPUTER DORMANT RELIABILITY STUDY

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Autonetics, A Division of North American Aviation, Inc.
Anaheim, California

SUMMARY

This report describes a six-month study of the affect of applied power on the reliability of integrated circuits and discrete components and the relationship between bipolar and MOS integrated circuit reliability. The Contract Work Statement is as follows:

Item 1 - Analyze the Minuteman Program component failure modes under two (2) specific input power modes; full power and dormant (no power). Provide a compilation of statistics relating the mode of operation to the cause of device failure. Hypothesize the performance of MOS devices under the above conditions by comparing MOS parameters to integrated circuits and discrete components. Determine a general mathematical model concept for relating integrated circuits and discrete component data to MOS predictions of reliability. Provide a compilation of achieved MOS reliability on existing non-classified Autonetics systems.

Item 2 - Perform an investigation of the theoretical effects on MOS devices when subjected to the above power input conditions. The study shall include the operating frequency characteristics. Develop expected failure modes for MOS under these conditions. This effort will be limited to theoretical analysis.

Item 3 - Develop predicted failure rates for MOS devices for the present industry technology and for a point in the late 1970's by use of the transfer model developed under Item 1 on a large scale MOS device. Perform an analysis relative to selecting the optimum method of storing spare modules in a space vehicle as it concerns input power conditions, considering MOS, integrated circuits and discrete parts.

In view of the overall objectives of the study, major emphasis was placed upon integrated circuit (IC) data analysis. The WS-133B systems have accrued 1,222,275 system-hours through 30 June 1967. This represents approximately 3.1 billion IC component-hours of field operation, as well as 1.4 billion transistor component-hours, 1.8 billion capacitor component-hours, 3.2 billion diode component-hours, and 4.8 billion resistor component-hours. During this time, 93 IC's, 28 transistors, 37 capacitors, 27 diodes, and 2 resistors were assessed as the primary cause of system failure. The best estimate achieved failure rates range from 0.00004 percent to 0.0027 percent per 1000 hours for these components.

The system electronics of particular interest during this study are the computer and a dormant module. These contain 2146 and 113 IC's, respectively. The failure modes of IC's from these modules were analyzed and several distributions were constructed. Also, the operating time of these failures was plotted to determine its significance.

A statistical analysis was performed using the failure data of all components, and a dormant/normal reliability ratio was calculated. Two important observations are as follows: (1) the improvement is generally less than the expected on an intuitive basis and, (2) the confidence band is quite broad due to the small number of failures.

The aspects of MOS devices which contribute to a uniqueness, relative to bipolar devices, are discussed. The effects of the specified storage modes on these MOS characteristics were studied. It is concluded that the dormant storage mode offers an advantage over normal power operation provided that the duration of storage is a significant part of the equipment mission time.

Integrated circuit and MOS device manufacturing process data have been compiled and are included in this report. Manufacturing flow charts are shown for both technologies, and a chart showing quantitative comparison is also given. A reliability prediction mathematical transfer model for these two technologies and examples of its application are shown. Both full power and dormant failure rate predictions are given for present day technology and for a 1970 period. Achieved reliability data is included for some existing MOS systems.

An analysis has been performed relative to selection of power conditions of spare modules in a space vehicle for discrete parts, bipolar IC's, and MOS IC's. The results of this analysis are contained in this report.

INTRODUCTION

Program Objectives

For long-term, deep-space missions a basic requirement exists to maximize the reliability of electronics. A significant portion of the electronics does not need to be operated during periods of the flight. And, assuming a manned flight, the reliability of spare modules must be considered. The question then arises as to the effect of application of power on the reliability of these modules (and spares, if they are on board) and the possibility of controlling power to maximize the reliability. The possible modes of operation considered in this study are (1) normal (full power) and (2) dormant (no power). Although bipolar technology is used in this study to derive failure modes and rates, the primary technology of interest is MOS and the objective of the study is to derive models and estimates of MOS dormant reliability.

Specific Objectives

The method of realizing the program objectives is similar to that used during the transistor to integrated circuit transition of Minuteman I to Minuteman II, i.e., relating data from currently produced devices of a specified technology to new devices produced by the same or a similar technology. In this case a measure of MOS reliability is sought in the demonstrated bipolar transistor and integrated circuit reliability. The several steps involved are diagrammed in Figure 1.

ANALYSIS AND COMPILATION OF MINUTEMAN COMPONENT FAILURE RATE DATA

Minuteman Weapon System

The Minuteman system consists of ground support and missile flyable hardware. The missile hardware consists of the computer, guidance electronics, etc., all of which have a large percentage of common components. The computer contains the greatest proportion of components and is therefore of particular interest. One amplifier assembly in the flight control system is nonoperative except for brief checkout periods of 30 seconds twice a month, while the computer is functional at all times. The distribution of components between these two sections is indicated in Table I. The accumulated time on all field systems is approximately 1.2 million system-hours. Less than 50 percent of the systems have logged in excess of 2000 hours operation and only one had logged in excess of 7000 hours as of February 1967.

Failure Rate Determination

The Minuteman II reliability concept is one of failure mode identification – corrective action – evaluation. This is necessary in view of the very low failure rate at the component level. Unfortunately, this concept also removes the emphasis on failure rate numerical determination. The Minuteman II numerical determination

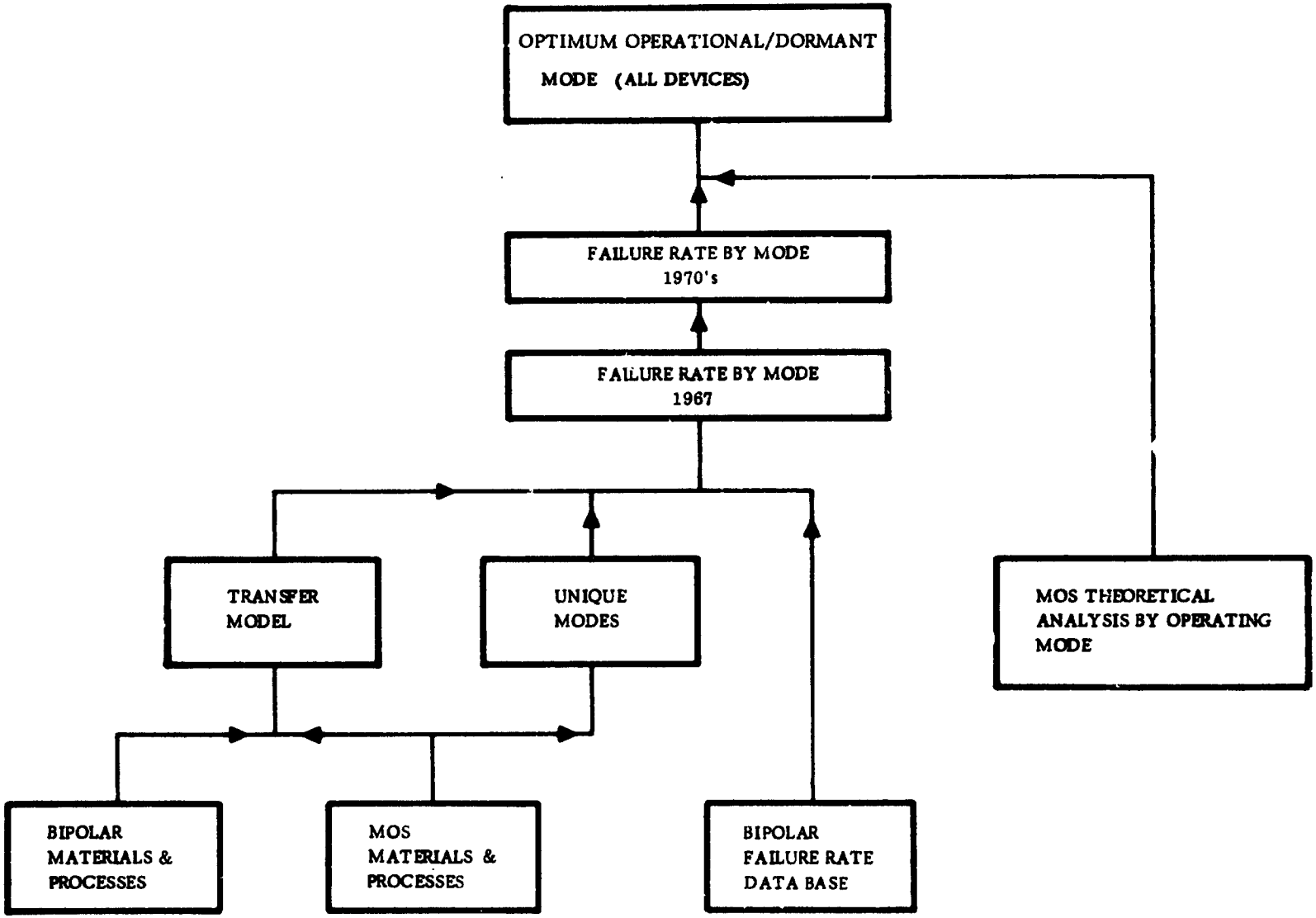


Figure 1. – Study Flow Diagram

follows from an assumed exponential gross failure rate distribution within the operating system. Thus, the operating time of a particular part loses significance. A further complication is that a failed system is subjected to a testing schedule prior to its return to the field, which results in additional component removals. It therefore becomes necessary to limit the statistical analysis to components assessed as the primary cause of field failure.

Figure 2 shows the distribution of failures according to system running time.

TABLE I

COMPONENT DISTRIBUTION FOR A FULLY OPERATIONAL AND DORMANT MODULE – MINUTEMAN II

Component	Computer (Operational)	Amplifier Assembly (Dormant)
IC's	2146	113
Transistors	507	168
Capacitors	416	218
Diodes	1268	401
Resistors	2063	1068

Bipolar and MOS Technologies

The two technologies under consideration are quite similar. In many ways the one MOS for which reliability predictions are sought is the simpler of the two in manufacturing. This relation is made possible by the great strides made over the last few years in the field of oxide passivation and planar diffusion. In fact, these contributions permitted the MOS structure to be formed successfully, although the theory had been well known for years. The advantage of the MOS structure stems primarily from its simpler construction (see Figure 3) which permits a more complex function to be formed in a monolithic circuit. This is the reason for the emphasis on bipolar IC's throughout this study.

Minuteman Components

The Minuteman active electronic components are primarily planar diffused structures. In particular, the IC's are multiple diffused, oxide passivated, planar monolithic components. There are approximately 25 different type numbers; however, the greatest proportion of IC's used are represented by only 3 or 4 types. Originally, an attempt was made to consider only 2 types (901 Flip Flop and 903/904/923 NAND Gates) produced by one manufacturer; however, this proved to be too restrictive in terms of the available data. The construction details (Manufacturer A) are shown in Figure 4 for these 2 types. These are representative of other types and manufacturers.

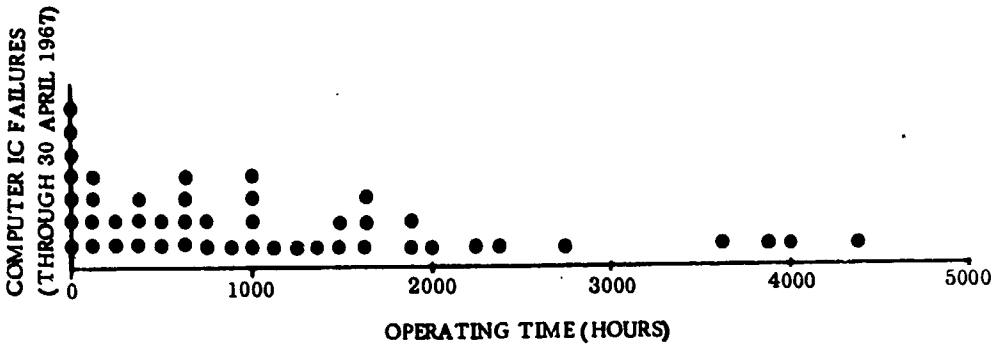


Figure 2. – Distribution of IC Failures With Time

Bipolar Integrated Circuit Failure Modes

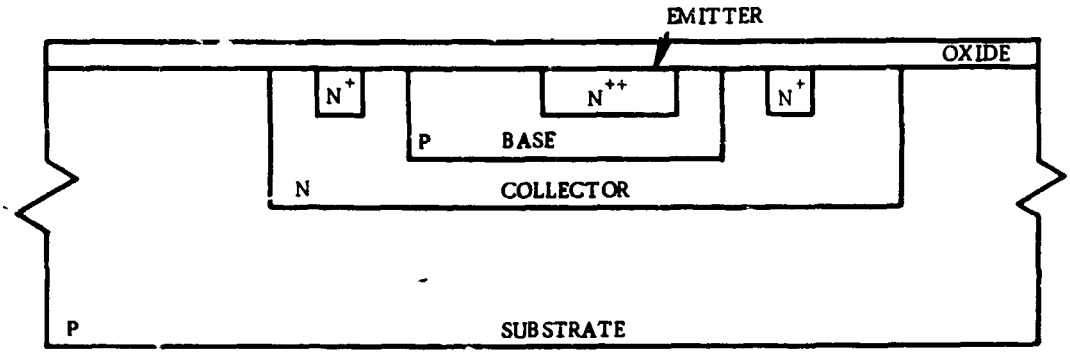
A list of typical IC failure modes is given in Table II. When all failures (build-up, screen, etc.) are considered, each mode is represented; however, the modes represented by field failures have a significantly different distribution. Table III lists the device type, manufacturer, and hours of field operation for all primary computer IC failures, cumulative to 1 April 1967.

Failure Statistics

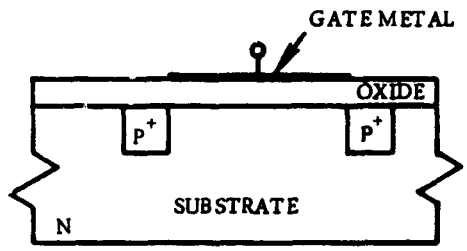
The reliability concept for the Minuteman program was discussed in a preceding section, and it was pointed out that the correlation of all failed devices with their operating history would produce uncertain results. Therefore, the decision had been made to concentrate attention on those devices which fail under a uniform, common environment, i.e. primary field failures. A consideration of only the simple triple diffused IC's would be more representative of the MOS technology, however, no definitive statements would be made concerning dormant mode reliability because of the extremely small number of triple diffused IC failures. For this reason, all device types are included in the statistical analysis to follow. This has the effect of making the statistical statements more conservative.

Tables IV and V summarize the normal mode and dormant mode failure statistics. The mean time between failure (MTBF) data were calculated using the exponential failure distribution assumption for the case of a fixed time sample. (A brief treatment of this theory is included in the Appendix). One failure is assumed where none had yet occurred. Likewise, the more conservative estimate is made when calculating the upper 90 percent confidence value by assuming that one additional failure would have occurred in the next increment of time, had the test continued.

Table VI contains the dormant/normal MTBF ratio data for each component type. The confidence interval has been increased to 98 percent in this instance because the ratios were formed using the 90 percent-10 percent (and 10 percent-90 percent) values.

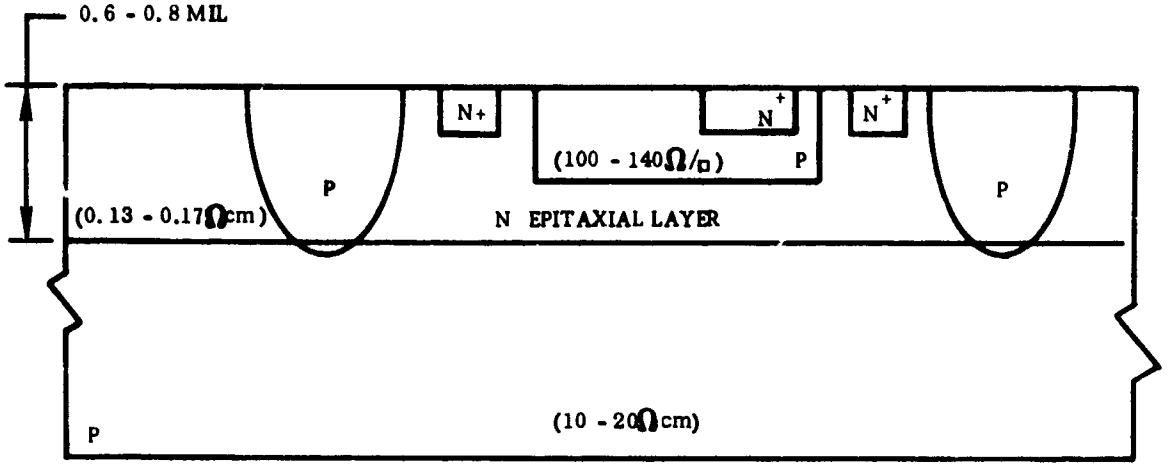


(a) BIPOLAR PLANER DIFFUSED STRUCTURE

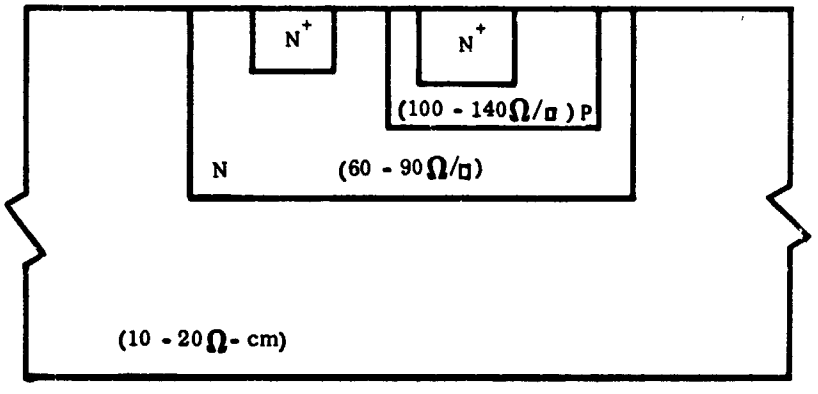


(b) UNIPOLAR TRANSISTOR - MOS STRUCTURE

Figure 3. – Bipolar and MOS Transistor Cross-Sections



TYPE 901



TYPE 903/904/923

Figure 4. – Construction Details for Two Minuteman IC's – Manufacturer A

TABLE II

TYPICAL INTEGRATED CIRCUIT FAILURE MODES

Failure Mode	Failure Mode
A. Oxides 1. Holes 2. Cracks 3. Undercutting 4. Feathering 5. Improper thickness 6. Flaking 7. Non-passivated area 8. Misaligned windows B. Lead Bond 1. Separation - Bond/Interconnect 2. Separation - Bond/External lead 3. Separation - Wire/Bond neck 4. Improper position 5. Undesirable intermetallics 6. Insufficient contact area 7. Voids or cracks C. Metallization 1. Poor adhesion 2. Improper thickness 3. Insufficient width 4. Oxidation 5. Erosion/corrosion 6. Mechanically damaged 7. Voids 8. Metal migration 9. Improper masking D. Internal Lead Discrepancy 1. Sagging lead 2. Excessive length 3. Mechanical damage 4. Improper routing 6. Faulty connection-lead/terminal 9. Fractured E. Faulty Diffusion F. Foreign Materials 1. Foreign material in package 2. Excessive contact material 3. Impurities in materials G. Die-Header Bonding 1. Cracked die	G. Die-Header Bonding (Cont) 2. Faulty bond-preform/die 3. Insufficient clearance-die/case 4. Voids under die 5. Faulty bond-preform/case or lead 6. Crack in bond 7. Undesirable intermetallic formation 8. Misorientation of die 9. Oversized die H. External Features 1. Mislabeled 2. Inverted lead frame 3. Wrong leads clipped 4. Physical damage (unable to test) 5. Lead length too short 6. Dimensionally incorrect J. Surface Defects 1. Inversion layer 2. Contamination 3. Overetch K. Crystal Imperfections 1. Etch pits/lineage/stacking faults 2. Pipes in silicon 3. Junction imperfections L. Testing and Use 2. Electrical overstress 5. Mechanical overstress 6. Electrical overstress - parasitic action 7. Parasitic action, no overstress M. Package Discrepancies 1. Faulty cap to case seal 2. Faulty terminal to insulator seal 3. Faulty insulator to case seal 4. External contamination 5. Weld failure 6. Cracked insulator 7. Voids in the package A. Non-hermetic seal Miscellaneous 00. Undetermined L3. Retest Good V1. Retest Bad-no further test required

TABLE III

COMPUTER IC ASSESSED PRIMARY FIELD FAILURES
(THROUGH 1 APRIL 1967)

Mfg	Type	*Hours
Damaged - Unable to Test		
A	901	200
A	923	800
B	901	1700
B	902	1100
B	903	200
B	903	1500
B	904	700
B	904	800
B	923	1200
B	923	1700
Lost, Destroyed, or Unknown		
A	901	0
A	901	1000
A	923	700
B	901	500
B	903	100
B	903	300
B	911	1300
B	921	2000
B	921	2400
Electrical Overstress		
A	904	0
A	904	700
A	906	3600
A	923	700
A	935	1000
B	903	0
B	921	2700
Cracked Die		
A	901	0
A	901	300
A	901	1600
Corrosion		
B	903	2300
B	903	3900
Diffusion or Masking		
A	923	100
A	935	900
Retest OK		
A	901	0
A	901	100
A	901	3800
A	904	0
A	904	500
A	923	1900
B	921	1900
C	904	1600
Oxide Holes		
A	901	0
A	901	100
B	921	1000
Other		
A	903	4400
A	905	1700
A	923	300
B	904	1000
B	921	1400

*Increments of 100 hours

TABLE IV

MTBF DATA FOR FULL POWER MODE COMPONENTS

Type	Quantity	Component Hours ($X10^6$)	Number Failed	MTBF ($X10^6$)		
				Lower 90%	Norm	Upper 90%
IC's	2146	2620	70	31.8	37.8	44.6
Transistors	507	620	15	29.1	41.3	62.0
Capacitors	416	509	10	33.2	50.8	82.5
Diodes	1268	1550	13	79	119.	185
Resistors	2063	2520	1	530	2522	25,220
Data Through 30 June 1967						

TABLE V

MTBF DATA FOR DORMANT MODE COMPONENTS

Type	Quantity	Component Hours ($X10^6$)	Number Failed	MTBF ($X10^6$)		
				Lower 90%	Norm	Upper 90%
IC's	113	138	2	25.3	69	276
Transistors	168	203	2	37.2	102	408
Capacitors	218	266	12	14.6	22	35
Diodes	401	490	1	125	490	4900
Resistors	1068	1300	0	546	∞	∞
			(1 assumed)	546	1300	13,000
Data Through 30 June 1967						

TABLE VI

DORMANT/NORMAL MODE IMPROVEMENT RATIO

Type	MTBF Ratio		
	Minimum (99%)	Expected	Maximum (99%)
IC's	0.57	1.83	8.78
Transistors	0.60	2.47	14.0
Capacitors*	0.18	0.44	1.05
Diodes	0.68	4.12	62.0
Resistors*	0.02 0.02	∞ 0.52	∞ 24.6

Data Through 30 June 1967

*Note: The ratios for these components is inconclusive because of induced capacitor failures and lack of resistor failures.

The data contained in these tables reflect systems status as of 30 June 1967. It will be noted that the active components exhibit a statistical improvement in the dormant mode while the passive components appear to be degraded. This latter conclusion is not warranted for the following reasons. No resistor failures have occurred in the dormant mode. There has been an identified incidence of equipment-caused capacitor failures due to reverse-bias transients.

The dormant improvement growth curves (Figure 5) are included to provide a means for extrapolation. These curves were computed using the observed dormant normal ratio and maximum 99% confidence ratio for various months during the past year. It will be seen that the active component curves are generally well behaved and therefore extrapolation is a reasonable process.

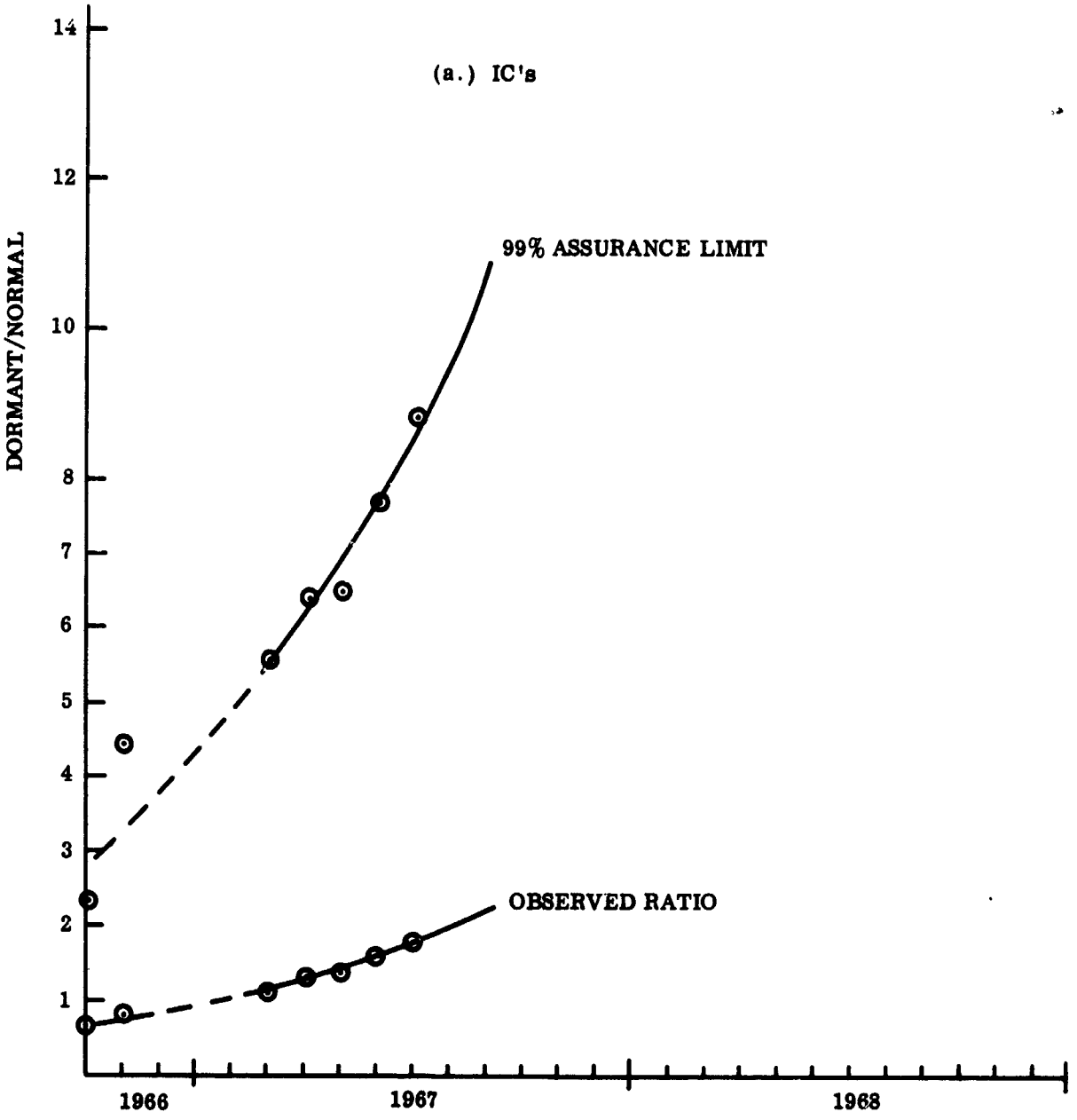


Figure 5. – Dormant/Normal Ratio Growth Curves (Sheet 1 of 5)

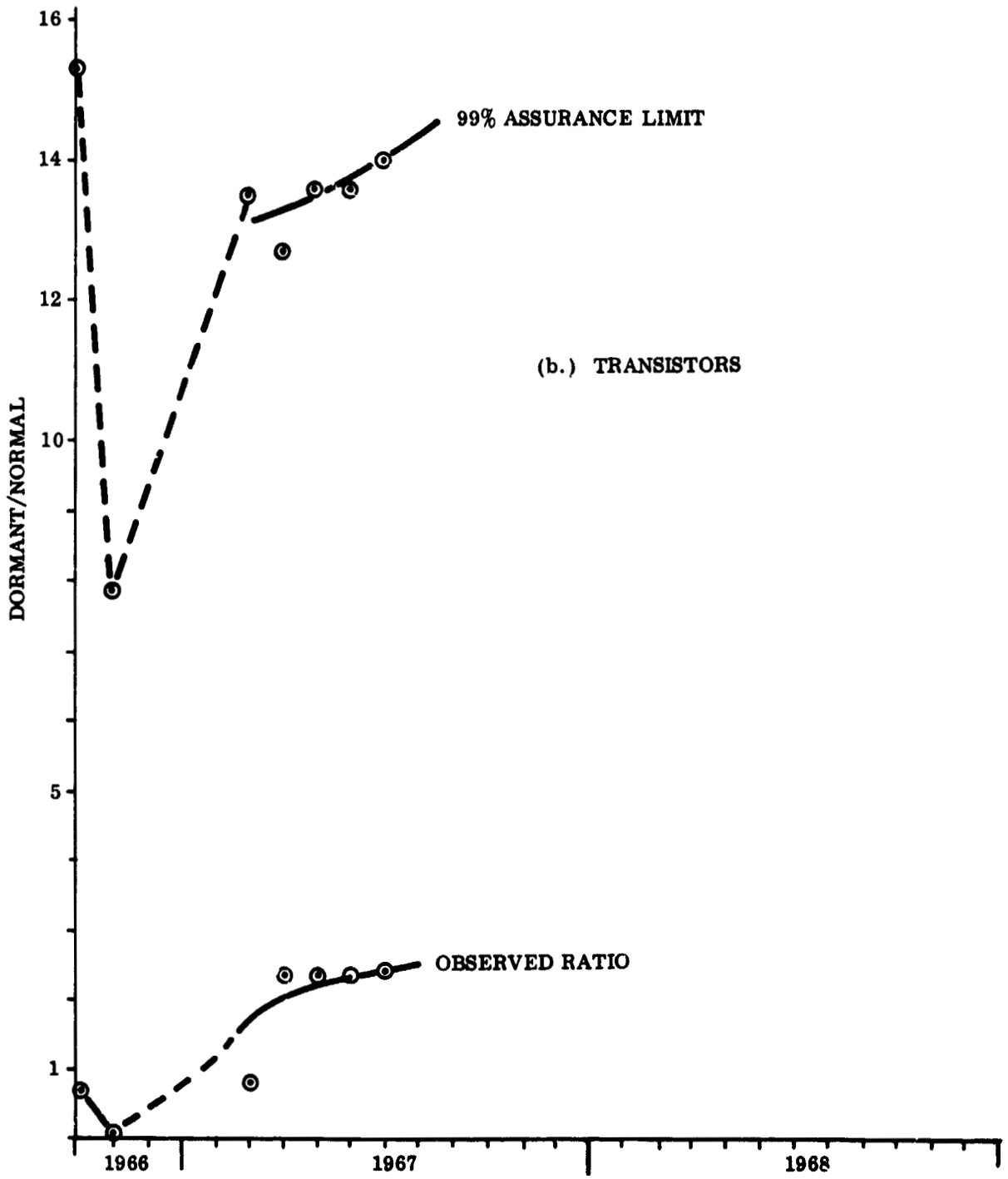


Figure 5. – Dormant/Normal Ratio Growth Curves (Sheet 2 of 5)

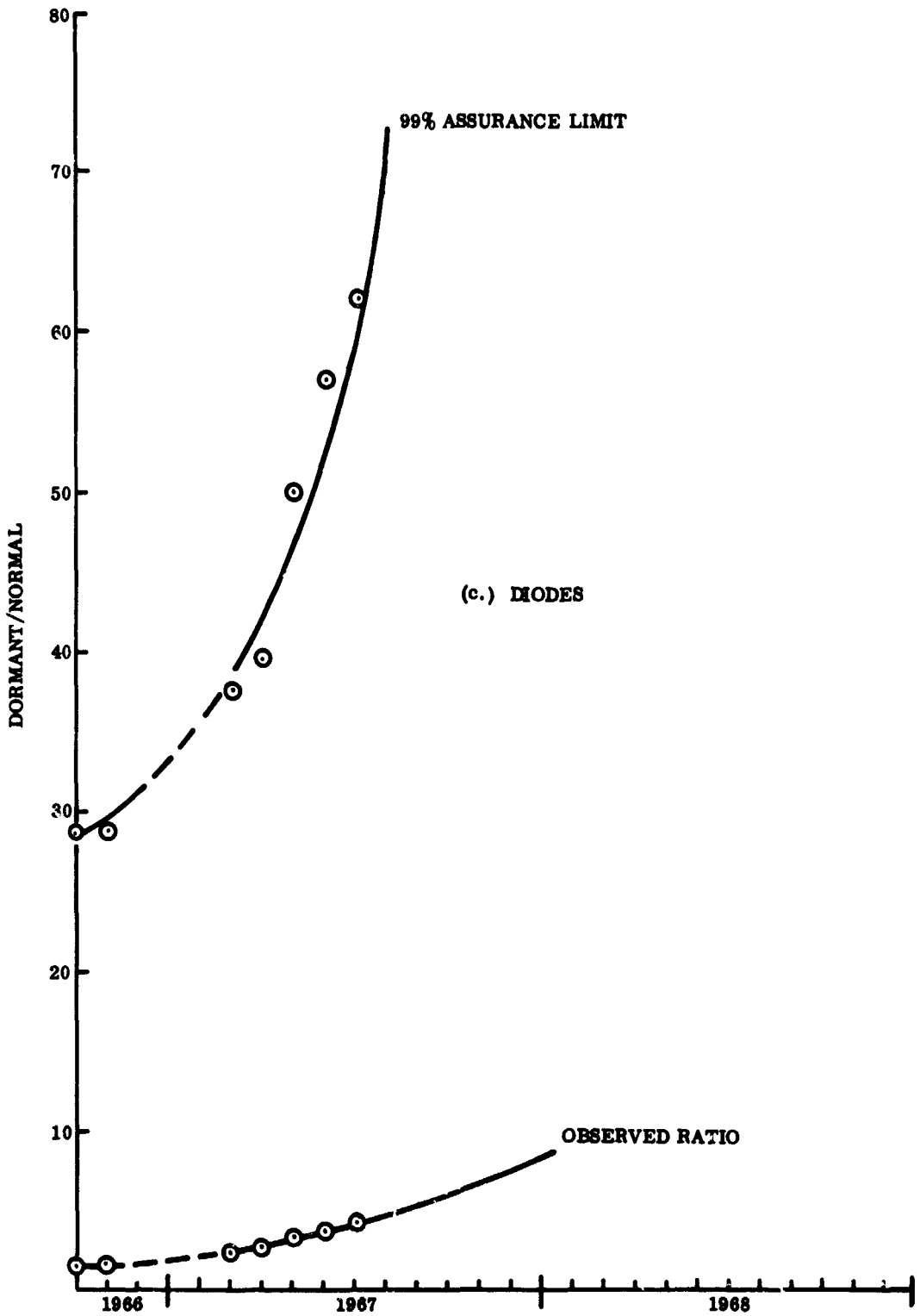


Figure 5. – Dormant/Normal Ratio Growth Curves (Sheet 3 of 5)

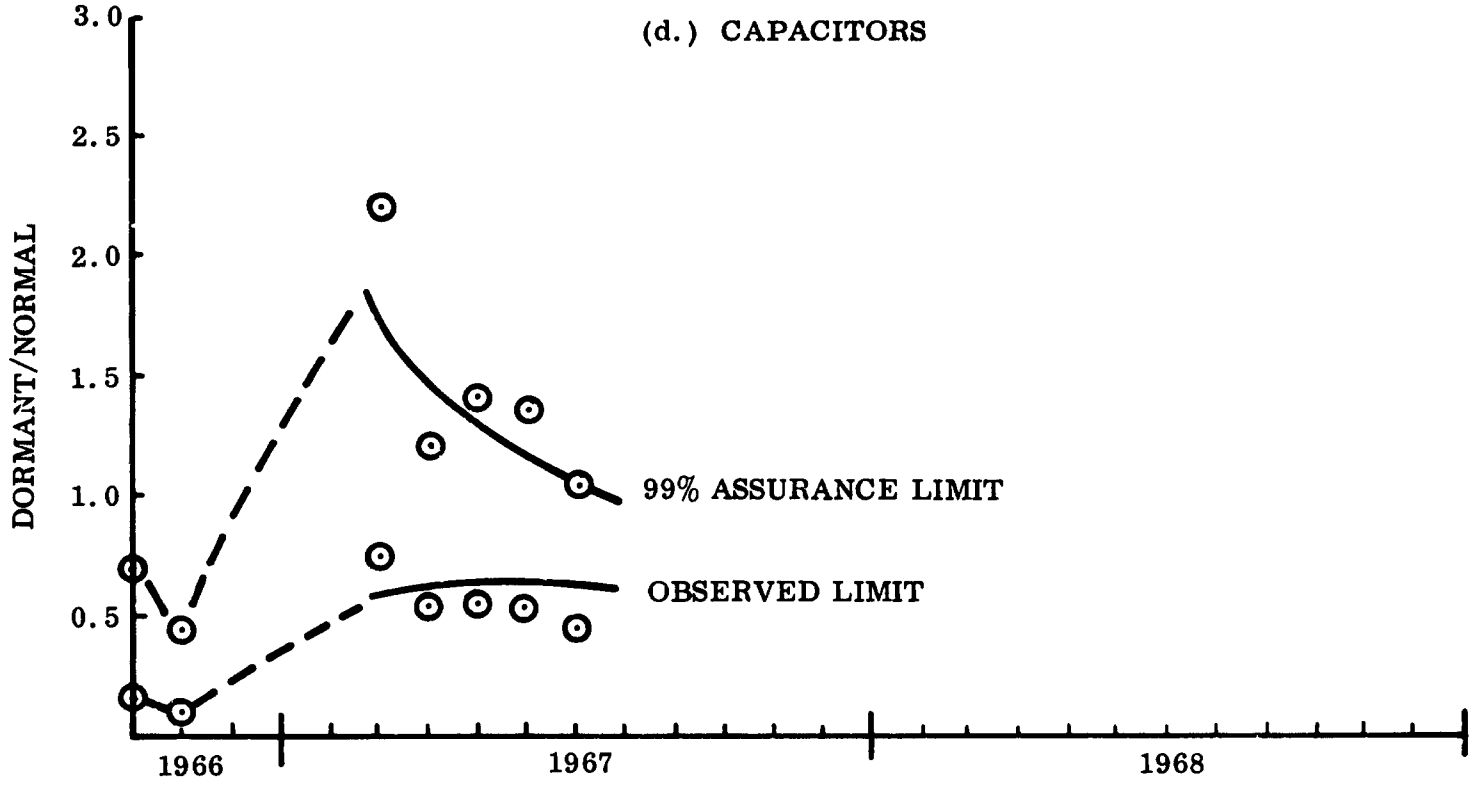


Figure 5. – Dormant/Normal Ratio Growth Curves (Sheet 4 of 5)

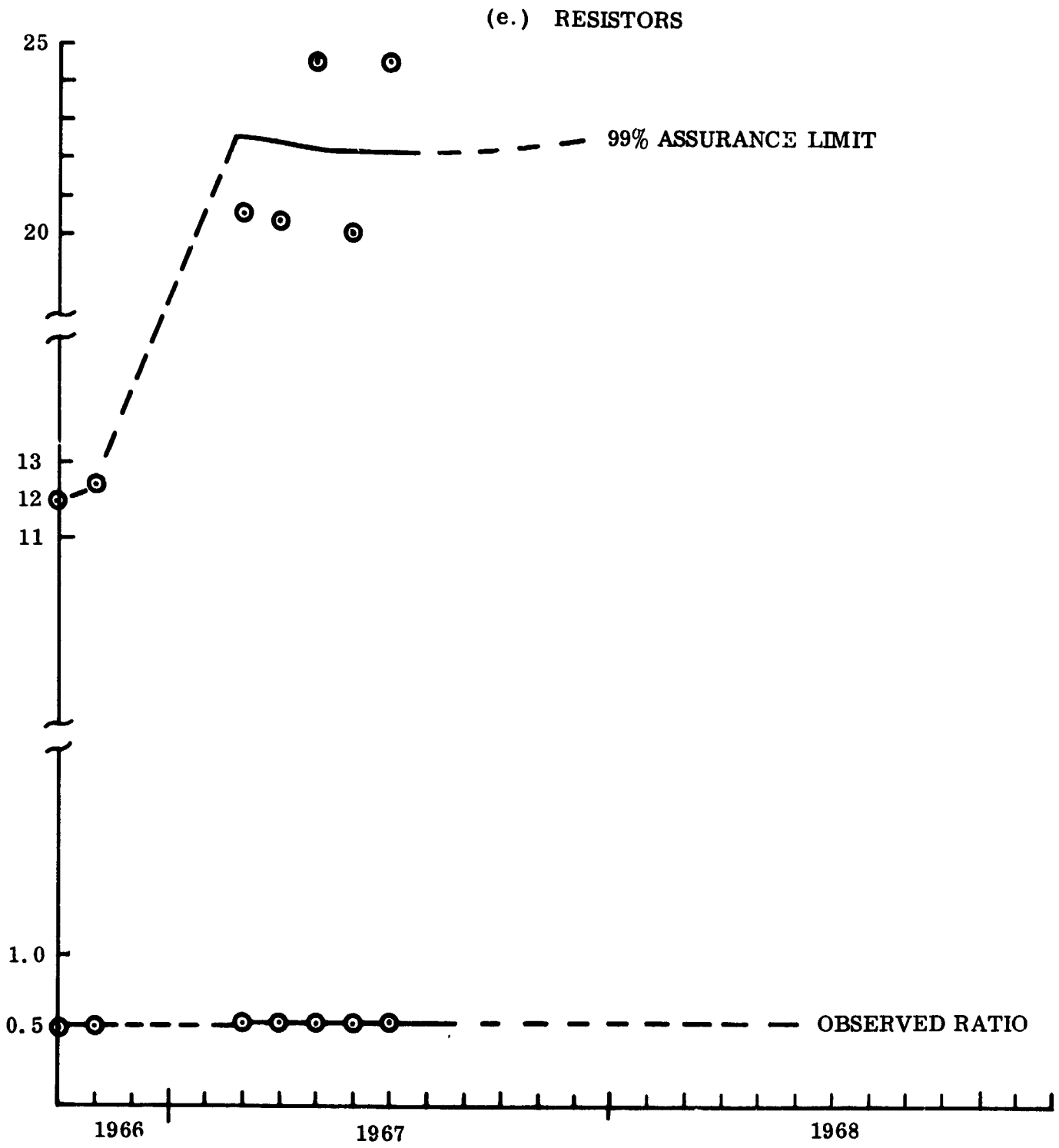


Figure 5. – Dormant/Normal Ratio Growth Curves (Sheet 5 of 5)

THEORETICAL CONSIDERATIONS OF MOS RELIABILITY

Part of this study was devoted to the development of a modeling technique whereby an estimate of MOS device failure rates could be made from known bipolar device failure rates. This technique was predicated upon process similarities producing equivalent failure mechanisms and, as such, left certain MOS-unique processes unaccounted. The purpose of this task is to ascertain, from a theoretical basis, the reliability aspects of these MOS-unique processes. The entire program has been directed towards the determination of the reliability improvement potential of placing the electronic equipment of a long-term, deep-space mission into some specific power mode when its operating capability is not needed.

Implications of Normal vs. Dormant Power

The ultimate objective of this study is the delineation of reliability-enhancing operational modes which might be utilized whenever a system or subsystem capability is not required. This condition will occur, for instance, during an appreciable portion of an unmanned, deep-space probe; also, the reliability of spare modules carried on a manned, long-term mission will benefit from this determination.

The several possible modes are: (1) maintain normal operating mode; (2) remove dynamic operation but retain static bias; (3) maintain dynamic operation but reduce static bias; (4) remove completely the power supply voltages. In view of the importance of computing circuitry, which generally requires a minimum bias level, the third condition will not be considered. The first condition will be referred to as normal power; the second, static power; the fourth, dormant power. The magnitude of the voltage sources is indeterminate, in each case. Under normal power, it may range to an arbitrarily small value, while dormant power is considered to be a special case of static power wherein all voltage supplies are adjusted to exactly zero volts.

These modes can be translated to fundamental quantities in terms of the device physics. That is, a given mode implies a certain distribution of electric field within the device, because of which certain currents flow, hence power is dissipated. These quantities may be time and circuit dependent. As before, our primary interest lies with logic circuitry; therefore, we neglect the effects on the device of self-heating. That this is valid may be demonstrated by the following reasoning. Logic circuitry is essentially an on-off operation; device dissipation in either state is low, provided that substantial, unwanted currents are not present. The power dissipated during the transition from state to state could be considerable, except that, in the case of MOS devices, impedance levels are quite high. The local temperature effects present at major junctions will have been accounted in the bipolar processes correlation model.

Implications of Operating Frequency

The effects on the device of operating frequency and duty cycle are two-fold. The first, power dissipation, has been discussed. The second is reducible to a consideration of the duration of a particular electric field distribution within the device. Therefore, this latter effect is considered to be a special case of the static and dormant power conditions.

Implications of Operating Temperature Environment

Temperature environment affects the devices in two ways. First is the variation of electrical characteristics with temperature. This is strongly influenced by the specific circuit configuration and rightfully belongs in the domain of the design engineer. The second is the affect of temperature on failure and degradation mechanisms. Some of these are unique to the MOS configuration and will be considered in subsequent sections of this report; some have been accounted in the process correlation model and will be considered only to the extent that some interaction exists with MOS-unique mechanisms.

The expected environment during a deep-space mission is a variable; therefore, some arbitrary limitations have been selected, viz. functional operation will be limited to ambient temperatures from 0°C to 100°C. (The ambient inferred is that of the device proper.) The non-operating temperatures still are limited by the materials used to fabricate the components. However, because reversible mechanisms are common in today's MOS technology, consideration will be given to specific non-operating temperature conditions wherever appropriate. Some additional reliability improvement might accrue during a manned flight wherein specific conditioning operations could be performed.

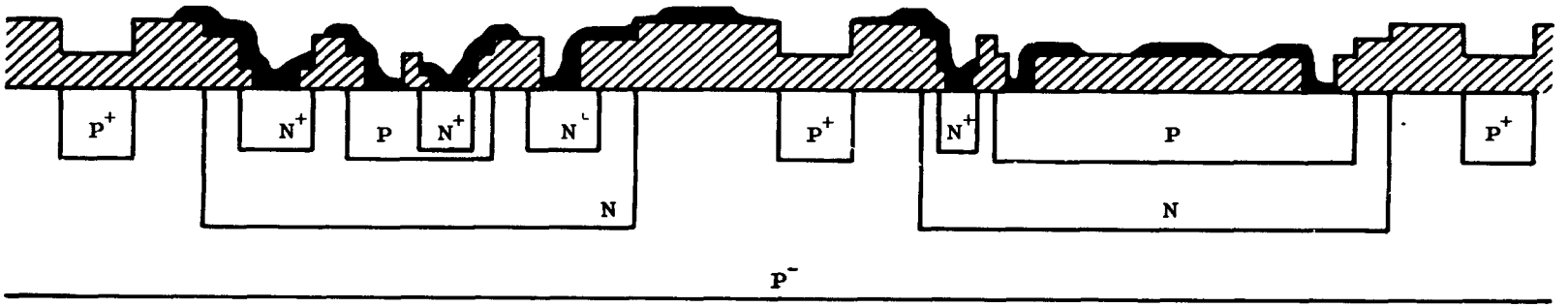
Failure Mechanisms In Oxide-Passivated, Planar Diffused Silicon Monolithic Circuits

A qualitative discussion of failure mechanisms is a prerequisite to identifying those that are either, (1) MOS-unique or, (2) produce effects in MOS devices which are significantly different than in bipolar devices. Reference will be made to Figure 6 which shows a section drawing of a typical triple diffused integrated circuit and a p-channel MOS circuit. (These drawings are purposely idealized and dimensionally exaggerated.) The functional equivalent of an active and passive component is shown for each configuration.

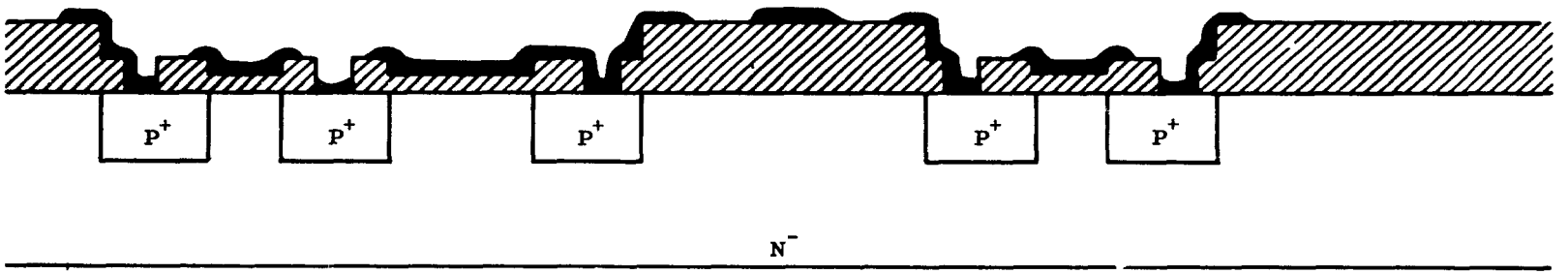
The MOS circuit has been specialized, somewhat, by the connection of the active load in the manner which is typical; that is, the MOS FET drain and "resistor" share a common diffused island. An interconnect, running perpendicular to the plane of the section, has been included for completeness.

Chemical Reactions. – Chemical oxidation, corrosion and anodic oxidation are included in this category. Reduction is generally not a problem. These processes are associated primarily with the metallization over the passivating layer and, since the materials and reagents used are similar, the physical effects will ultimately be the same in both configurations. However, galvanic corrosion can be expected to proceed at a slower rate in MOS circuits due to the generally lower current levels encountered.

Crystal Defects. – Frenkel, Schotky and impurity defects, dislocations, twin boundaries and stacking faults are included in this category. The emphasis on reducing these defects to increase component reliability has undergone a complete cycle. Initially, it was thought that defect-free starting material was a prerequisite to successful fabrication of reliable devices. Later, it was determined that defect reduction below a



a. Section through a triple diffused integrated circuit



b. Section through a P-channel MOS circuit

Figure 6. IC Cross-Sections

certain level did not materially improve the resultant device. During the process steps, notably high concentration diffusions, an even larger number of defects were introduced.

Defects in the starting material are now maintained below some arbitrary level primarily to reduce the incidence of spurious and enhanced diffusion in the bulk material which lowers fabrication yield. It has been known for some time that these defects tend to be nucleation sites and that surface oxidation, epitaxial deposition and diffusions encourage defect propagation inside the crystal and into the surface oxide or epi-layer. However, the correlation of these phenomena with long-term degradation processes has not been extensive.

Diffusion-induced defects should be greatly diminished in the MOS structure (Figure 6) since there is no need for multiple diffusions. This also removes the requirement for multiple compensatory doping used in fabricating bipolar IC's. Hence, the absolute impurity density may be much less in MOS. Neglecting other factors of design, a purer starting material would lead to greater reliability improvement in MOS than in bipolar devices. An extension of this reasoning must be deferred due to the constraints of the process correlation model which is based upon bipolar devices fabricated, typically, on <111> oriented slices, when evidence (Ref. 1) exists which indicates that a significant reduction of interface disorder is achieved with MOS devices fabricated on <100> oriented slices.

Surface Mechanisms. – Induced charge layers, undesired diffusion from the passivating oxide, metal and metal defect migration, structural defects and their propagation within the oxide, and electrical insulation defects are included in this category. During the past few years the greatest emphasis, by far, has been placed upon study and experiment involving the gate region of MOS structures. In the field of bipolar structures, renewed effort has been directed towards improvement of the electrical insulation properties of oxides, as well as the development of field control techniques. Thus, with the maturity of fabrication techniques, the never-ending quest for product improvement has broadened the common ground between the bulk and surface-effect technologies.

Oxide and Interface Charge. – With reference to Figure 6, it may be seen that less reliability degradation is inherent in the MOS structure due, primarily, to the smaller number of required processing steps. For instance, the probability of an oxide defect occurrence is only one-third that of the bipolar device, for unit oxide area. Metallization defects, such as thinning at oxide steps, will be reduced similarly. Metal and metal defect migration will be reduced in MOS circuits both because of the oxide step reduction noted, and also due to the lower current levels encountered. The probability of an oxide defect occurring under metallization away from active areas (such as the interconnect shown in Figure 6 perpendicular to the section place) would appear to be the same for bipolar and MOS circuits using comparable oxide thicknesses. Where metallization passes over an active region, termed a crossover, the probabilities of defect occurrence would again be equal for comparable oxide thicknesses. However, it should be noted that a reduced number of these sites is inherent in MOS circuits where the long resistor diffusions are not needed. (The exception occurs in X-Y matrix circuits where one crossover at each matrix element is required.)

Induced charge layers, while identical in origin, affect a MOS circuit quite differently and more adversely than a bipolar circuit. Likewise, the treatments in each case,

while similar, produce decidedly different effects. It has been well established that silicon-silicon oxide interface will contain a density of states which are always donor states, although the magnitude depends upon the specific fabrication process; therefore, the tendency to invert a p-region always exists. This is troublesome in the higher resistivity regions and it has become common to diffuse a heavily p-doped barrier (channel stopper) to prevent its spread to adjacent regions. (One such channel stopper is shown in Figure 6 (a). between the bipolar transistor and the adjacent resistor tub. Typically, a channel stopper surrounds all active regions in p-substrates, as well as the base regions of most NPN transistors.) This technique is useful for p-substrate MOS circuits, also, but of course has no applicability to the gate region. The termination of an induced-charge layer prevents conduction paths from shorting a useful junction, but the layer remains in parallel and its characteristics may determine the behavior of the combination rather than the desired bulk properties. A useful remedy for bipolar circuits has been to apply field control measures which take the form of metallization areas close to and surrounding a junction edge. Leakage currents and breakdown voltages quite close to the theoretical values for the bulk alone, have been achieved.

The true dichotomy in bipolar and MOS devices is therefore apparent. Induced charge layers in the MOS configuration cannot be merely subordinated to some other property, but rather must be reliably and reproducibly formed during the device fabrication. A significant portion of the next section is devoted to the reliability aspects of induced charge in a MOS gate region.

Physics of Storage Modes

In the preceding sections we have seen that a MOS device can be inherently more reliable than a comparable bipolar device and that this is due to the considerable reduction in fabrication complexity. Also, it was shown that there existed no fundamentally unique failure mechanisms in a MOS device but, rather, that the effects of some mechanisms are significantly different and, therefore, that the action taken to retard these mechanisms is unique. The purpose at hand, then, is to examine these mechanisms with respect to the electric fields and currents defined by the three storage modes; normal power, bias power and dormant power.

Chemical Reactions. – The chemical oxidation and/or corrosion rate of metals on the passivating surface is temperature dependent. A second order dependency upon localized hot spots, caused by a high current density, may exist; therefore, interrupting the current flow will retard the degradation. The presence of an electric field will have no effect.

Anodic oxidation and galvanic corrosion require only that the electrochemical cell exist with a closed current path, but the rate can be greatly modified by the potential applied on the metals by the bias voltages. The worse case would be a rate increase and, since the current path cannot be interrupted, the removal of bias voltages will at least ensure not aggravating the problem.

Migrating voids within the metallization coalesce which ultimately results in an open interconnect. The mechanism (Ref. 2) is current density dependent and non-reversible, so that a reduction of the current levels will prolong the time to failure.

Crystal Defects. – In the preceding discussion it was stated that the correlation of crystal defects with device failure has not been extensive. The enhanced diffusion and precipitation tendencies were noted, and it was pointed out that defects introduced during crystal processing as well as the modifying influence on original defects are far more significant relative to device reliability. These effects are predominantly concerned with the silicon surface and interface and are considered as surface mechanisms.

The severity of a region of enhanced diffusion or of a precipitation center is a function of its location relative to junctions in the bulk, and are strongly dependent upon crystal orientation. Degradation of device characteristics depends heavily upon elevated temperatures and, except as a high current density were to be incurred, are not advanced by operational mode.

Surface Mechanisms. – Defects within the surface oxide which affect its electrical insulation properties occur only under metallization regions. In the degradation phase, the electronic field at the site is highly distorted and usually enhanced, thereby encouraging the migration of metal and ionized specie into the defect. This process is field (and temperature) sensitive and is cumulative. During the breakdown phase the mechanism is dependent upon the energy available at the site, resulting in some cases in an ohmic connection through the oxide and in other cases in dielectric self-healing. Since it is unlikely that sufficient energy will be available at all possible sites, the removal of all applied potentials is preferred.

Surface contamination in the form of mobile or potentially mobile charge is one of the more serious degradation mechanisms operating in MOS systems. A number of reports* have been published, all substantiating the free ion/cation model, and the reader is referred to these for a detailed analysis. The conditions which cause the charge segregation are fringing fields of metallization layers and junctions which terminate at the silicon-oxide interface. The mechanism is enhanced by the presence of moisture or organic molecules of large dipole moment.

The net effect of the segregation of mobile charge on the oxide surface is to establish an electric field which may reach to a neighboring device or through the oxide into the silicon substrate. The former effect introduces a static coupling between elements of the circuit; the latter effect can regenerate itself by inducing "mirror" charge at the silicon-oxide interface with the result that an external influence is required to reduce the field. The precise time span involved in these processes is a function of the field strength, charged specie mobility, oxide thickness, substrate doping level, etc.; many values of accumulation/decay times have been reported, ranging from sub-seconds to hours. The surface charge mechanisms is primarily one of fabrication control, but it is quite conceivable that sufficient moisture, ionizing radiation or other contaminates could accumulate so that the problem would arise. In that case, only a long duration, zero applied voltage condition would permit an equilibrium distribution to be achieved.

Oxide and Interface Charge. – A considerable body of literature reporting investigation of oxide-based MOS instability has appeared during the past several years. In most cases the investigations were directed towards a particular type of instability and only recently has it been apparent that several mechanisms were operating simultaneously. The complexity of the silicon-oxide system in this respect is inferred in

*Reference 1 contains a quite complete bibliography through early 1966.

Figure 2, which shows a charge model developed by Schlegel (Ref. 1). The effects of the various charges may be divided into two categories: (1) those which change the device characteristics during its lifetime and, (2) those which determine the initial characteristics of the device. The latter effect, which is not of concern to this study, generally is reflected in a spread of gate threshold values.

Those charges which contribute to instability during the lifetime of the device include mobile alkali ions, hydrolyzed water (Ref. 4) and trapping states. These charges manifest themselves as a flat-band voltage shift (parametrically, gate threshold voltage charge) following exposure to some elevated temperature while an electric field exists within the oxide. Subsequent exposure to elevated temperature in the absence of an applied potential permits the mobile charges to redistribute, except that charge held at a trap site will empty at a rate also dependent upon the potential at the site.

The effect of an applied voltage will be opposite that of mobile positive specie for donor traps but will be the same for acceptor traps. However, the effect of trapping sites on the silicon is weaker than that of mobile charges. This situation is further complicated by the current practice of "stabilizing" the oxide with a phosphosilicate glass. This has been shown, variously, to getter (Ref. 5) the mobile sodium ions, and to creat a barrier (Ref. 6) to subsequent ion diffusion. The exact mechanism responsible for the stabilization is of some importance due to several second order effects. The first effect is the tendency for the phosphosilicate phase, itself, to polarize and contribute to silicon surface instability (Ref. 7). The second effect is dependent upon the location of the phosphosilicate phase layer relative to the silicon surface. That is, ample evidence exists to show that the sodium tends to accumulate near the silicon oxide interface (within 10Å - 1000Å) but that a considerable percentage is not ionized. Finally, the diffusion of phosphorous to the interface introduces the possibility of additional surface potential charge.

It now appears that, with so many variables unspecified, the only plausible storage mode which will not adversely affect the oxide and interface charge is one of zero applied potential. Since elevated temperature encourages redistribution of charge to the original equilibrium condition, this particular degradation is reversible.

Optimum Storage Mode Determination

The storage modes suggested in the preceding section are itemized as follows:

Chemical oxidation/corrosion - dormant (*static)

Anodic oxidation - dormant

Metal void migration - dormant (*static)

Crystal defects - dormant

Oxide defects - dormant

Surface contamination - dormant

Oxide and interface charge - dormant

The two static power entries, shown in parenthesis with an asterisk, are suitable only with time-volatile circuitry. Neglecting this case, complete removal of all power input to the circuitry is clearly favored. Other combinations of input power and frequency do not effect an appreciable reliability enhancement beyond that attributable to a reduction of power dissipation.

RELIABILITY TRANSFER MODEL

Model Concept

The methodology used for the reliability transfer model is similar to that used during the transistor to integrated circuit transition of Minuteman I to Minuteman II. Through correlation and similarity of manufacturing processes of bipolar and MOS technologies and failure rate by failure mode data on bipolar integrated circuits (full power condition), the reliability transfer model concept was formulated.

A detailed analysis of bipolar and MOS IC fabrication shows the following relationships to exist.

1. Both IC types are formed on silicon chips.

2. Aluminum is used as the metallization layer for interconnections for both device types.

3. The masking, etching and diffusion processes are common to both bipolar and MOS device technologies except for the number of times any one of these processes is performed in the fabrication of a single device.

4. Silicon dioxide (SiO_2) is used for the insulation layer in both technologies.

5. Lead attachment by thermocompression or ultrasonic bonding is common to both device types.

The main differences between bipolar and MOS device fabrication are in the number of times a given process is performed (such as diffusion), and the area of the chip affected by a given process (such as area under metallization).

Due to the commonality between the two technologies the known integrated circuit failure modes shown in Table VII also apply to MOS devices.

The units shown for failure modes 1 - 5 have been normalized to either a function of area involved, the number of bonds, or the number of times a process is performed. The remaining failure modes 6 through 9 are substantially less dependent on the size or complexity of the circuit.

The following information is needed about any given MOS device so that the transfer model described above can be utilized.

1. A list of the fabrication processes used showing number of times each step is performed.

2. Aluminum interconnect area.

3. Number of bonds.

4. Number of active elements per device.

TABLE VII

FAILURE MODES COMMON TO BIPOLAR AND MOS

Analogous Failure Modes	Failure Rate Units
1. Oxide layer	%/1000 hr/1000 sq. mils of device area
2. Lead bond	%/1000 hr/per bond
3. Metallization	%/1000 hr/1000 sq. mils under metallization
4. Internal lead discrepancy	%/1000 hr/bond
5. Faulty diffusion	%/1000 hr/diffusion
6. Foreign material	%/1000 hr
7. Die - header bonding	%/1000 hr
8. Surface defect	%/1000 hr
9. Crystal imperfections	%/1000 hr

A series relationship between failure modes was used which allows failure rates to be added.

Bipolar IC Fabrication Data

Figure 7 is an outline of a typical bipolar integrated circuit process flow chart. The base material of a bipolar integrated circuit is a silicon chip ranging in size from 2000 sq mils (903 gate) to 7000 sq. mils (901 flip-flop). Resistors are formed by linear diffusions within the silicon chip with resistor line width ranging from 0.5 to 1.5 mils; resistive diffusion ranges between 100 and 500 ohms per square. Capacitors for the Minuteman II bipolar monolithic IC's are primarily junction type with capacitance per unit approximately 0.1 pf/mil^2. Transistor size lies between 65 and 100 sq. mils, and diode size ranges from 35 to 50 sq. mils(excluding isolation diffusion). Emitter current density appears to range between 0.1 and 0.5 ma per sq. mil. Table VIII is a process breakout of a general element diffusion process used in IC fabrication. Shown in this chart are the steps involved in the diffusion process, critical results of each process step, and device properties affected by the process. Table IX is a process breakout chart of a double diffused, single epitaxy IC fabrication process. Table X is a glossary of terms and symbols used to denote the element parameter of an integrated circuit.

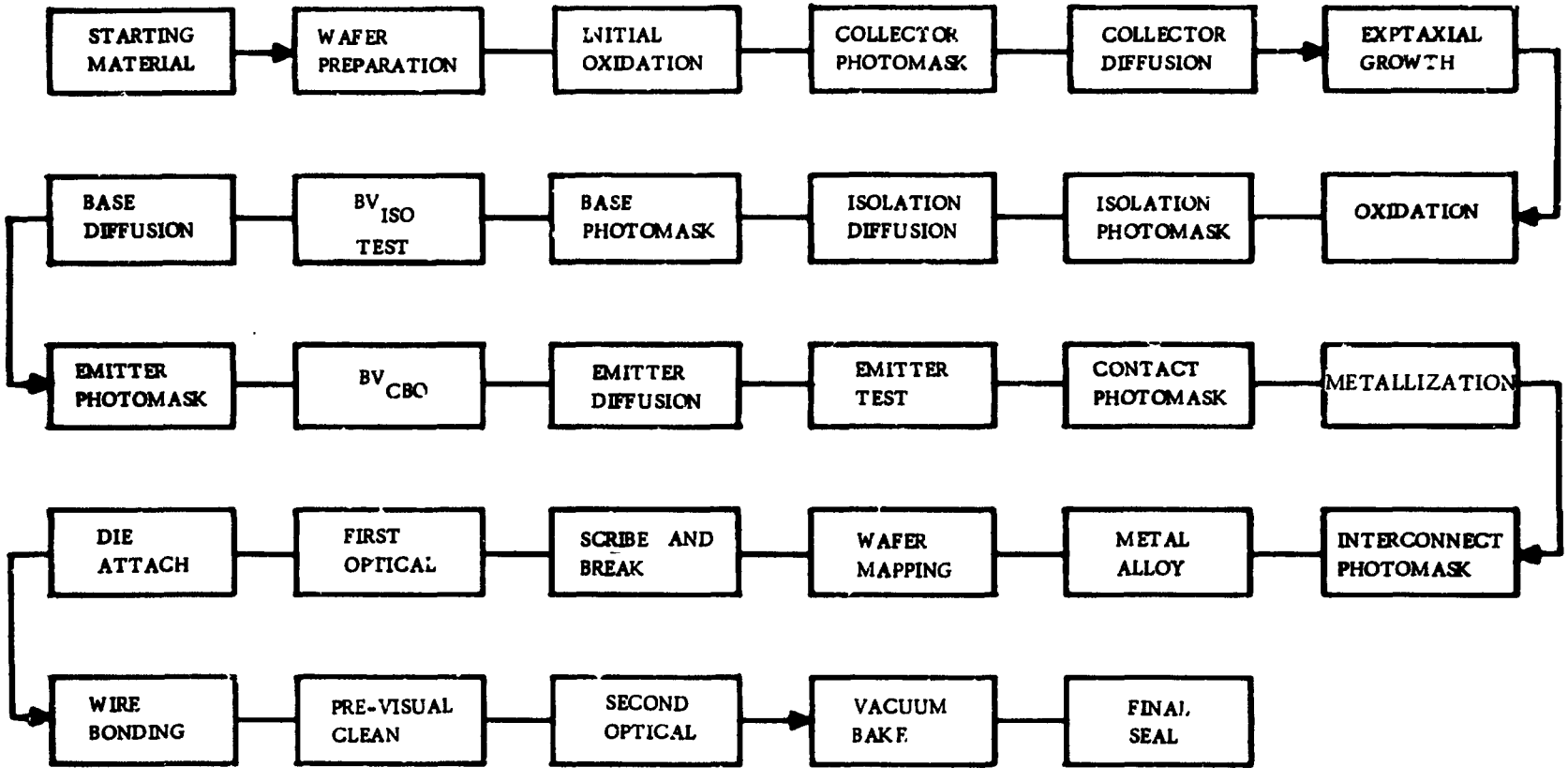


Figure 7. - Typical Bipoloar IC Manufacturing Process Flow Chart

TABLE VIII
BIPOLAR IC ELEMENT DIFFUSION PROCESS

Step No.	Process Step	Critical Results	Device Properties Affected	Related Failure Modes	Element Parameters Affected
1	Base photo-mask and oxide etch	a. Registration Accuracy	Improper registration may result in emitter-to-collector shorts. May also result in collector-to-base shorts after metallization.		BV_{CEO} (shorts) BVCBO (shorts)
		b. Line width	Resistance values		R (spread)
		c. Removal of all oxide in windows	Incomplete removal will affect base and resistor diffusions	Collector-emitter spikes will be enhanced by a shallow base (Refer to 4-b)	R (High) BV_{CEO} (shorts) h_{FE} (High)
2	Base diffusion and oxide regrowth	a. Resistivity (doping concentration)	Emitter-to-base breakdowns		BV_{EBO} (spread)
		b. Junction depth (and regularity)	(a) If too shallow resistances will be high, collector-emitter characteristics will be affected	Collector-emitted spikes will be enhanced by a shallow base (Refer to 4-b)	R (High) BV_{CEO} (short) h_{FE} (High)
			(b) If too deep, collector-base breakdown will be affected, resistances low		BV_{CBO} (low) R (low)

TABLE VIII (CONT)

Step No.	Process Step	Critical Results	Device Properties Affected	Related Failure Modes	Element Parameters Affected
2 (Cont)		c. Surface conditions	Surface recombination, surface stability	Surface-dependent parameters may degrade under thermal-electric stresses	h_{FE} (at low current) low BV_{CEO}/ I_{CEO} (low/high) I_{ECO} (high)
		d. Oxide thickness	No effect		
		e. Pinhole density	Subsequent metallization may fill pinholes and make contact with base regions	Such shorting may occur only after temperature stresses have been applied	BV_{CBO} BV_{EBO} (shorts)
3	Emitter mask and photo-oxide etch	a. Registration accuracy	Misregistration may result in emitter-to-collector shorts. May also result in emitter-base shorts after metallization		BVCBO (shorts) BV_{EBO} (shorts)
		b. Removal of all oxides in windows	Emitter diffusion - incomplete emitter will effect emitter-base voltage		V_{BE} (high)
4	Emitter diffusion and oxide regrowth	a. Resistivity (doping concentration)	Emitter efficiency, OHMIC contacts		BV_{EBO} (spread)

TABLE VIII (CONT)

Step No.	Process Step	Critical Results	Device Properties Affected	Related Failure Modes	Element Parameters Affected
4 (Cont)		b. Junction depth (and regularity)	(a) Shallow diffusion-wide base width, low mid-range beta		h_{FE} (at midrange) (low)
			(b) Deep diffusion - narrow base width, high mid-range beta, emitter - collector punch through	·rów base region ..ances the effect of emitter and base junction irregularities may cause emitter-to-collector shorts. Such shorting may occur after application of thermal/ electric stresses.	h_{FE} (at midrange) high BV_{CEO} (short)
		c. Surface conditions	Oxide over the base regions may be significantly altered during this step with the result that surface stability is affected.	Surface-dependent parameters may degrade under application of thermal/electric stresses (base-inversion, channeling)	h_{FE} (at low current) BV_{CBO}/ I_{CBO}, BV_{CEO}/ I_{CEO}, (low/high), I_{ECO}(low)

TABLE VIII (CONT)

Step No.	Process Step	Critical Results	Device Properties Affected	Related Failure Modes	Element Parameters Affected
4 (Cont)		d. Oxide thickness	Too thin an oxide may result in inadequate emitter - base junction protection	Emitter inversion or channeling may occur, particularly in the presence of surface contamination and under thermal/ electric stresses	BV_{EBO}/ I_{EBO} (low/high)
		e. Pinhole density	Unless diffused cross-unders are used, metallized circuitry from other areas of the circuit do not cross over the emitter oxide. If such is the case, however, pinholes in the oxide can cause shorts to the emitter	Such shorting may occur only after application of thermal stresses	BV_{CEO} (shorts)
5	Metallization photomask and oxide etch	a. Registration accuracy	Misregistration may result in placing contacts over junction areas and off of resistor ends.		BV_{CBO} BV_{CIO} BV_{EBO} (shorts) R (high or open)
		b. Etched pinholes	Etched pinholes may allow metallization to come into contact with active areas	Shorts may not occur until after application of thermal stresses	BV_{XYO} (shorts) (X and Y:

TABLE VIII (CONT)

Step No.	Process Step	Critical Results	Device Properties Affected	Related Failure Modes	Element Parameters Affected
5 (Cont)		b. (Cont)			collector, base, emitter, resistor, substrate
		c. Removal of all oxide from windows	Metallization contact resistance will be increased		V_{CE}(sat) (high) V_{BE}(high) R (high)
		d. Surface contamination	Stability of surface-dependent parameters may be affected.	Surface inversion, channeling or accumulation may occur after application of thermal/electric stresses	BV_{CBO}/ I_{CBO}, (low/high) BV_{CEO}/ I_{CEO} (low/high) I_{ECO}(high)
6	Metallization	a. Reaction between the metal and the silicon SiO_2	OHMIC Contact to the elements and adherence of the metal film to the die.	Adherence of the metal film to the die may affect the wire bond strength. Internal opens may occur as a result of mechanical and/or thermal stresses	V_{CE}(sat), V_{BE}, ΔV_{BE} (spread) BV_{xyo} (opens)

TABLE VIII (CONT)

Step No.	Process Step	Critical Results	Device Properties Affected	Related Failure Modes	Element Parameters Affected
6 (Cont)		b. Film continuity (discontinuities, nonmetalled areas, pinholes	Discontinuities may affect interconnect continuity. Voids in pad areas may affect subsequent wire bonding.	Interconnects with incomplete cross section may result in localized hot spots under operating conditions; opens may result	BV_{xyo} (open)
		c. Contamination	Stability of surface - dependent parameters may be affected. Wire bonding may be affected.	Surface inversion, channeling, or accumulation may occur after application of thermal/electric stresses. Wire bonds may open under mechanical and/or thermal stresses	BV_{CBO}/ I_{CBO} (low/high) BV_{CEO}/ I_{CEO} (low/high) I_{BCO}(high) h_{FE}(at low current) low BV_{xyo} (open)
7	Interconnect mask and metal etch	a. Registration accuracy	(a) Element contact areas may be reduced if mask is incorrectly aligned. Contact resistances may be high or open.	Marginal contacts may open under application of power	V_{CE}(sat) V_{BE} R (high) BV_{xyo} (open)

TABLE VIII (CONT)

Step No.	Process Step	Critical Results	Device Properties Affected	Related Failure Modes	Element Parameters Affected
7 (Cont)		a. (Cont)	(b) Elements may be shorted together if metallization is offset and contacts more than one element contact area.		BV_{xyo} (short
		b. Line definition	(a) Voids may occur in interconnect metallization, contact areas, and/or pad areas	Interconnects with incomplete cross sections may result in localized heating and opens may result. Wire bond strength may be affected. Internal shorts may occur as a result of mechanical and/or thermal stresses	BV_{xyo} (open) V_{CE}(sat) V_{BE}, R (high) ΔV_{BE} (spread)
			(b) Interconnects may not be completely separated	Narrow spacing may result in arcing between interconnects under operating stresses	BV_{xyo} (short)
		c. Contamination	Stability of surface-dependent parameters may be affected. Wire bonding may be affected	Surface inversion, channeling, or accumulation may occur after application of thermal/electric stresses. Wire bonds may	BV_{CBO}/ I_{CBO} (low/high)

TABLE VIII (CONT)

Step No.	Process Step	Critical Results	Device Properties Affected	Related Failure Modes	Element Parameters Affected
7 (Cont)		c. (Cont)		open under mechanical and/or thermal stresses	BV_{CEO}/ I_{CEO} (low/high) I_{ECO}(high) BV_{xyo}(open)

TABLE IX
BIPOLAR IC FABRICATION PROCESS

Step No.	Process Step	Critical Results	Device Properties Affected	Related Failure Modes	Element Parameters Affected
1	Starting material (purchased)	a. Resistivity and type	Saturation voltages and breakdown voltages		$V_{CE}(SAT)$ BV_{CBO}
		b. Crystal orientation	No significant effect at this point		
		c. Flatness	No effect		
		d. Size	No effect		
		e. Oxygen content	Compensated material usually exhibits lower mobility, thus affecting switching speeds		tsw
		f. Lifetime			
2	Wafer preparation	a. Surface finish	Surface damage will result in poor quality "EPI" (Step 9); can result in excessive "PIPES" and surface problems	Collector - base insulation irregularities, breakdowns, leadage may degrade under thermal-electrical stress	BV_{CEO} / I_{CEO} BV_{CBO} / I_{CBO}
		b. Surface cleanliness	No effect		
		c. Dimensions	No effect		

TABLE IX (CONT)

Step No.	Process Step	Critical Results	Device Properties Affected	Related Failure Modes	Element Parameters Affected
3	a. Oxide Thickness	No effect			None
	b. Pinhole density	No effect			
	c. Contamination	No effect			
4	Subcollector photomask and oxide etch	a. Reproduction of pattern to allowed tolerances	Improper location will affect subcollector position		V_{CE}(SAT) (High and spread)
		b. Removal of all oxide in windows	Incomplete removal will affect subcollector diffusion		
5	Subcollector diffusion and oxide regrowth	a. Doping concentration	Subcollector resistivity		V_{CE}(SAT SPREAD)
		b. Oxide and surface properties	Properties of subsequent "EPI" layer		

TABLE IX (CONT)

Step No.	Process Step	Critical Results	Device Properties Affected	Related Failure Modes	Element Parameters Affected
6	Isolation photomask and oxide etch	a. Registration accuracy	Gross errors will cause isolation regions to contact the subcollector, thereby reducing the collector-substrate breakdown voltage		BV_{CIO} (Spread)
		b. Removal of all oxide in windows	Incomplete removal will affect isolation diffusion operation		BV_{CCO}(low) I_{CCO}(high)
7	Isolation diffusion	a. Resistivity (doping concentration)	Grossly inadequate doping can result in incomplete isolation		BV_{CCO}(low) I_{CCO}(high)
8	Oxide removal	a. Complete removal of oxide	Incomplete removal of oxide or surface contamination will result in poor quality "EPI", pinholes, "PIPES"	Collector - base insulation irregularities, breakdowns and leakages may degrade under thermal-electric stress	BV_{CEO}/ I_{CEO} BV_{CBO}/ I_{CBO}
		b. Contamination			
9	Epitaxial layer growth	a. Thickness	a. Too thin a layer may result in the base being diffused into the n^+ subcollector		BV_{CBO}(low)

TABLE IX (CONT)

Step No.	Process Step	Critical Results	Device Properties Affected	Related Failure Modes	Element Parameters Affected
9 (Cont)		a. (Cont)	b. Too thick a layer may result in incomplete isolation and/or high saturation resistance		BV_{CCO} (spread) $V_{CE}(SAT)$ high
		b. Resistivity (doping concentration)			$V_{CE}(SAT)$ high
		c. Imperfection density	Subsequent processing may produce defective junctions or "PIPES". Surface combination or other surface problems may result.	Metalization to substrate sheets may occur through pinholes. Thermal-electric stresses may cause instability in surface-dependent parameters	BV_{XSO} shorts I_{CBO}, I_{CEO}, I_{ECO} (increase) h_{FE} (at low current low) (decreases)
10	Oxide growth and isolation np diffusion	a. Oxide thickness	No effect		
		b. Pinhole density	Subsequent metalization may fill pinholes and make contact with collector or substrate regions	Shorting may occur only after temp stresses have been applied	BV_{CEO}, BV_{CBO}, BV_{CCO}, BV_{XIO} } shorts

TABLE IX (CONT)

Step No.	Process Step	Critical Results	Device Properties Affected	Related Failure Modes	Element Parameters Affected
10 (Cont)		c. Contamination	Collector junction properties	Breakdowns and leakage current may degrade under thermal-electric stresses	BV_{CBO}/ I_{CBO} BV_{CEO}/ I_{CEO}
		d. Distance of upward penetration of isolation channels	Inadequate upward diffusion will result in incomplete isolation, collector-collector shorts.		BV_{CCO} shorts
11	Base photomask and oxide etch	a. Registration accuracy	Isolation channel in base mask must register with previous isolation channel to produce complete isolation.		BV_{CCO} (spread) BV_{CEO} (short)
		b. Line width	Resistance values		R (spread)
		c. Removal of all oxide in windows	Incomplete removal will affect base and resistor diffusions and diffusion depths.	Collector-emitter spikes will be enhanced by a shallow base.	R (high) BV_{CEO} (short) h_{FE} (high)

TABLE IX (CONT)

Step No.	Process Step	Critical Results	Device Properties Affected	Related Failure Modes	Element Parameters Affected
12	Base diffusion and oxide regrowth	a. Resistivity doping concentration	Emitter to base breakdown		BV_{EBO} (spread)
		b. Junction depth	(a) If too shallow, isolation will be incomplete, resistance high; collector-emitter characteristics will be affected.	Collector-emitter spikes will be enhanced by a shallow base.	BV_{CCO} (short) R (high) BV_{CEO} (short) h_{FE} (high)
			(b) If too deep, collector-base breakdown will be affected and resistances low.		BV_{CBO} (low) R (low)
		c. Surface conditions	Surface recombination, surface stability.	Surface-dependent parameter may degrade under thermal-electric stresses	h_{FE} at low current (low) BV_{CBO}/I_{CBO} BV_{CEO}/I_{CEO} I_{ECO}
		d. Oxide thickness	No effect.		
		e. Pinhole density	Subsequent metallization may fill pinholes and make contact with base or isolation regions.	Shorting may occur only after temperature stresses have been applied.	BV_{CBO}, BV_{EBO} BV_{XIO}, (shorts)

TABLE X
GLOSSARY OF TERMS AND SYMBOLS

I_{ECO}	Leakage Current	Emitter to collector (collector grounded) with the base open
BV_{CIO}	Breakdown Voltage	Collector to isolation region, with the other terminals open
IC_{CIO}	Leakage Current	Collector to isolation region, with the other terminals open
t_{sw}	Switching Times	(Includes delay, rise storage and fall times)
BV_{XLO}	Breakdown Voltage	Any single transistor terminal (collector, base or emitter) to the isolation region, with the remaining terminals open (e.g., BV_{CIO}, BV_{BIO} BV_{EIO})
BV_{XSO}	Breakdown Voltage	Any single transistor terminal to the substrate, with remaining terminals open
BV_{XYO}	Breakdown Voltage	Between any 2 transistor terminals with the remaining terminals open (e.g., BV_{CBO} BV_{CEO})
BV_{CCO}	Breakdown Voltage	From the collector of any transistor to the collector of any other transistor (usually adjacent) with the remaining terminals of the two devices open
I_{CCO}	Leakage Current	Same as BV_{CCO}
BV_{ISO}	Breakdown Voltage	Of the isolation region; used synonymously with BV_{CIO}
I_{ISO}	Leakage Current	Of the isolation region; used synonymously with I_{CIO}
g_m	Transconductance	
h_{FE}	Forward current gain	
R	Resistance	

MOS IC Fabrication Data

Figure 8 is an outline of a typical MOS integrated circuit process flow chart.

A typical digital MOS Array is a single p-type in an n-type substrate with a minimum active gate area for a single device of 0.4 mils sq. P-regions in a MOS Array are on approximately 1 mil centers. Adjacent devices on the same p-regions have been spaced as closely as 1.2 mils, but 3 mils is more typical. Metal interconnect line spacing is approximately 1 mil. Resistive elements are formed in the same manner as the MOS transistors and diodes, with the g_m made lower by a factor of 10 and with the gate tied to the drain. Capacitors are fabricated with a thin (1000 Å) silicon dioxide dielectric sandwiched between the silicon substrate and a layer of aluminum. The average surface area per device ranges from 15 to 60 sq mils per MOS device, including all vacant area between devices. The power dissipation per device (excluding output) is typically about 4 microwatts. A typical MOS device uses 38 fabrication processes, 5 masks, and 1 diffusion in its construction; whereas an average IC requires 130 fabrication steps, 6 masks, and 4 diffusions. The MOS device described above using 38 processes will functionally replace 100 of the 130 process step integrated circuits.

Table XI shows the geometry of several different MOS-FET's used in MOS arrays. The various gate metal overlap configurations shown in Table XI for FET's have different yields, threshold voltages, and g_m (transconductance).

TABLE XI
MOS-FET GEOMETRY

FET Number	Type**	Gate Metal Overlap*		Total Gate Metal Area*	Gate Metal Over P Region of Drain and Source*
		"X"	"Y"		
1	1 × 1	0.2	0.15	0.8 × 0.7	2 (0.4 × 0.15)
2	1 × 1	0.15	0.15	0.7 × 0.7	2 (0.4 × 0.15)
3	1 × 1	0.15	0.2	0.7 × 0.8	2 (0.4 × 0.2)
4	1 × 1	0.2	0.1	0.8 × 0.6	2 (0.4 × 0.1)
5	1 × 1	0.1	0.1	0.6 × 0.6	2 (0.4 × 0.1)
6	1 × 1	0.1	0.2	0.6 × 0.8	2 (0.4 × 0.2)
7	1 × 1	0.2	0.2	0.8 × 0.8	2 (0.4 × 0.2)
8	1 × 2	0.2	0.2	0.8 × 1.2	2 (0.4 × 0.2)
9	2 × 2	0.2	0.2	1.2 × 1.2	2 (0.8 × 0.2)
10	1 × 3	0.2	0.2	0.8 × 1.6	2 (0.4 × 0.2)

*All dimensions in mils.
**1 × 2 indicates the active gate area is 0.4 mil wide by 0.8 mil long.

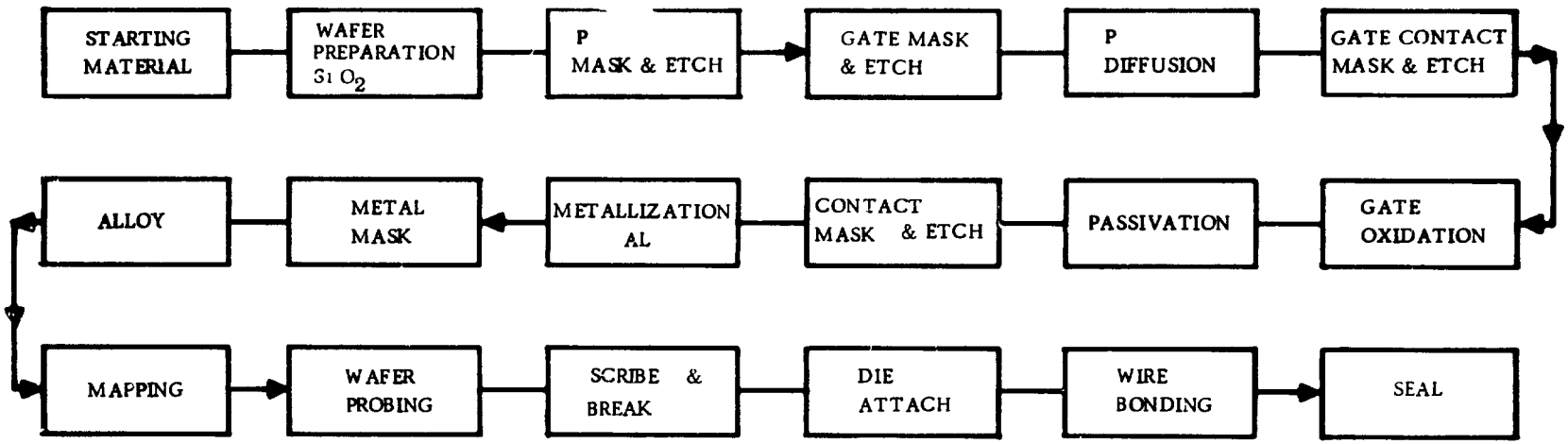


Figure 8. - Typical MOS IC Manufacturing Process Flow Chart

Comparison of Bipolar and MOS IC's

Both bipolar and MOS device types are formed on silicon chips and both employ aluminum as the metallization layer for interconnections. Silicon dioxide (SiO_2) is used for the insulation layers in both technologies. A general comparison of the masking, etching, and diffusion processes used for both device types shows that they are common to both technologies. Leads are attached to the chip by thermocompression or ultrasonic bonding in both integrated circuit and MOS device fabrication. Gold wires were used between the case and substrate in early Minuteman IC's and are sometimes used in present-day MOS arrays. This leads to an intermetallic problem of oxide formation, causing the bonds to become brittle. This is a known failure mode of IC's and in later Minuteman IC's has been changed to monometallic bonding (gold-to-gold or aluminum-to-aluminum) to eliminate this problem. Package sealing processes are basically the same for both technologies except for the size and number of external leads. For integrated circuits 12-16 external leads are typical, where a MOS device will have up to 40.

Epitaxial growth is a unique process used only in the fabrication of some bipolar IC's and is not used at all in the fabrication of MOS devices. Present Autonetics data indicate that the oxide pinhole defects at the gates of MOS devices are very critical. Voltage instability and radiation are two failure modes that require special consideration in MOS devices and cannot be determined from IC data.

Table XII lists some quantitative comparisons between bipolar IC and complex MOS circuit technologies with complexity factors assigned.

Bipolar IC Failure Rate by Failure Mode

The failure frequency and the failure rates shown in this section are based on Minuteman II IC achieved data. There have been 1481 reported failures on Minuteman II integrated circuits made by manufacturer A for which 1, 290, 000, 000 operational device hours have been recorded as of 1 April 1967.

The failure mode failure rates shown in Table XIII are based on field operational hours and include all failed integrated circuits, both in-house and field. This yields a much higher integrated circuit failure rate than using only assessed primary field failures such as in Tables III, IV, V, and VI. The total population of failures was used for the following reasons: Minuteman II in-house screen tests include (a) before build up, (b) during build up, (c) module functional test, and (d) system burn-in test. These screen tests find an extremely large number of failed parts. To calculate failure rates for individual failure modes these failures have to be included to determine the true failure mode frequency distribution.

All MOS device failure rates predicted in this section are applicable only in a benign environment (25°C and 50 percent of rated electrical stress). This condition exists because the Minuteman II data used to calculate the MOS device failure rates are based on a benign environment.

TABLE XII
BIPOLAR VS. MOS IC CHARACTERISTICS

	I/C	Factor	MOS
Oxide thickness under metallization	3500 - 20,000Å	1.2	10,000 - 20,000Å
Oxide thickness at gate	(not applicable)	3.0	1,000 - 1,500Å
Field intensity across oxide under metallization	3×10^5 volts/in	1.0	3×10^5 volts/in
Field intensity across oxide at gate	(not applicable)	1.0	3 to 10^6 volts/in
Number of epitaxial layers	0 or 1	0.0	0
Number of diffusions	3 or 4	0.25	1
Number of oxide growth	4 or 5	0.75	3
Number of masking/etching operations	5 or 6	0.85	5
Number of metallization depositions	1	1.0	1
Metallization thickness (approximate)	1 micron	1.0	1 micron
Minimum number of steps in metallization layer - collector/ drain lead	1	1.0	1
Minimum number of steps in metallization layer - base/ gate lead	2	1.0	2
Minimum number of steps in metallization layer - emitter/ source lead	3	0.33	1
Effective chip area per diode/ transistor (excluding isolation)	35 to 100 sq. mils	0.1	3 to 10 sq. mils

Two failure modes, radiation and gate oxide pin holes, were investigated since there is little or no correlation that can be drawn from bipolar IC data concerning these two failure modes. Radiation on MOS devices affects the bulk conductivity of the devices and especially the surface-state density. Present day devices fail due to surface effects long before the bulk conductivity is greatly affected. A data search was conducted to determine if information existed so that radiation effects on MOS devices could be translated into failure terms. No failure rate for MOS device radiation susceptibility could be determined. Actually, radiation is an environmental problem which accelerates existing failure modes rather than creating new failure modes.

Table XIII shows the 14 major failure modes of integrated circuits and their frequency of occurrence based on Minuteman II achieved data. An apportioned failure frequency for each failure mode is also shown. The last column gives the failure rate in percent per 1000 hours of each failure mode that is applicable to MOS technology. Failure mode No. 12 (Undetermined) represents failed parts where the failure mode has not been determined and are therefore potential failures that will fall in the other 13 categories. These failures were apportioned in the same frequency over the other 13 failure modes. The failures shown in No. 10 (External Features) and No. 14 (Retest Bad) were also apportioned over the other 11 failure modes in the original frequency because they were determined to be failures that should fall within the remaining 11 failure modes. Failure Modes Nos. 11 (Electrical Overstress) and 13 (Retest Good) represent parts removed and not actual failures, and for this reason they will be omitted from these calculations. The remaining nine failure modes were determined to be applicable to MOS devices.

The failure rates shown above were calculated in the following manner.

$$\frac{\text{Operating Hours}}{\text{Number of Failures}} = \text{MTBF}; \quad \frac{1}{\text{MTBF}} = \text{Failure Rate.}$$

Example:

$$\frac{1,290,000,000}{180} = 7,166,666$$

$$\frac{1}{7,166,666} = 0.000000132 \therefore 0.0132\ \%/1000 \text{ hours}$$

Based on the following information and data the failure rates in Table XIV were computed. The failure rates shown in this table take into account the relationship between failure modes and manufacturing processes. The failure rates shown for oxide and metallization are in percent per 1000 hours per 1000 sq. mils of area under metallization because these failure modes have been determined to be proportional to this area and not caused by the manufacturing process. An area under metallization of 2000 sq. mils was used for the Minuteman II IC's for these calculations. An average of 12 bonds both internal and external (leads) was assumed for the relationship of failure rate per bond. The failure rate for the failure mode associated with the diffusion process was divided by four to obtain a failure rate per diffusion. A four-step diffusion process is typical for the Minuteman II IC's. The remaining failure mode failure rates were determined to be directly related to MOS devices.

TABLE XIII

IC FAILURE RATE CHART

Failure Mode	Failure Frequency	Apportioned Failure Frequency	F/R %/1000 Hours
1. Oxides	52	180	0.0132
2. Lead Bond	8	32	0.0023
3. Metallization	19	65	0.0046
4. Internal Lead Discrepancy	10	34	0.0024
5. Faulty Diffusions	7	25	0.0019
6. Foreign Materials	5	14	0.001
7. Die-Header Bonding	24	84	0.0065
8. Surface Defects	1	5	0.0004
9. Crystal Imperfections	6	19	0.0014
10. External Features	509		
11. Electrical Overstress	111	390	
12. Undetermined	131		
13. Retest Good	359	633	
14. Retest Bad	239		
Total	1481	1481	

TABLE XIV

FAILURE RATE BY FAILURE MODE

Failure Mode	Failure Rate
1. Oxide Layer	0.0066 %/1000 hr/1000 sq. mils
2. Lead Bond	0.0002 %/1000 hr/bond
3. Metallization	0.0023 %/1000 hr/1000 sq. mils
4. Internal Lead Discrepancy	0.0002 %/1000 hr/bond
5. Faulty Diffusion	0.0005 %/1000 hr/diffusion
6. Foreign Material	0.0010 %/1000 hr
7. Die-Header Bonding	0.0065 %/1000 hr
8. Surface Defect	0.00004 %/1000 hr
9. Crystal Imperfections	0.0014 %/1000 hr

Example of Failure Rate Calculation.

$$\frac{0.0132}{2} = 0.0066 \text{ \%/1000 hr/1000 sq. mils}$$

Application of the Transfer Model

Shown below are predictions for 3 different MOS devices using the failure rates per failure mode derived from the Minuteman II integrated circuit data. These devices range considerably in size, functional capabilities and complexity. Device number 1 has an aluminum interconnect area of 2,500 sq mils as compared to 11,000 sq. mils for device number 3. Device No. 1 is a register and device No. 3 is a logic circuit. Table XV shows predicted failure rates for the full power and dormant conditions for present day MOS technology.

Achieved MOS Reliability Data

To improve the data concerning the statistical failure rate, an investigation was made of in-house systems utilizing complex MOS devices and failure rate data on the AIMP (Anchored Interplanetary Monitoring Platform) satellite program. It was found that one system which is turned on for one work shift (approximately 25 percent duty cycle) has accumulated 44,000 device hours while operating or 175,000 total device hours operating and non-operating without a single device failure (2.3 percent 1,000 hr

TABLE XV

MOS RELIABILITY PREDICTIONS

Device	AL Interconnect Area	Bonds	Failure Rate By (%/1000 hr) Failure Mode									Total Failure Rate (%/1000 hr)	
			Oxide Layer	Lead Bond	Metallization	Internal Lead	Faulty Diffusion	Foreign Material	Die-Header Bonding	Surface Defects	Crystal Imperfections	Normal	Dormant
1.	2,500	10	0.01650	0.00200	0.00575	0.00200	0.00050	0.00100	0.00650	0.00004	0.00140	0.03569	0.01950
2.	9,000	34	0.05940	0.00680	0.02070	0.00680	0.00050	0.00100	0.00650	0.00004	0.00140	0.10314	0.05636
3.	11,000	40	0.07260	0.00800	0.02530	0.00800	0.00050	0.00100	0.00650	0.00004	0.00140	0.12339	0.06743

1. 90-Bit Shift Register
2. Logic Circuit, approximately 50 flip-flops and associated gates
3. Logic Circuit, approximately 50 flip-flops and associated gates

and 0.57 percent/1,000 hr respectively). In a second system which is used sporadically for demonstrations (essentially dormant), it was found that 500,000 device hours have been accumulated with only one failure (0.2 percent/1000 hr). This failure was caused by wire bond lifting from a bonding pad which is not a failure unique to MOS technology. Both systems use 100-bit shift registers which contain approximately 630 FETs. It should be pointed out that not enough device hours have been accumulated to date on these systems to draw very specific conclusions. The Anchored Interplanetary Monitoring Platform (AIMP-D) satellite was launched July 1, 1966, at Goddard Space Flight Center, Greenbelt, Maryland. This satellite includes an encoder module which contains 748 MOS FET circuits in TO-5 cans. There are an average of 6 MOS FET elements in each can. A total of 16.7 million can-hours of test time had occurred by April 20, 1966. After one year in orbit, there have been no apparent MOS failures.

FUTURE MOS RELIABILITY EXTRAPOLATIONS

Figure 9 is the expected reliability improvement of MOS devices through technology advancement projected over the next five years. This projected growth will be realized only if the following contingencies are met:

1. Fairly wide military application and use
2. A good comprehensive failure prevention program
3. Implementation of corrective action to eliminate identifiable failure modes.

The curve shown in Figure 9 is based on the reliability improvement that has been realized on integrated circuits over the last five years. In 1962 integrated circuits had a failure rate of 0.4 percent per 1000 hours and in 1967 Minuteman II achieved data shows 0.003 percent per 1000 hours. Reliability improvement for a given device is strictly a function of application, use, and cost. This curve represents the improvement expected on a 40-lead, 400 to 800 active element MOS device. Simpler MOS devices should obtain a goal failure rate of approximately 0.0005 percent per 1000 hours during the same time span, but the contingencies of application, use, and cost are still the controlling factors.

Transistors were developed about 1950, but it was ten years before they reached industry-wide use (military and commercial). Integrated circuits were first introduced about 1962 and by 1965 were in very wide application by industry.

At the present time, based on past transistor and integrated circuit data, it would be unrealistic to show MOS device failure rates extrapolated beyond the 1972 time frame. Due to the reduction in time that it took integrated circuits to reach and surpass transistor reliability failure rate levels it is felt that MOS devices will achieve their major failure rate growth by the 1972 time frame.

Based on Minuteman achieved reliability improvements, the reliability of MOS devices has been extrapolated five years into the future as shown above. The growth curve shows an improvement factor of 500. Applying this to the prediction shown in Table XV, Table XVI was developed.

TABLE XVI
FUTURE MOS RELIABILITY PREDICTIONS

1972

Device	Normal (%/1000 hr)	Dormant (%/1000 hr)
1	0.00007	0.00004
2	0.00021	0.00011
3	0.00025	0.00013

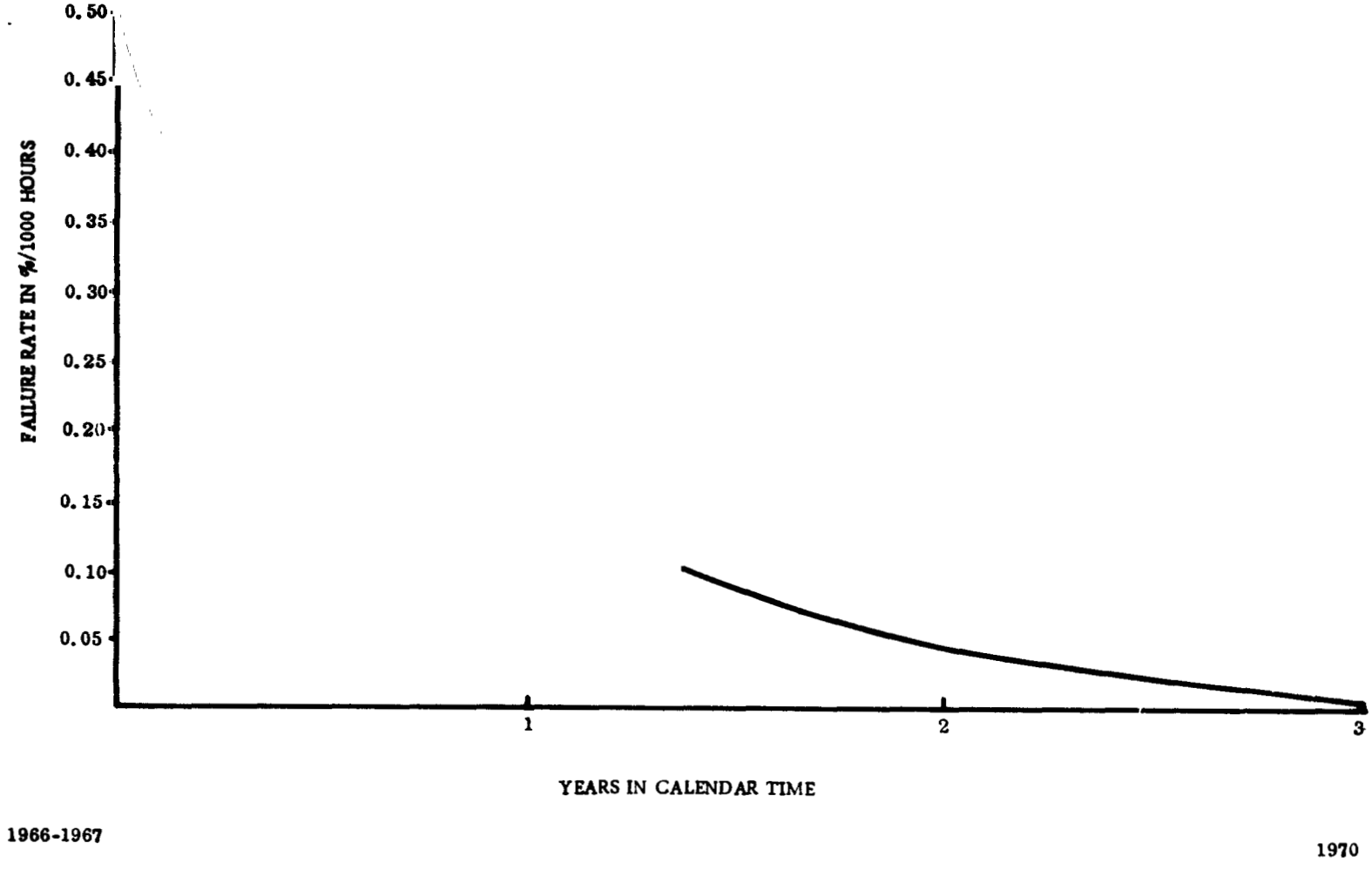


Figure 9. MOS Reliability Improvement Curve (a)

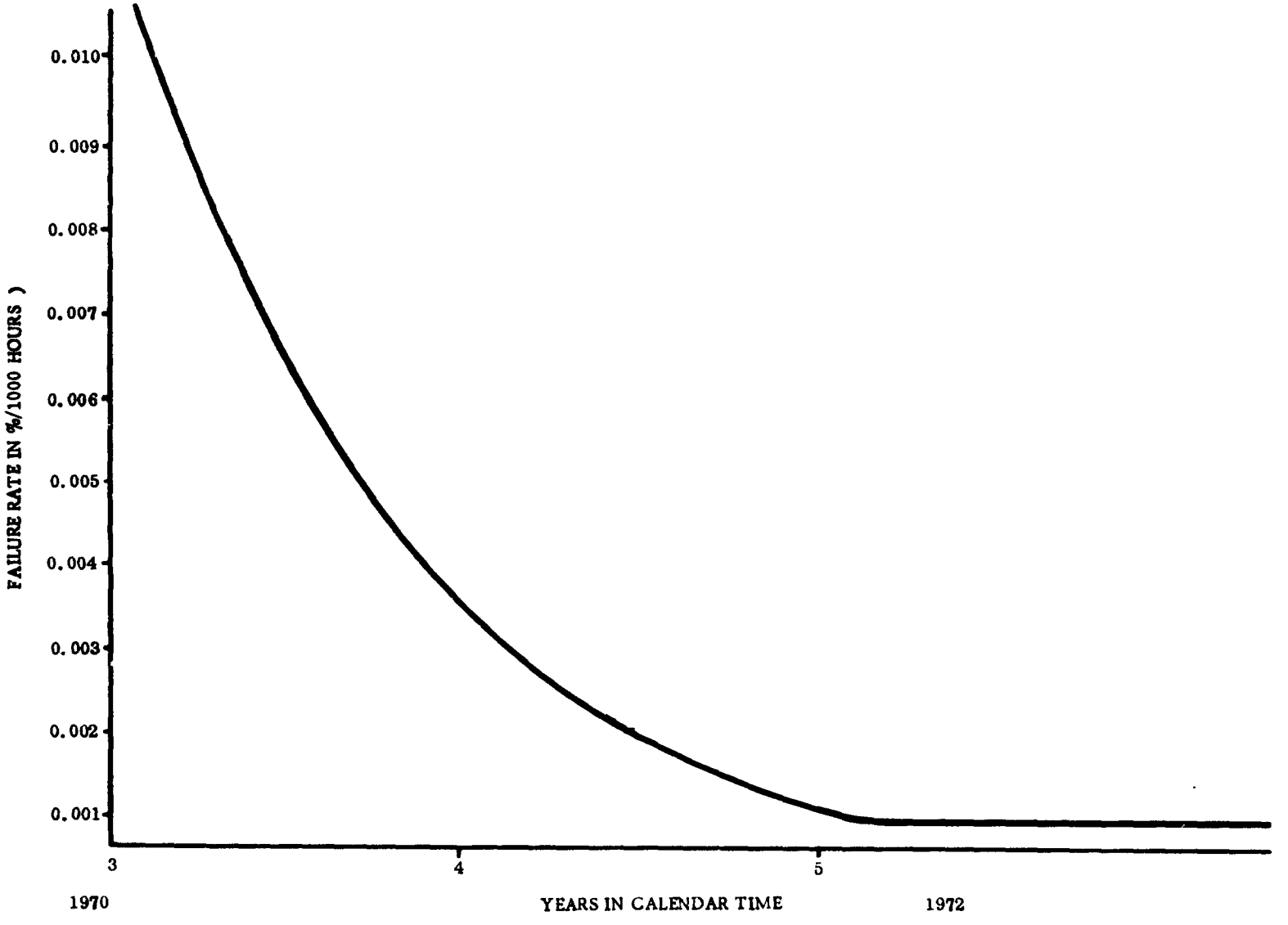


Figure 9. MOS Reliability Improvement Curve (b)

Power Condition of Spare Modules in Space Flight

In this analysis there are three different types of modules under consideration; those containing: (1) discrete parts, (2) bipolar IC's and (3) complex MOS IC's. Dormancy is the main condition that must be analyzed when considering the power condition of spare modules.

Table XVII shows a list of parts for mechanizing bipolar and MOS IC computers functionally equivalent to MARDAN, an Autonetics discrete component computer. Data from a previous study was used for the bipolar equivalent, and the MOS equivalent was derived using one MOS IC for 15 bipolar IC's. The failure rates used are based on present day achieved data except for MOS devices which have been extrapolated into the future so that all failure rates would indicate the same stage of technology development. The dormant failure rates were computed using the Dormant/Normal improvement ratios shown in Table VI except for capacitors and resistors. For these components the data is inconclusive due to design beyond limits for capacitors and lack of failures for resistors. A unity ratio was used for these parts.

The data in Table XVIII shows two things. First, the decrease in parts count and increase in reliability (summarized in Table XVII), and second the effects of dormancy of functionally equivalent computers made from the three device types under consideration.

Table XIX shows the Dormant/Normal mode MTBF improvement ratio for functionally equivalent computers built with discretes, bipolar IC's and MOS IC's.

It can be seen from the above analysis that the dormant/normal mode improvement ratio becomes less as the transition between discrete parts, bipolar IC's and MOS IC's takes place. This is caused by the reduction in those failure rates that the dormancy factors are operating on. It can be seen from Table XVII that the failure rate contribution of the miscellaneous parts (mechanical and electro-mechanical) such as transformers, connectors, switches, etc. becomes increasingly more important as the transition from discrete parts to bipolar IC's to MOS IC's takes place. The percentage of total failure rate contributions for the three technologies are 13 percent, 44 percent, and 65 percent, respectively. These percentages indicate that through the development and implementation of new device technologies the basic electronic failure rate contribution to a system becomes relatively small and that mechanical and electromechanical device failure rate contribution becomes increasingly more important.

TABLE XVII

COMPUTER SYSTEM FAILURE RATE ESTIMATES

Generic Part Type	Generic Failure Rate (%/1000 hr)	Discrete			Bipolar IC			MOS IC		
		Quantity	Normal	Dormant	Quantity	Normal	Dormant	Quantity	Normal	Dormant
Bipolar IC	0.0030				2,173	6.519	3.562			
MOS IC	0.0010							150	.150	.082
Transistor	0.0080	3,174	25.392	10.280	266	2.128	.862	266	2.128	.862
Capacitor	0.0015	2,377	3.566	3.566	460	.690	.690	460	.690	.690
Diode	0.0030	15,540	46.620	11.316	396	1.188	.288	396	1.188	.288
Resistor	0.0005	11,205	5.602	5.602	768	.384	.384	768	.384	.384
Misc.	--	467	12.582	12.582	299	8.624	8.624	242	8.376	8.376
Totals		32,763	93.762	43.346	4,335	19.533	14.410	2,255	12.916	10.682
MTBF (hrs)			1066	2307		5119	6940		7742	9362

TABLE XVIII

COMPUTER RELIABILITY IMPROVEMENT WITH TECHNOLOGY CHANGE

Transition	Discrete to Bipolar IC		Bipolar IC to MOS IC	
Power Mode	Normal	Dormant	Normal	Dormant
Decrease in parts factor	28,428 7.55	28,428 7.55	2,080 1.88	2,080 1.88
Increase in reliability factor	4,053 4.80	4,633 3.01	2,623 1.48	2,422 1.35

TABLE XIX

COMPUTER SYSTEM DORMANT/NORMAL MODE IMPROVEMENT RATIO

Device Type	Discrete	Bipolar IC	MOS IC
Dormant/Normal Improvement Ratio	2.16	1.36	1.21

CONCLUSIONS

1. The Minuteman data substantiates an improvement in reliability for the dormant mode over the operating mode. The data does not substantiate as high an improvement as was anticipated. The dormant/normal improvement ratios are shown in Table VI for components and Table XIX for a computer system. The curves in Figure 5 indicate that the dormant/normal improvement ratio is increasing for the Minuteman system as more data is accumulated.

2. The achieved data on MOS devices is as yet insufficient to demonstrate or contradict the predicted reliability of MOS devices.

3. The data in Table XVII indicates that the reliability of a MOS computer will be greater than the reliability of an equivalent bipolar IC computer.

4. In a large, high reliability system such as Minuteman the assessed primary field failures are sufficient to indicate the principal failure modes, but insufficient to gather statistics on second order failure modes. If this were not true, the principal failures would be so great in number as to preclude a high reliability system. The principal failures, however, are the ones that must be corrected for reliability enhancement.

5. Of the IC failures on parts passing post burn-in testing, only 3% were assessed as the primary cause of field failure. The rest were induced field failures or failures detected by screening and testing. This points out the value of screening and testing parts, modules and systems prior to operational readiness for enhanced system reliability.

6. As MOS reliability approaches the extrapolated failure rates of approximately 0.0001%/1000 hours in the future, it will become exceedingly difficult to measure the reliability. To accumulate 10 failures with this failure rate it would require one million components tested for a one-year period, which would be very expensive.

7. The theoretical analysis of MOS failure mechanisms indicates that the dormant mode has an increased reliability over the normal mode of operation. The two principal causes of MOS-unique failures relate to absolute high temperatures and temperature cycling. High temperature increases the mobility of contaminate charges. Thermal cycling induces mechanical defect sites due to differences in expansion inefficients which cause failures when electric fields are applied.

APPENDIX

Often we are interested in the confidence that we can maintain in asserting that the true mean life, or mean time between failures, (denoted by θ) of a component whose time to failure follows the exponential density

$$f(t;\theta) = \frac{1}{\theta}e^{-t/\theta}$$

is greater than, less than, or within plus or minus a stated percent of an observed mean life (denoted by $\hat{\theta}$). This section explains how confidence statements can be obtained from curves plotted by means of a chi-squared variable, according to the relation

$$P[\theta \geq R\hat{\theta}] = P\left[\chi^2(2r) \leq \frac{2r}{R}\right]$$

This relation follows from the fact that variable $\chi^2(2r) = \frac{2T}{\theta}$ is a chi-squared variable with 2r degrees of freedom; i.e.,

$$P[\theta \geq R\hat{\theta}] = P\left[\theta \geq \frac{RT}{r}\right]$$

$$= P\left[\frac{r}{R} \geq \frac{T}{\theta}\right]$$

$$= P\left[\frac{2T}{\theta} \leq \frac{2r}{R}\right]$$

$$= P\left[\chi^2(2r) \leq \frac{2r}{R}\right]$$

We should note that, as r becomes greater, our confidence increases in asserting that the MTBF is within a stated percent of our observed value, $\hat{\theta}$. For example, with 20 failures we are only 34-percent (71-37) confident in asserting that the true mean time between failures lies within ±10-percent of the observed MTBF, while with 100 failures we are 67-percent (86-19) confident in the same assertion. For a sufficiently large number of failures, the results of the procedure for a fixed time test differ insignificantly from the results of a fixed failure test.

Consider, as an example, a normal population with unknown mean μ and known standard deviation 3. Suppose a sample of four observations (1.3, 2.6, 0.5, 3.2) was obtained. The maximum-likelihood estimator $\hat{\mu}$ of the mean μ is

$$\hat{\mu} = \bar{x} = 1/4 \sum_{i=1}^{4} x_i = 1.9 \qquad (1)$$

We wish to obtain a confidence interval $[\bar{x} + C, \bar{x} - C]$ which is rather certain to contain μ, the true parameter. Suppose, in fact, that we wish to be 95 percent certain that our interval will contain μ.

Now, the statistic

$$z = \frac{\bar{x} - \mu}{\sigma/\sqrt{n}} \tag{2}$$

is normally distributed with zero mean and unit variance. Thus, the density function of z is given by

$$f(z) = \frac{1}{\sqrt{2\pi}} e^{-z^2/2} \tag{3}$$

and the cumulative function, by

$$F(z) = \int_{-\infty}^{z} f(x)\, dx \tag{4}$$

Then the probability that z will fall between two arbitrary numbers l_1 and l_2 is

$$P(l_1 < z < l_2) = F(l_2) - F(l_1) \tag{5}$$

If we wish to determine l_1 and l_2 such that $P(l_1 < z < l_2) = 0.95$, then we find from the cumulative normal table l_2 such that $F(l_2) = 0.975$, and l_1 such that $F(l_1) = 0.025$. This endeavor yields $l_1 = -1.96$ and $l_2 = 1.96$. Thus

$$P(-1.96 < z < 1.96) = 0.95 \tag{6}$$

$$P\left(-1.96 < \frac{\bar{x} - \mu}{\sigma\sqrt{n}} < 1.96\right) = 0.95 \tag{7}$$

$$P(\bar{x} - 1.96\, 3/\sqrt{n} < \mu < \bar{x} + 1.96\, 3/\sqrt{n}) = 0.95 \tag{8}$$

since $\sigma = 3$, and

$$P(-1.04 < \mu < 4.84) = 0.95 \tag{9}$$

using the sample data. Thus, we have a 95 percent confidence interval for μ.

It must be mentioned that (9) is not a true probability statement; that is, μ is not a random variable that has a 0.95 probability of falling between the two limits, as (9) would indicate. Mean μ is a fixed parameter which does not vary. The only true probability statements in this situation are

$$P(-1.04 < \mu < 4.84) = 1$$

or

$$P(-1.04 < \mu < 4.84) = 0$$

depending upon whether μ does or does not lie between the two limits. However, (9) does have a meaning. Equation (8) states that the probability that the random interval

$$[\bar{x} - 1.96\,{}^{3}/\sqrt{n},\ \bar{x} + 1.96\,{}^{3}/\sqrt{n}]$$

contains μ is 0 95; that is, if samples were repeatedly drawn, and the random interval

$$[\bar{x} - 1.96\,{}^{3}/\sqrt{n},\ \bar{x} + 1.96\,{}^{3}/\sqrt{n}]$$

computed for each sample, then these intervals would be expected to contain μ 95 percent of the time. Thus, for any specific interval, such as $[-1.04,\ 4.84]$, we can say that that interval is a 95 percent confidence interval, or that we are 95 percent confident that that interval includes the true μ. Our measure of confidence is 95 percent since, prior to the drawing of a sample, the probability was 0.95 that the interval which we would obtain would include μ.

The measure of confidence may be called "confidence level," "confidence coefficient," or "fiducial probability." "Fiducial probability" is denoted by P_F. Thus (9) can be written

$$P_F(-1.04 < \mu < 4.84) = 0.95 \qquad (10)$$

to distinguish it from a true probability statement. The term "fiducial" simply means that the probability was 0.95 before the sample was drawn that the interval that would be obtained would contain μ.

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