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OPERATIONAL AMPLIFIERS FOR USE IN NUCLEAR SPECTROSCOPY

by Theodore E. Fessler

Lewis Research Center

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SUMMARY

The design of pulse amplifier systems for use in nuclear research can be greatly simplified by the use of fast operational amplifiers. This report treats the design and use of operational amplifiers in circuits with rise times as low as 10 nanoseconds. A specific amplifier circuit is used to illustrate real amplifier performance. Phase-compensation methods and their relation to open-loop amplifier properties are described. Some closed-loop amplifier circuits are used to demonstrate practical phase compensation.

INTRODUCTION

Electronic pulse amplifiers for nuclear physics research must meet exacting requirements of linearity and stability (refs. 1 to 3). Typically, amplifiers that handle 1-microsecond pulses are now required to have less than 1 percent nonlinearity and less than 0.1 percent gain shift caused by temperature change or component aging. These levels of performance are needed to take full advantage of recent developments in particle accelerators and particle detectors (refs. 4 and 5).

The way to meet these requirements is to make liberal use of negative feedback (e.g., ref. 6). And the best way to approach the design of feedback amplifiers is by using the concept of operational amplifiers. An operational amplifier is a high-gain, dc-coupled amplifier in which feedback governs the input-to-output response. Many kinds of response functions can be formed by choosing the proper feedback network. The difference between the operational amplifier approach and earlier methods of pulse amplifier design is in the amount of feedback used. With operational amplifiers, so much negative feedback is used that the gain is determined almost entirely by the feedback network. Since the feedback network contains only passive components, linearity and gain stability are greatly improved.

A complete pulse amplifier system contains several stages of amplification and pulse shaping. (Ref. 1 gives a complete discussion of the current state of the art of pulse amplifier systems for nuclear spectroscopy.) The operational amplifier can serve as a building block in the design of such a system; each stage consists of an operational amplifier with an appropriate transfer function. Thus, the design of a complete amplifier system can be divided into two parts: the development of a number of functional circuits, each containing an operational amplifier, and the assembly of these circuits to synthesize the overall input-to-output transfer function.

There are currently available commercially a variety of inexpensive solid-state operational amplifiers, both discrete-device types and integrated circuits. These amplifiers were designed for use in analog computers and servomechanisms. For the most part, their high-frequency response is inadequate for use in nuclear instrumentation. But by tailoring circuits specifically for good high-frequency response and by using the newer fast transistors, operational amplifiers can be used in fast pulse amplifiers.

This report deals with the use of operational amplifiers in fast functional circuits. A specific amplifier design is used to show the relation of various open-loop parameters to the circuit component values. These open-loop parameters are then used to predict the phase compensation needed in closed-loop circuits. Finally, some functional circuits are described which use this sample amplifier.

IDEAL AND REAL OPERATIONAL AMPLIFIERS

An operational amplifier is a high-gain, dc-coupled amplifier designed to remain stable with large amounts of negative feedback from output to input. Some of these amplifiers are single ended. That is, some have only one input terminal and one output terminal. A ground lead serves as the reference potential for both input and output terminals. A more versatile type of amplifier is one with differential input (i.e., an amplifier with two input leads). The conventional symbol for such an amplifier is shown in figure 1. With this kind of amplifier, a positive signal at the positive input terminal produces a positive signal at the output. A signal at the negative input terminal appears inverted at the output terminal.

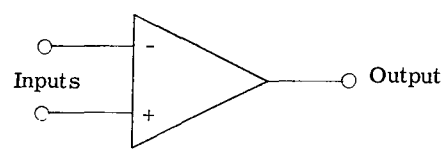


Figure 1. - Conventional symbol for differential-input operational amplifier.

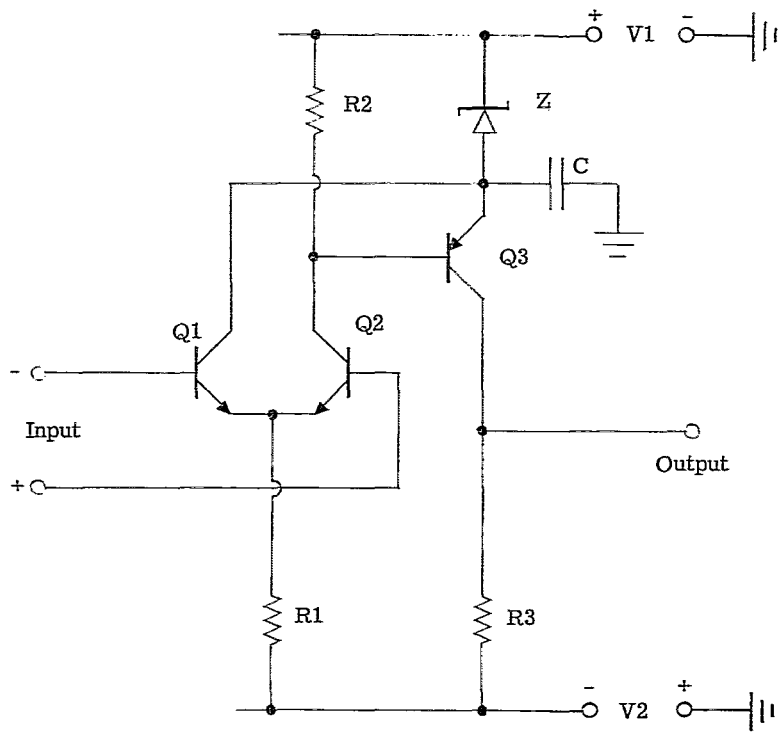


Figure 2. - Basic amplifier circuit.

Figure 2 shows the circuit of a simple differential amplifier. It has two stages: the input stage with transistors Q1 and Q2, and the output stage with transistor Q3. Direct coupling between these stages is made possible by using a PNP transistor for Q3 and NPN transistors at Q1 and Q2. The Zener diode Z and the capacitor C provide a voltage reference for the emitter of transistor Q3. The three resistors act as constant current sinks.

If the component values are chosen properly, the circuit of figure 2 can be made to have nearly zero offset voltage. Offset voltage is the voltage at the amplifier input which causes zero output voltage. A small offset voltage is important in amplifiers with dc gain. When the amplifier output is zero, the current flowing in resistor R2 must satisfy the following equation:

$$\left(I_{c,\,2} - I_{b,\,3}\right) R2 = V_z + V_{b,\,3} \qquad (1)$$

where

$I_{c,\,2}$ collector current of Q2

$I_{b,\,3}$ base current of Q3

$V_{b,\,3}$ base-emitter voltage of Q3

V_z voltage across Zener diode

At the same time, if transistors Q1 and Q2 are identical, equal currents will flow in them when both amplifier inputs are grounded. Under these conditions, the collector current $I_{c,2}$ must satisfy the following equation:

$$2(I_{c,2} + I_{b,2})R1 = V2 - V_{b,2} \tag{2}$$

where $I_{b,2}$ is the base current of Q2 and $V_{b,2}$ is the base-emitter voltage of Q2. Since I_b is usually negligible compared with I_c, equations (1) and (2) can be combined to obtain

$$\frac{R2}{R1} = 2\,\frac{V_z + V_{b,3}}{V2 - V_{b,2}} \tag{3}$$

as the relation between R1 and R2 which produces a minimum offset voltage.

The output current capacity of the circuit of figure 2 is much greater for positive output signals than for negative ones because the negative output current is limited by resistor R3. If the amplifier were required to have a high current capacity for negative output signals, the complementary transistor polarities would be preferred to those shown in figure 2. In other words, Q1 and Q2 would be PNP transistors and Q3 would be an NPN transistor. Reversing the polarity of the supply voltages and of the Zener diode would complete the change of polarity.

Negative feedback in circuits using operational amplifiers is obtained by connecting a feedback network Z_f between the amplifier output and the negative input (fig. 3). When this connection is made, the circuit behaves in the manner of a self-balancing bridge. The output voltage attains whatever value is necessary to cause a current in the feedback that keeps the differential input voltage nearly zero. This current must just equal any current introduced on the negative input terminal (I_i in fig. 3). The degree to which these conditions are met depends on the quality of the operational amplifier. Ideally, the

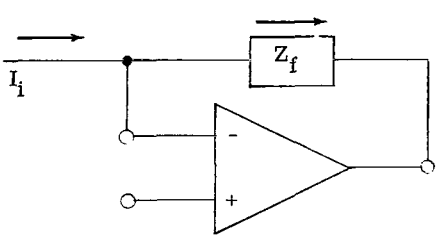


Figure 3. - Application of negative feedback element Z_f which maintains null input.

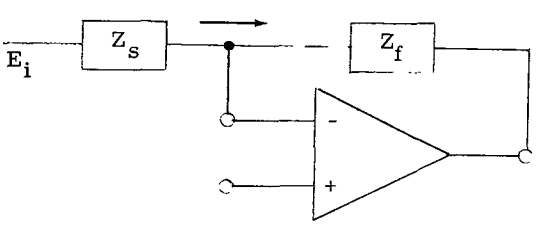


Figure 4. - Input network Z_s converts signal input voltage E_i to input current.

differential input voltage is identically zero, and the amplifier input currents are also zero.

In pulse amplifiers the input signal is usually a voltage rather than a current. In this case, an additional impedance (Z_s in fig. 4) is placed in series with the negative input. For example, if both Z_s and Z_f are resistors, the circuit becomes a simple voltage amplifier. In the limit of an ideal operational amplifier (with infinite open-loop gain), the voltage gain would be $-Z_f/Z_s$. By using reactive or nonlinear elements in Z_s and Z_f, other functional circuits are possible. Reference 6 gives a variety of these circuits together with their transfer functions.

The extent to which these operational amplifier methods can be applied to fast pulse amplifiers depends on how much the real circuit departs from the ideal. For instance, since the open-loop gain of a real amplifier is finite, the input voltage will not be exactly zero. And since the input voltage is not exactly zero, the amplifier input impedance becomes important insofar as it determines the input terminal current. Furthermore, the open-loop gain varies with frequency. It can be high at low frequencies but decreases rapidly above some frequency which is characteristic of the particular amplifier. And of course, any amplifier is limited in the amount of voltage and current that it can deliver to an external load. Whenever these limits are exceeded, the output signal no longer represents the desired function of the input. At high signal speeds, there is also a limit on the maximum rate of change of the output voltage. This limit is called the slewing-rate limit. These real amplifier characteristics are considered in the next section.

OPEN-LOOP PROPERTIES

The open-loop properties of concern are voltage gain, phase lag, input and output impedance, slewing-rate limit, and input offset voltage and current. A test amplifier based on the circuit in figure 2 was built in order that real performance characteristics could be considered. This circuit was chosen only for its simplicity, not because it is in any way superior to others. The component values used in the test amplifier are listed in table I. All measurements discussed in this section were made on this amplifier.

Voltage Gain

Figure 5 shows the test circuit used to measure the open-loop voltage gain of the test amplifier. The 10-ohm and 1-kilohm resistors present a low-level, low-impedance signal source to the test amplifier. The 15-kilohm resistor and the 20-kilohm potentiometer are used to adjust the amplifier-output voltage to zero.

TABLE I. - COMPONENT VALUES USED IN

TEST AMPLIFIER

Circuit element (fig. 2)	Specification
Transistor	
Q1 and Q2	2N2925
Q3	2N3702
Zener diode, Z	1N752 (V_Z = 5.6 V)
Capacitor, C	0.005 μF
Resistor	
R1	4.7 kΩ
R2	3.9 kΩ
R3	4.7 kΩ
Voltage, V1 and V2	16V

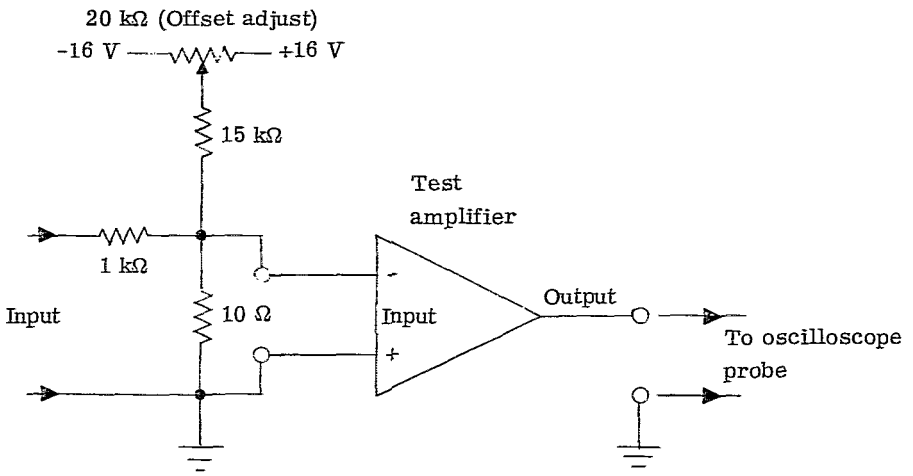


Figure 5. - Circuit used to measure open-loop voltage gain and phase lag of test amplifier.

The voltage gain is a complex function (with both real and imaginary parts) of the signal frequency. In this section, the magnitude and phase factors are discussed separately. Figure 6 shows the measured variation of voltage gain with signal frequency. These results were obtained under small-output conditions. (The logarithmic plots discussed in this section are known as Bode plots.)

The results presented in figure 6 show that below about 100 kilohertz, the voltage gain of the test amplifier is constant with frequency. In this region, the amplifier gain is determined by the dc gain β of the transistors. Between 100 kilohertz and about 10 megahertz, the voltage gain decreases as 1/f. In this range, the voltage gain decreases with increasing frequency because of the base-to-collector capacity in transistor Q3. This

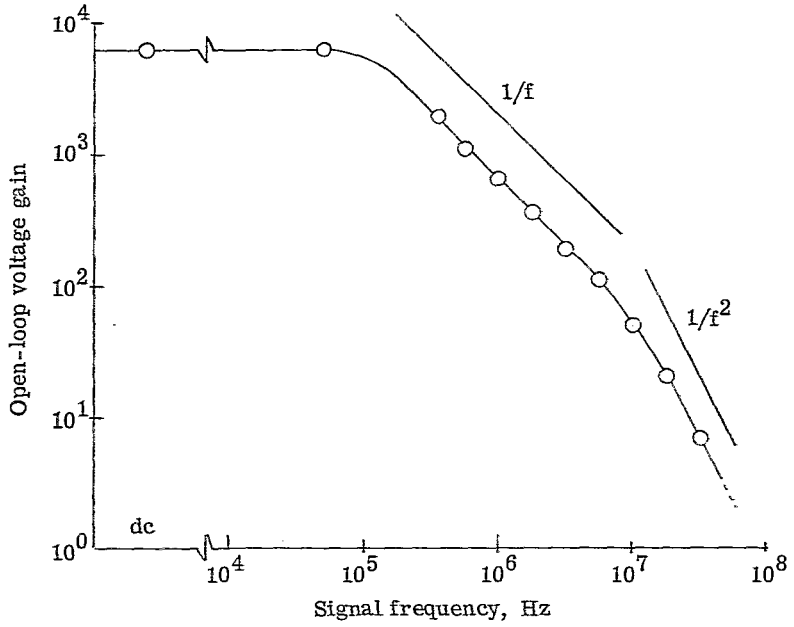


Figure 6. - Measured open-loop gain of test amplifier showing 1/f and $1/f^2$ variation regions.

capacity (about 12 pF in the 2N3702) produces a degenerative feedback effect. Since the impedance of this feedback capacity varies as 1/f, the voltage gain also varies as 1/f.

Above 10 megahertz, the open-loop gain drops still more sharply with frequency. At these high frequencies, the current gain of the input transistors is also decreasing with frequency with the result that the voltage gain varies approximately as $1/f^2$ in this region. Finally, the voltage gain becomes less than 1 near 100 megahertz.

Phase Lag

The phase lag of the test amplifier was also measured with the circuit shown in figure 5. The results are presented in figure 7, where the phase shifts are given as the amplifier output phase relative to that which would be obtained from a perfect inverting amplifier.

Phase lag is related to the gain-frequency behavior. At low frequencies, the amplifier acts as a straight inverter without additional phase change. In the range where the voltage gain decreases as 1/f, the phase lag increases to 90^o. The reason is that the capacitive reactance of the base-to-collector capacity of Q3 is the gain-controlling factor. Above 10 megahertz, where the open-loop gain decreases as $1/f^2$, the phase lag increases to 180^o. In this region, the transit times of Q1 and Q2 have become important. These phase-shift regions are shown by the dashed horizontal lines in figure 7.

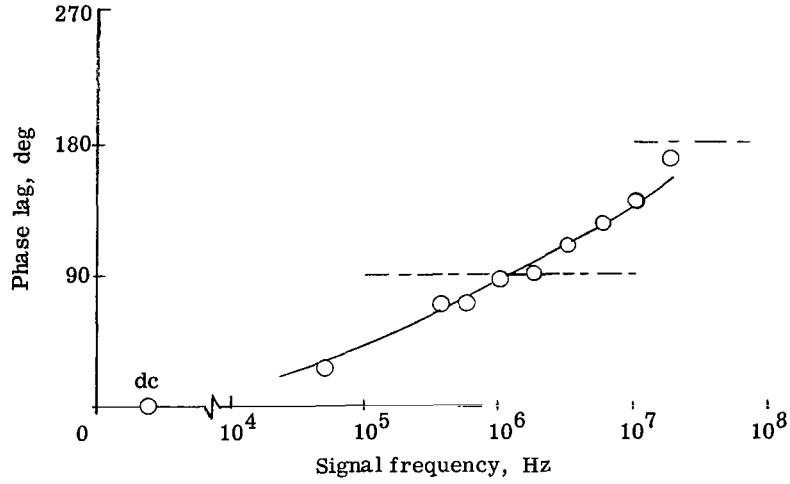


Figure 7. - Measured phase lag of test amplifier.

Input and Output Impedances

Ideally, the input voltage of an operational amplifier is always zero as a result of the self-balancing action of negative feedback. In this ideal limit, input terminal impedance is of no concern. But for real amplifiers, the input terminal voltage is not zero because the open-loop gain is not infinite. It is therefore necessary to consider the amplifier input impedance as an added element in the feedback network. The finite open-loop gain of real amplifiers also makes it necessary to consider the amplifier output impedance, particularly when low-impedance loads are involved.

Figure 8 shows the circuit used to measure the open-loop input impedance of the test

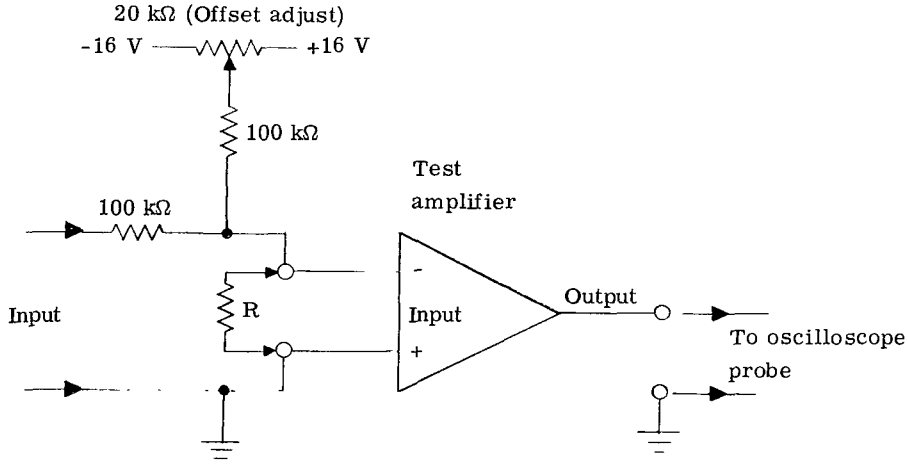


Figure 8. - Circuit used to measure amplifier input impedance.

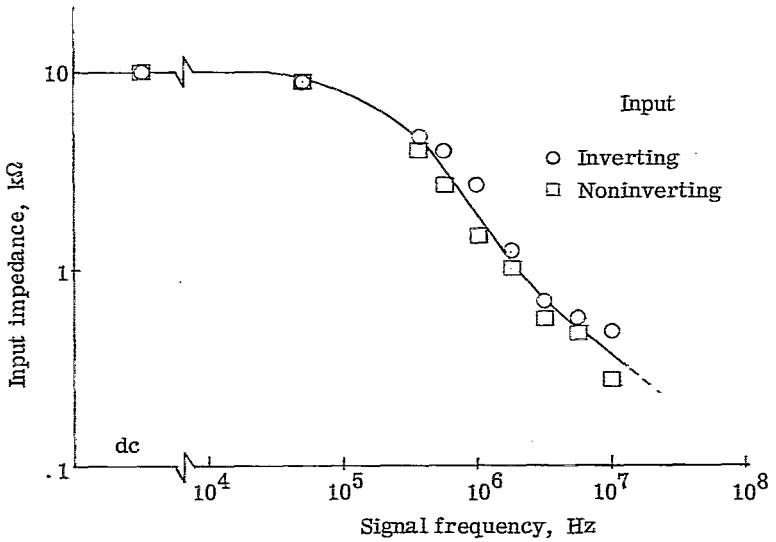


Figure 9. - Measured single-input input impedances of test amplifier.

amplifier. The value of resistor R which would halve the output signal was considered to be a measure of the input impedance. (These values are equal only if the input impedance is purely resistive.) Each input was tested separately. Figure 9 gives the measured values for both input connections.

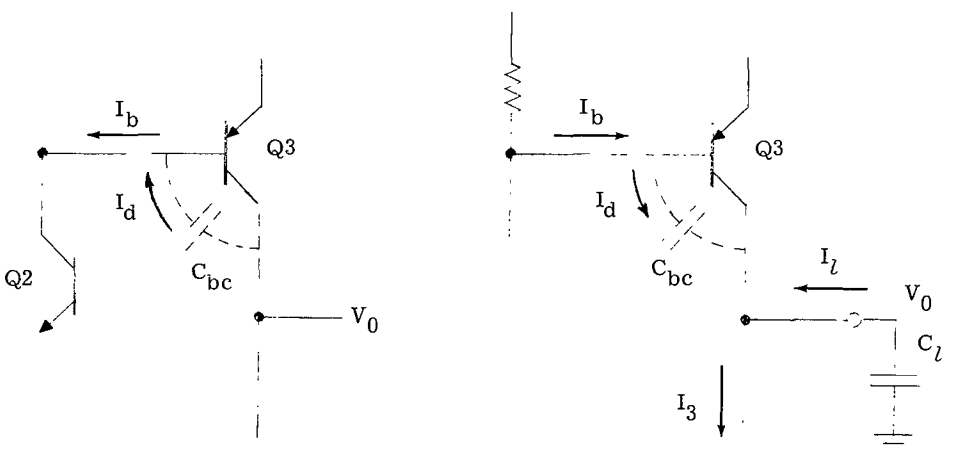
At low frequencies, the impedance at the input is 10 kilohms. This value is equal to the sum of the base-to-emitter resistances of Q1 and Q2. At about 100 kilohertz, the input impedance begins to decrease as 1/f mostly as a result of the decreasing impedance of the emitter-base junction capacity. However, there is a small effect of base-to-collector feedback in Q2 which makes the impedance of the noninverting input lower than that of the inverting input. The decrease in input impedance with increasing signal frequency is a factor to be considered in selecting the feedback network in a closed-loop amplifier.

The amplifier output impedance can be measured in a similar way by determining the value of load resistance which just halves the output signal. At low frequencies, the output impedance of the test amplifier is about 4 kilohms, the parallel combination of R3 (see fig. 2) and the collector impedance of Q3, which is about 20 kilohms. Between 100 kilohertz and 10 megahertz, the output impedance decreased just as does the voltage gain (fig. 6), as a result of the negative feedback effect of the base-to-collector capacity of Q3. At 1 megahertz, the measured amplifier output impedance is only 100 ohms. This low value is the dynamic output impedance, that is, the small signal impedance at a particular frequency. It cannot be used to predict the output power or output voltage capability of the amplifier.

Slewing Rate

As ever larger step pulses are applied to the input of an amplifier, a level is reached where the rate of change of the amplifier output no longer is proportional to the input. This limiting rate of change is called the slewing rate. The slewing rate is reached whenever the amplifier input is momentarily large enough to cause one of the transistors in the amplifier to reach saturation or cutoff.

Limiting conditions that occur in the test amplifier are presented schematically in figure 10. First, consider pulses which result in a positive amplifier output (fig. 10(a)).



(a) Positive output.

(b) Negative output.

Figure 10. - Simplified circuit diagrams used in analysis of slewing-rate limits.

If the input step signal is big enough, transistor Q1 will reach cutoff, and its quiescent current will then flow through Q2 from the base lead of Q3. This current is labeled I_b. The current actually drawn from the base-emitter junction of Q3 is less than I_b by the amount of displacement current I_d arising from the base-collector junction capacity C_{bc}. When the output voltage V_o changes rapidly, this displacement current can greatly reduce the base current drive available to Q3.

Obviously, I_d cannot exceed I_b. This condition then puts an upper limit (the slewing rate) on the rate of change of the output voltage V_o which is

$$\dot{V}_o C_{bc} < I_b \tag{4}$$

For the test amplifier, $I_b = 1.7$ milliamperes and $C_{bc} \cong 12$ picofarads. The positive slewing rate limit is therefore approximately 140 volts per microsecond.

To determine the slewing rate for pulses that give a negative output, it is necessary

to determine whether transistor Q2 or Q3 is the first to reach cutoff. If the drain current I_3 in figure 10(b) is large enough to prevent Q3 from being cutoff before Q2, the situation is the same as for positive output signals, and equation (4) applies as before. But if I_3 is smaller than I_b, or if there is appreciable load capacity C_l, transistor Q3 will reach cutoff first. At the moment Q3 is cut off, its collector current is zero, and the slewing rate can be calculated from the equation

$$I_3 = I_l + I_d = -\dot{V}_o\left(C_l + C_{bc}\right) \tag{5}$$

For example, for the test amplifier $I_3 = 3.4$ milliamperes. With the assumption of a load capacitance of 20 picofarads, equation (5) predicts a slewing rate of -106 volts per microsecond. This rate is smaller than the value obtained from equation (2), and, therefore, Q3 must reach cutoff before Q2.

Input Offset Voltage and Current

Input offset voltage is the voltage that must be applied between the amplifier input terminals to obtain zero output. Ideally, an amplifier should produce exactly zero output for zero input, but this cannot be realized in practice because of small mismatches between components in a real circuit. The output of a real amplifier will therefore have a dc offset even when there is no input signal. In amplifier stages with high gain, this offset voltage can become intolerably large.

A fixed input offset voltage is not an insurmountable problem because biasing circuits can be added to cancel it. But, if that should be necessary, then some of the attractive simplicity of differential input amplifiers is lost. On the other hand, drift of the offset with time or temperature must be regarded as a form of noise.

The input offset voltage is dependent on three kinds of circuit imbalance:

(1) Physical differences in the individual transistors in the input stage

(2) Unbalance of the quiescent currents in the input-stage transistors under zero output conditions

(3) Differences in the operating temperatures of the input transistors

As a result of variations in the manufacturing process, the base-to-emitter voltage at a given collector current varies, even between transistors of the same type. For the 2N2925 transistor used in the test amplifier, these variations average about 5 millivolts from one specimen to another.

The quiescent collector currents in the input-stage transistors can be made equal by proper sizing of the resistors. (For example, eq. (3) gives the correct values for the

circuit in fig. 2.) By using 10-percent-tolerance resistors, these currents can be matched within 10 percent of one another. The effect of a current imbalance can be calculated from the current-voltage relation for forward-biased junctions:

$$\frac{dI}{I} = k \ dV \tag{6}$$

In silicon, the constant k is approximately 40 volt^{-1}. Therefore, a 10-percent difference in current is equivalent to an offset voltage of 2.5 millivolts.

These two sources of input offset voltage can be eliminated by carefully adjusting the currents for a specific set of transistors. But the third source of circuit imbalance is not adjustable. In silicon, the temperature coefficient of a forward-biased junction at room temperature is -1.6 millivolts per ^{o}C. Therefore, it is important that the two input transistors be at the same temperature. For instance, the power dissipation in these transistors should be kept small and nearly equal. (The circuit of fig. 2 accomplishes this.) Also, the transistors should not be placed near other power-dissipating parts.

Input offset current is the difference between the input bias currents at zero amplifier output. If these two bias currents are nearly equal (zero offset), their effect can be canceled by making the impedance to ground equal at both inputs. Figure 11 shows this circuit in a simple voltage amplifier. However, differences in the input bias currents are equivalent to an input voltage offset and can cause the same problems.

Input offset currents are caused by differences in transistor current gain and by unequal base currents in the input transistors at zero output conditions. For the test amplifier, the base currents of Q1 and Q2 can range from about 8 to 4 microamperes because the current gain of individual 2N2925 transistors ranges from 200 to 400. As a result,

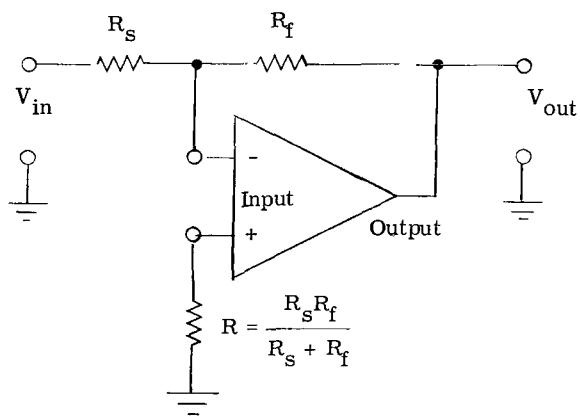


Figure 11. - Voltage amplifier circuit showing method of making impedance to ground equal at both inputs.

the input offset current in the test amplifier can range as high as 4 microamperes with the average lying between 1 and 2 microamperes for pairs of transistors selected at random. If the input transistors are selected to have equal current gains, and if their quiescent currents are balanced (by using eq. (3)) to within 10 percent of one another, then the residual offset current in the test amplifier will be less than 1 microampere.

PHASE COMPENSATION

In any amplifier with feedback, the phase of the feedback signal must be controlled to avoid oscillation. This fact is particularly true of operational amplifiers because their use always involves large amounts of feedback. Therefore, it is usually necessary to alter the natural frequency response of the amplifier by adding an appropriate resistance-capacitance (RC) network to the amplifier. These adjustments are referred to as phase compensation.

Frequency-Response Requirements

It is common practice to design operational amplifiers to have an open-loop gain which at high frequencies decreases as 1/f. (This decrease is also referred to as a 6-dB-per-octave rolloff.) An amplifier with this frequency response will have at most a 90° phase shift throughout its entire active range. Hence, it is stable under any amount of resistive feedback and is termed fully compensated.

Figure 12 shows again the natural frequency response of the test amplifier. Clearly, the test amplifier is not fully compensated. At the corner frequency f_1, the voltage gain begins to drop as 1/f, but beyond the corner at f_2, the gain varies as $1/f^2$. To compensate the test amplifier fully, it is necessary to alter the open-loop frequency response so that f_2 occurs beyond the point where the gain decreases to 1. This can be done by adding an appropriate RC network somewhere in the amplifier. The effect of this network must be to reduce the gain between f_1 and f_2. For the test amplifier, this gain reduction must be at least a factor of 10 and can represent a serious loss.

It is not always necessary to take this loss if less than full compensation can be accepted. The pulse amplifier designer is often interested in minimizing amplifier risetime. Shorter amplifier risetime can be obtained if the amount of phase compensation used is only as much as needed in each particular case, which usually means only that amount required to remove overshoot. (Overshoot refers to a damped oscillation in amplifier response to a sudden change in the input voltage.) Therefore, in terms of figure 12, it is not always necessary or even desirable to remove the high-frequency corner

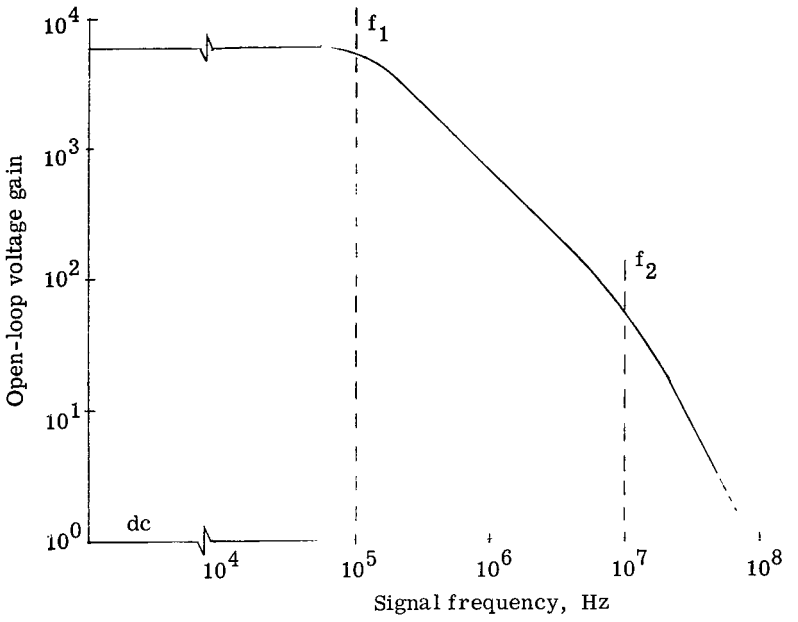


Figure 12. - Open-loop frequency response of test amplifier showing location of two corner frequencies.

altogether. For amplifiers that have only two corners in their frequency response, there is a simple relation between these two corner frequencies that can be used.

Once again consider the voltage amplifier circuit in figure 11. The closed-loop voltage gain of this circuit is given by

$$\frac{V_{out}}{V_{in}} = \frac{-K}{1 + \frac{R_s}{R_f} + K\frac{R_s}{R_f}} \tag{7}$$

where K is the dc open-loop voltage gain and where the input impedances of the amplifier have been ignored. The attenuation k of the feedback network between the amplifier output and the amplifier input is given by

$$k = \frac{R_s}{R_s + R_f} \tag{8}$$

(Again the amplifier input and output impedances have been ignored for simplicity.) There will be no overshoot in the amplifier response if

$$\frac{f_2}{f_1} \geq 2kK \tag{9}$$

(This result is derived from an analysis of the response of two-pole systems to a step function disturbance. Reference 8 contains a complete discussion of the relations between system response and the configuration of the poles and zeroes of the transfer function of that system.)

The largest possible value of k is 1.0 ($R_f = 0$). In this case, equation (9) requires that $f_2 = 2Kf_1$. Since the open-loop gain falls as 1/f between f_1 and f_2, this expression is equivalent to saying that f_2 must occur at or beyond the point where the open-loop gain has fallen to 1/2. If a voltage amplifier with a closed-loop gain of 100 is desired, k will be only 0.01 and equation (7) yields $f_2/f_1 = 100$ ($K \cong 5000$ for the test amplifier). In figure 12, f_2/f_1 is 100 without any phase compensation. In other words, the 1/f region of the test amplifier is large enough to accommodate closed-loop gain equal to or greater than 100 without adding phase compensation. In fact, using a fully compensated amplifier with a closed-loop gain of 100 would cause the amplifier risetime to be more than a factor of 10 larger than necessary.

Phase-Compensation Network

The easiest way to effect phase compensation is to increase the amplifier time constant that causes the corner at f_1 (fig. 12). For the test amplifier, this increase requires adding capacitance between the base and collector of Q3. This addition reduces the open-loop gain by a constant factor at frequencies greater than f_1, as shown by curve A in figure 13. Frequency f_2 is unchanged.

Better results are obtained if a small resistance is put in series with this compensating capacitor. Figure 14 shows this compensation included in the basic amplifier circuit. If this resistance is equal to the reactance of the capacitor at frequency f_2, the corner at f_2 is replaced by a corner at a higher frequency (curve B, fig. 13). In network theory, this procedure is called pole-zero cancellation. This improvement (in the ratio f_2/f_1) does not cause any further loss in open-loop gain.

The required values of resistance and capacitance can be determined either by trial and error or by calculation. If the open-loop behavior of the amplifier is known, it is a simple matter to calculate the values needed for any amount of feedback (e. g., in the calculation of the values for full compensation, k = 1.0).

The uncompensated amplifier corner frequencies are related by $f_2/f_1 \cong 100$. For full compensation, equation (7) requires $f_2'/f_1' \cong 10^4$, where the primes indicate the compensated corner frequencies. By using the compensation network shown in figure 14, it is possible to increase f_2'/f_2 by the same amount as f_1/f_1'. Therefore,

$$\frac{f_2'}{f_2} = \frac{f_1}{f_1'}$$

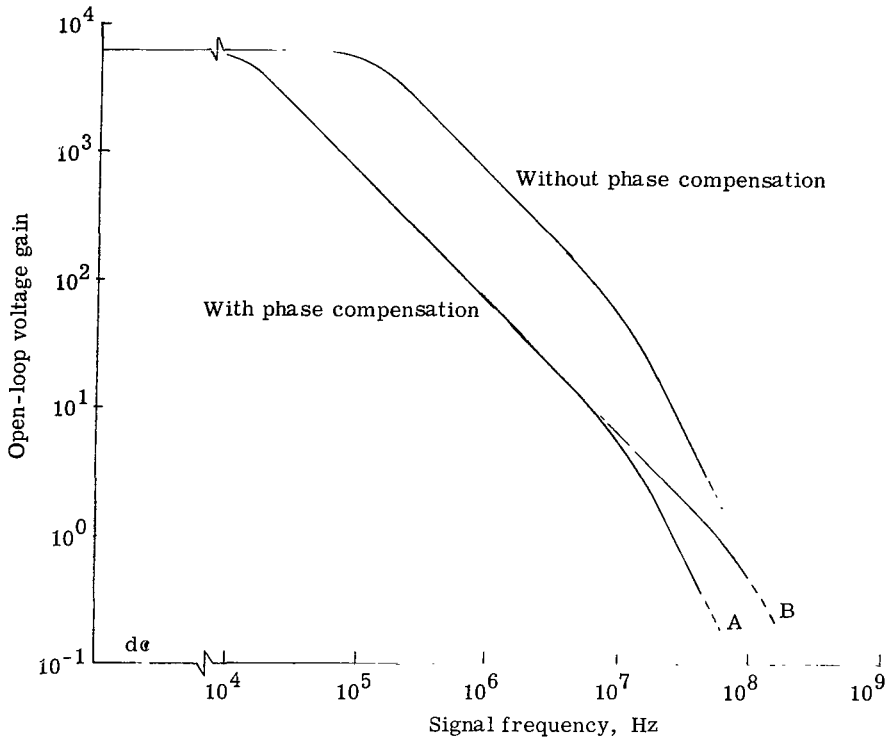


Figure 13. - Open-loop frequency response of test amplifier with and without phase compensation.

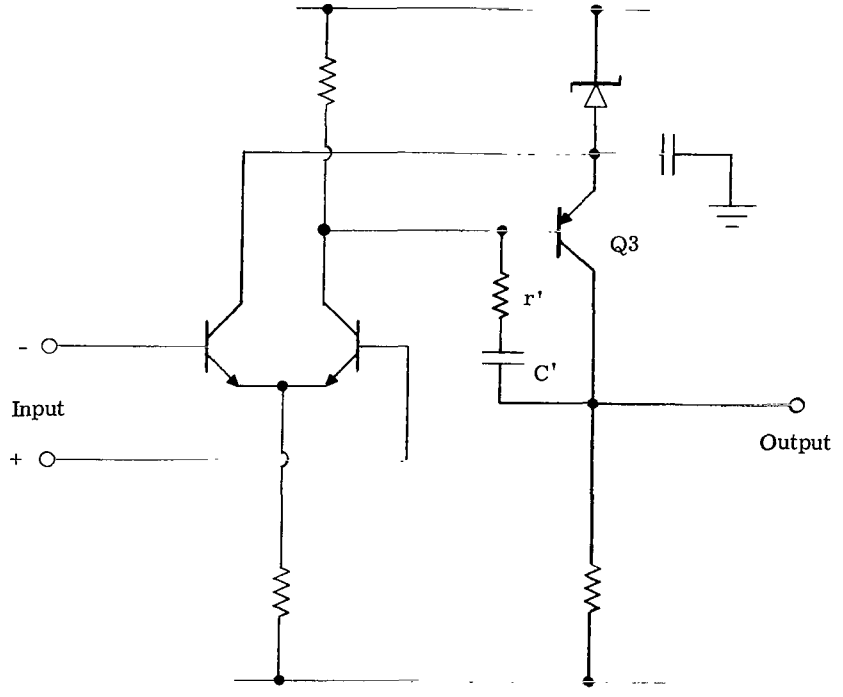


Figure 14. - Basic amplifier circuit with phase compensation applied across output transistor Q3.

and the required ratio becomes

$$\frac{f_1}{f'_1} = \sqrt{\frac{\frac{f'_2}{f'_1}}{\frac{f_2}{f_1}}} = 10$$

The compensation capacity C' is determined from

$$\frac{C' + C_{cb}}{C_{cb}} = \frac{f_1}{f'_1} = 10$$

or

$$C' = 9C_{cb}$$

For the 2N3702 transistor, the base-to-collector capacity C_{cb} is 12 picofarads, and so C' should be 110 picofarads. Then, the series resistance r' should be equal to the reactance of 110 picofarads at $f_2(10^7$ Hz), or 150 ohms. At higher closed-loop gains (lower k) the required ratio of f_1/f'_1 is smaller, with the result that smaller values of C' are needed. Table II(a) lists the proper values of C' and r' for several values of k.

Phase compensation is also possible with the network shown in figure 15. This circuit contains two poles and two zeros. In other words, both open-loop response corners are canceled and replaced by new ones; one at a lower frequency f'_1 and the other at f'_2.

TABLE II. - COMPONENT VALUES FOR PHASE-COMPENSATION CIRCUITS THAT OPTIMIZE AMPLIFIER RISE TIME

(a) Circuit shown in figure 14

Feedback network attenuation, k	Capacitance, C', pF	Series resistance, r', Ω
1.0	110	150
.5	75	220
.2	40	400
.1	20	650

(b) Circuit shown in figure 15

Feedback network attenuation, k	Resistance		Capacitance	
	r', Ω	R', Ω	c', pF	C', μF
1.0	100	900	16	0.015
.5	150	900	16	.01
.2	200	700	21	.0075
.1	300	650	22	.004

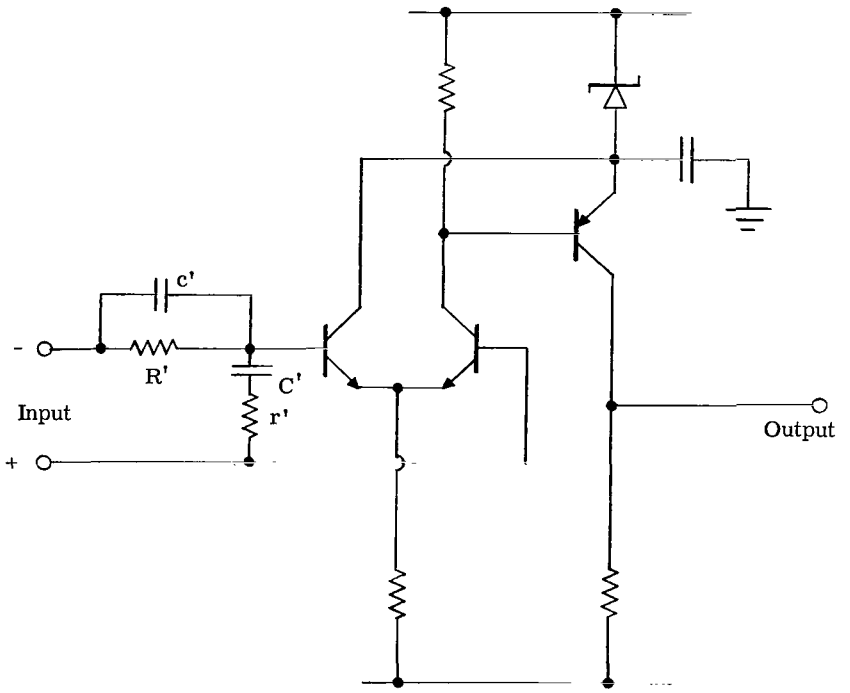


Figure 15. - Basic amplifier circuit with resistance-capacitance phase-compensation network at amplifier input.

Again, suppose that full compensation is desired. Since the test amplifier input impedance varies with frequency, it is important to make the value of r' (fig. 15) smaller than the amplifier input impedance at all frequencies up to f_2'. Otherwise, the capacitive reactance of the amplifier input will introduce another (unwanted) pole in the compensation network. From figure 9, an r' of 100 ohms would appear to be adequately low. Then, C' should have a reactance equal to r' at f_1 in order to cancel that corner. Since $f_1 = 10^5$ hertz, C' should be 0.015 microfarad. Resistance R' is then determined by the amount of open-loop-gain reduction required between f_1 and f_2, that is,

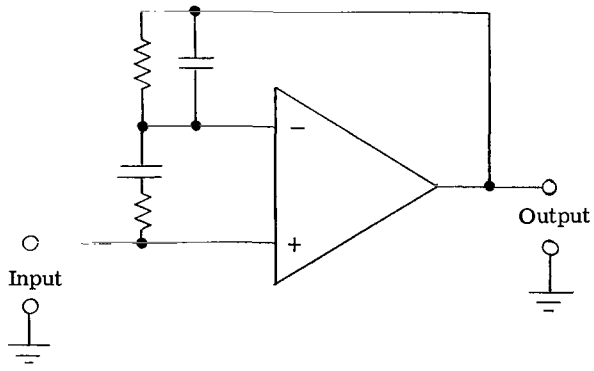
$$\frac{R' + r'}{r'} = \frac{f_1}{f_1'}$$

or

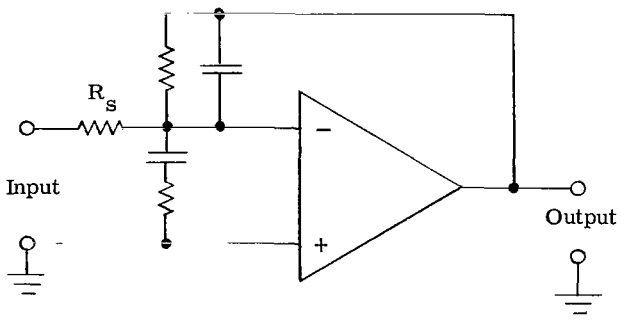
$$R' = \left[\frac{f_1}{f_1'} - 1\right] r'$$

Full compensation requires that R' be 900 ohms. Finally, the reactance of c' must equal R' at frequency f_2 in order to cancel that corner. Since f_2 is 10^7 hertz, c' should be 16 picofarads. Table II(b) lists values for C', R', c', and r' for other values of k also.

A third method of phase compensation is to put all or part of the compensation into the feedback network. This method is sometimes called closed-loop compensation to distinguish it from the methods already discussed, in which compensation was achieved by altering the open-loop response of the amplifier. The circuits used in closed-loop compensation are closely related to the circuit in figure 15. This similarity is even more apparent in figure 16. An open-loop phase-compensated unity-gain follower (voltage gain of +1)(fig. 16(a)) is compared with an inverting amplifier with closed-loop compensation (fig. 16(b)). Again, pole-zero cancellation has been used to change the system response.



(a) Unity-gain follower with open-loop phase compensation.



(b) Inverting amplifier with closed-loop compensation.

Figure 16. - Similarity between open-loop and closed-loop compensation circuits.

Equation (8) does not apply to closed-loop-compensated circuits because the feedback networks are not purely resistive. This fact reveals the chief disadvantage of closed-loop compensation: The values of the components used in the compensation network are uniquely dependent on the closed-loop gain of the amplifier stage and on the particular choice of resistance values used to achieve that gain. For this reason, closed-loop compensation is often best accomplished by a semiempirical approach.

The choice of which type of phase compensation to use depends partly on the use to which the amplifier is put. The advantage of phase compensation by the circuit shown in figure 14 is that only one resistor and one capacitor are needed. The disadvantage of this method is that the slewing rate is greatly reduced. For example, the slewing rate of the test amplifier with full compensation by this method ($k = 1$ in table II(a)) is only 14 volts per microsecond as compared with 140 volts per microsecond for the uncompensated amplifier.

Phase compensation by the circuit shown in figure 15 or by closed-loop compensation does not degrade the output slewing rate. But a disadvantage of these methods is that noise generated within the amplifier is passed on to the output unattenuated. These methods of compensation would therefore not be used in a low-level amplifier where noise is a consideration.

PRACTICAL CIRCUITS

The circuits described in this section were chosen to show how operational amplifier techniques can be used in pulse amplifiers. These circuits also show how phase compensation can be applied to real circuits. Unless otherwise noted, the amplifier indicated by the differential amplifier symbol (fig. 1, p. 2) is the test amplifier of table I.

Gain-of-10 Voltage Amplifier

Figure 17 shows schematically a voltage amplifier with a gain of 10 and a rise time of about 20 nanoseconds (1 nsec = 10^{-9} sec). The values of resistance and capacitance used in the compensating network are standard values nearest those listed in table II(b) for $k = 0.1$.

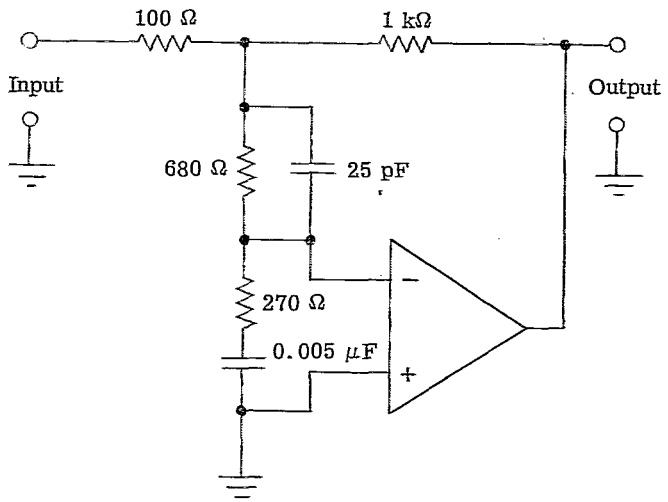


Figure 17. - Gain-of-10 voltage amplifier.

Differential Voltage Amplifier

Figure 18 shows a differential voltage amplifier with a gain of 5. The network consisting of the 1-kilohm, 5-kilohm, 164-ohm, and 820-ohm resistors was chosen to give good common-mode rejection and equal input terminal impedances (1000 Ω). Differential amplifiers are used to reject cable noise pickup and to switch pulse polarity.

The phase compensation consists of the attenuation from the 470-ohm resistor and the 0.005-microfarad capacitor across the amplifier input terminals and from the 3.6-picofarad phase-lead capacitor. This circuit is an example of closed-loop compen-

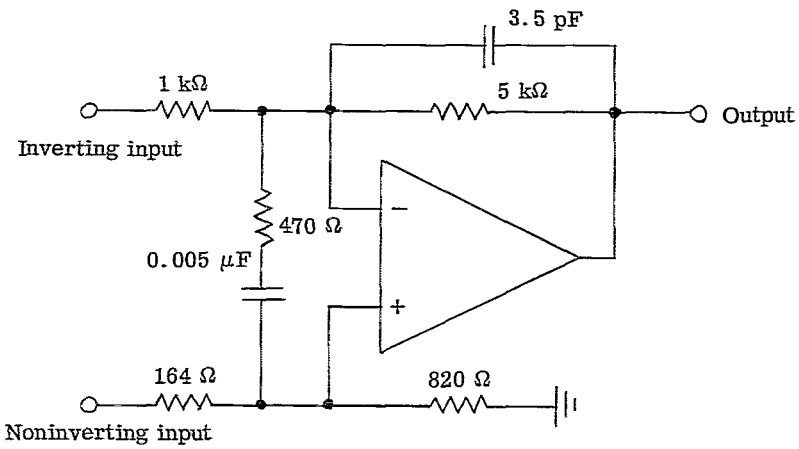


Figure 18. - Gain-of-5 differential amplifier.

sation. The odd value of the 3.6-picofarad capacitor was determined experimentally to produce the optimum pulse shape at the amplifier output. This amplifier also shows a rise time of about 20 nanoseconds.

Pulse-Shaping Amplifier

Linear pulse amplifiers usually have one or more pulse-shaping stages. Figure 19 shows a pulse-shaping voltage amplifier stage that contains a differentiating RC network (3.6 kΩ in series with 275 pF) followed by an integrating RC network (100 pF in parallel with 10 kΩ). The values of resistance and capacitance in each of these networks provide a voltage gain of -1 and time constants of 1 microsecond each. The phase-compensation network consists of the 910- and 100-ohm resistors and the 15-picofarad and 0.02 microfarad capacitors. The 11-kilohm resistor to ground from the positive amplifier input cancels the dc offset voltage caused by amplifier input bias currents.

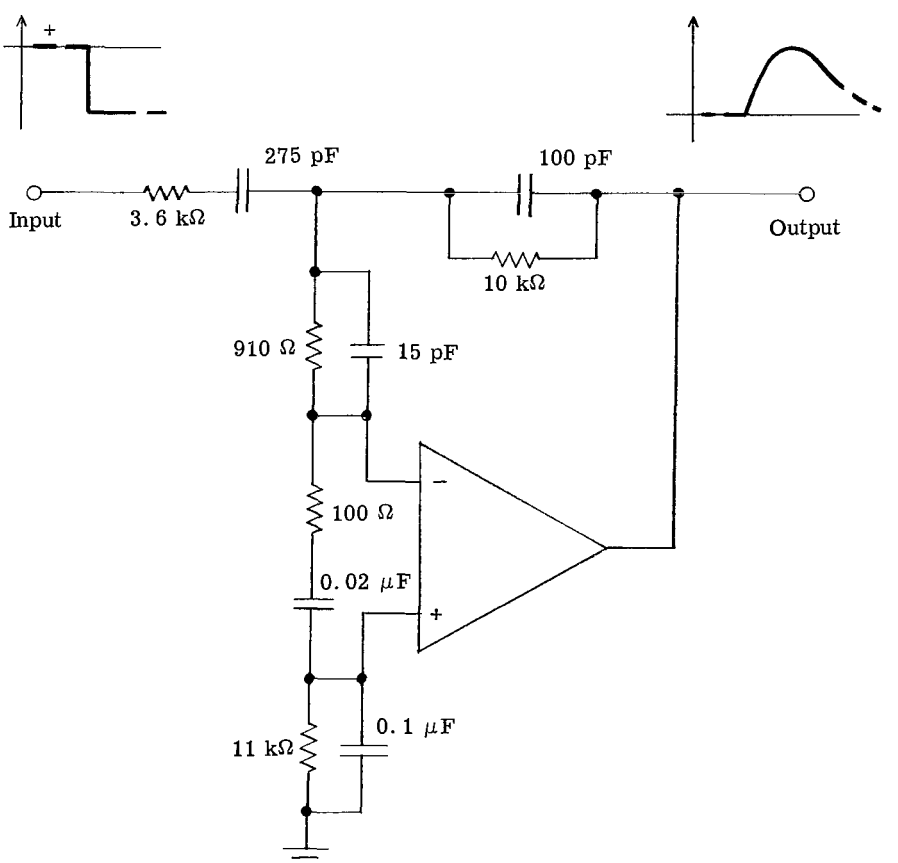


Figure 19. - Pulse-shaping amplifier. Values shown provide voltage gain of -1 and differentiating and integrating times of 1 microsecond.

High-Level, Low-Impedance Amplifier

One of the most difficult amplifier stages to design is the output stage. The output stage of a linear pulse amplifier that uses delay-line pulse shaping is a good example of extreme circuit requirements. The following requirements are typical of those encountered:

(1) The capability to drive terminated coaxial cables with impedances as low as 50 ohms

(2) The ability to handle pulses with amplitudes to ±10 volts

(3) The ability to handle bipolar pulses (pulses that swing both positively and negatively in voltage about the mean value)

(4) A rise time of less than 100 nanoseconds

The test amplifier considered herein is not able to meet these requirements. In the first place, the sink current in resistor R3 (fig. 2) is too small to drive a 50-ohm load. And it cannot be made sufficiently large without destroying transistor Q3. Secondly, the ability to handle large pulses with short rise times requires a high slewing rate. A 10-volt pulse of 100-nanosecond rise time has in initial slope of about 200 volts per mi-

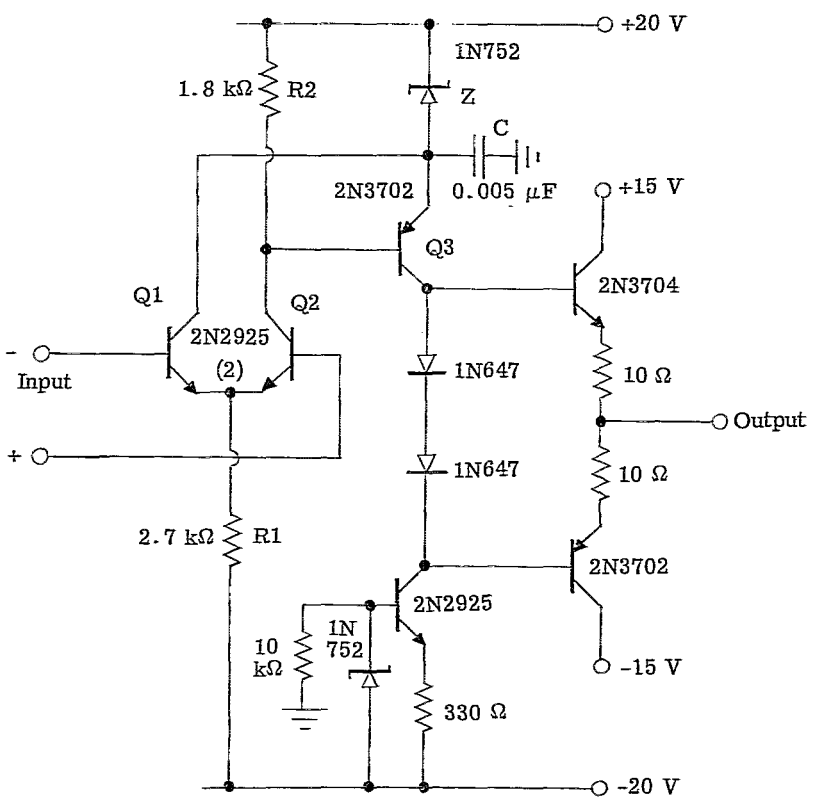


Figure 20. - Circuit diagram of test amplifier as modified for output-stage use.

crosecond, which is greater than the slewing-rate limit of the test amplifier.

The amplifier circuit in figure 20 is an extension of the basic circuit that was designed to meet the four requirements previously listed. This circuit contains all the components of figure 2 except R3, and these components are labeled the same in both figures.

The most important change in the circuit is the addition of the two output transistors. These transistors act as current boosters which make it possible to drive low-impedance cables. The two 10-ohm resistors in the emitter leads of these transistors and the two 1N647 silicon diodes produce the proper bias currents under zero output conditions.

The other circuit modification is the replacement of R3 with a constant current sink consisting of a 2N2925 transistor, a Zener diode, and the 330-ohm and 10-kilohm resistors. This change makes possible a full swing in output voltage to -10 volts. The current into this sink has been increased over that produced by the 4.7-kilohm value of R3 in the test amplifier. Similarly, the currents in Q1 and Q2 have been increased by reducing the size of R1 and R2. These changes were made to increase the slewing-rate capability of the amplifier. The open-loop frequency response of the modified amplifier differs from that shown in figure 6. As a result, values shown in figure 21 in the compensation network differ from those given in table II(b) for the test amplifier.

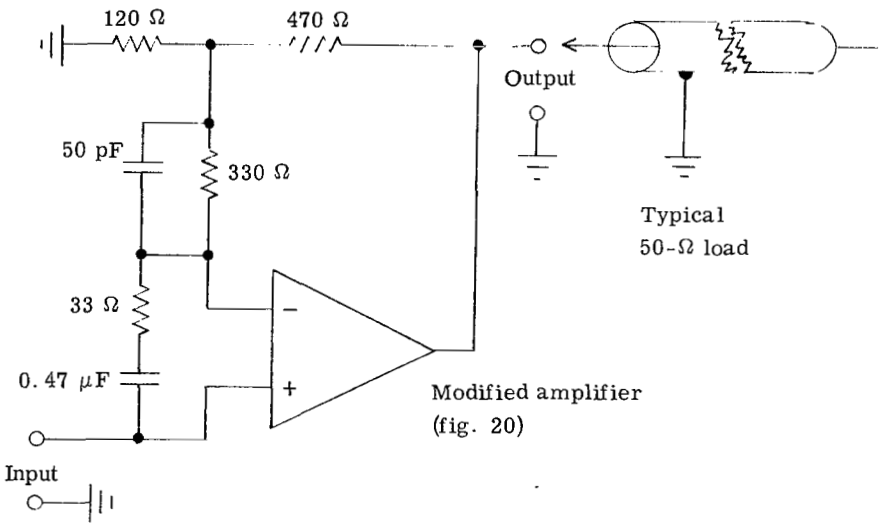


Figure 21. - Gain-of-5 voltage amplifier which uses operational amplifier shown in figure 20.

CONCLUDING REMARKS

A simple operational amplifier built from discrete components was described. The use of this amplifier was shown by giving specific circuit examples. Particular attention was given to the problem of phase compensation and to the matter of amplifier slewing rate.

As integrated-circuit operational amplifiers with high-frequency response become available, it can be expected that they will be widely used in nuclear instruments. Here too, it is important to consider the amplifier open-loop properties in order to realize the full frequency capabilities of each circuit. The methods described herein are applicable to these circuits as well as to discrete component amplifiers.

Lewis Research Center,
National Aeronautics and Space Administration,
Cleveland, Ohio, October 31, 1967,
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