Report No. 03-68-14

Seventh Quarterly Report

for

PHOTON-COUPLED ISOLATION SWITCH

(1 July to 30 September 1967)

Contract No. 951340

Prepared by

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Jet Propulsion Laboratory
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ABSTRACT

The photon-coupled isolation switch is a new type of semiconductor device which uses internal optical coupling to obtain electrical isolation between the driving source and the output terminals. Internal photon generation and detection techniques are used which combine a gallium arsenide (GaAs) photon-emitting diode with a silicon (Si) phototransistor. A third semiconductor wafer in the isolation switch is a monolithic Si driver circuit for supplying bias to the GaAs diode. The driver circuit uses DTL circuitry to provide for up to ten inputs.

This development program consists of two phases:

Phase I, development of the GaAs photon-emitting diode-Si phototransistor pair (GaAs switch) and the design of the driver circuit.

Phase II, integration of the driver circuit and prototype production of the complete isolation switch.

Previously Phase I was completed with development of the GaAs switch and completion of the design evaluation of the driver circuit. Twenty GaAs switches and a breadboard of the driver circuit were delivered for evaluation. Under Phase II a layout of components for the driver circuit was made, and diffusion and metallization masks were designed.

During the last quarter of the program the masks were fabricated, and processing of the integrated driver circuit was begun. Initially, marginal driver-circuit wafers were used in fabricating sample complete isolation switches. Preliminary measurements indicate that recent driver-circuit wafers meet the design criteria.

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SECTION I
INTRODUCTION

Under development is a solid-state device having output terminals which are electrically isolated from the driving source and other terminals of the switch. The isolation switch embodies internal optical coupling between a solid-state light emitter-detector pair to achieve signal transmission without electrical connections.

Isolation through internal optical coupling has previously been used in development of several other types of devices using the same type of light emitter-detector system. These devices include an isolated-input transistor, an isolated-gate PNPN-type switch, a multiplex switch not requiring a driving transformer, and an isolated-input pulse amplifier [1,2,3]. Each of these devices uses a gallium arsenide (GaAs) PN junction diode as the photon generator and a silicon (Si) PN junction diode as the photodetector. This optical pair has been found to produce the most efficient signal coupling of the available semiconductor systems.

The present isolation switch contains three wafers: a monolithic Si driver circuit, a GaAs photon-emitting diode, and a Si phototransistor. The driver circuit is designed as a DTL gate, providing for up to ten inputs. The output of the driver circuit is connected to the photon-emitting diode to control its bias current and thereby the photon emission. The GaAs diode is attached to the Si phototransistor with a high-refractive-index glass which provides optical transmission and electrical isolation.

This development program is divided into two phases. In Phase I the emitting diode-phototransistor pair (GaAs switch) is developed and the driver circuit is designed. In Phase II of the program the driver circuit is produced, and the three-wafer isolation switch is assembled in an integrated-circuit flat package. Phase I was completed [4] with the delivery of GaAs switches which met the design criteria of this subsection of the isolation switch. The design and breadboard analysis of the driver circuit were also completed. The design criteria and design equations for the driver circuit were described [5].

Previously, under Phase II, the integrated-circuit layout was developed for components of the driver circuit, and diffusion and metallization masks were designed. In the quarter of the program covered by this report, integrated driver circuits were made which, to judge from preliminary tests, appear to meet the design criteria. Initial marginal driver-circuit monolithic wafers were used in the fabrication of sample complete isolation switches.

SECTION II

TECHNICAL DISCUSSION

A. DRIVER CIRCUIT

1. Processing

Seven diffusion masks were designed for processing the integrated driver circuit [5]. Major processing steps are shown in Figure 1. The processing procedure is as follows:

a. Oxidize the slice. Use KMER with mask 1. Perform oxide removal and N-type diffusion into the P-type substrate. This forms the transistor collectors and resistor isolation tanks.

b. Re-oxidize the slice. Use KMER with mask 2. Perform oxide removal and P-type diffusions into the previous N-diffusions. This forms the transistor bases and the resistors.

c. Re-oxidize the slice, and use KMER with mask 3. Perform oxide removal and N-type diffusion into the P-diffusions of the transistors. This forms the transistor emitters.

d. Re-oxidize the slice, and use KMER with mask 4. Perform oxide removal, revealing the silicon areas which are to be metallized.

e. Evaporate metal over the slice. Use KMER with mask 5, leaving only metal within the oxide windows of step d, with pads for each for probing. At this point measurements can be made of the circuit parameters in slice form.

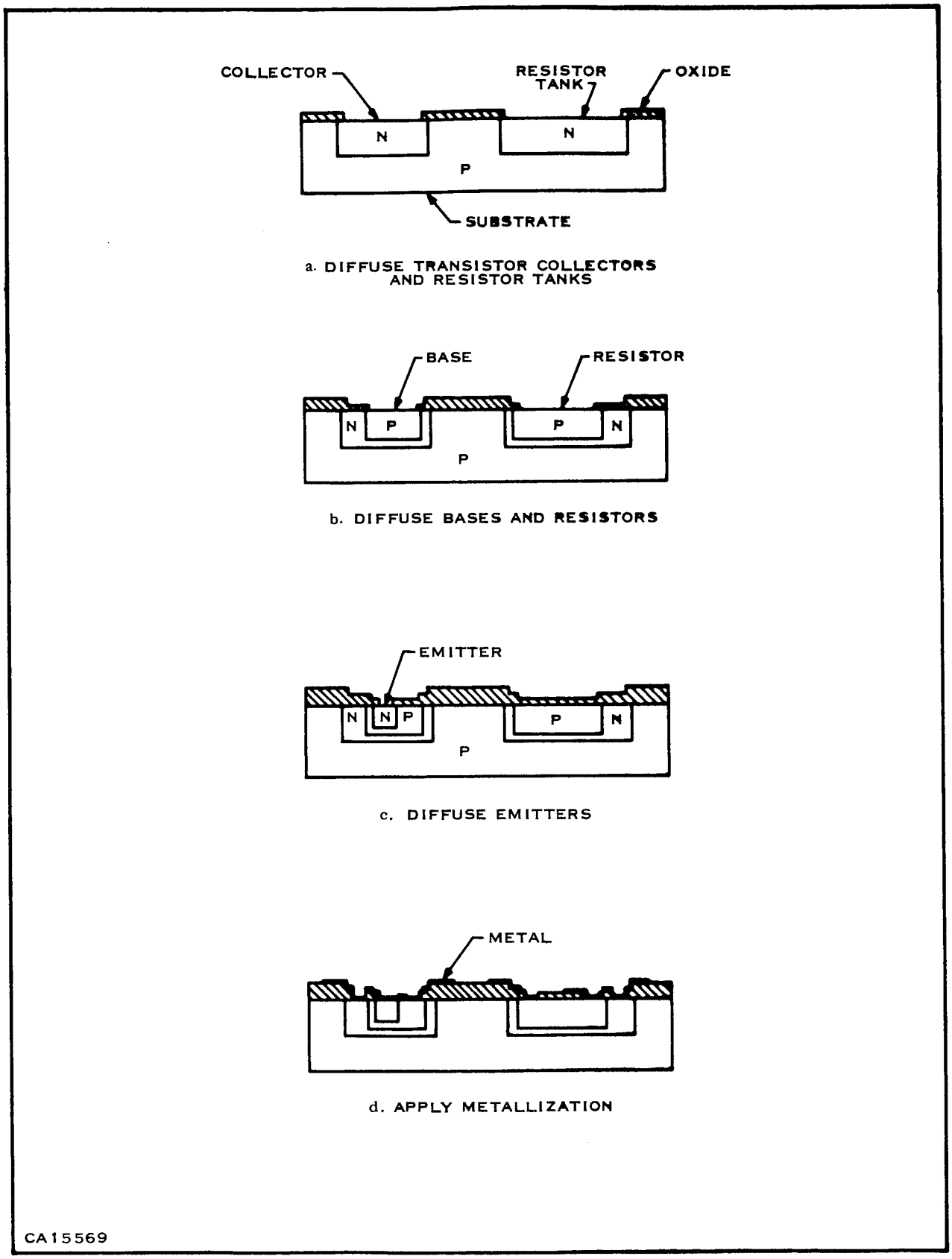

Figure 1. Major Processing Steps for Driver Circuit

f. Measure the circuit resistors to establish which of two resistance ranges has been produced within the manufacturing tolerance. Remetallize the slices and apply KMER. Use either mask 6 or 7 as appropriate for forming the interconnection pattern and selecting the proper resistor taps.

Many evaluations are made during processing. One important test is concerned with the forward current gains of the transistors. After step c a portion of a slice is taken from the lot, and all oxide is removed. Transistor current gains are measured by probing directly to the diffused regions. As indicated in step f, measurements of the resistors are needed to set the values within the range used in the worst-case analysis [5]. The values of most corresponding resistors in an entire diffusion run fall within a narrow range. A wider production tolerance is obtained when a significant number of runs is involved. Establishing the particular resistivity range for a given lot allows the choice between two metallization patterns. This determines the taps employed and the resistor limits for the lot.

2. Device Results

A completed driver-circuit wafer is shown in Figure 2. Individual components on the wafer can be identified with reference to the composite drawing of the diffusion masks in Figure 3 and the circuit schematic in Figure 4. A detailed discussion of the layout was previously presented [5].

For the first lot of driver circuits the resistor values were in the proper range, but transistor collection-emitter breakdown voltages were low. Processing of these devices was continued through fabrication of sample complete isolation switches. For the second lot of circuits, preliminary tests indicate that the parameters are within design limits. Fabrications and additional tests are in process.

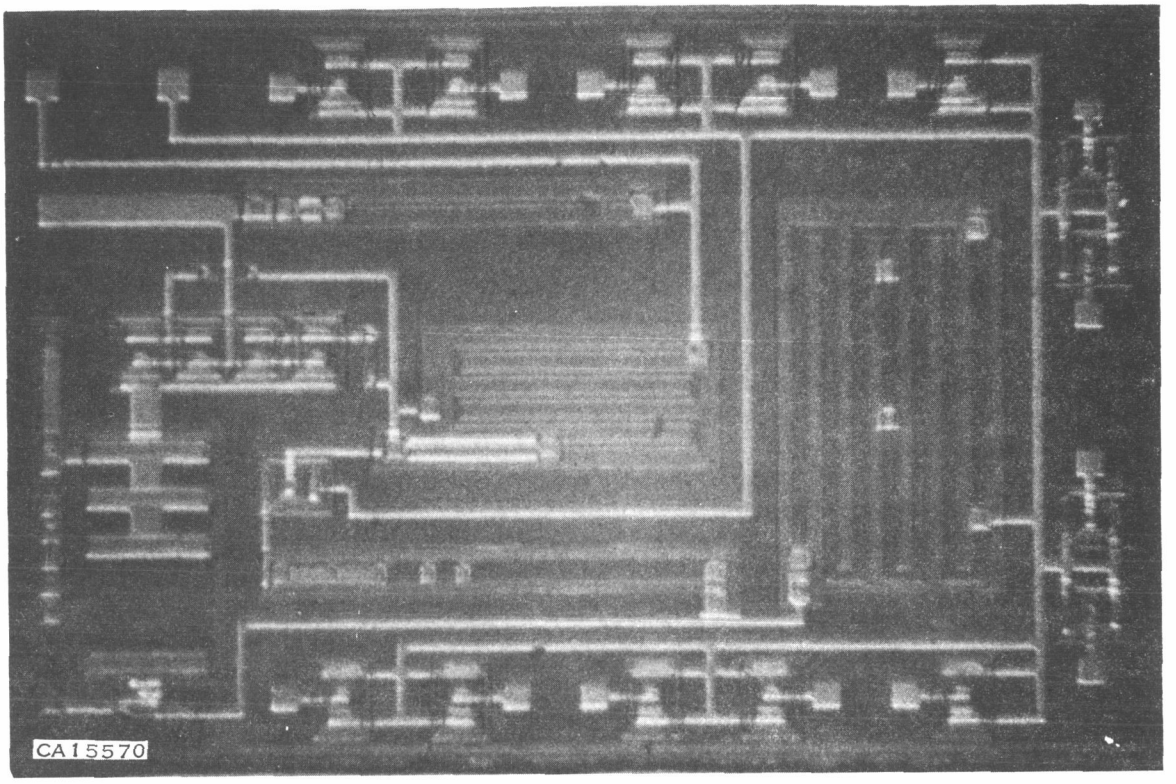

Figure 2. Driver-Circuit Wafer

Individual driver circuits are probed on the slice for overall evaluation. A circuit terminal characteristic in the on-condition, the voltage between the supply voltage terminal and the emitter of Q_2, is measured for values of current of 23 mA and 40 mA. These values correspond to the worst-case limits of GaAs photon-emitting diode current for the minimum and maximum values of supply voltage. The yield of driver-circuit wafers from the recent lot appears to be good.

B. ISOLATION-SWITCH ASSEMBLY

Parts assembled to form the complete isolation switch, shown in Figure 5, include the driver circuit, phototransistor, light-emitting diode wafers, two ceramic mounts, and a 14-lead TO-84 integrated-circuit header. Other parts not shown include the high refractive index glass which bonds the phototransistor and GaAs diode, bonding leads, and solder preforms. An assembled isolation switch is

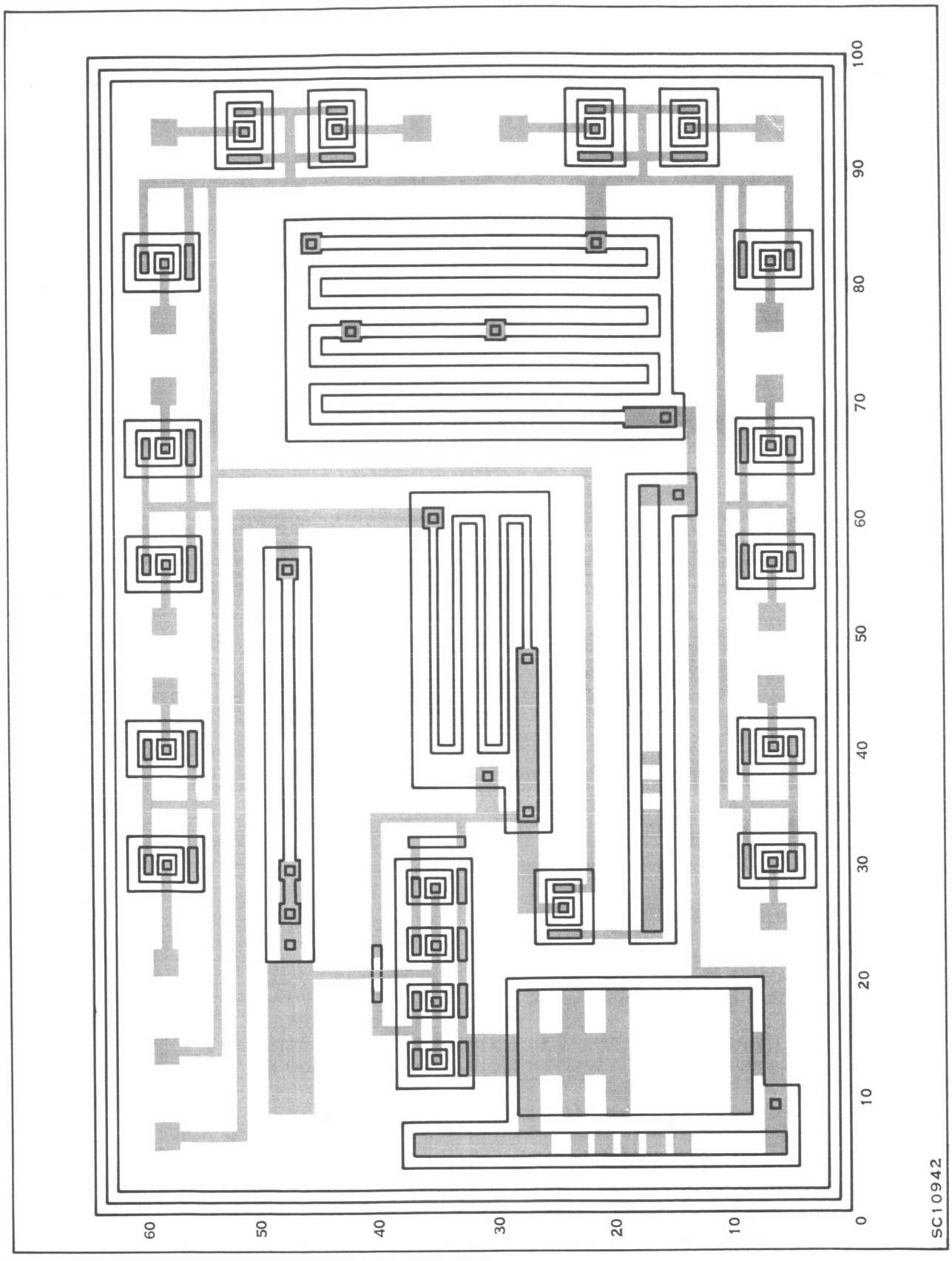

Figure 3. Driver-Circuit Component Layout

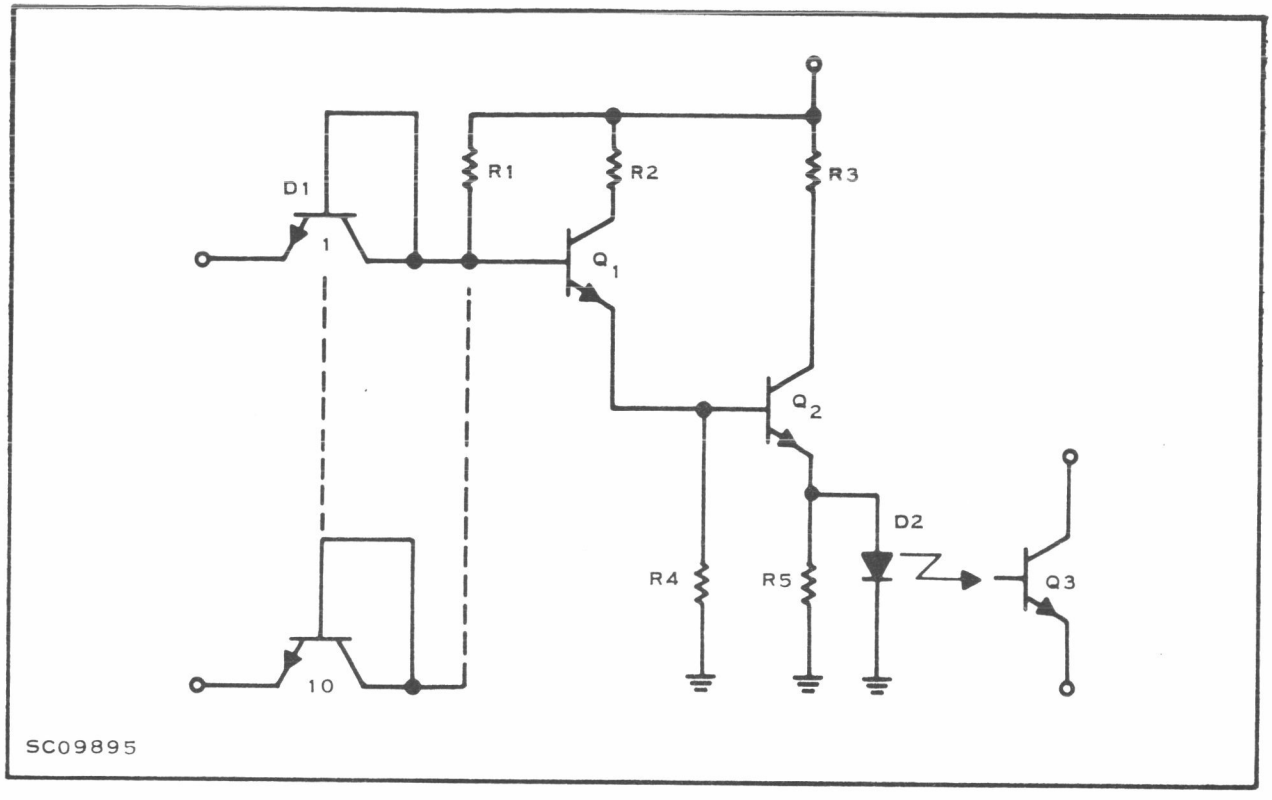

Figure 4. Isolation-Switch Schematic

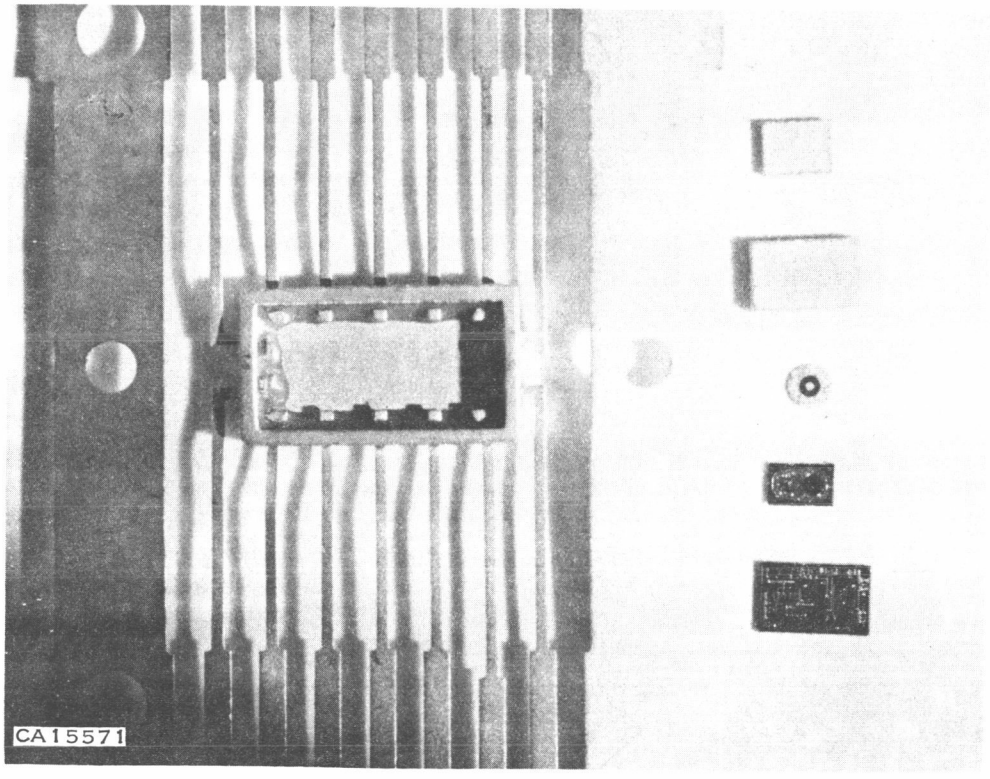

Figure 5. Isolation-Switch Parts

shown in Figure 6. The driver circuit was from the first run described in the previous section. The major assembly steps of the isolation switch are seen in Figure 7. The assembly procedure is as follows:

a. Solder the phototransistor and driver-circuit wafers to the ceramic submounts.

b. Solder the two metallized ceramic submounts into the header. The positions of the ceramics correspond to the location of the phototransistor and driver-circuit wafers in Figure 6.

c. Bond leads between appropriate pads on the phototransistor and driver-circuit wafers and the header pads.

d. Bond leads to the unmounted emitting diode wafer.

e. Mount the emitting diode to the sensitive region of the phototransistor with the high-refractive-index glass.

f. Bond the appropriate leads of the emitting diode to the header and driver circuit.

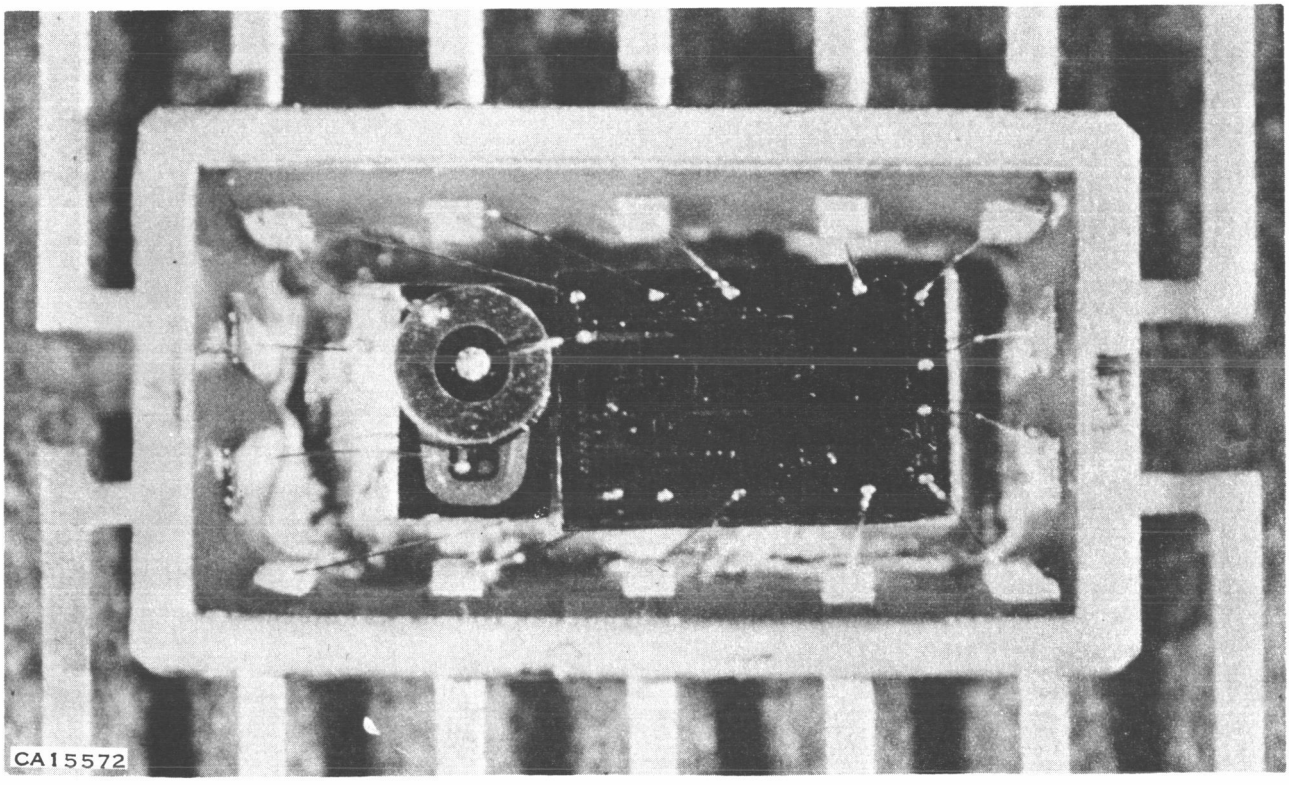

Figure 6. Internal View of Assembled Isolation Switch

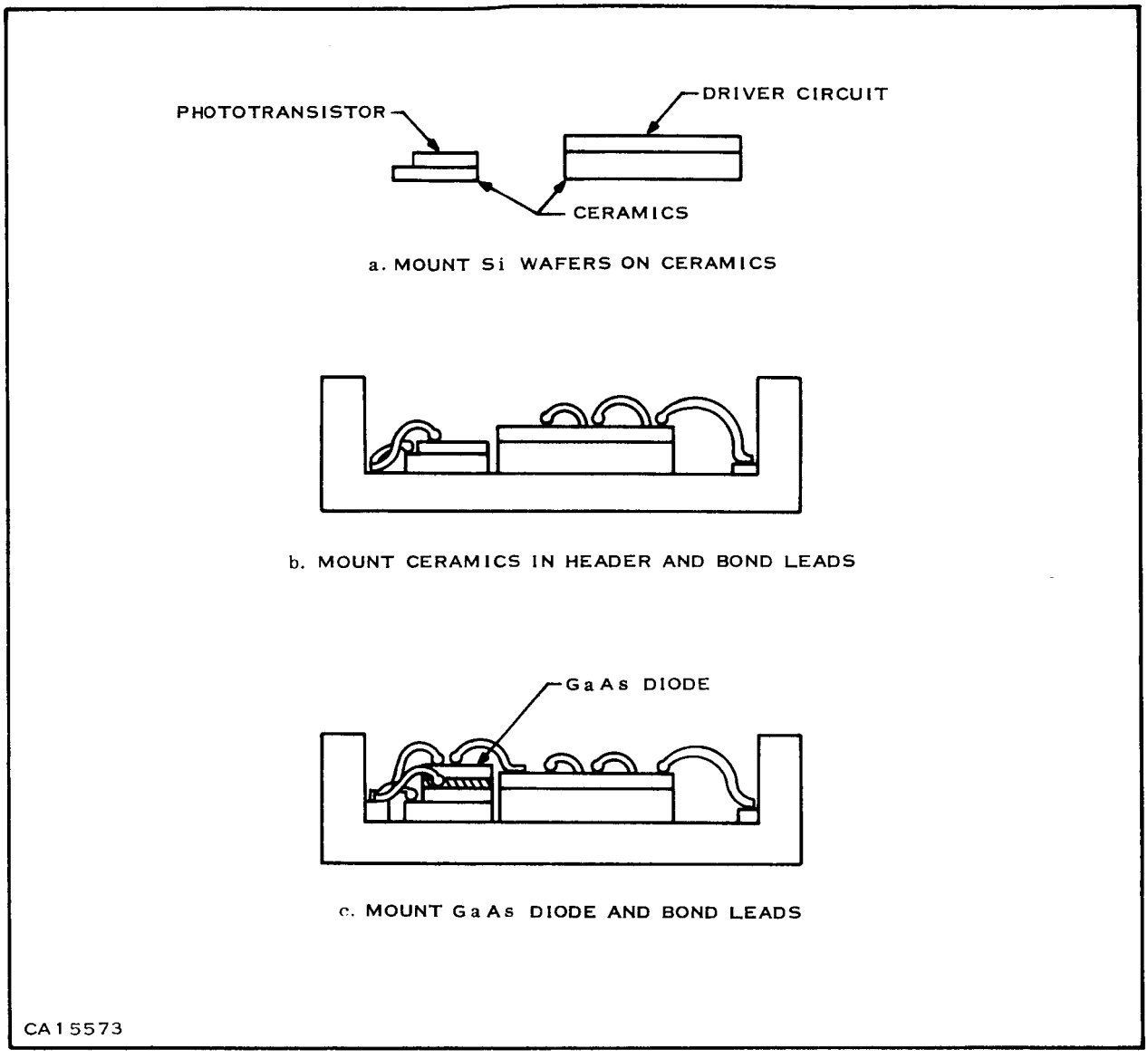

Figure 7. Major Assembly Steps for Isolation Switch

g. Cover the periphery of the emitting diode with epoxy.

h. Hermetically can the package.

The thickness of the ceramic submount for the phototransistor was made less than that for the driver circuit to allow butting of the ceramics without shorting of the metallizations. This provides sufficient clearance for the bonding wires which pass near or over the phototransistor wafer. Positioning of the parts in one end of the header, as shown in Figure 6, minimizes the lead lengths for bonds in this part of the header.

Bonding in the isolation switch is considered a monometallic system. Although aluminum and gold are presently used for metallization on the phototransistor and driver circuit, respectively, the corresponding type of bonding lead is used to each wafer. Actually all bonding leads are gold except for one aluminum lead required for the phototransistor emitter contact. Aluminum metallization is now used for the phototransistor because it requires a less complex technique of metal application for low surface leakage.

SECTION III

CONCLUSIONS AND RECOMMENDATIONS

Diffusion and metallization masks for integration of the driver circuit have been received, and processing has begun. Preliminary tests indicate that the last run of monolithic driver-circuit wafers meets the design criteria. Additional testing and isolation-switch fabrication are in process.

SECTION IV

REFERENCES

1. J. R. Biard and W. T. Matzen, "Advanced Functional Electronic Block Development, "Texas Instruments Incorporated, Contract No. AF 33(657)-9824, Report No. RTD-TDR-63-4203, January 1964.

2. J. R. Biard et al., "Optoelectronics as Applied to Functional Electronic Blocks, IEEE Proceedings, V 52, No. 12, pp. 1529-1536, December 1964.

3. "Integrated Electronic Gating System for Multiplexing Applications", IBM, JPL Contract No. 950492, 15 December, 1964.

4. E. L. Bonin, "Photon Coupled Isolation Switch, "Texas Instruments Incorporated, JPL Contract No. 951340, Fifth Quarterly Report, 1 January to 31 March, 1967.

5. E. L. Bonin and E. E. Harp, "Photon Coupled Isolation Switch", Texas Instruments Incorporated, JPL Contract No. 951340, Sixth Quarterly Report, 1 April to 30 June, 1967.