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SST TELEMETRY SIMULATOR

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ABSTRACT

As a component of the Goddard Space Flight Center PPM Telemetry ground station, the SST Telemetry Simulator provides an output simulating the demodulated PPM signal to the Servo Clock. Other outputs are similar to those of the Servo Clock. Clock rates of five, ten, or twenty kilohertz are selected by means of externally switched voltages to the appropriate internal relays.

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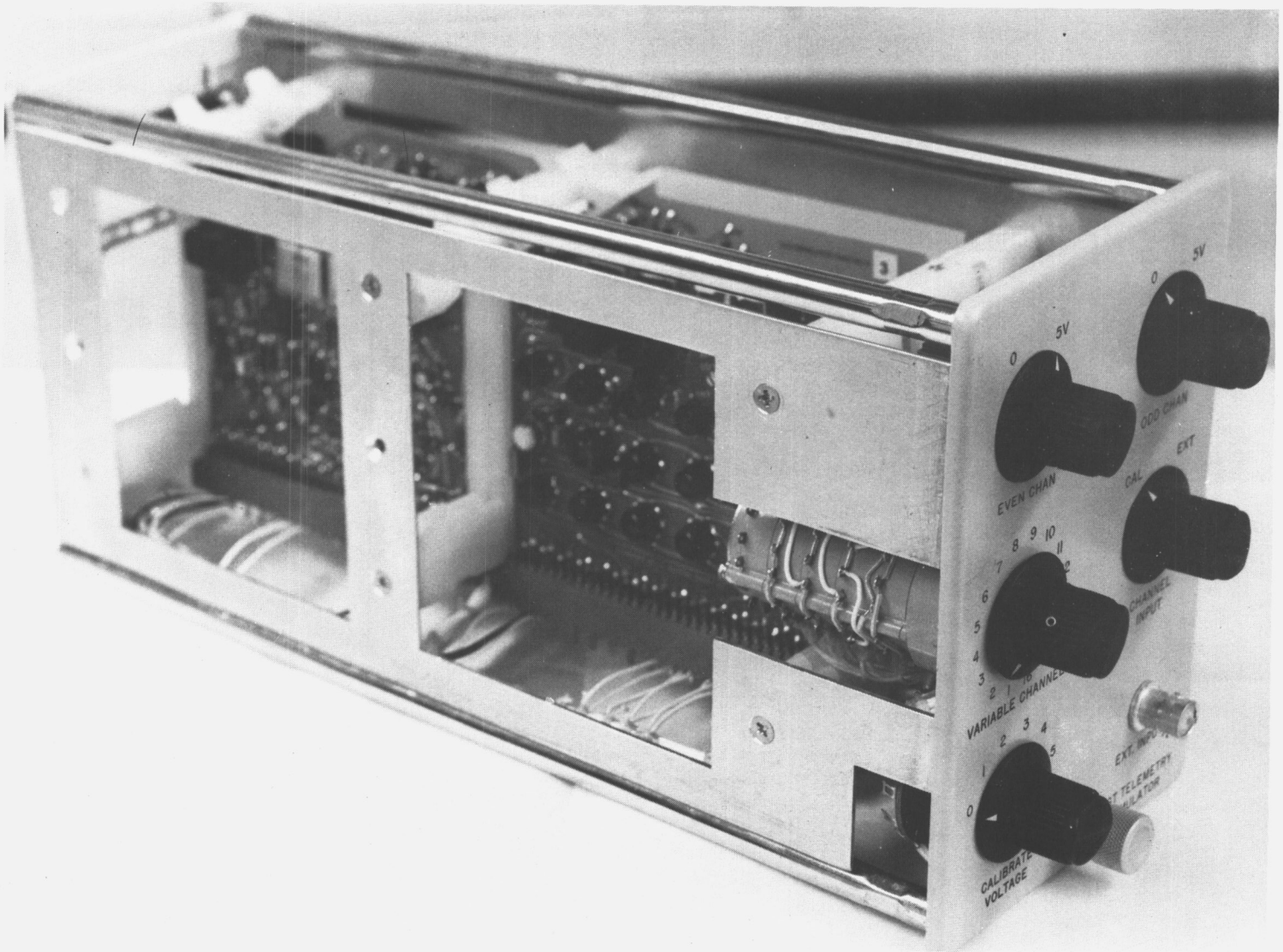


Frontispiece. SST Telemetry Simulator

SST TELEMETRY SIMULATOR

INTRODUCTION

The SST Telemetry Simulator is part of the PPM Ground Station at Goddard Space Flight Center. It produces a signal whose format simulates the demodulated data from the SST-3 Telemetry Transmitter, as well as certain related signals, useful in the adjustment of the ground station.

PPM SYSTEM

The PPM telemetry system used by Goddard is a time-sharing multiplex system in which a pulse-position/amplitude-modulation (PPM/AM) system is employed. In this system, the transmitter output is pulse modulated radio frequency, with full amplitude for a pulse, and zero amplitude in the absence of a pulse. Each of sixteen channels is supplied with data in the form of a voltage in the zero-to-five volts range. Each channel in turn is gated ON, and a pulse is generated. The timing of the pulse, relative to the total ON time for that channel, is a linear function of the input voltage.

The system output consists of a three-microsecond data pulse for each channel, plus a triple pulse at the beginning of CHANNEL 1. The total time reserved for each channel is the reciprocal of the clock rate. The total frame time is sixteen times the time for each channel.

TELEMETER. An unusual part of the Telemeter is the PPM encoder. This contains: a five kilohertz clock; a four-state counter and a matrix connected to 16 gates; a sawtooth generator, operating at the clock frequency and connected to all the gates; and a pulse generator. The counter-matrix combination ENABLES each gate, in turn. At the time that the sawtooth voltage is equal to the data input voltage, a gate output, which triggers the pulse generator, is produced. An output of the last counter stage triggers the triple generator at the beginning of Channel 1.

GROUND STATION. The ground station is capable of decommuting the PPM signal, or separating it by channels. This capability is made possible by the SERVO CLOCK, which is slaved to the clock in the transmitter, and which

times the channel gates. This clock contains a voltage controlled oscillator whose output frequency is eight times that of the clock, and an eight-to-one divider to provide the clock frequency. The clock output is connected to a one-shot multivibrator to provide the channel reference pulses, and is divided down by a sixteen-to-one counter, the output of which is fed to another one-shot multivibrator to generate the frame-reference-pulse. A phase comparator is used to compare the timing of the frame-reference-pulse with that of a pulse derived from the received triple pulse. Any timing difference produces an output voltage whose polarity causes the output frequency of the voltage-controlled oscillator to change so that the frame-reference-pulse and the triple pulse from the received signal will be locked together in the correct phase relationship. Data pulses and channel reference pulses from the servo clock are fed to PPM/binary and PPM/analog converters for conversion into one or both of these conventional forms in which data are stored.

FUNCTION OF THE TELEMETRY SIMULATOR

Figure 1 shows the relationship of the simulator to the operational components of the ground station. By using the simulator, the operator of the PPM ground station is able to adjust the station for best operation in the absence of received telemetry signals. It can substitute for the telemetry receiver, supplying simulated data in the normal PPM format. Alternately, it is able to supply to the system the outputs normally supplied by the servo clock. When doing this, it substitutes for the telemetry receiver and for the servo clock.

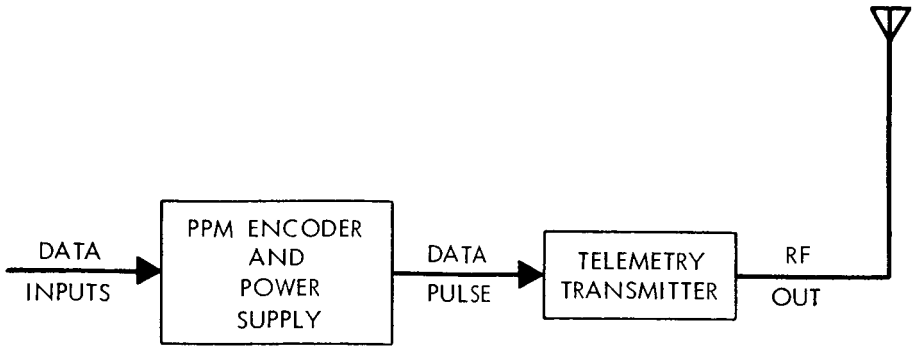
PHYSICAL DESCRIPTION

CHASSIS

The Simulator package is a six inch by four inch by twelve inch plug-in chassis, standard throughout the PPM ground station. Slides and connectors are provided for plugging in four standard 31-pin printed circuit cards, which contain all the circuitry except the control switches. A 24-pin connector mounted on the rear of the chassis provides power input and signal output connections. The Frontispiece shows a view of the unit complete with cards; Figure 2 shows the chassis without cards.

PRINTED WIRING CARDS

The printed wiring cards are approximately 4-1/8 inches by 4-3/8 inches, laminated board on which all the wiring and the connector pins have been etched. A lever is provided on one corner of each card to facilitate disengagement of the board from the connector.



SST-3 TELEMETER

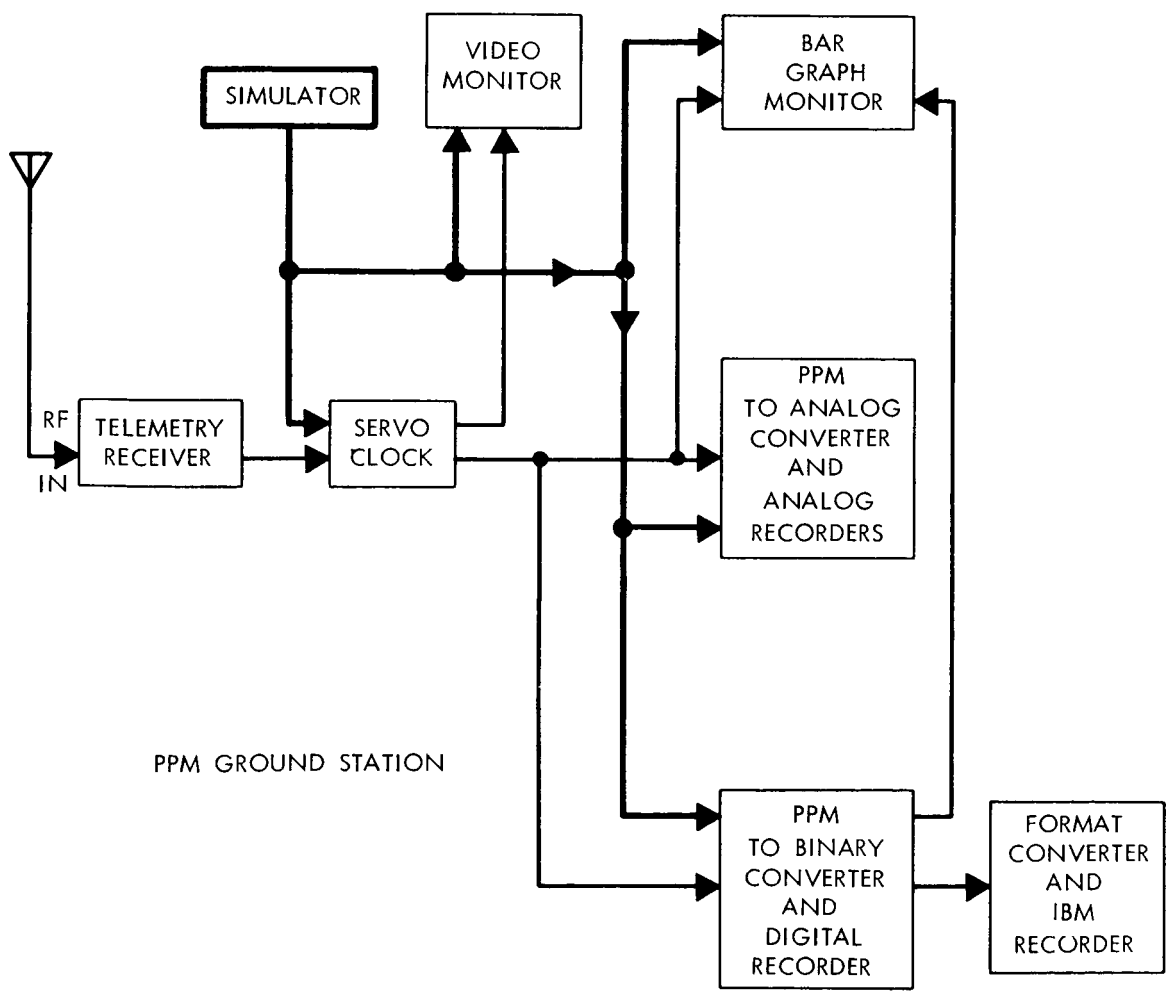


Figure 1. PPM Block Diagram, Showing Use of The Telemetry Simulator

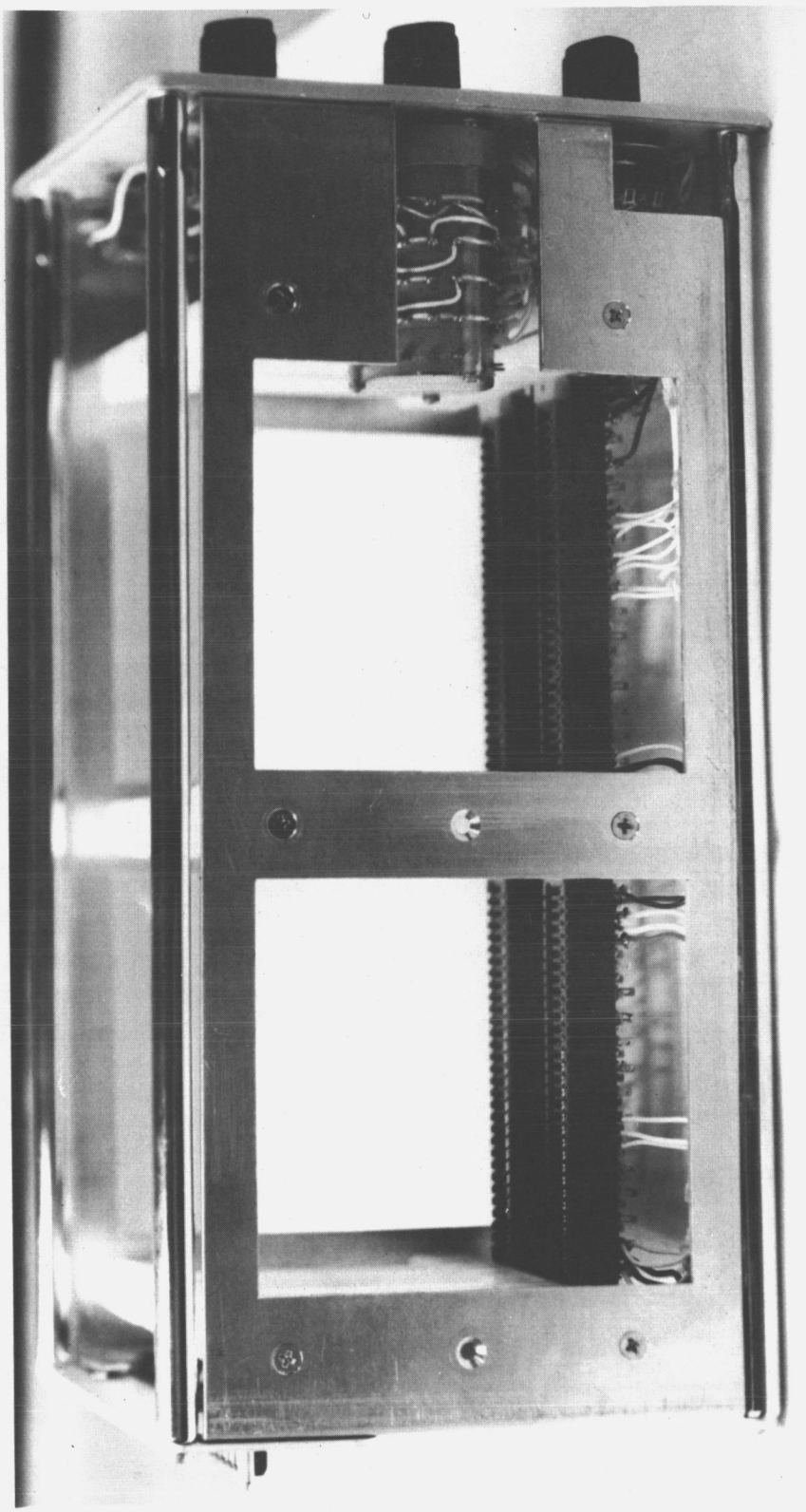


Figure 2. SST Telemetry Simulator, Chassis

FRONT PANEL CONTROLS AND CONNECTOR

The simulator controls and a front-panel connector are installed in holes, line-drilled through the front chassis wall, and through the removable front panel. Names of the controls and designations of their positions (Figure 3) are stencilled on the front panel, as follows:

EVEN CHANNEL. Selects either 0 or 5V as simulated data to be applied to all even numbered channels.

ODD CHANNEL. Selects either 0 or 5V as simulated data to be applied to all odd numbered channels.

VARIABLE CHANNEL. Selects one channel to receive simulated data through the CHANNEL INPUT switch.

CHANNEL INPUT. Selects either CAL (the output of the CALIBRATE VOLTAGE switch) or EXT (the output of whatever external voltage source is connected to the EXT. INPUT connector).

CALIBRATE VOLTAGE. Selects 0, 1, 2, 3, 4, or 5 volts to be placed on the channel selected by the VARIABLE CHANNEL switch, if the CHANNEL INPUT switch is set to CAL.

EXTERNAL INPUT CONNECTOR. A BNC type connector, into which an external voltage may be fed, is connected to the EXT. side of the CHANNEL INPUT switch.

CAPABILITIES

OUTPUT SIGNALS

The SST Telemetry Simulator (Figure 4) provides the following signals needed for the calibration and operating of the PPM ground station:

FORMAT PULSE TRAIN. This consists of a train, representing an entire frame, of 4-microsecond 10-volt positive pulses referenced to zero. It consists of one DATA pulse for each of sixteen channels, and a TRIPLE PULSE at or near the beginning of Channel 1. The TRIPLE PULSE consists of three pulses of the same specifications as above, except that the pulses are separated by 3.9 to 4 microseconds.

DATA PULSE. This output is the same as the FORMAT, except that the TRIPLE PULSE is omitted.

Figure 3. SST Telemetry Simulator, Front Panel

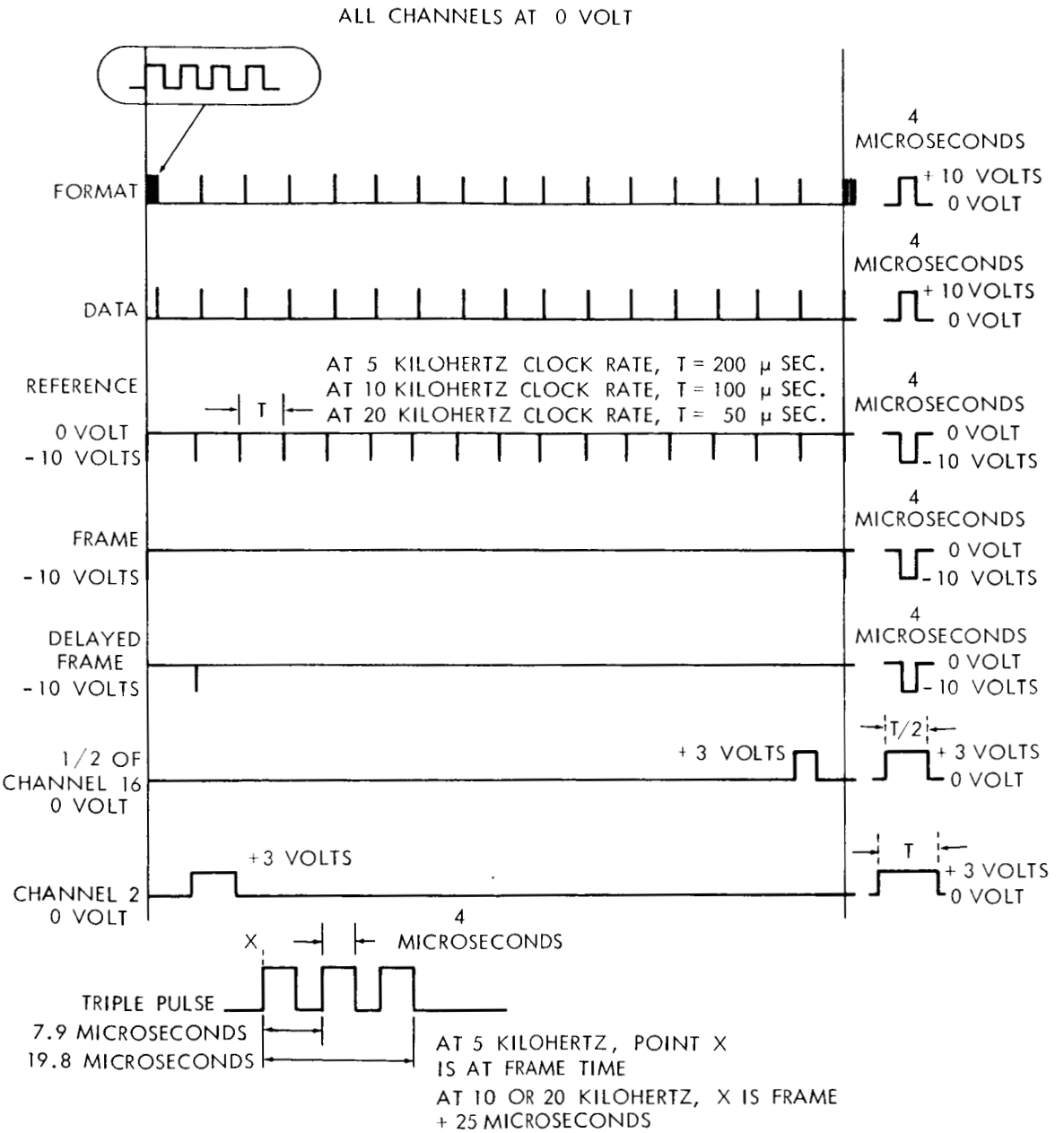


Figure 4. SST Telemetry Simulator, Outputs

REFERENCE PULSE. The reference pulse consists of a 4-microsecond 10-volt negative pulse referenced to zero, occurring at the beginning of each channel.

FRAME PULSE. The FRAME pulse is the same as the REFERENCE pulse, except that it occurs only at the beginning of CHANNEL 1.

DELAYED FRAME PULSE. This pulse occurs at the beginning of CHANNEL 2.

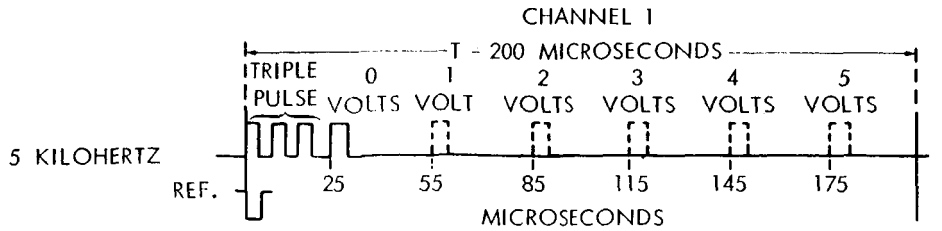
ONE HALF OF CHANNEL 16 PULSE. This is a 3-volt-positive dc pulse occupying the first half of CHANNEL 16 time.

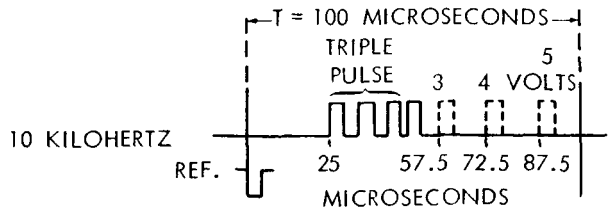
CHANNEL 2 PULSE. This is a 3-volt-positive dc pulse using the entirety of CHANNEL 2 time.

CHANNEL TIMING

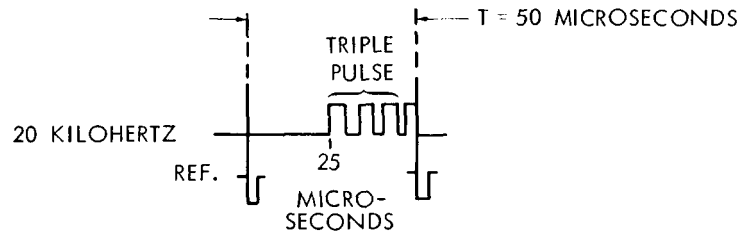
When the simulator operates at a 5-kilohertz clock rate, each channel uses 200 microseconds. A data pulse corresponding to zero volts occurs at 25 microseconds after the beginning of the channel ON time. Each volt increment delays the pulse 30 microseconds, so that a DATA pulse corresponding to +5 volts occurs at 175 microseconds. If any voltage greater than +5.2 volts should be introduced through the EXT. INPUT jack, the DATA pulse is generated by an internal 5.2-volt source, appearing at approximately +181 microseconds. At 10 and 20 kilohertz clock rates, these time delays are divided by two and by four respectively. Figure 5 shows channel time relationships.

CHANNEL 1 TIMING. When the simulator is operated at a 5-kilohertz rate, the TRIPLE PULSE begins at FRAME time, or the beginning of CHANNEL 1, and the three pulses are completed in 20 microseconds. They do not interfere with DATA pulses, since the earliest that it is possible for a data pulse to appear is 25 microseconds after the beginning of the channel. However, when the simulator is operated at either the 10 or the 20-kilohertz clock rate, the appearance of the TRIPLE PULSE is delayed 25 microseconds, bringing the total time to 45 microseconds. An examination of Figure 5 reveals that, with 10-kilohertz operation, DATA points corresponding to zero, one, or two volts would interfere with the TRIPLE PULSE. With 20-kilohertz operation, all DATA points would interfere. Therefore, the simulator is so designed that, if the DATA pulse would have occurred before or during the TRIPLE PULSE, it will appear approximately one microsecond after the TRIPLE PULSE.

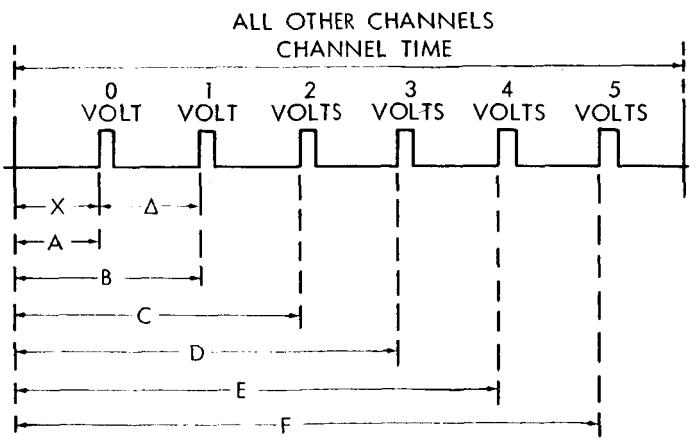




CHANNEL 1 SHOWN
SET 1 MICROSECOND
AFTER TRIPLE PULSE



CHANNEL 1 SHOWN
SET 1 MICROSECOND
AFTER TRIPLE PULSE



CLOCK RATE KILOHERTZ	X	Δ	A	B	C	D	E	F	CHANNEL TIME
5	25	30	25	55	85	115	145	175	200 MICROSECONDS
10	12.5	15	12.5	27.5	42.5	57.5	72.5	87.5	100 MICROSECONDS
20	6.25	7.5	6.25	13.75	21.25	28.75	36.25	43.75	50 MICROSECONDS

Figure 5. Channel Timing

PRINCIPLES OF OPERATION

This section describes the operation of the SST Telemetry Simulator in general terms. Figure A-1, System Block Diagram (contained in the Appendix) should be used as a reference.

SYSTEM CLOCK

The timing of the unit is derived from a 40-kilohertz oscillator, the output of which is divided down by a three-stage counter, to produce square wave outputs of 20, 10, and 5 kilohertz, respectively. Energizing one of two relays connects the system to the 20-kilohertz stage; energizing the other connects it to the 10-kilohertz stage; whereas, with neither relay energized, the system is connected to the 5-kilohertz stage. (The switches controlling these relays are external to the Telemetry Simulator chassis.) Whichever stage is connected to the system, its frequency is said to be the CLOCK rate of the system.

CHANNEL COUNTER AND DERIVED OUTPUTS

The CLOCK drives a four-stage binary counter, designated as the CHANNEL COUNTER. Each of these stages produce two square wave outputs, one of which is the complement of the other. The period of each stage is proportional to its binary "weight", so that we have outputs of 2^0, 2^1 2^2, 2^3, and their complements. (CHANNEL COUNTER waveforms are shown in Figure 6.) The outputs of the CLOCK and the CHANNEL COUNTER are used to synthesize the following five of the seven Simulator outputs.

CHANNEL 2 PULSE. This pulse is generated by gating four appropriate outputs of the CHANNEL COUNTER to give a 3-volt positive-dc pulse output for the duration of the output of CHANNEL 2.

DELAYED FRAME PULSE. The DELAYED FRAME pulse is formed by triggering a four-microsecond one-shot multivibrator with the leading edge of the CHANNEL 2 output, and amplifying and inverting the output of the one-shot multivibrator by means of a pulse driver circuit.

ONE HALF OF CHANNEL 16 PULSE. This dc level is generated by gating four outputs of the CHANNEL COUNTER and one CLOCK output. The output of the gate is +3 volts for the first half of CHANNEL 16.

FRAME PULSE. This pulse is generated by triggering a four microsecond one-shot multivibrator with output of the CHANNEL COUNTER complement or "zero" side of the 2^3 flip-flop. The output of the one-shot multivibrator is amplified and inverted by the driver circuit.

AT 5 KILOHERTZ, T = 200 MICROSECONDS
AT 10 KILOHERTZ, T = 100 MICROSECONDS
AT 20 KILOHERTZ, T = 50 MICROSECONDS

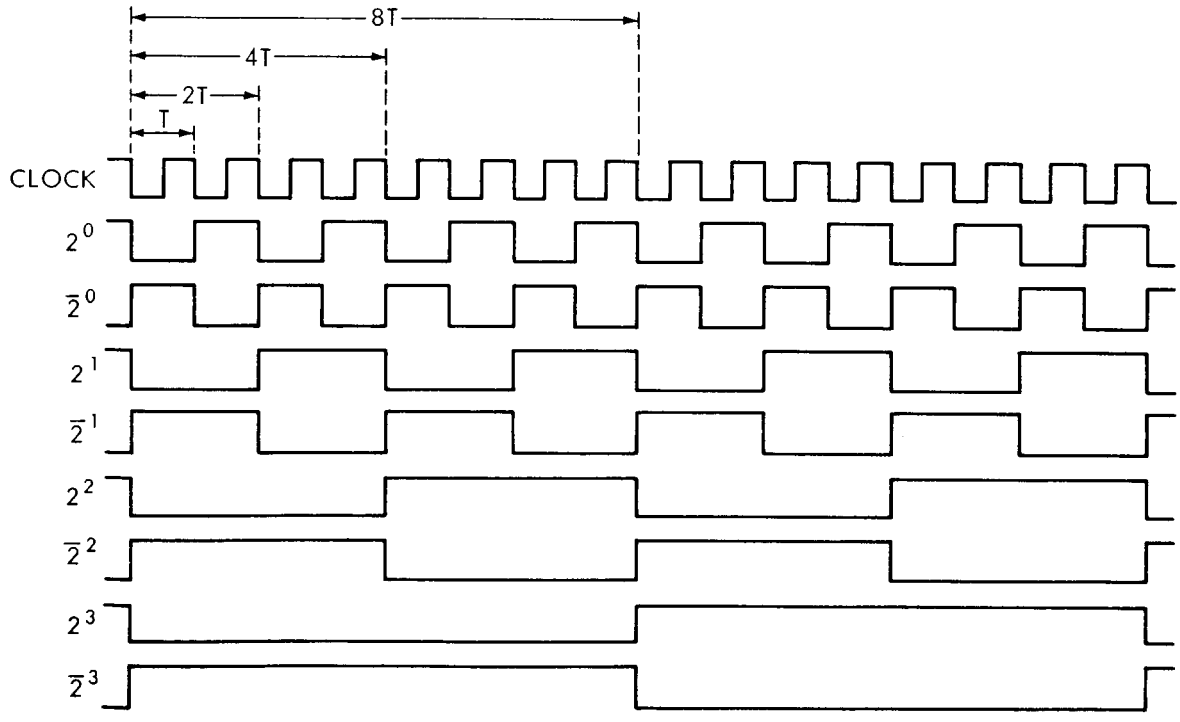


Figure 6. Channel Counter Waveforms

REFERENCE PULSE. The REFERENCE pulse is generated in the same way as the FRAME PULSE, except that the REFERENCE is initiated by the inverted CLOCK output.

DATA PULSE

When the DATA pulses are actually generated, the process is the same as for the generation of the FRAME and REFERENCE pulses. However, the time of appearance of each DATA pulse must be a linear function of the magnitude of the input data. This is accomplished in the Simulator by the use of gate transistors. Each of these is a PNP transistor, to the base of which is applied the simulated input data, and to whose emitter is applied a SAWTOOTH voltage (Figure 7). Thus when the emitter voltage becomes equal to the base voltage, conduction occurs, and the DATA pulse is initiated. However, since there are three possible sources of input data, EVEN CHAN, ODD CHAN, and VARIABLE CHANNEL, there must be three gate transistors. (There is also a fourth gate transistor, whose purpose will be explained later.) The SAWTOOTH pulse is applied to one input of an AND GATE on each emitter. Buffered outputs from the 2^0 stage of the CHANNEL COUNTER alternately enable and inhibit the GATE-EVEN and GATE-ODD circuits. When the 2^0 output on the GATE-EVEN is +10 volts, the SAWTOOTH pulse is allowed to appear on the emitter. At the same time that the opposite, or 2^0 complement output on the GATE-ODD circuit is -3 volts, and the SAWTOOTH PULSE is inhibited from the output of the AND GATE, which is connected to the emitter of the GATE-ODD transistor. During the next channel time these conditions are reversed. Each of these two AND GATES has another input, connected to the GATE-VARIABLE logic. These inputs are held at +10 volts at all times, except during the time corresponding to the channel selected by the VARIABLE CHANNEL switch. During that time they are at -3 volts, to inhibit both the GATE-EVEN and the GATE-ODD circuits.

The GATE-VARIABLE is enabled by the same waveform that is used to inhibit the other two gates, except that the inhibit voltage is the inverted enable voltage. This voltage is generated by gating four of the eight outputs of the channel counter. The eight outputs are connected to a rotary switch in such a pattern that, when the switch is set to a number, the switched outputs will all be low during the channel of that number, and the output of the NAND GATE to which they are connected will be high.

For proper operation of the Simulator, a DATA pulse must be produced during each channel. To guard it against the consequences of a connection to an external voltage too high for normal operation, a fourth gate, called the GATE-LIMIT, is provided. The SAWTOOTH pulse (Figure 7) is applied to the GATE-LIMIT transistor emitter through a diode, as is done at the other gates. The base of the transistor is connected to a 5.2-volt source, which produces a DATA

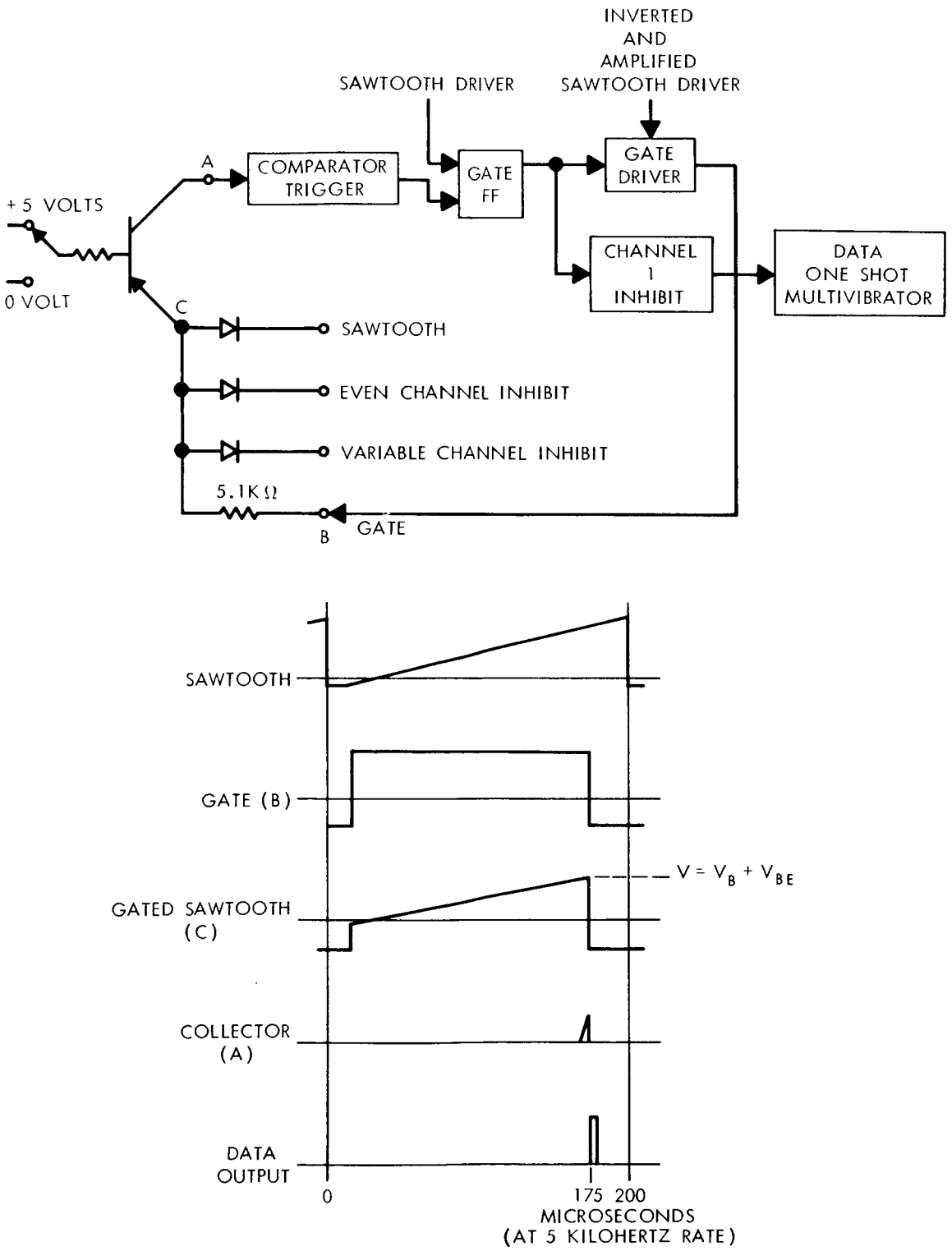


Figure 7. GATE-ODD Operation

pulse at 181 microseconds, if a pulse has not already been initiated by one of the other gates.

The SAWTOOTH pulse is initiated by the trailing edge of the SAWTOOTH DRIVER pulse, which is driven by the CLOCK. The SAWTOOTH DRIVER pulse is, among other things, a delay pulse, so its duration is changed by switching the components that determine pulse length whenever the CLOCK rate is changed. (It is 15 microseconds in length at 5-kilohertz, 7.5, at 10 kilohertz, and 3.75 at 20 kilohertz). In the SAWTOOTH GENERATOR, a different set of adjustable components are switched into the circuit when the CLOCK rate is changed, and the level and slope of the sawtooth pulse is adjusted for each rate. This is done in order that the SAWTOOTH pulse will reach a given voltage at the right instant, and therefore, that the timing of the DATA pulse will be a linear function of the data input voltage.

The leading edge of the (inverted) SAWTOOTH DRIVER pulse sets the GATE flip-flop. It is reset by a pulse from the COMPARATOR TRIGGER circuit. The collectors of the four GATE transistors are connected to the COMPARATOR TRIGGER circuit. Whenever one of the GATE transistors begins to conduct, the COMPARATOR TRIGGER pulse is generated. The output of the GATE flip-flop is inverted and amplified in the GATE DRIVER circuit, also, the leading end of it is gated out by means of an inverted and amplified SAWTOOTH DRIVER pulse. It is then applied to the emitters of the four GATE transistors, becoming the power supply voltage for the emitters and the AND circuits during the time that it is high (+10 volts). It may be noted that the GATE flip-flop is reset as soon as a GATE transistor begins to conduct, and the +10 volts will then be removed from the AND circuits and emitters. Therefore, the GATE transistors will remain in conduction for a very short time, thus drawing negligible current from the precision calibration voltage sources.

The level shift of the GATE flip-flop at this reset time is used to fire a four-microsecond one-shot multivibrator, to generate the DATA pulse. This pulse is then amplified to become the DATA output.

TRIPLE PULSE

In addition to a DATA pulse for each channel, the FORMAT output must contain a TRIPLE PULSE (3P). The TRIPLE PULSE is generated by 2 one-shot multivibrators connected as a ring multivibrator with a three input gate inserted in the loop. When triggered by the 2^3 Channel counter stage, these one-shots fire three times, while a two-stage flip-flop counter is counting to three. At this time an output of the counter closes the gate. This TRIPLE PULSE appears at FRAME time when the simulator is operated at the 5-kilohertz CLOCK rate, but at the other two rates it occurs 25 microseconds

later, triggered by the delay flip-flop, when it is reset by an output from the 20-kilohertz CLOCK stage. The pulses are approximately four microseconds long, and occur approximately eight microseconds apart, leading edge to leading edge. The duration is therefore approximately 20 microseconds in any mode.

Because at the 10 and 20-kilohertz CLOCK rates, certain low values of data would cause a DATA pulse to be generated at a time that would interfere with the delayed TRIPLE PULSE, a circuit has been placed between the GATE flip-flop and the DATA one-shot multivibrator, and labeled CHANNEL 1 INHIBIT. This circuit inhibits the DATA pulse in CHANNEL 1 until approximately one microsecond after the TRIPLE PULSE.

FORMAT PULSE TRAIN

The TRIPLE PULSE and the DATA pulse for each channel are combined, put through a driver, and emerge as the FORMAT output. The FORMAT for each frame consisting of the TRIPLE PULSE, and one DATA pulse for each of 16 channels, has a total of 19 pulses.

DETAILED CIRCUIT DESCRIPTION

This section of the report described each card assembly of the SST Telemetry Simulator. The diagrams found in the Appendix apply equally to all four of the cards, and should be used as reference material for this section.

CARD ONE

(Refer to Figures 7, 8, and Appendix Figures A-1 through A-4.) CARD 1 contains circuitry as described below.

CLOCK. The CLOCK consists of a 40 kilohertz Clapp, or series-tuned Colpitts, oscillator (transistor Q1 and associated circuitry), driving a one-shot multivibrator (Integrated Circuit (IC) number 1) which, in turn, drives a three-stage counter (or divider), composed of three flip-flops, (Integrated Circuits 2, 3, and 4). The three stages of the counter give square-wave outputs of 20, 10, and 5 kilohertz, respectively.

RELAYS. Card 1 also contains two relays. One of these, when energized, selects the output of the 20-kilohertz stage as the CLOCK output; the other selects the 10-kilohertz stage output. If neither relay is energized, the output is connected to the 5-kilohertz stage. In any case, the selected output becomes the CLOCK rate, or CLOCK frequency.

CHANNEL COUNTER. The CLOCK drives a four-stage counter, composed of Integrated Circuits 5, 6, 7, and 8, similar to the CLOCK counter. Eight

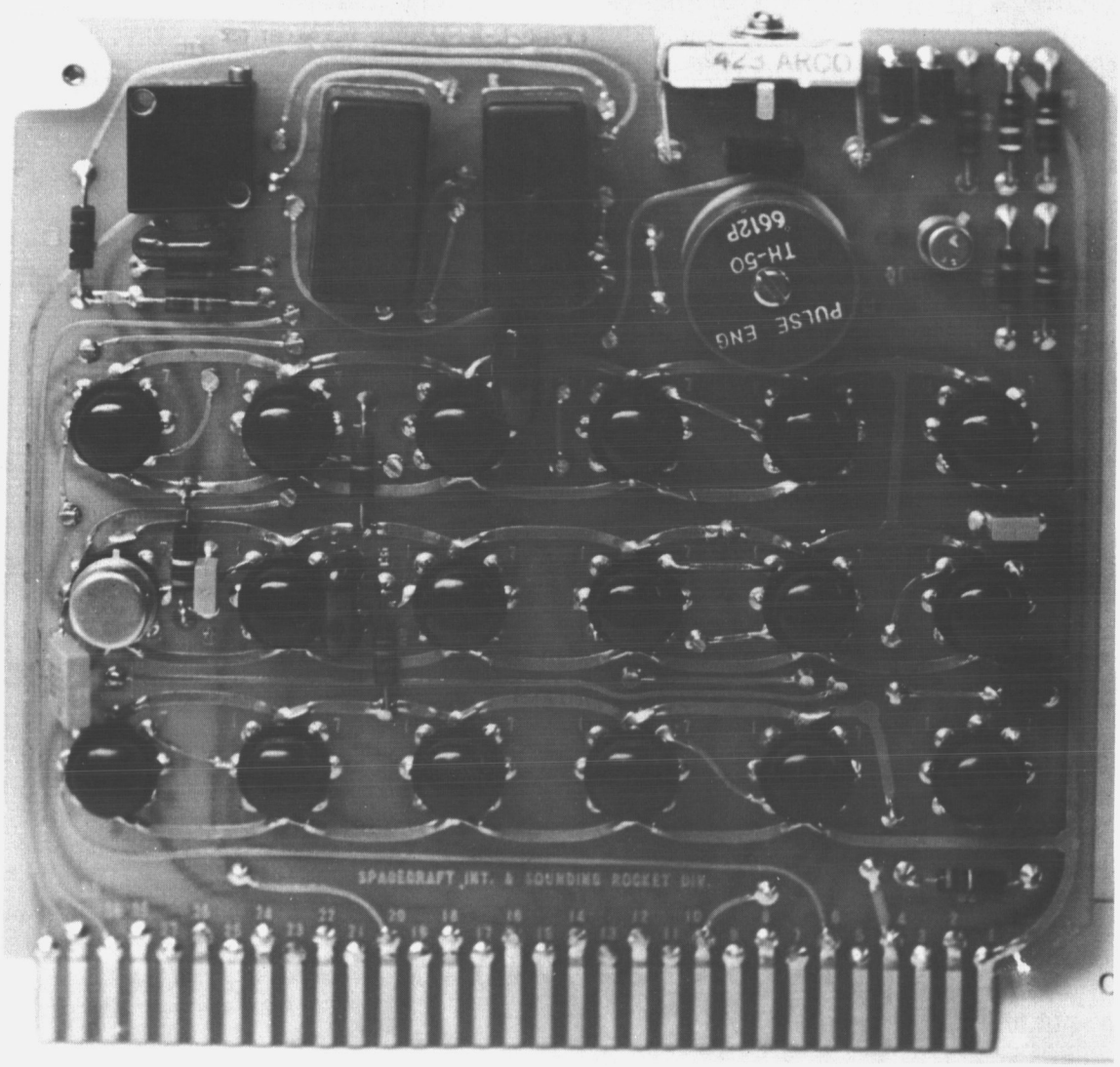


Figure 8. Card 1 Assembly

outputs are used, and each output is designated by the binary weight of the digit from which the output is taken, as: 2^0, 2^1, 2^2, and 2^3, and their complements.

SAWTOOTH DRIVER. The CLOCK pulse is inverted by Integrated Circuit (IC) 17, and used to trigger one-shot multivibrator IC18. The output of this circuit is a 3-volt negative pulse, referenced to zero. It is 15 microseconds in duration at the 5-megahertz CLOCK rate, 7.5 microseconds, at 10 megahertz and 3.75 microseconds, at the 20-megahertz rate. In common with some other circuits in the simulator, the one-shot multivibrator is connected between the d-c voltage levels of zero and -3 volts, necessitating the use of a-c coupling between inverter, IC17, and the one-shot multivibrator, IC18.

TRIPLE PULSE GENERATOR. The TRIPLE PULSE GENERATOR (Figures 9 and A-4) consists first of two one-shot multivibrators, connected as a ring multivibrator which can continue to trigger itself and produce pulses indefinitely. However, connected in the loop is a NAND (AND NOT) Gate, one of the inputs of which is the output of the second one-shot multivibrator. A second input is connected to the 2^3 output of the channel counter (when operating at the five-kilohertz CLOCK rate). The third input is the output of the NAND gate half of Integrated Circuit 16 whose inputs are the outputs of the zero sides of the TRIPLE PULSE counter flip-flops (Integrated Circuits 14 and 15). These inputs are designated $\overline{2}^0$ and $\overline{2}^1$.

At Channel 9 time (Figure 6), 2^3 of the channel connector becomes high. Connected to the PRESET lines of both TRIPLE PULSE counter stages, it sets $\overline{2}^0$ and $\overline{2}^1$ to high. The output of the NAND gate Integrated Circuit 16 is then low. At CHANNEL 1 time (Figure 6), when 2^3 from the channel counter becomes low, it triggers the one-shot multivibrator chain, which then triggers itself and produces pulses at a 125-kilohertz rate. However, the TRIPLE PULSE counter is counting these pulses, and at the count of 3 (binary 11), $\overline{2}^0$ and $\overline{2}^1$ are both negative and the output of the NAND gate (IC16) is positive. Since this is one of the inputs to gate IC11, further triggering of the TRIPLE PULSE generator is inhibited.

TRIPLE PULSE DELAY. When the Simulator is set for operation at the 10 or 20-kilohertz CLOCK rate, the 2^3 Channel counter output is not connected to gate IC11, Terminal 1, nor to the Preset terminals of the two TRIPLE PULSE counter flip-flops. Instead, side 1 of the delay flip-flop (IC 10), inverted in inverter IC 16, appears at these points. At CHANNEL 9 time, when 2^3 becomes high it sets and holds the delay flip-flop so that side 1 is low, and the high output at terminal 7 of inverter IC 10 appears on terminal 1 of gate IC 11, and at the preset lines of the two TRIPLE PULSE

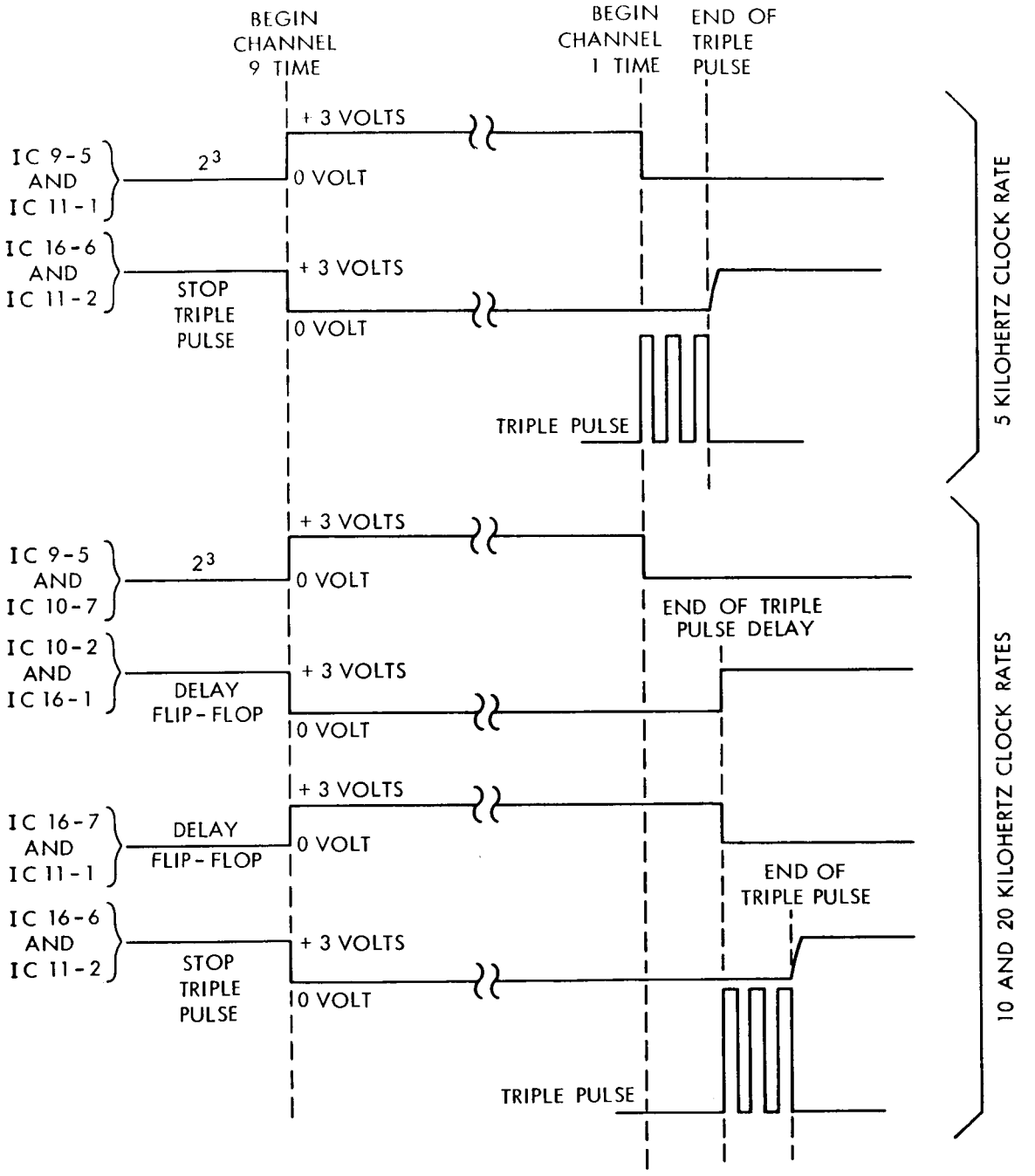


Figure 9. TRIPLE PULSE Gating Waveforms, Card 1

counter flip-flops. These flip-flops place a low on terminal 2 of gate IC11. The delay flip-flop is held in this condition by the high 2^3 level on terminal 6. At FRAME or Channel 1 time, 2^3 becomes low. Twenty-five microseconds later, a $\overline{20 \text{ kilohertz CLOCK}}$ pulse on terminal 2 triggers the flip-flop to its other state, IC terminal 1 of gate 11 goes low, triggering the TRIPLE PULSE generator. The counting and terminating of the TRIPLE-PULSE train is accomplished in the same way as is done when operating at the 5-kilohertz CLOCK rate. The output of terminal 6 of gate IC16, which stops the TRIPLE PULSE at the count of three, also appears on card terminal 26. Designated STOP TRIPLE PULSE, it becomes one of the components of the CHANNEL 1 INHIBIT pulse. The .01-microfarad capacitor connected across this output sufficiently increases the rise time of the STOP TRIPLE PULSE that the end of CHANNEL 1 INHIBIT occurs approximately one microsecond after the end of the TRIPLE PULSE.

CARD TWO

In addition to the figures listed as applying to all the cards, Figures 7 and 10, and Appendix Figures A-1 through A-3, and A-5 should be used as reference material in connection with the description of Card 2. The circuitry contained on this Card is as described below.

SAWTOOTH PULSE GENERATOR. The SAWTOOTH pulse generator may be divided, for circuit analysis, into three sections:

(1) The first consists of three sets of adjustable resistor-capacitor (RC) networks. Only one of these sets is used at any one time. For example, resistors R_4, R_g, and capacitors C3 and C7, are used for the 5-kilohertz clock rate. Through their use, the linearly rising voltage waveform is generated.

(2) The second section is a discharge circuit, composed of transistors Q1 and Q2. The SAWTOOTH DRIVER pulse is amplified and used to drive transistor Q2 into saturation, providing a low resistance discharge path for the capacitors, and delaying the beginning of the next SAWTOOTH pulse until the proper time. The emitter of transistor Q2 is returned to one of three switchable voltage dividers, so that the depth of discharge can be set for each CLOCK rate. This is the adjustment that sets the timing of the data pulse corresponding to the 0 volt. A byproduct of this circuit is an augmented $\overline{\text{SAWTOOTH DRIVER}}$ pulse.

(3) The third section is an amplifier circuit, composed of transistors Q3 through Q6, which provides power amplification and linearization of the SAWTOOTH pulse.

GATES. The four gate transistors and their associated circuitry are considered together. These are: GATE-ODD, which is transistor Q8; GATE-EVEN, which

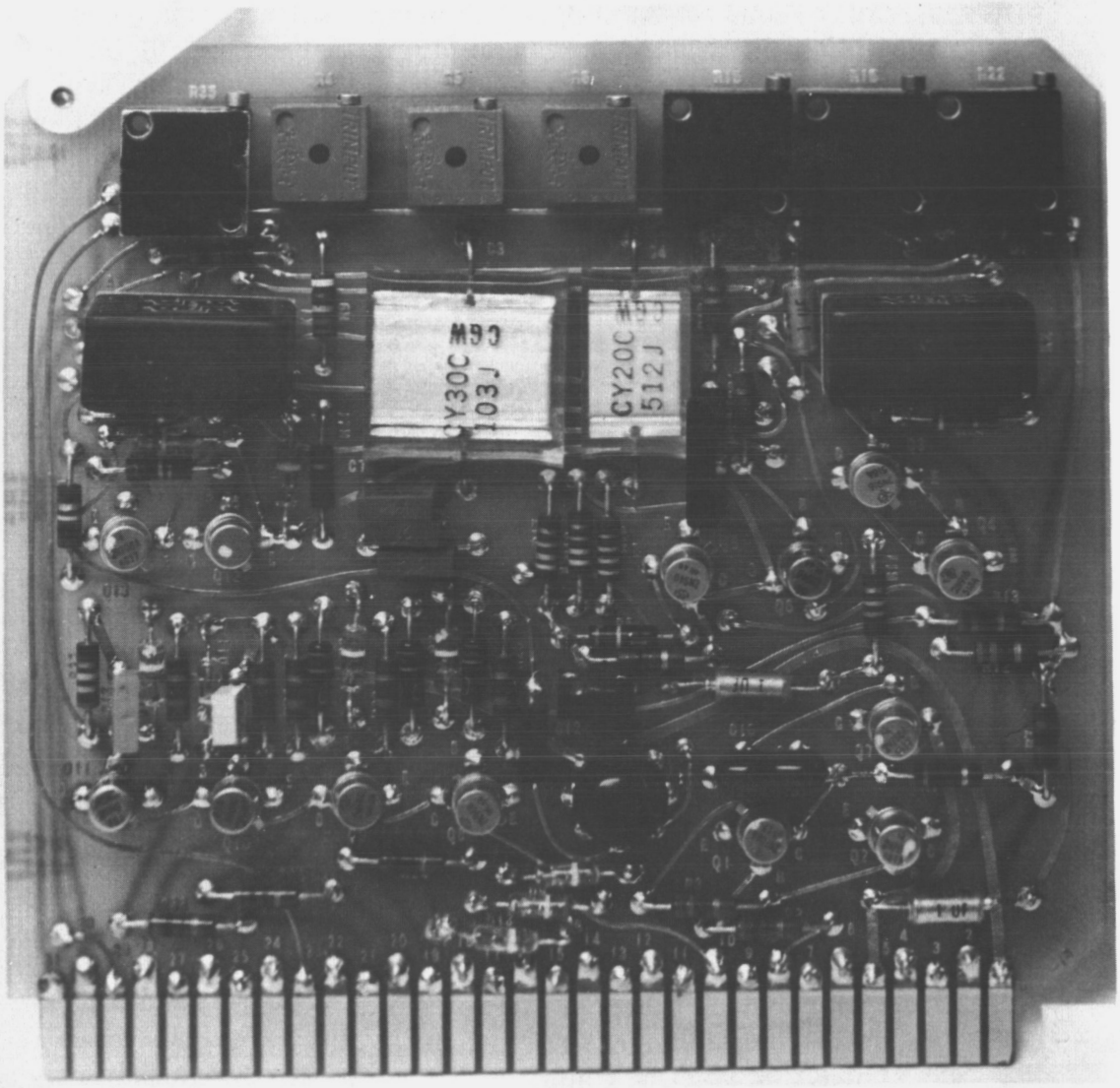


Figure 10. Card 2 Assembly

is transistor Q9; GATE-VARIABLE, which is transistor Q10; and GATE-LIMIT, which is transistor Q11.

All the gates have the same type of PNP transistor. Their collectors are connected at a common point. Each base is connected to a source of simulated data consisting of a voltage of 0 to 5 volts. Connected to each emitter is a diode AND circuit, which is composed of a number of diodes and a load resistor. (See Figure 7.) The load resistor is connected to a positive voltage supply, which is the amplified $\overline{\text{GATE}}$ flip-flop output. Connected to one diode input on each gate is the SAWTOOTH pulse. The GATE-LIMIT circuit has only the SAWTOOTH input. Connected to the other diode inputs are the inhibiting voltages. The operation of these circuits is described under PRINCIPLES OF OPERATION.

The base voltage on transistor Q11, the GATE-LIMIT transistor, is adjustable and should be set at 5.2 volts. It is taken from the junction of potentiometers R35 and R36, which are connected between +10 volts and ground.

EVEN-INHIBIT AND ODD-INHIBIT. The two inputs of the 2^0 stage of the Channel Counter, on Card 1, are buffered through Inverter IC 1, driven to greater levels by transistors Q12 and Q13, and applied to the AND circuits of GATE-ODD, and GATE-EVEN. These augmented waveforms are called EVEN-INHIBIT and ODD-INHIBIT, respectively.

CARD THREE

Figures 10, 11, 12, and Appendix Figures A-1, A-2, A-3, A-5, and A-6 should be used for reference in connection with the description of Card 3. The circuitry contained on this card is as described below.

GATE FLIP-FLOP. Integrated Circuit IC 3 is connected as a flip-flop. It is set with terminal 7 low, or at -3 volts, by the leading edge of the 3-volt amplitude inverted SAWTOOTH DRIVER pulse at the time of the beginning of each channel, and reset by the Comparator Trigger Circuit whenever a GATE transistor begins to conduct.

GATE PULSE DRIVER. The GATE pulse driver, consisting of transistors Q4 through Q7 contains a NAND gate with transistors Q4 and Q5, which inverts and amplifies the GATE pulse. Also, the amplified and inverted SAWTOOTH DRIVER pulse on the second input of the NAND gate is used to gate-out the leading portion of the GATE pulse. The complementary pair of transistors, Q6 and Q7, provides the required power gain, so that this circuit is able to supply power to the GATE transistors and their associated AND circuits.

COMPARATOR TRIGGER. The common lead from the collectors of all the GATE transistors (Figure A-5) is connected to transistor Q1 on Card 3, and to

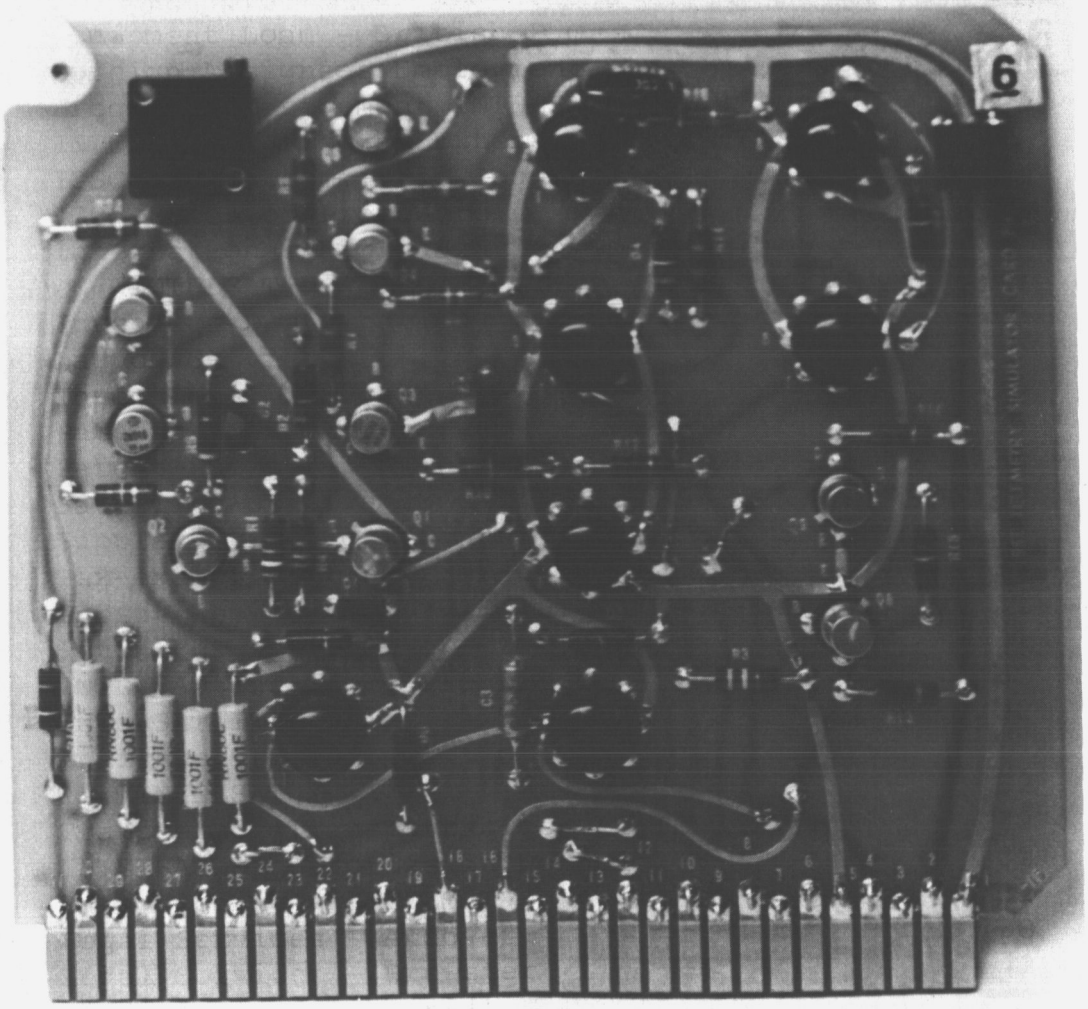


Figure 11. Card 3 Assembly

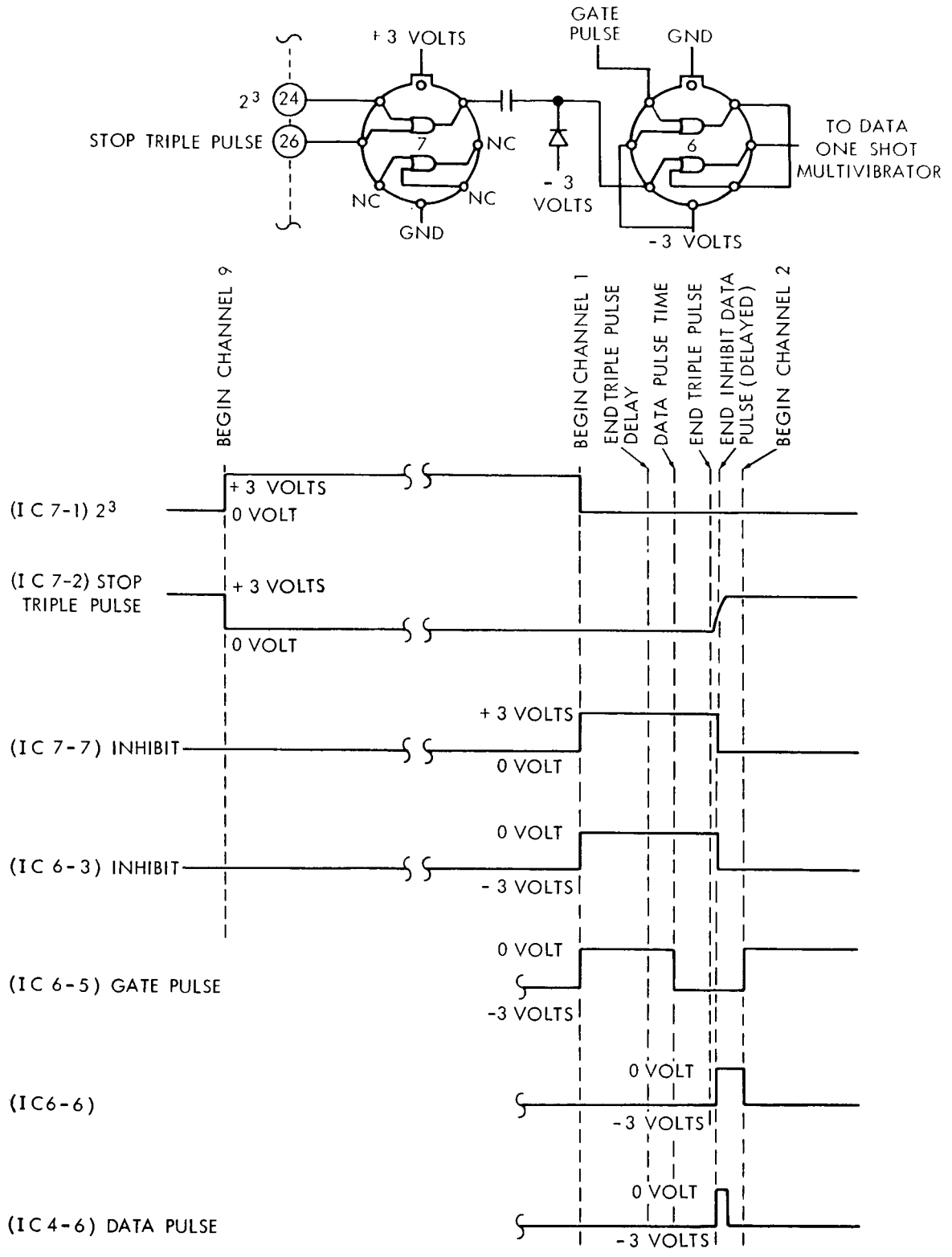


Figure 12. CHANNEL 1 INHIBIT, Card 3

-3 volts through a 240-kilohm load resistor. Transistors Q1 through Q3 form the Comparator Trigger circuit. When one of the GATE transistors begins to conduct, the circuit generates a pulse which resets the GATE flip-flop, removing the power from the GATE transistor emitters. The trigger circuit is regenerative, and power is removed from the GATE transistors before sufficient base current flows to produce any appreciable effect on the calibration voltage sources, which are extremely current-sensitive.

DATA ONE-SHOT MULTIVIBRATOR. When the GATE glip-flop is reset, as a GATE transistor begins to conduct, the output voltage on terminal 7 of Integrated Circuit, IC 3 undergoes a positive transition. This transition triggers the DATA one-shot multivibrator, which produces a 4-microsecond DATA pulse.

CHANNEL ONE INHIBIT. (Refer to Figure 12.) CHANNEL 1 INHIBIT circuitry consists of Integrated Circuits IC 6 and 7. The two sections of Integrated Circuit IC 6 are connected in series. One section is used as an inverter by connecting one input to -3 volts. The inverted GATE pulse is connected to one input of the second section of Integrated Circuit IC 6. Connected to the other input of this section is the CHANNEL 1 INHIBIT output from Integrated Circuit IC 7. Figure 12 shows how CHANNEL 1 INHIBIT is formed from 2^3 and STOP TRIPLE PULSE. During Channel 1 activity, both of the inputs to the second section of Integrated Circuit IC 6 start out high, or at zero volts. Whichever input changes to -3 volts last is the one that causes the output to go from -3 volts to zero, and initiates the DATA pulse.

FORMAT COMPILER. DATA pulses and TRIPLE PULSES are combined in one section of Integrated Circuit IC 5, and reinverted in the other section to make up the FORMAT pulse train.

VARIABLE CHANNEL-SELECT GATE. The eight outputs of the Channel Counter are fed to the Variable Channel Select switch. Four of these outputs are switched to the Variable Channel Select gate, IC 1. When these outputs are all at 0-volt, the gate will give a +3 volt output. This pulse is inverted in Integrated Circuit IC 2 then buffered by transistor Q8 and becomes the VARIABLE CHANNEL ENABLE pulse, which enables the GATE-VARIABLE circuitry, and (when inverted again in the Q9 circuitry) it becomes the VARIABLE CHANNEL INHIBIT pulse, which inhibits GATE-ODD and GATE-EVEN circuitry.

CALIBRATE-VOLTAGE GENERATOR. The CALIBRATE-VOLTAGE generator uses resistor R24 and zener diode D6 to drop the +10-volt supply voltage to a stable 6.2 volts. A precision-resistor voltage-divider network is used to provide outputs of 1, 2, 3, 4, and 5 volts.

CARD FOUR

Figure 13 and Appendix Figures A-1 through A-3, and A-7 should be used for reference in connection with the description of Card 4. The following circuitry is contained on this card.

CHANNEL TWO GATE. The outputs of the Channel Counter, which will be in the low voltage state during CHANNEL 2 time, are connected to the CHANNEL 2 gate. The output of the gate is a +3-volt pulse during CHANNEL 2 time.

DELAYED FRAME PULSE GENERATOR AND DRIVER. The DELAYED FRAME pulse generator is Integrated Circuit IC 2, connected as a one-shot multivibrator. When triggered by the leading edge of the CHANNEL 2 pulse, it produces a 4-microsecond DELAYED FRAME pulse. The DELAYED FRAME driver, consisting of transistors Q1 through Q3, and associated circuitry, inverts and amplifies this pulse to a 10-volt negative pulse referenced to zero volt.

FRAME PULSE GENERATOR AND DRIVER. The generation of the FRAME pulse by FRAME generator IC 3, and amplification by driver transistors Q4 through Q6, occurs when the output of the zero side of the 2^3 stage of the Channel Counter becomes positive at the beginning of CHANNEL 1 time.

REFERENCE PULSE GENERATOR AND DRIVER. The REFERENCE pulse generator is the one-shot multivibrator, IC 4. The REFERENCE pulse driver consists of transistors Q4 through Q6, and the circuitry associated with them. The $\overline{\text{CLOCK}}$ signal (the inverted CLOCK output) initiates the pulses.

DATA PULSE DRIVER AND FORMAT PULSE TRAIN DRIVER. The DATA pulse driver is made up of transistors Q13 through Q15. Transistors Q10 through Q13 make up the FORMAT PULSE TRAIN driver. The two sections of Integrated Circuit IC 5 invert the two pulse trains, so that the final output will have the correct polarity.

ONE HALF OF CHANNEL 16 PULSE GENERATOR. This signal is generated by Integrated Circuit IC 6, and one-half of Integrated Circuit IC 7 operating as a NAND gate. The inputs to the NAND GATE are the Channel Counter complements plus the CLOCK output. The second half of Integrated Circuit IC 7 inverts the CLOCK output to form the $\overline{\text{CLOCK}}$ signal to the REFERENCE pulse generator.

CALIBRATION AND OPERATION

The operation of the front-panel controls was explained in the "Physical Description" section under the heading "Front Panel Controls and Connector." This section explains the selection of the different CLOCK rates, and specifies the calibration required by the Simulator.

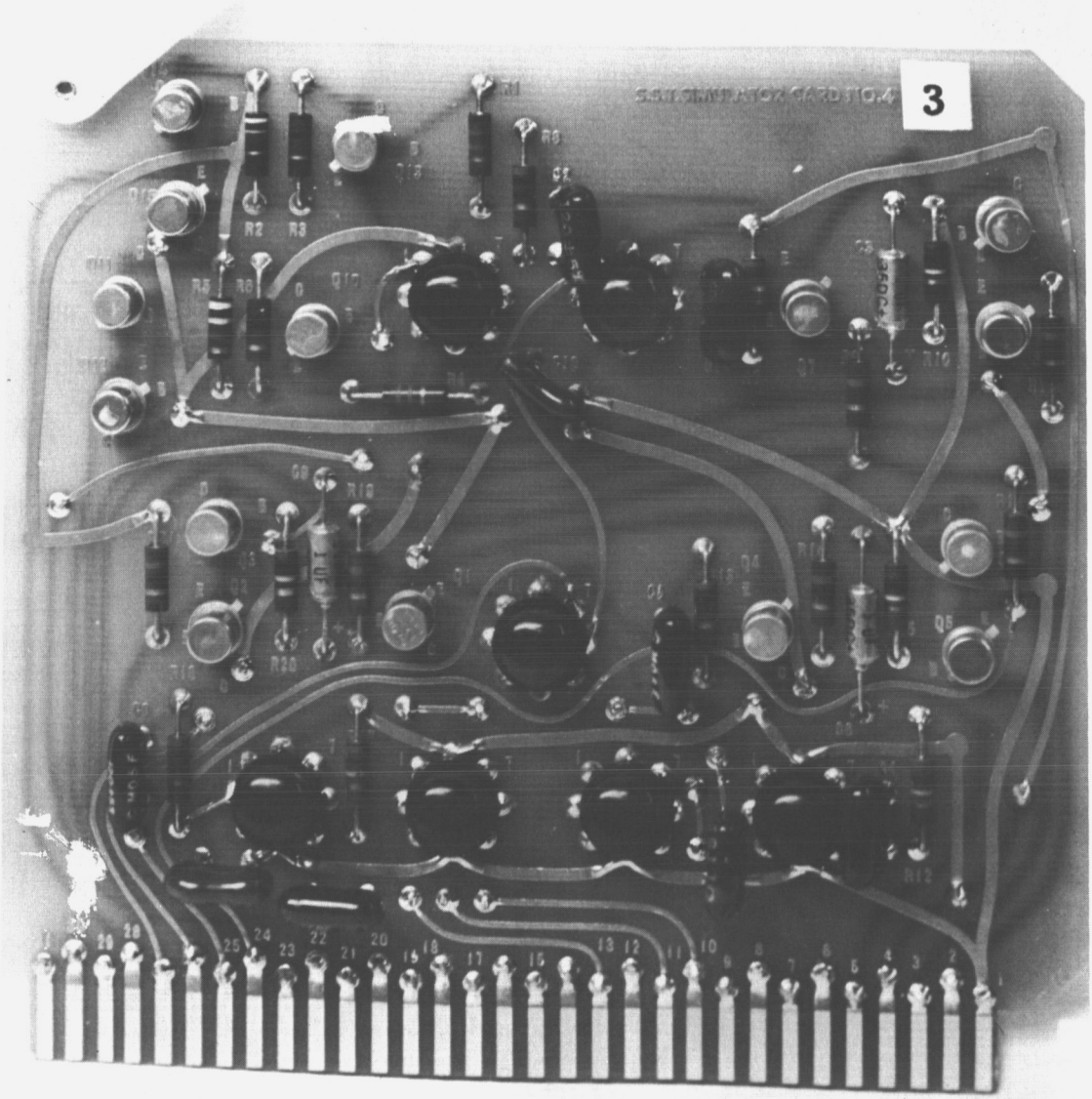


Figure 13. Card 4 Assembly

CALIBRATION AND OPERATION

CLOCK RATE SELECTION

To select the desired CLOCK-rate (frequency), apply voltage to pins of the 24-pin connector on the Simulator chassis.

A positive 10 volts, applied to Pin 14, enables operation at a 20-kilohertz CLOCK-rate.

A positive 10 volts, applied to Pin 13, enables operation at a 10-kilohertz CLOCK-rate.

When voltage is removed from both Pin 13 and from Pin 14, the operation procedes at a 5-kilohertz CLOCK-rate.

CLOCK ADJUSTMENT

The clock oscillator output is set to 40 kilohertz with the aid of a frequency counter. Connect the counter to pin 6 of single-shot multivibrator IC 1, and adjust capacitor C2.

DC VOLTAGE CALIBRATION

CALIBRATE VOLTAGE GENERATOR. The +5 volts on the Calibration voltage generator, on Card 3, is adjusted by means of the 1000 ohm potentiometer R17, using Pin 31 as a test point.

GATE-LIMIT VOLTAGE. The 5.2 volts on the base of the GATE-limit transistor Q11, on Card 2 should be set by adjusting the 15-kilohm potentiometer, R35.

TRIPLE PULSE FREQUENCY

The potentiometer, R10, on the second one-shot in the TRIPLE PULSE generator should be adjusted so that the pulses occur every 7.9 microseconds, from one leading edge to the next.

SAWTOOTH PULSE GENERATOR ADJUSTMENT

Use a dual-channel oscilloscope for the adjustment of the SAWTOOTH pulse generator.

Connect the external trigger and one oscilloscope channel to Pin 23 of Card 4.

Connect the other channel to Pin 28 of Card 4.

Set EVEN CHAN, ODD CHAN, and CALIBRATE VOLTAGE controls to zero volts. Set the Telemetry Calibrator for each of the three CLOCK rates, in turn, in accordance with the CLOCK RATE SELECTION paragraph. While set for each rate, adjust the appropriate 1000-ohm potentiometer, on the SAWTOOTH Pulse Generator on Card 2, so that the DATA pulse will follow the preceding REFERENCE pulse by the time shown in Table I.

TABLE I .

SAWTOOTH PULSE GENERATOR ADJUSTMENT AT 0 VOLTS

CLOCK RATE (kilohertz)	ADJUST	TIME (in microseconds) (Leading Edge to Leading Edge)
5	R22	25.0
10	R15	12.5
20	R16	6.25

Set EVEN CHAN, ODD CHAN, and CALIBRATE VOLTAGE controls to 5. Set the Telemetry Calibrator for each of the three CLOCK rates, in turn. Adjust the appropriate 25-kilohm potentiometer so that the DATA pulse will precede the following reference pulse by the times shown in Table II.

TABLE II.
SAWTOOTH PULSE GENERATOR ADJUSTMENT AT 5 VOLTS

CLOCK RATE (kilohertz)	ADJUST	TIME (in microseconds) (Leading Edge to Leading Edge)
5	R4	25.0
10	R5	12.5
20	R6	6.25

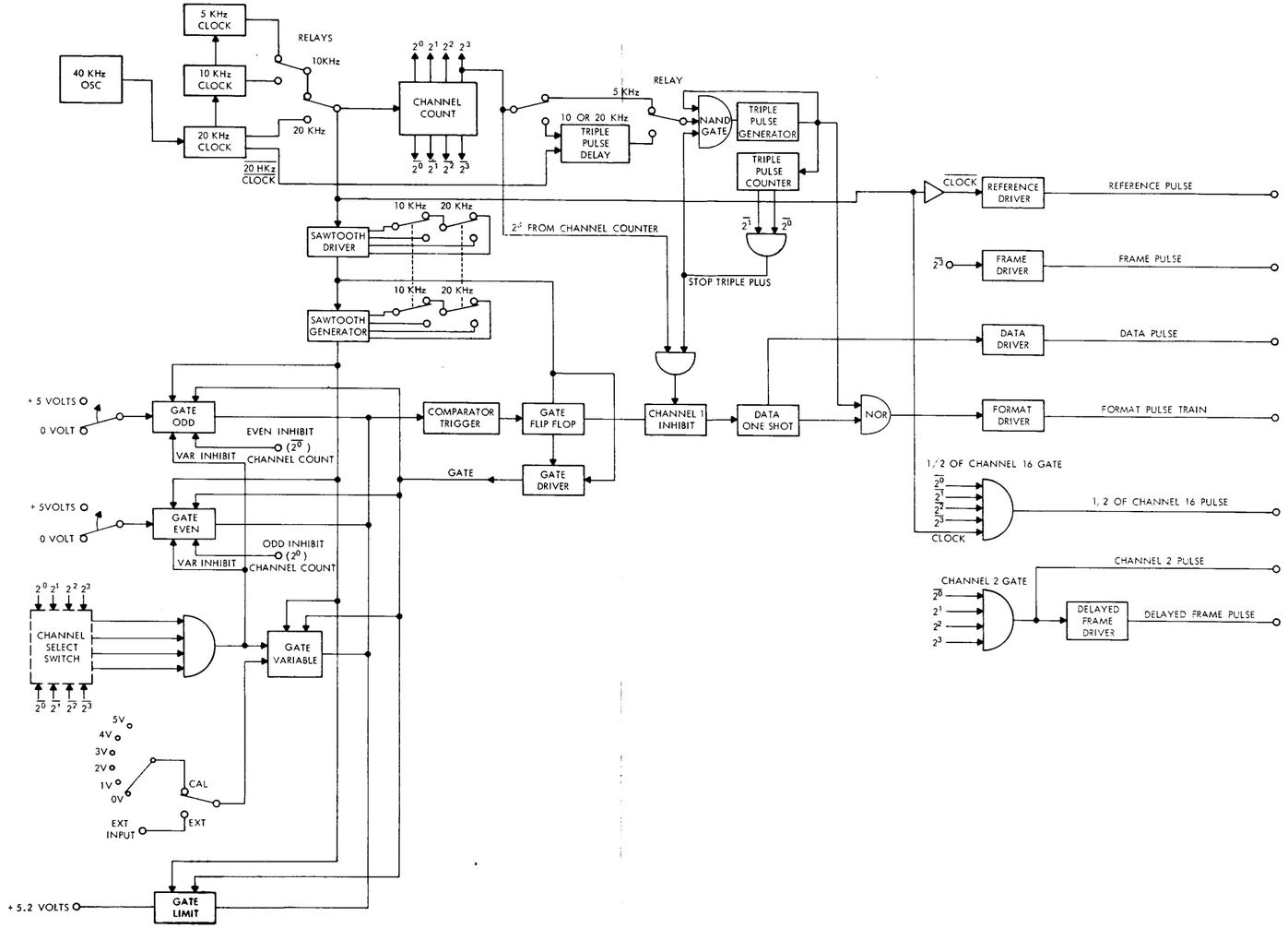
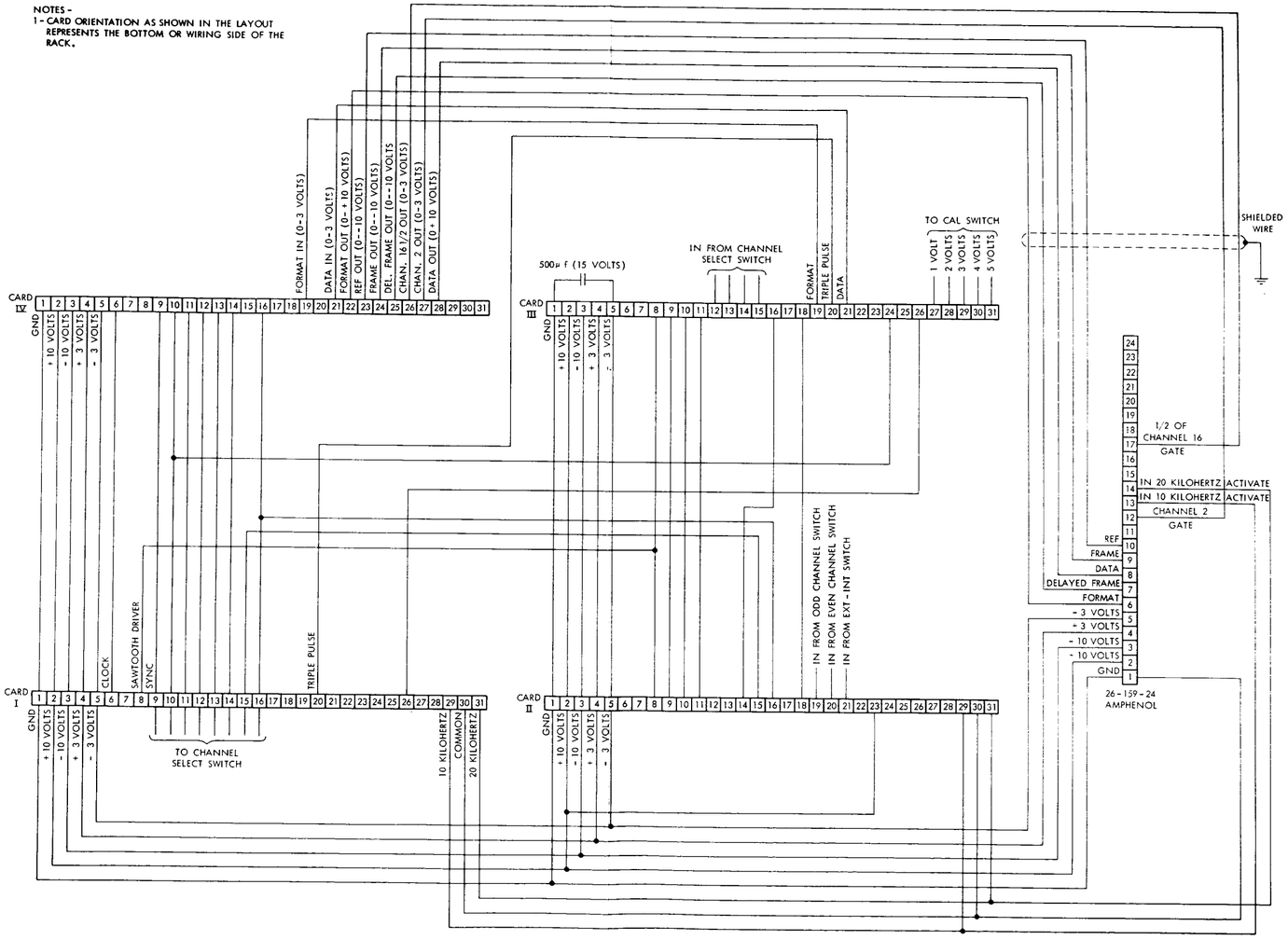


Figure A-1. Simulator Block Diagram

FOLDOUT FRAME 1

FOLDOUT FRAME 2



FOLDOUT FRAME 1

Figure A-2. Simulator Chasis Wiring Diagram

FOLDOUT FRAME 2

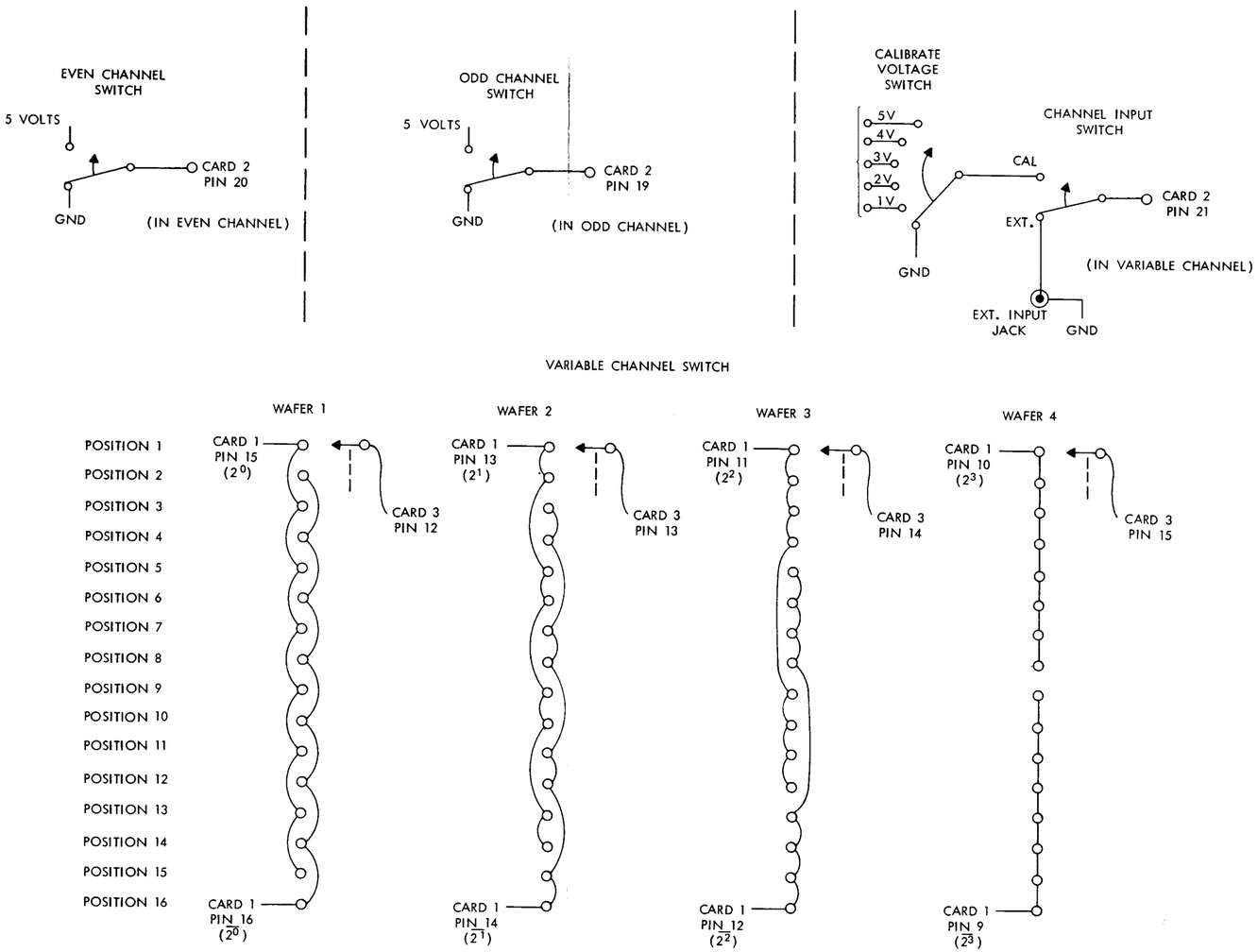


Figure A-3. Simulator Switches Wiring Diagram

FOLDOUT FRAME 1

A-4

A-5

FOLDOUT FRAME 2

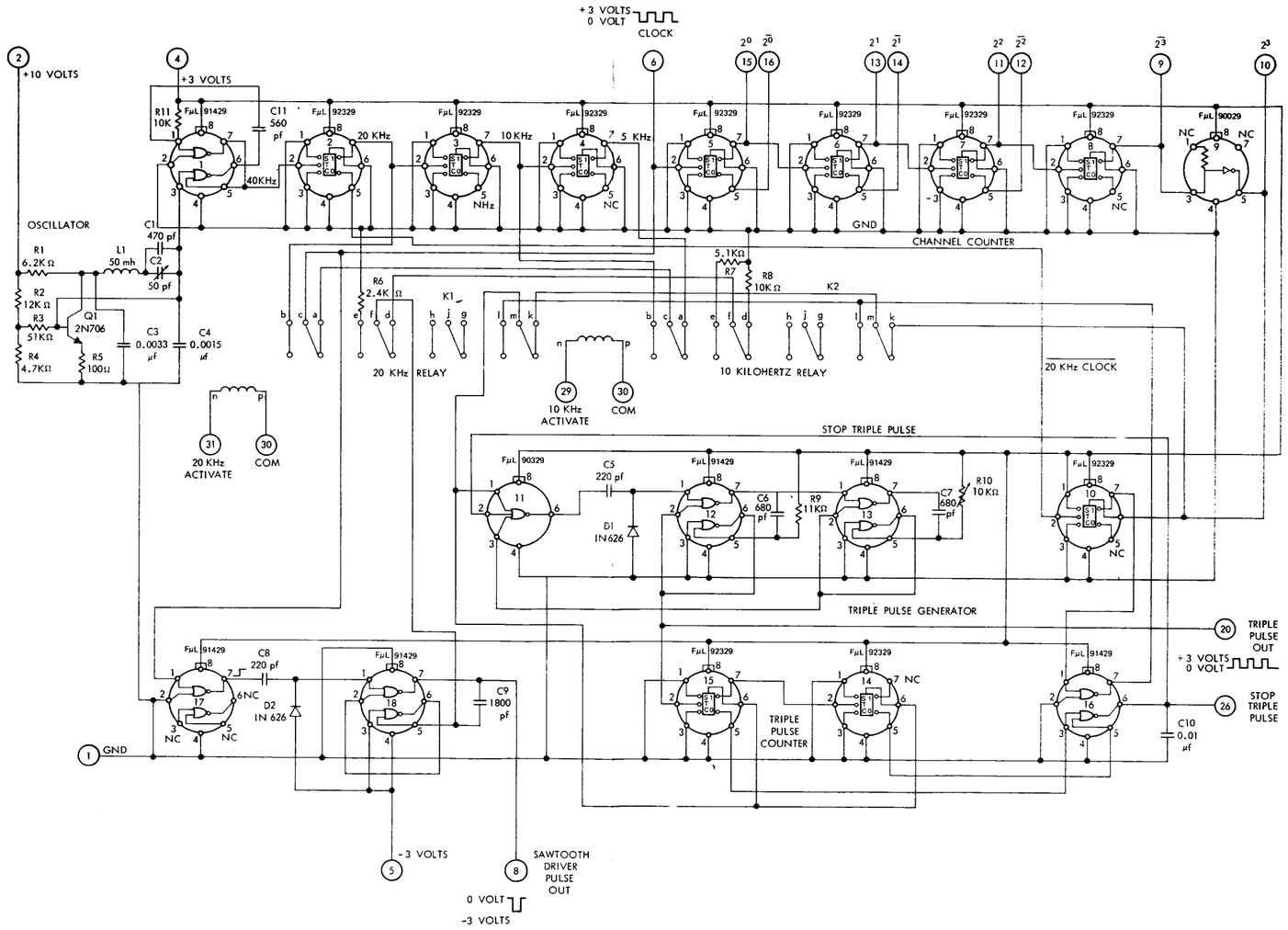
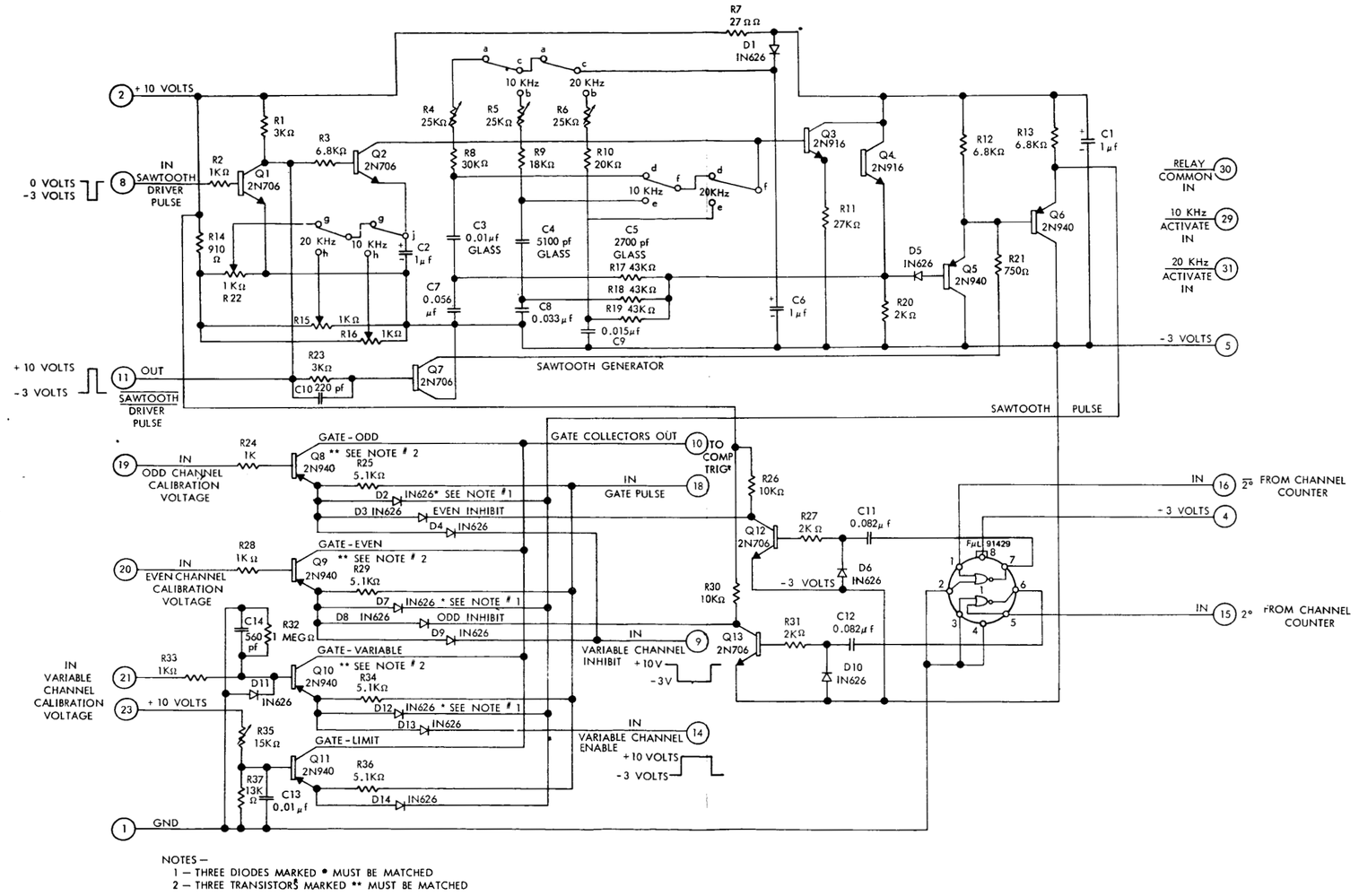


Figure A-4. Card 1, Schematic Diagram

FOLDOUT FRAME 1

FOLDOUT FRAME 2



NOTES —
1 — THREE DIODES MARKED * MUST BE MATCHED
2 — THREE TRANSISTORS MARKED ** MUST BE MATCHED

Figure A-5. Card 2, Schematic Diagram

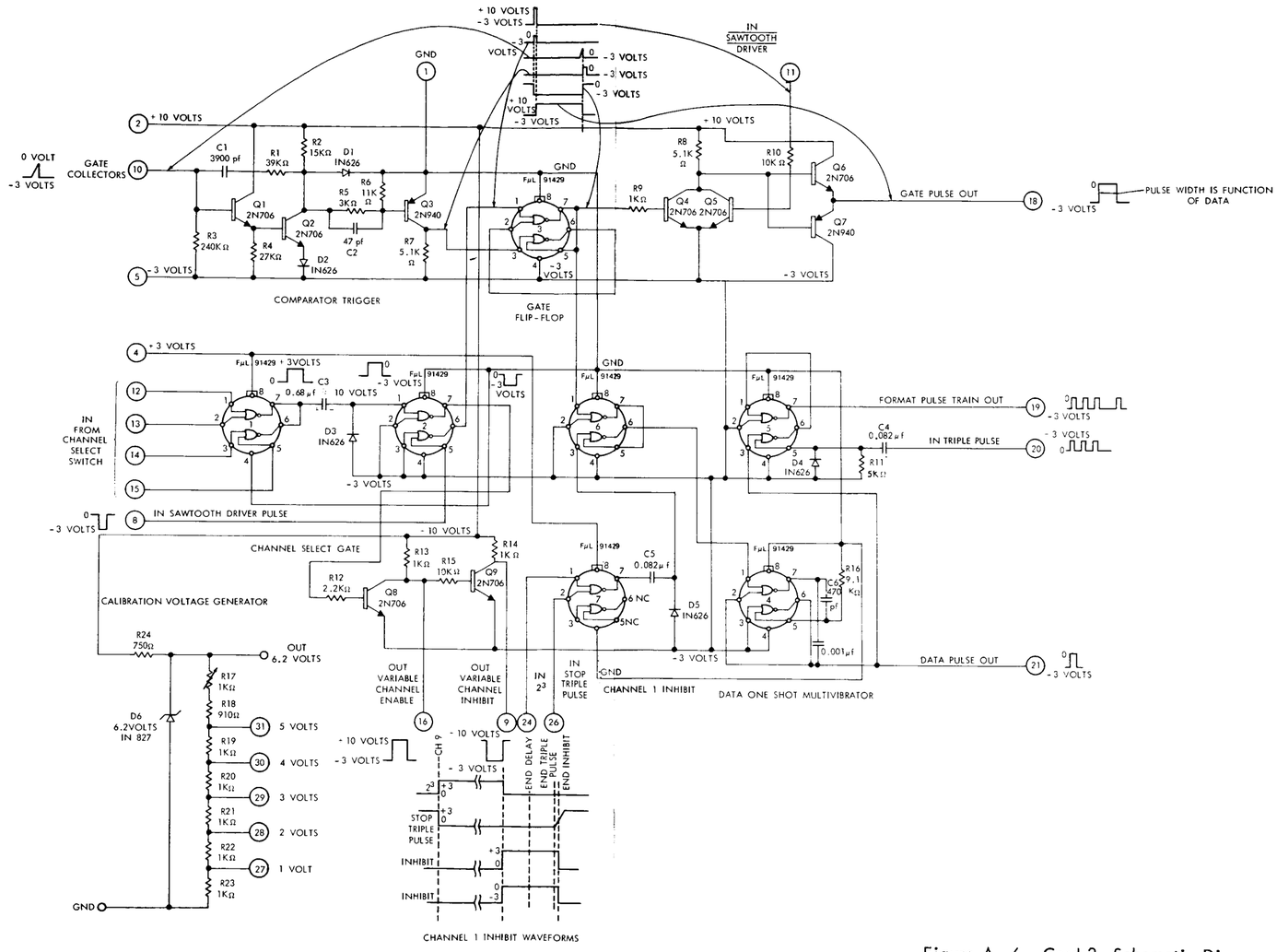


Figure A-6. Card 3, Schematic Diagram

FOLDOUT FRAME 1

FOLDOUT FRAME 2

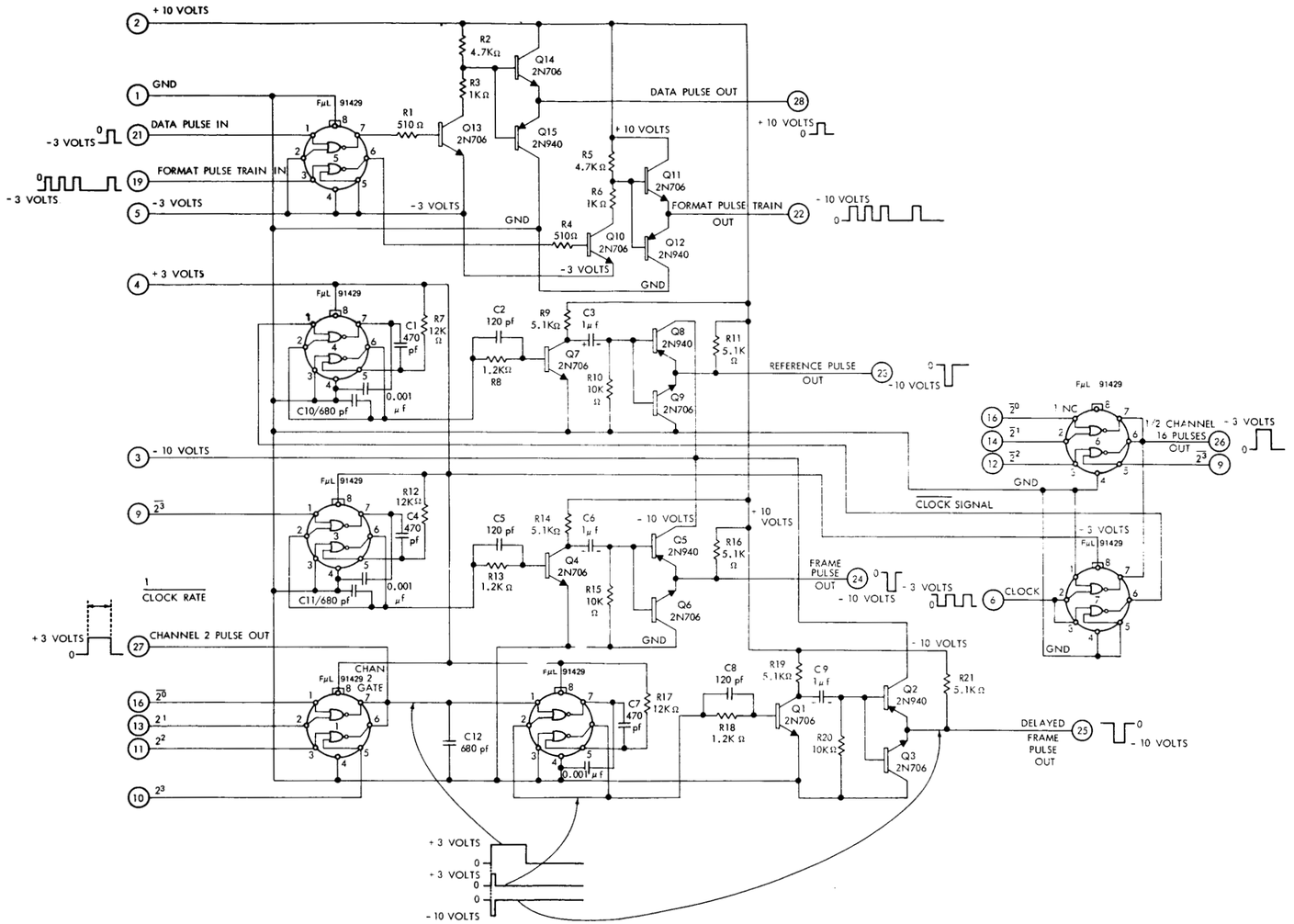


Figure A-7. Card 4, Schematic Diagram

FOLDOUT FRAME 1

FOLDOUT FRAME 2