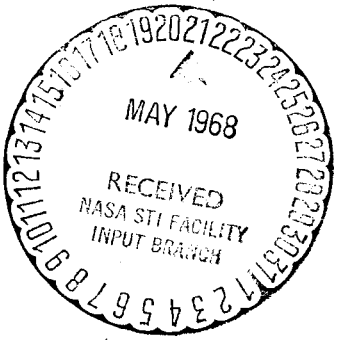
SEMIANNUAL STATUS REPORT

1 July through 31 December 1967

Research on

Field-Effect Transistor Stress Transducers

NASA Grant NGR 05-003-243
(Supplement No. 1)



ELECTRONICS RESEARCH LABORATORY

College of Engineering
University of California, Berkeley
94720

FOREWORD

The material contained in the following pages is intended to fulfill the requirement for the semiannual report (1 July through 31 December 1967) on National Aeronautics and Space Administration Grant NGR 05-003-243.

The project is entitled, "Research on Field-Effect Transistor Stress Transducers." The principal investigator is Professor R. S. Muller.

TABLE OF CONTENTS

FIELD-EFFECT STRESS TRANSDUCERS

(Professor R. S. Muller)

Present emphasis in research on field-effect transducers is on insulated-gate field-effect transistors (IGFET's) employing CdS or Te as the piezoelectric semiconductor material. The piezoelectric semiconductor stress-interaction theory has been confirmed by comparison of the polarity and magnitude of the stress-induced charge with observed changes in the drain current of IGFET devices. Present theoretical work is aimed at understanding the behavior of transducers of thickness equal to a Debye length, (appropriate to an exact theory for Te devices) and of classifying the performance to be expected from various alternative configurations. Fabrication techniques for single crystal CdS devices have been improved by high temperature surface doping of the polished CdS crystal using CdS : Cl powders. Additional work on CdS and Te IGFET devices is underway and work on junction gate devices is planned. Individual projects are described in the following.

SUMMARY OF RESULTS OBTAINED ON STRESS EFFECTS IN FET's

(J. Conragan)

The observation of a stress-dependent component of drain current in CdS IGFET's has led to the proposal and confirmation of the piezoelectric-stress interaction theory for FET's.[1] It has been shown that the major contribution to the stress dependent component of drain current

for these devices is due to the interaction between the channel charge and the stress-induced piezoelectric charge along the surfaces of the piezoelectric semiconductor.[2] This effect has been noted in IGFET's utilizing single crystal CdS and oriented thin-films of CdS, CdSe and Te in which the percentage change in drain current was typically 10 to 20 percent for an applied strain of 10^{-3}.[3]

The theory for these devices has been further corroborated by the direct observation of the piezoelectrically-induced charge on a stressed single-crystal of CdS. The polarity and order of magnitude of this charge were in agreement with the values indicated for these parameters on a transducer element constructed on the same mono-crystal.

MIPS transducer exhibit gauge factors which are comparable to those for silicon piezoresistive strain transducers. The deposited devices however have the advantage of smaller geometries and a wider range of substrate upon which the devices can be fabricated. As a practical example, a microphone has been constructed[4] utilizing a polyamide film of Kapton as the diaphragm upon which a CdS IGFET device had been deposited and used as the electro-mechanical transducer.

There are three basic configurations which can be used for these devices. These are the piezoelectric semiconductor, piezoelectric insulator and piezoelectric substrate configurations. The CdS IGFET is of the piezoelectric semiconductor type. This type will produce a

true dc response to an applied stress since the operation of this type of device depends upon neutralization of the stress induced charge, a process that takes place in the order of a dielectric relaxation time (in the order of 10 -100 ns for piezoelectric semiconductor used for IGFET's). On the other hand, the piezoelectric insulator and piezoelectric substrate configuration depend upon the induction of charge in the semiconductor by the piezoelectric charge. If the piezoelectric charge should be neutralized by internal mechanisms such as leakage, the effect upon the semiconductor will be lost. Thus these types do not produce a true dc response to an applied strain. However, they do have the advantage of greater potential sensitivity since the piezoelectric coefficients may be much higher than for the piezoelectric semiconductors. This is particularly true of piezoelectric substrate types since there exists a greater fabrication problem with the piezoelectric insulator devices, although ferroelectric insulator devices with a memory property

The effect of surface states must be taken into account when the performance of field-effect transistor strain transducers is being considered. The effect of the stress induced charge can be completely masked by surface states since the surface state density is typically several orders of magnitude greater than the stress-induced carrier concentration. This problem is readily overcome by the application of an appropriate gate bias for both the piezoelectric semiconductor and piezoelectric insulator

devices. However, this is not true for the piezoelectric substrate devices since the surface states of interest lie at the semiconductor-substrate boundary. Since this type of device shows great potential for applications, investigation is now under way to circumvent the surface state problem. Since the lowest surface state densities are still in the order of 10^{10} to 10^{11} states per square cm, a method of "biasing" these states rather than eliminating them is preferable. Two possible methods are to construct junction-gate FET's in which the drain depletion region extends throughout the semiconductor, thus biasing the surface states, or to construct IGFET's utilizing semiconductor films in which thickness is comparable to Debye length. This allows the gate-induced field to penetrate the semiconductor and to bias the surface states on the substrate side of the semiconductor. An analysis of the IGFET utilizing a thin semiconductor is presently under consideration in order to determine the effect of a stress induced charge in the substrate on device characteristics. IGFET's employing Te as the semiconductor do have a semiconductor thickness comparable to a Debye length and will be used in experimental studies of piezoelectric substrate FET transducers although the Te itself does possess piezoelectric properties. Such devices have been constructed on glass substrates while similar devices will be constructed on piezoelectric substrates in the future.

References

1. R. S. Muller and J. Conragan, Appl. Phys. Letters 6, 83 (1965).
2. R. S. Muller and J. Conragan, IEEE Trans. on Elect. Devices, ED-12, 590 (1965).
3. J. Conragan and R. S. Muller, Solid State Electronics 9, 183 (1966).
4. R. S. Muller, J. Conragan and J. R. Fiebiger, Proc. IEEE, 54, 337 (1966).

IMPROVED TECHNIQUES FOR METAL INSULATOR PIEZOELECTRIC-SEMICONDUCTOR TRANSDUCER FABRICATION

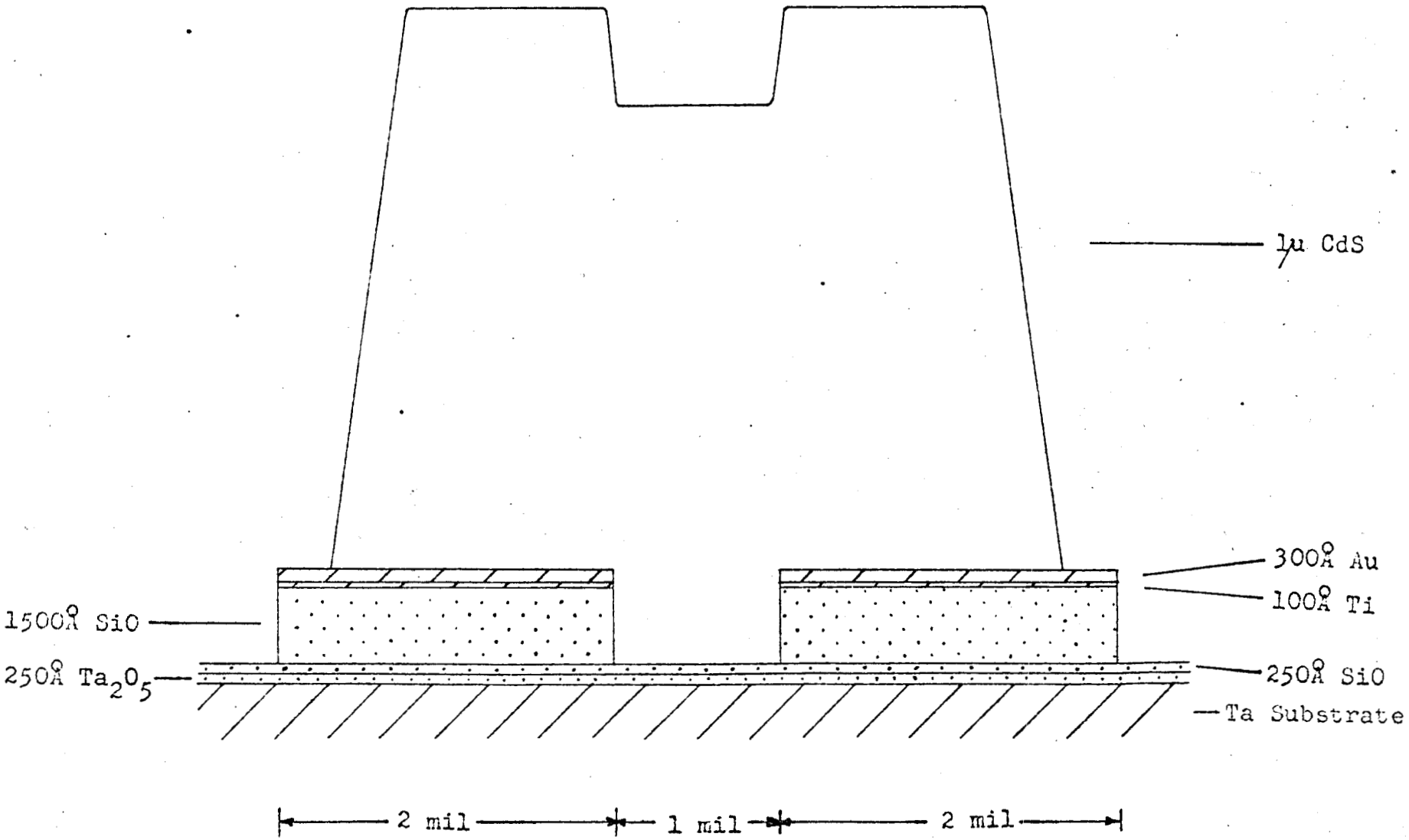
(R. D. Trout)

The purpose of this project is to develop MIPS stress transducers of higher sensitivity and frequency response by improved masking techniques. For high frequency response, the gate-drain and, to a lesser extent, gate-source capacitances must be minimized. For high sensitivity, the gate-channel insulator should be thin and of high permittivity. At the same time, the conductance of the active region of the semiconductor should be controlled solely by the gate potential. Thus far, MIPS transducers have been made by shadow mask techniques, and it has been found to be difficult to align several such masks to a tolerance much better than one mil. Therefore, there has been considerable overlap of the various structures of the MIPS devices. The addition of photo-resist techniques shows promise of considerably refining the tolerances, so that alignment of the source,

drain and channel can be assumed. Although neither the channel width nor the size of the source and drain contacts can be made arbitrarily small, they can be much smaller than could be accomplished by shadow-mask techniques. Another innovation is the use of a metal substrate which serves as the gate, while the rest of the device overlays it. This enables the transducer to be an integral part of the structure in which strain is being measured, and does away with the problems of providing a good mechanical coupling to the transducer. Such a fabrication technique is also compatible in some cases with the formation of the insulation layer by anodization. Insulating layers formed in this manner show promise of better stability and higher breakdown strength. A cross section of the device now being constructed is shown in the accompanying figure.

MINORITY-CARRIER MOBILITIES AT SEMICONDUCTOR SURFACES (J. Chen)

The theoretical calculation of surface carrier mobilities in terms of the semiconductor surface potential V_s was first carried out by Schrieffer[2] and later improved by Greene et al.[3] Schrieffer's calculations agree only qualitatively with experimental results.[4,5] Green's calculations do have fair quantitive agreement with experiment results when V_s is small. There are still many assumptions in Green's calculation which differ from reality. The difficulty in the experimental work is to find the excess carrier concentration at the surface more exactly.


1μ CdS
300Å Au
100Å Ti
1500Å SiO
250Å Ta_2O_5
250Å SiO
Ta Substrate
2 mil
1 mil
2 mil

Our work at present is concentrated on the use of a balanced-bridge circuit employing a phase-lock detector in order to measure currents very precisely at low gate biases. The purpose of this research is to discover to what extent present theory is adequate, and to improve understanding of free-carrier mobility at semiconductor-insulator surfaces.

Measurements have been carried out on experimental, large-area FET structures obtained from Fairchild semiconductors at surface potentials which are far lower than those resulting in inversion. At these levels, we have observed a drop in mobility which is not predicted by any theory, and which has not been reported thus far. It is suspected that surface trapping is responsible for the measurements.

References

1. N. Goldsmith and W. Kern, RCA Review, vol. 28, 153, March 1967.

2. J. R. Schrieffer, Physical Review, vol. 97, No. 3, February 1955.

3. R. F. Greene, et al., Physical Review, vol. 118, 1967.

4. O. Leistiko, Jr., et. al., IEEE Trans. on Electron Devices, May 1955.

5. J. Grosvalet, et. al., Surface Science, 5, 1966.

THIN FILM CdS-CdTe HETEROJUNCTION DIODES

(R. W. Dutton*)

Thin-film, Au-CdS-Te metal-semiconductor diodes, made by a vacuum, vapor-deposition process, have been shown to exhibit an excellent rectification ratio and a high reverse breakdown voltage. It is demonstrated that a layer of CdTe is formed at the CdS-Te interface in these diodes. The existence of the layer is confirmed using x-ray diffraction studies and selective chemical etches. The diode photocurrent shows a threshold photon energy that corresponds to the bandgap of CdTe. The presence of the CdTe layer can explain the favorable electrical properties of Au-CdS-Te diodes. The observed photoresponse, current vs. voltage and capacitance vs. voltage characteristics are shown to be consistent with those predicted by a semiconductor heterojunction model of the CdS-CdTe interface. An article describing this work is being submitted to "Solid-State Electronics." Research on these heterojunction diodes is prerequisite to attempts to build depletion-mode, barrier-junction transducers.

EVALUATION OF Au-CdS-Te BARRIER-JUNCTION FET's

(R. W. Dutton*)

Attempts were made to fabricate a CdS depletion-mode FET with a reverse-biased CdS-Te diode (see report above) used as the

---

* NSF Fellow.

gate. Although three sets of devices failed to exhibit the desired transistor action, information was obtained which will assist in further efforts to build this device. The difficulties encountered to date stem from the desire to realize two opposing goals simultaneously. From the work with CdS-Te diodes it was found that to form good diodes, the CdS resistivity has to be high. On the other hand, to achieve adequate drain-currents in the device, the CdS channel resistance must be low. Baking the devices in H_2S for short periods of time might act to increase the surface resistivity sufficiently to form better CdS-Te junctions with lower reverse leakage currents. By varying the CdS film thickness, it may be possible to optimize the two goals mentioned above.