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MISSILE AND SPACE DIVISION

MARS SPACECRAFT POWER

SYSTEM DEVELOPMENT

— INTERIM REPORT

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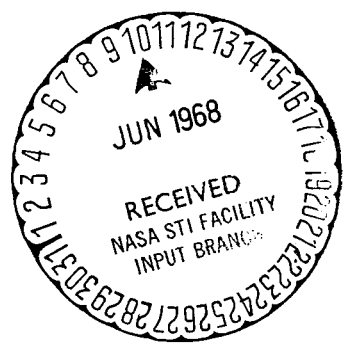
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25 APRIL 1968

MARS SPACECRAFT POWER

SYSTEM DEVELOPMENT

— INTERIM REPORT

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4800 OAK GROVE DRIVE
PASADENA, CALIFORNIA

UNDER JPL CONTRACT NO. 952150

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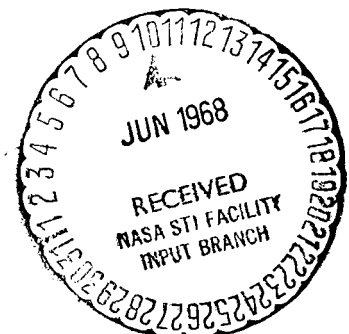P. O. Box 8555 • Philadelphia, Penna. 19101

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SECTION 1

INTRODUCTION

This is the midterm report of the Mars Spacecraft Power System Development Program conducted in accordance with JPL Contract No. 952150.

The aim of this program is to investigate and recommend possible changes in existing Mariner power system designs for use in future Mars flyby and orbiter missions. The Mariner Mars 1969 power system is used as the reference design against which all comparisons and recommendations will be made.

As evidenced by guidelines and information provided by JPL during the early phases of the program, the principal interest is centered on orbiter missions as exemplified by the 1971 opportunity. As a result, more emphasis is being placed on a design meeting orbiter requirements rather than flyby requirements. However, possible flyby improvements will be inclusive in the study of orbiter power systems, e.g., the application of fault sensing and redundancy. Thus, at the conclusion of the study, all of the necessary information will be available to identify potential flyby power system improvements as well.

A work plan for conducting the study was developed in the early weeks of the program and is shown on Figure 1-1. The cross-hatched areas indicate the degree of completion of the designated tasks. The principal results at this point in the study are summarized below:

- A shunt regulation system has been selected as the prime contender for more detailed study.

- Upon review of available test data it has been concluded that only silver-zinc and nickel-cadmium batteries will be considered in the upcoming study phase.

- Reliability sensitivity studies indicate that fault sensing and switchover devices should be considered only if their net reliability is equal to or greater than the reliability of the functions being protected (e.g. regulator or inverters). No clearcut reliability advantage has been identified for fault sensing the regulator and inverter separately or as a pair. The choice will lie more in which approach is easier to implement.

- Fault criteria have been identified for the principal types of power conditioning units (PCUs'). These criteria distinguish between PCU and source/load faults.

- A frequency optimization study indicates that a change from the presently used frequency of 2.4 kHz is not warranted.

- General guidelines and design practices in the area of power switching and distribution have been provided.

- Circuits of the MM '69 power system were reviewed, several potential problem areas identified, and alternate approaches suggested.

WORK FLOW DIAGRAM – MARS SPACECRAFT POWER SYSTEM DEVELOPMENT

(WEEKS FROM GO AHEAD)

| 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 |

APRIL 25

Milestone boxes:

- SYSTEM DESIGNS COMPLETE
- COMPLETE ANALYSIS
- CALCULATE RELIABILITY
- SENSITIVITY STUDY MM '69
- MODEL SHUNT SYSTEM
- SENSITIVITY STUDY – SHUNT SYSTEM
- FINAL REPORT PREPARATION
- FINAL SYSTEM SELECTION
- PREPARE DESCRIPTION

Task rows (left labels):
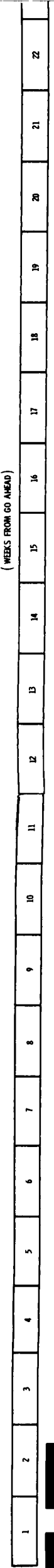
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- TASK 3.0 POWER SYSTEM DEFINITION AND DESIGN IMPLEMENTATION
- TASK 2.0 FAULT SENSING RELIABILITY
- TASK 4.0 SYSTEM LEVEL RELIABILITY ANALYSIS
- TASK 5.0 POWER SYSTEM SELECTION AND DETAILED DESCRIPTION
- TASK 6.0 AC DISTRIBUTION FREQUENCY STUDY
- TASK 7.0 POWER SWITCHING AND DISTRIBUTION
- MEETINGS AND REPORTS
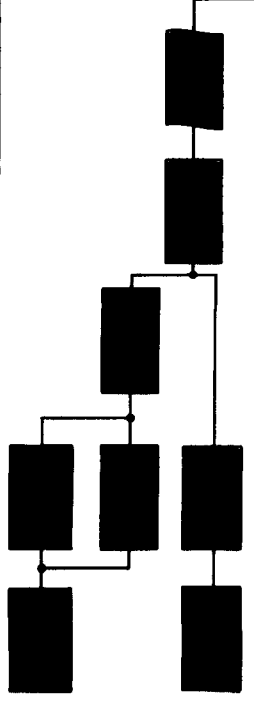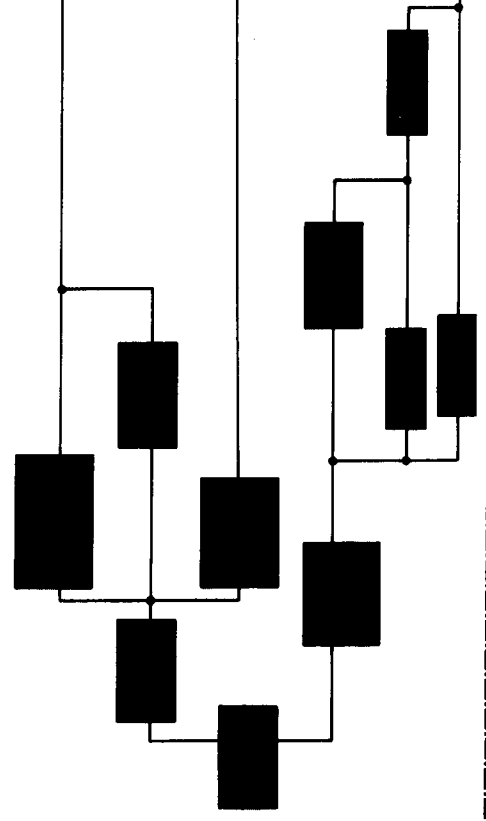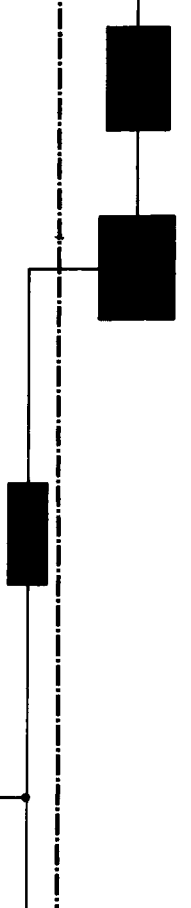
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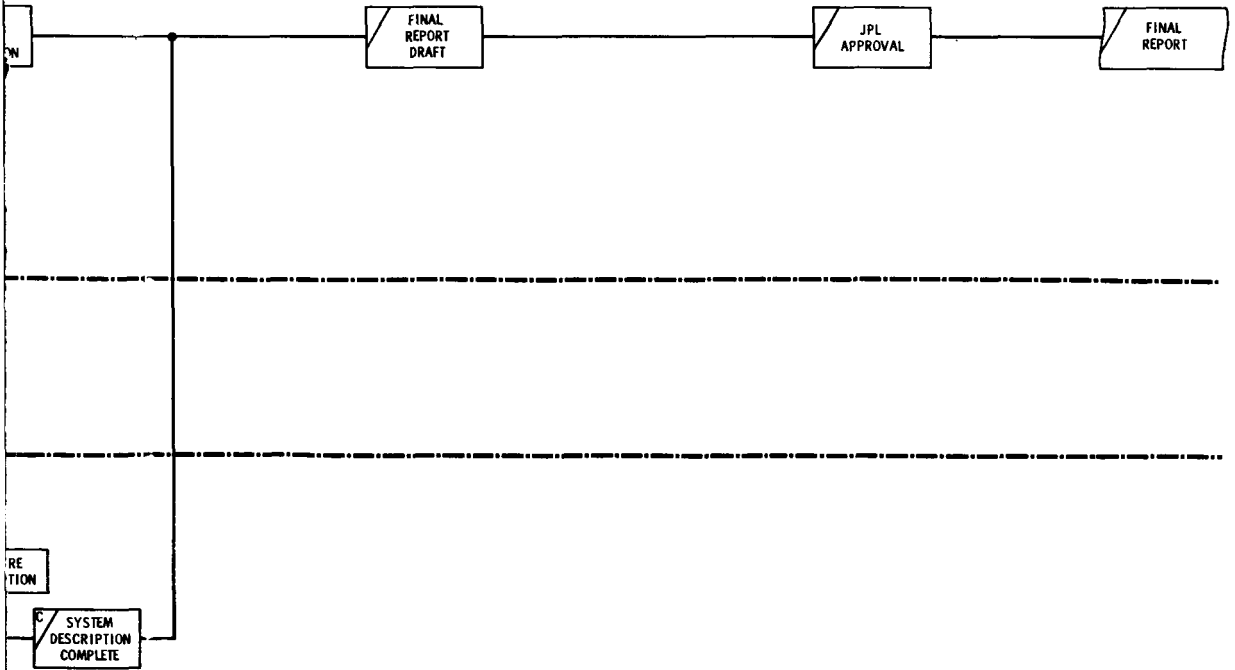
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MILESTONE
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M  MONTHLY REVIEW
   WITH JPL
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Figure 1-1. Work Flow Diagram - Mars
Spacecraft Power System Development

SECTION 2

CONSTRAINTS AND GUIDELINES

Guidelines for the study are largely drawn from the requirements for the MM '69 power system and from load profile estimates for a 1971 orbiter mission. Specific characteristics, either specified or implied, are summarized below.

2.1 POWER SYSTEM TYPE

The power system will utilize solar arrays for power generation and electrochemical batteries for energy storage.

2.2 SOLAR ARRAY ORIENTATION

The solar arrays will be fully sun oriented, except for brief maneuver periods when power will be supplied by the spacecraft batteries.

2.3 DISTRIBUTION

To least disturb the power system interface with other spacecraft subsystems and OSE as presently defined for the MM '69 system, the types of distributed power will be identical to that of the MM '69 system:

Regulated ac power

50 volt rms, single phase, 2.4 kHz

27.2 volt rms, three phase, 400 Hz

28 volt rms, single phase, 400 Hz

Unregulated dc power

25 to 50 volts, extreme limits

2.4 LOAD PROFILE

Power requirements by user designation, power type, and mission phase for the 1971 orbiting mission have been furnished by JPL and are summarized on Table 2-1.

Table 2-1. Power Requirements (Watts), 1971 Orbiting Mission

Flight Phases

Power Form	Load Designation	One	Two	Three	Four	Five	Six	Seven	Eight	Nine	Ten	Eleven	Twelve	Thirteen	Fourteen
2.4 KHz	DAS	-0.00	-0.00	-0.00	-0.00	-0.00	20.00	-0.00	-0.00	-0.00	-0.00	20.00	-0.00	-0.00	-0.00
	TVS	-0.00	-0.00	-0.00	-0.00	-0.00	32.00	-0.00	-0.00	-0.00	-0.00	32.00	-0.00	-0.00	-0.00
	IRR	-0.00	-0.00	-0.00	-0.00	-0.00	3.00	-0.00	-0.00	-0.00	-0.00	3.00	-0.00	-0.00	-0.00
	IRS	-0.00	-0.00	-0.00	-0.00	-0.00	4.00	-0.00	-0.00	-0.00	-0.00	4.00	-0.00	-0.00	-0.00
	UVS	-0.00	-0.00	-0.00	-0.00	-0.00	12.00	-0.00	-0.00	-0.00	-0.00	12.00	-0.00	-0.00	-0.00
	FTS	15.00	15.00	15.00	15.00	15.00	15.00	15.00	15.00	15.00	15.00	15.00	15.00	15.00	15.00
	FCS	3.20	3.20	3.20	3.20	3.20	3.20	3.20	3.20	3.20	3.20	3.20	3.20	3.20	3.20
	CC&S	39.00	19.00	19.00	19.00	19.00	19.00	19.00	19.00	19.00	19.00	19.00	19.00	19.00	19.00
	PYRO	-0.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00
	PWRD	2.25	2.25	2.25	2.25	2.25	2.25	2.25	2.25	2.25	2.25	2.25	2.25	2.25	2.25
	DSS	21.00	22.00	10.00	10.00	10.00	18.00	10.00	19.00	10.00	10.00	23.00	15.00	19.00	18.00
	A/C1	13.00	25.00	4.00	4.00	23.00	4.00	23.00	4.00	23.00	4.00	4.00	4.00	4.00	4.00
	A/C2	-0.00	-0.00	-0.00	-0.00	10.50	-0.00	10.50	-0.00	10.50	-0.00	-0.00	-0.00	-0.00	-0.00
	SCNE	5.30	5.30	5.30	5.30	5.30	28.50	5.30	5.30	5.30	5.30	16.50	5.30	5.30	5.30
	RES	32.20	32.20	32.20	32.20	32.20	32.20	32.20	32.20	32.20	32.20	32.20	32.20	32.20	32.20
	GYRE	8.00	8.00	-0.00	-0.00	8.00	-0.00	8.00	-0.00	8.00	-0.00	-0.00	-0.00	-0.00	-0.00
	T/C1	50.00	50.00	50.00	50.00	50.00	-0.00	50.00	50.00	50.00	50.00	-0.00	50.00	50.00	50.00
400 Hz, 3φ	GYRO	9.00	9.00	-0.00	-0.00	9.00	-0.00	9.00	-0.00	9.00	-0.00	-0.00	-0.00	-0.00	-0.00
400 Hz, 1φ	SCNM	-0.00	-0.00	-0.00	-0.00	-0.00	12.00	-0.00	-0.00	-0.00	-0.00	12.00	-0.00	-0.00	-0.00
	IRSM	-0.00	-0.00	-0.00	-0.00	-0.00	-0.00	-0.00	-0.00	-0.00	-0.00	3.50	-0.00	-0.00	-0.00
28 VDC	VALV	-0.00	-0.00	-0.00	-0.00	30.00	-0.00	30.00	-0.00	30.00	-0.00	-0.00	-0.00	-0.00	-0.00
	GIMB	-0.00	-0.00	-0.00	-0.00	35.00	-0.00	35.00	-0.00	35.00	-0.00	-0.00	-0.00	-0.00	-0.00
25-50 VDC	T/C2	7.30	15.00	15.00	15.00	15.00	15.00	15.00	15.00	15.00	15.00	15.00	15.00	15.00	15.00
	T/C3	4.90	10.00	10.00	10.00	10.00	10.00	10.00	10.00	10.00	10.00	10.00	10.00	10.00	10.00
	TWT	55.00	55.00	55.00	55.00	55.00	89.00	55.00	89.00	55.00	55.00	89.00	55.00	89.00	55.00
	BTCG	0.50	0.50	25.00	0.50	0.50	0.50	0.50	25.00	0.50	25.00	0.50	0.50	0.50	0.50
	BRFS	1.50	1.50	1.50	1.50	1.50	1.50	1.50	1.50	1.50	1.50	1.50	1.50	1.50	1.50

Special Load Conditions:

1. For those cases where GYRO = 0.00, abnormal alternative condition may be that GYRO = 9.00 with concurrent condition that

   A/C 1 = 16.00 and GYRE = 8.00.

2. T/C 2 = 15.00 (array operation)

   = 7.30 (battery operation)

3. T/C 3 = 10.00 (array operation)

   = 4.90 (battery operation)

Table 2-1. Power Requirements (Watts), 1971 Orbiting Mission (Cont)

Phase Number	Phase Name	Duration
One	Launch	45 minutes max.
Two	Star Acquisition	Not specified
Three	Cruise I (Battery Charger On)	Not specified
Four	Cruise II (Battery Charger Off)	Not specified
Five	Maneuver	40 minutes
Six	Far Encounter	Not specified
Seven	Orbit Insertion	100 minutes
Eight	Playback - Far Encounter	Not specified
Nine	Orbit Trim	20 to 40 minutes (Note A)
Ten	Orbit Cruise - CC&S Update	Not specified
Eleven	TV Sequence	Not specified
Twelve	Earth Occultation	Not specified
Thirteen	Playback ATR	Not specified
Fourteen	Playback DTR	Not specified

Notes:

A. 1st orbit trim no sooner than 24 hours after Orbit Insertion; subsequent orbit trims no sooner than 24 hours after previous orbit trim.

B. Sun-probe distance:

Encounter: 212×10^6 kilometers

Encounter plus 30 days: 217×10^6 kilometers

Encounter plus 90 days: 228×10^6 kilometers

2.5 TRANSIT AND ORBIT CHARACTERISTICS

Also based on information supplied by JPL, the significant orbit characteristics relating to the power system design are:

Transit time: Approximately 8 months

Arrival date: 14 November 1971

Orbit period: 12 hours

Onset of Solar Occultations: 130 days after arrival

Length of Solar Occultations: Up to 90 minutes

SECTION 3

POWER SYSTEM SELECTION

A shunt regulation system has been selected for further detailed design and comparison with the MM'69 power system. This selection was based on the relatively higher scoring of the shunt system over other candidates when judged against numerous criteria.

Three principal power system candidates were evaluated in the selection process: (1) a boost regulation system, (2) a series switching (buck) regulation system, and (3) the shunt regulation system. A single representative arrangement of the functional elements was evaluated for each candidate. Only those functions necessary to provide regulated and raw dc power were considered. Although the guidelines listed earlier indicate the distribution of ac power, its impact on candidate evaluation is not significant since dc/ac conditioning equipment is quite similar for any candidate. Any other features that could be applied with equal advantage to all candidates were also not included, such as improved methods of battery charging. The solutions to this and similar questions are considered as part of the detailed design phase which follows the selection of the principal candidate.

3.1 INFLUENCE OF SOLAR ARRAY

The variations in solar array characteristics associated with Earth/Mars transfer provide a logical starting point for considering power system candidates. It seems valid to consider that future Mariner spacecraft will utilize rigid deployed panel solar arrays similar to those used previously. Given a particular solar array design, its voltage-current characteristics with sun distance will vary in a particular way depending to a large extent on its thermal properties.

The variation in voltage-current characteristics are thus largely independent of the subsystem arrangement of which the solar array is a part. It is therefore possible to use a generalized set of solar array characteristics in examining possible subsystem arrangements.

Figure 3-1 shows a set of normalized power-voltage curves for a representative Mars spacecraft solar array design. The relative variations in the P-V curves are based on the temperature distance profile shown on Figure 3-2. The P-V curves are based on measurements made on a set of RCA 1-ohm/cm N/P cells. The procedures used in predicting the P-V variation with sun distance are summarized in Appendix A. The effect of possible errors in temperature prediction are also included in the P-V plot for 1.0 AU.

To permit relative assessments of the solar array effect on candidate subsystem arrangements, the P-V curves are normalized and hence independent of specific series-parallel arrangements of the solar cells. Normalization is shown with respect to maximum power and voltage at 1.0 AU and 140°F.

In the power system candidate discussion which follows, the influence of the P-V curves of Figure 3-1 will be referenced. It is stressed that these curves are the result of a particular cell type, namely the RCA cells mentioned earlier. The conclusions regarding solar array influence on candidate selection may be somewhat modified if other cell types are considered. This is a question being analyzed presently in relation to the shunt system detailed design activity.

The use of the P-V curves previously described implies that no active means would be used to electrically rearrange solar array sections by switching. The purpose of such switching would be twofold: (1) to add or remove array sections and thus minimize problems of handling excess power, (2) to change the series-parallel solar cell matrix to permit power availability at more favorable voltage levels as a result of large changes in V-I characteristics with sun distance. All of the power system candidates described later are able to cope with these conditions without the necessity for switching; therefore, this possibility was not considered further.
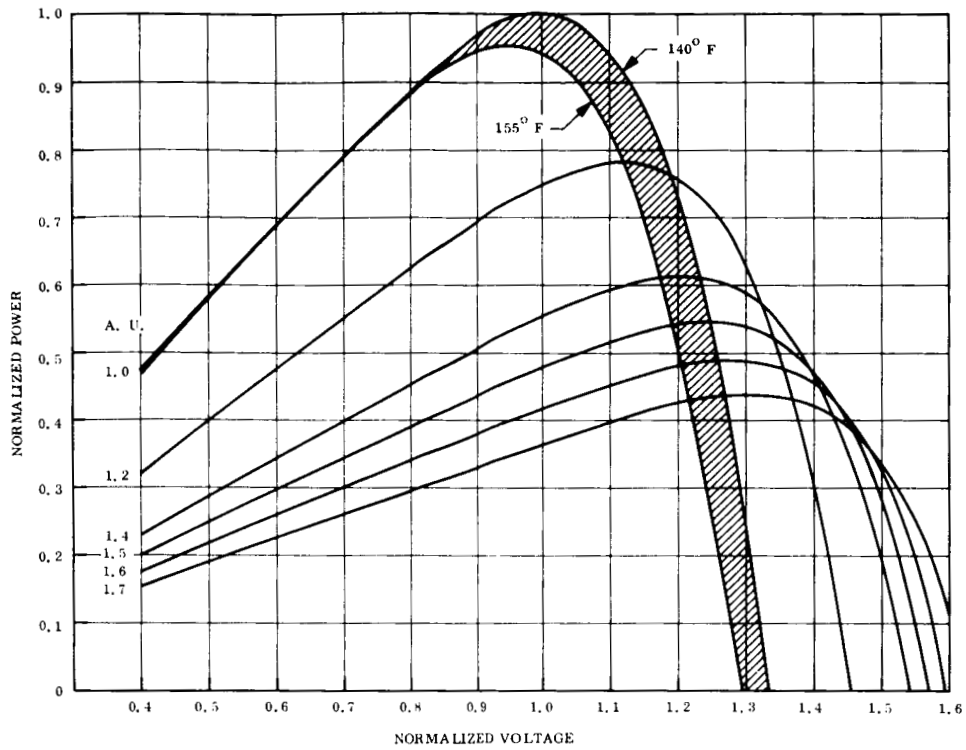
Figure 3-1.   Normalized P-V Solar Array Curves
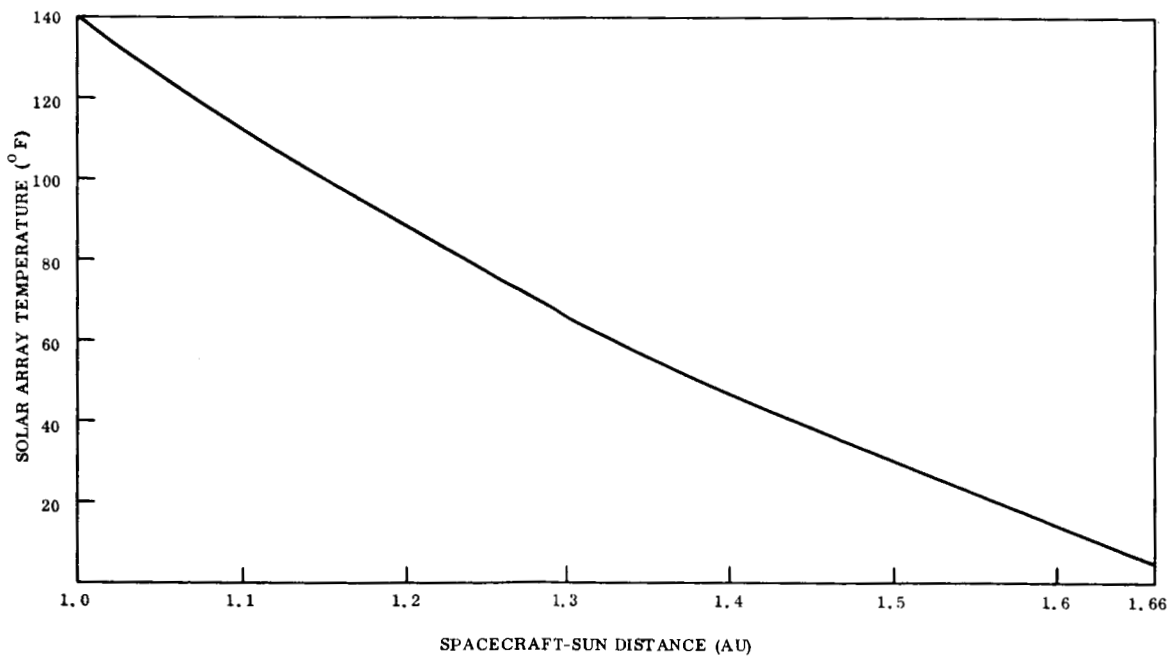
Figure 3-2.   Solar Array Temperature Versus Sun Distance

3.2 REGULATOR EFFICIENCY

Regulator efficiency data used in evaluating the candidate systems is shown on Figure 3-3.
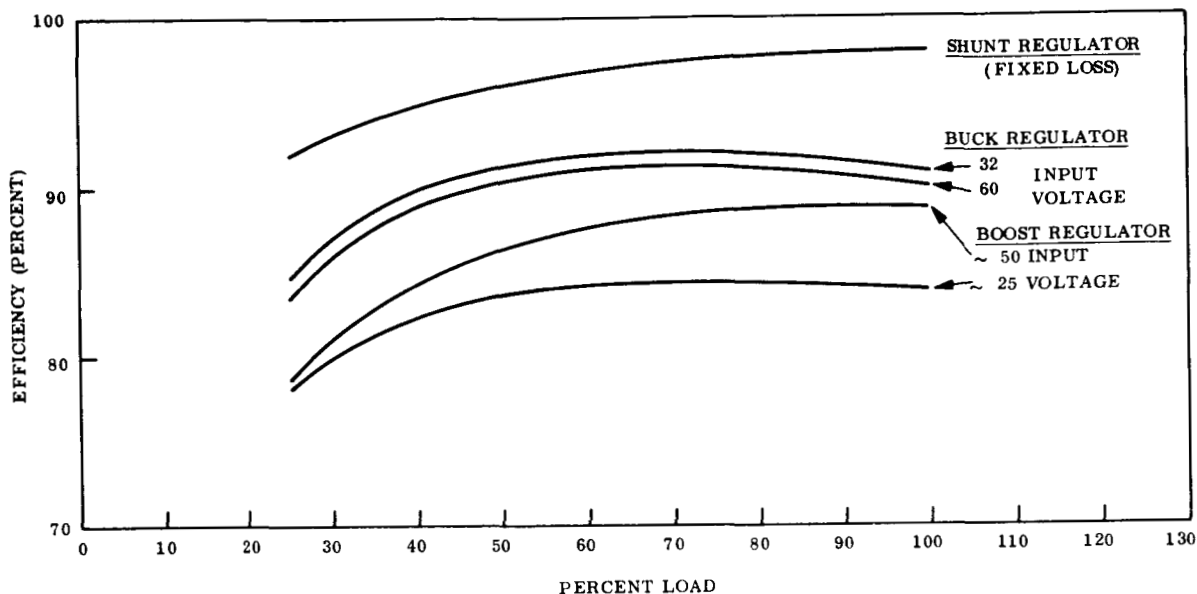
Figure 3-3. Regulator Efficiency Data

The boost regulator data is based on the efficiencies cited in the 1971 load profile information and reflects the performance of the regulator used in the MM'69 power system.

The buck regulator data is based on a design rated at 600 watts and 30 vdc which was built as a breadboard and performance tested.

The shunt regulator data is based on assuming an efficiency of 98 percent at rated load with 2 percent used for the regulator control electronics. At partial loads, it is assumed that the same amount of control power is required which results in the overall efficiency decrease shown.

3.3 CANDIDATE DESCRIPTIONS

3.3.1 BOOST SYSTEM

This candidate system is shown on Figure 3-4(a) and has the general characteristics of the MM'69 power system.

The boost regulator requires that all input operating voltages be lower than the regulated output voltage. The necessary voltages to meet this condition are shown on Figure 3-4(b) with reference to the normalized values for the solar array (Figure 3-1). The procedure for selecting these levels is described in the following paragraphs.

First, as shown on Figure 3-1, for an arrival at Mars between 1.4 and 1.6 AU, maximum power is available at a normalized voltage, V_N, of around 1.25. For these particular P-V curves, there is a negligible power difference if V_N is used between 1.2 and 1.3, corresponding to AU distances of 1.4 and 1.6, respectively. An intermediate value of 1.25 appears appropriate under this circumstance.

With array power at Mars drawn at $V_N = 1.25$, it is necessary that the maximum allowable boost input level be set higher than 1.25, with allowance made for zener shunt tolerances. The zener shunt is used to assure that the boost input limit is not exceeded. This could occur as a result of solar array tolerance buildups or upon emergence from solar occultations (i.e., a cold array producing high voltage). With these constraints, V_N for the boost output bus is set at 1.4 with a loose zener tolerance of V_N equal to 1.3-1.4.

A battery charging voltage must be selected which does not interfere with the ability to draw sufficient array power in the near-Earth phase of operations. If, for example, a series dissipative charge regulator is used and its minimum input voltage is set at $V_N = 1.25$, then Figure 3-1 indicates that insufficient array power is available at 1.0 AU, especially if the solar array operates at $155^{\circ}F$ rather than the nominally predicted temperature of $140^{\circ}F$ for Mariner panels. By lowering the charger input to $V_N = 1.05$, this problem is avoided and the only penalty is the need for a wider boost input voltage range.

The battery charge to discharge voltage ratio is typically 1.35:1 (for Ag-Zn, $V_{charge} = 1.94$ and $V_{discharge} = 1.44$). With a conservative allowance made for a voltage drop through the charge regulator, the total voltage ratio of charger input to battery discharge is about 1.5:1 corresponding to the V_N values of 1.05 and 0.7 shown on Figure 3-4(b).

The limits described above result in a 2:1 variation in raw voltage.

With a boost system designed for these general limits, considerable latitude exists in the design voltage for the solar array. If the array were designed to provide sufficient near-Earth power at $V_N = 1.05$ (the charger input lower limit), this would represent an array voltage reduction of 12 percent from the V_N value of 1.19 which provides the same power for 1.0 AU and $155^{O}F$ array as at $V_N = 1.25$ and 1.5 AU. This is the same as saying that the number of solar cells in series may be varied by about 12 percent without affecting system operation.

The boost system requires a means for avoiding the simultaneous supply of power from the solar array and battery, although the array might be fully capable of supplying all power. This possibility could occur during certain sequences when the battery clamps the array voltage at a value below its optimum point. A share boost regulator is incorporated to avoid this condition in the manner used on the MM'69 system. Another possibility is to reduce the load momentarily through appropriate sensing logic.

3.3.2 SERIES SWITCHING (BUCK) SYSTEM

This candidate system is shown on Figure 3-5(a).

The buck regulator requires that all input operating voltages be higher than the regulated output voltage as shown on Figure 3-5(b).

As with the boost system, maximum power at Mars is available at $V_N \approx 1.25$. Sufficient near-Earth power is available at $V_N \approx 1.2$ which sets the minimum charge regulator input

SOLAR ARRAY

CHARGE REGULATOR

SHARE BOOST

BOOST REG

RAW

$\eta_A = 0.89$
$\eta_B = 0.85$

(A)

BOOST INPUT CHARACTERISTIC

ARRAY V_N RANGE: ~ 0.25
MARS/EARTH MATCHING PENALTY $= 0$

V_N, NORMALIZED VOLTAGE

RAW $\sim 2:1$

$V_N = 1.25$

ZENER LIMITS
REG BUS

1.4
1.3

1.05

MIN CHARGER INPUT

0.7

DISCHARGE

$V_N = 0.95$

155F

I
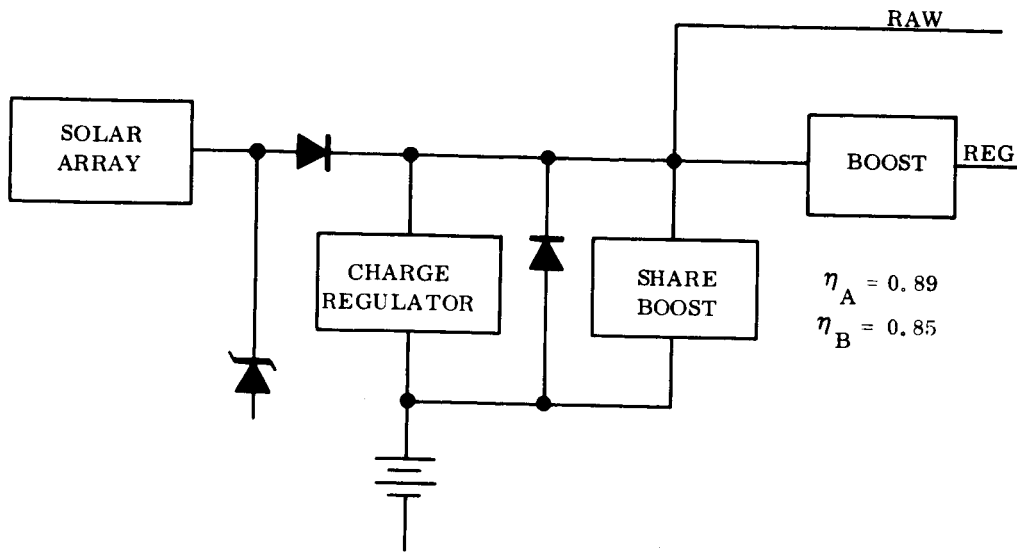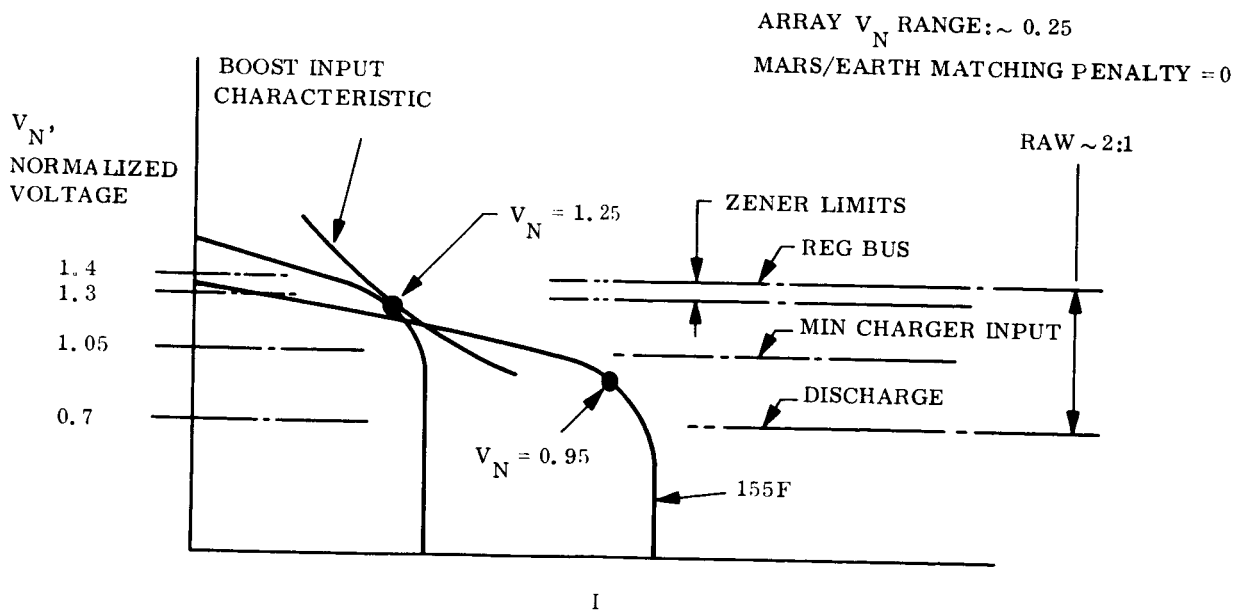
(B)

Figure 3-4. Boost Candidate

RAW

SOLAR
ARRAY → ▷ ─── CHARGE
REGULATOR ─── ▲ ─── SHARE
BOOST ─── BUCK ── REG

$\eta_A = 0.92$
$\eta_B = 0.91$

(A)

ARRAY V_N: 1.2

MARS/EARTH MATCHING PENALTY = 0

BUCK INPUT
CHARACTERISTIC

V_N,
NORMALIZED
VOLTAGE

$V_N = 1.25$

RAW 1.7:1

1.2

MIN CHARGER INPUT
DISCHARGE

0.8
0.75

REG BUS

$V_N = 0.95$

155 F

I
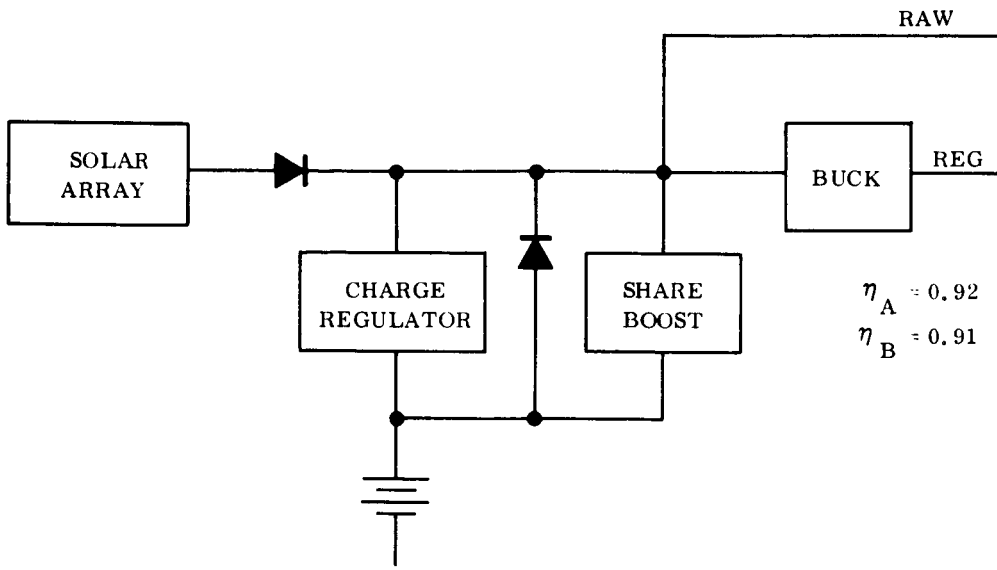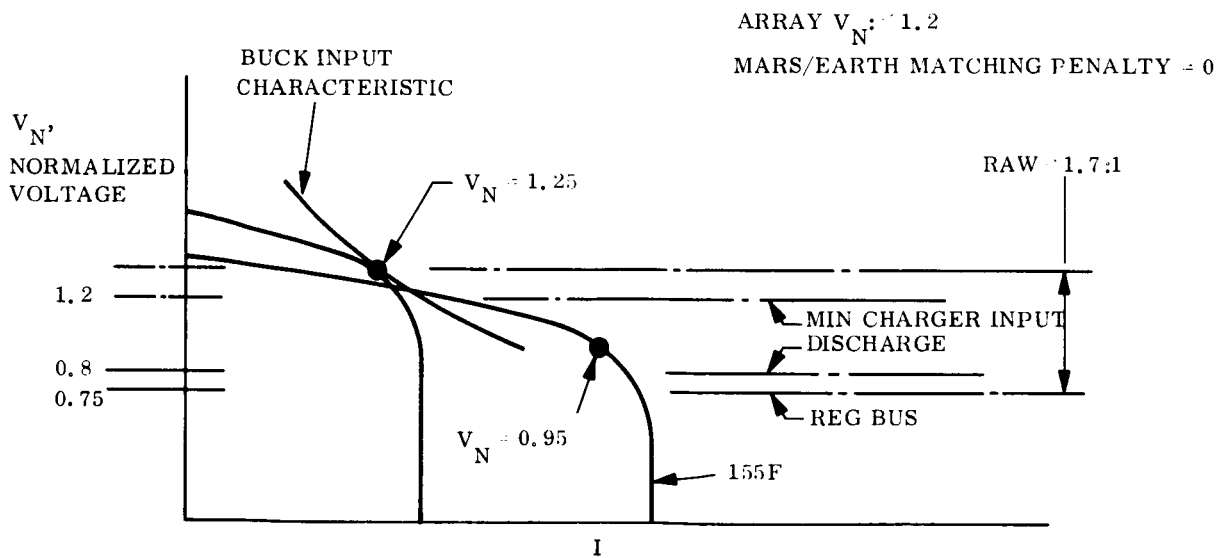
(B)

Figure 3-5. Buck Candidate

voltage. Again, conservatively allowing a 1.5:1 ratio for the relationship of charger input voltage to battery discharge voltage, the latter voltage is set at $V_N = 0.8$. An estimated minimum voltage drop of $V_N = 0.05$ is allocated to the buck regulator to result in a regulated bus level at 0.75.

These established limits result in a 1.7:1 variation in raw voltage.

In this system, an even greater variation in the array design voltage exists. The lower limit is set by conditions which mutually satisfy the near-Earth power demand and the charger input voltage. The higher limit is set by the regulator transistor ratings or the desire to limit the raw power range. A 2:1 input to output range for a buck regulator is realistic which would allow an increase to $V_N = 1.5$ over 1.25. This is equivalent to permitting an array design with 20 percent more cells in series. If the 2:1 range on the regulator was an absolute requirement, it is likely that zener shunts would be required to prevent excess voltage during cold array conditions (emergence from occultations, etc.).

This system also requires a means for avoiding the array/battery load sharing problem.

3.3.3 SHUNT SYSTEM

This candidate system is shown on Figure 3-6.

Regulated dc power is drawn directly from the solar array and is controlled by a partial shunt regulator in the form of multiple shunt transistors across separate semi-sections of the solar array.

The Sequence Control provides the base drive signal to the shunt transistors and also provides control signals for sequencing operation of the charge regulator and boost regulator. This sequencing is necessary to prevent (1) simultaneous shunt and boost operation, and (2) simultaneous battery charging and boost operation. The method of sequencing is explained more fully on Figure 3-6(b). The Sequence Control establishes shunt, charge regulator,

and boost regulator operation as a function of the voltage level within the voltage regulation range. Assume for example that the regulated bus is set at 50 volts ± 1 volt; then the voltage regulation range is 2 volts. Figure 3-6 indicates that the range is divided into three roughly equivalent bands, each devoted to a different control mode. The range of the upper band varies the shunt from "full on" at its high level to "full off" at its low level. The middle band similarly varies the charge regulator, and the lower band inversely varies the boost from "full off" at its high level to "full on" at its low level. The Sequence Control of the charge regulator is an override control over the normal charge regulator control functions. If the shunt regulator is operating, i. e., it is draining away excess array power, and the battery is fully charged, the charge regulator would probably only be supplying trickle power depending on the charging method used. Any subsequent Sequence Control override signal would in that case not affect the charge regulator operation.

Raw power is drawn from a separate set of solar array isolation diodes or through a diode from the battery. It would have been possible to use the scheme shown on Figure 3-7 which results in an additional diode voltage loss for solar array power. In the interest of efficiency, the arrangement of Figure 3-6(a) was selected for further study.

The determination of relative voltage levels is shown on Figure 3-6(c). Again $V_N = 1.25$ provides the maximum power capability at Mars. However, since the array voltage is constant throughout the mission (same as regulated voltage), there would be a power deficiency in near-Earth operation as seen on Figure 3-1. The selection $V_N = 1.2$ avoids this condition with a penalty of several percent in the power available at Mars.

The 1.5:1 ratio for the relative values of charger input to battery discharge is used as before which results in a similar ratio for the raw power range.

The selection of a partial shunt over a full shunt is based on its lower thermal dissipation within the shunt elements. Figure 3-8 shows the full and partial shunt options and their modes of operation relative to the solar array V-I curve. If the voltages of the two V-I curves for

3-10

(A)

(B)

(C)
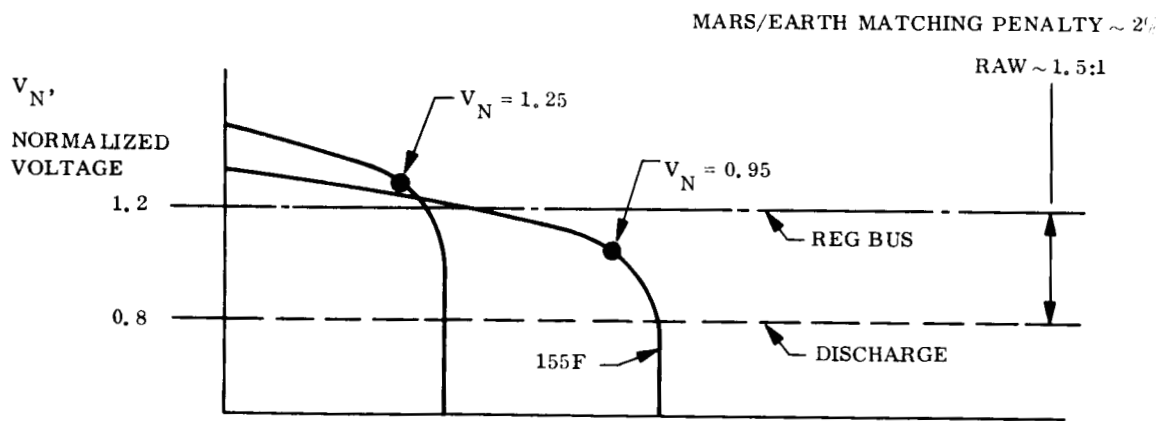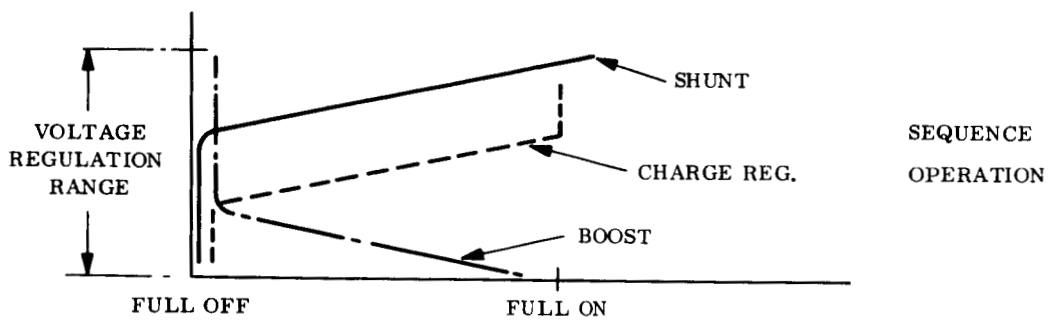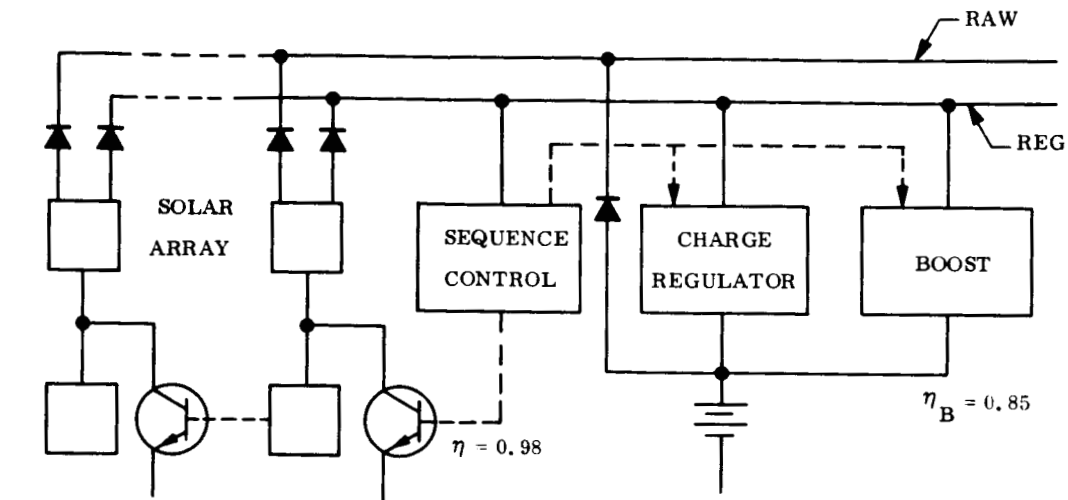
Figure 3-6.   Shunt Candidate

ADDITIONAL DIODE LOSS

RAW

REG

SOLAR
ARRAY

SEQUENCE
CONTROL

CHARGE
REGULATOR

BOOST
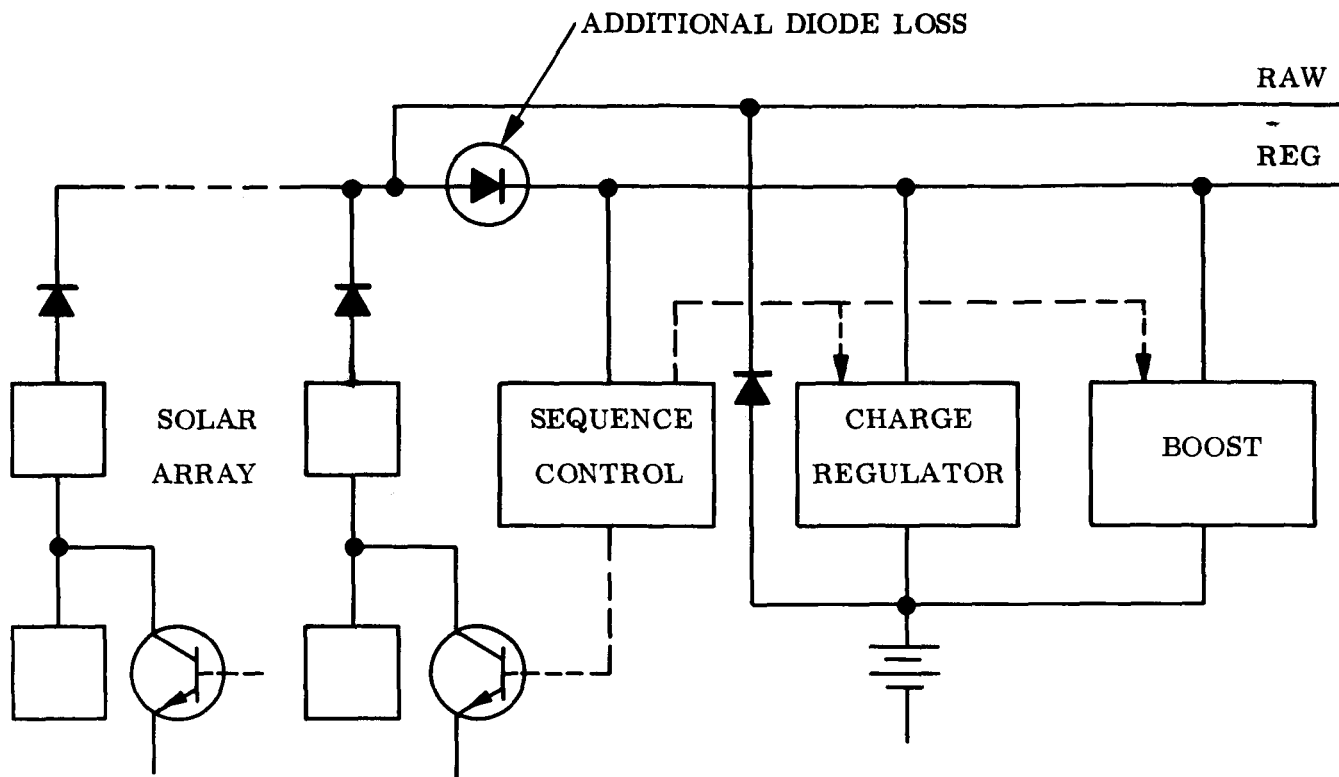
Figure 3-7. Raw Power Source Alternative

the partial shunt case were added, they would result in the full shunt V-I curve. As shown on the sketch, these are drawn to scale relative to each other, and it becomes apparent that the partial shunt dissipation is significantly less. It is also clear that the current requirement for both types is about equivalent.

Figure 3-9 shows the shunt analysis for a solar array quite similar in size to the MM'69 solar panels. This particular array would produce about 900 watts at 1.0 AU at a panel temperature of 100°F. The curve shows the dissipation from either a full or partial shunt for a nominal demand load of 200 watts. The dissipation is shown as a function of array temperature to identify the maximum dissipation that might occur during emergence from an Earth eclipse. Each shunt section has a transistor and resistor in series. The dotted lines indicate the heat dissipation associated only with the transistors which is almost the same for the full and partial shunt cases. It is possible that no resistors will be required for the partial shunt case. It was therefore selected for use in the shunt system candidate.

● FULL SHUNT
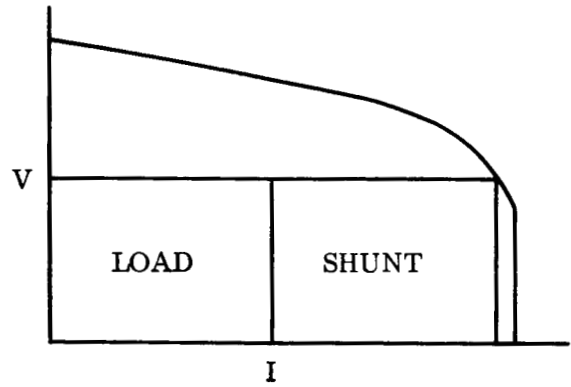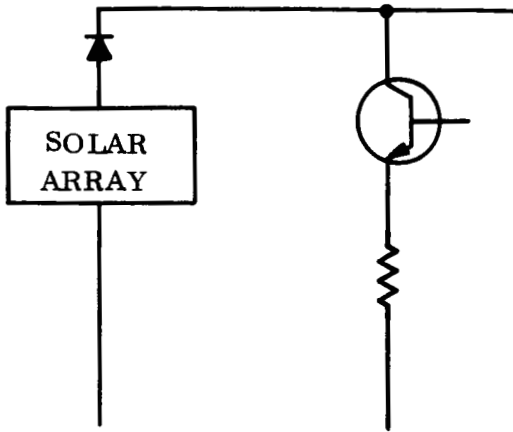
● PARTIAL SHUNT - SINGLE SECTION
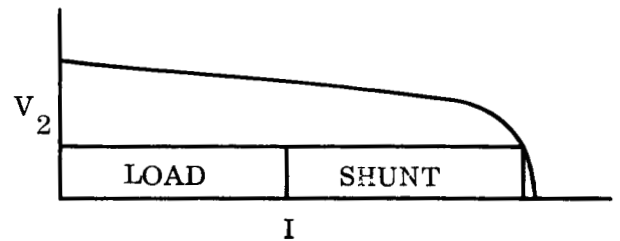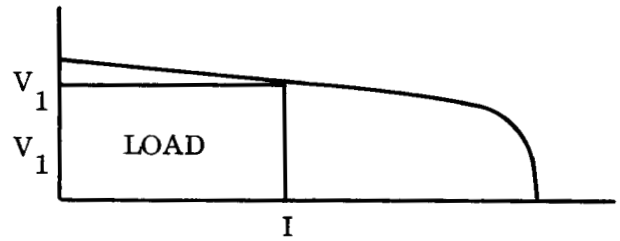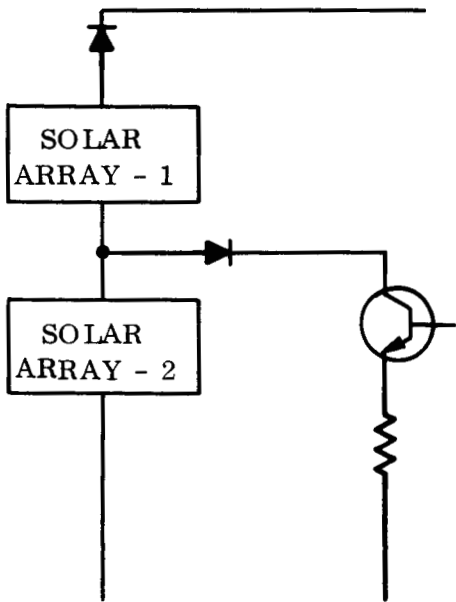
Figure 3-8. Shunt Regulator Options
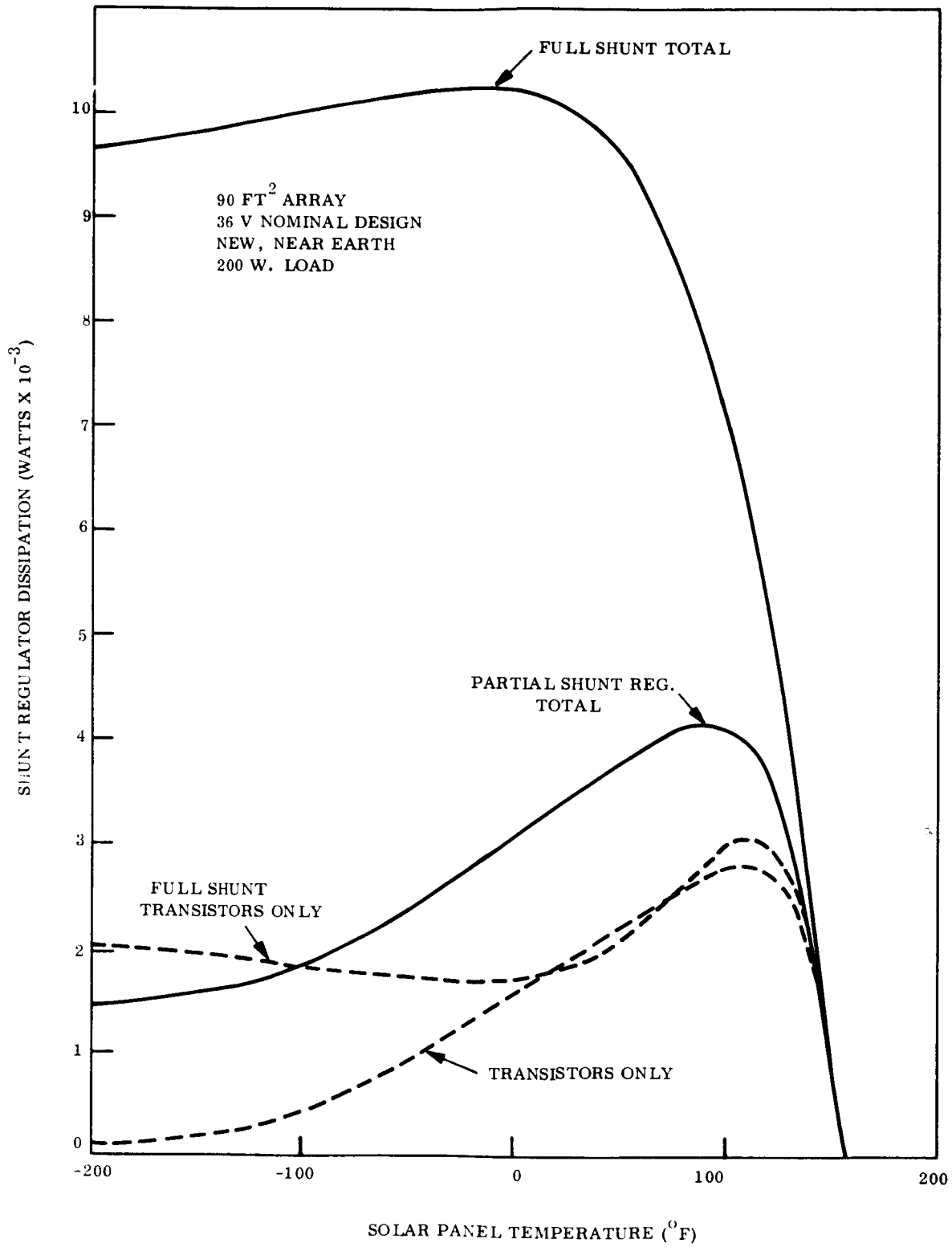
Figure 3-9. Shunt Performance

3.4 CANDIDATE COMPARISON

The three candidate systems are compared on the matrix shown on Table 3-1. The rating of each candidate against a particular criterion is indicated in the rating columns where "1" indicates the highest rating, "2" the intermediate rating, and "3" the lowest rating. The lowest summation of these ratings provides the basis for candidate selection.

Pertinent discussion for each criterion is provided below:

Relative Battery Demand

For regulated loads, battery demand in the boost and buck systems is inversely proportional to the regulator efficiency and the discharge diode efficiency, assumed to be 0.97. Then the relative demands are:

$$\frac{\text{Buck demand}}{\text{Boost demand}} = \frac{0.85 \times 0.97}{0.91 \times 0.97} = 0.94$$

using the regulator efficiencies cited in Figure 3-3. The shunt system does not contain a battery discharge diode to the boost regulator and therefore,

$$\frac{\text{Shunt demand}}{\text{Boost demand}} = \frac{0.85 \times 0.97}{1.85} = 0.97$$

For raw loads, all three candidates provide battery power to the raw bus through diodes and therefore no battery demand difference exists.

Relative Array Demand

For regulated loads, array demand is inversely proportional to regulator efficiency:

$$\frac{\text{Buck demand}}{\text{Boost demand}} = \frac{0.89}{0.92} = 0.97$$

Table 3-1. Candidate Comparison

Criterion		Boost	R*	Buck	R*	Shunt	R*
Relative Battery Demand	Reg loads	1.0	3	0.94	1	0.97	2
	Raw loads	1.0	–	1.0	–		–
Relative Array Demand	Reg loads	1.0	3	0.97	2	0.93	1
	Raw loads	1.0	1	1.0	1	1.02	2
	Charge Power	small+	–	small	–	small-	–
Packaging		Compact	2	Compact	1	Shunt wiring	3
Bay Thermal Design		Battery Integr.	–	Battery Integr.	–	Battery Integr.	–
Raw Bus Limits		2:1	2	≥ 1.7:1 (Zeners?)	2	1.5:1	1
Reg Bus Limits		±2%	–	±2%	–	±2%	–
Ripple, day		PWM reg	2	PWM reg	2	Shunt	1
Ripple, night		PWM reg	–	PWM reg	–	PWM reg	–
Response		Medium	–	Medium	–	Medium	–
Battery Charger Integration		Variable Voltage Input	2	Variable Voltage Input	3	Fixed Voltage Input	1
Operational Complexity		Share Boost	2	Share Boost	2	Sequence control, no switching	1
Flexibility/ Growth		Regulator Size Limit	2	Regulator Size Limit	2	Add shunt elements (day operation)	1
Redundancy Implementation		Single Function	1	Single Function	1	Multi-Functions	2

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Table 3-1. Candidate Comparison (cont)

Criterion	Boost	R*	Buck	R*	Shunt	R*
Failure Modes						
Regulator-Array Operation:						
Open	Results in short	2	Complete power loss	2	Minor effect (multiple units)	1
Short	$V_{BUS}<V_{BATT}$	3	$V_{BUS}=V_{ARRAY}$	2	Array section loss	1
Control Failure	$V_{BUS}\geq V_{ARRAY}$	3	$0 \leq V_{BUS} \leq V_{ARRAY}$	2	$V_{BATT}\leq V_{BUS}\leq V_{ARRAY}$	1
Regulator-Battery Operation:						
Open	Results in short	–	Complete power loss	–	Results in short	–
Short	$V_{BUS}<V_{BATT}$	2	$V_{BUS}=V_{BATT}$	1	$V_{BUS}<V_{BATT}$	2
Control Failure	$V_{BUS}\geq V_{BATT}$	1	$0 \leq V_{BUS} \leq V_{BATT}$	2	$V_{BUS}\geq V_{BATT}$	1
Ease of Test On Pad	Wide ground power limits	1	Wide ground power limits	1	Tight ground power limits, shunt simulation probable	2
Flight Demonstration	Yes	1	Partly (Nimbus B)	3	Partly (Lunar Orbiter)	2
TOTALS		33		30		25

* Rating Scale:

    1 = Highest
    2 = Intermediate
    3 = Lowest

$$\frac{\text{Shunt demand}}{\text{Boost demand}} = \frac{0.89}{0.98} = 0.91$$

The shunt system incurs an Earth/Mars matching penalty of several percent (see Subsection 3.3.3) and therefore, the relative shunt demand is raised to 0.93.

For raw loads, array power is supplied directly to the raw bus for all candidates. Again the shunt system is penalized by two percent to raise its relative demand to 1.02.

For charge power, small differences in charge power are associated with the relative battery demand--this is not significant as a measure.

Packaging

No major differences are involved. The bay equipment is about the same for all candidates. The buck system may or may not require zener shunts on the array. The boost system requires zeners; the shunt system requires transistors plus additional wiring for the base drivers. Therefore, they are rated 1, 2, 3 in that order.

Bay Thermal Design

No significant difference. Main thermal problem is probably battery integration which is common to all candidates.

Raw Bus Limits

Limits are indicated on Figures 3-4, 3-5 and 3-6.

Regulated Bus Limits

No measure--similar limits should be achievable with pulse width modulated electronics of all candidates.

Ripple, day; with array power, the shunt system should be best since switching electronics is not in use.

Ripple, night; no measure--with battery power switching electronics is used in all candidates.

Response; no measure--all candidates depend on response of switching electronics.

Battery Charger Integration

A smaller variation in the charger input voltage results in a smaller average drop through the regulator resulting in more efficient power usage. The shunt system, with a fixed charger input voltage, is best in this regard. The buck system may or may not be worse than the boost system depending on whether or not zener array voltage limiters are used.

Operational Complexity

The boost and buck systems require some means for avoiding solar array/battery load sharing while the shunt system requires a sequence control. Since no switching of relays is required for the shunt system, it is rated better.

Flexibility/Growth

Power capability during array operation for the boost and buck system is limited by the regulator ratings. The growth of the shunt system is accommodated by adding shunt elements. (Shunt control can be initially designed for possible growth.) During battery operation all systems are limited by regulator size.

Redundancy Implementation

Redundancy schemes for the shunt system may be complicated by multi-functions operating from a single Sequence Control.

Failure Modes

Regulator-Array Operation

a. Open power transistor: Circuit review of the boost regulator indicates that an open circuit of one transistor would result in a short to ground of the remaining transistor with complete power loss; the bypass diode capability would be ineffective. An open transistor in the buck regulator obviously results in complete power loss. An open shunt transistor of the shunt system results in no power loss; the system can be easily designed to permit several such failures with remaining transistors absorbing the additional shunt load.

b. Shorted power transistor: For the boost regulator circuit, this is a short to ground with probable full power loss. For the buck regulator, this is a through short and the output is the same as the array voltage input. A shorted shunt transistor only results in loss of the associated array section.

c. Control failure: With bypass diode capability in the boost regulator the output could be higher but no less than the array input voltage. Inherently the buck regulator cannot produce an output voltage higher than its input; therefore, a control failure could result in output between zero and the highest array input. With the shunt system the array voltage and bus voltage are identical; this voltage can be drawn downward to the battery voltage by virtue of the bypass diode capability of the battery discharge boost regulator.

Regulator-Battery Operation

a. Open power transistor: Complete power loss for all candidate systems--no measure.

b. Shorted power transistor: Probable complete power loss for boost system or shunt system due to short to ground of boost regulator. Through short of buck regulator results in bus voltage same as battery voltage.

c. Control failure: With bypass diode capability in boost regulator the output could be higher but no less than the battery input voltage; this applies to the boost and shunt systems. Buck regulator maximum output is limited to battery input voltage.

Ease of Test-On Pad

Both the boost and buck systems can accept wide variations in ground power voltage during on-pad operations by way of array simulation or other power supplies. The boost and buck regulators automatically condition this raw input. The shunt system cannot function in this

way since the shunt transistors are diode isolated on the solar array. Until appropriate solutions are found, the shunt system is rated lower on this criterion.

Flight Demonstration

The boost system has been used extensively on Mariner and Ranger spacecraft. The buck system has been used on battery powered military satellites and is used on the Nimbus B spacecraft to be launched shortly. The shunt system was used on the Lunar Orbiter space-craft in a somewhat different arrangement.

The summation of ratings results in the selection of the shunt system as the candidate for further comparison with the MM'69 power system.

SECTION 4
BATTERY CONSIDERATIONS

4.1 REQUIREMENTS

The power requirements for the Mars vehicle have been summarized in Section 2. Some of the more important facts concerning the battery design will be outlined here.

The primary difference between the battery requirements for this mission and other Mariner missions is that battery power will be required at the time of planet encounter and also after encounter. This requirement may exist for one of two cases. In Case I power is required for orbit insertion maneuvers and subsequent orbit trim maneuvers. In Case II power is required for solar eclipse periods during planetary orbit in addition to the insertion and orbit trim maneuvers. The orbit cycle would be in the order of 12 to 24 hours with a 1 to 2 hour eclipse. The battery requirement could be from just a few to several hundred cycles, with the battery being charged during daylight periods by the solar array.

4.2 BATTERY CANDIDATES

There are three types of batteries which could be considered for use in the Mars vehicle power system. These batteries, all of the alkaline class, are secondary silver zinc, silver cadmium, and nickel cadmium.

The present Mariner battery is representative of a secondary silver-zinc battery and is an important contender in any future Mariner-type missions. Other silver-zinc batteries specifically designed for maximum cycle life with maximum energy density, are also worthy of consideration. Consequently GE-MSD initiated a test program two years ago to investigate the operating characteristics of such silver-zinc and silver-cadmium batteries. Previous work carried out by GE-MSD and work performed by other investigators was believed extensive enough to develop the characteristics of standard nickel-cadmium cells and were not included in the aforementioned test program. However, cells containing a new "third electrode" charge control device have been purchased recently and are being tested. Some of the highlights of the silver cell test program are reported here.

As mentioned previously, these test were concerned with secondary, or rechargeable cells. The primary purpose of the test program was to determine the float capability and cycle life of silver cells representative of the latest state of the art. The Eagle Picher Company of Joplin, Missouri was selected as the vendor for both types of cells.

4.2.1 SILVER-ZINC CELLS

The silver-zinc cells have a nominal capacity of 50 ampere-hours and are assembled in Lustran plastic cases with pressure gages attached. Each cell measures 6-1/8 inch high by 3-1/8 inch wide by 1-1/16 inch thick and weighs 1.55 pounds, exclusive of the pressure gage assembled to each cell. The 152 square inches of silver oxide is contained on 6 plates while the negative electrode consists of 7 zinc plates containing 2 percent mercuric oxide. Separation consists of two layers of polyvinyl alcohol and six layers of cellophane. Each cell contains 113 cc of 40 percent KOH electrolyte.

Cells were tested in packs of five and underwent charge and discharge characteristic tests, and 7- and 24-hour charge/discharge cycles. In addition, some cell packs were placed on float charge for several months and then subjected to repetitive cycling. A summary of tests on the silver-zinc cells is shown in Table 4-1. All cycle tests included a one hour discharge.

Table 4-1. AG-ZN Test Summary

Pack No.	Months Test 1 2 3 4 5 6 7 8 9 10 11	Cycles To Failure
1 to 5	✗ Charge Tests	--
6 to 10	✗ 7 Hr Cycle, 40% DOD	94
11 to 15	✗ 7 Hr Cycle, 20% DOD	314
16 to 20	✗ 24 Hr Cycle, 40% DOD	83
21 to 25	7 Mo. Float ⊢✗ 7 Hr Cycle 20% DOD	169
*26 to 30	✗ 24 Hr Cycle 20% DOD	290
*31 to 35	➤ Voyager Power Profile-Float and Cycle	
*36 to 40	➤ Float and Cycle at 30° F	

* Tests Continuing

4.2.1.1 Charge Tests

To determine the most favorable charging procedure to use with these cells, the first part of the test program consisted of charge characterization tests. The charge regime selected was a constant current to a selected voltage limit, with the current tapering at this point holding the charge voltage at the selected level throughout the remainder of the charge period.

After several formation cycles, the pack was discharged a fixed amount (60, 40, or 20 percent of nominal capacity) and recharged to a specified voltage limit (1.96, 1.94, or 1.92 volts/cell, average). Maximum current levels were from 2 to 10 amps. Most of the charge tests were carried out at 75°F, with a few at 30°F for comparative purposes. The only difference attributable to the lower temperature was that charge acceptance was somewhat lower at low temperatures.

Typical data is plotted in Figure 4-1, where charge acceptance as a function of charge time is shown for three different voltage levels for a battery which had previously been discharged to a 60 percent depth of discharge.
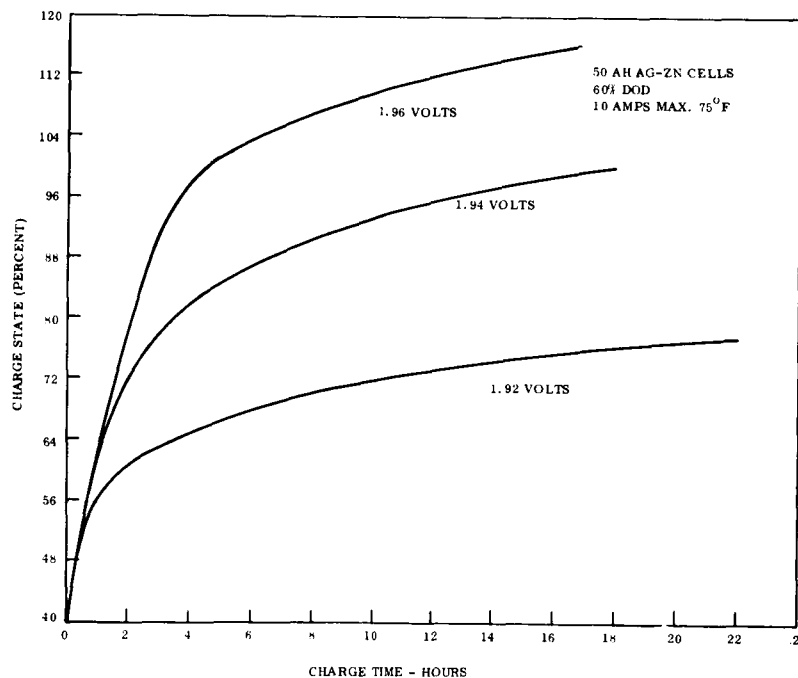
Figure 4-1. Ampere Hours Versus Charge Time

From these tests it was possible to determine the optimum charge voltage to use as a function of depth of discharge and charge time. It was determined that an average voltage level of 1.92 volts per cell was generally too low to allow completion of the charge while a voltage level of 1.96 volts per cell frequently resulted in gas generation during the charge. The level of 1.94 volts was selected for charging, resulting in a limitation on the depth of discharge for shorter cycles.

The charge data may be represented in another way as shown in Figure 4-2. Here the point at which tapering of the current occurs is plotted as a function of the charge current. The curve is valid for a cell voltage limit of 1.94 volts per cell. The plot shows the time necessary to complete the charge from a given depth of discharge. In Case A, a 2.0 amp rate is used as the maximum charge current. Starting from a 50 percent depth of discharge (DOD) it can be seen that 15 ampere-hours may be returned in 7.5 hours reducing the DOD to 20 percent. To complete the charge requires an additional 14.5 hours.

A close study of the data presented in Figure 4-2 suggests that it might be advisable to operate the battery at less than full charge. Suppose that it is desired to remove 15 ampere-hours of capacity from the battery. Case A shows that in operating between 20 and 50 percent DOD, the 15 ampere-hours could be returned to the battery in 7.5 hours, while Case B shows that trying to return this 15 ampere-hours to a battery operating between 30 percent DOD and full charge would require 17.5 hours. It must be assured that cycle life does not suffer from the fact that the battery is operating from less than a fully charged condition.

4.2.1.2 Discharge Tests

A set of typical V/I curves was generated for this cell by discharging the cell at various rates and measuring the corresponding stabilized voltage. Data is shown in Figure 4-3 for temperatures of 40, 75, and 90°F.
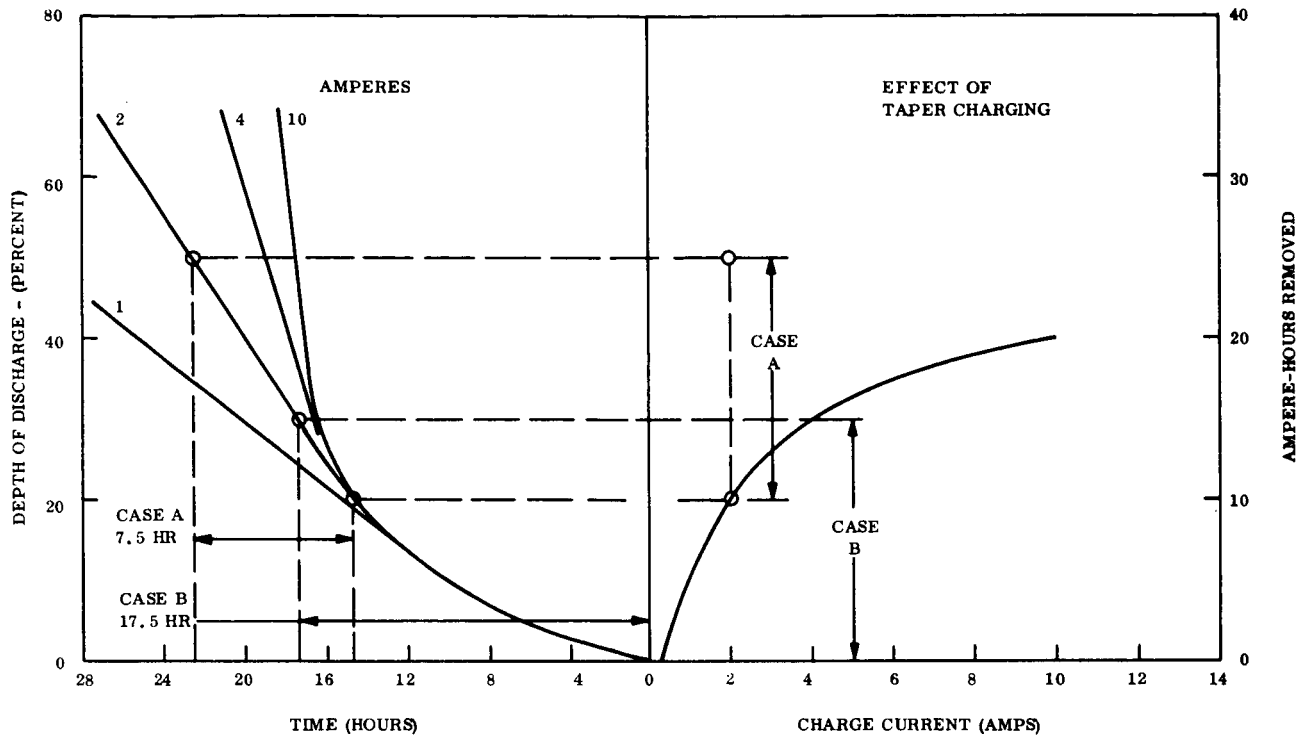
Figure 4-2. Charging Characteristics 50 AH, Ag-Zn Cells, 1.94 Volts/Cell Limit
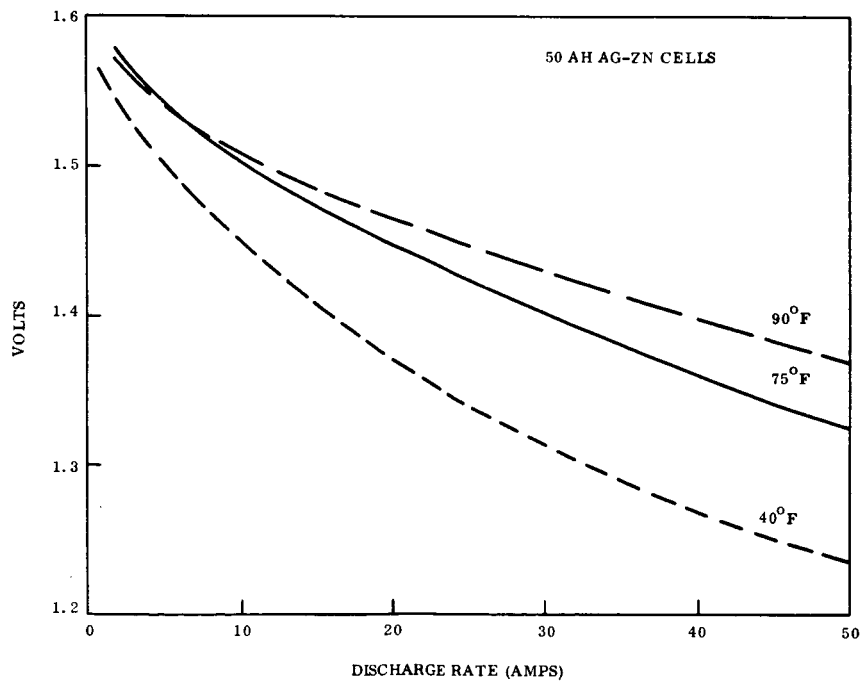
Figure 4-3. Volts Versus Discharge Rate

4.2.1.3 Cycle Tests

Cell packs were put on automatic 7- and 24-hour cycles at room ambient conditions discharging to a 20 or 40 percent depth of discharge. The results of the tests are summarized in Table 4-1. When comparing the results of the tests it may be noted that the total life of the battery pack appears to be a function of the number of cycles rather than the time on test. Compare the 40 percent DOD tests (94 7-hour cycles and 83 24-hour cycles) with the 20 percent DOD tests (314 7-hour cycles and 290 24-hour cycles). While the results of the 40 percent DOD tests are disappointing, the 20 percent DOD tests are encouraging, especially when it is recalled that this silver-zinc cell at a 15 percent DOD is equivalent in usable energy density to a nickel-cadmium cell at a 60 percent DOD.

Plots of average end-of-discharge voltage versus cycle number are shown in Figure 4-4 for the 20 percent DOD 7-hour cycle and in Figure 4-5 for the 20 percent DOD 7-hour cycle.

In all cases, silver-zinc cell failure was caused by internal cell shorting. Because of the use of a relatively low charge voltage limit, 1.94 volts/cell, cell gassing was not a problem and cells did not leak or dry out. Also the polyvinyl alcohol, coupled with the cellophane separator system virtually eliminated the problem of silver migration. Failure was eventually caused by solution and precipitation of the negative material until the separator was either punctured or bypassed.

4.2.1.4 Float Tests

Pack 811-21 to 25 was floated in a fully charged condition at an average voltage level of 1.87 volts/cell for 7 months. Following the float period, the pack was put on a 7-hour cycle at a 20 percent DOD. Figure 4-6 shows the results of several capacity discharges of this pack.
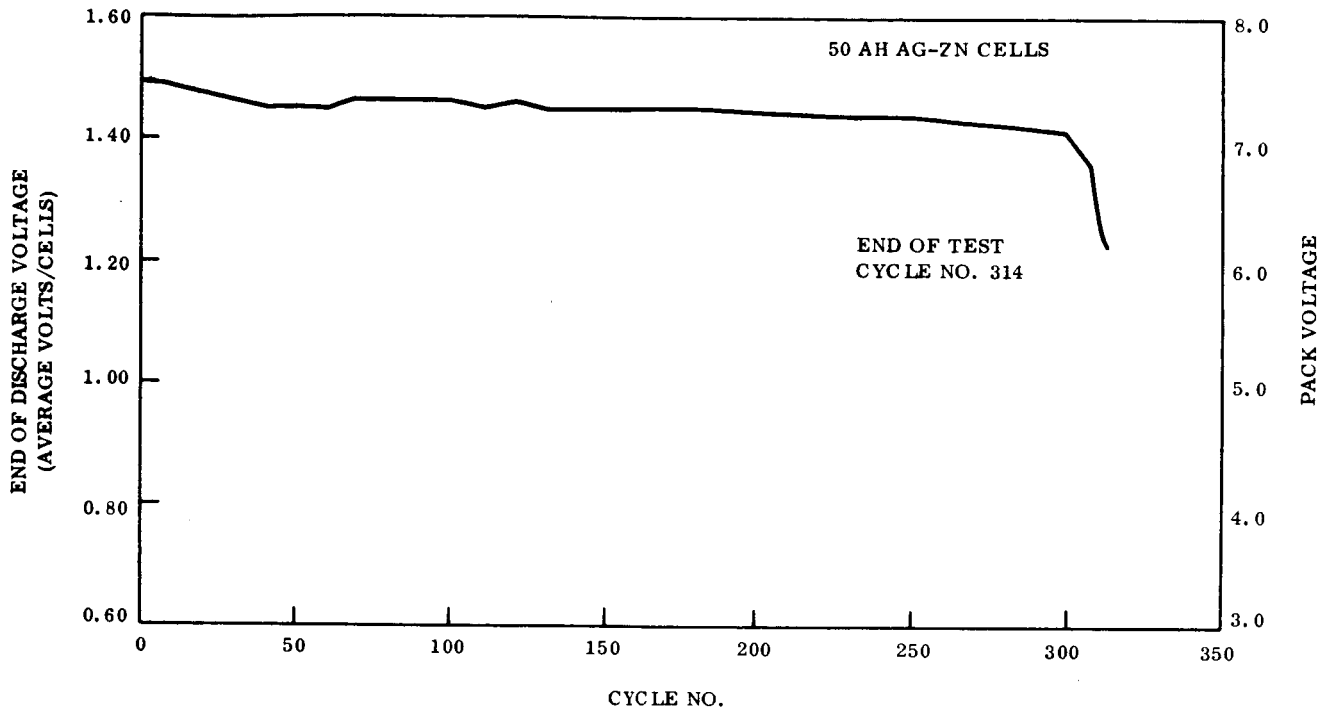
Figure 4-4. End Discharge Voltage Versus Cycle, 20 Percent DOD, 7-Hour Cycle
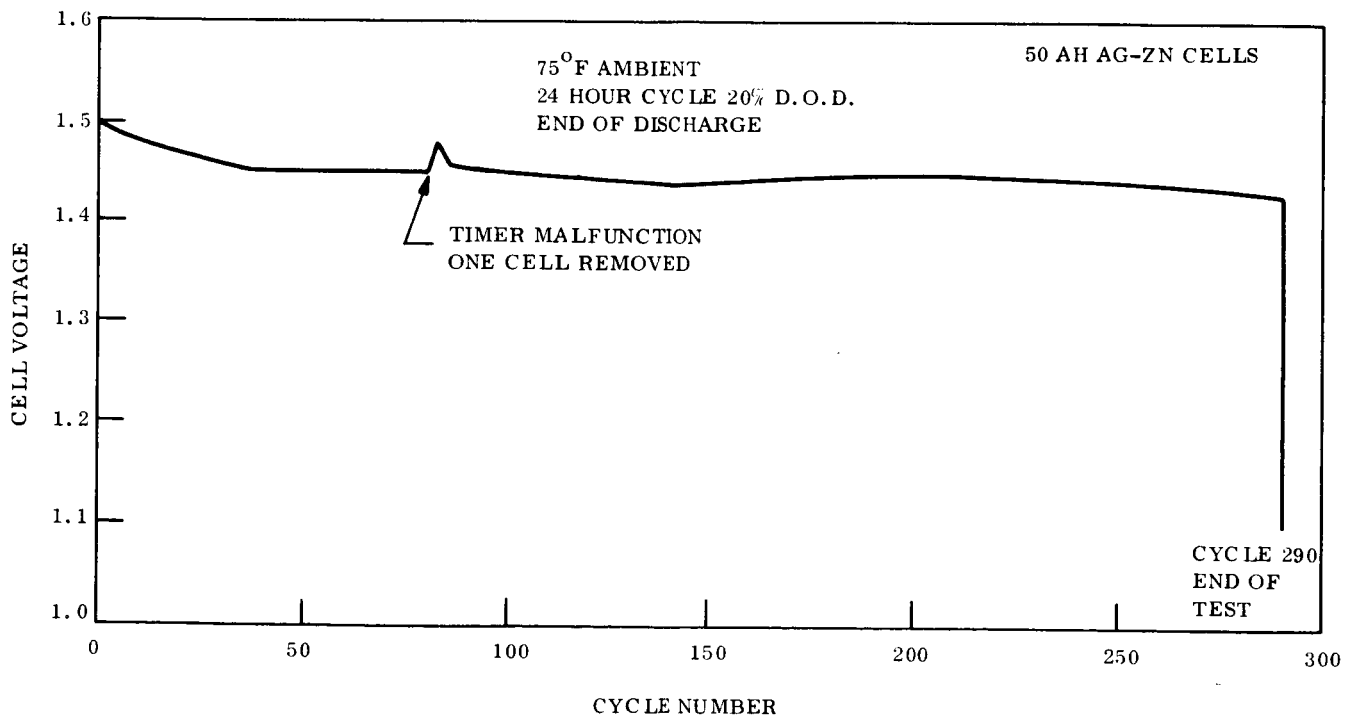
Figure 4-5. Pack 811-26 to 30, 5-50 AH Ag-Zn Cells
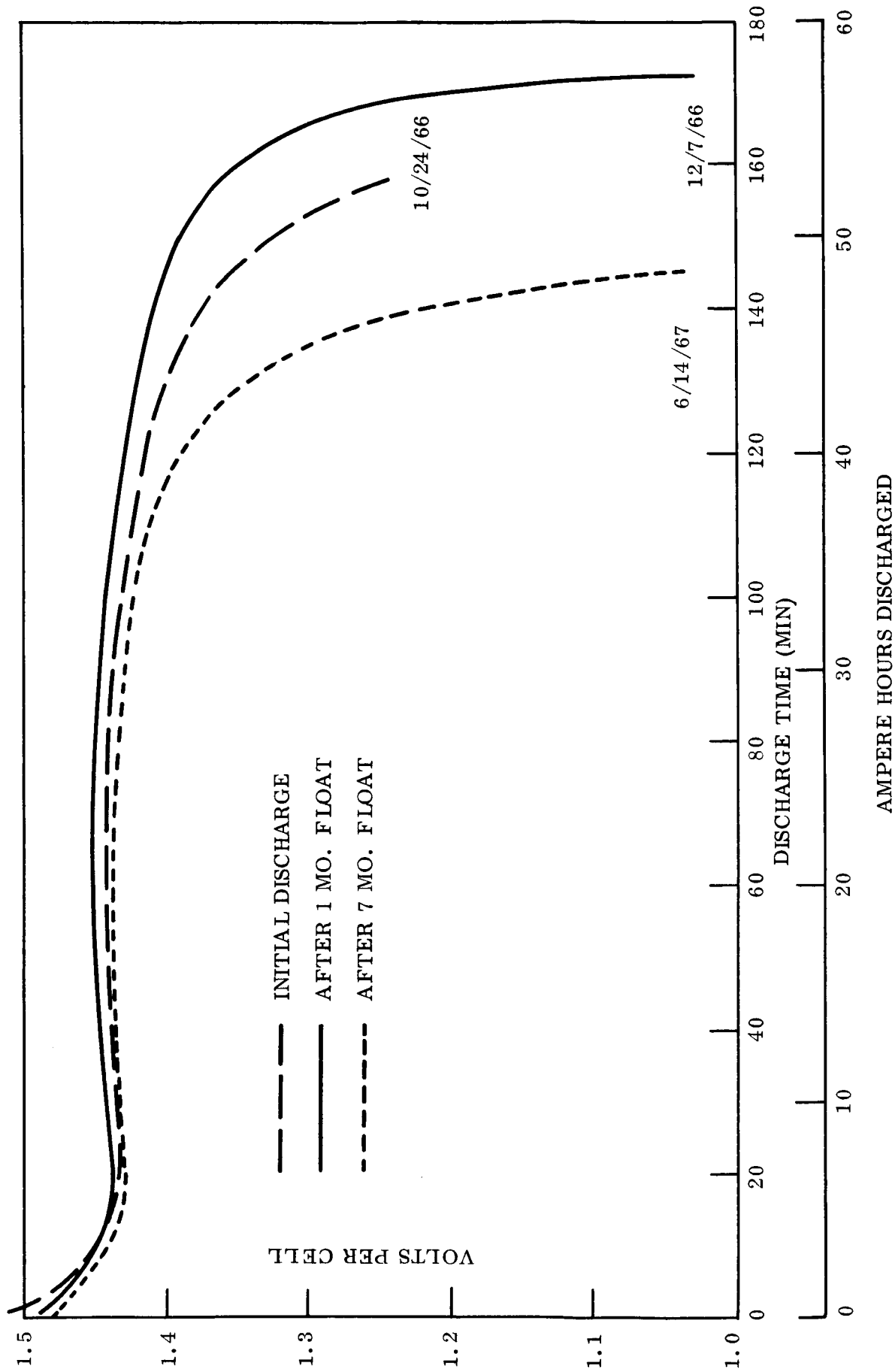
Figure 4-6. Silver-Zinc Secondary Cells Discharge Volts Versus Time for 20 Amp Discharge

It may be seen that the total capacity of the pack was not appreciably degraded; however, when placed on cycle test the pack failed after only 169 20-percent DOD cycles as compared to 314 cycles for a pack which had not undergone the float period. Upon inspection of the failed cells it was observed that the PVA separator had degraded considerably and this was believed to be the reason for the decreased cycle life.

Additional packs are now in the float portion of other float/cycle tests to determine if lower depths of discharge can be sustained for longer time periods and to see if a 30°F environment causes a significant change in operation.

4.2.2 SILVER-CADMIUM CELLS

The silver-cadmium cells have a nominal capacity of 20 ampere-hours and are assembled in 302 stainless steel cans. Each cell has two ceramic bushings, insulating the negative and positive terminals from the case. Each cell measures 3-7/16 inches high by 3-3/16 inches wide by 1-7/16 inches in thickness and weighs 1.5 pounds, exclusive of the pressure gage. The 154 square inches of silver oxide is contained on 12 plates while 13 plates contain the negative cadmium material. Separation consists of two layers of polyvinyl alcohol and four layers of cellophane. The electrolyte, in all cases but one, consists of 93 cc of 30 percent KOH. Pack 812-F contains 80 cc of 40 percent KOH.

Cells were tested in packs of six to determine charge and discharge characteristics and cycling capability on 7- and 24-hour charge/discharge cycles. In addition, one pack was placed on float to determine cycling capability after an extended period of floating in a fully charged condition. A summary of the silver cadmium tests is shown in Table 4-2.

4.2.2.1 Charge Tests

Charge tests, similar to tests carried out on the silver-zinc cells, were also performed on the silver-cadmium cells. Voltage levels of 1.48, 1.50 and 1.52 volts/cell average were used, recharging from 60, 40, and 20 percent depth of discharge. A 3.0 amp maximum rate was used in all cases. All of the charge tests on the silver-cadmium cells were conducted at

room ambient, about 75°F. Data was obtained similar to that obtained for the silver-zinc cells. It was determined that 1.48 volts/cell was too low for efficient charging, but that 1.50 or 1.52 volts/cell would be satisfactory under certain conditions, if the depth of discharge is not too great. Under certain conditions (pack 812-F) 1.54 volts/cell was used satisfactorily, but usually this voltage level resulted in severe unbalancing during charging with the result that gassing occurred in some cells in the test pack.

4.2.2.2 Discharge Tests

Silver-cadmium cells were discharged at 40, 75, and 90°F to generate typical V/I curves. The results are shown in Figure 4-7 where data is plotted for rates of 1 to 20 amps.

4.2.2.3 Cycle Tests

Packs were put on 24-hour cycles at 60 and 40 percent DOD and on 7-hour cycles at 40 and 20 percent DOD. Results of these tests are summarized in Table 4-2. No correlation of cycle life with depth of discharge or cycle period is possible, however, cycle life was disappointingly poor except for pack 812-F.
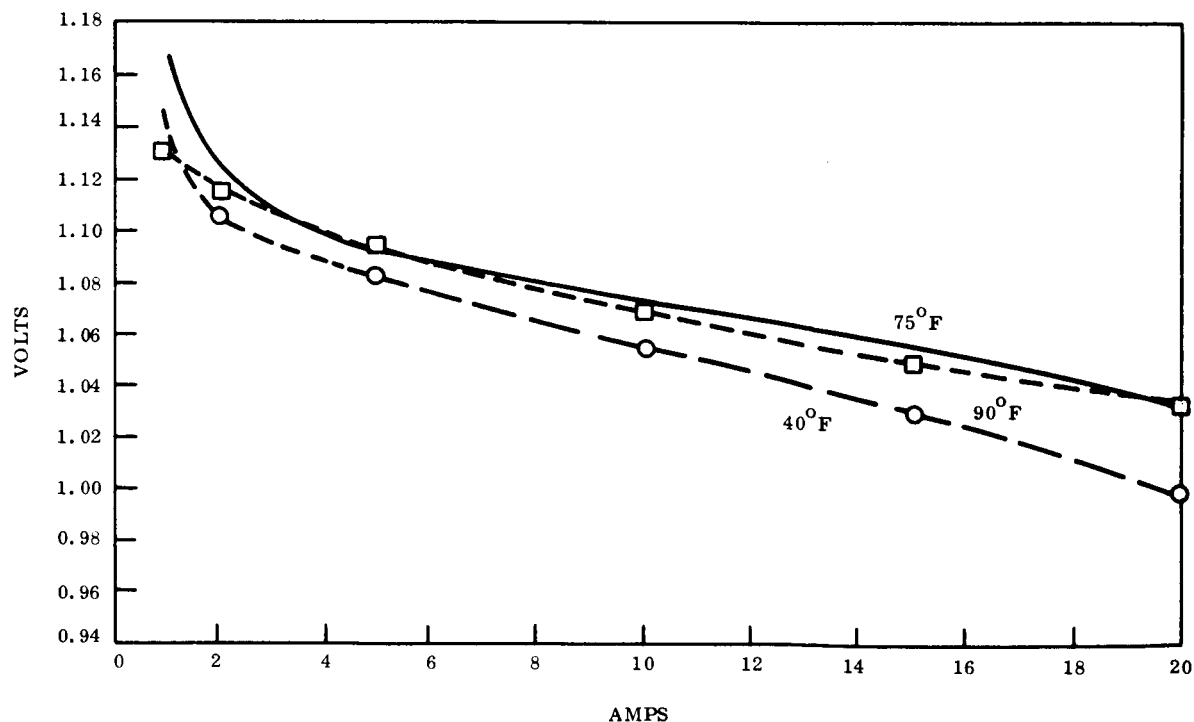
Figure 4-7. Volts Versus Discharge Rate for 20 AH Silver-Cadmium Sealed Cells

4-10

Table 4-2. AG-CD Test Summary

Pack No.	Months Test 1 2 3 4 5 6 7 8 9 10 11	Cycles To Failure
A	Charge Tests — 7 Mo Float — ✗ 7 Hr Cycle 20% DOD	97
B	✗ 7 Hr Cycle, 40% DOD	285
C	✗ 24 Hr Cycle, 60% DOD	126
D	✗ 24 Hr Cycle, 40% DOD	135
E	✗ 7 Hr Cycle, 20% DOD	705
*F	7 Hr Cycle 40% DOD 40% KOH, 2 Step Change	> 1000

* Test Continuing

Considering that the nominal energy density is only about 14 watt-hours per pound, these cells would not be competitive with nickel-cadmium cells unless a definite magnetic cleanliness requirement existed.

All silver-cadmium cells failed by a low end-of-discharge voltage phenomenon. When the end-of-charge voltage was increased to increase the charge input, cell unbalancing occurred resulting in gas generation in some of the cells. Failure analysis showed no signs of internal shorting or silver migration. From this it was deduced that failure was caused by negative plate fading or passivation. This phenomena was discussed with the manufacturer who concurred in the explanation, because the negative plate was of pasted construction rather than impregnated on a sintered nickel substrate.

Pack 812-F behaved quite differently and has exceeded 1000 cycles at a 40 percent DOD on a 7-hour cycle. Figure 4-8 shows end-of-discharge voltage versus cycle number. The reason
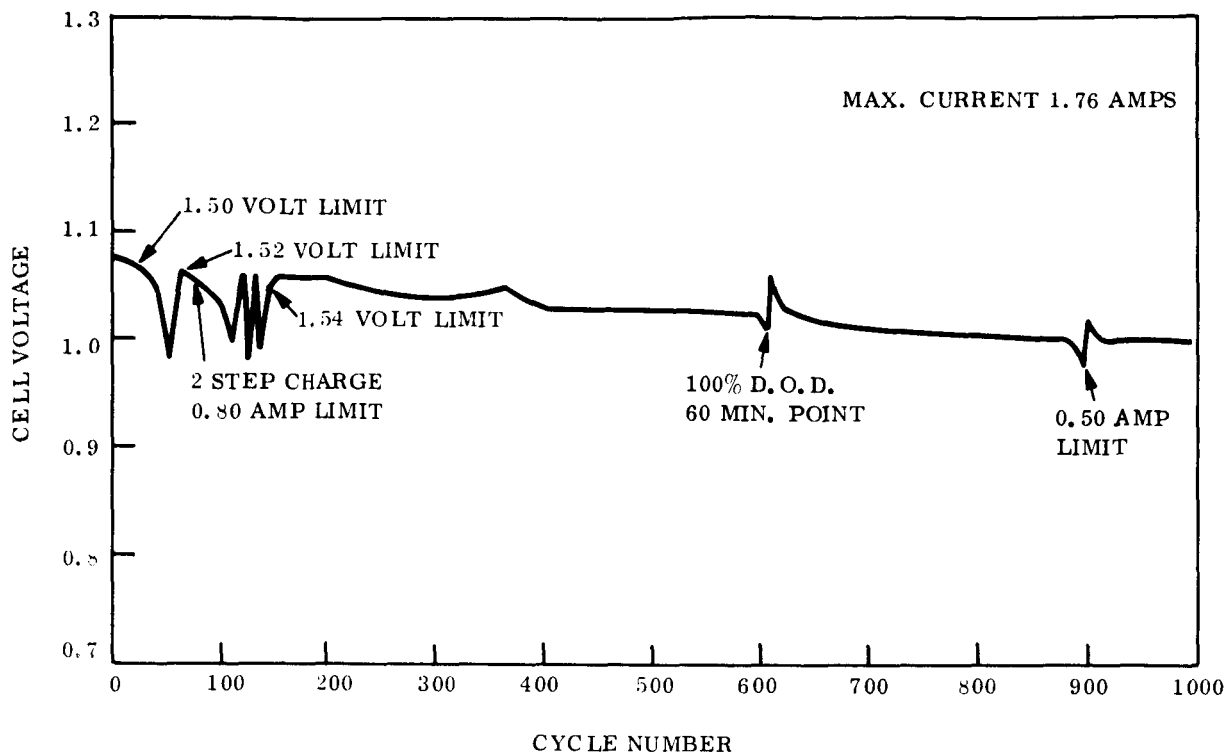
Figure 4-8. Pack 812-F 6 20 AH Ag-Cd Cells 7-Hr Cycle, 40 Percent DOD, 75°F End-of-Discharge

for this improved operation can be explained by any one of three unique factors existing for this pack:

a. By an extremely fortunate set of circumstances, six well-balanced cells were selected that can be operated at a charge voltage equivalent to 1.54 volts per cell without becoming unbalanced and generating gas.

b. The inception of a two-step voltage limit causes the charge voltage to drop to a safe value before unbalancing occurs. Operation in this mode is illustrated by Figure 4-9, where the upper voltage level of 1.54 volts per cell is maintained until the charge current decays to 0.21 amp. At this point the cell voltage is reduced to an average of 1.42 volts/cell, just above the open circuit voltage.

c. The cells were filled with 40 percent KOH rather than 30 percent KOH electrolyte, resulting in less severe fading and degradation.

4-12
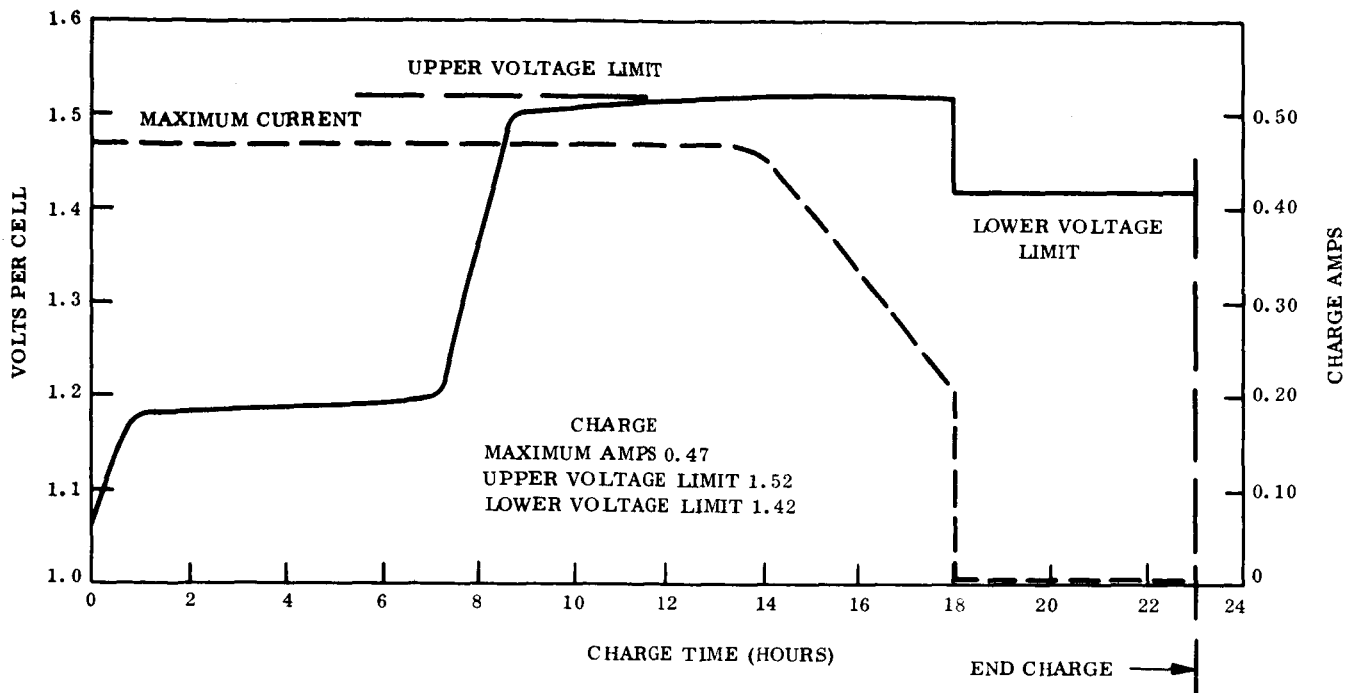
Figure 4-9. Silver-Cadmium Cell Pack 8-2-D Cycle 109, 40 Percent DOD, 24-Hr Cycle

4.2.2.4 Float Tests

One pack was placed on a 7-month float at 1.42 volts/cell and then cycled at a 20 percent depth of discharge on a 7-hour cycle. The pack survived only 97 cycles before failure occurred as a result of the inability to accept a charge. It was concluded that this cell is severely penalized by long periods on float charge and would not be satisfactory for a Mariner-type mission.

No additional silver-cadmium cells were placed on float test, but it was decided that the use of 40 percent KOH electrolyte for silver-cadmium cells did warrant further investigation.

4.2.3 NICKEL CADMIUM CELLS

4.2.3.1 Standard Nickel Cadmium Cells

The Space Systems Organization has carried out a considerable amount of testing with hermetically-sealed nickel-cadmium cells. Batteries have been tested in thermal-vacuum chambers to determine thermal characteristics, on 5-hour and synchronous orbit-type cycles to determine cycle life capability, and on continuous overcharge tests.

Cells used for the latter tests were 11 to 12 ampere-hour cells, purchased in late 1961, which were placed on a continuous charge for over 500 days at a $C/7$ rate and following a capacity discharge, when they delivered over 12 ampere hours of capacity, were put in storage in the laboratory for over two years. They were subsequently removed from storage, given a few conditioning cycles, and placed on a continuous 24-hour cycle, discharging to a 60 percent DOD. These cells have completed over 500 cycles and are still operating satisfactorily.

4.2.3.2 Third Electrode Nickel-Cadmium Cells

A relatively new method in battery charge controls employs the use of a third or auxiliary electrode to signal when a cell has reached full charge. Using this method, a nickel-cadmium battery may be recharged at a rapid rate, and reduced to a safe trickle rate when the charge has been completed. Several 20 ampere-hour cells containing third electrodes have been procured for evaluation. It is expected that they will be tested at several charge rates and temperatures to determine the effect of these parameters on the third electrode signal and the charge acceptance of the cells.

An overall comparison of silver-zinc, silver-cadmium cycle-life capability as a function of depth of discharge is shown in Figure 4-10.
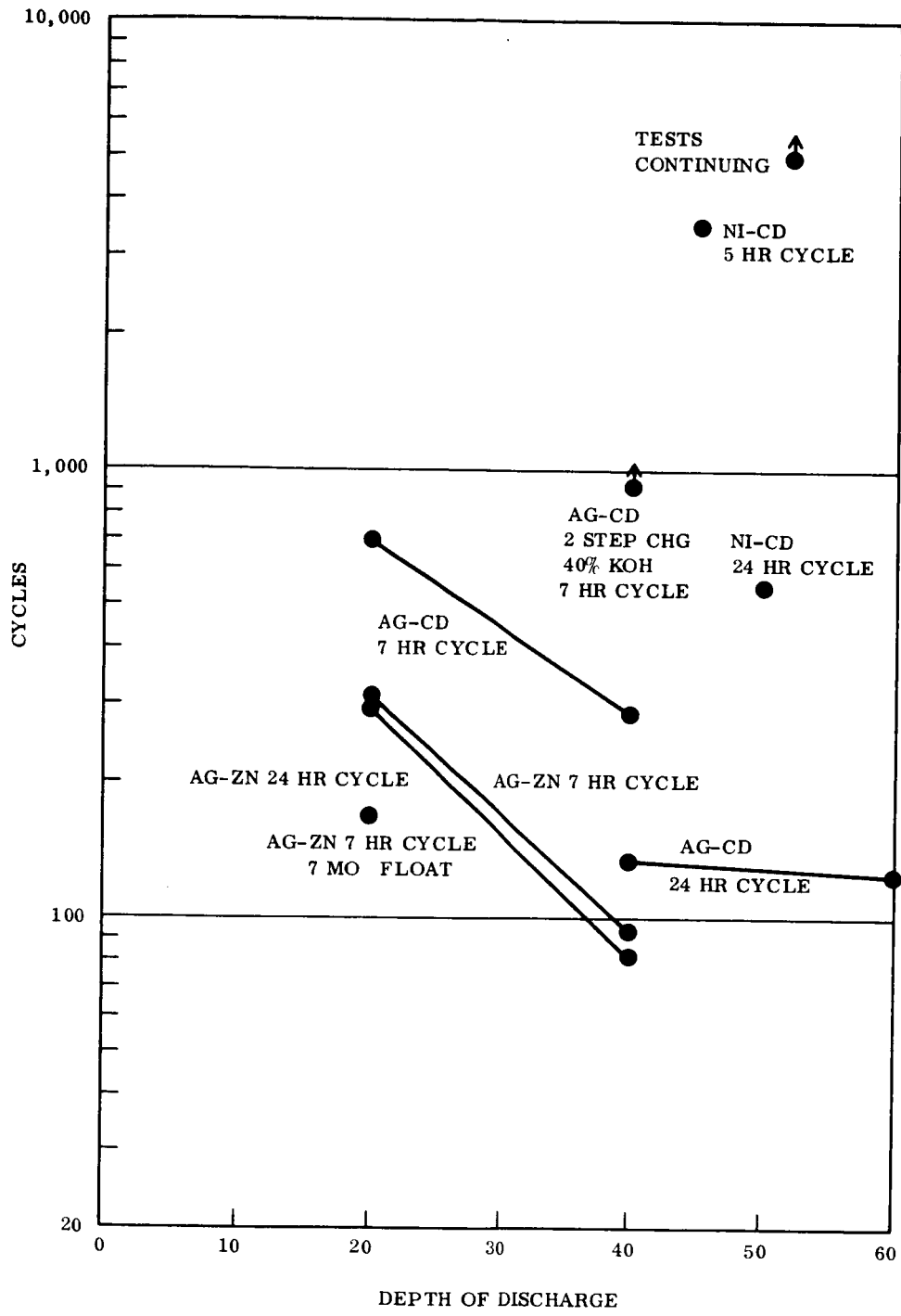
Figure 4-10. Cycle Life Versus DOD for Ag-Zn, Ag-Cd, and Ni-Cd Cells at 25°C

SECTION 5

RELIABILITY SENSITIVITY STUDIES

5.1 APPROACH

It is very difficult to accurately predict or calculate the reliability of various piece parts, subunits of a blackbox or the complete blackbox, because of uncertainties in reliability data and shortcomings in reliability modeling techniques. Consequently, the approach taken on this study is to perform selected sensitivity studies in a parametric fashion to illuminate key questions concerning the operation of the subsystem elements.

Utilizing parametric sensitivity studies we can plot results, for specific points to be analyzed, for the full range of reliability from 0 to 1, and then we can assess the relative importance of various questions, even though we do not know with any confidence the actual hardware reliabilities of the various elements. By way of illustrating this approach, and how the results of such studies can provide insight into certain fundamental questions, the first two examples, discussed separately in the following section, consider the cases of two series elements and two parallel elements. These examples, as well as the remainder of the analysis in this section, have been studied with the use of the remote access time sharing computer system.

5.2 SERIES EXAMPLE

Figure 5-1 shows the block diagram being analyzed. R_π represents the reliability of one black box and R_N represents the reliability of the second black box. For the system to work both black boxes must work; hence, the series diagram. R_s is the reliability of the system and is:

$$R_s = R_\pi \times R_N \qquad\qquad (5-1)$$

Figure 5-2 is a plot of the system reliability, R_s, versus the reliability of the first black box, R_π. The parameter represents the reliability of the second black box, R_N.

Figure 5-1. Series Block Diagram

Figure 5-2. Series System Reliability

5.2.1 CONCLUSIONS

Several general conclusions concerning a series system can be seen from examination of Figure 5-2 and Equation 5-1.

a. R_π and R_N are interchangeable; consequently any statement made about one black box equally applies to the other.

b. The system reliability never exceeds the reliability of the lower element.

c. The system reliability improves linearly with improvement of the lowest element until the lowest element is nearly as reliable as the highest element.

d. Once the most reliable element is about any order of magnitude better than the lowest element, no significant system improvement follows from further improvement of the highest element.

e. R_π and/or R_N can represent the reliability of a single black box or the reliability of several black boxes in series.

f. From b and c, above, it follows that to improve the system, effort should be concentrated on improving the least reliable element.

5.3 PARALLEL EXAMPLE

Figure 5-3 shows the block diagram being analyzed. R_π represents the reliability of one black box and R_N represents the reliability of a second black box. The system works successfully if either black box works, hence the parallel diagram. R_s is the reliability of the system and is:

$$R_s = R_\pi + R_N - R_\pi R_N \tag{5-2}$$

Figure 5-4 is a plot of the system reliability, R_s, versus the reliability of one black box, R_π. The parameter represents the reliability of the second black box, R_N.
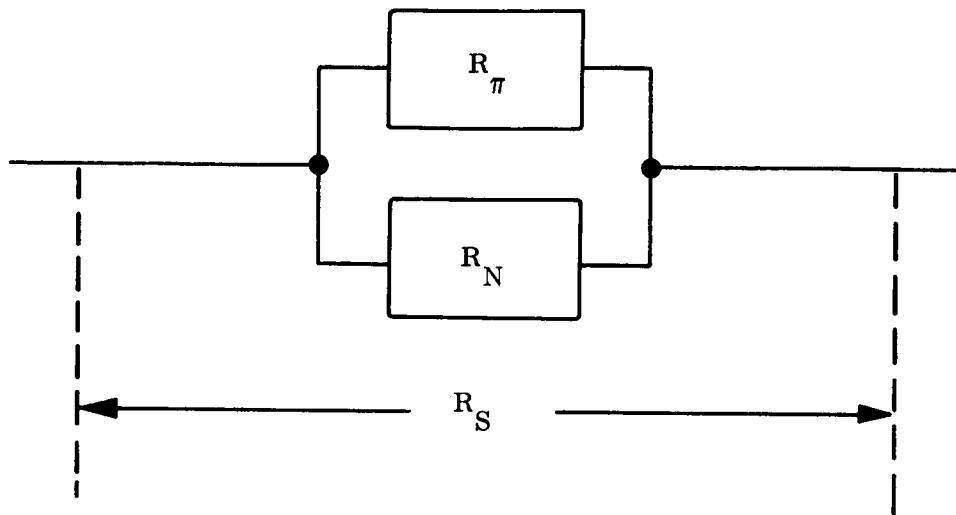
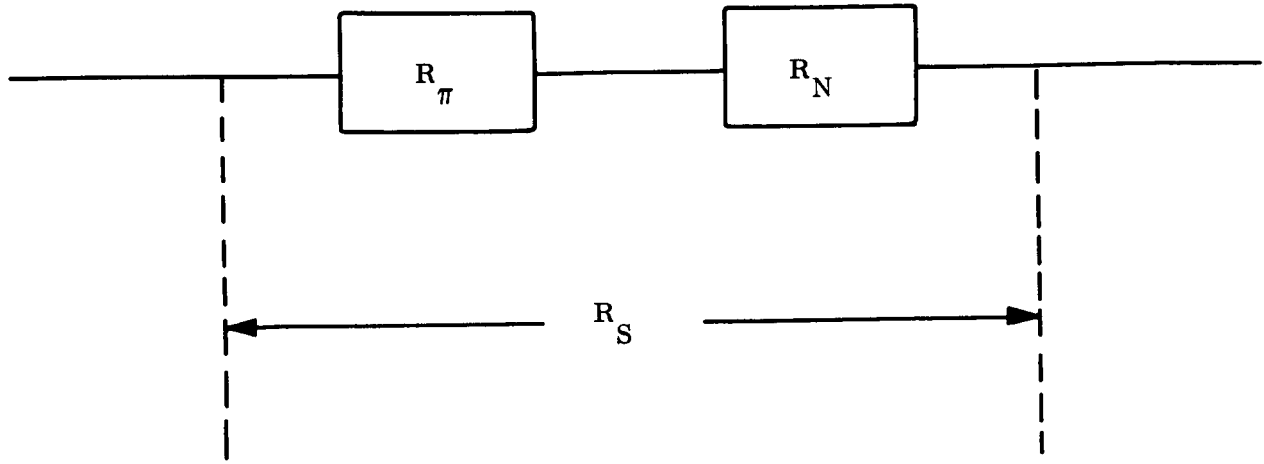Figure 5-3. Parallel Block Diagram

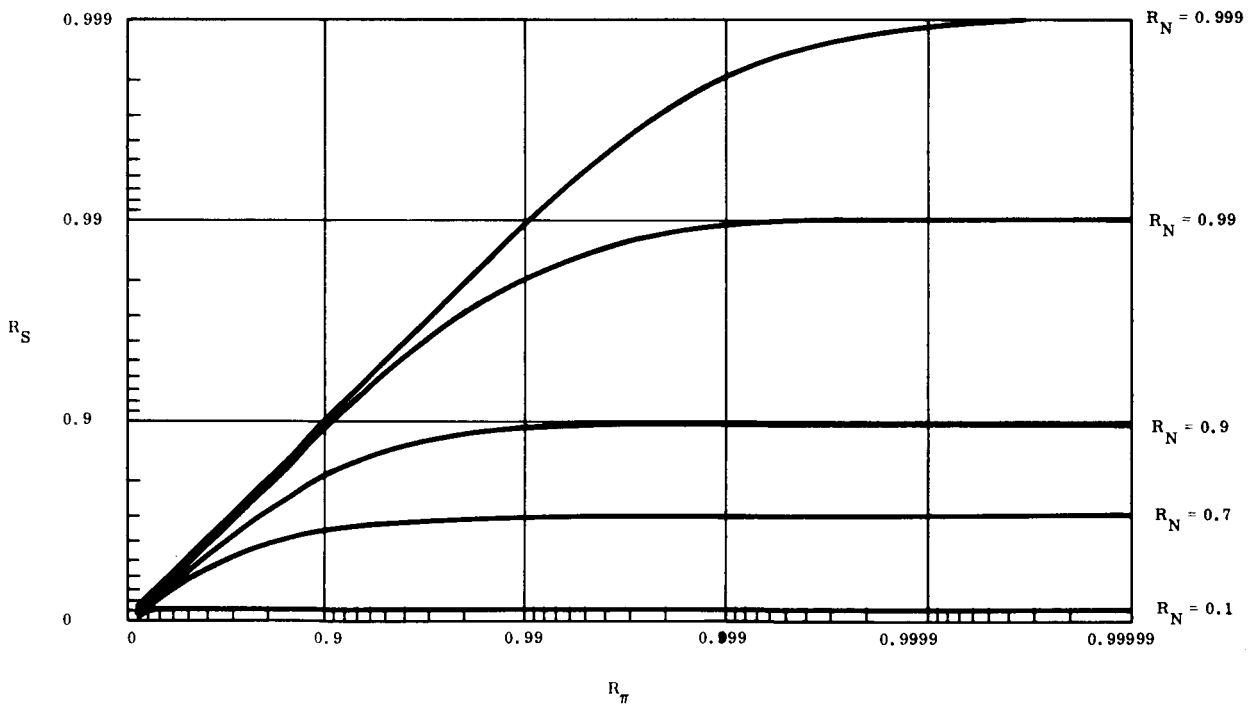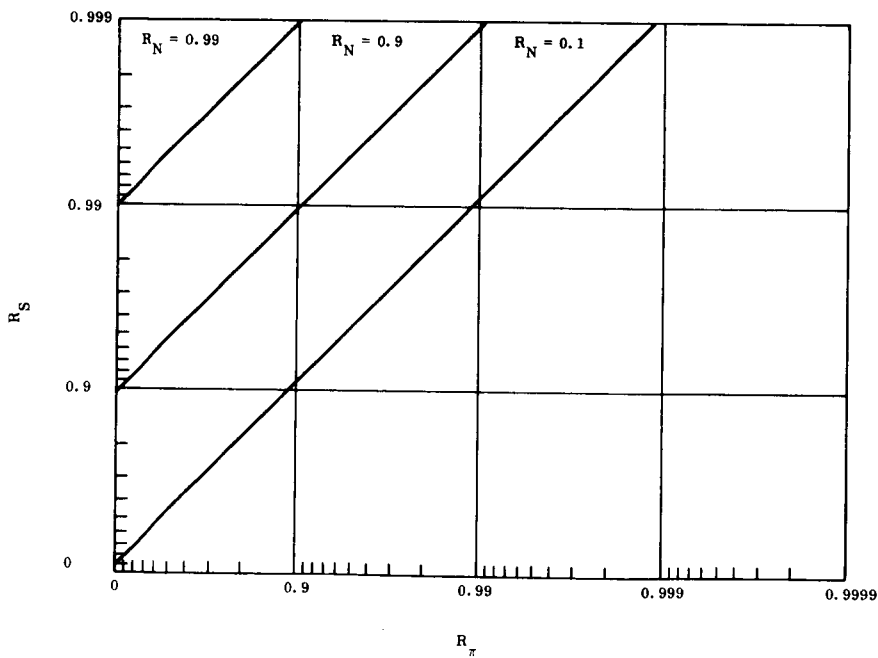Figure 5-4. Parallel System Reliability

5.3.1 CONCLUSIONS

Several general conclusions concerning a parallel system can be seen from Figure 5-4.

a. R_π and R_N are interchangeable, consequently any statement made about one black box equally applies to the other.

b. The system reliability always exceeds the reliability of the highest element.

c. The system reliability improves with improvement of either element.

d. The system reliability always improves with improvement of either element reliability: no matter what the relative reliabilities are.

e. R_π and/or R_N can represent the reliability of a single black box or the reliability of several black boxes in series.

f. From b, c and d, it follows that to improve the system, effort can be applied to either element; hence, which element is easiest to improve would become the main criteria.

5.4 FAULT SENSING AND SWITCHING

One of the major areas of interest on this study is the subject of switched redundancy for regulators and inverters. The use of a standby regulator and/or inverter in conjunction with a fault detection and switching system always raises the question of whether the system reliability might not have actually been degraded by the additional fault sensing complexity. The following sections describe studies aimed at illuminating this general question.

5.4.1 COLD VERSUS HOT REDUNDANCY

Standby redundancy can be implemented in two ways:

a. Hot redundancy where the standby unit is always turned on

b. Cold redundancy where the standby unit is not turned on until the main unit has failed.

Presumably cold redundancy would be the most reliable since the standby unit is not on until the main unit fails, hence, its operating life is shorter. The following analysis sheds some light on this specific question as well as the general subject of fault sensing and switching of a redundant element.

Figure 5-5, Part A, shows the basic circuit being analyzed, and Figure 5-5, Part B, the corresponding block diagram used to assess the system reliability.

R_R and R_I represent the reliabilities of the regulator and inverter, respectively. The A, B, and C blocks represent the reliability of the fault sensing and switching. The failure modes which are incorporated in the A, B, and C blocks are listed below:

<u>A</u>	<u>B</u>	<u>C</u>
• Open top relay contacts	• Pole of relays open	• Open relay coil
		• Welded top contacts
• False detection and switching	• Pole side relay connections open	• Fault sensor fails to detect failure and/or switchover
		• Bottom contact open

For the hot redundancy situation the total system reliability is:

$$R_s = [1 - (1 - R_R R_I R_A)(1 - R_R R_I R_C)] R_B \qquad (5\text{-}3)$$

For the cold redundancy situation the total system reliability is:

$$R_s = e^{-(\alpha + \lambda_\beta) T} + \frac{\alpha}{\beta - \alpha} e^{-(\beta + \lambda_\beta) T} \left[e^{-(\alpha - \beta) T} - 1 \right] \qquad (5\text{-}4)^*$$

---

* This equation assumes: (1) the A block must work from the beginning of the mission until a switchover to the redundant string occurs, (2) the B block must work for the entire mission, and, (3) the C block must work from the time the standby chain is first used until the end of the mission. Actually most of the C block items must work only until a switchover to the standby chain occurs. This analysis was checked and the numerical results are essentially the same for either time of operation of the C block.
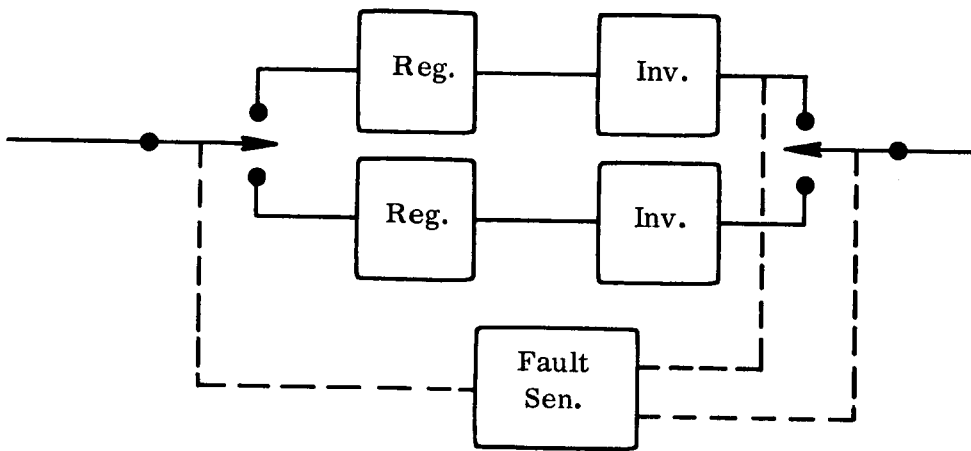
A
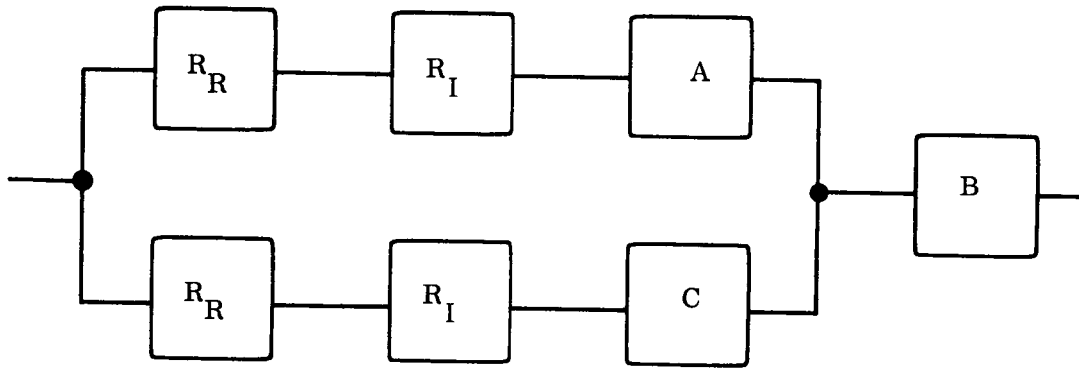
B

Figure 5-5. Paired Regulator Inverter

where:

$$\alpha = \lambda_R + \lambda_I + \lambda_A ,$$

$$\beta = \lambda_R + \lambda_I + \lambda_C ,$$

λ_i = the failure rate of the ith component,

T = mission time

all reliability functions are assumed to be exponential functions.

5.4.1.1 Conclusions

Figure 5-6, shows the system reliability, R_s, versus the "C" reliability, R_c, with "A" as a parameter, R_A. Figure 5-6, Part A, is for the case where we have poor black boxes whose reliabilities are $R_R = R_I = 0.9$. Figure 5-6, Part B, is for better boxes where $R_R = R_I = 0.99$. And Figure 5-6, Part C, is for very reliable black boxes where $R_R = R_I = 0.999$. The single string reliability for just the regulator and inverter is shown as a horizontal line in this illustration.

Since "B" is in series with the whole system, its reliability is very important to the problem (see Section 5.2) and must obviously be kept very high. For the following studies it is assumed perfect, hence, $R_B = 1.0$.

The following conclusions are drawn from Figure 5-6:

    a.   The redundant system is always more reliable than the single string system if the fault sensing reliability, R_A and R_C, is equal to or higher than the black box reliability, R_R and R_I.

    b.   The failure modes of the fault sensing system included in "A" are frequently ignored in many analyses, and their importance is seen to be very significant.

    c.   There are many values of fault sensing reliability, R_A and R_C, which cause the redundant system to be less reliable than the single string system.
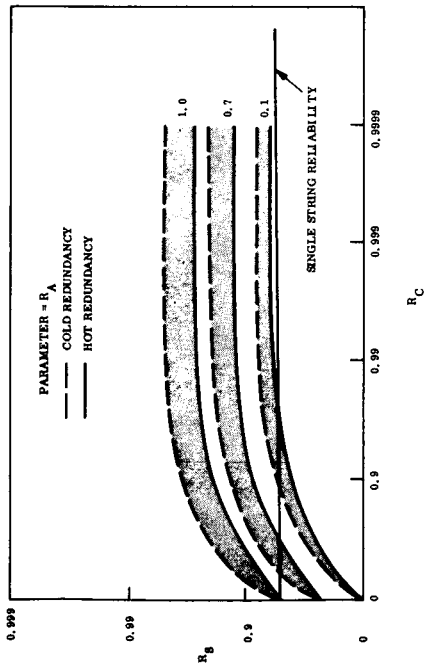
PART C. $R_R = R_I = 0.999$

PART A. $R_R = R_I = 0.9$
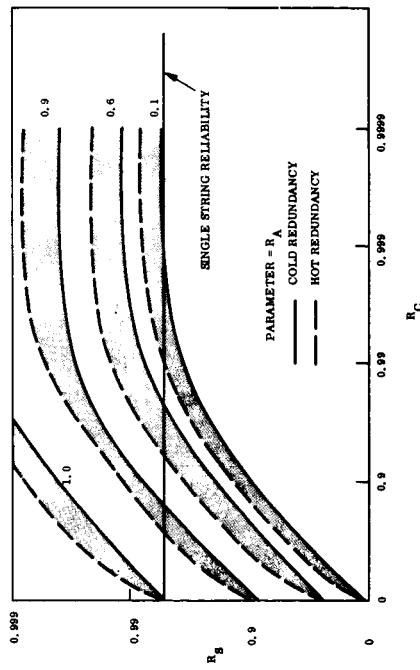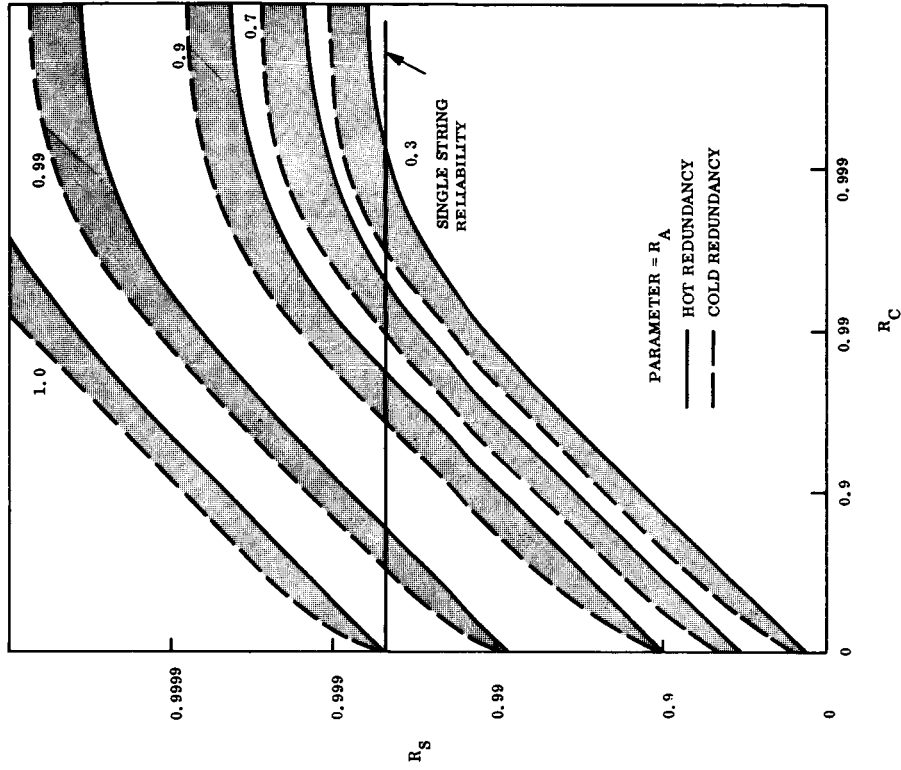
PART B. $R_R = R_I = 0.99$

Figure 5-6. Cold Redundancy versus Hot Redundancy

d. The improvement in system reliability for the cold case over the hot case is real, but not of large significance. The reliability of actual hardware for a cold system would be somewhere inbetween the hot and cold cases (the shaded region) since the hardware would be degrading to some extent even in the off condition, e.g. radiation damage to semiconductors.

e. Based on a, above, and Section 5.2.1, it is extremely important in implementing a switched redundancy system to assure that R_A and R_C are at least equal to R_R and R_I and that R_B is very high.

5.4.2 SPLIT STRING VS PAIRED SWITCHING

The regulator/inverter pair analyzed in the previous section could have been implemented in a split fashion such that if either the main regulator or the main inverter failed it would be switched out and the standby unit switched in and, then, when the remaining main unit failed its standby unit would be switched in. Figure 5-7, Part A, shows the basic split string being analyzed in this section and Figure 5-7, Part B, shows the corresponding block diagram used to assess the system reliability.

The analysis for this situation is performed on a hot redundancy basis and compared to the data in the previous section for a "paired" regulator and inverter (see Figure 5-5). The total split string system reliability is:

$$R_s = [1 - (1 - R_R R_A)(1 - R_R R_C)][1 - (1 - R_I R_A)(1 - R_I R_C)]R_B \qquad (5-5)$$

where the nomemclature is the same as in the previous sections.

5.4.2.1 Conclusions

Figure 5-8 shows the system reliability, R_s, versus the "C" reliability, R_C, with "A" as a parameter, R_A. The results of this section, the split string case, are shown as well as the paired regulator/inverter results from the previous section. The results are presented for three levels of black box reliability with Figure 5-8, Part A, being the lowest, $R_R = R_I = 0.9$ and Figure 5-8, Part C, being the highest, $R_R = R_I = 0.999$. The single string reliability

5-10
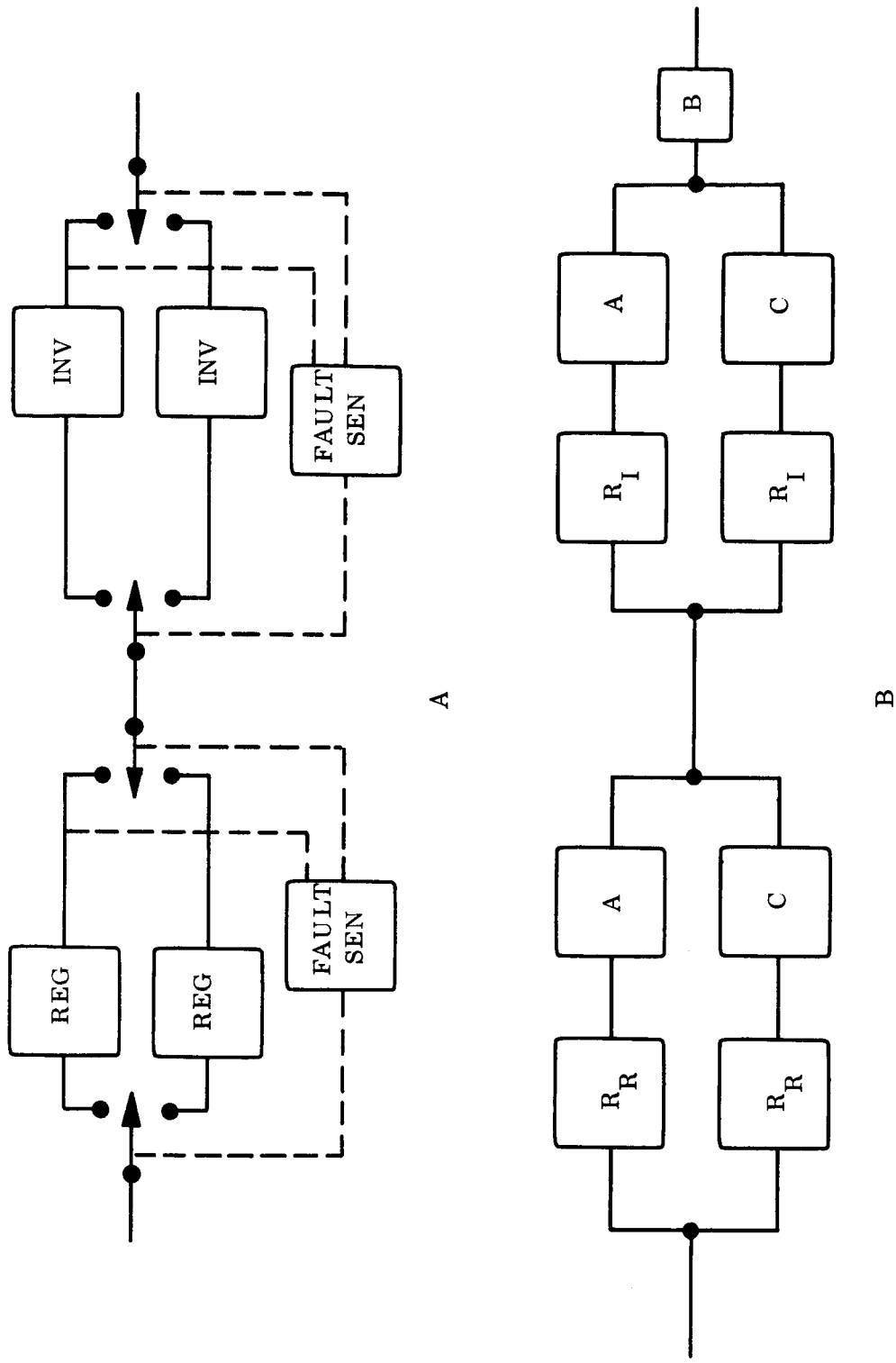
Figure 5-7. Split String Regulator/Inverter
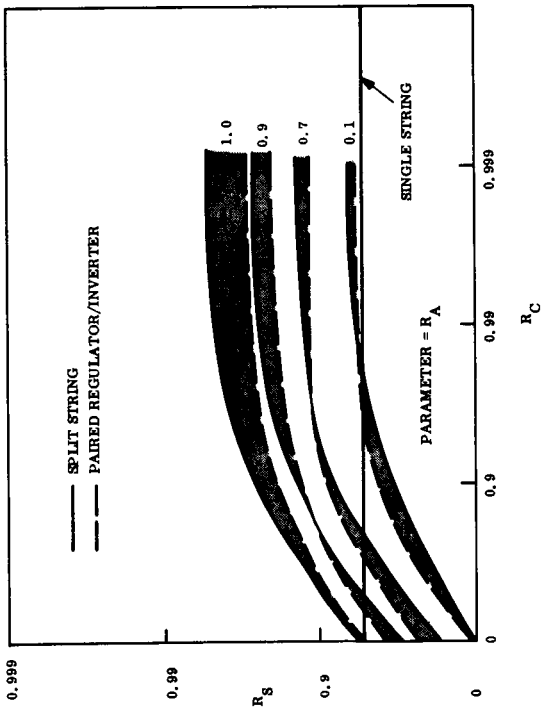
PART C. $R_R = R_I = 0.999$

PART A. $R_R = R_I = 0.9$
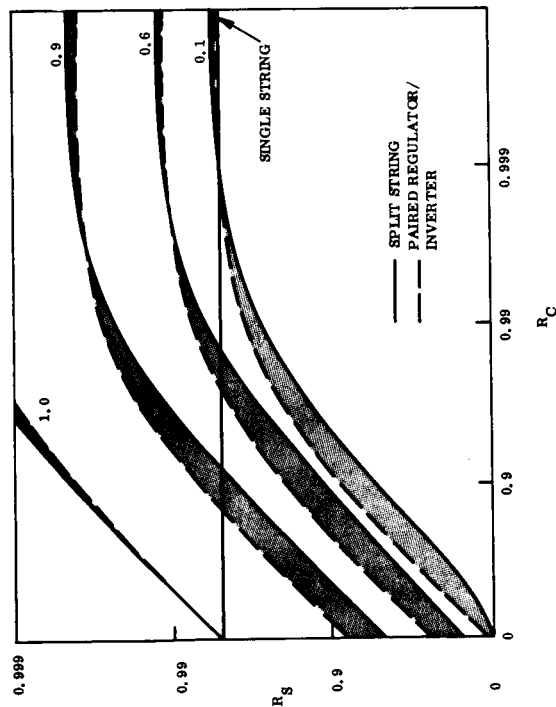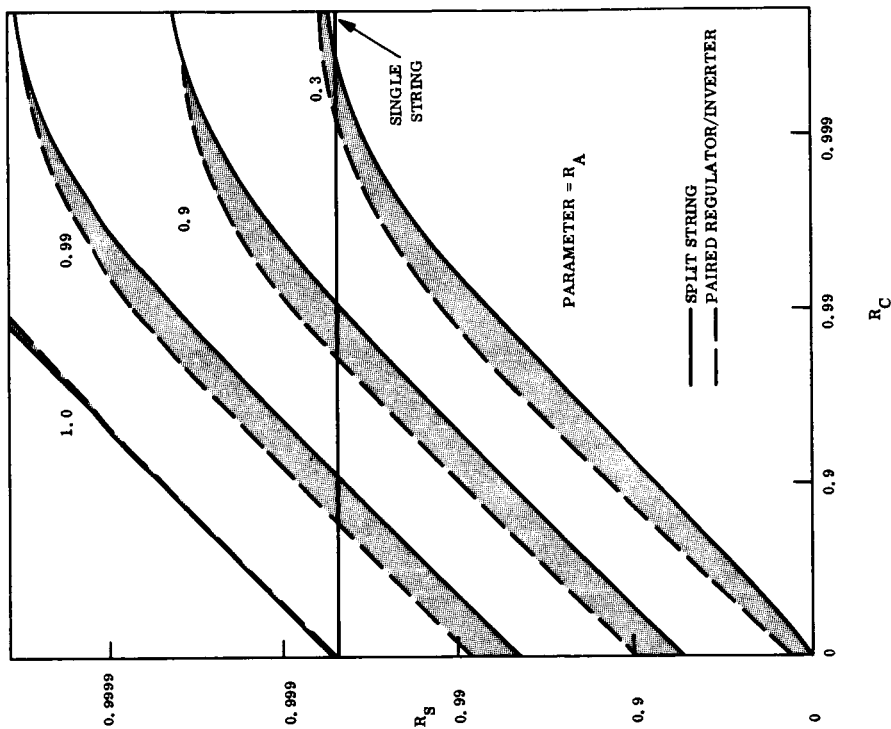
PART B. $R_R = R_I = 0.99$

Figure 5-8. Split String versus Paired Regulator/Inverter

of a single regulator and inverter is shown as a horizontal line. Also, as before, "B" is assumed perfect, hence, $R_B = 1.0$. Of course, the split string case "B" includes portions of an additional relay.

Examination of Figure 5-8 indicates the same general conclusions pertaining to the comparison of a single string system versus a switched redundant system as previously seen and only the specific conclusions from the comparison of the split string versus the paired regulator/inverter are listed below:

a. For low values of fault sensing reliability, R_A and R_c, the "paired" regulator/inverter system is more reliable than the split string approach.

b. For high values of fault sensing reliability, R_A and R_c, the split string system is most reliable.

c. The relative advantage of either system does not appear to be too significant, hence, the dominating consideration in choosing between approaches should be which system is easiest to implement so that the reliability of the "A" and "C" fault sensing hardware is highest.

5.4.3 MARINER MARS 1969 CASE

The Mariner Mars 1969 regulator, inverter, and fault sensing were partially reviewed using the techniques discussed above. The failure rate data for the components were supplied by JPL* and are listed in Table 5-1. The circuit analyzed is shown in Figure 5-9 and the equation used is Equation 5-4. The results, for an assumed mission time of 5700 hours, are shown in Figure 5-10.

5.5 GENERAL CONCLUSIONS/RECOMMENDATIONS

Table 5-2 presents a summary of the main conclusions reached from the reliability sensitivity studies to date.

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* Mariner Mars 1969 Flight Power Subsystem Design Review Report, Power Conditioning Equipment; Electro-Optical Systems Report No. 7178-DRR-002A, 17 April, 1967.
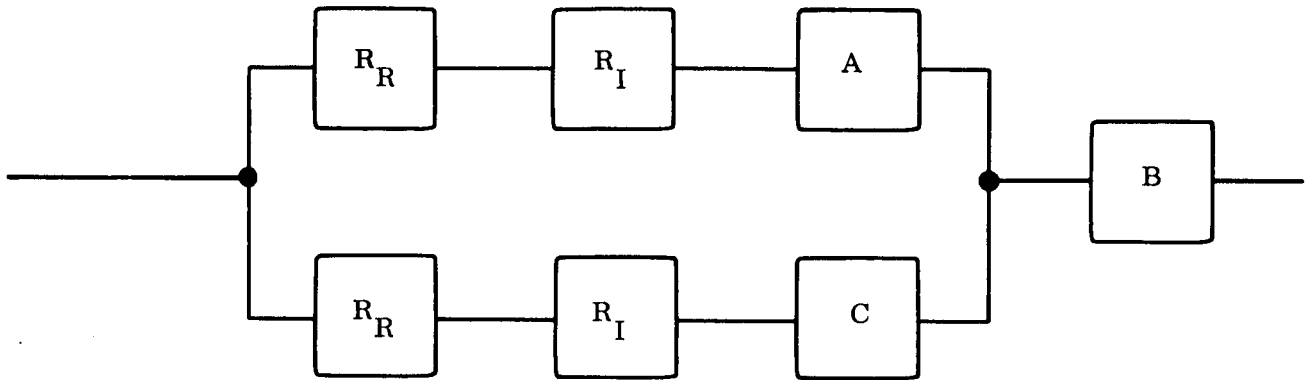
Figure 5-9. Mariner Mars '69 Regulator/Inverter/Fault Sensing
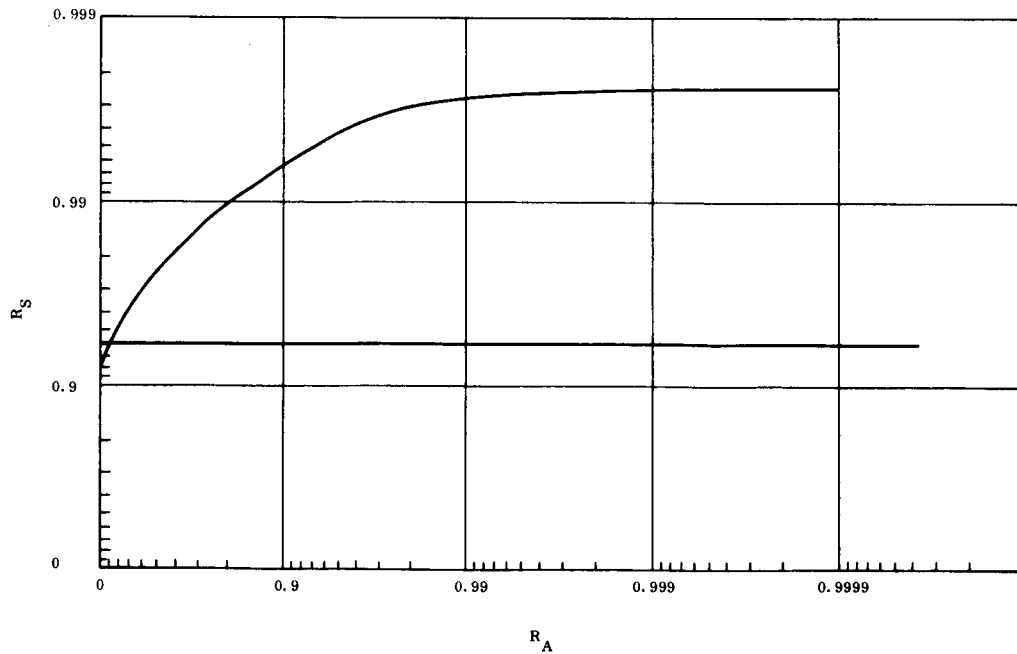
Figure 5-10. Mariner Mars '69 Regulator/Inverter/Fault Sensing

Table 5-1. Mariner Mars '69 Component Failure Rates

Component	Failure Rate (Per 10^6 Hours)	Reliability (Mission Time = 5700 Hours)
Regulator	5.76	0.968
Inverter	4.95	0.972
Failure Sensor, "C"	2.93	0.983
Relay, "B"	0.0085	0.99995

Analysis of the JPL document did not identify anything equivalent to the "A" block used in this study, hence, the reliability was plotted versus R_A. Examination of Figure 5-10 indicates that the redundant system is better than the single string regulator/inverter for any value of $R_A > 0.1$. This is the result we would expect, based on the conclusions of the previous sections, when the components have reliabilities as listed in Table 5-1. The question of how valid the component reliabilities really are is, as pointed out in the introduction to Section 5, very difficult to answer.

The analysis of this section is not completely representative of the actual MM '69 system. Future work on this task, utilizing a more complete model of the MM '69 system, is discussed in Section 10.

Table 5-2. Summary of Main Conclusions

Question	Conclusion	Study Recommendation
In general, is fault sensing and switching of a standby element a good step?	It completely depends on the relative reliability of the main black boxes but as long as the fault sensing is comparable to the black boxes in reliability, then it is well worthwhile.	a. Review carefully the "A" block-which includes: 1. Hardware failures in the fault sensing which cause a false switching to the redundant chain, 2. Design of the level and duration of the fault criteria. If too tight, the system is more prone to false switch to the redundant chain. b. Assure that R_A and R_C, the fault sensing reliabilities, are equal to or greater than R_R and R_I, the regulator and inverter reliabilities.
Is separate fault sensing and switching of regulator and inverter better or worse than for the pair?	It depends: if R_A and R_C are low, no; if R_A and R_C are high, yes.	Relative improvement less than uncertainties of actual values of various elements, hence, other criteria should be used, such as: 1. Which approach is easiest to implement. 2. Which approach provides highest fault sensing reliabilities.
Where should effort be concentrated in overall power system to improve reliability?	For series elements always work on the element which is significantly lower than any other element. For parallel elements work on easiest element to improve.	a. Model MM '69 system and Shunt System- b. Perform sensitivity studies to identify which elements should be further improved.
Is the reliability improvement of cold redundancy over hot redundancy real?	Yes, however, it does not necessarily follow that the improvement is so great that it should always be used. That is, if some good engineering/reliability reason exists for using a hot redundancy situation, it might be worthwhile and should be studied.	Do not "blindly" be constrained by a cold redundancy requirement when designing the power components and subsystem.

SECTION 6

FAULT SENSING CRITERIA

The concept of replacing a faulty power conditioning unit (PCU) with a standby unit implies that measurement of the original unit against a set of performance criteria is necessary. Figure 6-1 shows the functions of a fault detector based on such criteria for transferring operation to the standby unit. This section considers and defines such criteria for representative types of PCU's.

Any particular PCU has a defined functional requirement for a given set of external conditions. For example, a series dissipative voltage regulator is required to deliver power within a specified voltage tolerance providing the input power is available within a certain voltage range and providing the output load is within certain limits. If these external operating conditions are satisfied, the regulator requirements themselves serve as the criteria for proper unit operation. Thus, in the case of the series regulator, the delivery of power within a specified voltage range serves as the fault sensing criterion providing the other external conditions are satisfied. A broader set of criteria must, however, be postulated to cover those situations where the external conditions are not satisfied. The series regulator, for example, cannot be expected to function normally if the input voltage is too low. And yet, the fault sensing criterion established for normal input conditions would have indicated a failed regulator. Thus, the general definition of fault sensing criteria must consider both normal and abnormal external conditions.

There are several ways for attacking this general problem. First, the behavior of a properly functioning PCU can be studied for the entire range of normal and abnormal external conditions, and the results, either analytical or experimental, used to establish fault sensing criteria. Consider again the series regulator. If the input voltage is too low, a properly functioning series regulator will simply produce the input voltage at its output with some deviation depending on the load. By varying the input voltage over its entire abnormal range, the PCU behavior (specifically the output voltage variation), can be mapped for different load
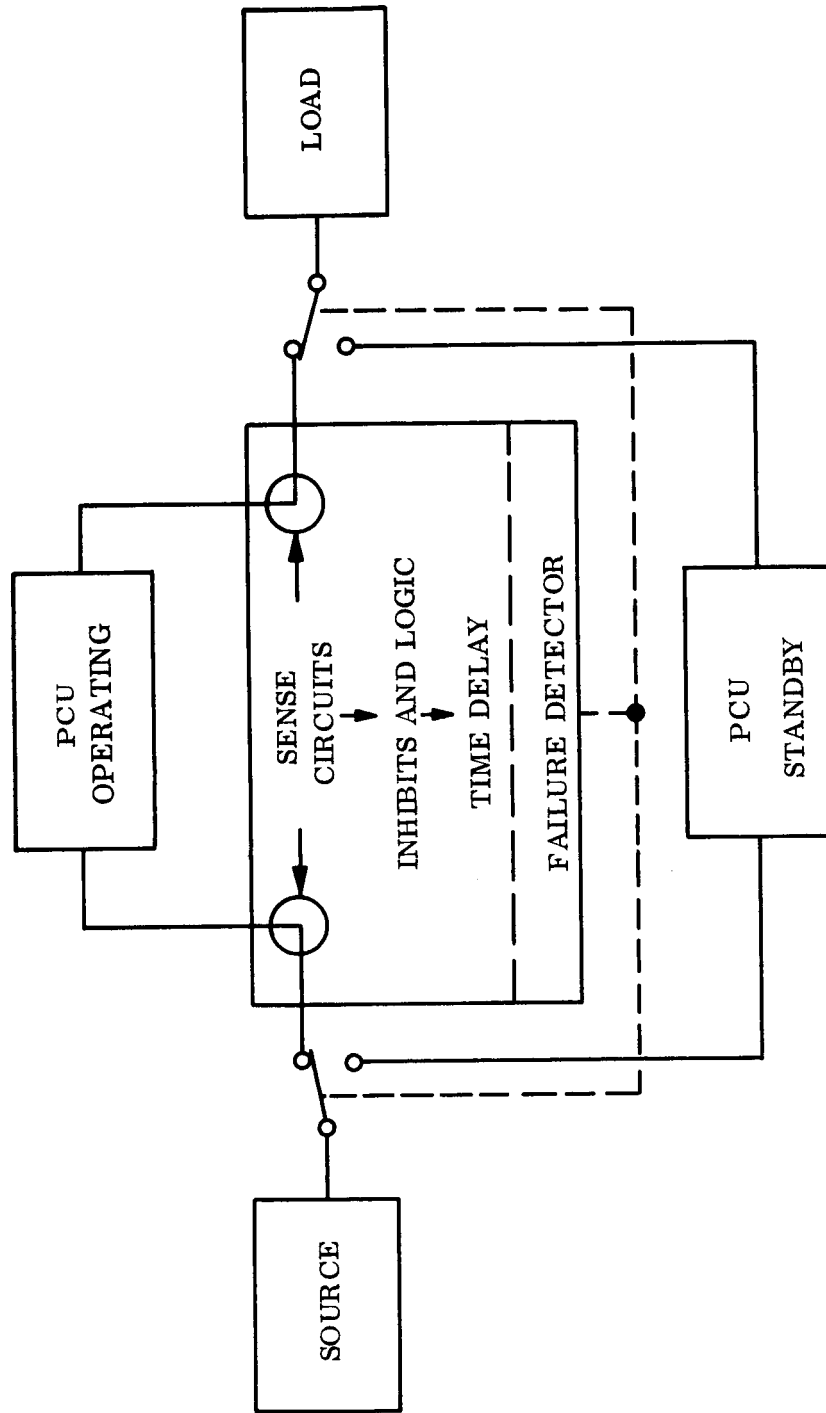
Figure 6-1. System Block Diagram

conditions. The resulting mapping function can be considered as an analog model representative of proper operation of the PCU. Conceptually, this model could serve as the basis for fault sensing criteria, i.e., in an actual mechanization the behavior of the operating PCU would be compared to the analog model. Practically, of course, this approach is difficult to implement. It would probably be complicated because of the implied computer functions, and the mapping function might be difficult to predict, duplicate, and verify.

A second more practical way of considering normal and abnormal external conditions is to recognize the abnormal conditions and avoid comparisons during such periods. For example, if load on a PCU is excessive, its corresponding low output voltage would be ignored as a criterion of failure. The definition of such inhibit functions is not always obvious and must be examined carefully for each PCU type. For example, a low input voltage to the series regulator could have been caused by failure of the regulator and a fault sensing inhibit would not be desirable.

The second approach has been adopted in examining the fault sensing criteria for the following typical PCU's:

a. Series dissipative regulator
b. Inverter or converter
c. Switching regulator (buck, boost, etc.)
d. Shunt regulator

Table 6-1 summarizes the fault sensing criteria and inhibit functions for these PCU's in accordance with the nomenclature shown. As indicated for the first criterion, the table should read as follows: "Failure indicated when $V_o > V_{RMAX}$ except if $V_I > V_{IMAX}$ or $I_o < I_{oMIN}$".

Sections 6.1 to 6.4 provide more detailed discussion on each PCU type.

Table 6-1. Fault Criteria Summary

PCU Type	Failure Criteria	Inhibit Zones
Series dissipative regulator	Failure indicated when → $V_O > V_{RMAX}$	except if → $V_I > V_{IMAX}$ or $I_O < I_{OMIN}$
	$V_O < V_{RMIN}$	$V_I < V_{IMIN}$ or $I_O > I_{OMAX}$
	$I_O < I_I$	$I_I < I_{IMIN}$
Inverter, Converter	$V_O \neq K_1 V_I$	$V_I < V_{IMIN}$ or $I_O > I_{OMAX}$
	$I_O \neq K_2 I_I$	$I_I < I_{IMIN}$
Switching Regulator	$V_O > V_{RMAX}$	$V_I > V_{IMAX}$ or $I_O < I_{OMIN}$
	$V_O < V_{RMIN}$	$V_I < V_{IMIN}$ or $I_O > I_{OMAX}$
	$P_O < \eta_{MIN} P_I$	$I_O < I_{OMIN}$ or $I_O > I_{OMAX}$ or $I_I < I_{IMIN}$
Shunt Regulator	$V_O > V_{RMAX}$	$I_S (= I_I - I_O) > I_{SMAX}$
	$V_O < V_{RMIN}$	$I_S (= I_I - I_O) < I_{SMIN}$

Nomenclature:

I	Current
V	Voltage
P	Power
η	Efficiency, output power/input power
K	Arbitrary constant

Subscripts:

I	Input
O	Output
R	Regulated
S	Shunt
_MAX	Maximum value of previous subscript. Ex. V_{OMAX} = maximum output voltage
_MIN	Minimum value of previous subscript
1,2,...	Arbitrary designations

6.1 SERIES DISSIPATIVE REGULATOR

The series dissipative regulator is described by the three curves of Figure 6-2. Their relation with each criterion of Table 6-1 is as follows:

a. $V_O > V_{RMAX}$: Curve A shows the relationship of V_I and V_O. V_O follows V_I up to a certain minimum value (V_{IMIN}) and remains constant until some maximum allowable value of V_I (V_{IMAX}). Thereafter V_O increases accounting for the inhibit function $V_I > V_{IMAX}$. Curve C shows the relationship of V_O and I_O. At very low values of I_O, V_O can increase above the regulation limits accounting for the inhibit $I_O < I_{OMIN}$. For series dissipative regulators, I_{OMIN} is practically zero, and therefore, the possible rise in V_O is not shown.

b. $V_O < V_{RMIN}$: The inhibit function $V_I < V_{IMIN}$ follows from curve A when $V_O \approx V_I$ up to the point where $V_I = V_{IMIN}$. Curve C shows a drooping output for $I_O > I_{OMAX}$ accounting for this second inhibit.

c. $I_O < I_I$: In a series dissipative regulator, the input current is equal to the output current for all conditions with appreciable inequality only at very low loads as shown on curve C. The appropriate inhibit function is, therefore, $I_I < I_{IMIN}$.

6.2 INVERTER OR CONVERTER

Inverters or converters are described by the three curves of Figure 6-3. Their relation with the criteria described in Table 6-1 are as follows:

a. $V_O \neq K_1 V_I$: Since inverters and converters are strictly voltage transformation devices, the voltage ratio shown by curve A is constant providing V_I is greater than some V_{IMIN} (usually about 10 volts determined by switch voltage efficiency). Normal performance is expected as long as V_I is above V_{IMIN} as shown by curve A and C. Curve C also shows that with $I_O > I_{OMAX}$, V_O decreases causing the ratio $V_O/V_I \neq K$; however, a transfer is inhibited because $I_O > I_{OMAX}$ is an overload. Therefore, an output voltage failure is indicated when $V_O \neq K_1 V_I$, except for inhibit conditions of $V_I < V_{IMIN}$ and $I_O > I_{OMAX}$.

b. $I_O \neq K_2 I_I$: Curve B shows the input current, V_I, as a function of load current, I_O. This ratio under normal performance is constant above I_{IMIN} (established by fixed losses of PCU). If I_I rises due to additional internal losses, then $I_O \neq K_2 I_I$ and the PCU is failed, except if $I_I < I_{IMIN}$. If $I_O \neq K_2 I_I$ and $I_I > I_{IMIN}$, the PCU is failed.

Curve A — VOLTAGE-V_I plotted against VOLTAGE-V_O, with V_{IMAX} and V_{IMIN} marked, $I_O > I_{OMAX}$, and V_R.

Curve B — CURRENT-I_I plotted against CURRENT I_O, with $\dfrac{I_O}{I_I} = K \approx 1$, $V_O = R$, and I_{OMIN}.

Curve C — VOLTAGE plotted against CURRENT-I_O, with V_{IMIN}, V_R, I_{OMAX}, OVERLOAD, SHORT TRANSISTOR.
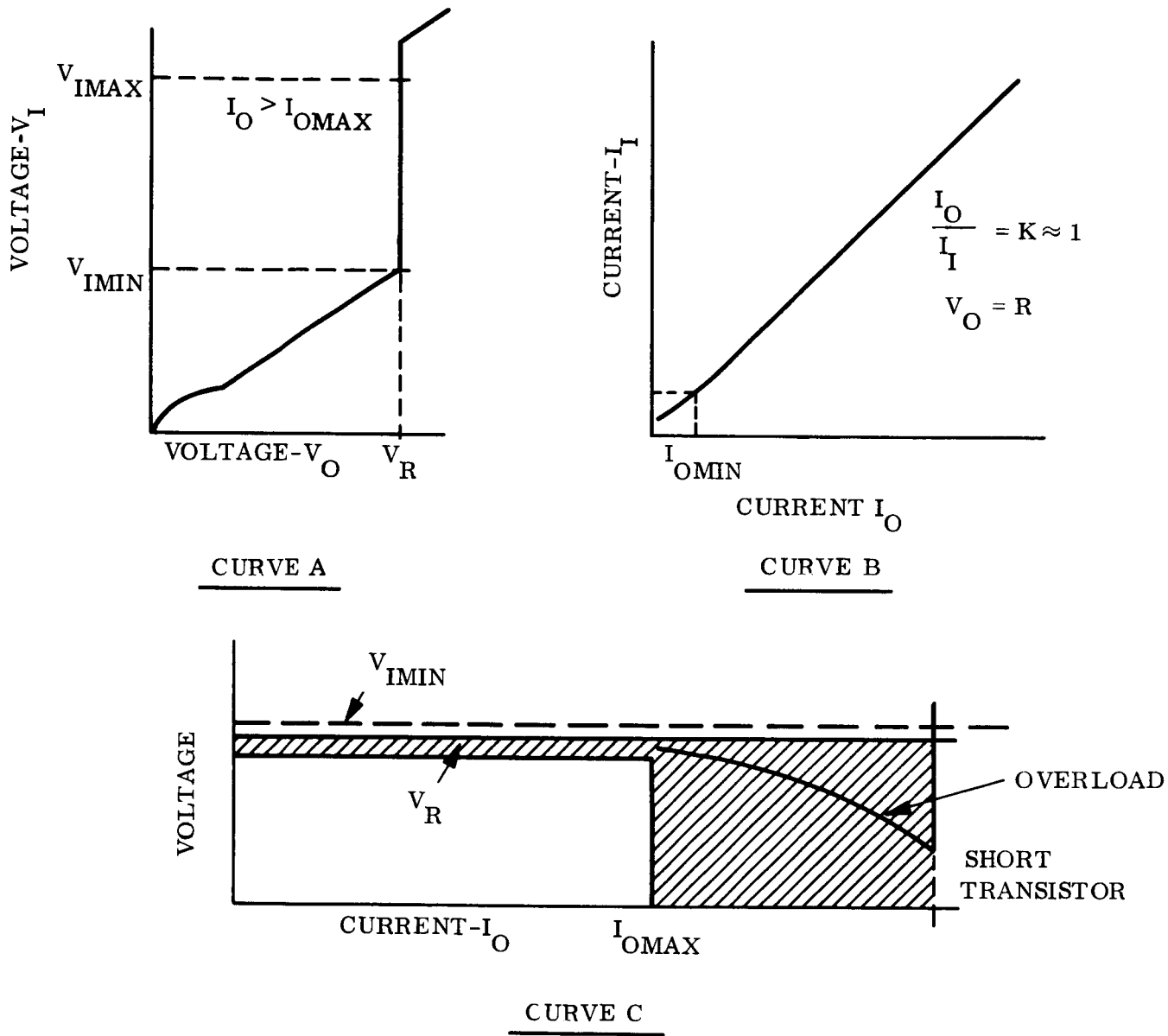
Figure 6-2. Voltage – Current Characteristics of Series Dissipative Regulator
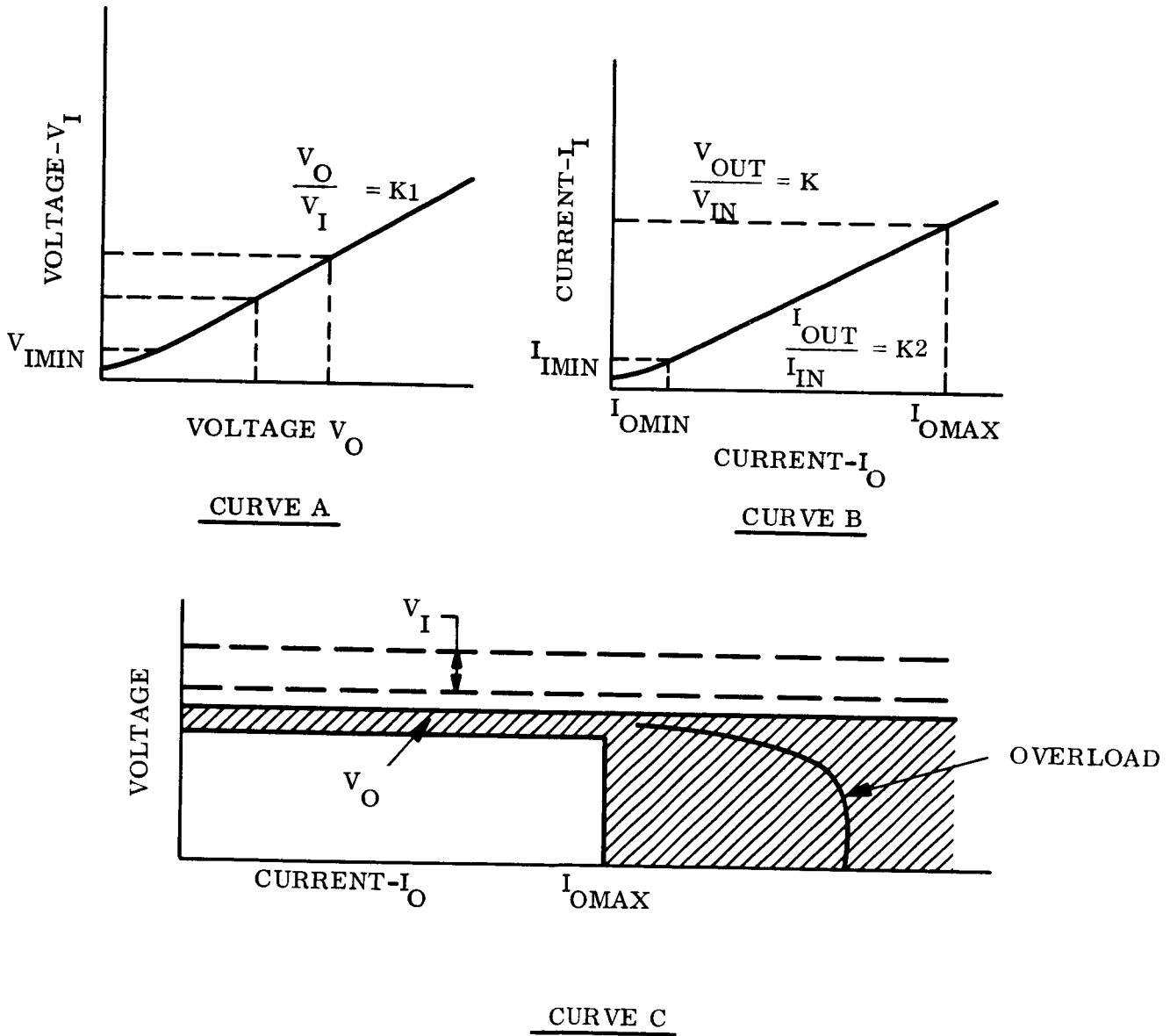
Figure 6-3. Voltage – Current Characteristics of Inverter or Converter

6.3 SWITCHING REGULATORS

The switching regulator is described by the three curves of Figure 6-4. These curves describe the general characteristics of buck, boost, buck-boost and converter or inverter/regulator combinations with a single critical output. Their relation with the criteria described in Table 6-1 are as follows:

a. $V_O > V_{RMAX}$: Curve A shows the relationship between V_I and V_O. This curve is similar to the series dissipative regulator V_I V_O curve, except V_O may be greater or less than V_I. Curve A shows that $V_O > V_{RMAX}$ when $V_I > V_{IMAX}$; therefore, the PCU is failed when $V_O > V_{RMAX}$, except if $V_I > V_{IMAX}$. Curve C shows that $V_O > V_{RMAX}$ if $I_O < I_{OMIN}$ (a characteristic of the LC output filter under light loads). Therefore, the PCU is failed when $V_O > V_{RMAX}$, except if $I_O < I_{OMIN}$.

b. $V_O < V_{RMIN}$: Curve A shows that $V_O < V_{RMIN}$ when $V_I < V_{IMIN}$ and Curve C shows that $V_O < V_{RMIN}$ when $I_O > I_{OMAX}$. Therefore, the PCU is failed when $V_O < V_{RMIN}$, except when $V_I < V_{IMIN}$ and $I_O > I_{OMAX}$.

c. $P_O < \eta_{MIN} P_I$: Curve C shows that between I_{OMIN} and I_{OMAX}, V_O is within regulation limits and the efficiency is reasonably constant and greater than η_{MIN}. If $P_O < \eta_{MIN} P_I$ the PCU is failed, except if $I_O < I_{OMIN}$ and $I_O > I_{OMAX}$. It is possible to have an efficiency failure when $I_O < I_{OMIN}$. Curve B shows that for $I_O = I_{OMIN}$, there is a $I_I = I_{IMIN}$. If $P_O < \eta_{MIN} P_I$, the PCU is failed if $I_I > I_{IMIN}$ or not failed if $I_I < I_{IMIN}$.

6.4 SHUNT REGULATOR

The shunt regulator is described by the curve of Figure 6-5. Its relations with each criterion of Table 6-1 is as follows:

a. $V_O > V_{RMAX}$: At $V_O = V_{RMAX}$, the regulator is shunting maximum design current. For higher shunt current, it cannot maintain regulation, and therefore, the inhibit function is $I_S > I_{SMAX}$.

b. $V_O < V_{RMIN}$: At $V_O = V_{RMIN}$ the regulator normally shunts minimum current. If $I_S > I_{SMIN}$ when $V_O < V_{RMIN}$, the regulator is considered failed since I_S should be $< I_{SMIN}$. Therefore, the failure indication is $V_O < V_{RMIN}$, except if $I_S < I_{SMIN}$.
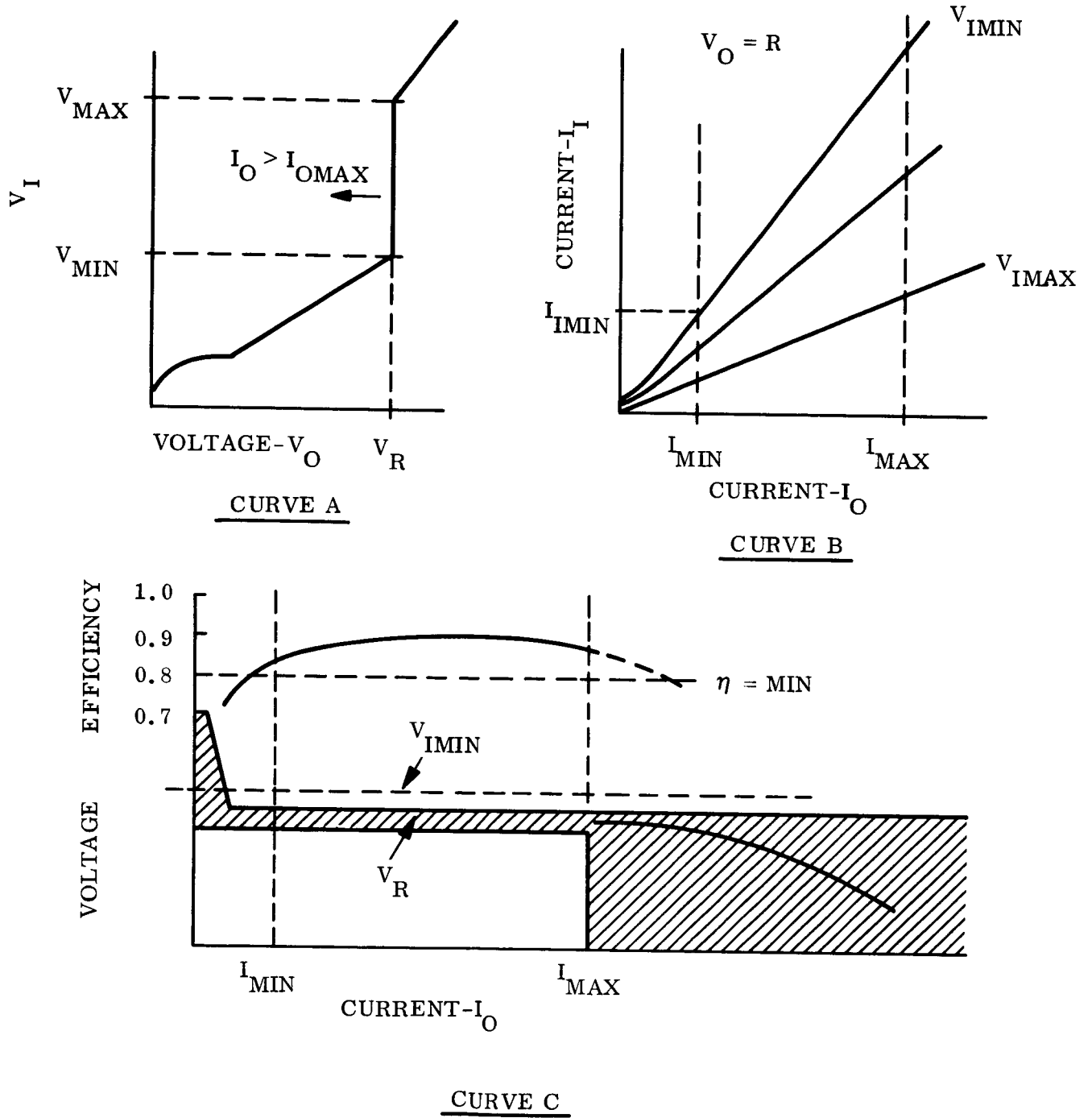
Figure 6-4. Voltage – Current Characteristics of Switching Regulator
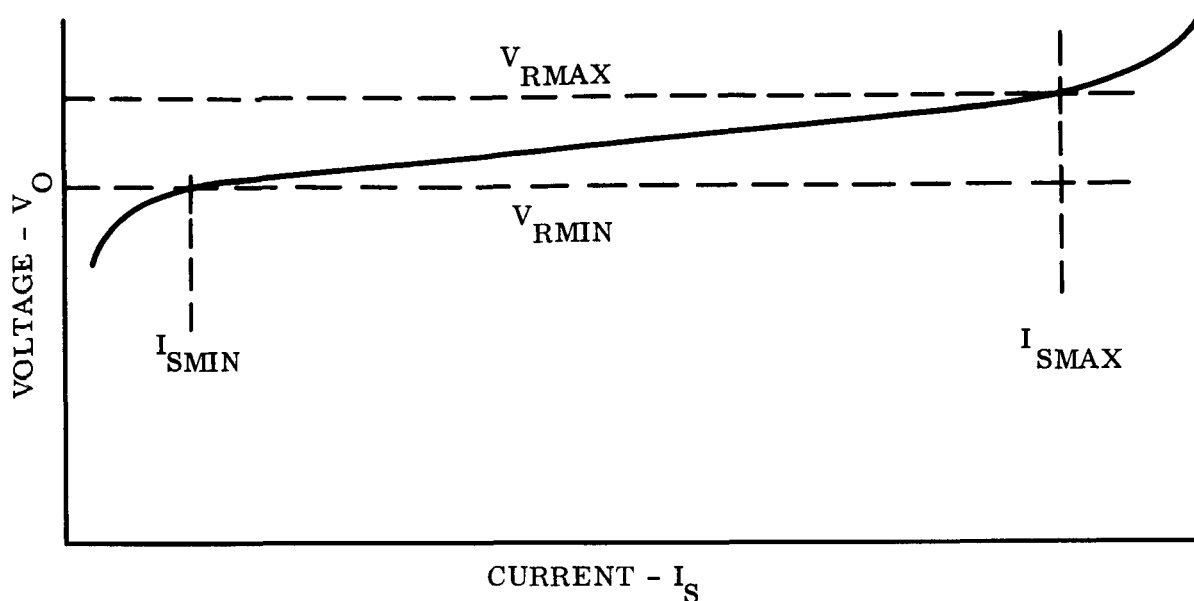
Figure 6-5. Shunt Regulator Characteristics

6.5 DISCUSSION

Of all the failure detector requirements discussed, the failure detector for the switching regulator requires the greatest number of circuit functions (Refer to Table 6-2). Note that the circuit functions required for any of the other failure detectors is included in the switching regulator failure detector which is easily modified for use with the other PCU's discussed.

The fault detector developed by GE can perform the functions described. Its application to Mariner power systems will be examined in the forthcoming phase of the program using the criteria described above. Any decision to ultimately employ such fault detectors will depend on the outcome of the reliability sensitivity studies described in Section 5.0.

Table 6-1. Circuit Summation for Relative Complexity

PCU	Series Dissipative Regulator		Converter or Inverter		Switching Regulator		Shunt Regulator	
	Vout	Eff.	Vout	Eff.	Vout	Eff.	Vout	Eff.
Failure Indicators	2-volt divider	2-curr 1-curr ratio	2-volt divider 1-volt ratio	2 curr 1 curr ratio	2 volt divider	2 curr 2 volt 2 (mult.) 1-power ratio	2 volt divider	1 curr
Load Inhibit	2 current		2 current		2 current		2 current	
Source Inhibit	2 voltage		1 voltage 1 current		2 voltage 1 current		None	
Circuit Summation	9		9		14		5	
Logic Circuits	-		-		Highest Most Complex Failure Detector		Lowest	

SECTION 7

DISTRIBUTION FREQUENCY OPTIMIZATION

Much of the power of the MM '69 spacecraft is ac distributed at a frequency of 2.4 kHz. This section provides an analysis of whether this frequency is near optimum from the standpoint of weight. The only constraint is that the wave form be essentially square.

The principal elements whose weights are affected by frequency are: (a) dc/ac inverters; (b) ac/dc transformer-rectifiers; (c) power source equipment whose size is affected by possible efficiency changes in the inverters and transformer-rectifiers. Each of these elements are considered separately below.

7.1 INVERTER WEIGHT

As a function of frequency, inverter weight is primarly sensitive to power transformer weight. The weight of the power switch transistors and drive circuits in comparison to the output power transformer is relatively constant. Thus transformer weight as a function of frequency may be studied separately since the results will provide the most sensitive data for observing inverter weight effects.

Transformer size depends on power output, efficiency, temperature rise, voltage levels, and frequency. Specific designs were analyzed and the results are plotted in Figure 7-1. The frequency was varied from 60 to 5000 Hz under the following constraints:

    a.   Power level is constant.

    b.   Efficiency is constant--hence for equal assembly materials and procedures temperature rise is also considered constant.

    c.   Voltage levels are not in a range where extra insulation affects size or weight.

SPECIFIC DESIGNS BASED ON
ARNOLD SILECTRON CORES
TYPE-C CORES
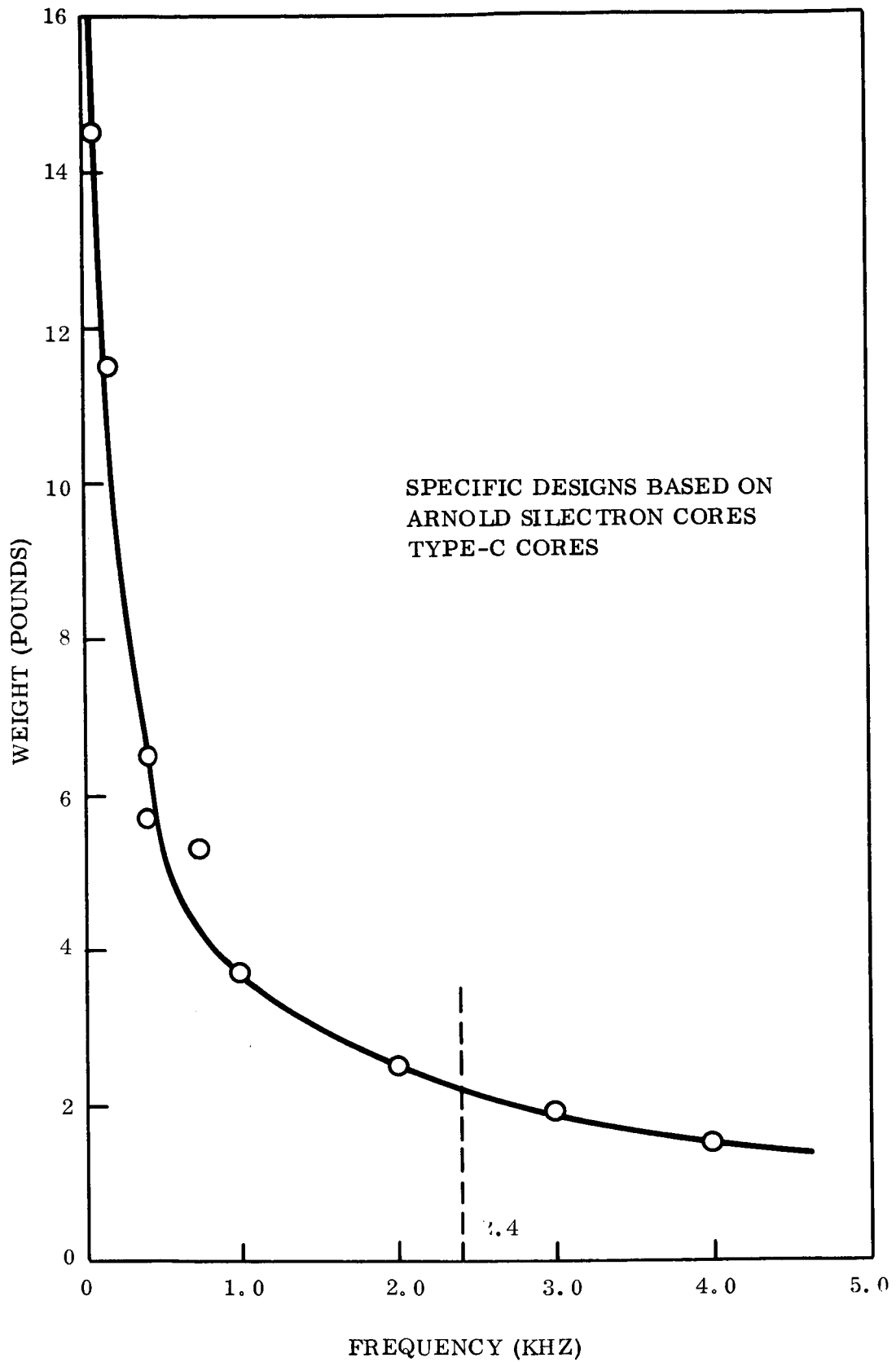
Figure 7-1.   Transformer Weight 200 Watt Output, 97 Percent Efficiency

In addition to the designs of Figure 7-1, a search was conducted to obtain results of other design procedures. The results of this search are plotted in Figure 7-2. The levels in this figure are relative and are representative of three design procedures as a function of frequency. Note that regardless of procedure the percent change in weight beyond 1000 to 2000 Hz is not appreciable.

7.2 TRANSFORMER-RECTIFIER (T/R) WEIGHT

The same assumptions established for determining inverter weight sensitivity to frequency are directly applicable to the T/R weight. The curve generated for the inverter/transformer weight is directly applicable to T/R weight.

7.2.1 PRELIMINARY CONCLUSION

Based on the weight of the inverters and T/R's, a preliminary conclusion is that operation beyond 1.5 kHz does not provide sufficient weight gain to merit its consideration. To substantiate this conclusion, the question of overall power system weight effects must be answered.
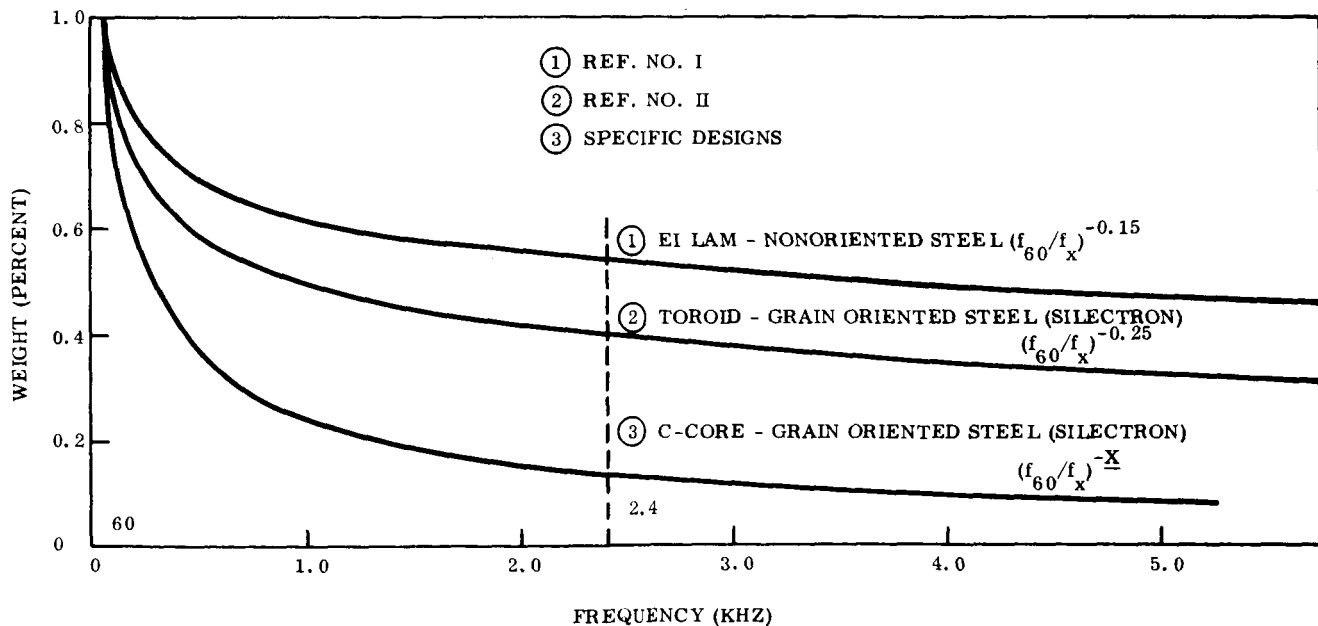
Figure 7-2. Transformer Weight Percent Reference to 60 Hz

answered. The parameter which effects solar array and battery sizing is inverter and T/R efficiency. This parameter is examined in the following paragraph.

7.3 POWER SOURCE WEIGHT

7.3.1 TRANSISTOR EFFICIENCY

The power switch operates either full on or full off with a finite time required for transfer. This transfer time is determined by intrinsic transistor characteristics and results in switching power losses. The more frequent the switch transfers the greater are the switching losses.

Since power transformer efficiency is constant by design, the inverter efficiency can be analyzed by considering only power switching losses as a function of frequency. These losses are expressed by the following equation which is derived in Appendix B:

$$P_{sw} = f V_{in} I_c \left[0.71 t_s + 4/3 \left(\frac{t_s t_f}{t_s + t_f} \right) + 5/3 \left(\frac{t_f^2}{t_s + t_f} \right) + 0.33 t_f \right] X$$

$$\left[\frac{1}{1 - 4 f (t_s + t_f)} \right]$$

where:

P_{sw} is power switch loss in watts (P_{sw} occurs twice per cycle)

f is frequency

V_{in} is supply voltage less $V_{ce_{SAT}}$

I_c is peak collector current

t_s is storage time

t_f is fall time

7.3.2 RECTIFIER EFFICIENCY

Rectifier efficiency is treated similarly to the transistor switch efficiency as a function of frequency. The losses are expressed by the following equation, which is derived in Appendix C:

$$P_{rsw} = f \, V_R \, I_D \, 1/6 \, t_{rec}$$

where

P_{rsw} is power rectifier switching loss in watts

f is frequency

V_R is peak reverse voltage seen by rectifier

I_D is rectifier peak current

t is recovery time of diode

P_{rsw} occurs twice per cycle.

Since recovery time of diodes is at least an order of magnitude faster than transistor switching times, it is considered negligible in this analysis for the frequency range considered.

7.3.3 INVERTER EFFICIENCY

Transistor switching losses along with other transistor losses (drive losses and saturation losses) were used in a computer program to determine inverter efficiency as a function of frequency. The results are shown in Figure 7-3 for an inverter of the Mariner '69 design for two sets of t_s and t_f.

7.3.4 POWER SOURCE WEIGHT

Based on the Mariner '71 load profile, the specific weight in pounds per watt at the inverter input can be determined when the inverter operates from the solar array only and from the battery only. Table 7-1 derives the specific weight (0.288 lb/watt) for the solar array, and Table 7-2 derives the specific weight (0.117 lbs/watt) for the battery.
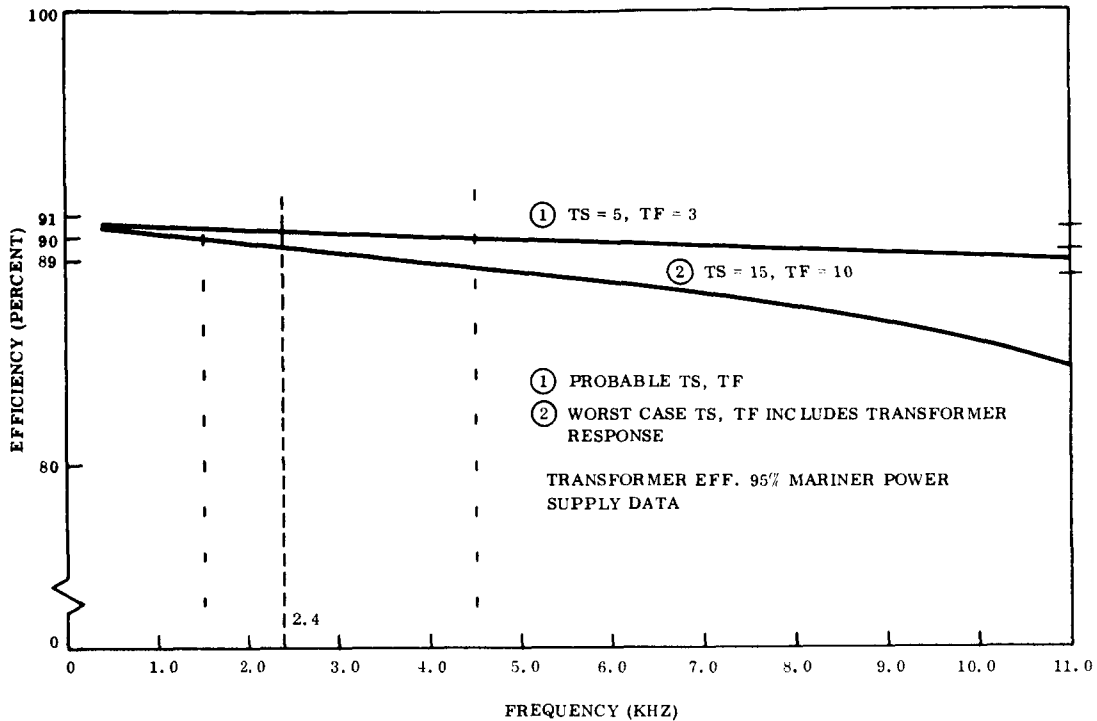
Figure 7-3. Square Wave Inverter Efficiency

Using these specific weights and knowing the inverter efficiency and transformer weight as a function of frequency, total power system weight can be determined as a function of frequency. The results are tabulated in Table 7-3 for several values of frequency and bracketing values of t_s and t_f.

7.4 CONCLUSIONS

The results of Table 7-3 indicate that frequency has little effect on weight within the frequency range examined. While operation at 4 kHz appears optimum, the weight gain is only about 0.5 pounds (or 0.5 percent) compared to that at 2.4 kHz. This provides little incentive for considering a change from the frequency presently used on the MM '69 system. These results are consistent for the extremes of t_s and t_f considered.

Table 7-1. Primary Power Source Weight – Pounds per Watt at Inverter Input

- MM '71 load profile

- Far Encounter phase – Solar Array Case

- 2.4 kHz Inverter load = 214 w

- Inverter Input (214/0.918) = 233 w

- Inverter load reflected at array

  Boost Reg. Efficiency = 0.887
  Distribution Losses = 0.97

  $$\frac{214}{0.918 \times 0.887 \times 0.97} = 271 \text{ w}$$

- Total array demand = 421 w

- Percent array for inverter loads = $\frac{271}{421}$ = 64%

- Array Weight:

  Cell ass'y –   50 lb
  Structure –   54.5 lb
                   104.5

- Percent array weight for inverter loads 0.64 x 104.5 = 67 lb

- Array weight per watt at inverter input =

  $\frac{67}{233}$ = 0.288 lb/watt

Table 7-2. Secondary Battery Source Weight – Pounds per Watt at Inverter Input

- MM '71 load profile

- Orbit insertion phase – Battery Case

- 2.4 kHz Inverter load = 179.5 w

- Inverter input (179.5/0.910) = 197 w

- Inverter load reflected at battery

  Boost Regulator efficiency = 0.842
  Distribution loss = 0.97

  $$\frac{179.5}{0.910 \times 0.842 \times 0.97} = 242$$

- Total Battery demand = 326 w

- Percent battery for inverter = $\frac{242}{326}$ = 74%

- Battery weight = 31 lb

- Percent battery weight for inverter = 0.74 x 31 = 23 lb

- Battery weight per watt at inverter input = $\frac{23}{197}$ = 0.117 lbs/watt

Table 7-3. Power System Weight

FREQ Hz	Inverter Load SA/B	Inverter Efficiency	Inverter Input SA/B	Total Transformer Weight	Solar Array Weight	Battery Weight	Total Weight
$t_s = 5, t_f = 3$							
1,000	214 180	0.905	236 198.9	7.4	68.0	23.2	98.6
2,400	214 180	0.904	237 199.2	4.4	68.3	23.3	96.0
4,000	214 180	0.900	238 200	3.0	68.6	24.0	95.6
$t_s = 15, t_s = 10$							
1,000	214 180	0.902	237.5 199.5	7.4	68.4	23.3	99.1
2,400	214 180	0.896	239 201	4.4	68.8	23.5	96.7
4,000	214 180	0.888	241 203	3.0	69.4	23.7	96.1
6,000	214 180	0.879	244 205	2.6	70.2	24.0	96.8

Total Trans Wt. Includes T/R and Inverter.

Weight – pounds
Array – 0.288 lb/watt
Battery – 0.117 lb/watt
SA/B – Solar Array/Battery

SECTION 8

POWER SWITCHING AND DISTRIBUTION

This section discusses the present status of electrical equipment design in the power control, switching, and distribution areas of power system design as they might relate to future Mariner spacecraft. The information presented here is based primarily on hardware experience with the Nimbus satellite, the Gravity Gradient Test Satellite, Biosatellite, and classified programs. All of these systems use dc distribution and the concepts discussed are applicable to such dc systems in general. The specific design characteristics to be discussed are:

- Flexibility to incorporate changes

- Command Input Redundancy

- Driver Failure Protection

- Command Matrix Implementation

- Noise Sensitivity

- Relay Coil Suppression

- Soft Commutation

- Contact Suppression

8.1 FLEXIBILITY

In the context of power switching and distribution design, flexibility pertains to the ease of incorporating changes which normally arise in the course of a hardware program.

Such flexibility has been attained by locating as many switching functions as possible within a single distribution unit including the provision for spares. The use of a single distribution unit has the advantage of concentrating switching and distribution design within one area of specialization and usually results in a more uniform selection of switching devices, more efficient packaging, and reduced noise susceptibility.

All power switching has been typically accomplished with standard latching and holding relay styles. Most applications can be accommodated with contact ratings of two or ten amperes. A long history of performance of these standard devices increases confidence in their use and also reduces replacement costs and simplifies logistics.

The practice has been to separately compartment the relays and relay drivers. Relays are insensitive to noise, require a significant energy pulse to activate the contacts, but are noise generators. The transistorized relay drivers are very sensitive to noise and are protected from relay transients by a separate enclosure. The wire carrying the relay coil signal can have noise induced on it between the transistor driver and the relay coil, but the coil will not respond to this low energy noise.

Spare relays are provided in the power control unit for flexibility and growth as the system evolves. All contacts are wired out to the electrical connector on the component, and multiple diode isolated lines are prewired to allow for redundant commanding. The spare relays are tested as part of the component acceptance and qualification test program, and thus are available in the vehicle to support required changes. The multiple use of similar relays in the component qualifies the new application without special attention to the previously unused relay.

The spare relays are made accessible to the system by changes in the vehicle distribution harness. The concept here is a rear-release crimp contact in the harness connector that allows wires to be switched from one termination point to another without cutting, splicing, soldering, or potting. The electrical connector is disassembled, the required change or additional wiring applied, and the connector reassembled. The changed hardness is revalidated by a full electrical functional test to assure that the required change meets the application. The change does not require that a component be recycled back to the wire shop, thru an electrical functional check, or thru a requalification cycle. The schedule impact on the vehicle flow cycle when the change is incorporated in the vehicle harness is in the order of four to twelve hours, depending on the complexity of the electrical functional test to verify and revalidate the harness.

The crimp contacts eliminate a requirement for skill, judgment, and competence on the part of the operator. The wire is cut and stripped of insulation to a calibrated length with an automatic hand operated tool, the contact is placed on the stripped end of the wire, and a calibrated crimping tool makes a metallurgical pressure bond between the wire and the contact. These tools are calibrated daily as they flow to and from the tool crib. The finished contact can be inspected after the operation is complete to insure that the wire protrudes past the crimp portion, that the indentations at the crimp section are of a sufficient but not excessive depth, and that the insulated portion of the wire extends sufficiently.

8.2 COMMAND INPUT REDUNDANCY

Protection against an open command line on an essential function can be designed into the hardware by providing two or more commands to the same relay coil from various coil drivers in the same or different sources. An example of this is a lock-stepped sequence with a timed command capability. Once the critical sequence is initiated, the initial and each subsequent command activates its own event and starts a separate timing circuit that will time out after the next command is due. If the command does not occur, the back-up timer activates the next event, and diode isolation prevents a fault in the command system from preventing the back-up timer from initiating the next event.

As shown on Figure 8-1 this concept provides protection against an open command line, but does tend to complicate the required vehicle wiring.

8.3 DRIVER FAILURE PROTECTION

When it is necessary to protect against a shorted relay driver applying continuous power to a latching or holding relay, the protection can be provided by switching both ends of the relay coil. It should be noted that a shorted relay coil driver in a conventional system with a common ground return will prevent deactivation of either a latching or a holding relay. This is obvious in the case of the holding relay, and is also true for the latching relay, since the magnetomotive force generated by both the set and reset coil are essentially equal and in opposite directions. It is thus impossible to reset a latching relay when continuous power is
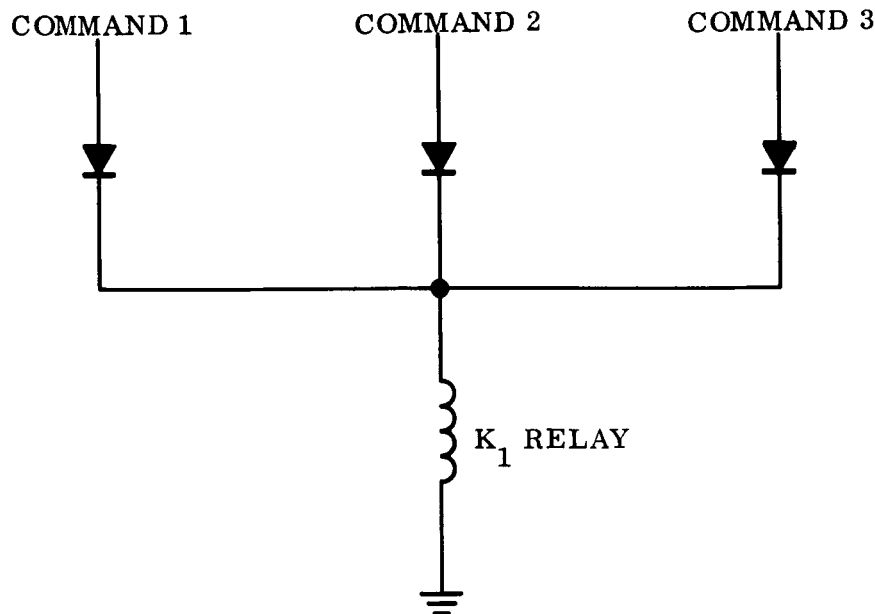
Figure 8-1. Redundant Commanding

being applied to the set coil. To activate an event it is then necessary to turn on positive power to the top of the coil and also provide a ground return for the bottom. Failure of either switch in a shorted position is insufficient to maintain power on the relay coil.

Figure 8-2 shows how protection is provided against a shorted command line on either the positive or ground side. Two failures are required to cause a malfunction of the relay.

8.4 COMMAND MATRIX IMPLEMENTATION

The driver failure protection described above at least doubles the amount of vehicle wiring. When power control is centrally located, the protection can be provided and the vehicle wiring can be reduced by using a matrix concept for relay activation as shown on Figure 8-3. When the X_1 command line is energized, nothing will occur until one of the three Y command lines is returned to ground. If command line Y_2 is returned to ground at the same time that the X_1 command line is energized, then relay coil K_{12} will be activated, but no other relay.
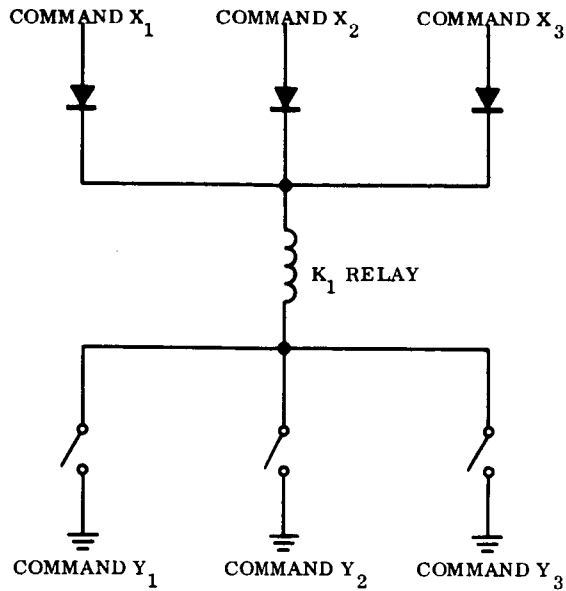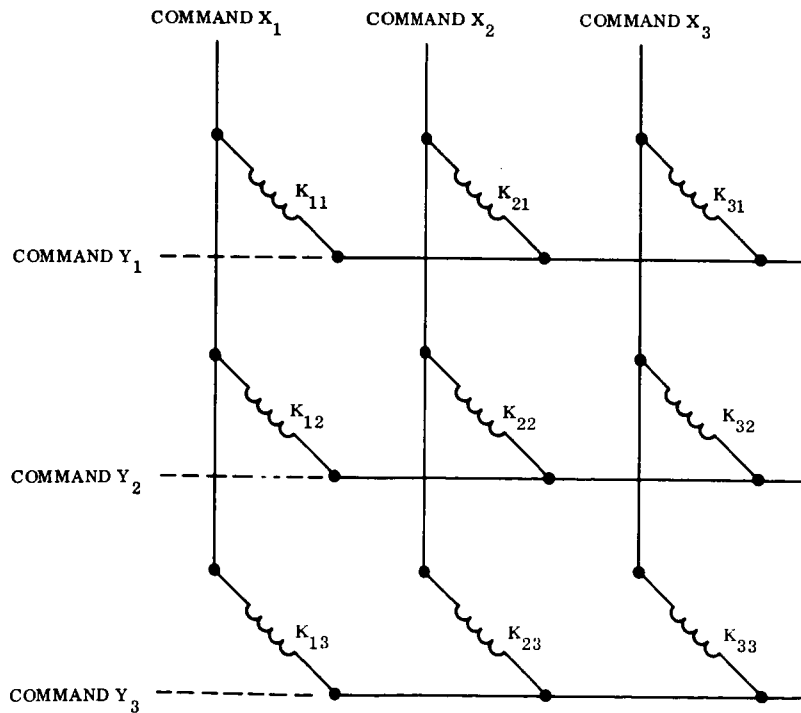
Figure 8-2. Driver Failure Protection

Figure 8-3. Simplified Command Matrix

This concept allows n^2 events to be commanded with 2n separate commands when the commands are arranged in a square array as shown. At least two failures are required before a malfunction occurs. However, if any one command line fails, two events will occur whenever a command is issued. The desired event will occur, and at the same time the valid command will complete the circuit for the failed command line, and allow that event to occur also. It is relatively easy to verify the failure, and a contingent mode capability would allow all subsequent command lists to reset the undesired event immediately after a valid command completed the circuit for a failed command line.

8.5 NOISE SENSITIVITY

When a relay is to be activated, sufficient energy must be supplied in the form of an electrical pulse to establish a magnetic field sufficient to overcome a spring force restraining the moving contact. Electromagnetic relays are relatively insensitive to noise, since a pulse of a significant magnitude and duration is required to accomplish the event. Figure 8-4 shows a typical relay characteristic for a coil rated for twelve-volt service used in a twenty-eight volt system.

The transistorized relay driver is an active amplifier, and will act on a noise pulse of the proper polarity thru the gain of the transistor to possibly cause problems. These problems are minimized by locating the relay drivers in a relatively quiet region remote from the relays. The relays are extremely noisy and would cause the relay drivers to react in a detrimental fashion. However, the relays can exist in their own environment and are insensitive to their own noise.

8.6 RELAY COIL SUPPRESSION

When the current through an inductive circuit is interrupted, a large potential may appear at the terminals of the inductor. The energy stored in an inductor because of a steady-state current must be dissipated before the current goes to zero. When the coil is driven by a semiconductor switch, the energy may destroy the switch if not controlled. A simple
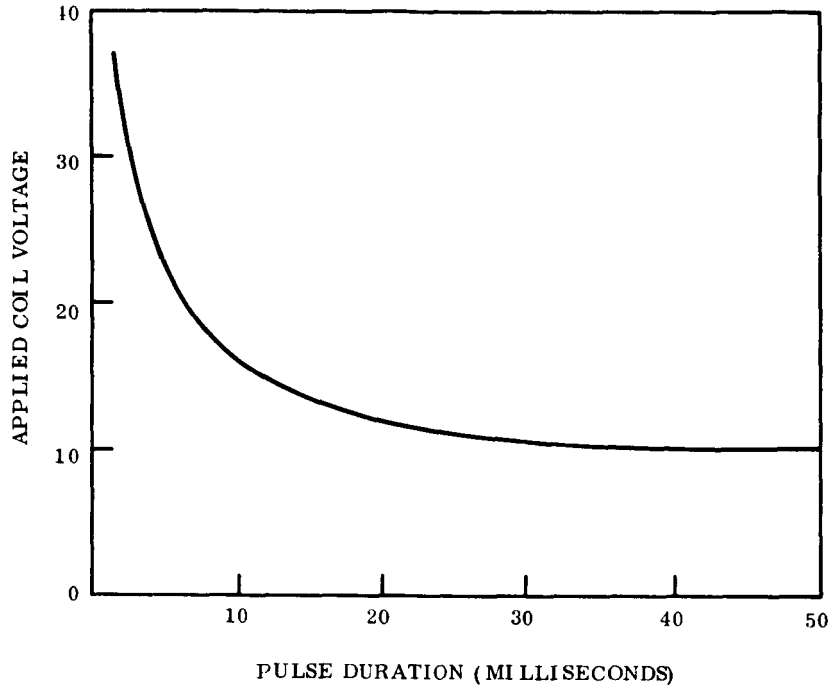
Figure 8-4. Relays Insensitive to Noise

protection method uses a conventional diode suppression circuit where the induced voltage
forward biases a diode to provide a current path as shown on Figure 8-5.

The turn-off transient can be more effectively controlled by replacing the switch with an
active circuit capable of supplying to the coil a current with diminishing magnitude. The
rate of change of current may then be constrained to values low enough to avoid induced
voltages. In Figure 8-5 the transistor traverses the active region at a slow rate, and the
only consequence is an increase in the pull-in and drop-out times of the relay.

8.7 SOFT COMMUTATION

Of special interest in power control is the radiated field generated when current changes in
a vehicle harness wire. To limit these fields to acceptable levels, it is necessary to control
the rate of current rise or fall to values in the order of 5000 amperes per second. This can
be accomplished by providing line inductance, or by controlling the rate of change of current
with semiconductor switches. Figure 8-6 illustrates these approaches.
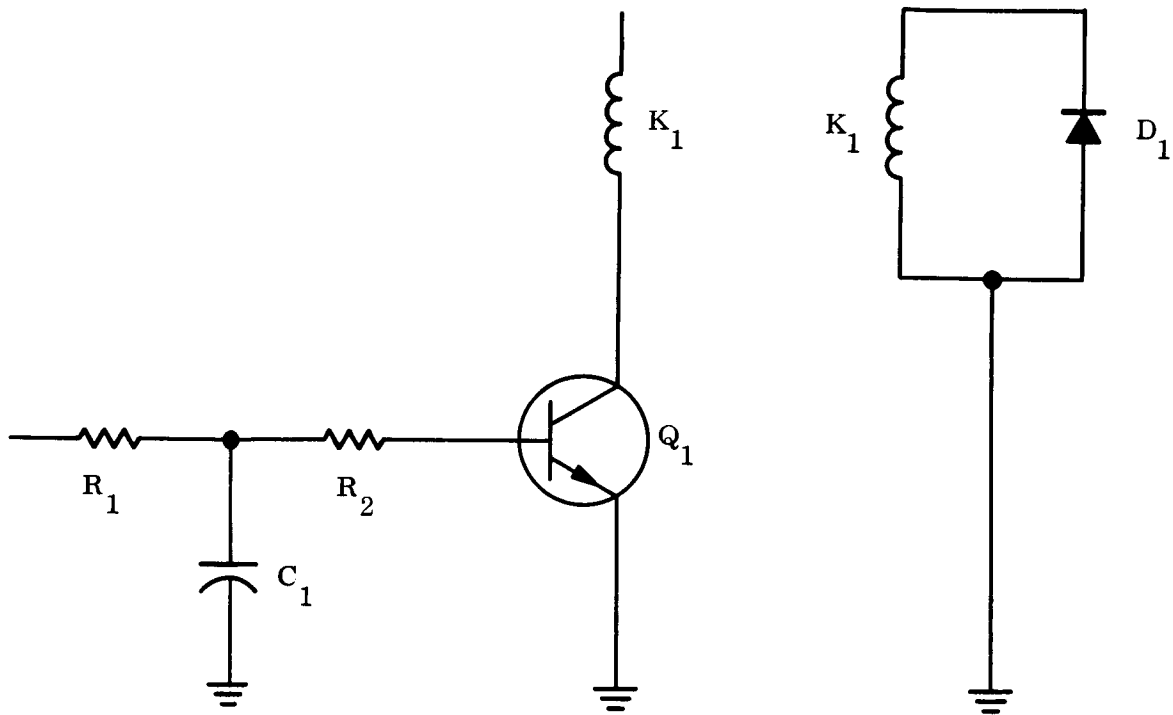
Figure 8-5. Coil Suppression
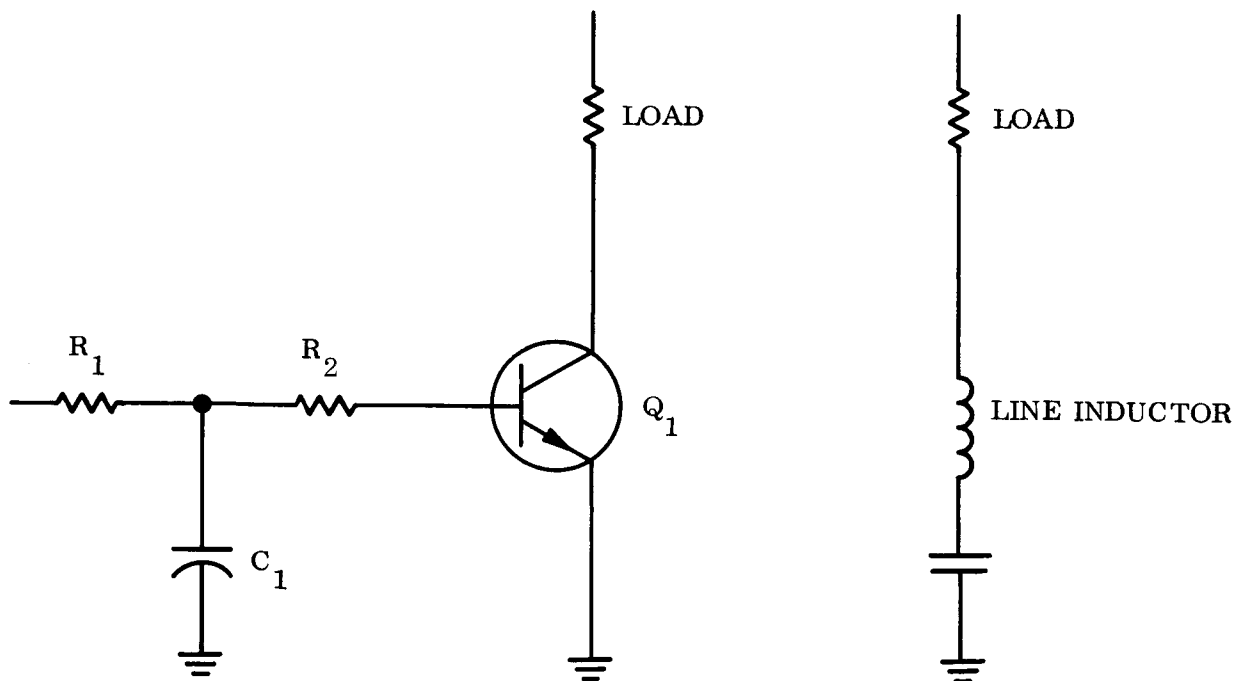
Figure 8-6. Soft Commutation

8.8 CONTACT SUPPRESSION

An inductive load will not allow current to change instantaneously, and when a relay contact attempts to interrupt such current flow an arc is established. The duration of the electro-magnetic noise generated is increased by coil suppression, since the drop-out time increases, and is also increased if the load is deliberately made inductive to control the rate of current rise at turn-on.

The arc suppression problem can be solved by a resistance-diode-capacitance network across the relay contacts as shown on Figure 8-7. The rapid voltage rise at contact opening is caused by the inductive load keeping the load current essentially constant. This current, on contact opening, is fed from the distributed capacity of the circuit wiring. As the voltage rises, at some value of voltage, arcing will occur across the contacts, discharging the wiring capacity. If the load inductance is large, the load current will not have decreased appreciably, and the process will be sustained at an increasing value of breakdown voltage since the contact gap will have increased.

Figure 8-7. Contact Suppression

The value of capacity to be furnished must be sized to limit the arc-over voltage. Its size is a function of the load current and the opening time of the contacts.

$$C = \frac{It}{V}$$

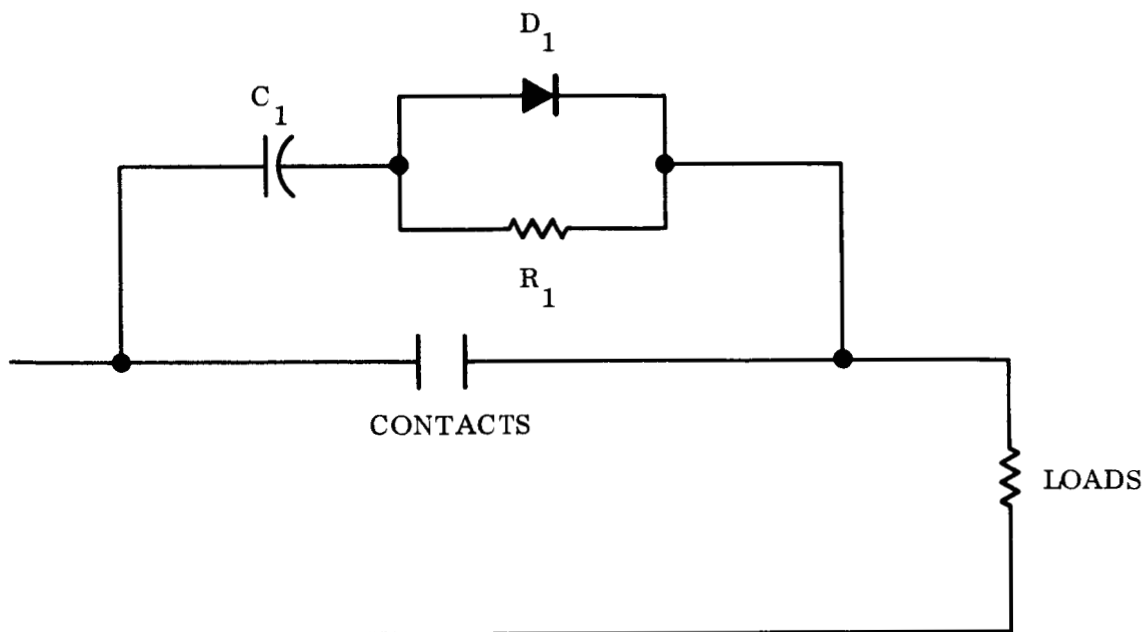where: C = Capacitance required in farads

   I = Load current in amperes

   t = Opening time in seconds (to any gap value)

   V = Gap breakdown at any spacing in volts

Just prior to contact closure this capacitor is charged to the bus voltage that has been across the open contacts. When the contacts close, this capacitor is short-circuited across the contacts, causing excessive surge currents and rapid contact deterioration. This reclosure surge can be controlled by a resistor in series with the capacitor to limit the surge current to a safe value. A good approximation is to make this resistance equal to the load resistance. The load current will increase from zero because of the inductive load, and the surge current will decrease from its initial value due to the CR time constant.

The series resistance destroys the capacitor's effectiveness to furnish the current when the contacts open, but this defect can be corrected by shorting the resistor with a diode. The series resistance for surge protection on contact closure is still retained.

Information required to size the arc suppression circuit is:

   a. Equivalent series inductance of the load
   b. Equivalent series resistance of the load
   c. Distributed shunt capacitance of wiring between contacts and the load
   d. Contact closure time, maximum at worst case

Preliminary experimental evidence indicates that arc-over occurs at some low value of voltage before any significant gap has been achieved, and that this arc is maintained at

15 volts or less during an opening time of two milliseconds. The capacity would have to furnish load current to prevent this voltage from appearing across the contacts. The phenomenon apparently is controllable only by the rate of voltage rise across the contacts. A minimum value of capacity would then appear to be:

$$C = I_{LOAD} \times \frac{1}{\frac{DV}{Dt}}$$

where $\frac{DV}{Dt}$ is the maximum voltage rise that will not ignite the arc. It is on the order of one volt/microsecond, making:

$$C = I_{LOAD} \text{ microfarads}$$

SECTION 9

MM '69 POWER SYSTEM CIRCUIT REVIEW

As an aid in understanding the MM '69 power system, a review of the circuit designs was conducted. As a result of this review some possible modifications to the circuits were developed. These are discussed below.

9.1 DIODES ACROSS POWER TRANSISTORS

Under reactive load conditions resulting from transformer and load impedances, the current level in switching power transistors is maintained during a transfer from on to off states. This can result in excessive voltage buildup arross the transistors. By placing a properly polarized diode across the transistor this condition can be relieved with a possible improvement in reliability.

9.2 FAILURE DETECTOR TRANSIENT SUSCEPTIBILITY - MODULE 4A

Transfer from the main to the redundant regulator/inverter chain should occur when an out-of-specification voltage exists for greater than 1.5 ± 0.5 seconds. The Schmitt trigger, used to start the one second delay, may not reset if the voltage deviation exists for less than 1.5 ± 0.5 seconds and could result in an undesireable transfer. This transient susceptibility could result because the 0.1 volt hysteresis level of the Schmitt trigger may be too high. Testing with signal pulses between 0.1 and 1.0 second duration would provide an indication of whether this is indeed a problem.

9.3 INVERTER SYNCHRONIZATION

On startup the inverter operates in the free-run mode until voltage output from the inverter starts the crystal oscillator and countdown chain to provide the synchronization pulse. Since the synchronization pulse can occur any time during the free run, the summation of T2 voltage support time and synchronization time results in a time great enough to cause the power transformer to saturate. This reduces voltage to the oscillator and count down chain which may result in operational instability. However, since the saturation time of the output transformer

is short (20 to 30 microseconds) the voltage to the oscillator may not fall to a low enough level to cause the oscillator to stop. Also, this short saturation time probably would not damage the power transistors. A possible solution to the instability question is to operate the oscillator directly from the dc input voltage to the inverter. The free-run pulse would operate only if the synchronization pulse is lost.

An additional problem concerns crystal oscillator failure after normal operation is attained. The last flip-flop of the count down chain remains in a fixed state and would apply a constant voltage to the Q4A or Q4B base circuit through C12R15. This RC time period is 17.1 milliseconds. Transformer, T1, saturates in a time period of 0.521 milliseconds. This time (T1 to saturate) is greater than the time the output transformers, T3 and T4, can support voltage (0.329 milliseconds). Thus Q5 or Q6 will probably short removing drive power from Q7 and Q8 and would present a heavy load to the boost regulator. Thus a failure of this oscillator would not result in free-run operation but in loss of output voltage. A transfer to the redundant chain would occur based on a voltage decrease rather than a frequency shift. Note also that the standby inverter has the same potential deficiency. Testing would verify the above possibilities.

A potential solution is to free run at a frequency 5 to 10 percent below 2.4 kHz and to reduce synchronization pulse duration to approximately 1/8 to 1/4 of the synchronization period. This solution would also relieve the operational instability question previously discussed.

9.4 BOOST REGULATOR OVERLOAD PROTECTION

Heavy overloads are reflected to the boost switching power transistors through the boost transformer, and could degrade or destroy the power transistors.

The most probable failure of the power transistor would be a short. High current could then be drawn from the battery resulting in the possible welding of the input relay contacts.

A possible modification is to provide an overload control which would reduce the duty cycle on the power transistors as a function of the overload current.

9-2

SECTION 10

FUTURE PLANS

The planned activities for the remainder of the contract are shown in Figure 1-1. The emphasis during the coming month will be on the following tasks:

Task 3.0 System Design - Shunt

- Detailed Circuit Approaches

- Battery Selection

- Battery Charging Approaches

- Redundancy Implementation

Task 2.0 Fault Sensing

- Relative Evaluation of Various Approaches

Task 4.0 System Level Reliability Studies

- Exercise MM '69 Model

    - Redundancy Comparison

    - Component Sensitivity

APPENDIXES

APPENDIX A

PROCEDURE FOR PREDICTING SOLAR ARRAY VOLTAGE-CURRENT CHARACTERISTICS

The basic data required to predict solar array performance as a function of sun distance are (1) measured voltage-current characteristics (V-I) of solar cells preferably at 1 sun intensity and various temperatures and (2) temperature-sun distance history. Figure A-1 shows a typical set of V-I curves at various temperatures as measured under a carbon-arc simulator adjusted to a one sun intensity. The cells are 1 ohm-centimeter N/P cells supplied by RCA. Through curve-fitting techniques, these data are stored in a computer program which can produce the necessary V-I data for any interpolated value of temperature.

The program also produces adjusted V-I curves in response to series and parallel multiplying factors, adjustments in short circuit current and adjustments in open circuit voltage. Each of these is described below:

a. Series and parallel multiplying factors. This is a straightforward multiplication of current for paralleled cells and voltage for series cells.

b. Short circuit current adjustment. The short circuit current at a particular operating temperature and 1 AU is adjusted by the following multiplying factors:

	Typical Value
Filter loss	0.92
Radiation degradation	0.935
Sun distance	$(AU)^{-2}$
RMS loss & contingency factor	0.90
which includes:	
–Manufacturing loss 2%	
–Measurement uncertainty 4%	
–Micrometeroid erosion 4.5%	
–Ultraviolet effect on filter 5.5%	
–Random cell failures 5%	

The predicted V-I characteristic is obtained by translating the 1 AU bare cell characteristic to the adjusted value of short circuit current. This translation is not purely in the X direction but also slightly in the Y direction to take account of a series resistance effect. The method for estimating this effect is shown on

Figure A-2. Measurements taken on unilluminated cells show that the diode characteristic shown on the left quadrant has the same basic shape as the illuminated V-I characteristic at 1 AU but is shifted higher in voltage by an amount Vs equivalent to the short circuit current at 1 AU times Rs, the series resistance effect. This effect is temperature sensitive and for the RCA cells cited has an average value of about 0.4 ohms. Though the effect is small, the computer program takes it into account by translating the V-I shape along the Rs line to the adjusted value of short circuit current.

c. Open circuit voltage adjustment. This is a direct translation in the Y direction to take account of radiation degradation of voltage. A typical value of the multiplying factor is 0.96.

Other features of the program include allowances for protective diode voltage drops and nonnormal solar incidence angles.
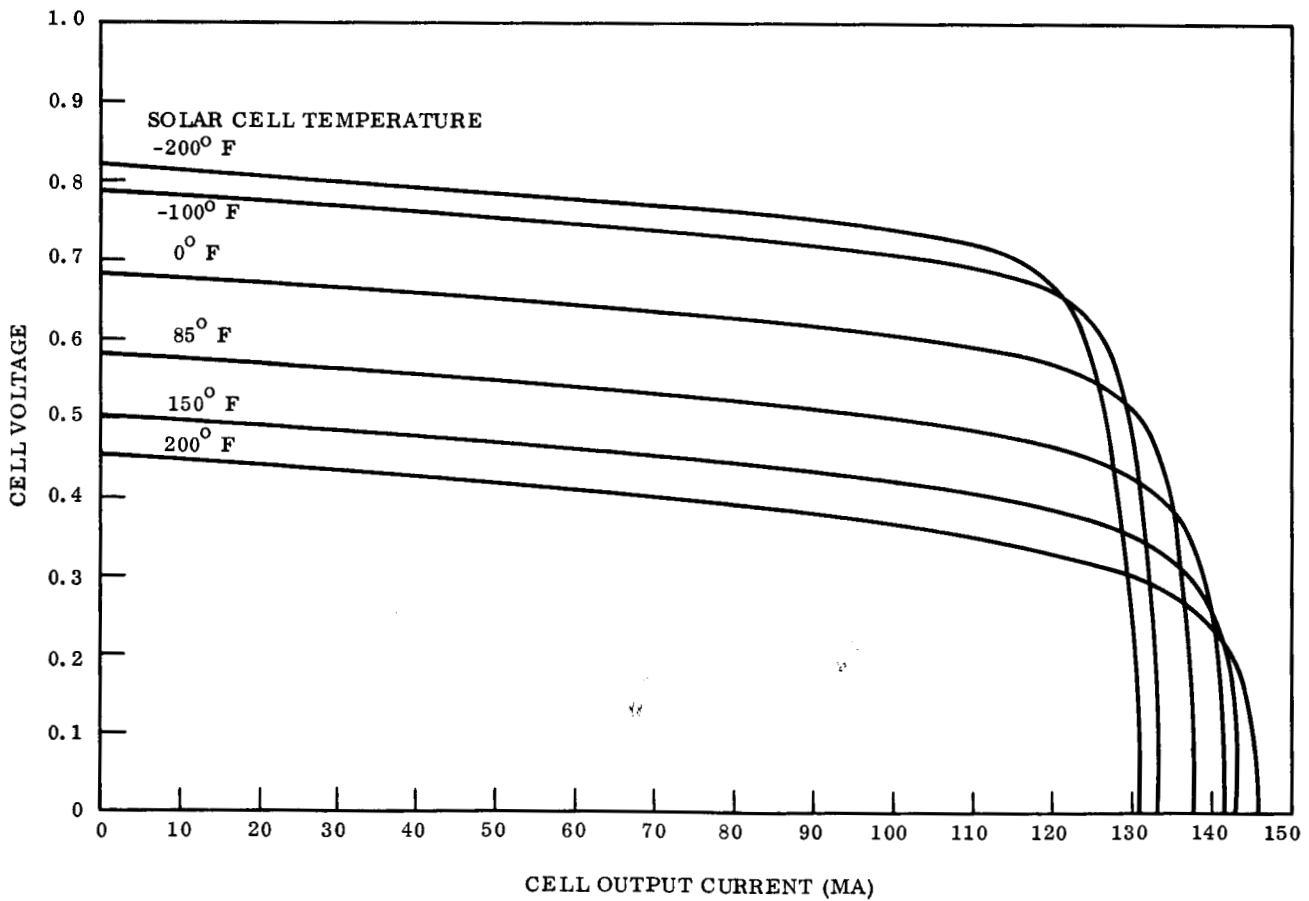

Figure A-1. Voltage-Current Characteristics of 1-ohm-cm N/P Solar Cells
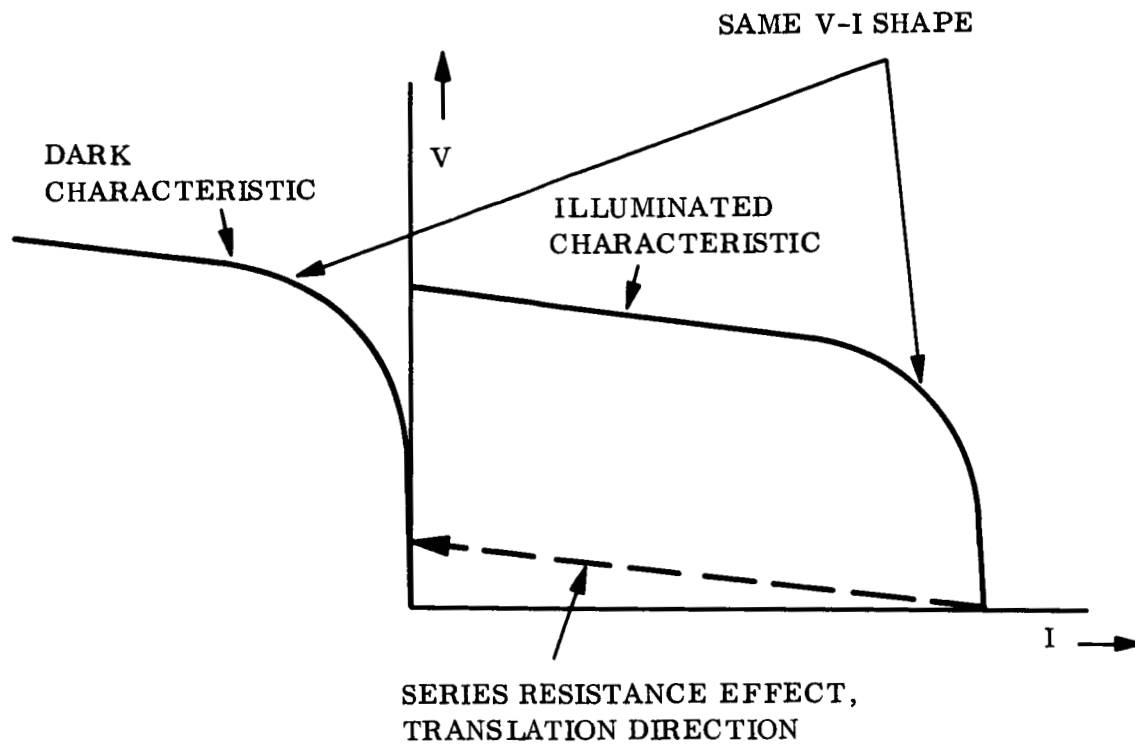
Figure A-2. Voltage-Current Translation for Reduced Illumination

APPENDIX B
INVERTER EFFICIENCY ANALYSIS

Inverter efficiency is mostly affected by transistor and transformer losses. The transformer losses are relatively constant over a wide range of frequency. The transistor losses, on the other hand, are sensitive to frequency and are accordingly treated in detail below.

B.1 TRANSISTOR SWITCHING LOSSES

The switching losses are determined by intrinsic switch characteristics. These characteristics are altered by drive control and load. Drive control is primarily determined by load current magnitude, and it affects switching losses only if insufficient reverse bias is provided during the switch off time. Assuming that drive control conditions are adequate, load is the only remaining parameter to affect the intrinsic characteristics of the transistor switch. Part of the real load is the power transformer, and it is examined along with load to establish the conditions during switch transfer from on to off.

The equivalent circuit seen by the transistor switch is shown in Figure B-1. Switches Q1 and Q2 are the power transistors, T is the ideal transformer, R_L is the nominal load, and the balance is the transformer impedances seen by the power switch. The transformer impedances somewhat distort the desired square wave. Further, the switches are not considered fully open or closed until the transformer is in a stable state. Thus, the transistor switching time is affected by the transformer frequency response. Note that high frequency characteristics are desireable for the transformer.

The design of transformers with high frequency response involves many factors. Their effect may be analyzed indirectly by considering switching losses over a wider range than those suggested by the transistor manufacturer.
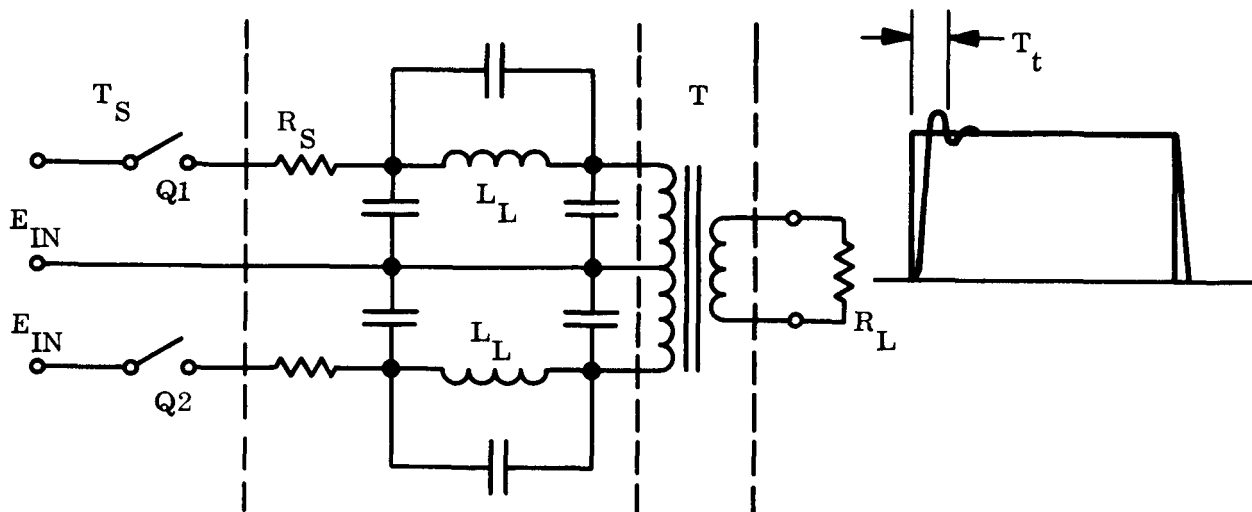
Figure B-1. Transformer Equivalent Circuit

B.2 TRANSISTOR SWITCHING DIAGRAMS

The transistor switching diagram for a push-pull configuration is shown in Figure B-2. The switch forcing function is the drive power shown in time only for Q1 and Q2. Consider that Q1 is on and the level of collector current I_c is determined by R_L. At time t_1 the drive to Q1 is removed and drive to Q2 is applied. Collector current of Q1 continues to flow due to load effects and transistor storage time, t_s. Transistor Q2 starts to turn on denoted by the fall of V_{ce} and rise of I_{c2}. Since Q1 is still on and Q2 is turning on, the high impedance normally presented by the transformer is reduced such that I_c of Q2 rises to a level determined by transistor drive current and gain. For this analysis a gain limit of two times that required is assumed. Therefore, I_{c2} rises to $2I_{c2}$ until Q1 begins to open such that the impedance presented by the transformer increases reducing I_{c2} to I_{c2} level determined by R_L. Thus, the diagram shows the relation between rise, fall, and storage time of a transistor. Note that the rise time, t_r, is a function of t_s and t_f. The switching diagram associated
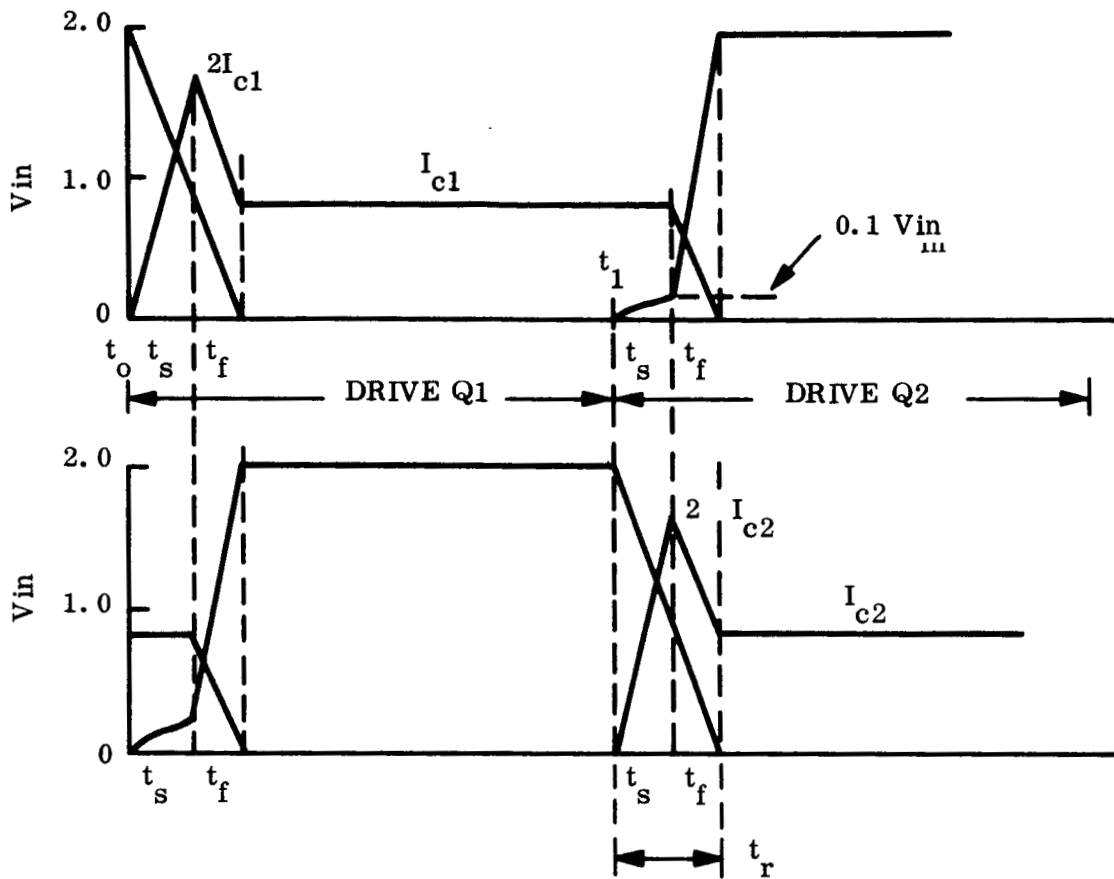
B-2

Figure B-2. Switch Voltage-Current-Time Diagram of Push-Pull Inverter

with the time diagram is Figure B-3. The power dissipated during the switching period is
then the summation of each period of t_r, t_s, t_f; where t_r is $f(t_s, t_f)$.

B.3 POWER DISSIPATION GENERAL CASE

Since the voltage-current for each time period of the diagram can be considered linear, a
general case power dissipation for each time period may be derived. Consider the general
case for linear switching shown in Figure B-4. The instantaneous current is

$$i = I_x + \left(\frac{I_y - I_x}{t_1} \right) t,$$
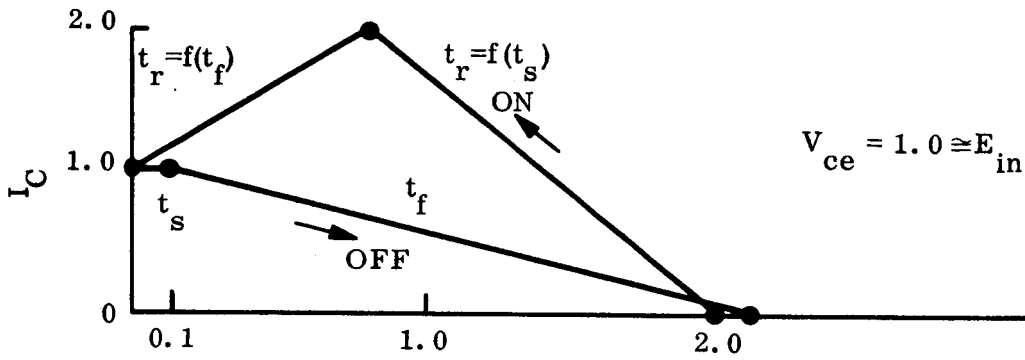
and the instantaneous voltage is
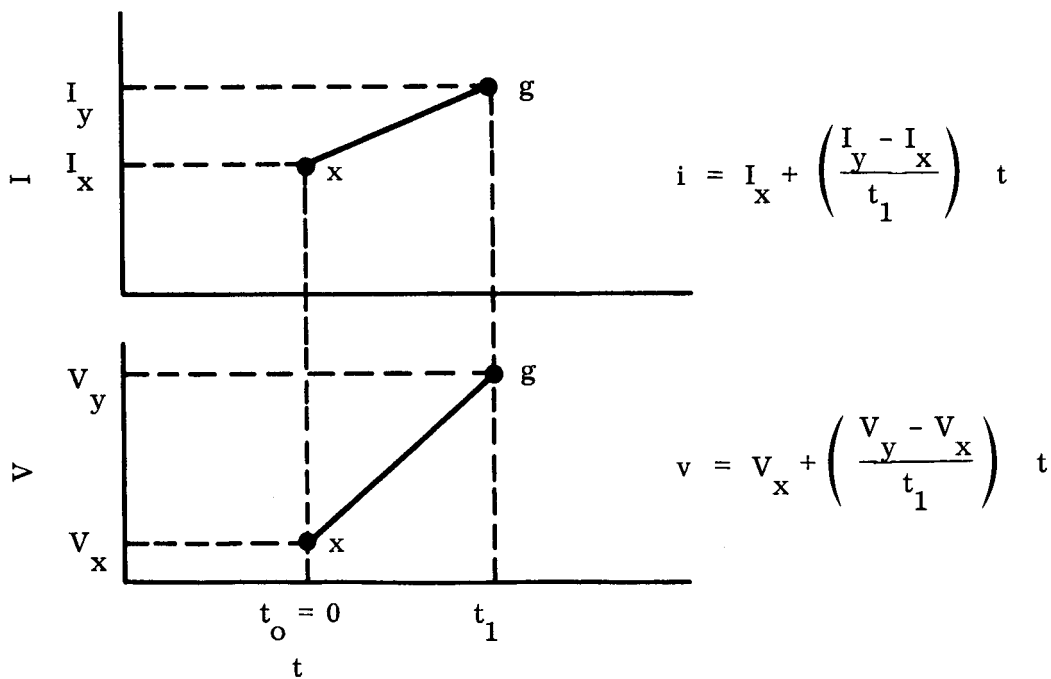
Figure B-3.   Switching Diagram

$$i = I_x + \left(\frac{I_y - I_x}{t_1} \right) t$$

$$v = V_x + \left(\frac{V_y - V_x}{t_1} \right) t$$

Figure B-4.   Linear Switching

$$v = V_x + \left(\frac{V_y - V_x}{t_1} \right) t.$$

The power for this interval is

$$P = \frac{1}{T} \int_0^{t_1} v\, i\, dt,$$

where T is the period of reoccurrance.

This equation reduces to

$$P = \frac{1}{T} t_1 \left[1/6\, (V_x I_y + V_y I_x) + 1/3\, (V_y I_y + V_x I_x) \right].$$

Thus each interval is examined using this equation and the total switching losses is a summation of each interval during period T where T is $\frac{1}{f}$ and f is frequency of operation.

B.4 DERIVATION OF TRANSISTOR SWITCH LOSS

The general equation for linear switching is

$$P = ft \left[1/6(V_x I_y + V_y I_x) + 1/3\, (V_y I_y + V_x I_x) \right].$$

Referring to Figure B-2, at Q2 turnon the rise time, t_r, is shown in two parts. The first is shown related to storage time, t_s, and the second is shown related to fall time, t_f. Power loss during this time period is

$$P_r = f(t_s) + f(t_f) = P_r (t_s + t_f).$$

Since V_{ce} nearly equals $2V_{in}$ when the transistor is off, V_{in} is used for clarity because V_{ce} appears later when the transistor is on. For the switching period calculations the transistor $V_{ce_{SAT}}$ is considered zero since the error is much less than one percent.

The power loss during rise time is as follows:

P_r (Part 1)

$$P_r(t_s) = f t_s \left[1/6 \left(2V_{in} \, 2I_c + 0\right) + 1/3 \left(2V_{in} \, \frac{t_f}{t_s + t_f} \, 2I_c + 0\right) \right]$$

$$P_r(t_s) = f V_{in} I_c \left(2/3 \, t_s + 4/3 \cdot \frac{t_s t_f}{t_s + t_f} \right)$$

P_r (Part 2)

$$P_r(t_f) = f t_f \left[1/6 \left(2V_{in} \, \frac{t_f}{t_s + t_f} \, I_c + 0\right) + 1/3 \left(0 + 2V_{in} \, \frac{t_f}{t_s + t_f} \, 2I_c\right) \right]$$

$$= f V_{in} I_c \left(1/3 \, \frac{t_f^2}{t_s + t_f} + 4/3 \, \frac{t_f^2}{t_s + t_f} \right)$$

$$P_r(t_f) = f V_{in} I_c \left(2/3 \, t_s + 4/3 \, \frac{t_s t_f}{t_s + t_f} + 5/3 \, \frac{t_f^2}{t_s + t_f} \right).$$

Power loss during the storage time is $P_s(t_s)$.

$$P_s = f t_s \left[1/6 \left(0 + 0.1 \, V_{in} I_c\right) + 1/3 \left(0.1 \, V_{in} I_c + 0\right) \right]$$

$$P_s = f V_{in} I_c \left(0.05 \, t_s\right)$$

Power loss during the fall time is $P_f (t_f)$.

$$P_f = f t_f [1/6 (0 + 2V_{in} I_c) + 1/3 (0 + 0.1 V_{in} I_c \rightarrow 0)]$$

$$P_f = f V_{in} I_c (1/3 t_f) .$$

The total switch losses are

$$P_{sw} \text{ loss } = P_r + P_s + P_f \equiv$$

$$P_{sw} \text{ loss } = f V_{in} I_c [0.71 t_s + 4/3 \frac{t_s t_f}{t_s + t_f} + 5/3 \frac{t_f^2}{t_s + t_f} + 1/3 t_f] \qquad \text{(B-1)}$$

This power loss due to switching is described by f, V_{in}, I_c, t_s, t_f. (Note that this loss occurs twice per cycle.)

Note that if frequency increases, the percent time that the transistor is on becomes less. Therefore, in order to supply the same average load current the peak collector current I_c must increase as frequency increases. The derived factor for this is,

$$\left[\frac{1}{1 - 4f (t_s + t_f)} \right] \qquad \text{(B-2)}$$

B.5 COLLECTOR CURRENT FREQUENCY CORRECTION

In terms of transistor efficiency as a function of frequency where the average current is a constant and the percent of on time decreases due to fixed switch time and shorter on time, I_c increases as a function of frequency to maintain the average current.

$$I_{AVE} = K_A \equiv \text{Constant per load requirements}$$

$$I_{AVE} = I_c \text{ at frequency equal to zero}$$

then $I_{AVE} = K_f I_c$ at frequency greater than zero, where K_f is a factor which changes as a function of frequency causing I_c also to change in order to maintain a constant I_{AVE}. The factor K_f is determined by reference to Figure B-5 and the following text.

For simplicity it is assumed that no power is delivered to the load during the periods $(t_s + t_f)$. Then

$$I_{AVE} = \frac{\frac{1}{2f} - 2(t_s + t_f)}{\frac{1}{2f}} I_c$$

where:

$$\frac{\frac{1}{2f} - 2(t_s + t_f)}{\frac{1}{2f}} \equiv K_f .$$

K_f simplified is $1 - 4f(t_s + t_f)/1$.

If K_f decreases as a function of frequency I_c must increase as a function of frequency by the inverse of K_f in order to maintain a constant I_{AVE}. Thus, I_c is corrected for frequency by

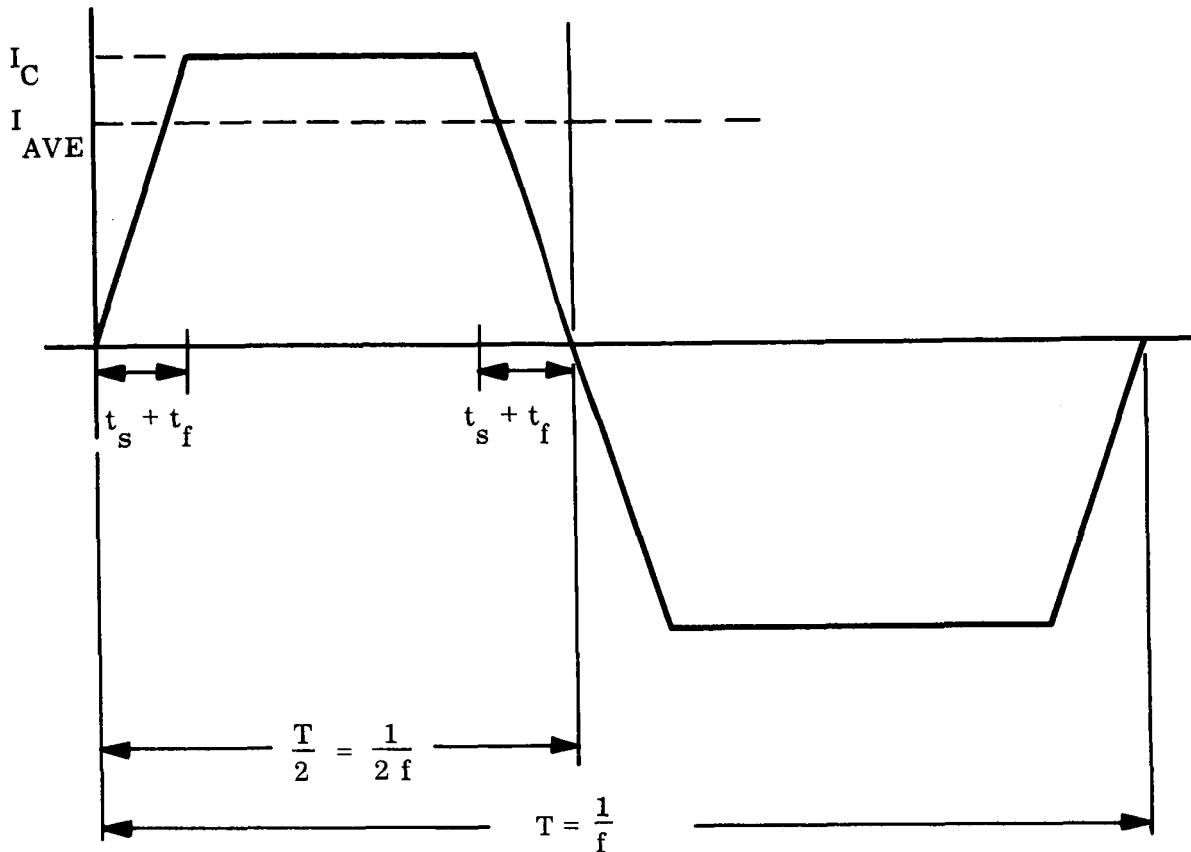$$\left[\frac{1}{1 - 4f(t_s + t_f)} \right] .$$

B-8

Figure B-5. Inverter Collector Current-Time Diagram

Note that if the peak I_c increases then the base drive must correspondingly increase, therefore the base drive must also be adjusted by the same factor. Note also that saturation losses increase by the same factor and is accordingly adjusted.

The inverter efficiency is

$$\eta = \frac{P \text{ output}}{P \text{ output} + \text{Transformer loss} + \text{Transistor loss}} \quad ,$$

$$\eta = \frac{P_o}{P_o + (0.05) P_o + \text{Transistor loss}} \quad , \text{ with a 95 percent efficient transistor}$$

$$\eta = \frac{1}{1.05 + \dfrac{\text{transistor loss}}{P_o}} \quad .$$

Knowing transistor losses permits calculation of efficiency.

Transistor losses are

$$P_{total} = 2P_{sw} + P_{drive} + P_{sat}$$

where:

P_{sw} = EQ $\underline{1}$,

P_{drive} = 0.025 P_o, and

P_{sat} = $V_{ce_{SAT}} I_c$ where P_{sw}, P_{drive}, P_{SAT} are corrected by multiplying by EQ $\underline{2}$ since all are related to I_c.

A computer program was prepared where t_s, t_f, V_{ce}, I_c, $V_{ce_{SAT}}$, P_o are inputs, f is varied from 400 Hz to 11,000 Hz, and outputs are P_{sw}, P_{drive}, P_{SAT}, P_{total}, EFF (η). A computer printout for two cases are in Table B-1.

Table B-1. Computer Printout for Inverter Efficiency as a Function of Frequency

```
READY
$FORT
```

CALCULATION OF TRANSISTOR SWITCHING LOSSES

TS	TF	VIN	IC	VCE	PL= 5	3	55.3	4	.7	200

F	PSW	PSAT	PDRIVE	PTOTAL	EFF
400.0	0.079	2.804	7.409	10.371	0.908
1000.0	0.198	2.809	7.424	10.623	0.907
1500.0	0.297	2.814	7.436	10.844	0.906
2000.0	0.397	2.818	7.448	11.060	0.905
2500.0	0.497	2.823	7.460	11.276	0.904
3000.0	0.597	2.827	7.472	11.494	0.903
3500.0	0.698	2.832	7.484	11.712	0.902
4000.0	0.799	2.836	7.496	11.930	0.901
5000.0	1.002	2.846	7.520	12.370	0.899
7000.0	1.412	2.864	7.570	13.258	0.896
9000.0	1.827	2.883	7.619	14.157	0.892
11000.0	2.248	2.902	7.670	15.069	0.889

TS	TF	VIN	IC	VCE	PL= 15	10	55.3	4	.7	200

F	PSW	PSAT	PDRIVE	PTOTAL	EFF
400.0	0.254	2.811	7.439	10.749	0.906
1000.0	0.639	2.828	7.475	11.582	0.903
1500.0	0.964	2.843	7.513	12.283	0.900
2000.0	1.292	2.857	7.551	12.992	0.897
2500.0	1.623	2.872	7.590	13.708	0.894
3000.0	1.958	2.887	7.629	14.431	0.891
3500.0	2.296	2.902	7.668	15.162	0.888
4000.0	2.638	2.917	7.708	15.900	0.885
5000.0	3.332	2.947	7.789	17.400	0.880
7000.0	4.765	3.011	7.957	20.497	0.868
9000.0	6.260	3.077	8.132	23.730	0.856
11000.0	7.824	3.146	8.315	27.108	0.843

APPENDIX C

RECTIFIER SWITCHING LOSSES

Using the general equation for linear switching derived in Appendix B, the diode rise and fall time losses are derived with reference to Figure C-1 as follows:

The rectifier voltage-current curve shows that very little power is lost in the diode during the rise time. The primary power loss is during the fall time, which is the diode recovery time.

$$P = ft \left[1/6 \left(V_x I_y + V_y I_x \right) + 1/3 \left(V_y I_y + V_x I_x \right) \right]$$

$$P_f = ft \left[1/6 \left(0 + V_R I_D \right) + 1/3 \left(0 + 0 \right) \right]$$

$$P_f = f V_R I_D \, 1/6 \, t_{rec},$$

where

P_f is power rectifier switching loss in watts.

t is time

f is frequency

V_R is reverse voltage seen by rectifier

I_D is forward current at time of switching off

t_{rec} is recovery time of rectifier.

Total rectifier losses are

$$P_{total} = P_{forward} + 2P_f,$$

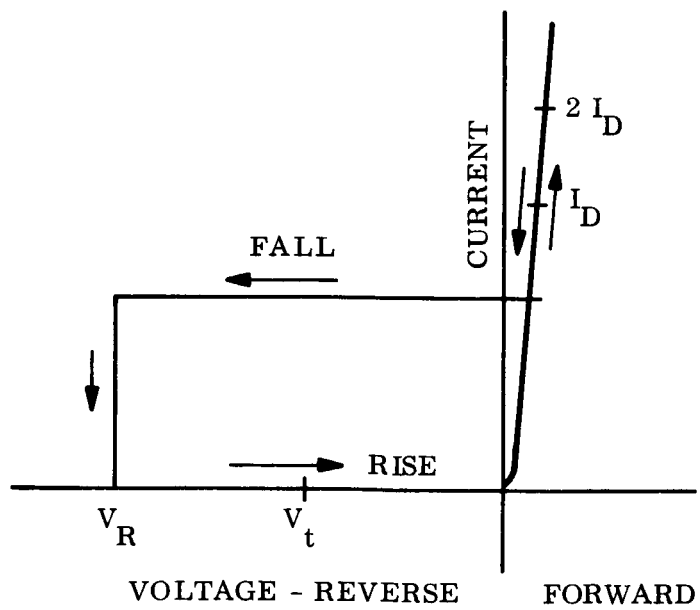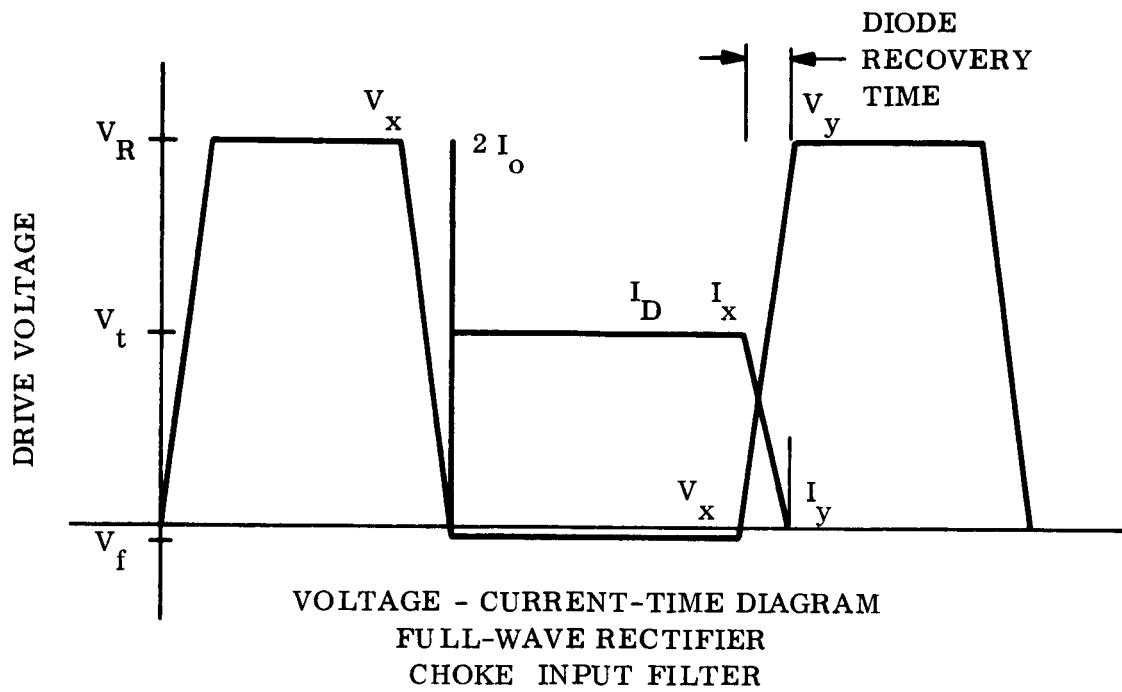$$P_{total} = V_f I_d + 1/3 \, f \, V_r I_d t_{rec},$$

where V_f is forward voltage drop.

Figure C-1. Rectifier Switching Characteristics