MODELING INTEGRATED CIRCUITS PUTING

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I. INTRODUCTION

Modeling procedures are being developed to describe the characteristics of integrated circuits for computer analysis and design. These models apply to planar diffused, thin and thick film, MOS and hybrid IC's. They depend to a large extent upon how well components are isolated from each other in the same circuit. For example, when a transistor is fabricated on a substrate and is well isolated from the remainder of the circuit, the model would be identical to the discrete transistor model. However, more commonly, there is considerable interaction between elements of an IC, either at boundaries or through the substrate. These interactions, usually distributed in nature, require the use of approximation techniques to predict the performance of the circuit. The problem of obtaining and using IC models is additionally complicated by nonlinear and high frequency effects.

Development of analysis and design techniques including all of these factors is prohibitively difficult, even with the aid of a computer. The speed and storage capacity of a computer are used most efficiently when a suitable model has been selected based upon good engineering judgement. Procedures for modeling the geometrical and material structure of IC's must therefore be based upon a compromise between accurate representation of the physical processes and simplification through approximation techniques which distinguish clearly between first order and higher order effects.

The IC modeling procedures described in this paper are both a review of those presently employed in available computer programs and newly proposed techniques which appear promising for future programs. This includes a description of the commonly used elemental-equivalent modeling technique as well as approaches which retain the distributed nature of the IC structure. Lumped-parameter modeling of IC's, which proceeds directly from the material and geometrical characteristics of the structure, is developed and applied to model a typical integrated circuit component. Modeling of MOS integrated circuits, which are finding wide application in large arrays, is described in this paper as well as models of thin and thick film integrated circuits.

II. PLANAR DIFFUSED IC MODELS

Integrated circuits fabricated by the planar diffusion process result in components defined within a single crystalline substrate by regions of alternate doping and are electrically isolated by either reverse-biased PN junction boundaries or dielectric regions.[1] In the dielectrically-isolated planar-diffused IC, leakage currents between circuit elements are minimized and these elements may therefore be represented by discrete equivalent circuit models with capacitors placed between appropriate terminals to represent displacement currents.[2] However, when reverse-biased PN junctions are employed to isolate circuit components, the model must include the parasitic effects of these junctions.

A typical PN junction-isolated IC is shown in Fig. 1. The NPN transistor fabricated in the planar diffused IC is modelled by two discrete transistors--an intrinsic NPN that represents the desired transistor and a PNP that represents the parasitic junction effects. The intrinsic transistor is drawn in solid lines while the parasitic transistor, drawn in dashed lines, has its collector labeled substrate. Each of these devices is modelled according to its discrete equivalent circuit, depending on the signal amplitude and frequency of operation.[2] The diode, resistor and capacitor are modelled in a similar fashion, with their parasitic elements. The equivalent circuit of an IC gate modelled in this manner is illustrated in Fig. 2.

For greater accuracy over a wider range of operation, a distributed model is useful.[3] Consider the diffused resistor in Fig. 3. In the model, Fig. 4, ρ is the resistance per unit length. The isolation junction between the P and N regions is represented by a parallel combination of ideal diodes with their associated capacitances, distributed along the junction. The parallel combination of capacitance C_s and ideal diode represents the isolation junction between the heavily doped N and substrate regions. The number of elements needed for the distributed model varies depending

on the desired accuracy. In the final model, the distributed resistance is represented by a T-section as shown in the M-stage schematic representation of Fig. 5.

An example of a distributed model of a bipolar NPN transistor is illustrated in Fig. 6 together with the model schematic.[4] Note that within each of the five regions the model is uniformly distributed. Each region of the model corresponds to its physical counterpart.

A more complex approach, the lumped-parameter method,[5], is required for circuits that operate over a wide range of environmental conditions. It is based directly on the physics of the structure and may be employed to model thermal gradients, high minority carrier level and electromagnetic, nuclear and cosmic radiation effects. The method differs from the distributed parameter technique in the way the physical structure is partitioned for modeling. Instead of dividing the structure into equivalent diodes and associated capacitances, the material is separated into non-uniform lumps, each representing a significant portion of the structure. A 3-lump model of a typical diode structure is represented in Fig. 7. Observe that the hole and electron currents entering each node divide into drift and diffusion components flowing to the next lump and the recombination and storage effects within each lump.

As an illustration of the lumped-parameter modeling technique, the device characteristics of the TJ10A diode were calculated by computer over a range of current from $5x10^{-5}$ to $5x10^{3}$ milliamperes. An iteration technique was employed to determine the electric field in the bulk region at the high injection levels of current through the junction.[6] Fig. 8 shows the results of this calculation compared with experimental data taken on the diode. Note the close agreement between the computer calculations and experimental data over approximately six orders of magnitude (low, moderate and high carrier concentrations). Above one Ampere the experimental data exhibits rapid falloff due to heating effects, which were not included in the calculations. The lumped-parameter modeling technique can be extended to include spatial-dependent effects within IC's. At present, only the NASAP[7] and SCEPTRE[8] computer programs are capable of applying the lumped models.

III. MODELING THIN AND THICK FILM IC's

Film circuits may be divided into the following categories; films on passive substrates (ceramic or glass) and films on active substrates (silicon). Film components deposited on passive substrates are well isolated from each other and may be considered as closely placed discrete components with few interactions. The only exception to this modeling guideline is for distributed RC structures, illustrated in Fig. 9. The model for this structure, shown in Fig. 10, is a finite transmission line with distributed resistance and capacitance.[9] The describing parameters for distributed RC structures are transcendental functions which can be manipulated readily by computer.[10]

Films on active substrates containing active devices are deposited there to reduce the interactions between components and the substrate, thereby increasing the quality of the passive components compared with planar diffused elements. Here again, the interactions are small and the components may be represented by discrete model representations. Thin-film transistors are modelled in a manner similar to the MOS-FET's described in the next section.

IV. MODELING MOS-FET INTEGRATED CIRCUITS

MOS-FET integrated circuits are being used extensively in large arrays because of their area-per-function advantage ratio of between 5 and 10 over the equivalent bipolar IC's.[11] Considerable information is available concerning the operation and models of discrete MOS devices,[12] illustrated in Fig. 11. The primary difference between discrete MOS-FET operation and their characteristics in large arrays of IC's is their interaction through the common substrate between devices.[13] The MOS-FET transfer curves (I_D as a function of V_G) shifts with respect to gate voltage V_G as the substrate is back-based. Fig. 12 shows the typical variation of threshold voltage V_{TP} with variation of substrate-to-source voltage V_B, where V_X is the effective change in V_{TP} from the V_B=0 value and K_B is an empirical fit constant.

The model for an integrated MOS transistor is shown in Fig. 13, showing the effect of substrate voltage V_B. This model may be represented in the form shown in Fig. 14, where the controlled current source is a function of the gate and substrate voltages.[14] This model was employed in calculating the response of a two-input complementary NOR gate IC.

V. CONCLUSIONS

Procedures for modeling integrated circuits are based upon a compromise between accurate representation of the physical processes

and simplification through approximation techniques. In most applications, the elemental-equivalent modeling technique, which consists of using the discrete device representations of the intrinsic and parasitic elements, is sufficient to obtain approximate response computer solutions. However, over a wider range of operating and environmental conditions, the distributed and lumped-parameter models must be employed for accurate results. Large MOS-FET arrays may be modelled for computer analysis and design by including the effect of substrate voltage on the gate threshold in the discrete device model.

VI. ACKNOWLEDGMENTS

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VII. REFERENCES

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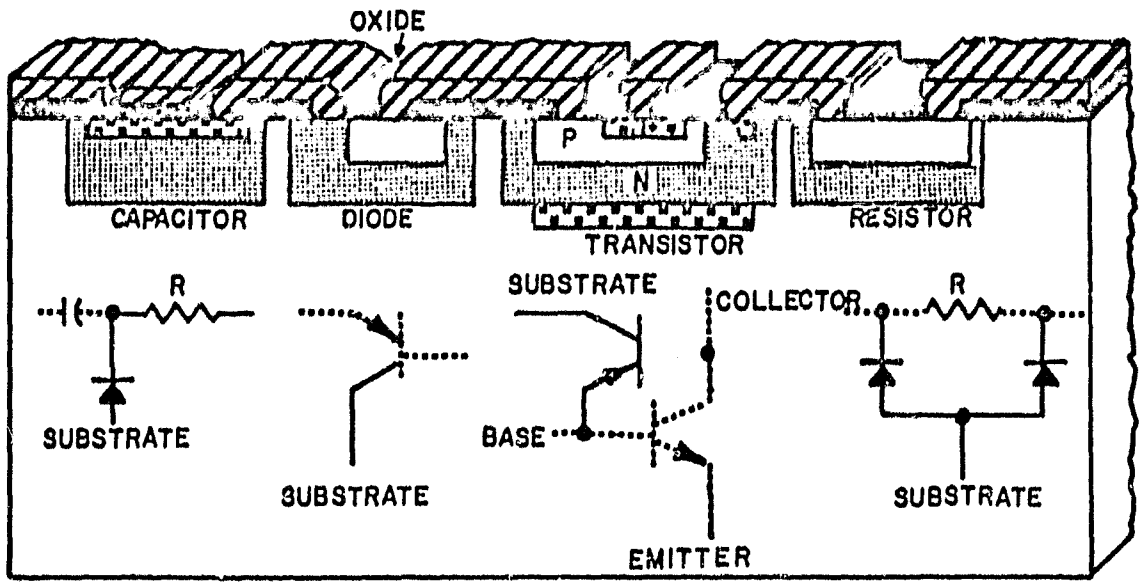
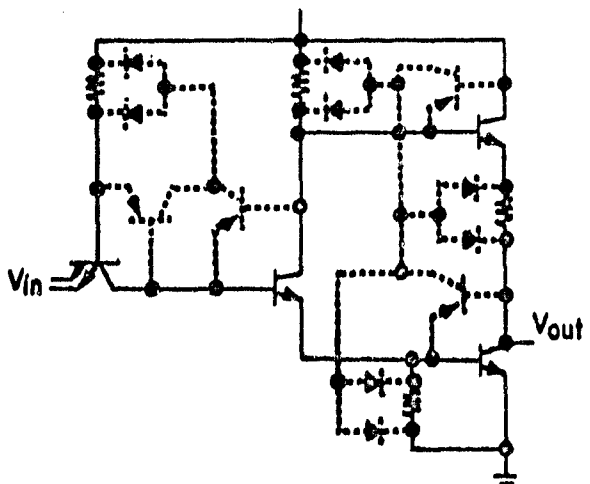


FIG. 1



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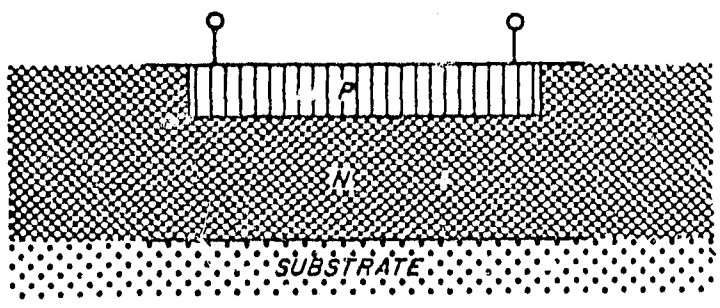

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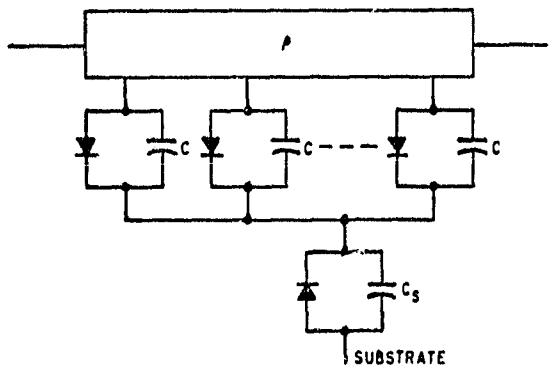

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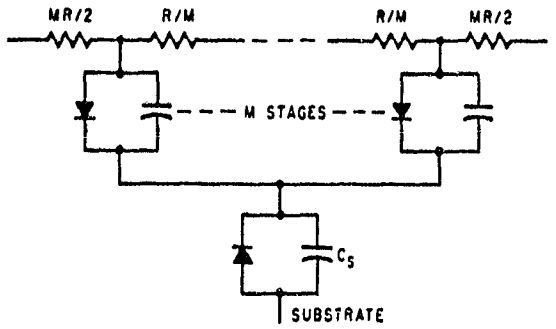

FIG. 5

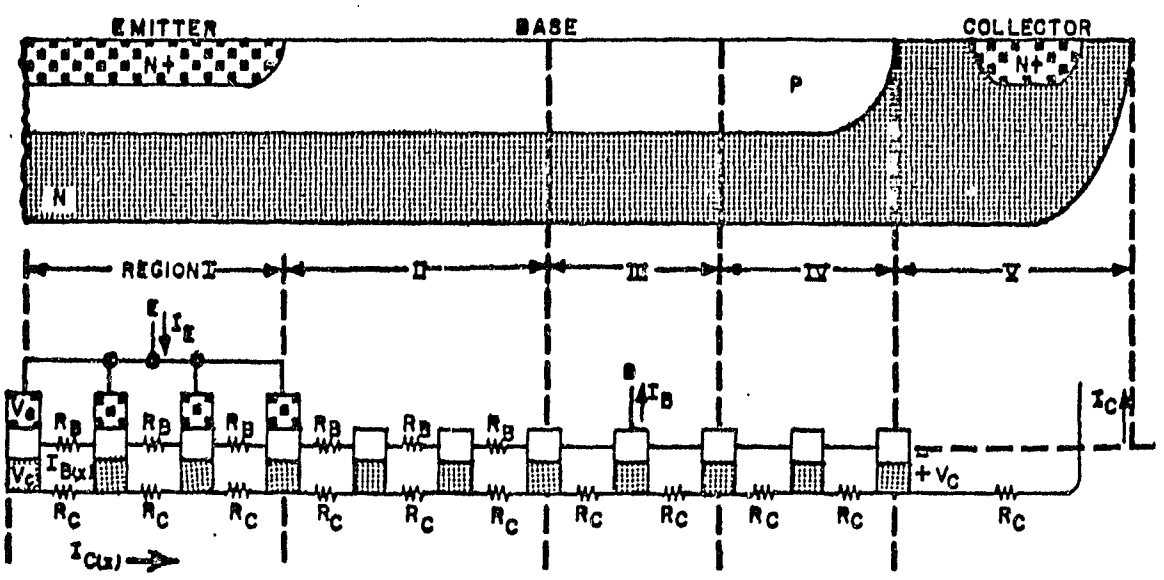

FIG. 6

FIGURES 1 AND 6
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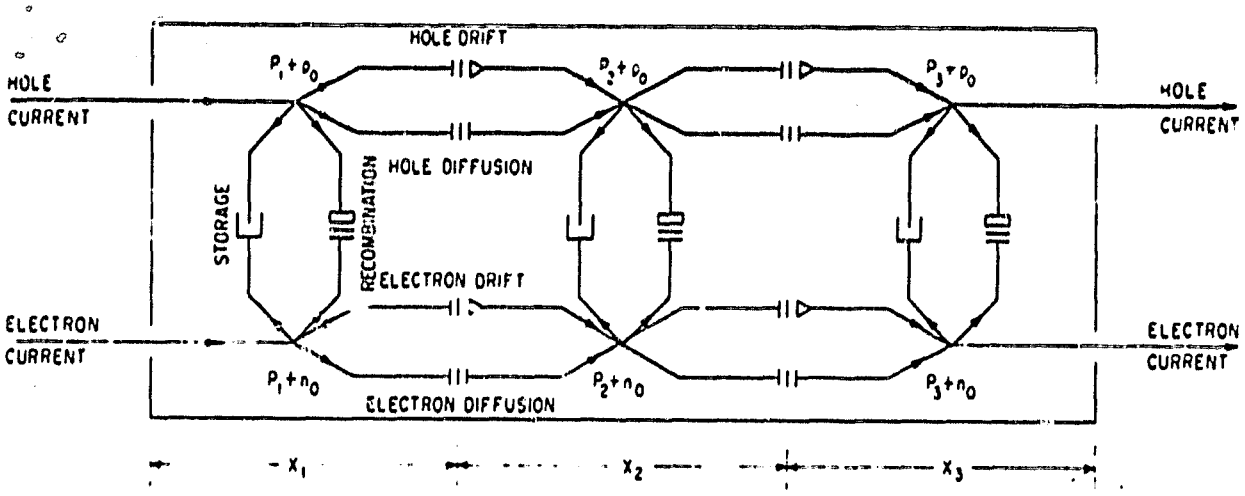


FIG. 7

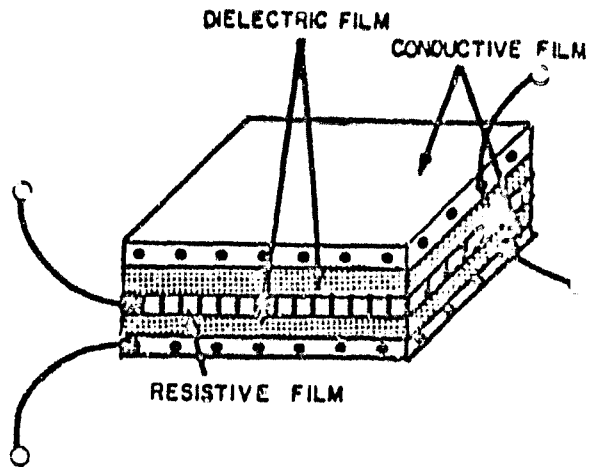
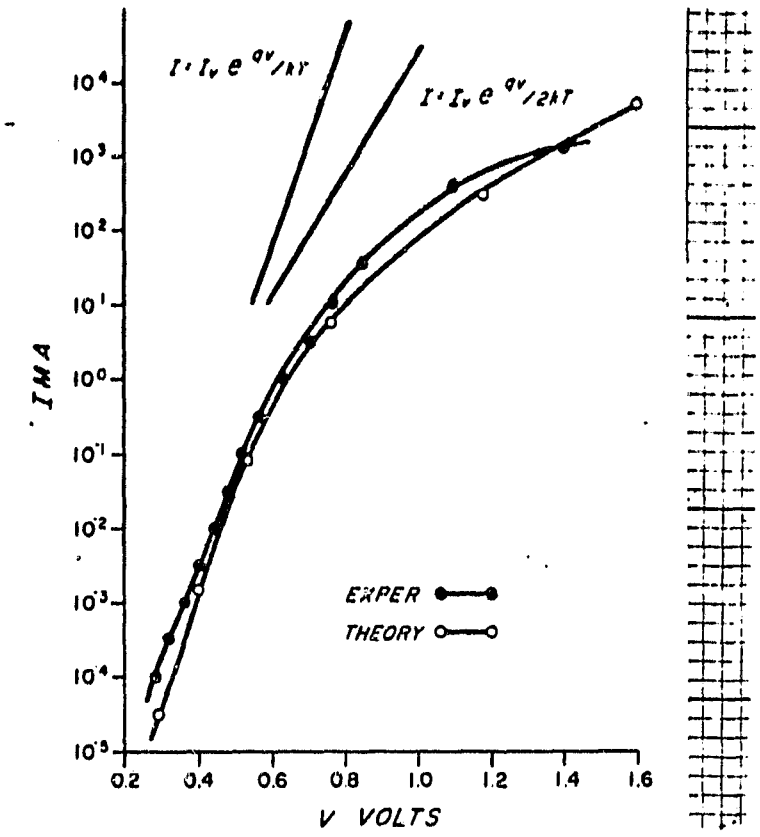


FIG. 9



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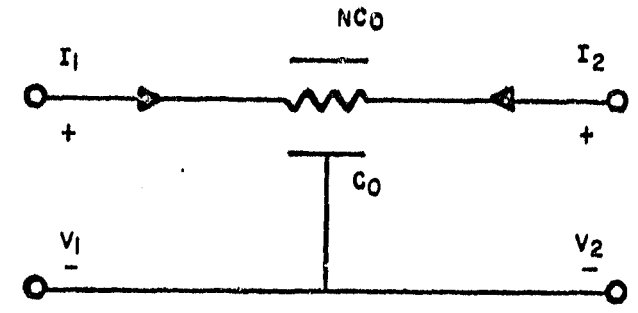

FIG. 10

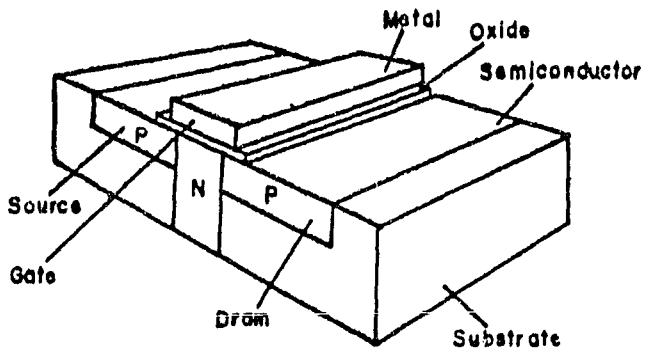

FIG. 11

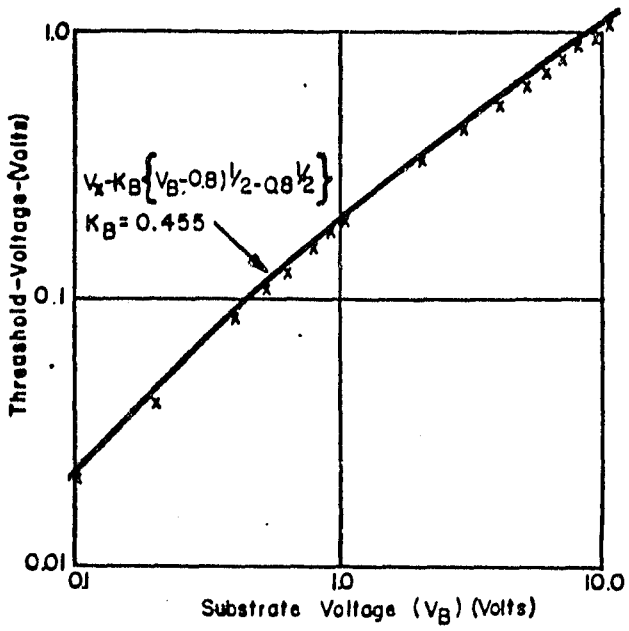

FIG. 12

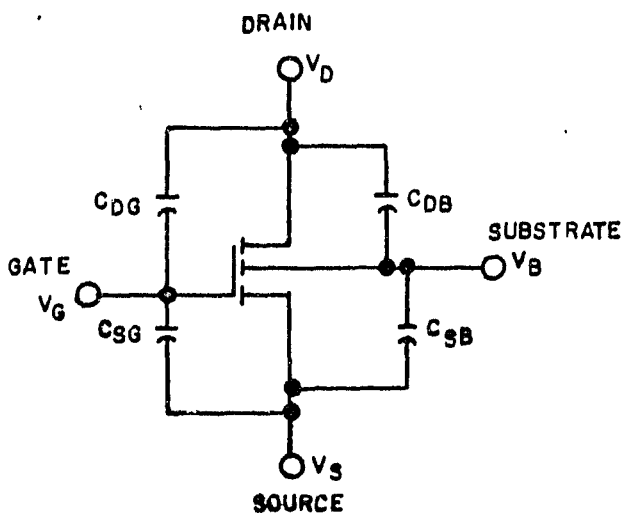

FIG. 13

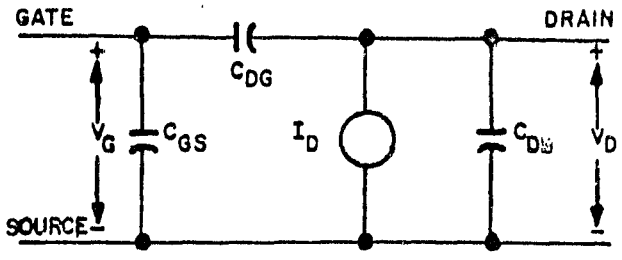

FIG. 14