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A DC-TO- PULSE-WIDTH CONVERTER

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ABSTRACT

An analytical design method is presented for a DC-TO- Pulse-Width converter with good linearity over a wide temperature range. The transfer-characteristic curve of the converter can be varied to minimize the zero offset by a relatively simple resistor adjustment. This converter may be used in analog-to-digital converter applications.

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A DC-TO- PULSE-WIDTH CONVERTER

1.0 INTRODUCTION

The purpose of this report is to discuss the operation, design, and linearity of a dc-to- pulse-width converter. The converter consists of a complementary monostable flip-flop controlled by the constant current discharge of a capacitor. The circuit was breadboarded and its linearity checked over a temperature range of -20° C to +60° C. The results of these tests are included in this report.

2.0 CIRCUIT OPERATION

The schematic diagram of the dc-to- pulse-width converter is shown in Figure 1. Under these conditions, with no trigger pulse applied, transistors Q_3 and Q_4 are OFF; diode D_1 is reverse-biased; and capacitor C_T is charged to the input analog voltage.

When the input trigger pulse is applied to the base of transistor Q_8, the complementary monostable flip-flop switches to the opposite state, thereby initiating the linear discharge of C_T through the constant current generator, Q_1. Because the discharge rate of C_T is constant, the time required for the flip-flop to return to its original state is proportional to the voltage across C_T; and the voltage across C_T is proportional to the dc-voltage input.

Transistor Q_7 is a constant current generator. Its function is to supply a bias current to the input circuitry to overcome the diode and base-emitter voltage drops of D_2, D_3, Q_2, and Q_6.

This enables the converter to handle small dc-voltage inputs. Transistor Q_2 is an emitter-follower that prevents the input circuitry from loading the converter.

3.0 CIRCUIT DESIGN

The design of the dc-voltage-to-pulse-width converter may be divided into two major parts; digital circuitry and analog circuitry.

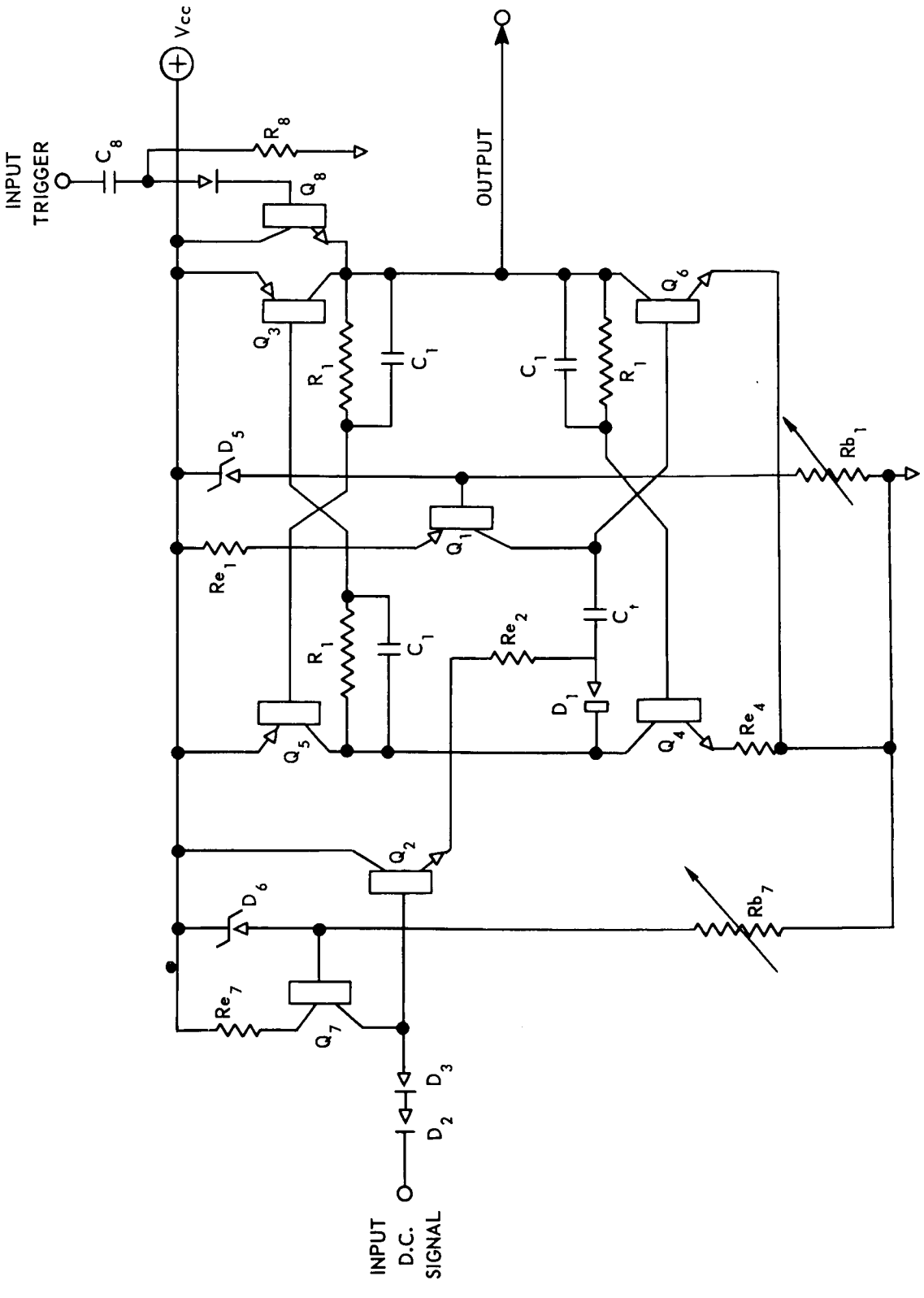

Figure 1. DC-To-Pulse-Width Converter Schematic Diagram

3.1 Digital Circuitry

The schematic diagram of a complementary flip-flop is shown in Figure 2. Any flip-flop can be made into a monostable by unbalancing the circuit. In Figure 2, if the R_1 and C_1 associated with transistor Q_4 is replaced by a time constant network, a complementary monostable flip-flop is produced. The parameters to be determined are R_1, C_1, R_L, and the minimum h_{fe} required to insure reliable operation. In the schematic diagram Figure 2, Q_3, Q_4 are ON and Q_5, Q_6 are OFF. The design equations for the parameters under worst-case conditions are:

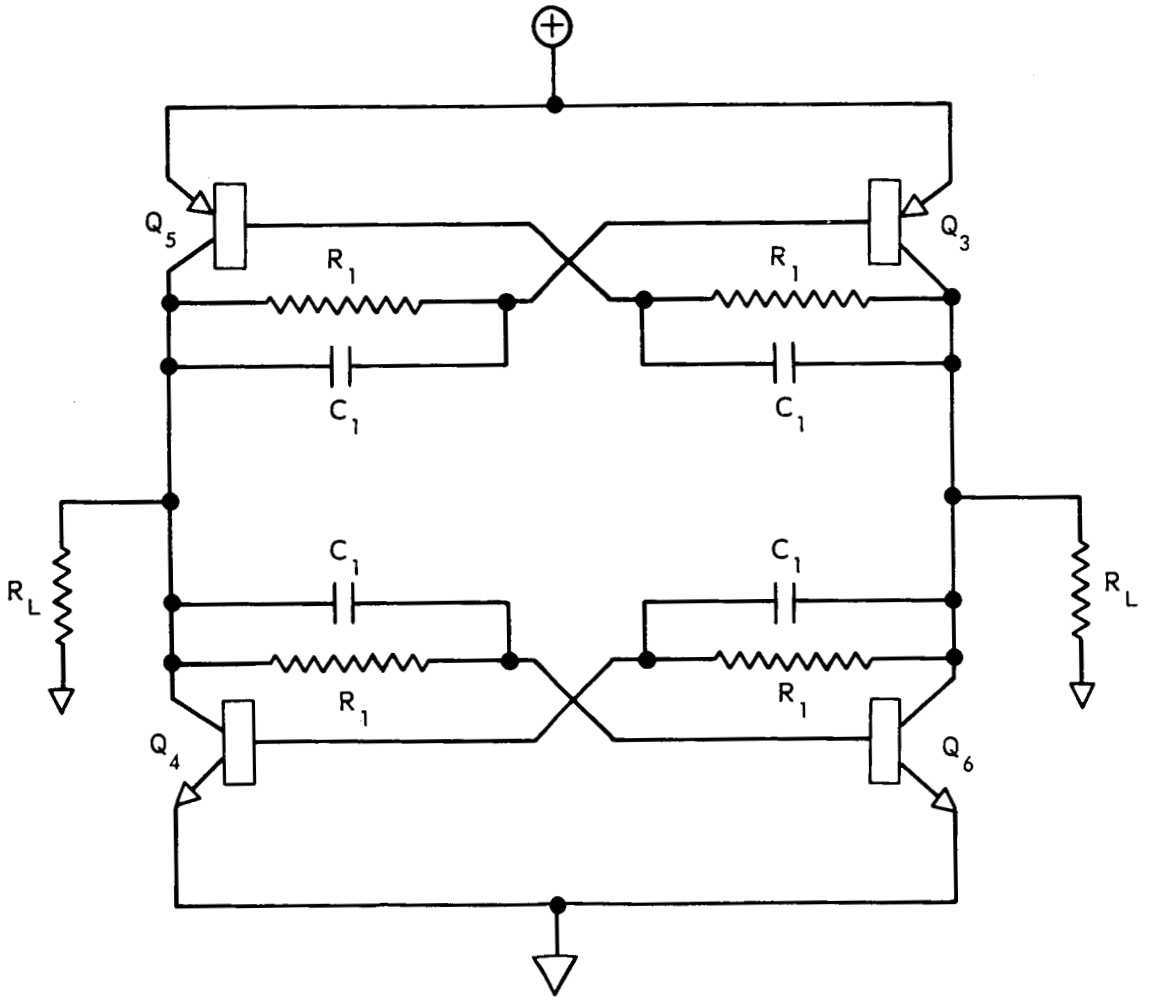

Figure 2. Complementary Flip-Flop Schematic Diagram

$$\overline{R_1} = \frac{\overline{V_{cc} - V_{bes(Q_3)} - V_{ces(Q_4)}}}{i_b}$$

$$\underline{R_L} = \frac{\underline{V_{cc} - V_{ces(Q_3)}}}{\underline{i_c}}$$

$$C_1 \leq \frac{R_1 + R_s}{R_1 \cdot R_s} \times \frac{1}{\text{max trigger frequency}}$$

$$h_{fe} = \frac{\underline{V_{cc} - V_{ces(Q_3)}}\ \overline{R_1}}{\underline{R_L}\left[\underline{V_{cc}} - \overline{V_{bes(Q_3)}} - \underline{V_{ces(Q_4)}}\right]}$$

Where:

$V_{be(Q_3)}$ equals base-to-emitter voltage drop at saturation of Q_3,

$V_{ce(Q_4)}$ equals collector-to-emitter voltage drop at saturation of Q_4,

$V_{ce(Q_3)}$ equals collector-to-emitter voltage drop at saturation of Q_3,

$V_{be(Q_4)}$ equals base-to-emitter voltage drop at saturation of Q_4,

R_s equals combined saturation resistance of Q_3 and Q_4,

f_t equals trigger frequency.

3.2 Analog Circuitry

The schematic diagram of a constant current generator is shown in Figure 3. The function of this circuit is to supply a constant current to capacitor C_T. This current source employes a zener diode for temperature compensation. The

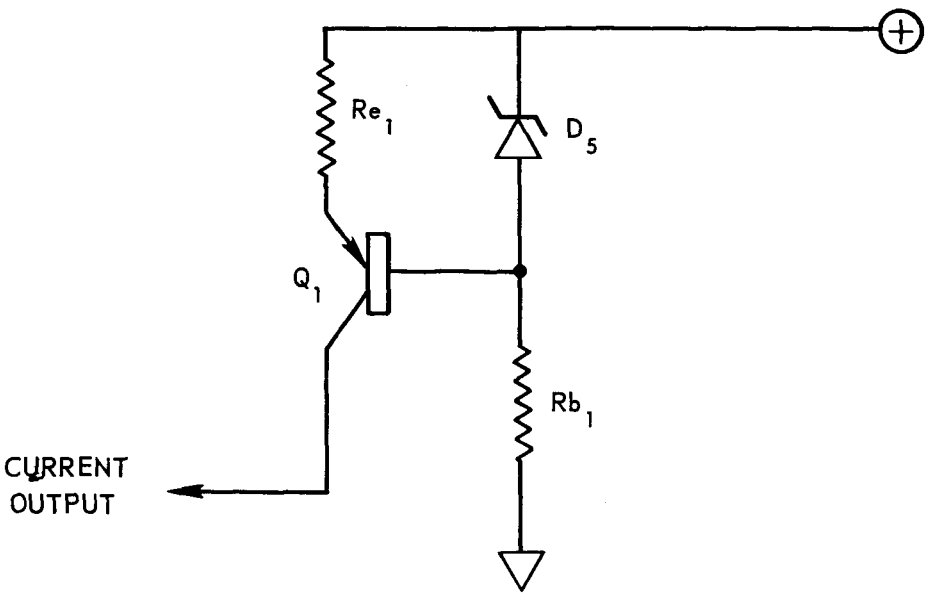

Figure 3. Constant Current Generator

zener diode characteristic must be similar to the base-emitter-diode characteristics of Q_1. If diode D_5 (Figure 3) is properly selected, the voltage across the zener may be increased, may be decreased, or may remain constant with temperature. This is the equation to be satisfied for proper zener diode selection.

Where:

δ_R equals temperature coefficient of reverse breakdown voltage,

δ_F equals temperature coefficient of forward bias function of the zener diode.

4.0 TEST AND EVALUATION

Figure 4 is a block diagram of the test setup used for checking the converter circuit. These tests include:

a. Output linearity of the converter

b. Stability of the converter as temperature is varied over a temperature range of -20°C to +60°C

c. Control of the output slope of the converter

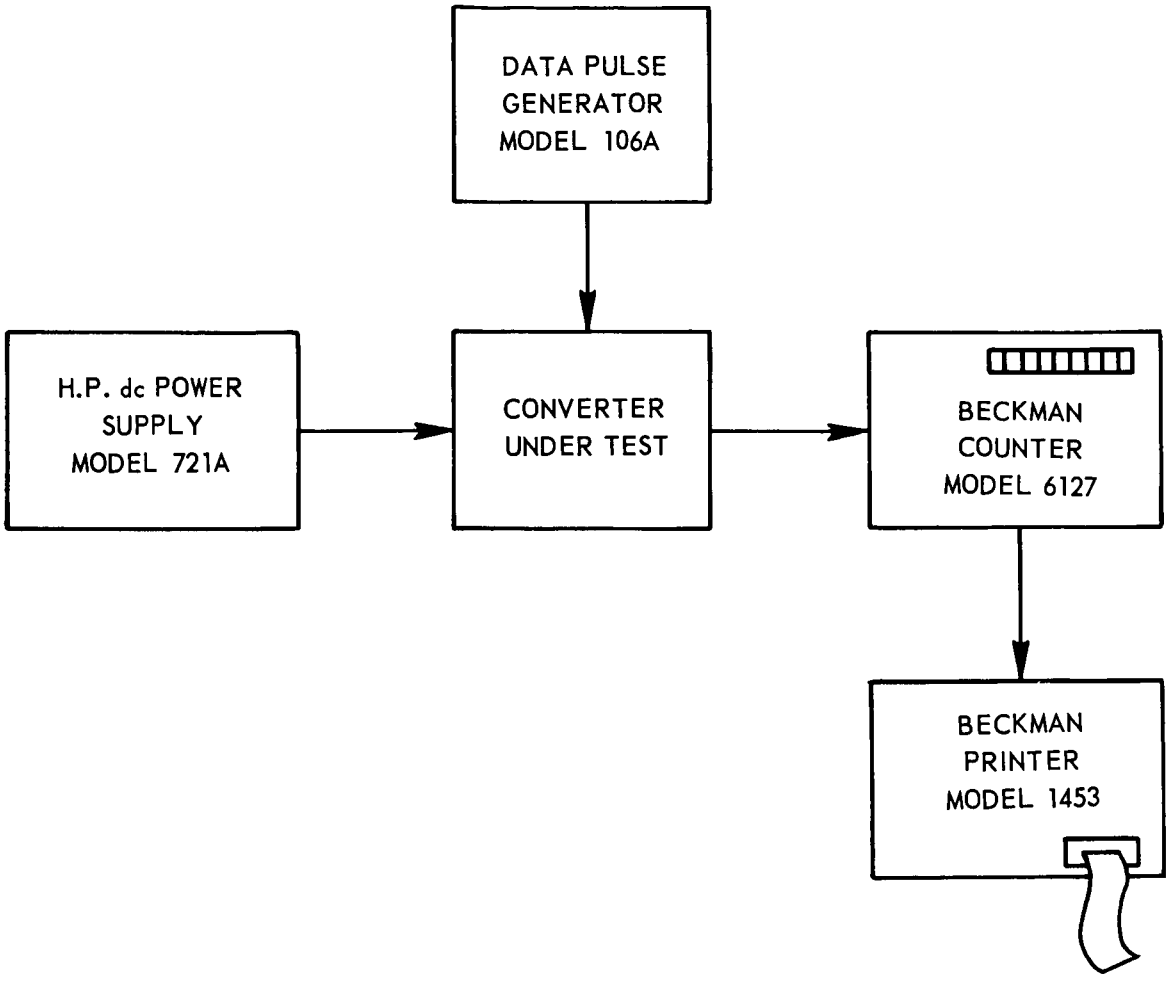

Figure 4. Test Setup for the Pulse-Width Converter, Block Diagram

4.1 Output Linearity of Converter

Linearity is defined as the percentage deviation from the best-fit straight line. Table 1 shows the output pulse width in microseconds as a function of dc-input voltage over the range from zero to 5 VDC. The equation of the line that best represents this data may be obtained by employing the method of the least square line.[2] When the dc-voltage input is X and the pulse-width output is Y, the least-square-line equation is developed from the data in Table 1:

$$Y = -3.25 + 20.25X \tag{5}$$

Table 1

Input: X	Output: Y
0.00	1.25
0.25	3.00
0.50	6.25
0.75	11.50
1.00	16.50
1.25	22.00
1.50	26.25
1.75	32.00
2.00	36.75
2.25	42.25
2.50	47.00
2.75	52.50
3.00	57.00
3.25	63.00
3.50	67.00
3.75	72.00
4.00	77.00
4.25	82.25
4.50	87.15
4.75	92.80
5.00	97.25

A plot of Equation 5 and the actual data is depicted in Figure 5.

The root-mean-square (rms) percent of deviation is 0.5 percent.

4.2 Temperature Stability of Converter

The converter was tested within a temperature range of -20° C to +60° C. The data obtained from these tests are plotted in Figure 6. The least square line equations at the temperature extremes are:

$$Y_{60°C} = -3.82 + 20.43X \qquad (6)$$

and

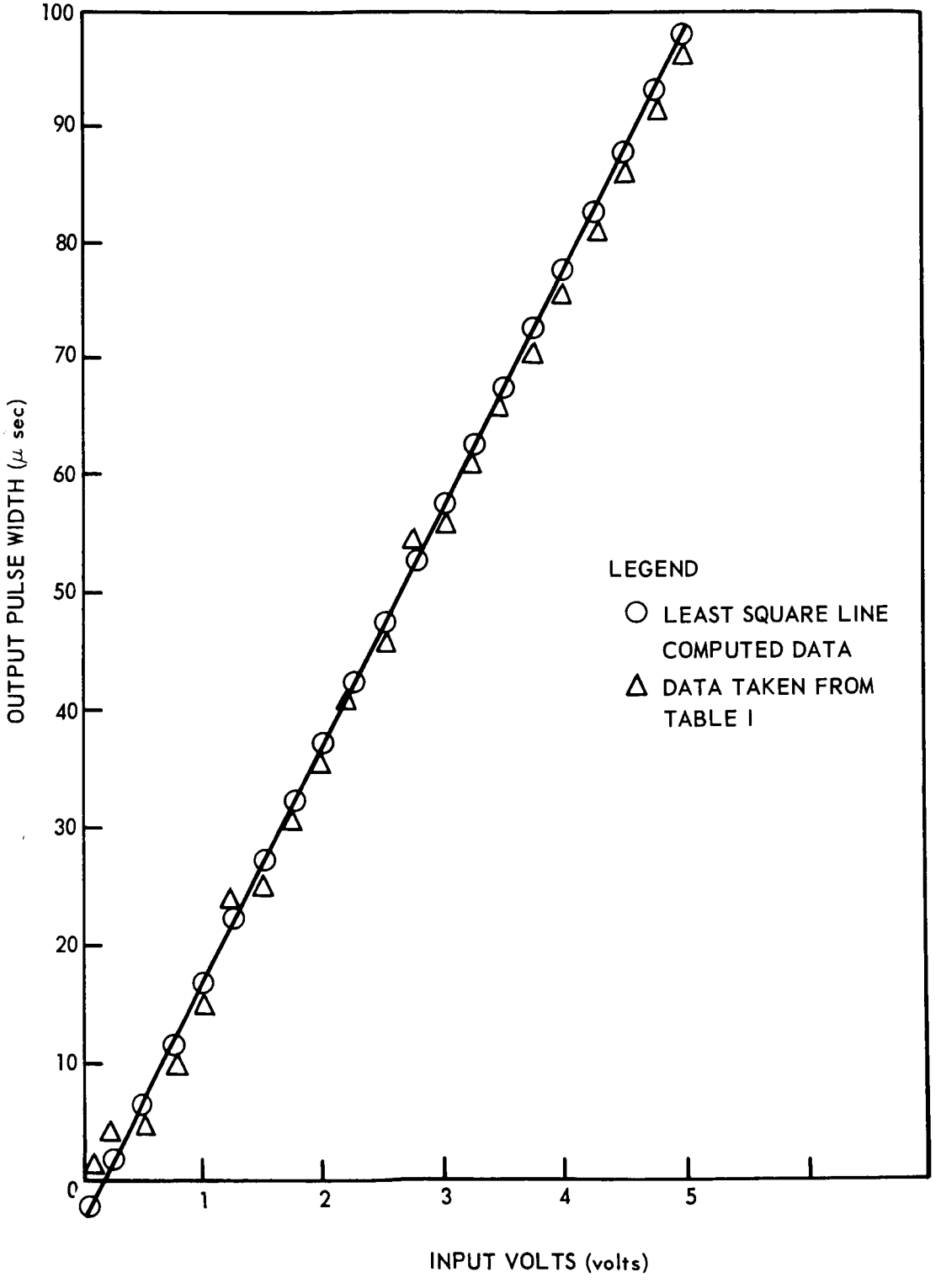

Figure 5. Least Square Line vs Actual Data Points

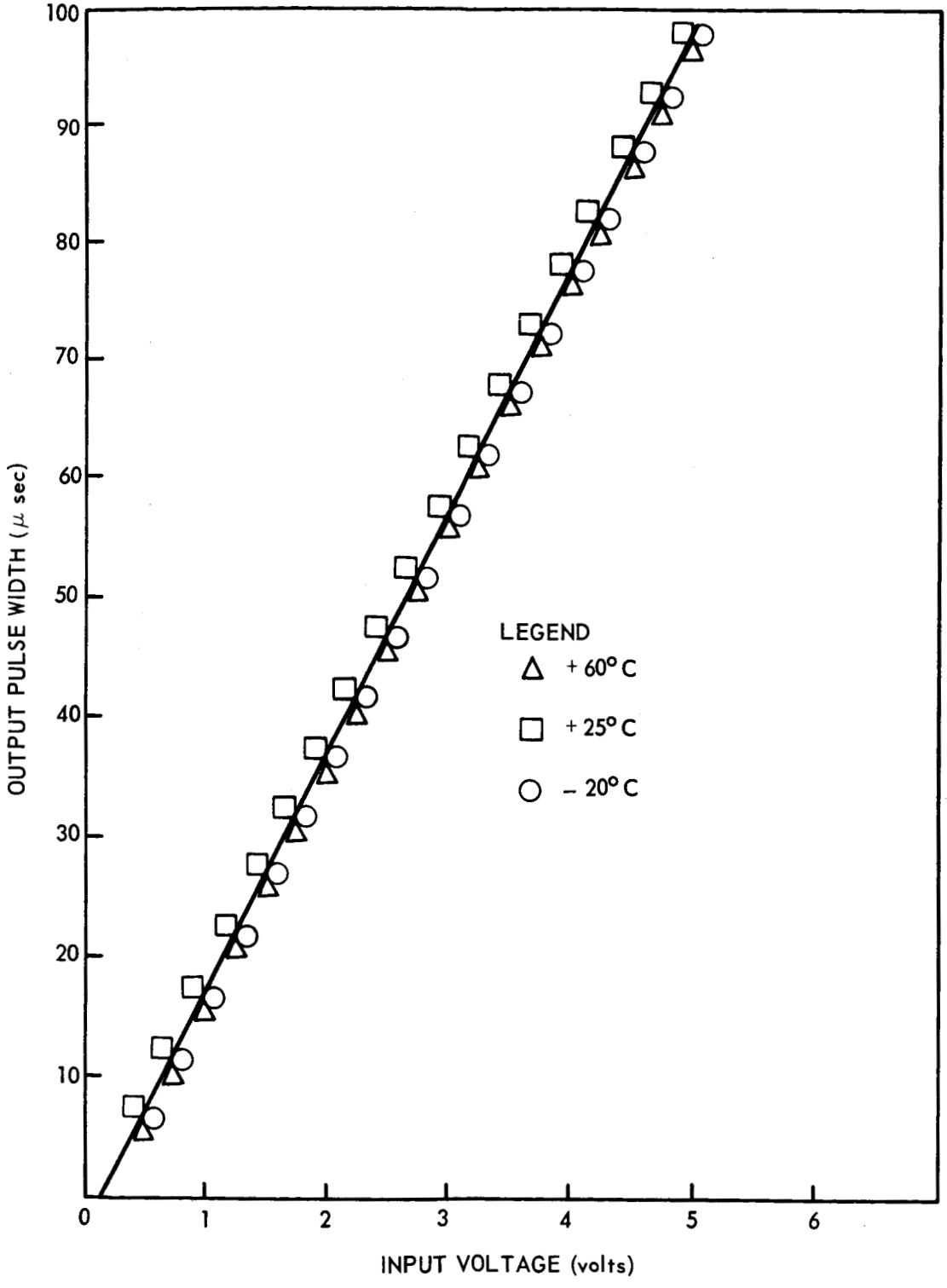

Figure 6. Linearity vs Temperature Curves

$$Y_{20°C} = -3.41 + 20.37X \quad (7)$$

The maximum rms percent of deviation due to temperature variation is less than one percent.[3]

4.3 Control of Output Slope of Converter

If the portion of the characteristic curve (shown in Figure 5) below 0.5 VDC is considered, the Y-intercept can be made to approach zero by adjusting R_{b1} and R_{b7}, shown in Figure 1. R_{b1} also controls the pulse-width output at high dc-voltage input. Figure 7 shows how the slope of the output characteristic curve is changed by varying resistor R_{b1}. When R_{b1} is equal to 20K Ω the output from the converter appears to be linear within an input voltage range from zero to 5.0 VDC; and the Y-intercept approaches zero. From Table 2, the least square line equation is:

$$Y\ 0.333 + 12.92X \quad (8)$$

Note the Y-intercept has changed from -3.25 to 0.333. From these calculations, it follows that the Y-intercept can be made equal to zero if caution is exercised in selecting R_{b1} and R_{b7}. The rms percent of deviation for the input voltage range is 0.5 percent.

5.0 CONCLUSION

The dc-voltage-to-pulse-width converter presented in this report is a combination of a complementary monostable flip-flop and a constant current generator. It has been shown that the linearity of this circuit is relatively independent of temperature variations and that the slope of the transfer-characteristic curve can be adjusted to minimize the zero offset by relatively simple resistor adjustment. These features make it particularly useful for analog-to-digital converter applications in scientific satellites where reliability and good linearity are prime requirements.

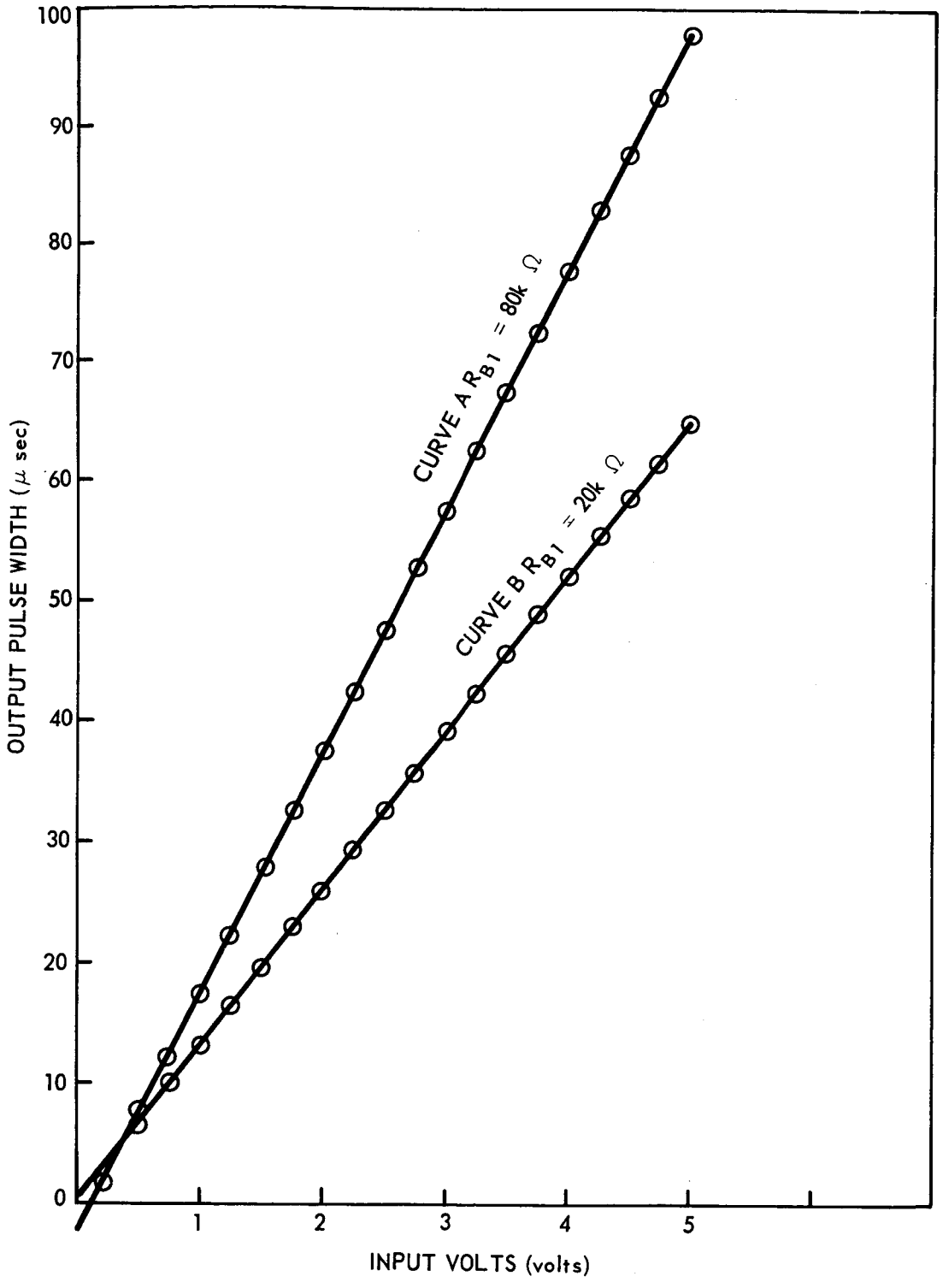

Figure 7. Variation of the Output Slope vs Variation of R_{b1} Resistor

Table 2

Input vs Output Linearity when R_{b1} is 20kΩ

Input: X	Output: Y
0.00	0.00
0.25	3.60
0.50	6.90
0.75	10.10
1.00	13.25
1.25	16.50
1.50	19.90
1.75	23.00
2.00	25.95
2.25	29.25
2.50	32.70
2.75	36.00
3.00	39.10
3.25	42.25
3.50	45.30
3.75	48.80
4.00	52.10
4.25	55.45
4.50	58.60
4.75	61.80
5.00	65.00

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