CR 86076

STUDY OF
ADVANCED ASSOCIATIVE PROCESSOR TECHNIQUES

Interim Report

by

Harvey I. Jauvtis

February 1968

Prepared under Contract NAS 12-543 by

Magnetic Memory and Logic Development Department

Electronics Division of
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SUMMARY

The application of DTPL (Domain Tip Propagation Logic) to the design of an associative processor has been studied. This report represents the results of the first six-month's work effort in which solutions to most of the basic problems have been obtained. In particular, word selection logic and memory cell structures have been designed, implemented and found to function satisfactorily. Techniques for performing the various search and processing operations required of an associative processor for spaceborne applications have been developed and methods for reducing the basic search cycle time considered. Materials and fabrication studies were undertaken in an effort to improve upon existing multilayer and laminated film techniques.

The report concludes with a preliminary design for a 1000 word, 100 bits per word DTPL associative processor. A work plan for the second half of the program is also presented.

1. INTRODUCTION

The Study of Advanced Associative Processor Techniques, Contract NASA 12-543, is a program to investigate the application of DTPL all-magnetic memory-logic techniques to the implementation of spaceborne associative processors. DTPL (Domain Tip Propagation Logic) is a newly-developed magnetic thin-film technique that utilizes controlled domain tip propagation and interaction for performing any desired memory or logic function, and thus lends itself to the realization of a wide variety of batch-fabricatable digital memory and logic devices of miniature size, low power and high speed. The combination of the various memory and logic techniques offers new and unique solutions to the problem of constructing reliable, low-cost associative processors to meet the requirements of future space vehicles.

This report represents the results of the first six months of theoretical and experimental work performed on the program. The study is divided into the following principal tasks: (1) evaluation of logic structures, (2) evaluation of memory cells and (3) memory system analysis. Task 1 is involved with the study of new DTPL logic structures which, in addition to existing elements, are required for performing such functions as address selection, film-film information transfer and conditional erase. "Evaluation of memory cells" describes the effort to determine the optimum associative memory cell configuration based upon an experimental study and comparison of the various designs that are possible with DTPL memory-logic techniques. Size, speed, control conductor pattern and logic capability are the cell characteristics which must be considered, and trade-offs between these would most likely result. In the final and most important task, memory system analysis, principal emphasis is placed on how to best achieve associative processor search (equality, inequality, maximum/minimum) and processing (field addition, operand addition) operations. The results of this study and the experiments and investigations performed in

the course of the previous two tasks should produce several approaches to the implementation of a full 1000-word, 100-bits-per-word associative processor. Analysis of the different memory array organizations in light of known ranges of requirements, e.g., adaptive data acquisition and trade-off capabilities between functional characteristics of these processors is an integral part of this task.

The following sections contain descriptions of the work performed on the aforementioned tasks. The material is presented in a manner which leads the reader from the basics of DTPL technology through memory cell design to the organization of a memory array.

To begin with, section 2 contains a review of the basic DTPL elements, the new elements and techniques developed during the program and methods of readout from a DTPL film plane. Section 3 describes the design and operation of a memory selection network in which only n input control conductors are required to select one of 2^n output channels for writing into or reading out of a 2^n word associative memory. The several associative memory cells investigated in the course of the program are discussed in section 4. These are classified on the basis of their outputs during an equality search operation i.e., output-on-match or output-on-mismatch. For each of the cell configurations, the method of performing the write, read, erase and test for match functions is illustrated. A preliminary evaluation of these designs considering such characteristics as speed, size and logic capability is presented at the end of the section.

Section 5 is devoted to the various search and processing operations required of a general-purpose associative processor. The approach taken has been to develop algorithms for accomplishing these functions in memories composed of both types of storage cells. It will become apparent from this discussion

that the output-on-mismatch cell is inherently better suited for the tasks of information transfer and comparison which are the basis of such operations. A description of the materials and fabrication studies performed during the program is presented in section 6.

The culmination of the first six months' work effort is presented in section 7 in the form of a preliminary design for a full 1000-word DTPL associative processor. The memory would be compable of meeting the functional requirements of an adaptive data acquisition system, a system potentially useful for performing a variety of tasks aboard a long-range exploratory aerospace vehicle. Included in the discussion is a description of the memory film planes, drive and sense electronics, magnetic field generating coils and a summary of the important system characteristics -- namely speed and power.

The program plan for the second half is presented in section 8.

2. DTPL LOGIC TECHNIQUES

2.1 Review of Basic Elements

A comprehensive discussion of the fundamentals of DTPL technology is presented in the proposal for this program submitted to NASA/ERC by the Applied Research Department, Electronics Division of Laboratory for Electronics, Inc.[1] For the reader who is not familiar with the material in this document, but principally for the purpose of completeness, a review of the basic elements and techniques of DTPL is seen to be in order. This subsection, then, describes the operation of pertinent channel structures and establishes the schematic representation utilized in the illustrations of logic networks, memory cells, etc., presented in the pages to follow.

Channel - The work "channel" refers to the low coercive force region embedded in the DTPL film plane of generally high coercivity which functions as a reciprocal magnetic transmission path for the propagation of domain tips. Figures 1a and 1b depict channels containing domain tips propagating in opposite directions. Associated with a channeled domain tip is an interaction field resulting from the accumulation of "magnetic charge," the origin of which is the non-zero divergence of the magnetization ($\bar{\nabla} \cdot \bar{M} = -\rho_m$) in the vicinity of the tip. The polarity of magnetic charge depends upon the direction of tip propagation with respect to the high coercive force background magnetization (see Figures 1a and 1b).

For the most part, channels are oriented parallel to the easy axis of magnetization, but deviations of up to 30° are often required to perform certain logic functions and interconnect neighboring elements. Channel widths w typically vary from .001 to .008 inches according to the requirements of tip coercivity H_t (threshold field

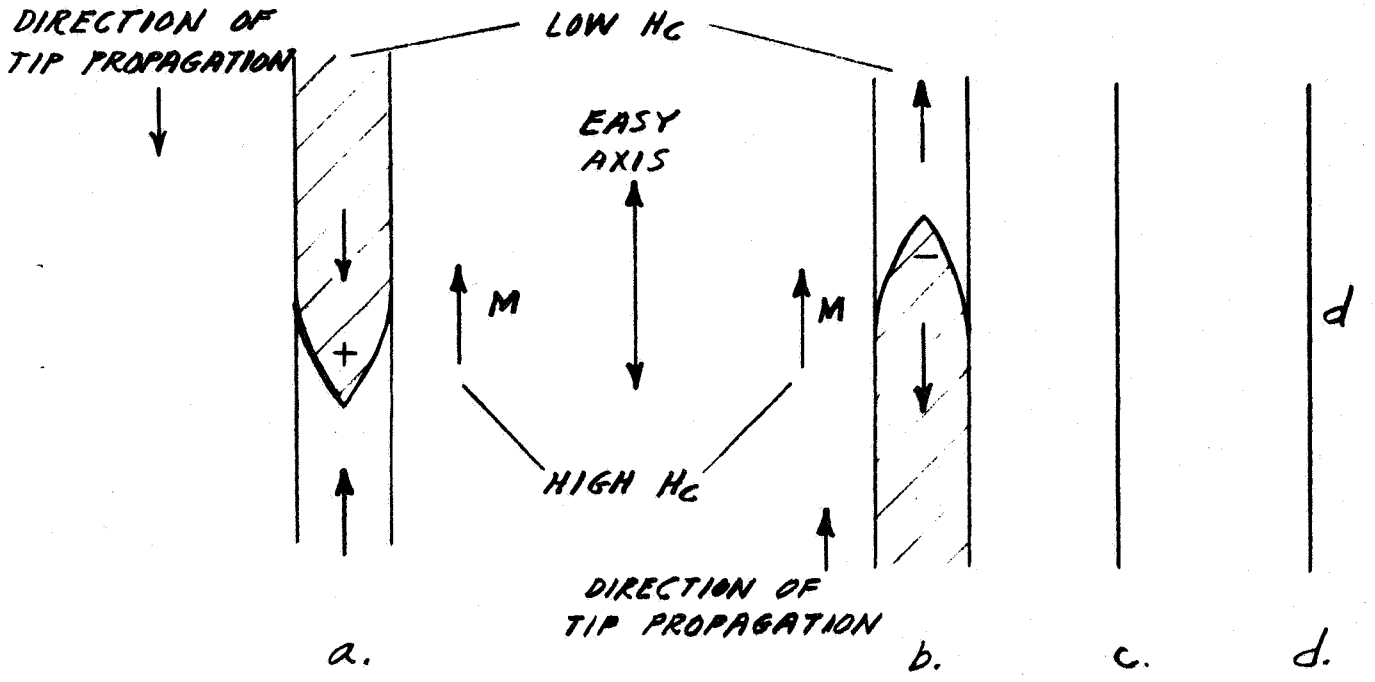


Figure 1 Channeled domain tips (a, b,) and schematic representation of channels (c, d).

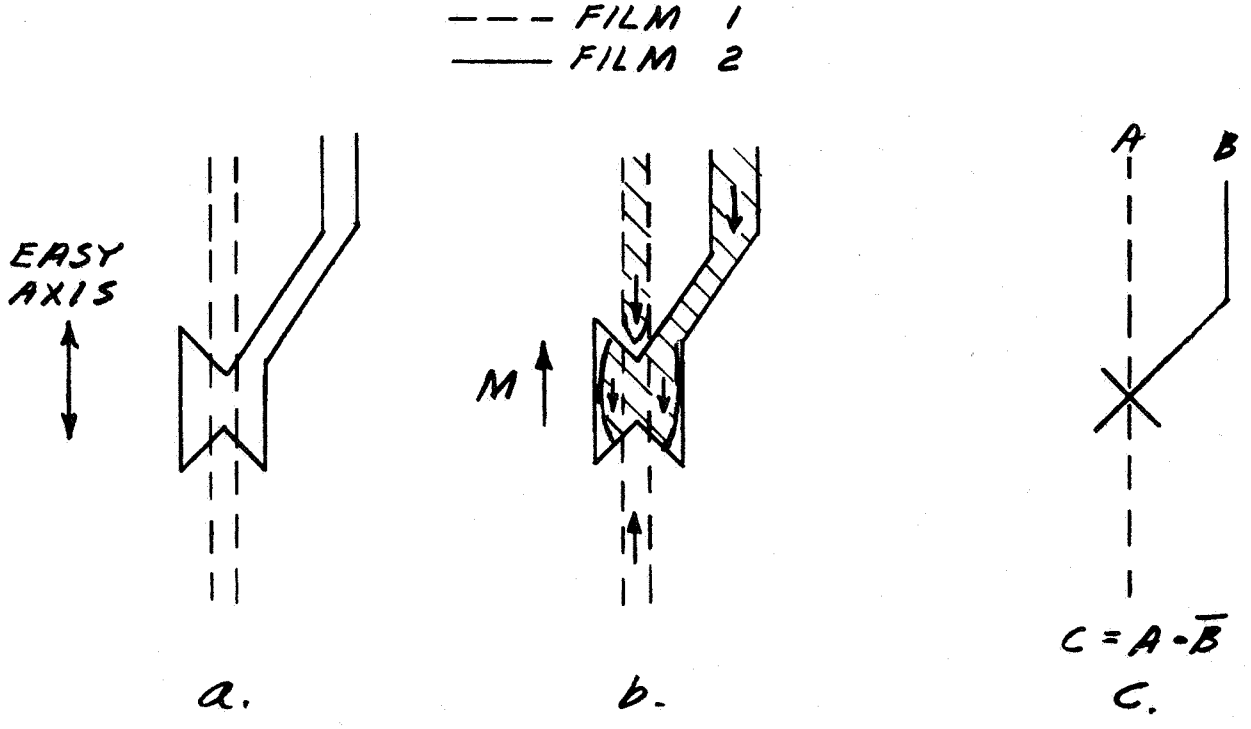


Figure 2 DTPL inhibit gate (a, b) and its schematic representation (c).

for tip propagation) and velocity v_t (a function of applied field H_A). The former is inversely proportional to channel width, i.e., $H_t \propto \frac{1}{w}$, while the latter can be expressed as $v_t\ (H_{A_{const.}}) \propto (w)^{1/2}$. This dependence of velocity upon channel width is the important characteristic which makes possible the introduction of delays into specific channels of a logic network. The schematic representation of a regular channel (.003 to .008 inches) and delay segment (.001 to .003 inches) are illustrated in Figures 1c and 1d. A more complete expression for tip velocity as a function of H_A, w and H_K (anisotropy constant proportional to the percentage of cobalt in the ternary film alloy NiFeCo) is given by

$$v_t = \left(\frac{3.5}{H_K} - .07\right)\ (H_A - 3)\ (w)^{1/2}\ \times 10^5 \text{ cm/sec} \qquad (1)$$

where the units of H_A and H_K are oersteds and w is in mils.

Inhibit Gate - The basic DTPL logic element is the inhibit gate or inverter shown in its optimum two-layer configuration in Figure 2a, and known for obvious reasons as a "hatchet gate." As illustrated in Figure 2b, the presence of a domain of reversed magnetization in the hatchet-shaped information channel, contained in one magnetic layer, creates a configuration of magnetic charges and interaction fields which inhibit tip propagation in the narrow main channel located in a second, superimposed magnetic layer. The gate will perform over a drive field range of 4-10 oe (±43% tolerance) independent of the direction of tip propagation in the main channel. The schematic representation is shown in Figure 2c where the output $C = A \cdot \overline{B}$ for input variables A and B. If the input A =1 at all times (A driven by a 1 generator), then $C = \overline{B}$ and the gate functions as an inverter i.e., $B \rightarrow \overline{B}$.

Film-Film Transfer - In order to realize complex logic networks using the two-layer inhibit gates, it must be possible to transfer information (domains of reversed magnetization) between overlying film planes. The film-film transfer element developed for such purposes is shown in Figure 3a and consists of two easy-axis, .008 inch channel segments contained in the superimposed magnetic layers and overlapped .010 inches. The entire structure is approximately .025 inches in length. Transfer from channel A to channel B is said to have occurred when a domain of reversed magnetization is nucleated in B as the direct result of the presence of a tip at the end of A (see Figure 3b). This process will only occur if the applied field H_A plus the tip stray field H_S excess the nucleation threshold in channel B. In typical film-film structures, a minimum applied field of $\tilde{=}$ 4 oe is sufficient for this operation. Figure 3c depicts the transfer element schematically.

Crossover - The principal requirement of a crossover element is that there be complete magnetic isolation between the component overlying channels. Figure 4a illustrates a suitable configuration of channels in which no film-film transfer will occur for applied fields up to 10 oe. This limit is required if the full operating range of the inhibit gate is to be realized in general two-layer networks. The operation of the crossover and its descriptive symbol are depicted in parts b and c of the figure.

Diode - The DTPL equivalent of an electronic diode is a non-reciprocal magnetic transmission path. A single-film channel configuration which permits only unidirectional tip propagation is presented in Figure 5a. Its operation is based upon two effects known as "tip steering" and "wall pinning." The former makes possible the

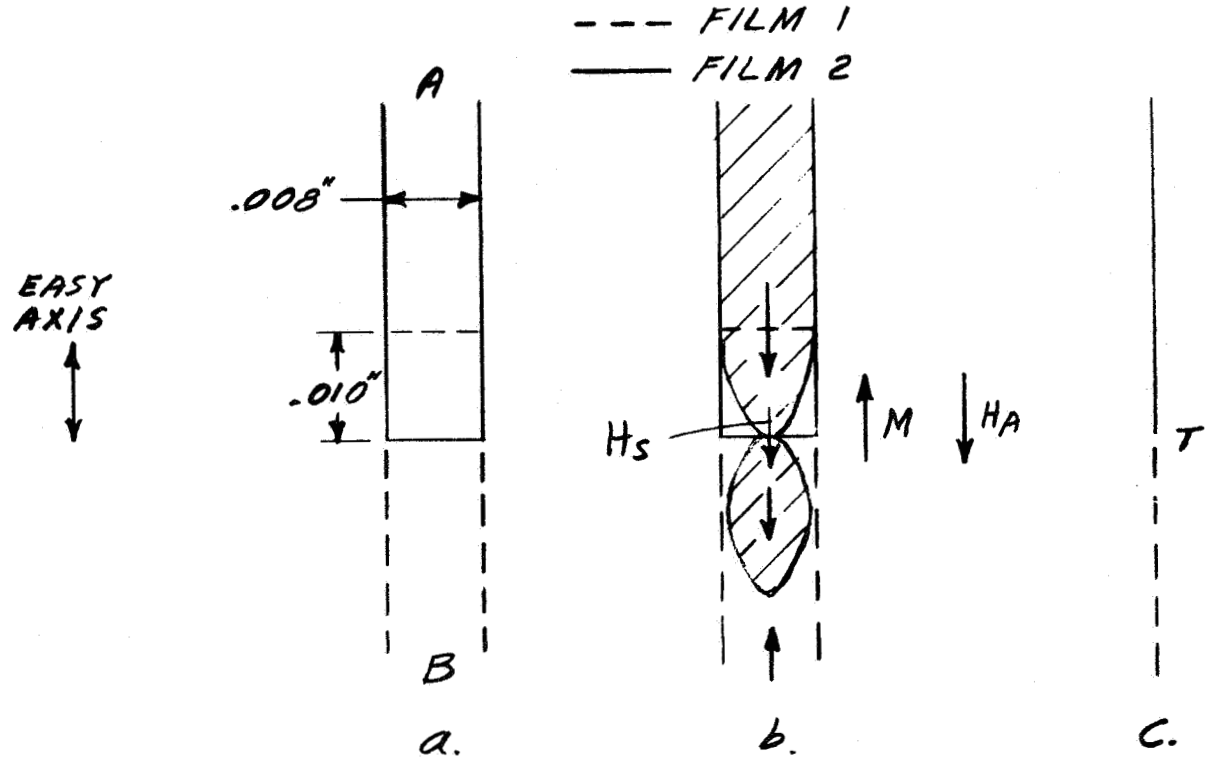


Figure 3 DTPL film-film transfer element (a, b) and its schematic representation (c).

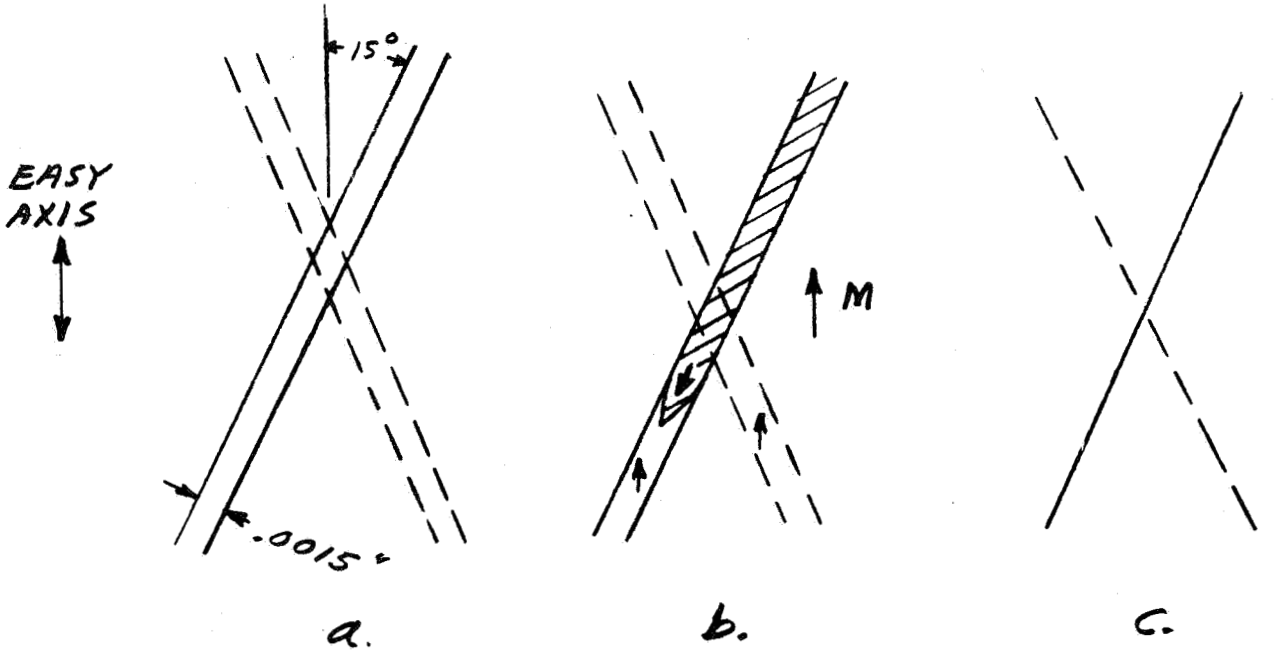


Figure 4 DTPL crossover element (a, b) and its schematic representation (c).

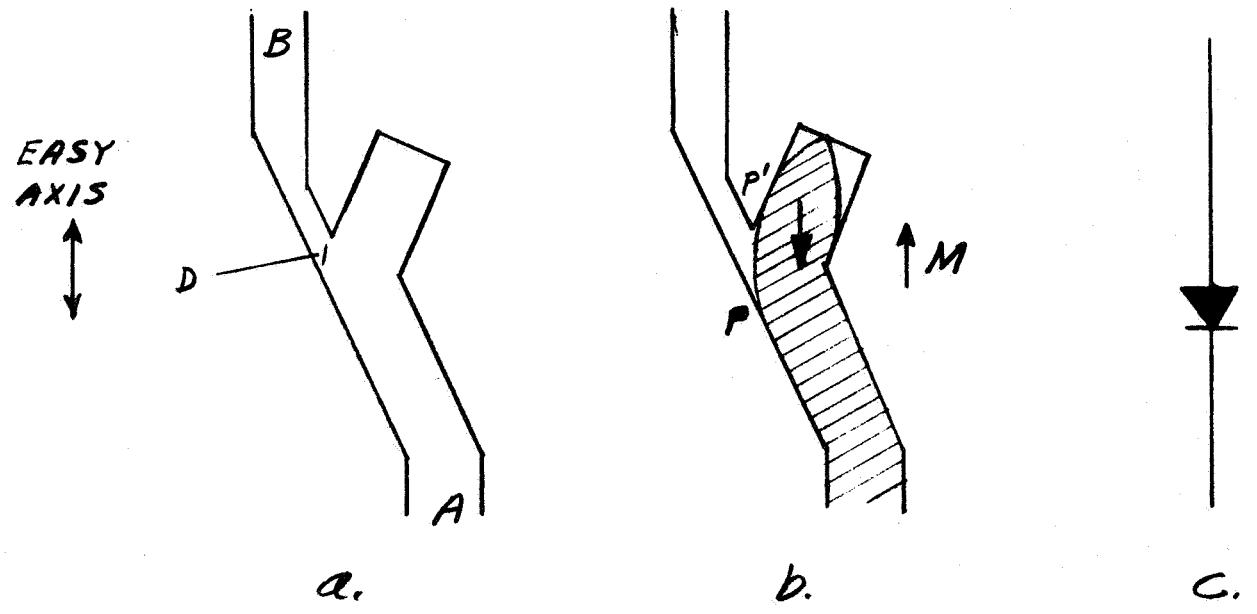


Figure 5 DTPL magnetic diode (a, b) and its schematic representation (c).

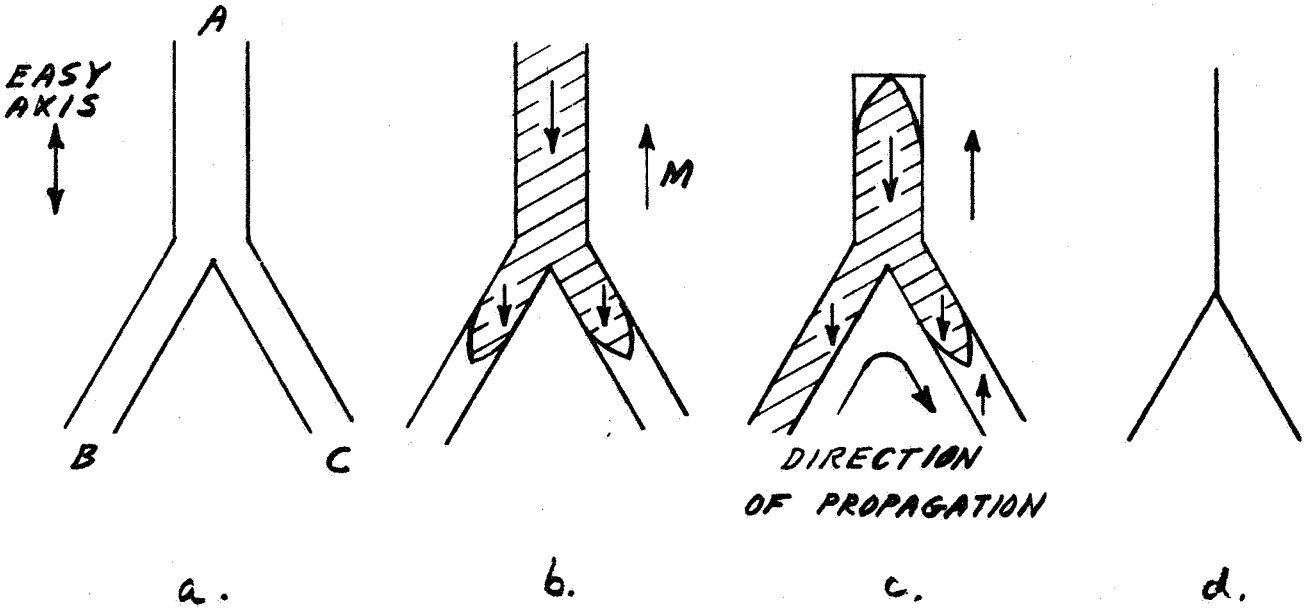


Figure 6 DTPL fan-out element (a, b, c) and its schematic representation (d).

propagation of a tip in channel A past the opening O without entering channel B. After this has occurred, the second effect comes into play, and the domain wall which now bridges the opening O becomes "pinned" between P and P'. Thus, no output into channel B will occur as shown in Figure 5b. The forward direction of the diode is from B to A which is an easy direction of propagation for fields exceeding the coercive force of the narrow channel segment. The latter value is ~ 4 oe while the upper threshold determined by the breakdown of the pinning effect in the back direction is ~ 10 oe. Figure 5c is the symbol for the DTPL diode.

Fan-Out - Since domain tip propagation is a lossless phenomenon, fan-out from a single channel is essentially unlimited. A simple structure which permits a fan-out of two is shown in Figure 6a. The minimum applied field for successful operation as illustrated in part b is approximately 3 oe. If the input channel A is terminated and channels B and C are designated as the input and output, then the element functions as a corner which enables the direction of tip propagation across a film plane to be reversed. This mode of operation and the symbol for the fan-out element are illustrated in figure 6c and 6d.

Fan-In (OR Gate) - The channel configuration for a fan-in element is equivalent to the wired OR case in electronic circuits i.e., a pair of input channels are merely interconnected magnetically with no isolation. Figure 7a depicts the fan-in (OR gate) which is a fan-out operated in reverse. The threshold field for the former is somewhat less than 3 oe since the fan-in and fan-out effects are not magnetically equivalent. Figure 7b is the symbol representing the fan-in (OR gate).

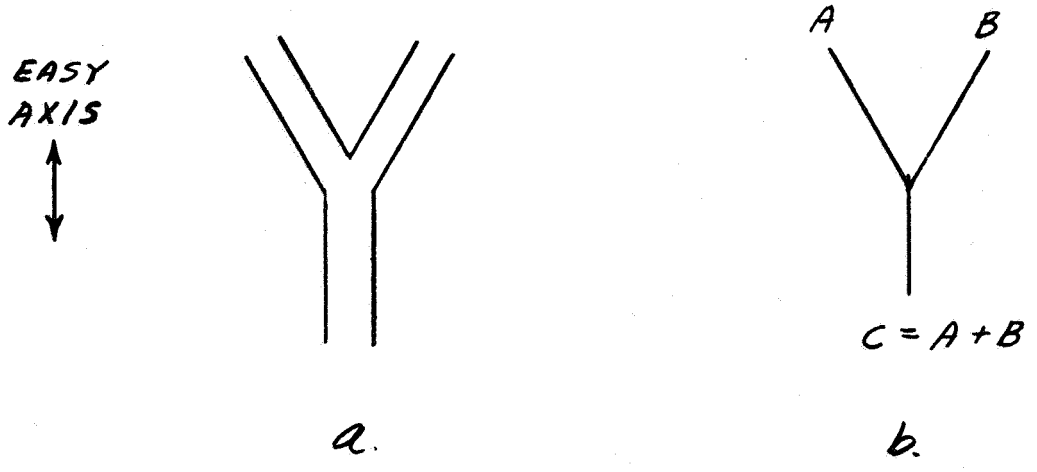


Figure 7 DTPL fan-in (OR Gate) element (a) and its schematic representation (b).

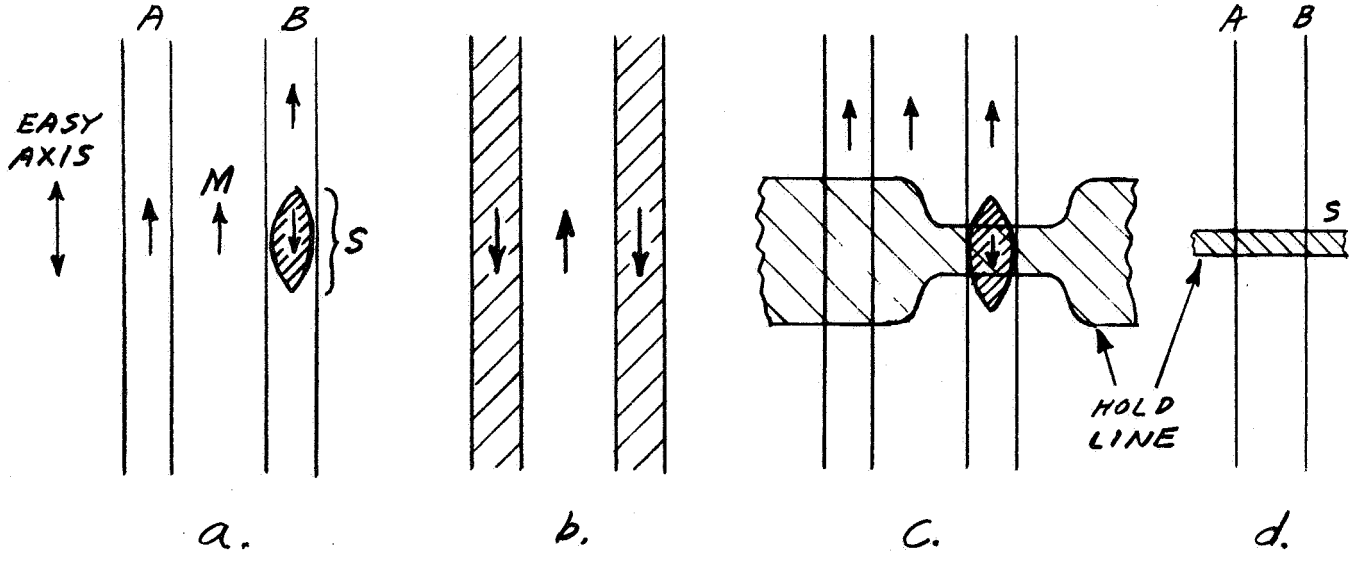


Figure 8 DTPL storage configuration (a, b, c) and its schematic representation (d).

Storage Configuration - In the operation of most DTPL devices and networks, a drive or propagate phase is followed by an erase and hold cycle which resets (erases) the magnetization in the various logic elements and interconnecting channel segments while preventing erasure at specific storage locations. The latter effect is accomplished by energizing hold conductors which produce fields in opposition to the erase field and cancel the effect of the latter. Where a hold conductor is forced to cross channels in which erasure must occur, the width of the line is increased to reduce the effective holding field. This condition occurs throughout the film planes containing the storage cells of an associative memory and is illustrated in Figures 8a - c. Part a depicts an initial state in which channels A and B are reset and a domain is stored in segment S. Let us assume that all channels are switched during the succeeding drive cycle. This new state of the magnetization is given in Figure 8b. In order to return to the initial state, an erase and hold cycle must occur in which the hold is effective in channel segment S alone. The specially-shaped hold line depicted in part c performs this function when it is energized in coincidence with the erase field. Figure 8d is the schematic representation for storage location S, regular channels A and B and the hold line. It must be emphasized that in similar configurations in sections 4 and 5, the hold line is only effective where it intersects a channel designated S.

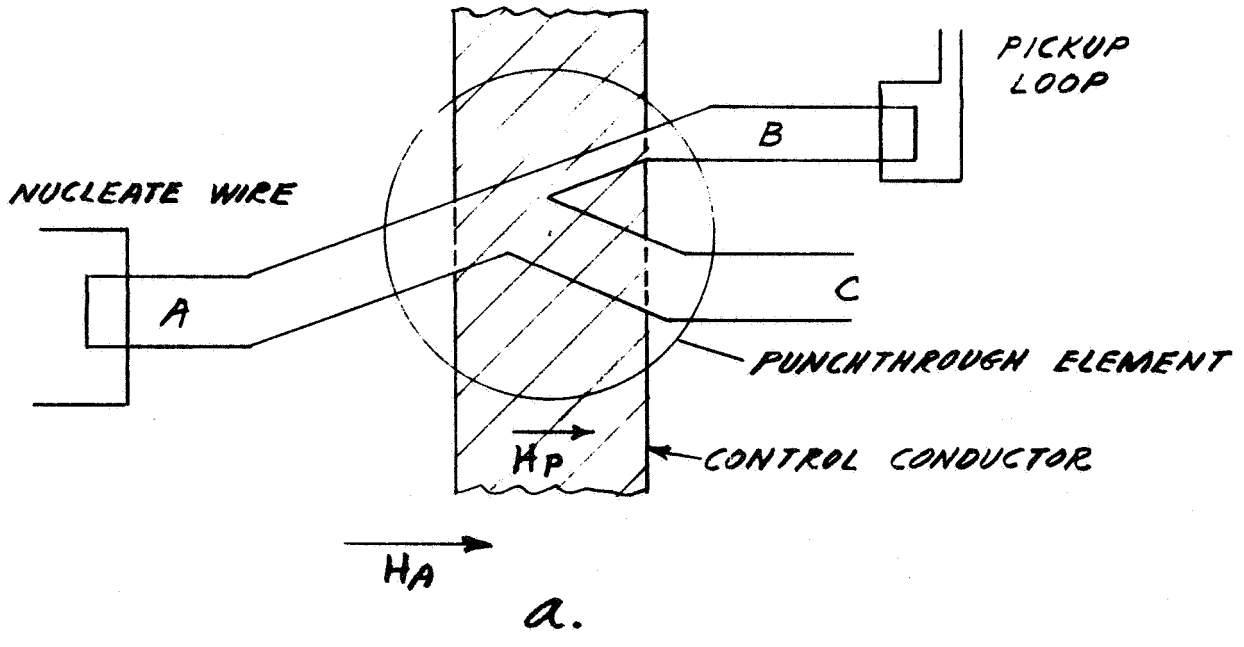
2.2 New DTPL Elements and Techniques

Although the DTPL all-magnetic logic elements described in the previous section form what might be called a "complete set" with which any memory-logic function can be realized, the need for improved elements with greater logical power has become evident in the course of this study program. The

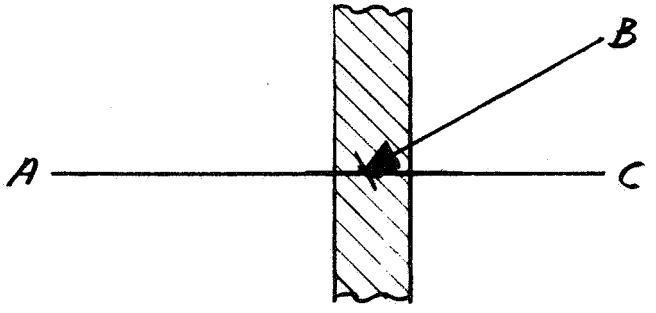
problem of optimizing the size, speed and logic capability of DTPL associative memory cells has been the principal motivation behind the work effort devoted to the study of new logic elements and storage and processing techniques. In the discussions which follow, the pertinent results of these studies are described. The significance of the new elements and techniques which have emerged will become apparent to the reader in later sections of this report.

Punch-Through Diode - The operation of the DTPL tip steering diode (Figure 5) has been described. A punch-through diode element consists of the basic diode and control conductor as shown in Figure 9 and schematically in 9b and performs the tip-field AND function required in the design of an associative memory cell (see section 4). In the operation of the element, the presence of a domain tip in channel A and a pulse of field from the conductor causes punch-through of a tip into channel B. The conductor thus acts to "gate" the diode when a tip enters via the back direction. This operation is somewhat reminiscent of a solid-state silicon controlled rectifier (SCR).

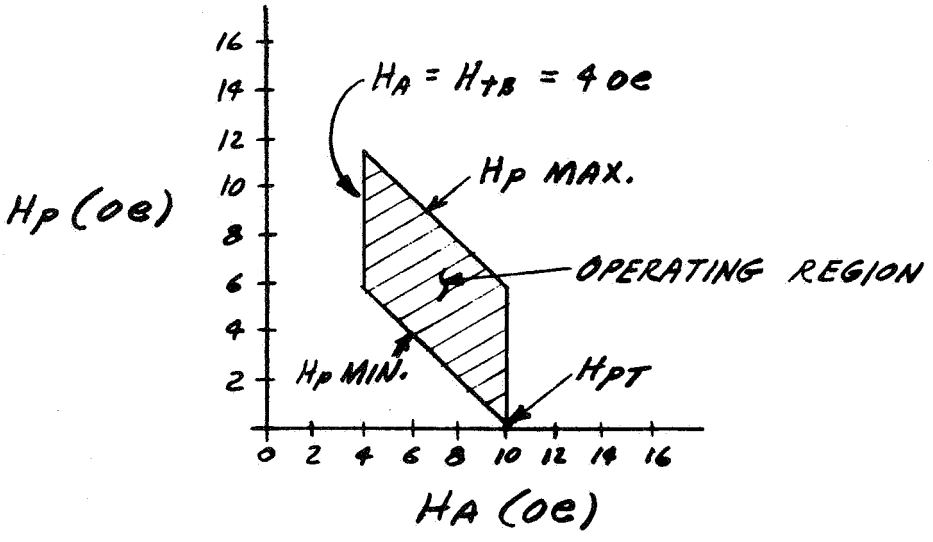
The experimental configuration utilized in the study of the punch-through diode is depicted in Figure 9a. A domain tip is introduced into channel A by means of the nucleate wire and propagated to C using the uniformly-applied easy axis field H_A. When the tip reaches C the control conductor is pulsed producing an easy axis field H_P which, in addition to H_A, causes punch-through into channel B. Readout is accomplished by means of the pickup loop at the end of channel B. The upper limit on H_P is designated $H_{P_{max}}$ and is the field at which spontaneous nucleation occurs. It is determined by increasing H_P until an output is obtained with no input domain tip in channel A. The lower limit $H_{P_{min}}$ is the minimum pulse field which causes punch through when an input is present in A. $H_{P_{max}}$



a.



b.



c.

Figure 9 Experimental configuration used in study of DTPL punch-through diode element (a), schematic representation of element (b), and operating region (c).

and $H_{P_{min}}$ are related to H_A, the diode forward and back thresholds H_{tB} and H_{PT}, and the nucleation field H_N by the following expressions:

$$H_{P_{min}} = H_{PT} - H_A \tag{2}$$

$$H_{P_{max}} = H_N - H_A \tag{3}$$

where $H_{tB} \leq H_A < H_{PT}$ (4)

For a given value of uniform drive field, the range and tolerance % T on H_P are:

$$H_{PT} - H_A \leq H_P < H_N - H_A \tag{5}$$

and $$\%T_{H_P} = \pm \frac{H_N - H_{PT}}{H_N + H_{PT} - 2H_A} \times 100\,\% \tag{6}$$

What makes this element reliable (high $\%T_{H_P}$) is the fact that the value of H_N in equation (6) is not the overall nucleation field in a multi-channel logic structure nominally ~12 oe, but the nucleation field in a channel when this field is produced by a narrow conductor which can exceed 20 oe. Choosing H_A = 8 oe with H_N = 16 oe and H_{P_T} = 10 oe in equation (6), we obtain a theoretical tolerance of ± 60% for H_P. The operating region of the punch-through diode element is obtained using equations (2) to (4) and the above values. It is depicted in Figure 9c.

An experimental study was undertaken to determine the effect of film composition upon the shape of the operating region in order to optimize element performance. Film samples containing diodes were fabricated with NiFeCo magnetic layers of 13, 19 and 22% cobalt, the NiFe ratio adjusted for zero magnetostriction. A control conductor placed across the diodes and driven by a high-

current pulse generator provided the field H_P. The results are presented in Figure 10 for the critical thresholds $H_{P\,min}$ and $H_{P_{max}}$ as defined previously. Referring to the figure, it is seen that both $H_{P_{min}}$ and $H_{P\,max}$ increase with the percentage cobalt (the nucleation and punch-through fields increase with the anisotropy constant H_K which is related to the cobalt concentration). The most predominant effect is the sharp increase in $H_{P_{min}}$ between 19 and 22% Co which greatly reduces the operating region of the latter. In the 13 and 19% Co cases, the minimum thresholds are somewhat alike, but $H_{P_{max}}$ is higher in the latter. Thus, from these curves, it appears that optimum performance of the punch-through diode is obtained using a film composition containing 19% cobalt. The use of this element in the word selection network and several storage cell configurations is described in sections 3 and 4.

Punch-Through Transfer - The film-film transfer elements required in memory cells relized using a superimposed film structure significantly affect the size of these logic networks. As described previously, the transfer elements are .025 inches in length and .008 inches in width. Smaller configurations can be utilized, but only at the expense of overall network tolerance since larger applied fields are then necessary for proper information transfer.

A new logic element has been conceived which virtually eliminates film-film transfer channels of theabove type in memory-logic networks containing the punch-through diode. The structure is called a "punch-through transfer" and is illustrated in Figures 11a and b. It consists of a DTPL diode and a narrow (.0015 inch) channel in a superimposed film which overlaps the shortened output channel of the diode. The

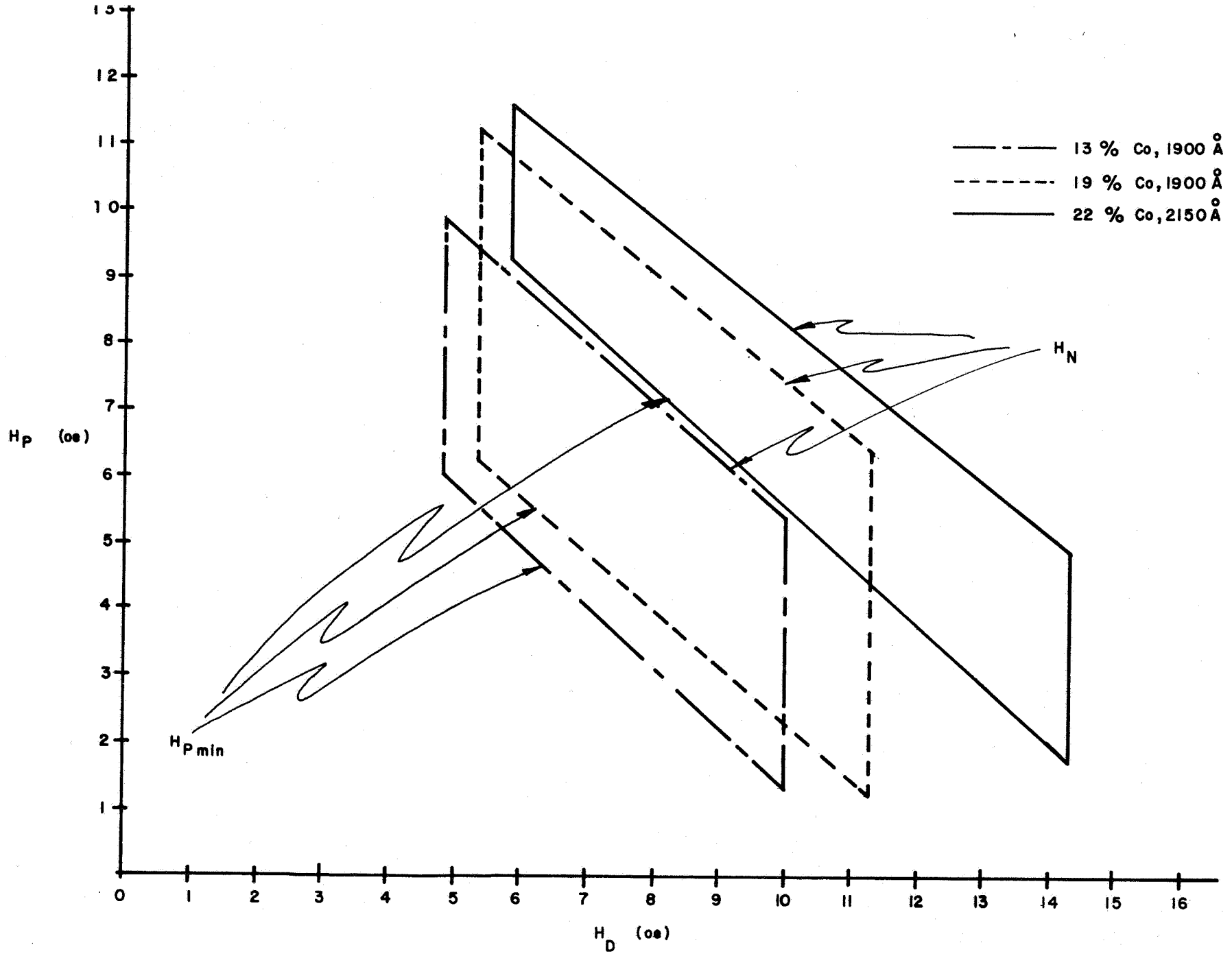


Figure 10 Operating Regions of Punch-Through Diodes in Film Elements of Different Cobalt Concentrations

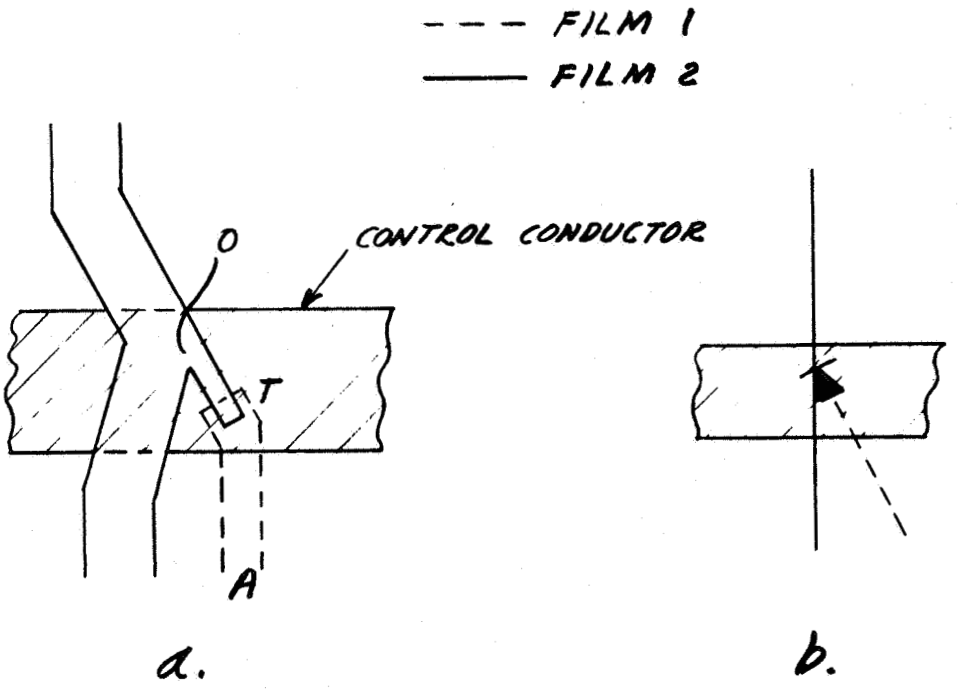


Figure 11 DTPL punch-through transfer element (a) and its schematic representation (b).

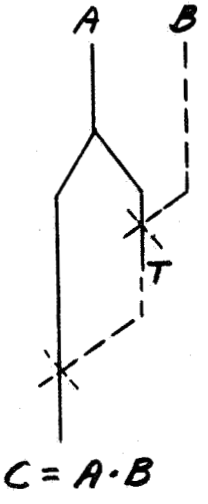


Figure 12 Standard DTPL AND Gate.

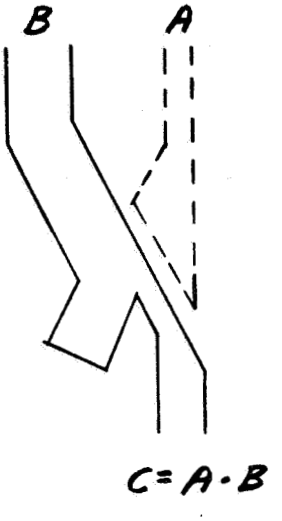


Figure 13 Channel configuration of small DTPL AND Gate.

control conductor which provides the punch-through field also produces the additional field required for transfer from the narrow output channel of the diode into the overlying channel segment since it crosses both the diode opening O and transfer region T. Using the experimental result that the field for transfer between overlapped .0015 inch channels in ~6 oe and the fact that a net field $(H_A + H_P) \geq$ 10 oe is applied to the diode for punch-through, it is apparent that transfer into channel A will occur when the control conductor is energized. Thus, two logical operations are possible with an element no larger than a diode. The reduction in memory cell size possible with this element is illustrated in section 4 (Basic Memory Cell Structures).

Small DTPL AND Gate - The standard method of performing an AND operation using DTPL is depicted schematically in Figure 12. To obtain the correct output, input B must enter the network before A in order that an inhibit occurs at G_1 permitting A to pass through G_2. Although this network is simple in design and functions reliably, it occupies an area .080 inches by .015 inches, which is rather large in comparison to the basic logic elements, i.e., inhibit gate, fan-out, diode, etc. Smaller AND gates utilizing the stray fields from two domain tips to cause nucleation in a third channel have been studied, but their operating margins are not sufficient to meet present DTPL memory-logic network requirements.

An extremely small AND gate has been investigated for possible use in memory cells and arrays. The two-layer element is illustrated in Figure 13 and consists of a DTPL diode and superimposed gate channel A. Its operation is analogous to the punch-through element, in this case, the punch-through field being supplied by a

domain tip in A. Information in channel B alone will not produce an output in C (diode effect), and A alone will not transfer into C. When domains are present in both channels, the stray field from the gate channel will cause punch-through into C and an output.

AND gates of this type have been tested to find the optimum position of the gate channel. A maximum operating margin of 3 oe was achieved, the principal source of failure being unwanted transfer from the gate to the output channel. A reduction in the effective gate interaction field results when it is positioned to avoid this type of error. Other channel configurations using this punch-through technique to realize the AND function are being considered.

Two-Input Inhibit Gate - A natural extension of the hatchet type inhibit gate is the channel structure illustrated in Figures 14a and 14b. The study of memory cell designs has shown the need for a gate with entries on either side of the main channel. For such purposes, the two input channels must be isolated. This is accomplished by adding diodes as depicted schematically in Figure 14c. Two-input gates of this type have been operated successfully with no loss in tolerance as compared to the basic gate. The former is incorporated in the output-on-match memory cell described in section 4.3.

DTPL Galvanomagnetic Transfer Technique - The use of galvanomagnetic effects for the rapid transfer of information between widely separated locations on the same or different film planes was described in the proposal[2] for the program. Figure 15 illustrates the manner in which two channels A and D are interconnected by means of the planar-Hall element. A domain is introduced in channel C as part of the normal drive cycle by the nucleate wire. This tip is stopped at P due to the increased coercivity of the necked-down channel segment.

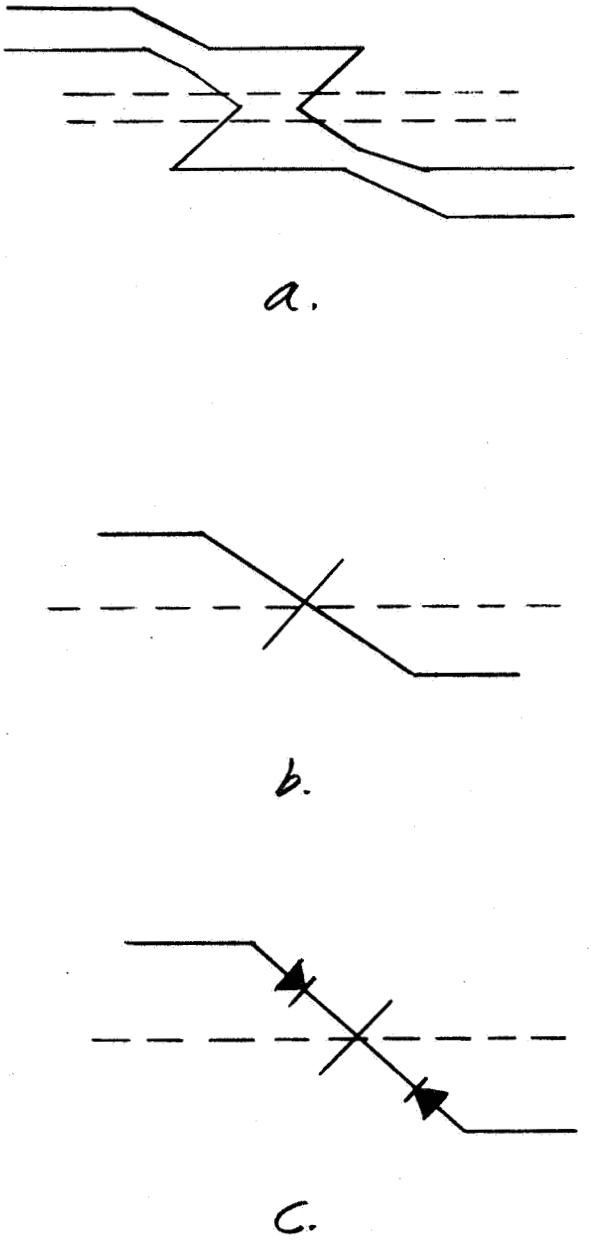


Figure 14 DTPL two-input inhibit gate (a) and its schematic representations (b, c).

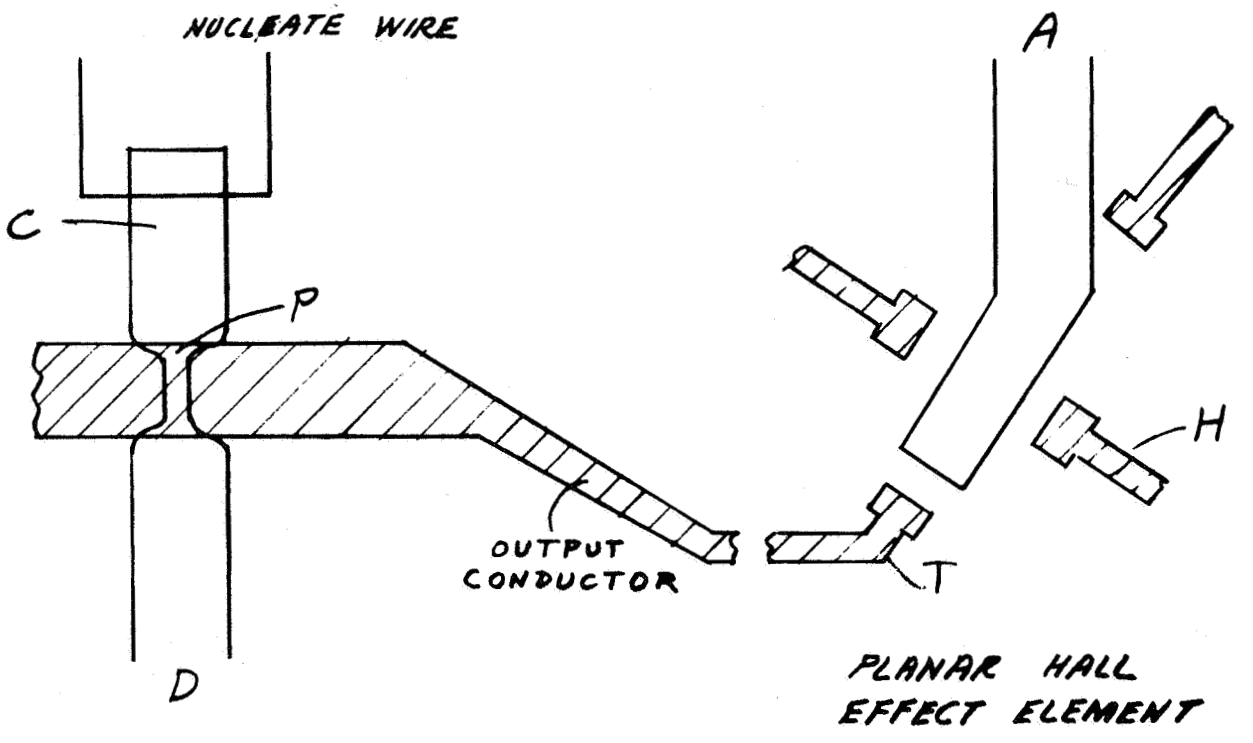
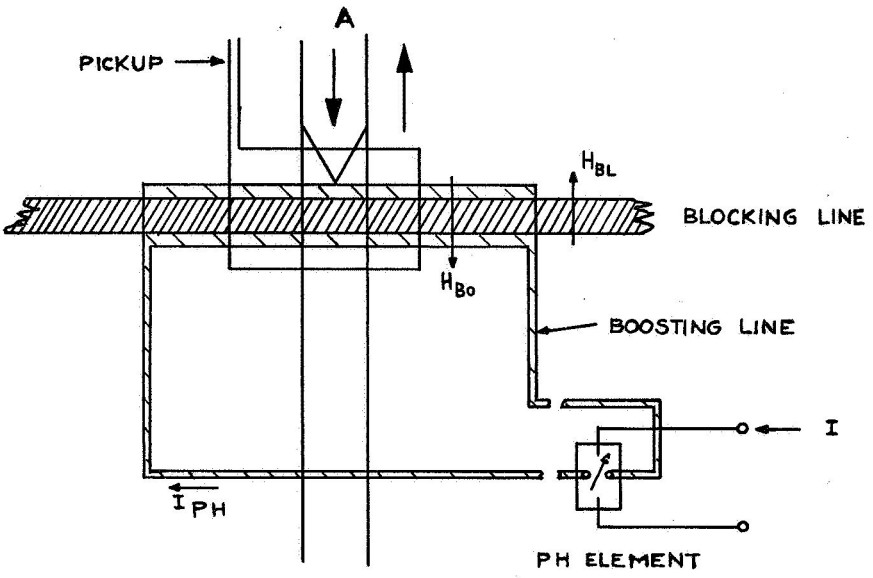


Figure 15 Channel and conductor configuration for galvanomagnetic transfer element.

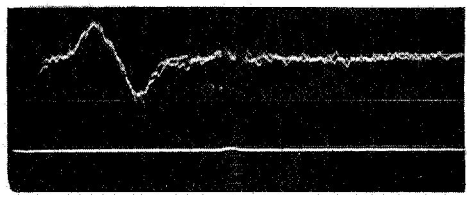
An output from the Hall effect element via T occurs if a tip is present in channel A when conductor H is energized with a pulse of current. This output is used to produce a field which forces the tip in C through the constriction at P so that it appears at D. The control element output conductor T is directly above narrow channel segment P as shown in the figure.

While complete structures of the type shown in Figure 15 have not been implemented, an experiment was performed using an isolated planar-Hall element to determine feasibility of the aforementioned scheme. In this case, the necked-down channel segment P (see Figure 15) was replaced by a blocking conductor which, when energized, produced a field H_{BL} inhibiting tip propagation. The experimental configuration is presented in Figure 16a. It is seen that a boosting line driven by the output of an isolated planar-Hall (PH) element is positioned above the blocking line. When the state of the magnetization $\overline{M}$ in the PH element is such that $I_{PH} = I_{PH_{min}}$, the field produced by the boosting line $H_{BO} = H_{BO_{min}} < H_{BL}$ and a tip entering channel A will come to rest as shown in the figure. This magnetic state will be known as $\overline{M} = O$. If $\overline{M}$ is oriented such that $I_{PH} = I_{PH_{max}}$ ($\overline{M} = 1$), $H_{BO} = H_{BO_{max}}$ and $H_{BO_{max}} > H_{BL}$. Thus, the effect of the blocking field is cancelled and the input tip propagates to B. Figures 16 b, c, d and e show the bipolar tip readout signals and I_{PH} for the situations indicated. The positive and negative signals correspond to the input domain tip as it enters and leaves the vicinity of the control conductors respectively.

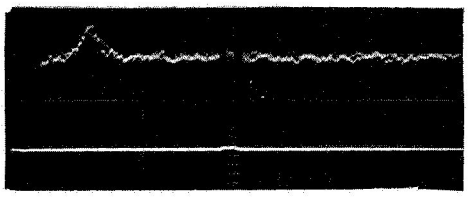
Additional study of galvanomagnetic transfer elements is planned. In the above experiment, an input current pulse I to the planar-Hall element of 4 amperes was required to obtain an output current of



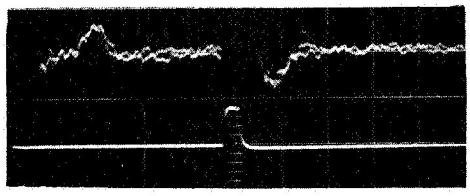
(a)



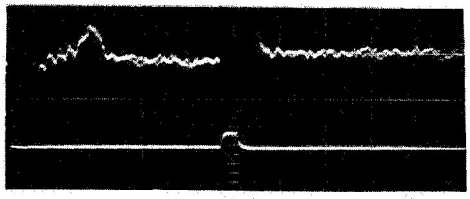
(b)



(c)



(d)



(e)

Figure 16 Experimental configuration used in study of galvanomagnetic transfer technique (a) and readout signals (b, c, d, e) - (see text).

only 27 ma. Techniques must, therefore, be developed to improve the "transfer" characteristic $I_{PH_{max}}/I$ of planar-Hall elements, particularly those using channeled magnetization which, in previous experimental studies, have yielded a maximum of 5.6 mv/ampere. Among those factors to be considered are the electrode configuration, channel width and angle and element isolation. The latter involves photo etching slits in the magnetic film around the PH element to direct the flow of input current across the readout channel.

2.3 DTPL Readout Techniques

Reliable readout of information from a propagation channel is essential to the success of DTPL as a means for realizing complex memory-logic functions. At present, two techniques are utilized for detecting the presence of an information-bearing domain of reversed magnetization. The first method involves inductively sensing the signal from a propagating domain tip and yields an output of the order of 50-100 μv per turn of pickup loop and readout channel. The second class of readout elements utilizes galvanomagnetic effects, magnetoresistance and planar-Hall, which are capable of producing output signals of several millivolts. In this case, an angular difference, approaching 90°, between the switched and unswitched states of the magnetization within the output channel is required. This difference is a result of the shape anisotropy and can, therefore, be controlled by the channel width and orientation.

The basic advantage offered by the inductive readout scheme is the simplicity of fabricating pickup loops. These photo-etched conductors are normally contained in a wiring pattern which includes nucleate, hold and punch-through control conductors upon which is placed the DTPL memory-logic film plane. A principal limitation of this technique is signal amplitude.

The use of multiple readout channels and multiturn pickup loops can significantly increase the output signal, but only at the expense of network or memory cell size and speed. Furthermore, a multiturn sense loop of the type illustrated in Figure 17a is not conveniently fabricated since a connection to the center pad is required. An "equivalent" configuration (same number of turns) with both coil connectors in the same layer is shown in Figure 17b. The increased coil area, however, results in larger noise signals (component due to turn-on of drive and control fields) which, in many cases, mask the information-bearing output.

Recently, significant progress has been made in the development of a multiturn inductive pickup configuration which makes use of a plated-through hole to interconnect matching loops photo etched on both sides of a control conductor substrate. Figure 18 illustrates the component loops, location of the plated-through hole and the output terminals a and b. The fabrication technique for making contact between layers without shorting the various turns is quite tedious, and accurate registration techniques are required. Sample pickup loops have been fabricated which were continuous, thereby demonstrating the feasibility of the technique. In actual operation as the readout element of a DTPL device, a three-turn loop pair positioned over a single readout channel produced a signal four times larger than normally obtained with a single turn. Although there are six turns in the loop pair, the contribution from the bottom conductors was diminished by the film conductor spacing which was approximately .004 inches. In addition, there is some signal spreading due to the spacing between adjacent turns. Thus, the observed one-third reduction in sighal strength from a possible 6V to 4V, where V is the single-turn output, is to be expected.

The use of plated-through multiturn pickup loops as the bit slice sense line in an associative memory array poses somewhat of a problem. With

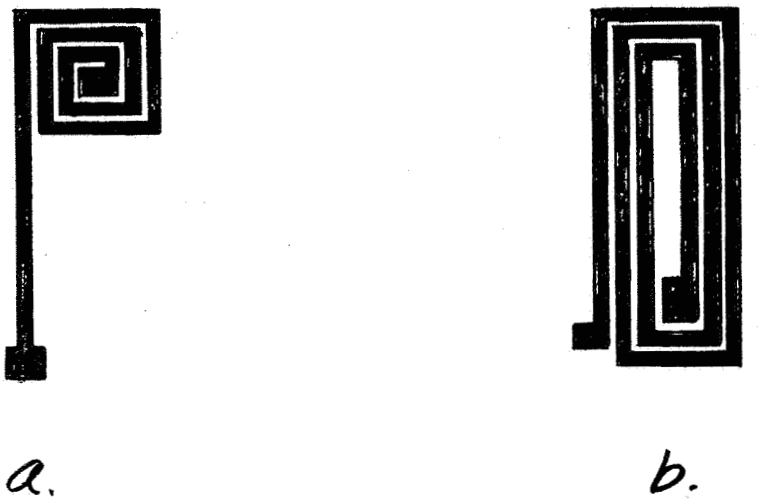


Figure 17 Multiturn pickup loops.

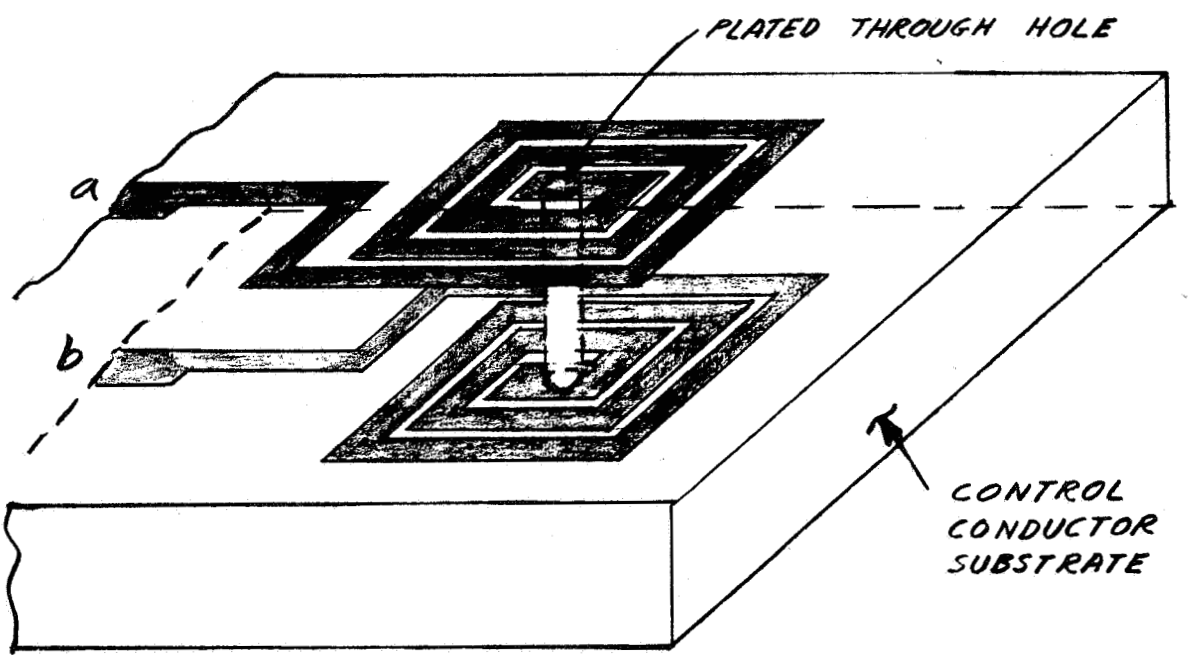


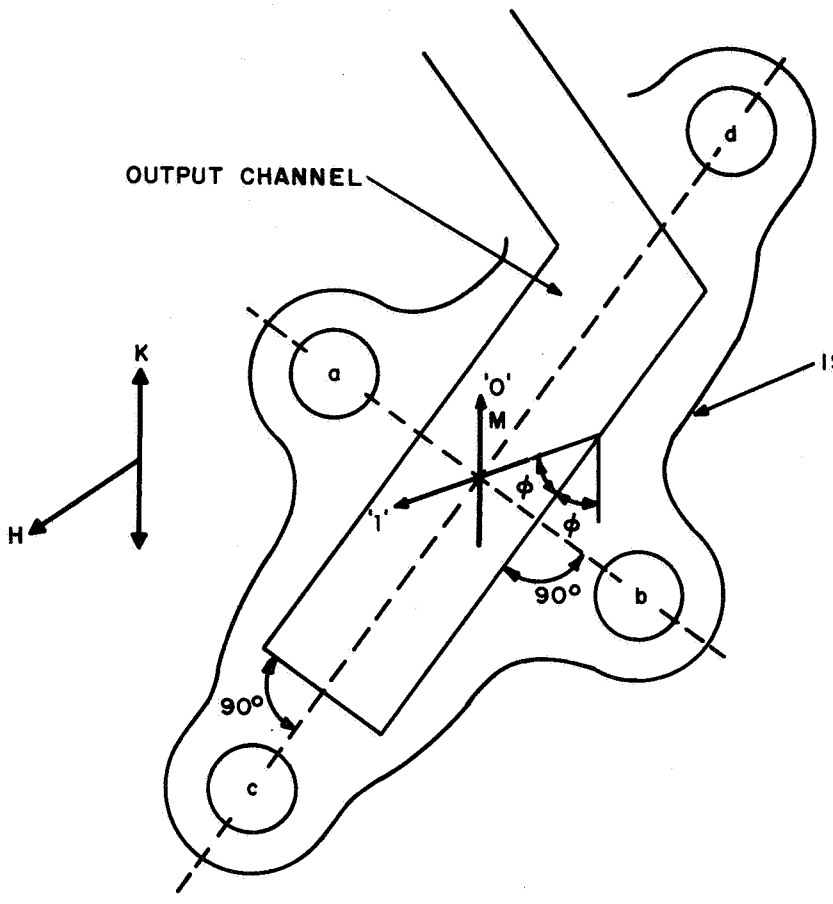
Figure 18 Multiturn pickup loops employing plate-through hole.

typical loop resistances being 1 ohm, a total sense line resistance exceeding 100 ohms could be expected. Sense amplifiers with high input impedance would then be required to avoid losing the entire signal in the line itself. Amplifiers of this type are susceptible to noise transients, thermal noise included.

The configurations of DTPL planar-Hall effect and DTPL magnetoresistance readout elements are depicted in Figure 19. Fabrication of these elements requires photo-etching copper electrodes a to f on the film element around the output channel. The lead-in conductors (not shown in the figure) are formed in a similar manner and insulated from the magnetic film by a layer of photo resist. Referring to figure 19, it is seen that isolation slits are located around the electrodes to assure that all of the input current passes through the active area of the output channel (between electrodes a and b in the planar-Hall element, c and f in the magnetoresistance element).

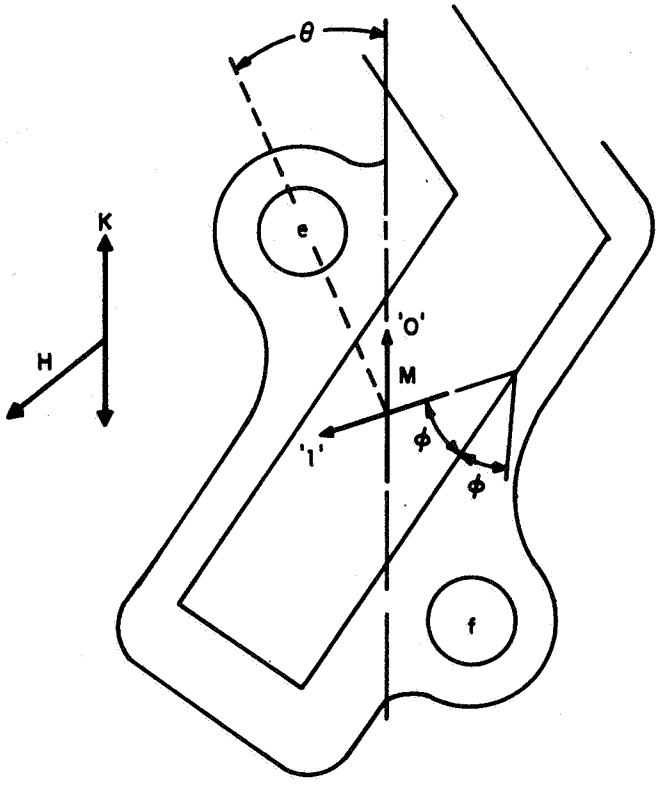
A number of DTPL readout elements using the planar-Hall effect and magnetoresistance have been fabricated and tested. Figure 20a is a photograph of a planar-Hall element positioned above the output channel of a DTPL zig-zag device. No isolation slits were utilized in this case. Part b of Figure 20 depicts the change in output voltage produced as the tip propagating down the zig-zag channel enters the output channel. Additional results obtained using galvanomagnetic readout elements are summarized in Table I. In the case of the planar-Hall element, the effect of displacing current electrodes off center toward one of the voltage electrodes was examined. For the magnetoresistance element, different angles ϕ (see Figure 19b) were investigated. The effect of isolation slits was also considered.

The results presented in Table I indicate, very clearly, the improved output made possible by partially isolating the readout elements. Planar-Hall



(a)

planar Hall effect

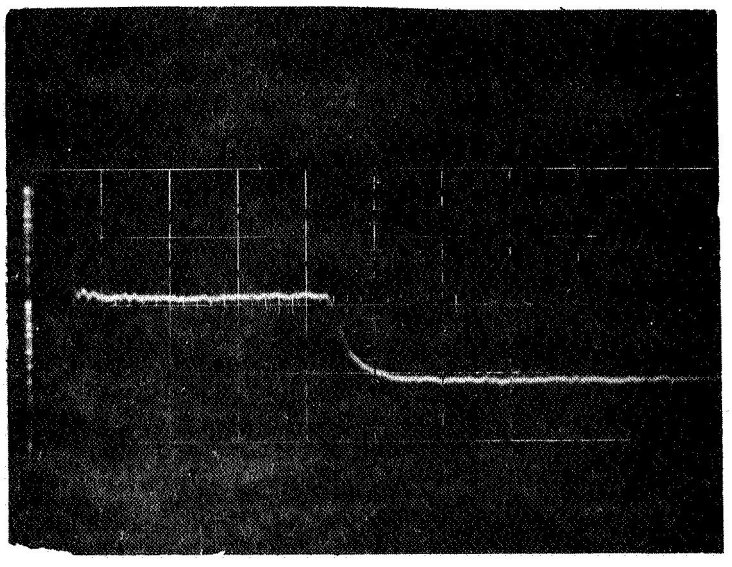


(b)

magnetoresistance

Figure 19 Configuration of DTPL-galvanomagnetic readout elements.

(a)



(b)

Figure 20 a) Planar Hall effect readout element

b) Output from DTPL--planar Hall effect readout element without isolation slit

Vertical scale: .2mv/div
Input current to readout element = 400 ma

Type of Readout Element	Isolation Slit	Geometry	Signal Output (mv/amp)
planar Hall effect	no	current electrodes centered	2.0
planar Hall effect	yes	current electrodes centered	5.6
planar Hall effect	no	current electrodes off-center	1.6
planar Hall effect	yes	current electrodes off-center	3.2
magnetoresistance	no	$\theta = 15°$	2.1
magnetoresistance	yes	$\theta = 15°$	3.0
magnetoresistance	no	$\theta = 45°$	1.2
magnetoresistance	yes	$\theta = 45°$	2.4

Table 1. DTPL-galvanomagnetic readout from a shift register output channel. The output channel is 4.5 mils wide, at 30° from the easy axis. The films are 1500 Å thick and contain 13% Co. The applied field was such as to stimulate shift register operation.

elements are seen to yield a lower output signal in the off-center configuration, while the magnetoresistance elements produce larger signals with $\phi = 15°$ as compared to $\phi = 45°$. Although somewhat lower outputs were obtained with the magnetoresistance effect, critical positioning of the electrodes is not required (leakage currents often dominate planar-Hall outputs). Thus, element design and fabrication is simplified and reliability improved.

Experiments were also performed to determine if magnetoresistance readout elements behave in accordance with the theoretical expression for their operation. This relationship is given by

$$\Delta R = G \left(\frac{\Delta\rho}{\rho}\right) \frac{\rho}{T} \cos^2 \theta - \cos^2 (\theta + 2\phi) \qquad (7)$$

where $\left(\frac{\Delta\rho}{\rho}\right)$ is the magnetoresistance coefficient, ρ/T is the resistance/square of film, G is a geometrical factor, and angles θ and ϕ are defined in Figure 19b. No isolation slits were used in the test elements. Typical 13% Co, 1500 Å film planes containing readout elements with varying electrode angles θ and $\phi = 30°$ were prepared by vapor deposition in the usual manner. Evaluation was performed on the DTPL AC test bench with fields applied at 45° to the easy axis. The results of these experiments are shown in Figure 21, in which the signal out in MV/amp is plotted as a function of electrode angle θ. The dotted line represents the equation for ΔR normalized for comparison with the experimental data. It is seen that the data is in good agreement with equation (7). A maximum ΔR occurs for $\theta = 105°$ and a zero value for $\theta = 75°$. The difference between the curves is attributed to the fact that the magnetization within the output channel in the "1" state does not lie at 60° (2ϕ) to the easy axis. It is reasonable to assume that 2ϕ is less than 60° -- let us say 40° -- which would yield $\Delta R = 0$ for 70°. The experimental result of

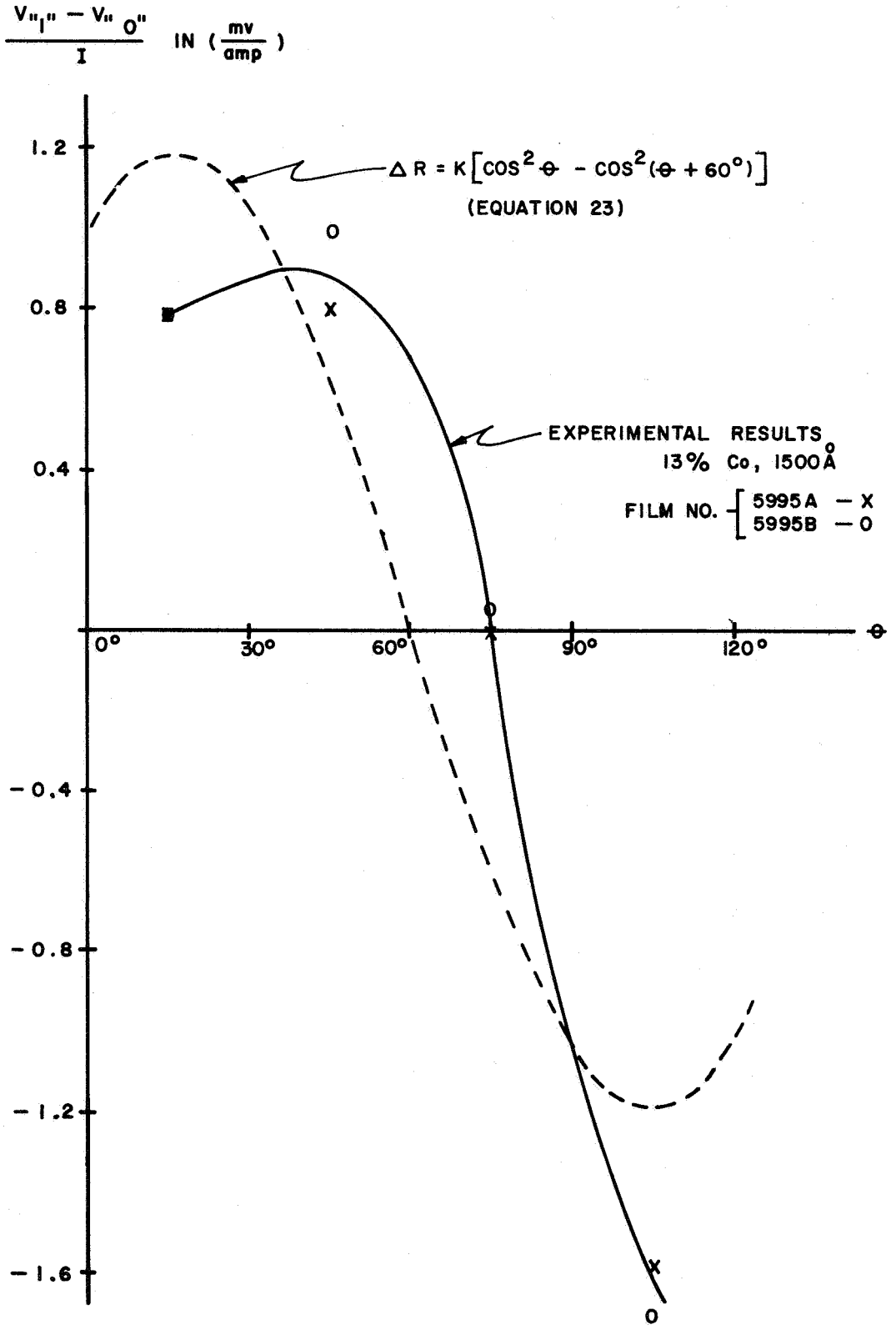


Figure 21 Output from Magnetoresistance Readout Element as a Function of Electrode Angle θ. $V_{"1"} - V_{"0"}$ is the difference in signal from switched and unswitched output channels.

$\theta = 75°$ for the zero point verifies this assumption. Further study of these elements is planned. There use in memory cells and memory arrays is described in section 4.

3. WORD SELECTION LOGIC

3.1 Introduction

While storage cell selection circuits are required in most computer memories, their use in associative processors depends upon the application and organizational approach. If, for a particular application, it were desirable to include among the various associative processor functions the capability of reading and writing by address, word selection logic would then be required to perform address decoding. Electronic hardware of this type usually comprises a major portion of the memory system electronics and thus determines, to a considerable extent, the cost of the memory. The DTPL techniques of information processing make possible the design of batch-fabricatable selection networks which offer many advantages in cost and power requirements over conventional memory selection schemes. This section contains a description of one of the three proposed channel selection networks which have been implemented and tested during the first half of the program.

3.2 Decoding with Domain Tips and Conductors

The technique of decoding by a combination of domain tip propagation and control conductor logic has been described in the proposal. A brief review of this scheme follows.

Let us consider the configuration in Figure 22a which consists of two propagation channels containing high coercive force, narrow segments n_1 and n_2 crossed by a U-shaped control conductor. Part b of the figure depicts the schematic representation. When input domain tips A and B enter channels 1 and 2 under the influence of an applied fiend $H_A < H_{t_n}$ (tip coercive force in narrow segments), they come to rest at n_1 and n_2

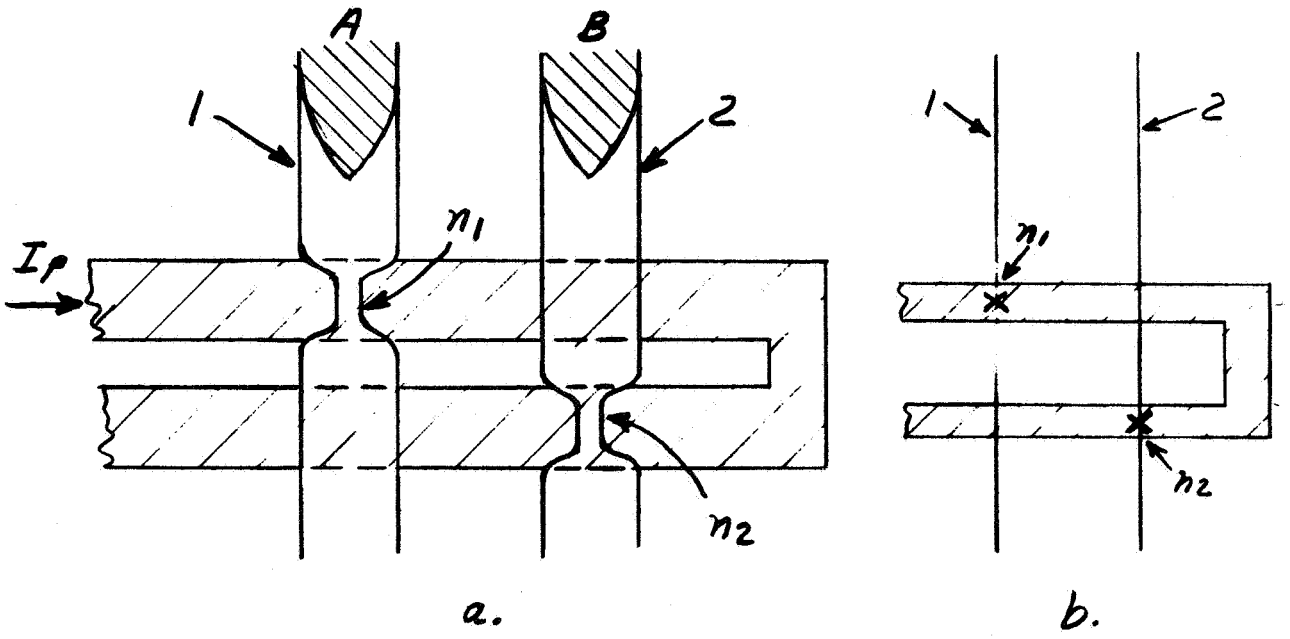


Figure 22 A portion of DTPL decoding network (a) and its schematic representation (b).

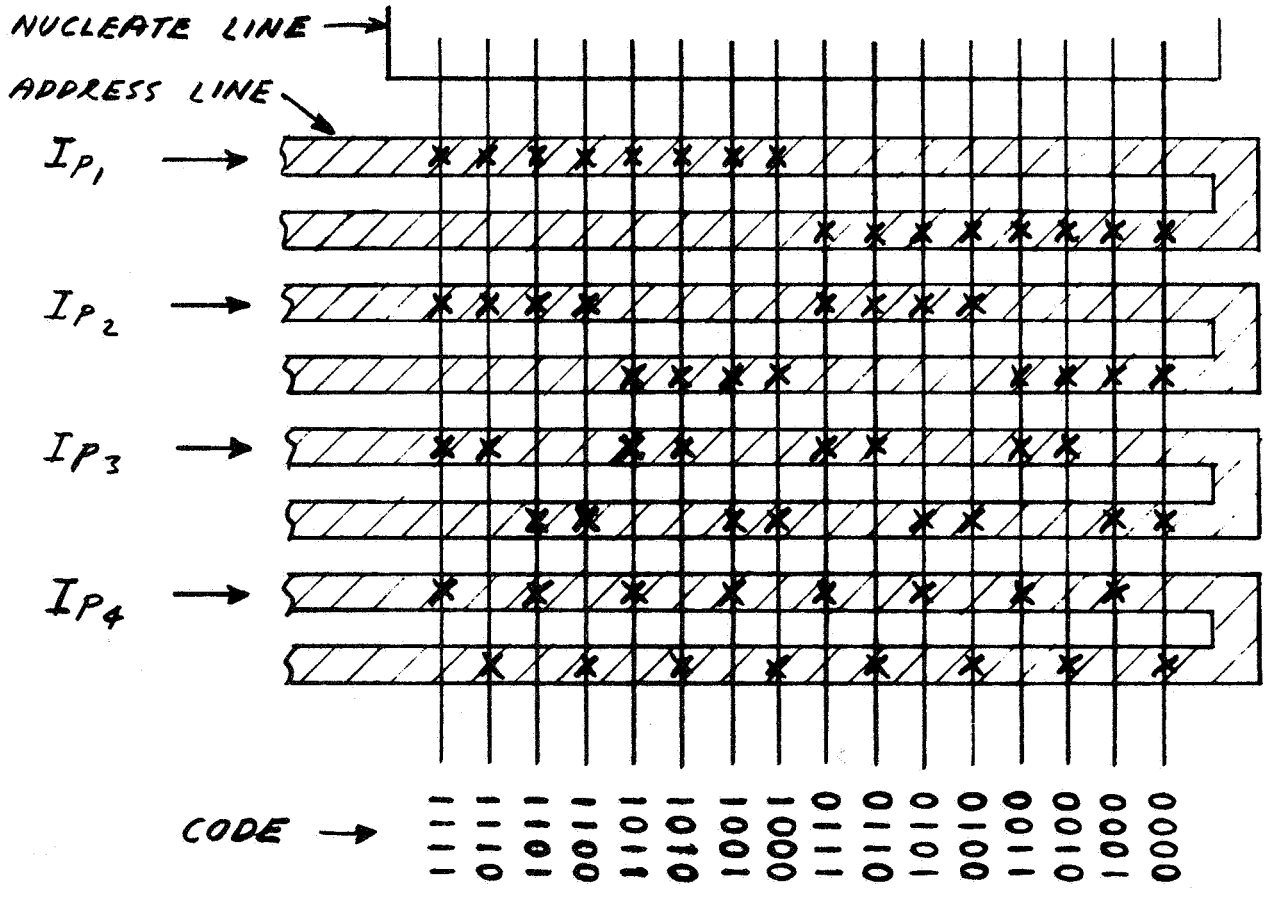


Figure 23 16-Channel DTPL word selection network.

respectively. If, at this time, the control conductor is energized with a positive current pulse I_p producing a field H_p which satisfies $H_p + H_A > H_{t_n}$, tip A will be forced through n_1 and emanate from channel 1. At n_2, H_p is in opposition to the applied field and tip B remains at that location. If, on the other hand, the control conductor is energized with a negative current pulse, the opposite effect occurs and an output is obtained from channel 2. Channel selection, therefore, depends upon the polarity of control conductor current and position of the high coercive force channel segments n_i.

A 16-channel DTPL word selection network using the configuration in Figure 22 as the basic building block is depicted schematically in Figure 23. Each coded output channel corresponds to the input channel, or channel pair of a word in the associative processor. The four address lines are driven from bipolar drivers, the polarity of current pulse I_{P_j} determined by the contents of j^{th} bit of the word address register. The code for each word is given in the figure and corresponds to the position of the channel segments n with respect to each address line. A 1 is represented by an n channel crossed by the upper half of a U-shaped conductor, while the intersection of an n and the lower half of an address line is designated as a 0. The nucleate line indicated in Figure 23 is used to simultaneously introduce domains of reversed magnetization into all channels at the start of a decoding operation.

Referring to Figure 23, it is seen that only four address lines are required to select one of sixteen output channels (words). Describing this in another way, M words of memory can be selected by N lines where $M = 2^N$ or $N = \log_2 M$. The important feature of this network is the fact that the decoding takes place in the channel structure and the address lines can be driven directly from an address register i.e.

no electrical decoding is required although the address register must be provided with facility for producing positive and negative currents. Electronics hardware is, therefore, minimized.

A preliminary design for the word selection network was implemented, tested and found to function satisfactorily. The 5X photo-masks for the sixteen output channels and four U-shaped control (address) conductors are presented in Figure 24. In order to increase the tip coercivity in the narrow channels, these segments were oriented at an angle to the main channels and thus the film easy axis. Control conductor width was approximately .005 inches yielding a field factor of ~50 oe/amp. Film samples containing the coded channels were prepared in the usual manner by vapor deposition of a 71.5/15.5/13, Ni/Fe/Co, 1500 Å, magnetic layer over the photo etched aluminum channel pattern. Address conductors were fabricated by photoetching copper-clad epoxy board which was subsequently mounted upon a flat drive coil. The film element to be evaluated was positioned face down on the conductors to insure maximum uniformity of the localized address fields.

Using the Kerr magneto optic effect to observe the state of the magnetization within the output channels and a simple switching circuit to energize the address lines, correct network operation was verified under pulse drive conditions. With the applied field oriented to optimize the "blocking" effect of the narrow high coercive force channel segments, an addressing line current of ~100 ma (5 oe) was sufficient to overcome that effect over a drive range of 3 - 8 oe. The use of narrower control lines .0025 inches and less would make possible a reduction in this current requirement to ~50 ma. Under these conditions there would be no need for conventional driver circuits as an interface between the memory address register and DTPL selection network. There exists today simple semiconductor buffer devices capable of supplying pulse

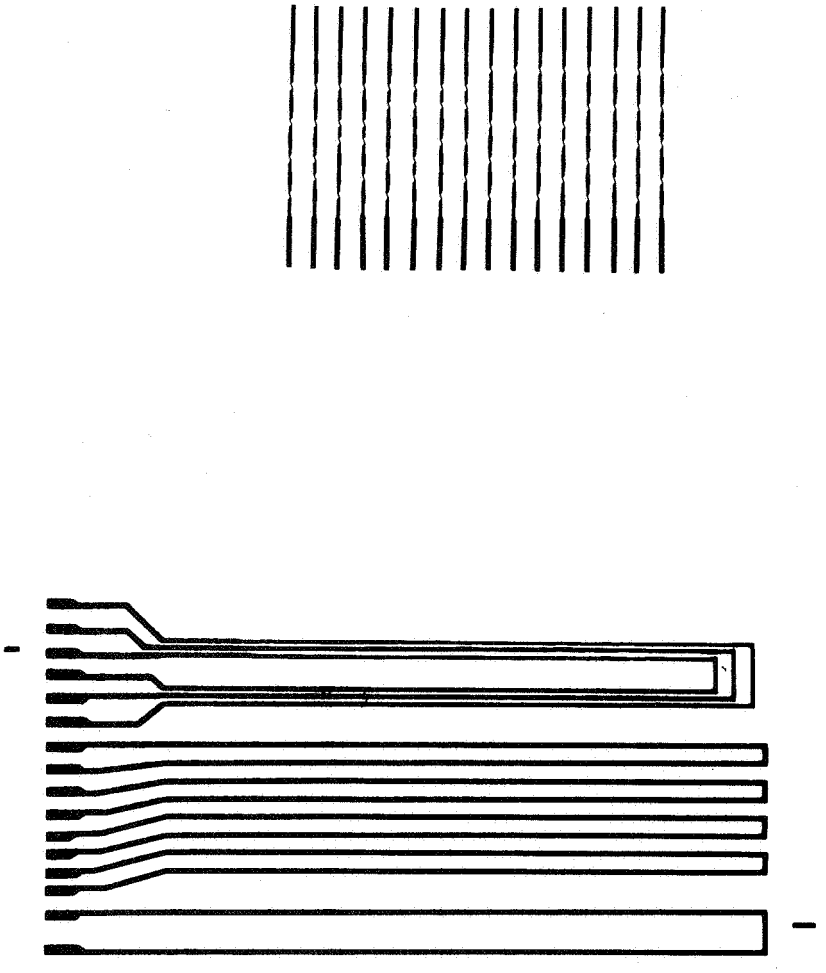
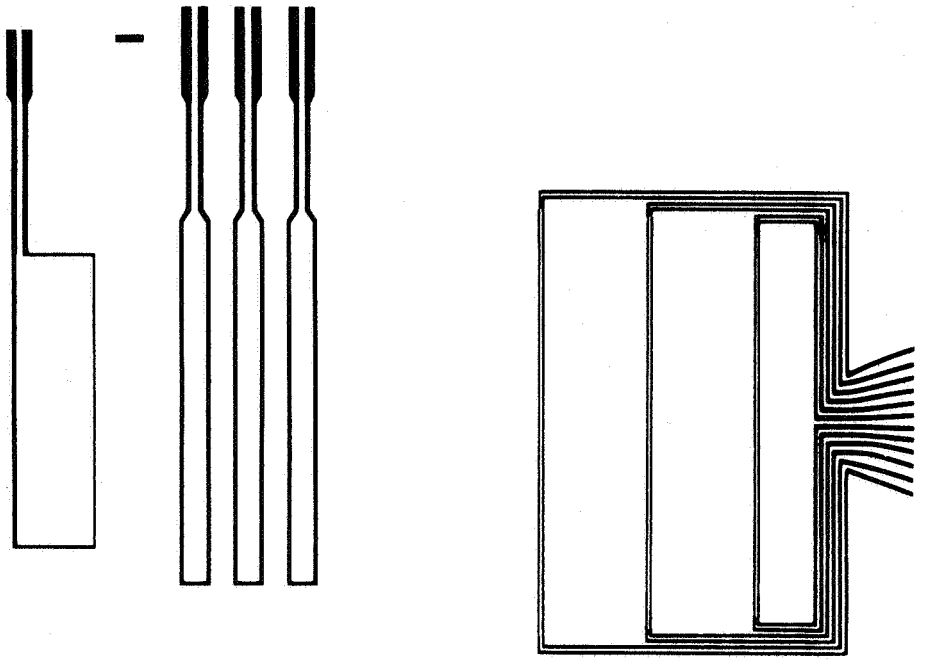


Figure 24 Channel (a) and conductor (b) photo-masks at 5X for preliminary word selection network.

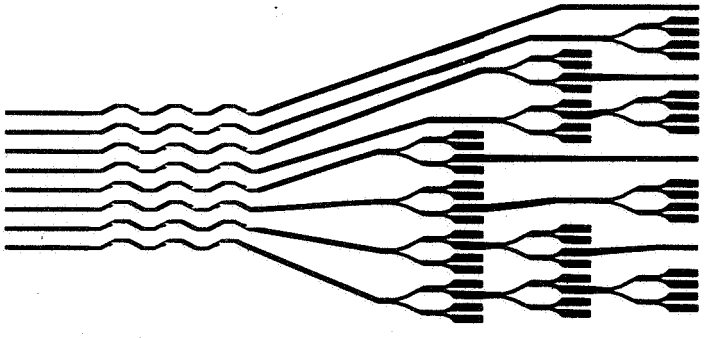
currents of 50ma which can be used in the design of the associative processor address register.

With the advent of the punch-through diode logic element (see section 2.2) significant improvement in the operation of the word selection network is possible. To begin with, punch-through elements would replace the narrow channel segments contained in the preliminary design (ref. Figure 24) and .0015 inch (~150 oe/amp) address lines utilized A drive range of 4.5 to 10 oe would be obtained (nearly ± 40% tolerance), and the larger tip velocities achieved at the higher fields (~7 oe) would reduce the time required for tip propagation through the network. Tip velocity data indicates that a selection operation in a 1024 word selection network employing ten U-shaped address lines would require 3 μsec of memory cycle time.

An improved 8-word selection network using the punch-through elements has been designed. The channel and conductor configurations are presented in Figure 25. In addition to the basic channel structure, the logic unit contains a coded readout network. The latter will facilitate interpretation of the electrical output signals when the unit is operated. This scheme may also be employed in the associative memory as a means of identifying the address of a word responding to a particular search operation. It is planned to fabricate and evaluate the selection and coded readout device during the second half of the program.



a.



b.

Figure 25 Photo-masks at 5X for improved word selection network-channel pattern (a), conductor pattern (b).

4. BASIC MEMORY CELL STRUCTURES

4.1 Introduction

A major portion of the first six-months work effort was devoted to the design of a suitable associative memory cell using DTPL two-layer memory-logic techniques. The intial phase of this study was concerned with the problem of establishing techniques for performing the basic cell operations namely storage, write, read, erase, and test for match. Attempts were then made to combine these capabilities in a single simplified channel and control conductor configuration and render it as compact as possible in order to maximize both density and speed.

We recall that in the proposed memory each of the binary digits (bits) of a word consisted of two identical associative memory cells for storing the 1's and the 0's. Two interrogate lines were required for the match operation and all tests were based upon the presence of a domain tip in a low coercive force channel. The designs described in this section represent a new philosophy in which a single cell per binary bit is utilized for storing and comparing 1's and 0's. The state of a cell - binary 1 or binary 0 - is represented by the presence or absence of reversed magnetization within the cell storage channel. This will have the effect of nearly doubling the overall bit density and simplifying the task of performing search and processing operations.

The cell structures are classified according to their outputs during an equality search operation i.e., output-on-match or output-on-mismatch. A storage cell which produces an output when there is a match between the stored and search bits is designated as type #1 while type #2 is used to describe a basic memory cell which produces an output on a mismatch condition. The relative merits of implementing an associative processor

with a type #1 or type #2 memory cell will depend upon the functional and organizational requirements of the system. It will become apparent from the discussion which follows and that presented in section 5 that the output-on-mismatch cell has the greatest logical power and is therefore, best suited for performing the various search and processing operations.

This section presents detailed descriptions of the principal memory cell configurations under investigation at this time. In each case, the channel and control conductor patterns are illustrated, the techniques for performing write, read, erase and test for match operations described, and the basic characteristics - speed, size, power - specified for the present and improved designs based on potential advances in the DTPL technology. The method or interconnecting type #1 cells and type #2 cells to form simple memory arrays concludes the discussion. A more complete analysis of array organizations for the several search and processing operations follows in section 5.

4.2 Preliminary Type #1 Cell Design

A first design of an associative memory cell based upon the single cell per bit concept is shown in 25 times actual size in Figure 26a and schematically in Figure 26b. The structure is included in this discussion for the purpose of illustrating the design improvements, principally in areas of size and complexity, which have been made in the course of the program. Since this design progressed no further than the "drawing board" a detailed analysis of its operation will not be considered. A brief discription of the configuration should, however, be of interest to the reader.

Referring to Figure 26b we observe that all of the basic DTPL elements - gates, transfers, diodes etc. are contained in the network, the total count

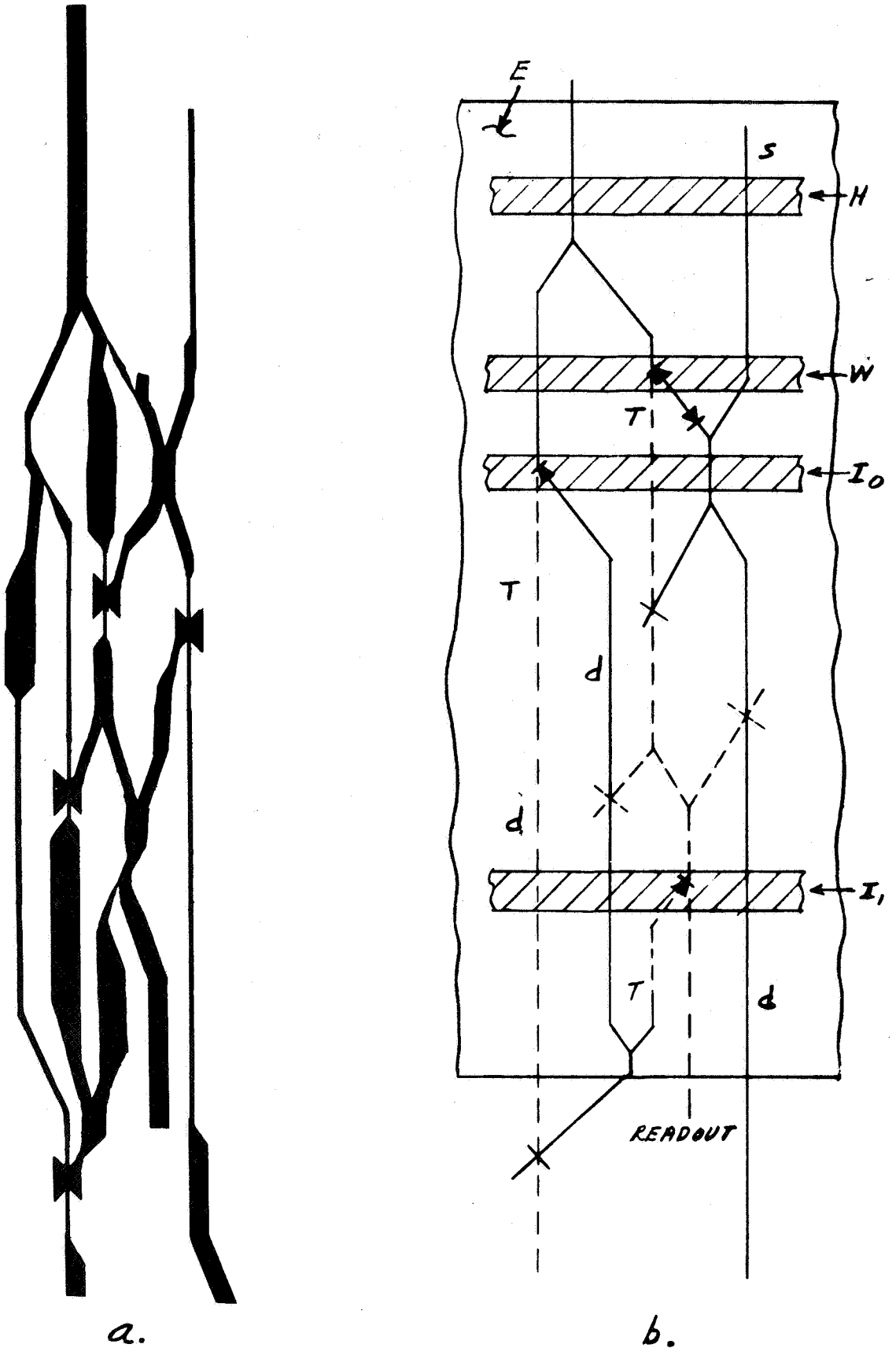


Figure 26 Preliminary type #1 memory cell-channel pattern at 25X (a) and schematic representation (b).

being 15 elements excluding the delay and storage channel segments. Five control conductors are required for the operation of the cell. Three of conductors - Interrogate 1 (I_1), Interrogate O (I_0), and Write (W) - are used to activate the punch through elements; one conductor - Hold (H) - is used to hold the stored bit of the cell during a general erase operation and one conductor - Erase (E) - is used to partially erase a region of the memory cell during the controlled erase of a stored bit. The latter operation is described in section 4.3 as it is also utilized in the improved type #1 storage cell.

While no attempts were made to reduce the size of the structure in Figure 26, the length and width dimensions --.275 inches and .060 inches -- represent a reasonable solution to the design problem caused by the three transfer elements T and delay segments d. A memory array density of 60 bits per square inch is implied by the above figures. With a delay per bit for writing, reading, etc. of $\sim$10 μsec and word format consisting of, for example, 100 serially interconnected storage cells, memory cycle times for search operations would approach 1 msec.

The memory cell designs described next offer significant advantages in terms of density, speed and power.

4.3 Improved Type #1 Basic Memory Cell

4.3.1 General Description

A second output-on-match memory cell is depicted in Figure 27. This design represents the result of an effort to improve the preliminary configuration and is one of the two principal cell structures considered in the mechanization of the various search and processing operations described in later sections. In addition to requiring one less control conductor, the design in Figure 27 makes use of a two-input inhibit gate and eliminates two of the inhibit gates, a delay and one of the space-consuming film-film

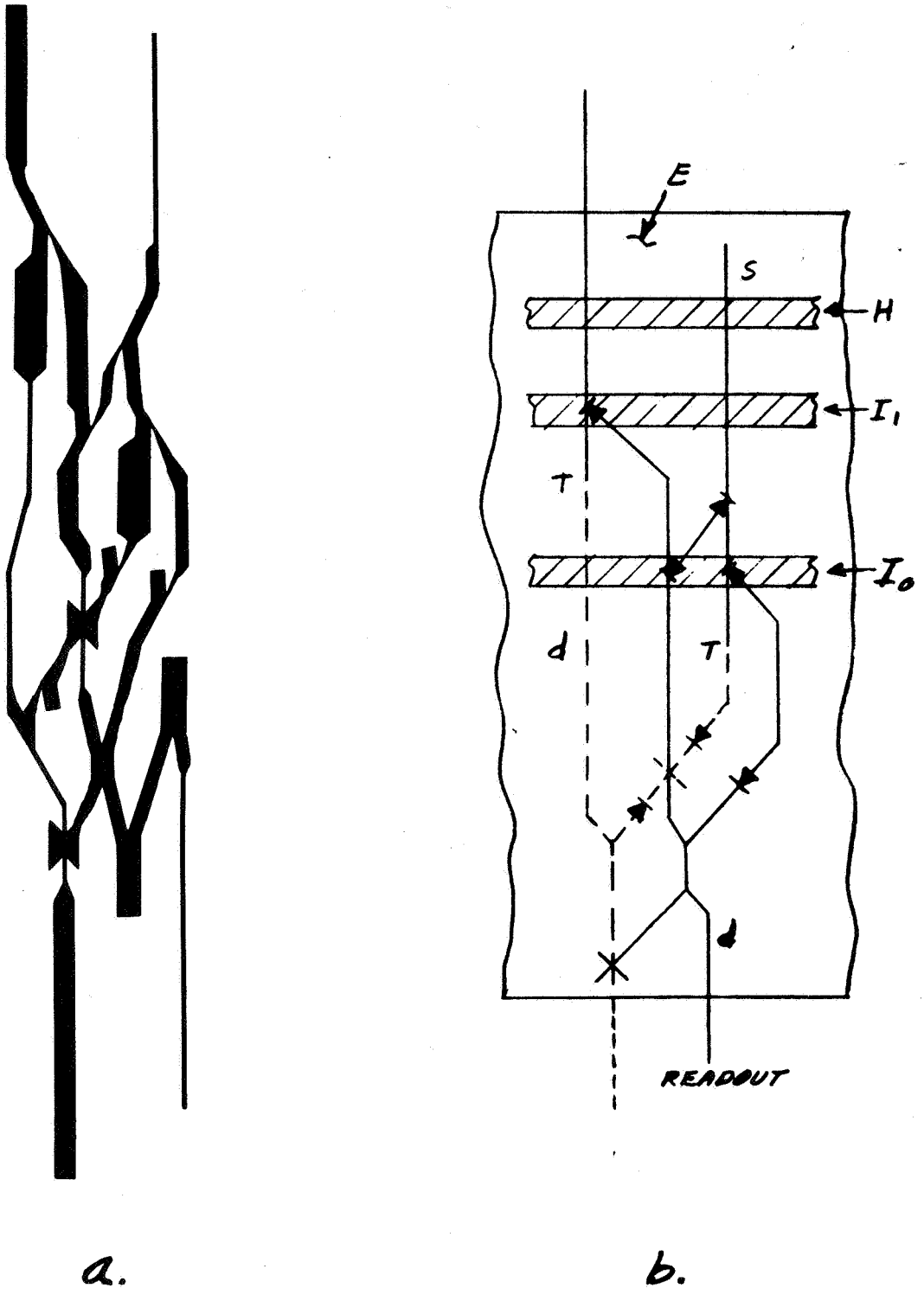


Figure 27 Improved type #1 memory cell-channel pattern at 25X (a) and schematic representation (b).

transfer elements of the previous storage network (see Figure 26). This has led to a significant reduction in the size of the memory cell to .190 inches by .045 inches. An array density of ~ 120 bits per square inch is obtained with a delay per bit of ~8 μsec. The eventual fabrication of both magnetic layers and control conductors upon a single substrate and the use of punch-through transfer elements, only recently developed, will make possible a further reduction in these demensions and a 4 μsec delay per bit. These improvements will be described at the end of this section.

The memory cell under consideration is redrawn in Figure 28 along with the timing diagram of the required drive and control fields. Pertinent logic elements and channel segments have been numbered to assist the reader in following the detailed description of the cell operations.

4.3.2 Cell Operations

Write To perform a write operation, a domain of reversed magnetization must be present in the word channel (see Figure 28) which interconnects all bits of a memory word. This domain may be introduced during a word select or "on match" operation. To write a 1 into the cell then, a general drive field is applied and interrogate lines I_1 and I_0 are energized. This has the effect of "activating" punch-through elements numbered 1 and 2 (see Figure 28a), thereby permitting a domain tip to propagate from the word channel to the storage channel S via channel 3 and diode 4. A general erase field occurs next coincident with a holding field which is only effective at S due to a specially-shaped hold line. This erases (resets) the magnetization in all of the channels "switched" by domain tip propagation except S wherein a domain of reversed magnetization is now stored. To write a 0, neither I_1 nor I_0 are pulsed during the above cycle and the cell remains completely erased.

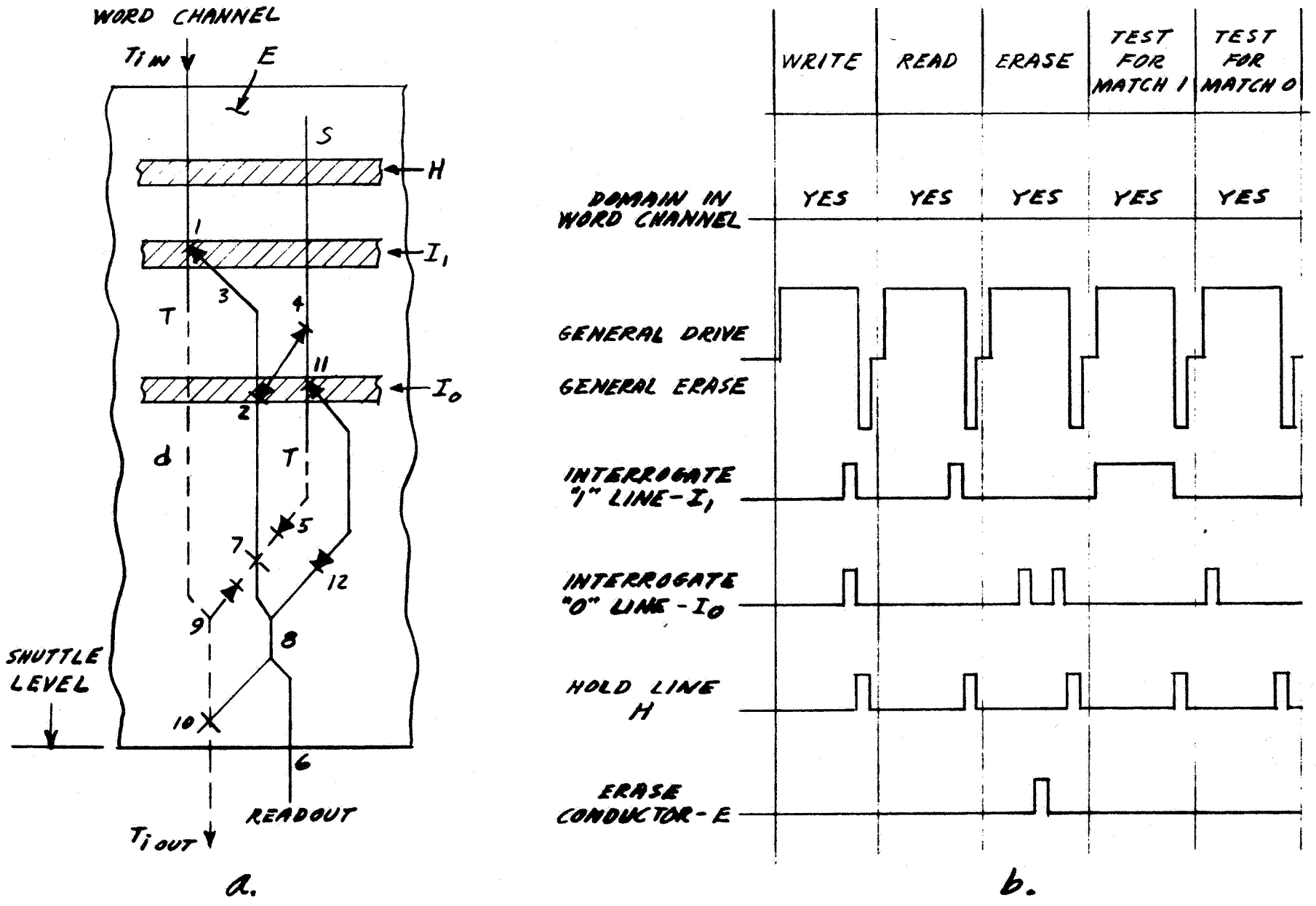


Figure 28 Improved type #1 memory cell (a) and timing

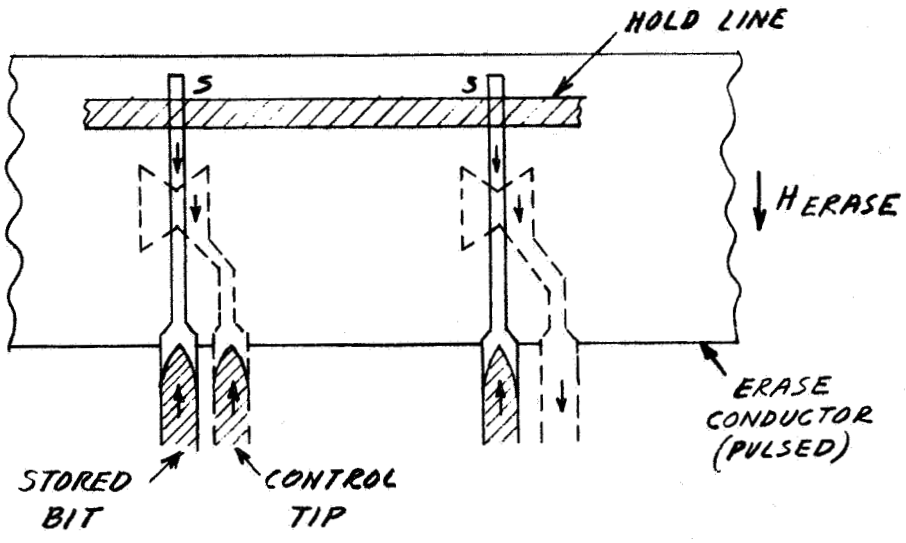
The pulse sequence for the Write operation is depicted in the timing diagram of Figure 28b. To minimize the power consumed in this and other operations when possible, the interrogate pulses I_1 and I_0 are of a short duration in comparison to the general drive field and, therefore, must be delayed with respect to onset of the latter to insure that a domain tip propagating in the word channel has reached punch-through element 1 of the cell. More critical timing is required if the minimum pulse width to operate a punch-through element is utilized since I_1 and I_0 are physically displaced in the memory cell.

Read In the memory cell depicted in Figure 28a, channel 6 is designated as the readout channel. To obtain a readout of the information stored in channel S, punch-through element 1 must contain a domain via the word channel as in the case of write operation. With the general drive field applied, I_1 is pulsed, causing punch through of a domain tip into channel 3. If no domain is stored in channel S, i.e., the cell is in the 0 state, the tip in channel 3 propagates through the main channel of gate 7 and fanout 8 to the readout station. An output during a read operation thus represents a binary 0. If, on the other hand, a domain is present in channel S, i.e., the cell is in the 1 state, a tip will propagate from S through diode 5 to gate 7 and inhibit the other tip propagating from channel 3, thereby preventing a readout. The absence of a readout signal, therefore, implies that a 1 is stored in the cell. A general erase and hold operation, which preserves a stored domain if initially present, occurs next completing the read cycle, In this manner, readout is non-destructive.

The timing diagram (Figure 28b) illustrates the pulse sequence required to perform this read function. It is important that the I_1 pulse occur after the general drive field is energized in order to prevent a race condition at gate 7 involving domain tips originating in the word and storage channels.

Erase. The technique used to perform an erase operation in this and other associative memory cells is described as "tip shuttling." Basically, what occurs is as follows. A local erase conductor is pulsed following entry of a control tip into a storage cell. This has the effect of partially erasing the stored information to the extent that upon termination of the erase pulse, the stored information is prevented from returning to the storage channel by the action of the control tip in an inhibit gate. The sequence is illustrated in Figure 29. In part a, two cells are shown during the time the local erase conductor is energized, one in which a stored bit is to be erased by means of a control tip, the other in which a stored bit is to be retained since no control tip is introduced. When the erase pulse is terminated, the situation in part b of Figure 29 results. The tip in the left storage channel is inhibited by the control tip and the right storage channel is completely switched by domain tip propagation. A subsequent general erase and hold operation will cause complete erasure on the left and leave a domain of reversed magnetization at S on the right.

The local erase conductor for the memory cell is shown in Figure 28a. Except for a short segment of channel 6 designated as the shuttle level in the figure, the conductor encompases the entire channel structure. The control tip required in the erase operation originates in the word channel and enters the memory cell and erase gate 7 via fanout 9. The complete sequence of events in this operation is as follows. A general drive field is applied propagating a control domain tip (resulting from a word select or on-match operation) through the entire word channel. At that time, I_0 is energized. Assuming that the cell contains a stored bit, the latter causes an output from punch-through element 11 which, under the influence of the general drive field, propagates through diode 5 and fanout 8 into channel 6. The local erase conductor is then pulsed, erasing The entire cell up to the shittle level where tips remain in the word



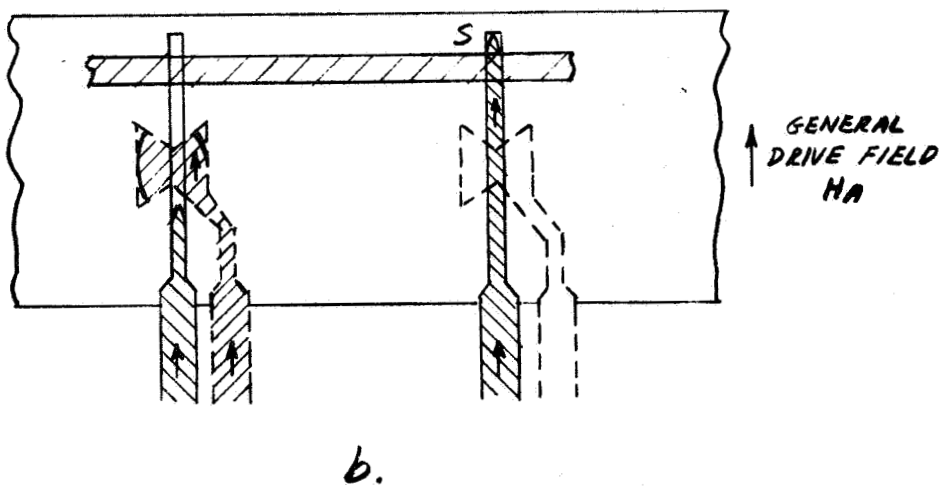


Figure 29 "Tip shuttling" erase technique.

channel and channel 6. When this pulse terminates (general drive field still applied), the aforementioned domain tips propagate back into the cell via fanouts 8 and 9. Since the propagation delay from the shuttle level to gate 7 through fanout 9 is less than the delay from the shuttle level to the main channel of 7 via fanout 8, the control tip will arrive at 7 in time to inhibit propagation from channel 6 to punch-through element 2. In order to prevent erasure in the memory cells of other words crossed by the same local erase conductor, i.e., of the same bit slice, I_0 is energized for the second time in the cycle. This enables the information (domains) in those cells to be rewritten into the storage channels by way of punch-through element 2 and diode 4. This is not the situation in the cell being erased since no domain is present at 2 when I_0 is pulsed due to the inhibit at gate 7. A general erase and hold operation follows, and the cell in question is completely erased. All other memory cells of that bit slice retain their original information. The pulse sequence for this operation is reviewed in the timing diagram.

Test for Match (Equality). A type #1 memory cell, as previously described, produces an output when a match exists between the stored bit X_i and the corresponding bit of a search word S_i. In the cell design depicted in Figure 28a (and in the other memory cell configurations to be discussed), the test for match is performed, for the most part, by energizing interrogate line I_1 when $S_i = 1$ or line I_0 when $S_i = 0$. The Boolean function which describes the output of the i^{th} cell during a test for match operation is given by

$$T_{i_{out}} = T_{i_{in}} \cdot X_i \cdot I_{1_i}(S_i) + T_{i_{in}} \cdot \overline{X_i} \cdot I_{0_i}(\overline{S_i}) \qquad (8)$$

where $T_{i_{in}}$ and $T_{i_{out}}$ are tips which enter and exist, respectively, the input and output segments of the word channel depicted in Figure 28a.

The input tip $T_{i_{in}}$ will hereafter be referred to as the "test" tip and the output tip $T_{i_{out}}$ as the cell output.

Referring to equation (8), it is seen that the first term represents the conditions which must be satisfied to obtain an output on a test for match 1 while the second describes the conditions for an output on a test for match 0. In each case, then, the cell must function as a three-input AND gate. The manner in which these tests for match are performed is as follows:

Match 1 - To test for match 1, a test tip is introduced into the word channel under the influence of a general drive field and interrogate line I_1 is energized. When the tip reaches element 1, a second tip is punched through into channel 3 and propagates to the main channel of gate 7 as the test tip continues in the word channel toward fanout 9. If the cell contains a stored bit ($X_i = 1$) in channel S, i.e., a match condition exists, at this point in the cycle a domain would be present in gate 7 via diode 5 to inhibit propagation of the above second tip to gate 10 via fanout 8. As a result, inhibit gate 10 remains unswitched and the test tip proceeds through fanout 9 and the main channel of gate 10. A cell output then occurs indicating that the conditions for a match 1 have been satisfied.

If the cell was in the 0 state ($X_i = 0$), i.e., no domain was present in channel S at the beginning of the match operation, inhibit gate 7 would remain unswitched during the above sequence of events. In this case, the "second" tip punched through element 1 into channel 3 would propagate uninhibited through the main channel of gate 7 through fanout 8 to gate 10. Since the propagation delay between elements 1 and 10 via the word channel is greater than the delay via channel 3 and fanout 8, the "second" tip

arrives at inhibit gate 10 before the test tip and inhibits the latter. Thus, no output occurs in agreement with the mismatch condition. A general erase and hold completes the cycle and the stored information is retained for subsequent search or processing operations.

In summary, the test for match 1 is basically a self-inhibit operation with the test tip being "split" into two paths by the interrogate line I_1. If the cell is in the 1 state, the stored tip prevents the self-inhibit and an output results. If the cell is in the 0 state, the self-inhibit on the test tip takes place and no output results.

The required sequence of drive, control and erase-hold fields for this match operation is presented in the timing diagram. With reference to the timing of the I_1 pulse, it must be emphasized that I_1 must be energized at the time the test tip reaches punch-through element 1. If a pulse of short duration is utilized to conserve power, accurate velocity techniques must be developed to fix the position of a tip in a word channel at any time during the general drive operation. At this time, the more conservative approach of wider I_1 pulses is advisable to insure proper operation of the cell.

Match 0 - The test for match 0 is less complex than the test for match 1 described previously in that only one inhibit gate (gate 10) is required to realize the function $T_{i_{out}} = T_{i_{in}} \cdot I_{0_i} \cdot \overline{X_i}$. To perform this operation, a test tip, $T_{i_{in}}$ is propagated in the word channel and interrogate line I_0 is energized. If the cell contains a stored bit ($X_i = 1$), a tip is punched through element 11 and propagates to gate 10 via diode 12. The test tip is then inhibited at 10 and no cell output occurs. If, however, a match condition exists ($X_i = 0$), no tip is

restrictions on the I_{1_i} pulses in the read operation also arise from the fact that a test tip must enter each memory cell. Thus, a timing sequence similar to the write cycle is utilized.

To perform the local erase with I_{0_i} pulses of duration $T_{I_{min}}$, these pulses are delayed until the entire word channel is switched by the test tip. I_{0_i} interrogate lines are then energized simultaneously in the sequence shown in Figure 28b. The local erase is pulsed accordingly.

The situation is not the same for the test for match 1 operation. In this case, I_{1_i} must be "on" when the test tip reaches cell X_i. Two modes of operation are then possible. One requires that the location of the test tip in the word channel during the general drive cycle be determinable. Each I_{1_i} driver would then be energized at the appropriate time for the minimum duration, $T_{I_{min}}$, and the test for match 1 performed. The special sequencing of drivers requires additional electronics. A more suitable approach would be to energize all I_{1_i} conductors at the beginning of the general drive cycle and terminate each when the cycle is complete. Maximum power is consumed in this manner, but the operation is easier to implement.

The test for match 0 sequence requires only that the I_0 line be energized before the test tip reaches the cell. Thus, $T_{I_{min}}$ man be utilized (see Figure 28b.)

4.3.3 Memory Array

In order to simplify the illustrations of memory cells and arrays in the remaining sections of this report, the configuration shown in Figure 30 will be adopted as the standard schematic representation of a type #1 associative memory cell. Referring to the figure, it is noted that a diode

present at 11 when I_0 is pulsed. Gate 10 remains unswitched and test tip $T_{i_{in}}$ propagates through the main channel of the gate, producing a cell output $T_{i_{out}}$.

The cycle ends in the usual manner with a general erase and hold sequence to preserve the original state of the cell. This is illustrated in Figure 28b. It is to be noted that the test for match 0 is the only operation in which an interrogate pulse may terminate before a test of control tip in the word channel reaches the memory cell.

An additional comment is in order concerning the timing of interrogate pulses as illustrated in Figure 28b. The power consumed during the various cell operations depends upon the number of control conductors energized and the duration of the current pulses. In the type #1 memory cell, all operations are performed by means of a test tip. In most cases, one or both of the interrogate pulses must coincide with the presence of this tip at the cell. The method of interconnecting cells to form a word, described in the next section, implies that the test tip will not be present at all bits of a word simultaneously. Thus, in order to minimize power by utilizing interrogate pulses of minimum duration herein denoted by $T_{I_{min}}$, special consideration must be given to the timing sequence.

In the write operation, the interrogate conductors may be energized at any time after the test tip has propagated past the cell. This delay is necessary to prevent a self inhibit in the word channel. To avoid special sequencing of each bit slice, the appropriate I_0 and I_1 lines would be energized simultaneously at the end of the general drive cycle (see Figure 28b) after the test tip has propagated through the entire word. In this manner, $T_{I_{min}}$ can be utilized and power minimized. The

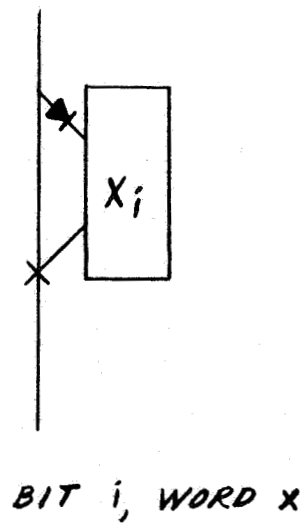


Figure 30 Simplifier schematic representation of improved type #1 memory cell.

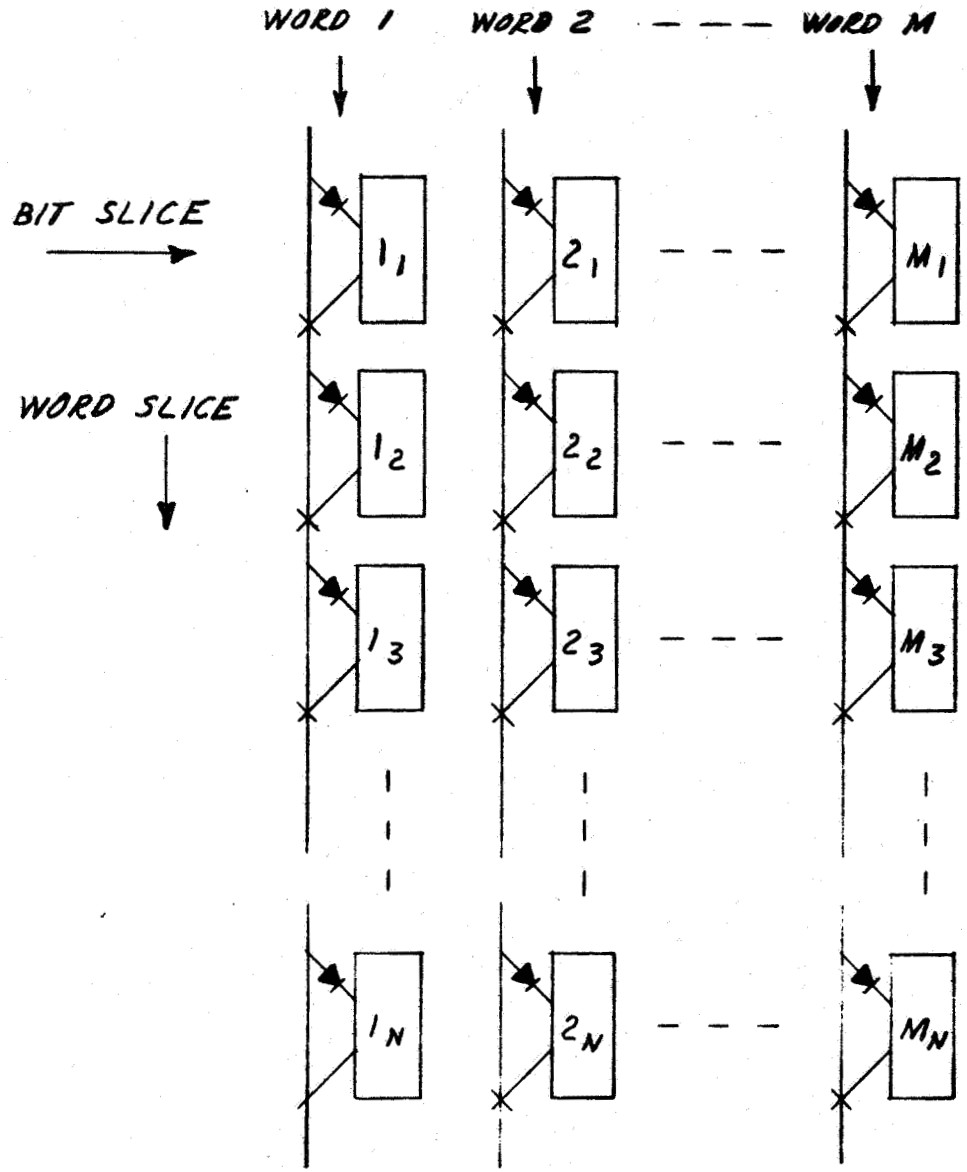


Figure 31 Basic associative memory array of type #1 cells.

is contained in the input channel of the cell, although this is not the case in the actual cell (refer to Figure 27). The diode is intended to illustrate the fact that the cell contents X_i cannot be read out into the word channel.

The basic method of interconnecting these memory cells to form an array is schematically depicted in Figure 31. Word slices run vertically and bit slices horizontally in the figure. It is seen that a word channel interconnects all bits of a word in a serial manner. Thus, the outputs from all cells during test for match operations are effectively ANDed together in the word channel. The additional cells and logic configurations required for search and processing operations are not shown at this time. More complete arrays for these purposes will be presented in section 5.

An experimental evaluation of the type #1 memory cell was performed using a simple two-word, two-bits-per-word array. The DTPL film structure was fabricated by means of the superimposed film technique (see section 6.2) and the conductor pattern prepared in the usual manner using printed circuit techniques. Figure 32 represents a composite of the channel and conductor patterns for this array at five times actual size. Six readout channel configurations, four for the stored bits and two for the words, are located at the lower portion of the network to facilitate electronic sensing of outputs by means of inductive pickup loops. The hold conductors are specially shaped to prevent storage of information in the word channels.

Initial testing was performed using the Kerr magneto-optic effect and the standard DTPL pulse-generating equipment. Control conductors located under the film element (see Figure 32) were energized in the appropriate sequence to produce the localized diode punch-through fields. These, in addition to a uniform drive field, enabled the write, store,

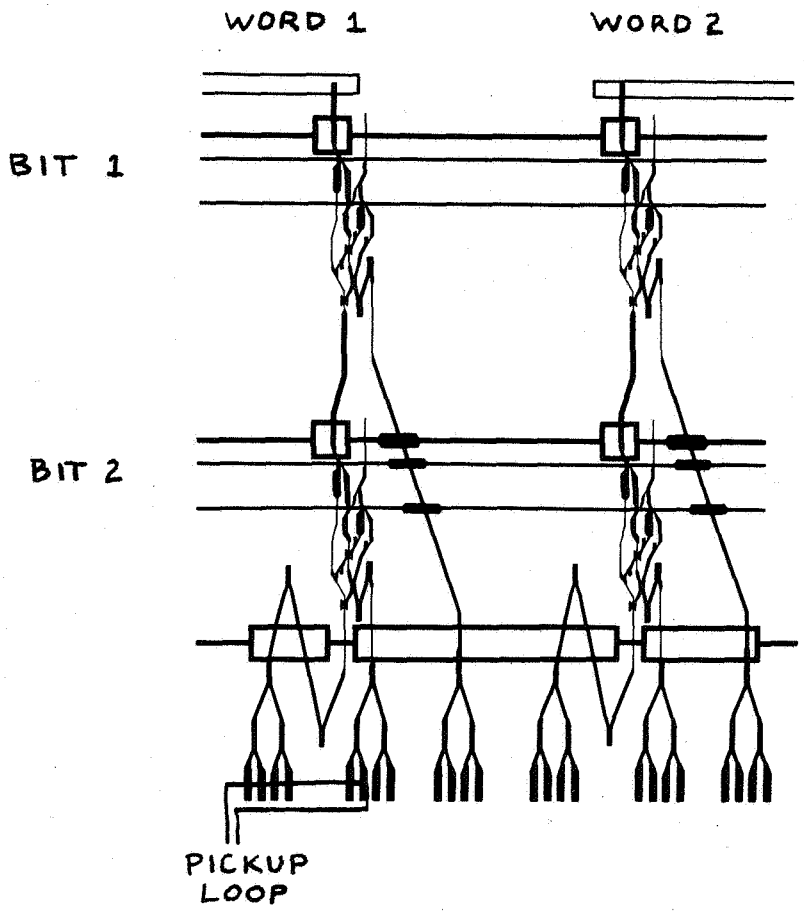
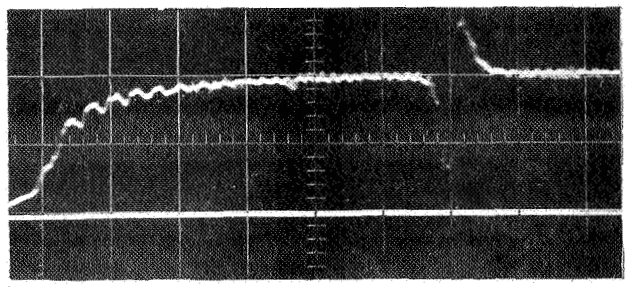


Figure 32 Composite of channel and conductor configurations a 5X of experimental memory array - ype #1 cells

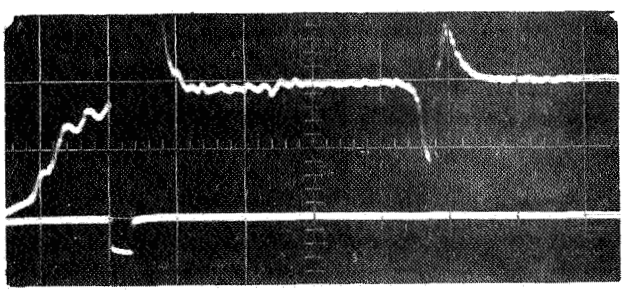
read, test for match 1 and test for match 0 operations to be performed. Typical readout signals obtained during the test for match operations are presented in the photographs of Figure 33. In this case, the pickup loop was positioned as shown in Figure 32 in order to distinguish between the word 1 and bit 2 (of word1) outputs which occur during the same general drive cycle. The large and small bipolar signals in the upper trace of the photographs thus correspond to the word and bit outputs respectively. The lower trace displays the current in the I_0 or I_1 interrogate line, depending upon the test for match being performed.

To begin with, Figure 33a shows the word channel output when a test tip, nucleated at the top of word 1, is propagated through bits 1 and 2 without energizing any of the interrogate lines. This is equivalent to a "don't care" or masked condition in the two memory cells. The output during a test for match 1 performed on bit slice 2 with a 1 stored in memory cell 2 is illustrated in Figure 33b. The photograph shows the I_1 interrogate line being energized for 3 μsec and the domain tip readout signal signifying a match condition. No output from bit 2 is obtained in the memory cell readout channel since I_0 is not pulsed and an inhibit takes place at the two-input gate. When a test for match 0 is carried out on bit slice 2 with a 1 stored in cell 2 of word 1, no word channel output results as shown in Figure 33c, due to the mismatch conduction. A bit output is obtained since I_0 is pulsed.

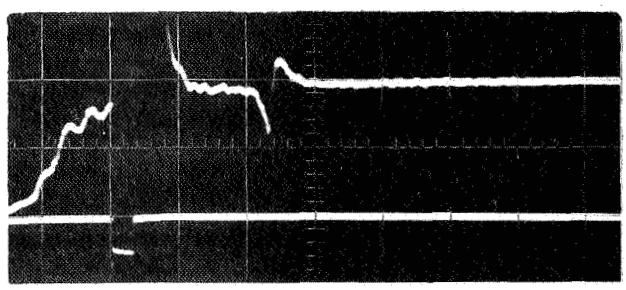
The tests for match 1 and 0 performed when a 0 is stored produce the output signals presented in Figure 33d and 33e respectively. In the former operation, the mismatch produces no word out. However, a tip readout is observed in the cell output channel. This appears as a result of uninhibited tip propagation from the punch-through element at the input of cell 2 through the main channel of the two-way inhibit gate into the



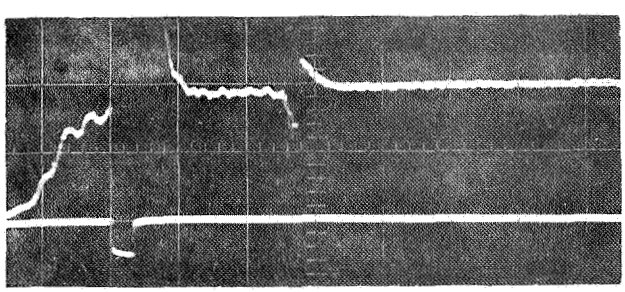
(a)



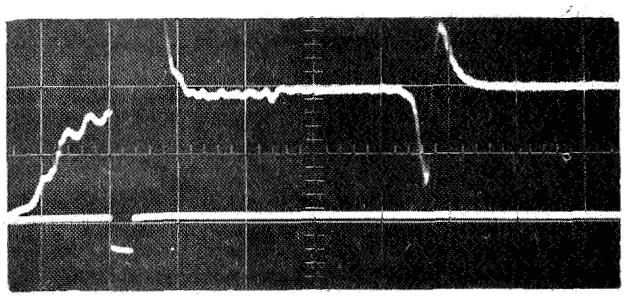
(b)



(c)



(d)



(e)

Figure 33 Readout signals from experimental array in Figure 32 - (see text).

readout channel. Finally, the test for match 0 produces the match signal shown in the last figure. No cell output appears since no information enters the cell during this operation and the network was initially erased.

The electrical readout technique was also utilized to determine the delay per bit for match operations which was found to be 10-15 μsec, depending upon the magnitude of the uniform drive field.

4.3.4 Improvements

The DTPL punch-through transfer logic element was described in section 2.2. This channel structure, no larger than the diode itself, can be employed in the type #1 memory cell to perform the film-film transfer function thereby eliminating the need for the space-consuming film film transfer elements presently utilized.

Figures 34a and 34b schematically depict the memory cell under consideration and the modified design employing the punch-through transfers in place of elements 1, 2 and 11. It can be seen that the elimination of T_1 and T_2 in this manner requires a change in the channel configuration contained in the individual magnetic layers, although the overall network remains the same. Removal of T_2, in particular, makes possible a .020 inch reduction in cell size, while the absence of T_1 simplifies the problem of achieving adequate propagation delay in the word channel for the test for match 1 operation.

The film-conductor separation which results in a DTPL superimposed film memory-logic device must be considered in the design of the channel

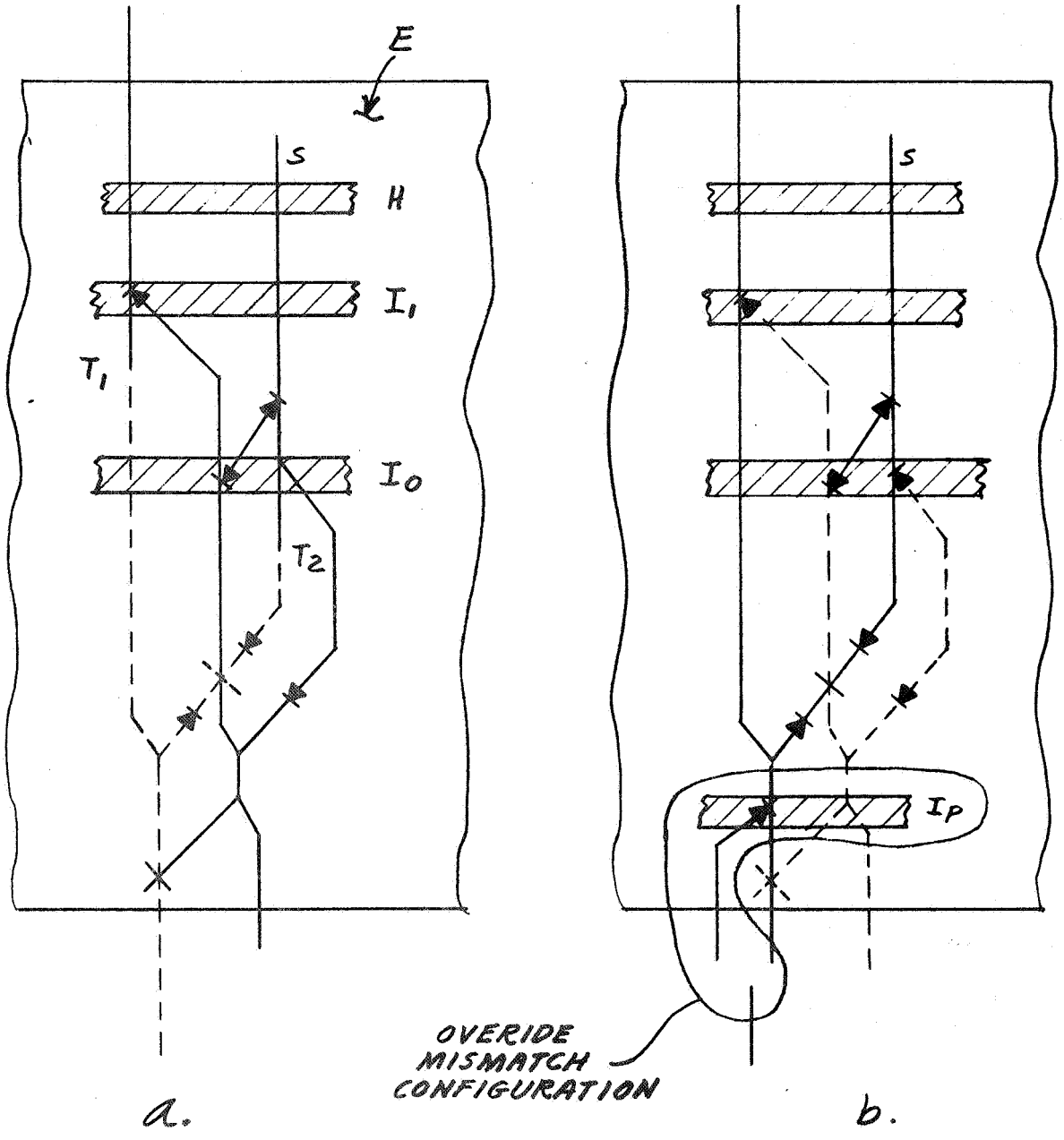


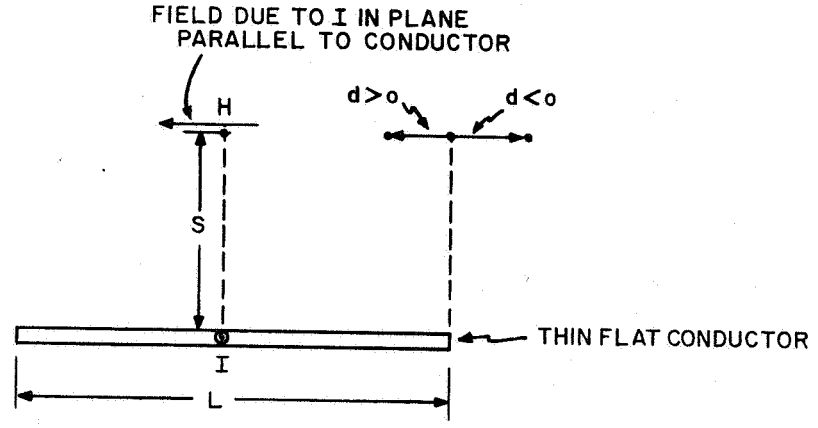
Figure 34 Schematic representation of type #1 memory cell (a) and modified design employing punch-through transfer elements (b).

configuration for the device. For example, adjacent, independently-controlled, punch-through elements designated as A and B must be adequately separated on the film plane in order that the fringing fields from the control conductor for element A do not affect the operation of element B. Another problem results when it is required to hold information in one of two neighboring channels crossed by the same hold line. In this case, the hold line must be specially shaped to reduce the fields in the appropriate channel.

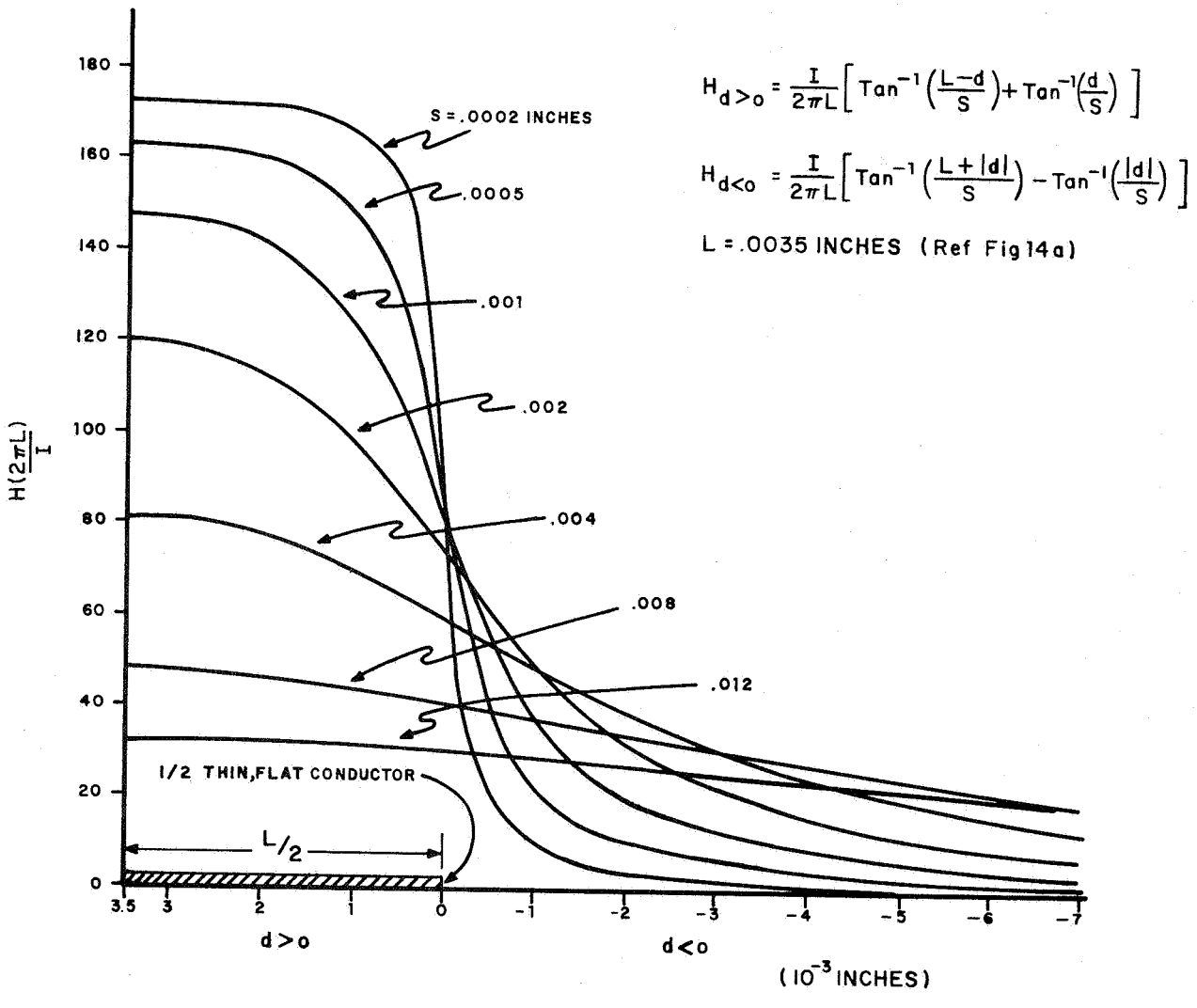
These factors have been taken into consideration in the design of the type #1 memory cell shown in Figure 27a. In this network, punch-through elements 1 and 2 (refer to Figure 28a) are spaced .020 inches from diode 4 in order to reduce the fringing fields from interrogate lines I_1 or I_0 at the diode. In determining a suitable separation, use was made of the calculated distributions of fields in planes above a current carrying flat conductor which are presented in Figure 35. The film-conductor spacing parameter S is then approximately equal to the thickness of a film substrate which is about .010 inches.

A multilayer structure in which both magnetic layers and control conductors were fabricated on a single substrate would solve the problem of fringing fields. In this case, S would be approximately .0002 inch (the thickness of an insulating layer required between magnetic film and conductors) and the field from a control conductor would be concentrated above the conductor (refer to Figure 35, S = .2 mils). Under these conditions, the spacing between the punch-through elements and diode 4 in the memory cell could be reduced to $\sim$ .005 inches, thereby reducing the overall length of the cell by .030 inches.

The use of a multilayer structure would also simplify the hold conductor



(a)



(b)

Figure 35 Geometry for calculation of field distribution above current carrying flat conductor. (b) Distribution of H field for configuration in part a.

design since the field above the conductor would then be inversely proportional to its width. An additional .025 inches reduction in cell length could be achieved in this manner.

Combining the improvements possible with punch-through transfer elements and those just described, a net cell length reduction of .075 inches is obtained. The final dimensions would then be .120 inches x .045 inches, which yields an array density of 185 bits per square inch. A delay per bit of 4 μsec is attainable under these circumstances.

One final point is made concerning the configuration in Figure 34b. It is seen that an additional punch-through element and associated control conductor may be incorporated in the cell design. The purpose of this modification is to obtain an "override mismatch" capability. Then in the operation of the cell, an output is possible on a mismatch if I_p is pulsed. This facility is useful for the proximity search to be described in section 5.

A discussion of the type #2 DTPL associative memory cell is presented next.

4.4 Type #2 Basic Memory Cell

4.4.1 General Description

The type #2 output-on-mismatch DTPL memory cell structure presently under investigation is shown at 25 times actual size and schematically in Figure 36. This cell design is unique in that no film-film transfer elements are required in the channel configuration. An additional feature is the "1 generator" depicted in Figure 36b. A 1 generator is a channel segment which behaves as a source of domains of reversed magnetization as a

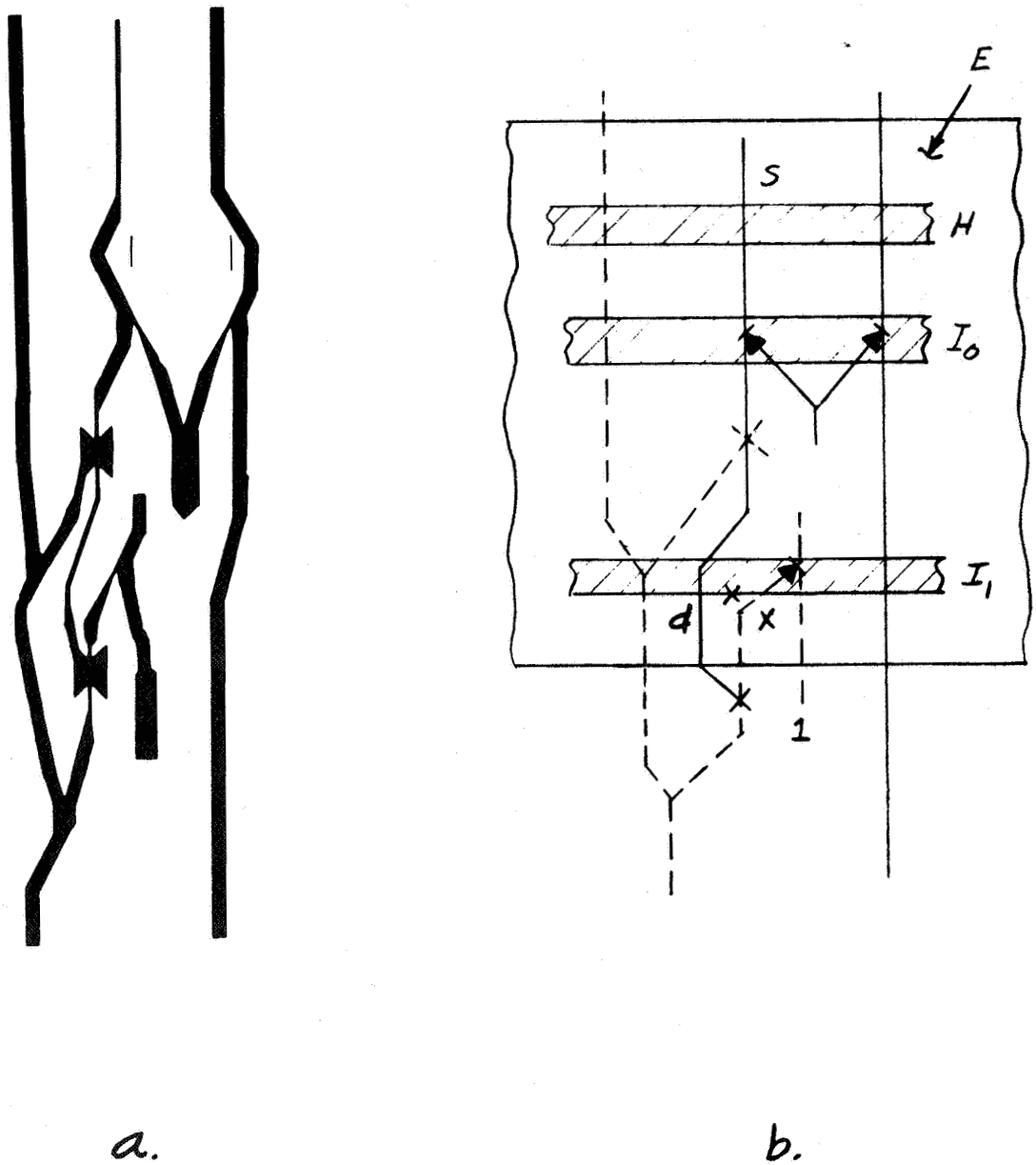


Figure 36 Type #2 memory cell - channel pattern a 25X (a) and schematic representation (b).

result of the stray fields associated with an intentially-created discontinuity in the low coercivity magnetization. This discontinuity is obtained by selectively photo-etching a hole through the magnetic layer within the channel. The wiring pattern for the cell consists of two interrogate lines, I_1 and I_0, an erase conductor and the usual hold conductor.

The channel and control conductor designs shown in Figure 36a are based upon a superimposed-film implementation of the memory cell. Due to the significant film-conductor spacing which characterizes this type of multilayer structure, special attention must be given to the placement of punch-through elements and interrogate lines and the shape of the hold line as previously described in section 4.3, "Improvements." This leads to a cell which is larger in size than the component logic elements would imply. In the design of Figure 36, the length x width dimensions are .160 inches x .050 inches, yielding a memory array density of 125 bits per square inch. Since no narrow channel delays are located in the mismatch output channels (refer to Figure 36b), the delay per cell can be minimized to $\sim$4 μsec. This compares quite favorably with the 8 μsec per cell figure for the type #1 cell illustrated in Figure 27. The use of improved multi-layer fabrication techniques will make possible a redesign of the type #2 cell of Figure 36 and a reduction in the delay factor to $\sim$2.5 μsec. The "Improvements" portion of this section contains a discussion of this and other pertinent subjects concerning the potential characteristics of this cell design.

A detailed description of the operation of the type #2 memory cell is presented next. It is suggested that the reader refer to Figures 37a and 37b which contain a specially-numbered version of the network schematic and a timing diagram for the various cell operations.

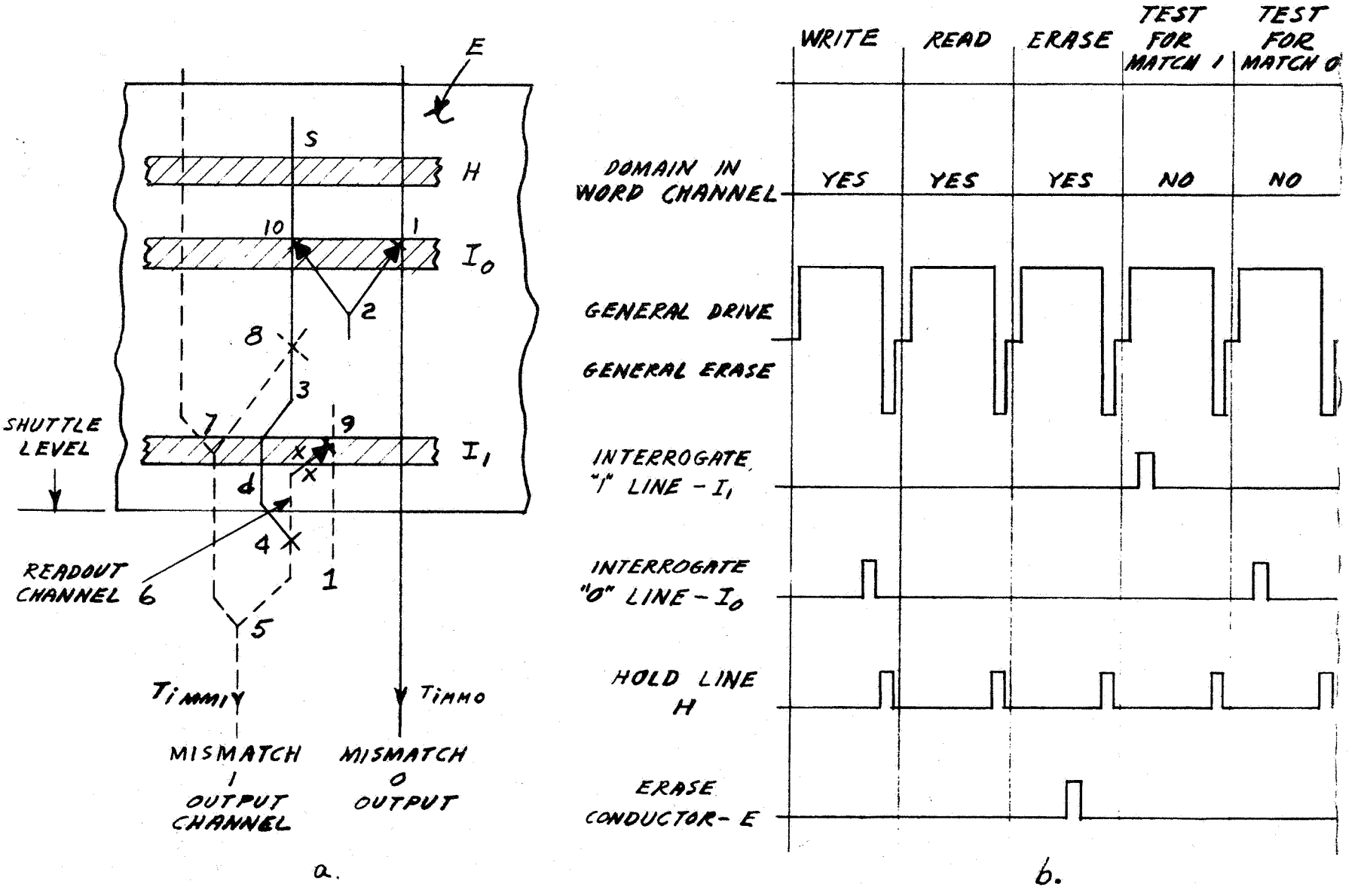


Figure 37 Type #2 memory cell (a) and timing diagram (b).

4.4.2 Cell Operations

Write. In the write operation, a domain tip is propagated in the mismatch 0 output channel by means of a general drive field. If a 1 is to be written into the initially erased cell, interrogate line I_0 is energized when that tip reaches or passes punch-through element 1. This introduces a second tip into channel 2 which continues to channel S via element 10. A general erase and hold cycle occurs next, and a domain of reversed magnetization is stored in channel S as all other channels are erased. Since the binary 0 storage state is represented by a completely erased memory cell, I_0 is not energized in the above sequence when a 0 is to be written. The erase-hold operation is still required in order to erase the mismatch 0 output channel and preserve the 1's written into other memory cells. Figure 37b depicts the timing of the pulses required in the write operation.

Read. Referring to Figure 37a, it is seen that channel 6 is designated as the readout channel. The x's on either side of 6 represent the possible location of electrodes for a magnetoresistance readout element if this technique is employed. To perform the read operation, then, a general drive field is applied and a tip introduced and propagated in the mismatch 1 output channel. This tip will enter the cell via fanout 5 and continue to the readout location. If, at the beginning of the cycle, the cell contained a stored bit in $S(X_i = 1)$, then at this time gate 4 will be switched by a tip propagating from S via channel 3. An inhibit operation will take place at gate 4 and no output obtained. If the cell were in the 0 state when the read operation began, gate 4 will remain erased during the cycle, and a readout obtained. Thus, the presence (absence) of a domain of reversed magnetization in channel 6 indicates a 0 (1) is stored in the memory cell. Channel 6 cannot be erroneously switched by a tip from the "1 generator" since punch-through element 9 is not activated during this sequence of events.

The read cycle is completed in the usual manner by a general erase and hold as shown in the timing diagram. This retains the original information (if any) stored in channel S as the other channels are erased in preparation for subsequent operations.

Erase. The tip shuttling technique described in conjunction with the improved type #1 memory cell is also employed in performing a local erase in this cell design. Figure 37a depicts the shuttle level which coincides with the lower edge of the local erase conductor. The operation takes place as follows. A control tip is propagated in the mismatch 1 output channel by means of a general drive field as the stored domain to be erased grows through channel 3 to gate 4. When the control tip reaches or passes the shuttle level, the local erase conductor is pulsed erasing the contents of the cell and the mismatch 1 output channel up to the shuttle level. Upon termination of the local erase pulse the control and information tips propagate toward gate 8, the former via fanout 7, the latter via channel 3. With the propagation delays properly adjusted, the control tip will reach gate 8 first and inhibit propagation back into the storage channel S. If no control tip is present, the information tip propagates through the main channel of gate 8 into S to be retained during the subsequent general erase-hold cycle. Since the control tip is present in this case, the general erase and hold completely erases the memory cell including the mismatch 1 output channel.

The pulse sequence for the local erase is presented in Figure 37b. It is important to note that interrogate line I_1 is only energized one time during the cycle. In comparison, the type #1 cell utilizes two I_1 pulses to perform the same operation (refer to Figure 28b). The write and read sequences for the type #2 cell just described also require fewer control pulses.

Test for Match (Equality). A type #2 memory cell as defined in section 4.1 is one which produces an output on a test for match when a mismatch occurs between the stored and search bits. In the cell design under consideration, separate channels are required to collect the mismatch 1 and mismatch 0 outputs, $T_{i_{out\ mm1}}$ and $T_{i_{out\ mm0}}$. The latter are related to the stored bit X_i and the search bit S_i, represented by a current in I_1 if $S_i = 1$ or in I_0 if $S_i = 0$, by the following Boolean functions:

$$T_{i_{out\ mm1}} = I_1 \cdot \overline{X_i}, \quad T_{i_{out\ mm0}} = I_0 \cdot X_i \tag{9}$$

That no test tip is required in the test for match operation is apparent from equation (9). As a result of this important feature of the type #2 memory cell, the timing of control pulses I_1 and I_0 is not critical and the minimum pulse width can be utilized.

Match 1. In the match 1 operation, a cell output is required when the stored bit $X_i = 0$, i.e., channel S is erased. It is for this reason that the "1 generator" (see Figure 37a) is incorporated in the memory cell. To test for a match 1, the general drive field is applied and, after a short delay, I_1 is pulsed activating punch-through element 9. Since a domain of reversed magnetization is present in 9 from the 1 generator, the punch through operation produces a tip in channel 6 which propagates toward fanout 5. If the cell contained a stored bit ($X_i = 1$), gate 4 is, at this time, switched as a result of the tip which propagated from channel S via channel 3 before I_1 was energized. Thus, an inhibit will take place at gate 4 and no cell output occurs. If, however, the cell was initially erased ($X_i = 0$), a mismatch condition exists when I_1 is pulsed. Inhibit gate 4 remains unswitched, and the tip resulting from the punch-through element 9 propagates through the main channel of 4 into the mismatch 1

output channel. A general erase-hold cycle completes the match 1 operation as illustrated in Figure 37b.

Match 0. The match 0 operation does not utilize any inhibit gates and the interrogate pulse I_0 need not be delayed with respect to the general drive field. To perform the match 0, the general drive field is applied and I_0 energized activating punch-through element 10. If $X_i = 0$, channel S is erased and no output will occur. If $X_i = 1$, the conditions for a mismatch are satisfied (equation (9)) and a tip is punched through element 10 by I_0. Under the influence of the general drive field, this tip then propagates into the mismatch 0 output channel via channel 2. The usual general erase-hold occurs next and the stored bit is held in channel S.

Reviewing the timing diagrams for the type #1 and type #2 memory cells presented in Figures 28b and 37b respectively, it is seen that the write, read, and local erase operations are performed with fewer control pulses (I_1, I_0) in the type #2 structure. Furthermore, no test tip is required in the test for match operations using a type #2 cell. As a result, the minimum width interrogate pulse may be employed in both the test for match 1 and match 0 operations. Thus, on the average, less power is consumed in performing the basic cell operations with a type #2 DTPL memory cell.

4.4.3 Memory Array

The simplified schematic representation of a type #2 associative memory cell is presented in Figure 38. This configuration will replace the more detailed representation depicted in Figure 36b in the remaining illustrations describing arrays of this basic storage cell for performing search and processing operations. In the figure, the channels between the cell and the

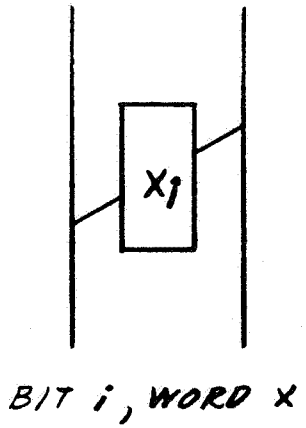


Figure 38 Simplified schematic representation of type #2 memory cell.

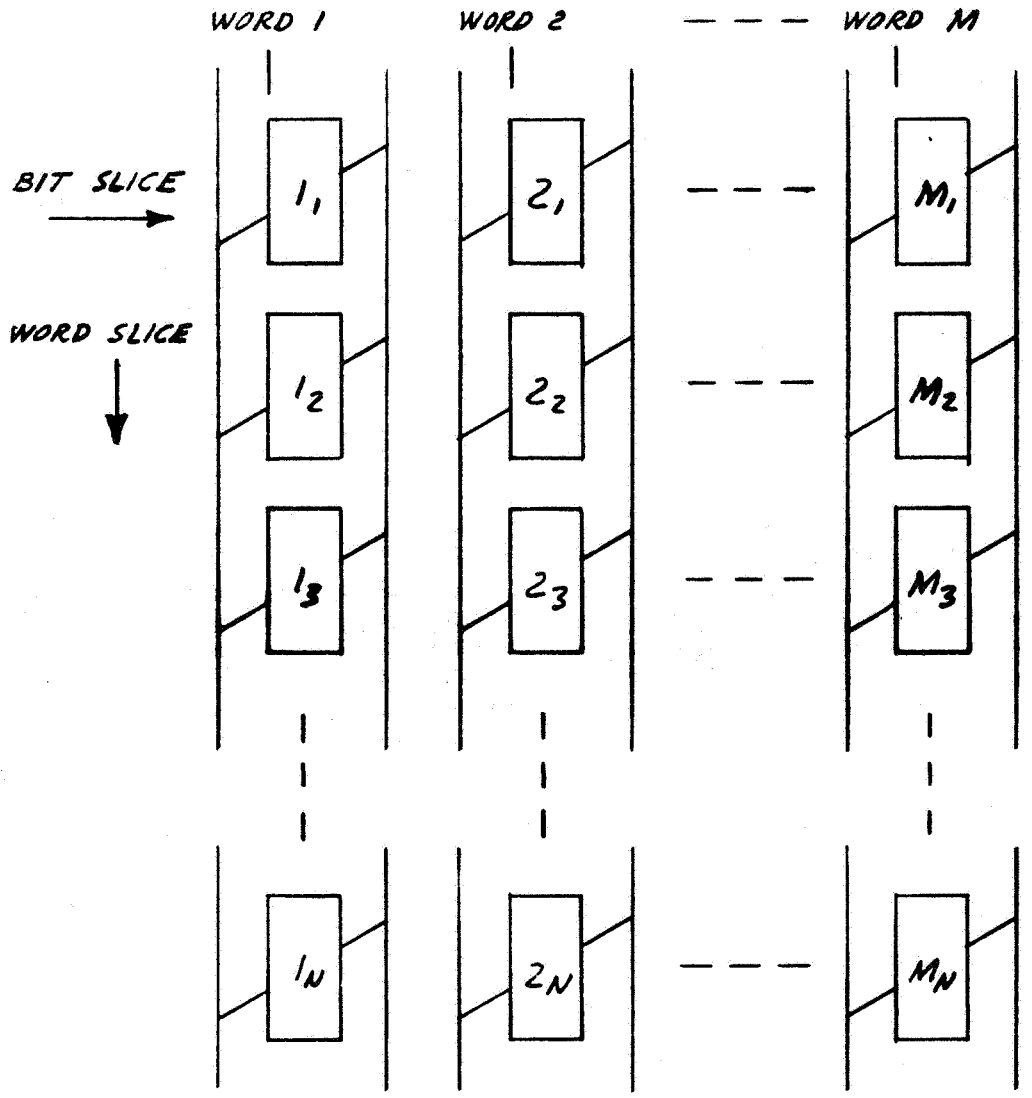


Figure 39 Basic associative memory array of type #2 cells.

mismatch 0 and 1 output channels are shown as bidirectional paths. It is recalled that domain tips normally propagate into and out of the cell in the mismatch 0 and 1 output channels.

The interconnection of these cells to form the basic array is schematically depicted in Figure 39 where the word slices run vertically and the bit slices horizontally. It is noted that a mismatch 0 and mismatch 1 output channel interconnect all bits of a word in what is effectively a parallel organization. Thus, the outputs from all cells of a word slice are ORed together in the two mismatch output channels. In contrast, the outputs in a word slice of an array of type #1 memory cells are ANDed in the word channel.

A small 2 x 2 array of type #2 storage cells has been prepared for evaluation. Figure 40 shows, at five times actual size, a composite of the channel and conductor patterns for this array. The network contains only two readout configurations, each representing the ORed outputs from the mismatch 1 and 0 output channels of a word. While complete testing of the structure has not been performed at this time, proper operation of the 1 generators has been verified. Based upon the successful performance of the type #1 cells in the first array evaluated (refer to section 4.3.3), no technical problems are expected in the operation of the configuration of Figure 40. The complete evaluation of that array will be performed early in the second half of the program.

4.4.4 Improvements

Several improvements are possible in the design of the type #2 memory cell shown in Figure 36a. To begin with, use of a multilayer structure would permit a reduction in the separation between the hold and I_0 interrogate

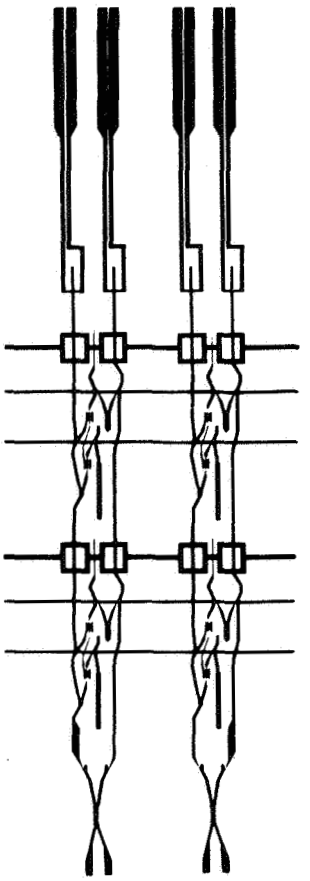


Figure 40 Composite of channel and conductor configurations at 5X of experimental memory array - type #2 cells.

lines (refer to section 4.3.4) from .040 to .010 inches. The channel structure could be compressed an additional .030 inches in the length dimension and .010 inches in the width dimension to produce a final cell size of .090 inches x .040 inches. This implies a potential array density of 275 bits per square inch. The delay per bit would then be approximately 2.5 μsec.

A design change is also required to obtain a more suitable readout channel. The schematic representation of the basic type #2 cell is presented again in Figure 41a. It can be noted that the read channel is not readily accessible by sense lines. By shifting the position of the 1 generator and adding a fanout element in channel 6, the improved configuration shown in part b of Figure 41 is obtained. More optimum positioning of readout element electrodes is now possible in this case.

A summary and evaluation of the type #1 and #2 DTPL memory cells is presented next.

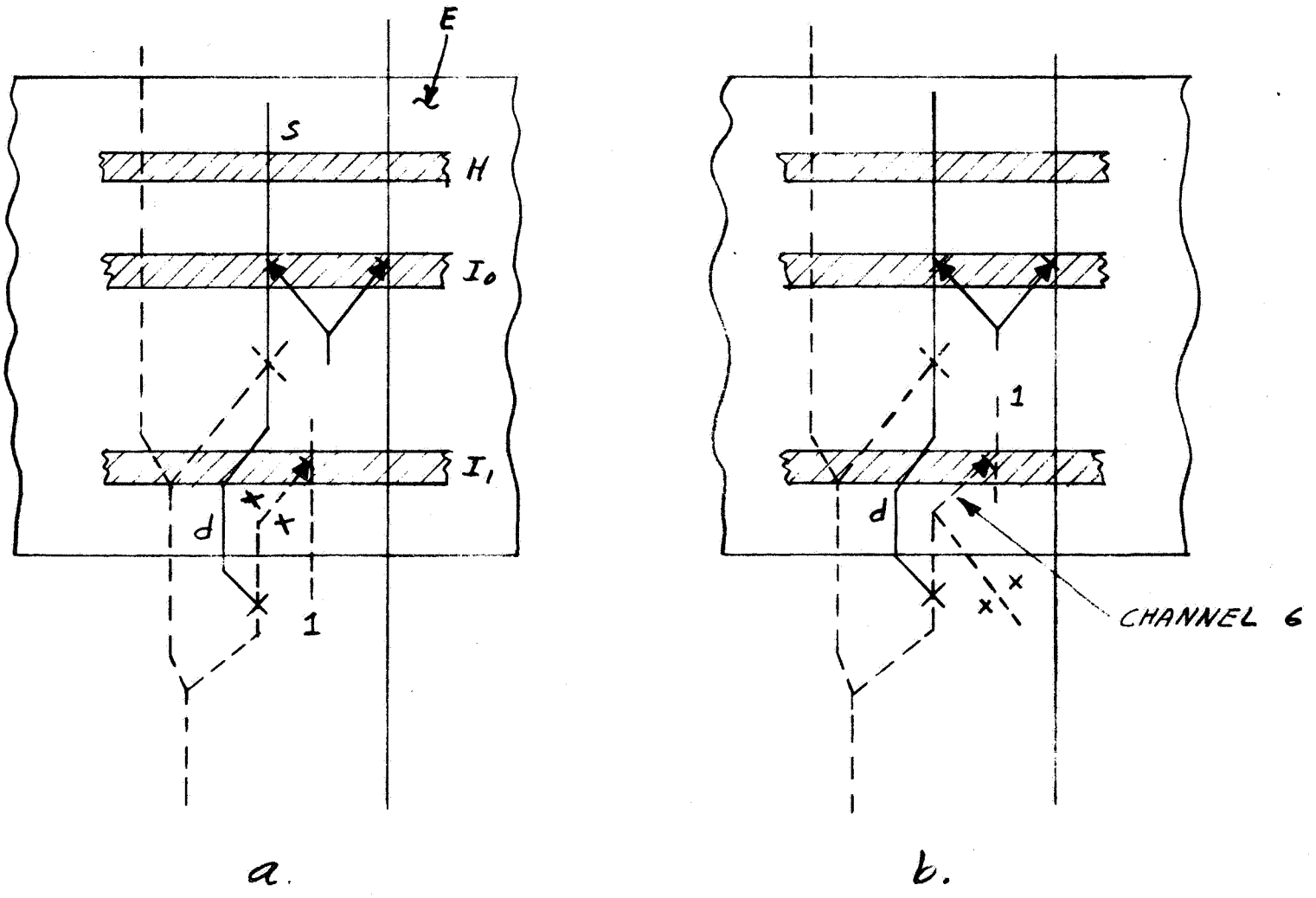


Figure 41 Type #2 memory cell (a) and design employing repositioned readout channel (b).

4.5 Summary

The following tables are presented as a brief summary of the DTPL associative memory cells under investigation. It is evident that the type #2 cell is superior to the type #1 configuration on the basis of the factors considered.

Cell Characteristics

Cell Type	Size	Array Density	Delay	Control Conductors
#1	.120" x .045"	185 Bits / in^2	4 μsec	Interrogate 1 = I_1 Interrogate 0 = I_0 Local Erase - E
#2	.090" x .040"	275 Bits / in^2	2.5 μsec	Same as Above

Cell Operations

	Write	Read	Local Erase	Test For Match 1	Test For Match 0
#1	H_A, Test tip I_1, I_0	H_A, Test tip I_1	H_A Test tip I_0, E	H_A, Test tip I_1	H_A, Test tip I_0
#2	H_A, Test tip I_0	H_A, Test tip	H_A, Test tip E	H_A I_1	H_A I_0

Word Slice Outputs (N cells - X_i), M_i = Match in i^{th} Type #1 Cell

#1	Test Tip $\cdot M_1 \cdot M_2 \cdot$ ------- $\cdot M_N$ (Logical AND in word channel)
#2	$X_1 + X_2 +$ --------- X_N - (Logical OR in mismatch 0 output channel) $\bar{X}_1 + \bar{X}_2 +$ --------- $\bar{X}_N$ (Logical OR in mismatch 1 output channel)

5. SEARCH AND PROCESSING OPERATIONS

5.1 Introduction

One of the more important features of a DTPL associative processor is its ability to perform search and processing operations simultaneously over all words with a minimum of external logic and storage. This comes as a direct result of (1) the memory-logic capability of the individual memory cells; (2) the fact that these cells are magnetically interconnected in a word structure permitting storage of search results in another cell without sensing; and (3) the ability to perform combinational logic within the storage medium as previously described in Sections 2, 3 and 4.

During the first half of the program, algorithms and techniques were developed for performing the basic search and processing operations normally required of a general-purpose associative processor. The searches considered are the following: equality, inequality, maximum (minimum), proximity, and the intersection and union of searches. Processing operations studied include field addition, operand addition, summation, counting, shifting, complementing, logical sum and logical product. In the discussion which follows, each of these operations is defined and the techniques for accomplishing them in arrays of type #1 and type #2 memory cells described. A word length of 100 bits is assumed for the purpose of determining the basic search time. Methods of processing the results of searches such as the resolving of multiple matches, generation of the address of a match word, and readout of the match words are also discussed. In each case, a memory size of 1000 words is assumed. The section concludes with a summary of the times required to perform all operations in the two arrays under consideration. It will be shown that an array of DTPL type #2 cells is most suitable for constructing an associative processor.

5.2 Search Operations

5.2.1 Equality Search

The capability of performing an equality search is required in most, if not all, associative memories for space applications.[3] This search is defined as the operation of finding all stored words which are equal to a search word in all unmasked bit positions. To describe this operation logically, we consider two cases: first, a memory in which the stored words M_1 are composed of N type #1 output-on-match memory cells; and second, an array of words M_2 composed of N type #2 output-on-mismatch memory cells. With the search word denoted by S, and the i^{th} search and stored bits by S_i and X_i, the Boolean expressions for the equality search are given by:

$$M_1 = S \text{ if } \prod_{i=1}^{N} (X_i S_i + \bar{X}_i \bar{S}_i) = 1 \tag{10}$$

and

$$M_2 = S \text{ if } \sum_{i=1}^{N} (X_i \bar{S}_i + \bar{X}_i S_i) = 0 \tag{11}$$

where $\prod$ and $\sum$ represent the logical sum and logical product. While equations (10) and (11) are equivalent, we associate the former with the type #1 cell and the latter with the type #2 cell for the following reason: The i^{th} terms represent the output of a cell during a match operation. We recall from sections 4.3 and 4.4 that in an M_1 word, the cell outputs are logically ANDed in the word channel; whereas the cell outputs in an M_2 word are logically summed in the mismatch output channels. Therefore, equation (10), which represents a logical product or AND (condition for all matches), is most applicable to stored words M_1; while the logical sum expression given by (11) (condition for no mismatches) is most suitable for stored words M_2.

Memory Array--Type #1 Cells. In a DTPL associative memory array composed of the type #1 memory-logic cells, the equality search consists of performing, simultaneously on all words, a series of test-for-match operations on all

unmasked bit slices during one general drive cycle. The operation can be described as "all parallel" since all bits are interrogated simultaneously. However, the actual tests for match are performed sequentially in a given word by a test tip which propagates from bit to bit in the word channel before reaching the match output channel.

Figure 42 schematically depicts the portion of a simplified memory array pertinent to the equality search operation. In the figure, the word slices run vertically and the bit slices horizontally. To perform the search, the nucleate line is pulsed and test tips are introduced into each word channel at location T. The first half of the test for match operation takes place as described in section 4.3 with the appropriate interrogate lines being pulsed as the test tip propagate down the word channels. In those words equal to the search word, i.e., in words which satisfy

$$\prod_{i=1}^{N} (X_i \cdot I_{1i} + \bar{X}_i I_{01}) = 1, \qquad (12)$$

the test tip propagates uninhibited through the entire word channel to the output channel. In the other words which contain one or more mismatches, the test tip is inhibited by the first cell containing a mismatch, and thus never reaches the output channel. With general drive field still applied, control line E is pulsed and the "match" tips are punched through elements F_1 into the flag bit memory cells f_1. A general erase and hold occurs next, erasing all channels while retaining all stored bits X_i and flag bits f_1. Thus, at the end of the equality search, a flag bit is stored in each word satisfying the search.

The minimum functional requirement of the flag bit memory cell is that it be possible to propagate the flag bit into the word channel for an on-match operation. We recall that the type #1 cell design is not provided with this capability. A second requirement is that the cell contain a readout configuration which makes it possible to generate an address for each word. These features are described in greater detail later in this section.

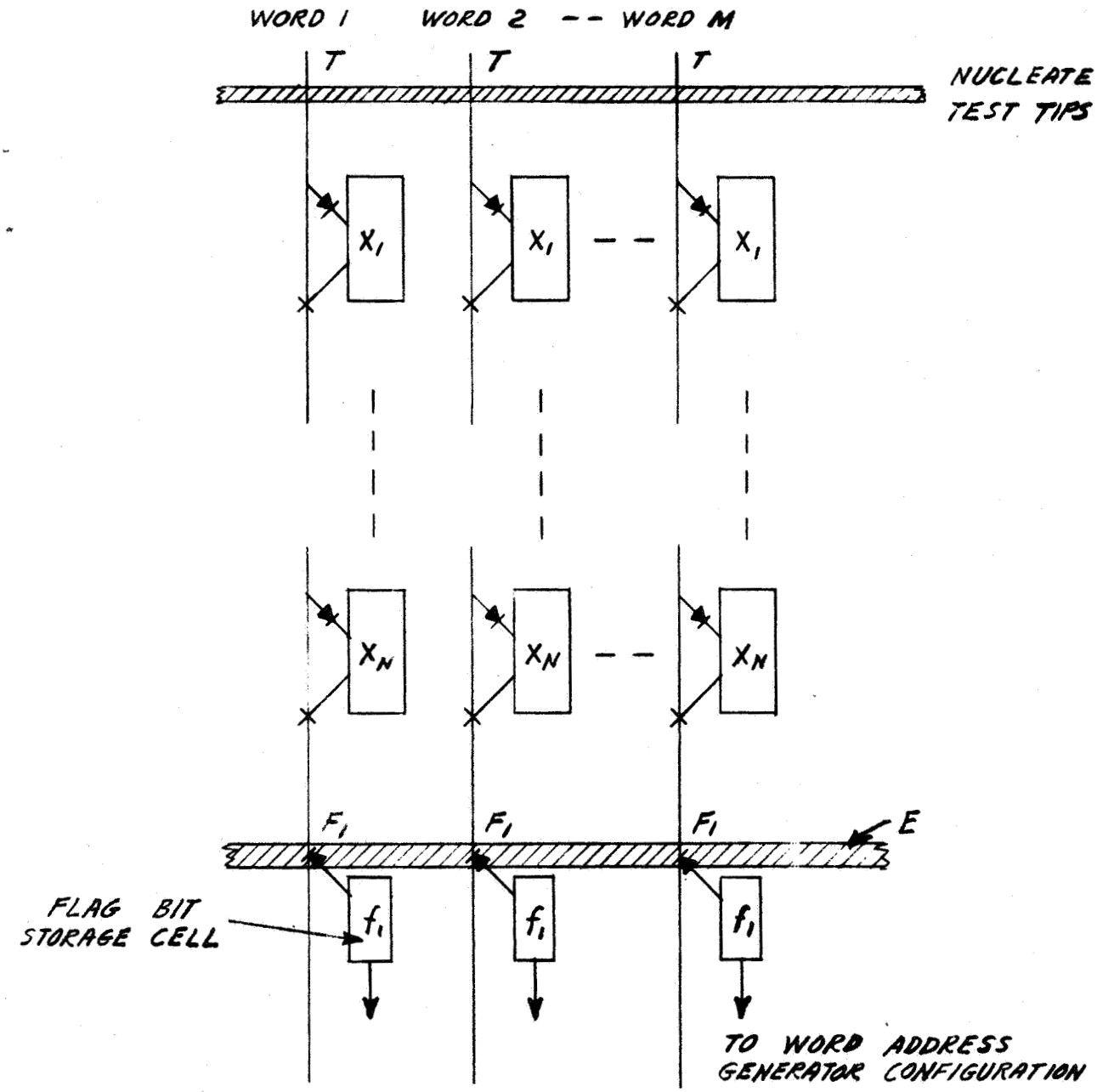


Figure 42 Memory array of type #1 cells and logic configuration pertinent to the equality search operation.

The time required to perform the equality search in the manner described above is equal to the propagation delay in the word channel from T to the output channel and is thus directly proportional to the number of bits per word of memory. Using the delay factor of 4 μsec per bit for the improved type #1 cell, a memory with a word length of 100 bits would, therefore, require approximately 400 μsec for an equality search. This figure can be significantly reduced by modifying the array design shown in Figure 42. For example, two "nucleate test tip" lines can be used, one at either end of the array, and the output channel and flag memory cells shifted to the center of the words. This would necessitate a 180° rotation of one-half of the memory cells and the addition of an AND gate per word at the input to the flag memory cell as shown in Figure 43. Thus, the two halves of the array would be searched in parallel and the results ANDed on a per-word basis before a match tip can be written into the flag bit memory cell. A 50 per cent reduction in search cycle time is possible in this manner.

The technique of dividing the bits of all words into two segments can be readily implemented if all of the bits of a given word are contained in one magnetic film plane. However, if multiple film planes must be utilized due to the size of the cells, or if further segmentation is desired on a given film plane, it must then be possible to logically AND the spatially-separated results of the individual equality searches at the time they occur if the overall search time is to equal the segment search time. This could be accomplished by electrical readout and comparison techniques, but the hardware cost would be prohibitive, e.g., one sense amplifier per search segment per word. A more suitable approach would be to use the galvanomagnetic transfer elements described in section 2.3 to rapidly transfer information (results of individual searches) across a film plane or between film planes to the DTPL AND gate for final processing. The trade-offs between search time and system complexity which result as the number of segments is increased and more transfer elements are employed have not been investigated. A study of this subject is planned for the second half of the program.

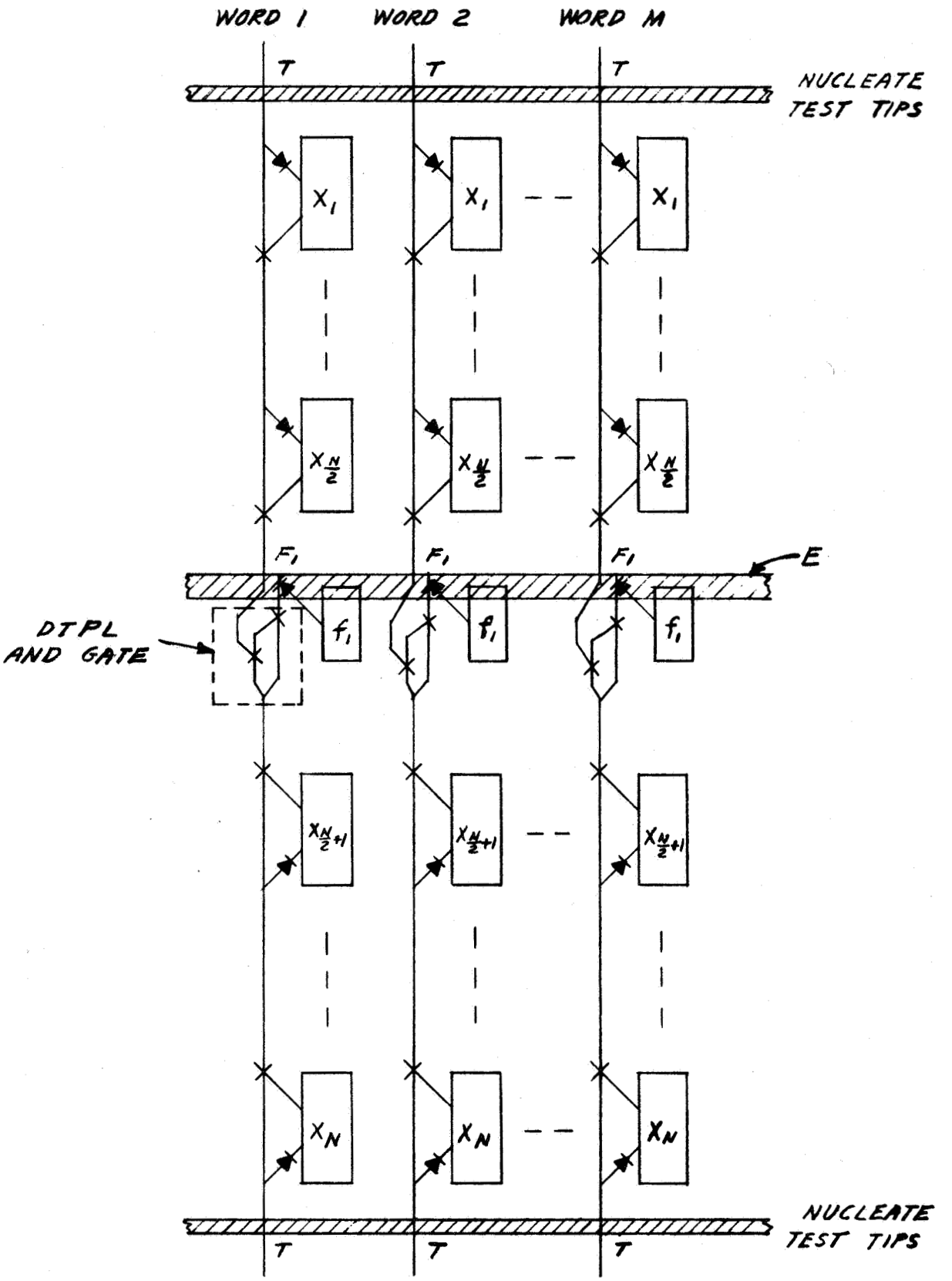


Figure 43 Modified array of Figure 42 for reducing equality search time.

Memory Array--Type #2 Cells. The configuration of type #2 cells and output channels required for the equality search are illustrated schematically in Figure 44. Referring to the latter, the word slices run vertically and bit slices horizontally. Collect mismatch 1 and 0 output channels for each word are ORed by fan-in elements 1. Gates 2, the 1 generators and the flag bit memory cells f_1 are used for inverting the mismatches to obtain the matches and storing these results.

To perform the equality search, a test-for-match operation is performed on all bits in parallel by energizing the general drive field and the appropriate interrogate lines as described in section 4.4. The words which are equal to the search word will satisfy

$$\sum_{i=1}^{N} (X_i I_{0i} + \overline{X}_i I_{1i}) = 0 \qquad (13)$$

and thus no tips will be present in the collect mismatch output channels. In the other words which contain one or more mismatches, one or both of the mismatch output channels will contain a domain tip which, under the influence of the general drive field, propagates to element 1 and into gate 2.

At this point in the cycle, the results of the search must be inverted and written into the flag bit memory cells. This operation is accomplished by energizing control lines E_1 and E_2. In the words which satisfy the search, gate 2 remains unswitched and an output tip from the 1 generator is written into the flag memory cell. In the words which contained a mismatch, gate 2 is switched and propagation to the flag cell is inhibited. Thus, no information is written into the flag cell. The usual general erase and hold complete the cycle. A flag bit is then stored in each word, satisfying the search.

The equality search cycle time is determined, for the most part, by the time required to propagate a mismatch output tip through an entire mismatch output

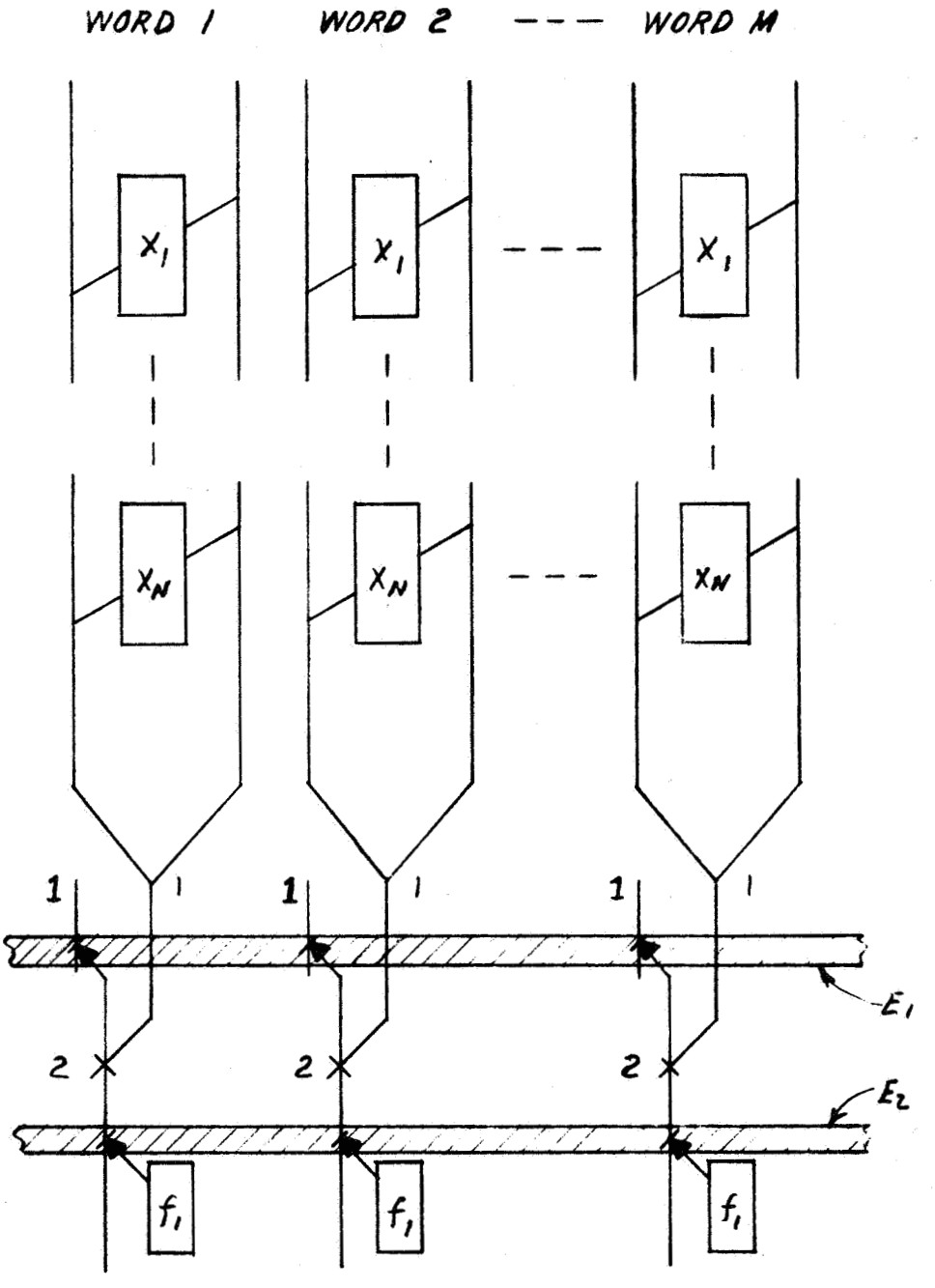


Figure 44 Memory array of type #2 cells and logic configuration pertinent to the equality search operation.

channel. With the delay per cell being about 2.5 μsec (refer to section 4.4), a word length of 100 bits would imply a cycle time of approximately 250 μsec. This figure can be halved by organizing the memory array to collect mismatches at the center of the word. This is depicted in Figure 45. Additional reduction in this search time can be realized using the techniques described previously.

5.2.2 Inequality Search

The inequality search is defined as the operation of finding the stored words X which are greater or less than a search word S. If we define X_d as the most significant bit in which $X_i \neq S_i$ then logically

$$X > S \text{ if } X_d = 1 \text{ and } S_d = 0 \tag{14}$$

$$X < S \text{ if } X_d = 0 \text{ and } S_d = 1. \tag{15}$$

The operation requires that the mismatch condition in the most significant bit for which $X_i \neq S_i$ be determinable. This requirement cannot be satisfied with type #1 cells since no output occurs for a mismatch. The opposite is true in the case of the type #2 cell.

Memory Array--Type #1 Cells. The method of performing the inequality search in this type of array is based upon an algorithm[4] applicable to an associative memory with an all-parallel equality search capability. The algorithm requires a number of equality searches equal to the number of 1's (0's) in the search word depending on whether a greater-than (less-than) search is being performed. No change in the memory array configuration utilized for the equality search is necessary.

The procedure for a greater-than (less-than) search is as follows:

1. Convert the least significant 0 (1) of the search word to a 1 (0).
2. Masking out all bits of lesser significance than the converted bit, perform an equality search with test tips in the standard manner. A flag

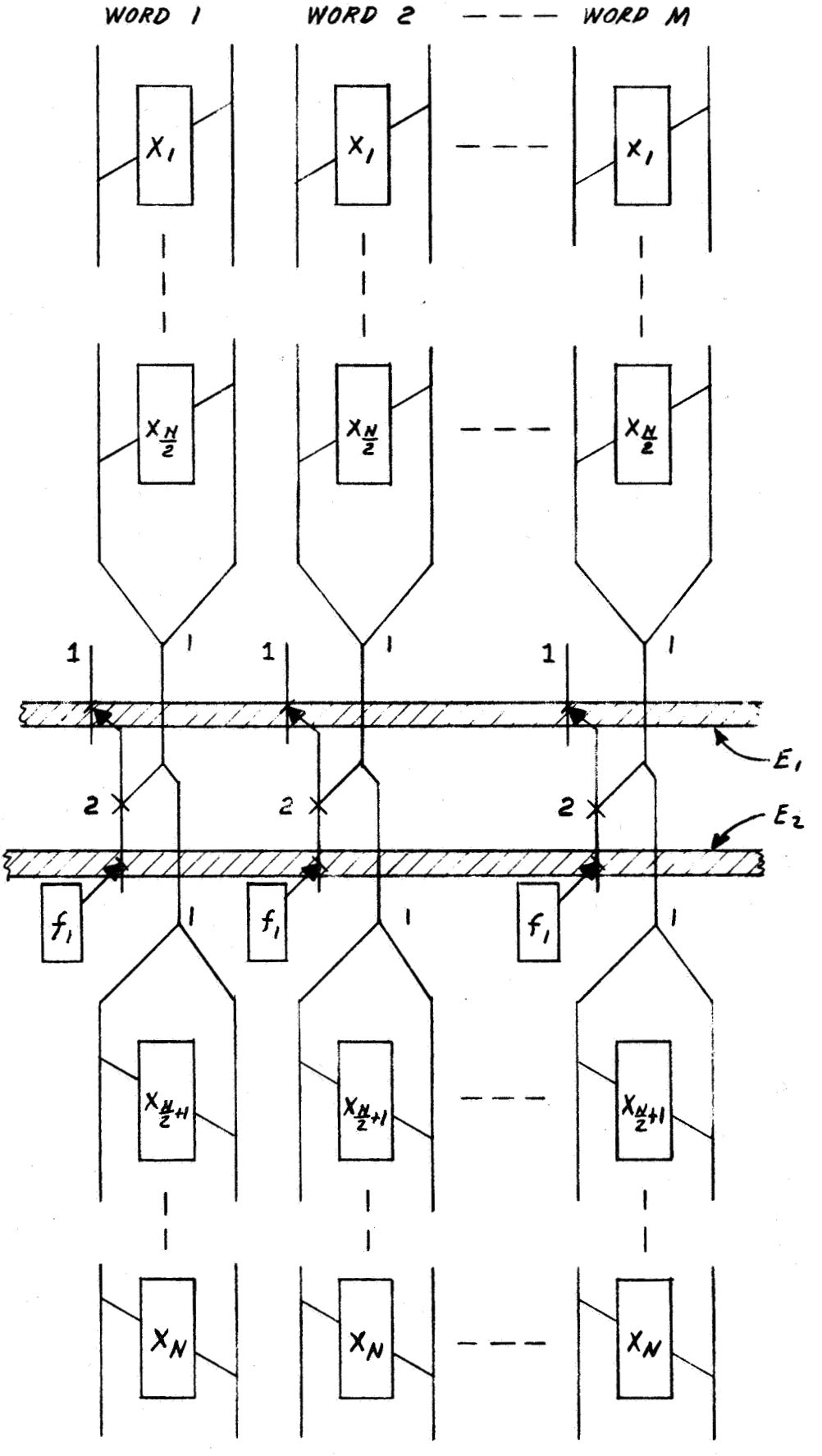


Figure 45 Modified array of Figure 44 for reducing equality search time.

bit is then stored, satisfying the search word (and remains therein through subsequent searches). These words are members of the set which is greater-than (less-than) the search word.

3. Repeat steps 1 and 2 until all of the 0's (1's) in the search word have been converted. At this point, all of the words satisfying these searches contain a flag bit. This is the complete set of words greater-than (less-than) the search word.

Since the number of 1's or 0's in the search word will change from one inequality search to another, the cycle time for this operation using the type #1 cells cannot be predicted. On the average, however, half of the S_i's will be 1. Thus, in a memory with a 100-bit word length, 50 equality searches will be required, on the average, to perform a single inequality search.

Memory Array--Type #2 Cells. The inequality search can be implemented quite readily using type #2 storage cells since the output signal (domain tip) not only indicates a mismatch condition but also identifies the type of mismatch which has occurred. This ternary output capability (mismatch 1, mismatch 0, no mismatch) greatly simplifies the task of distinguishing between greater-than and less-than mismatch conditions.

The procedure for performing the inequality search operation is based upon the results of an equality search performed on all bit slices of the memory in parallel. A mismatch in any bit of any word indicates an inequality which is represented by the presence of a domain of reversed magnetization in one or both of the mismatch output channels of a word slice. The type of inequality, greater-than or less-than, is determined by identifying the output channel containing the highest order (most significant) mismatch. In this operation, the domain tip representing the highest order mismatch is used to inhibit a lower order mismatch from reaching the inequality test location and thereby producing a false output.

Figure 46 depicts the now-familiar array of type #2 memory cells and the additional channel and control conductor configurations pertinent only to the inequality search operation. With reference to the figure, gate 1 (2) performs the function of inhibiting tip propagation to the inequality test location in the mismatch 0 (1) output channel when the most significant mismatch occurs in the mismatch 1 (0) output channel. Depending upon the search criterion, i.e., greater-than or less-than, control conductors I_G or I_L are energized to activate punch-through elements 3 or 4, enabling a "mismatch" tip to enter the flag bit memory cell f_1 for storage.

A typical inequality search takes place as follows: A test for match (first half of the equality search) is initially performed on all bit slices of the array in parallel. The mismatch 0 (1) output channel will contain a domain if at least one memory cell tested for a 0 (1) contains a 1 (0). If the highest order mismatch occurs in the mismatch 0 channel, then $X > S$; whereas $X < S$ if that output occurs in the mismatch 1 channel. Under the influence of a general drive field, output tips are propagated to the test locations at the end of a word nearest the most significant bit. If, for example, $X > S$, the output information will fan out at 5, propagate to gate 2 and inhibit any lower order output tip in the mismatch 1 channel. The fact that mismatch outputs from the different order bits are delayed is due to the physical distance between cells. It is this effect which makes the inhibit and thus separation of inequalities possible.

With the result of the search now contained in the $X > S$ channel, the final operation of writing into the flag bit storage cell takes place by energizing either I_G or I_L. If a greater-than search were in effect, the word in question satisfies this criterion and a domain of reversed magnetization is stored in the flag cell. If, however, a less-than search were being performed, no information is written into the flag cell since no output tip is present in the $X < S$ channel. The cycle ends with a general erase and hold.

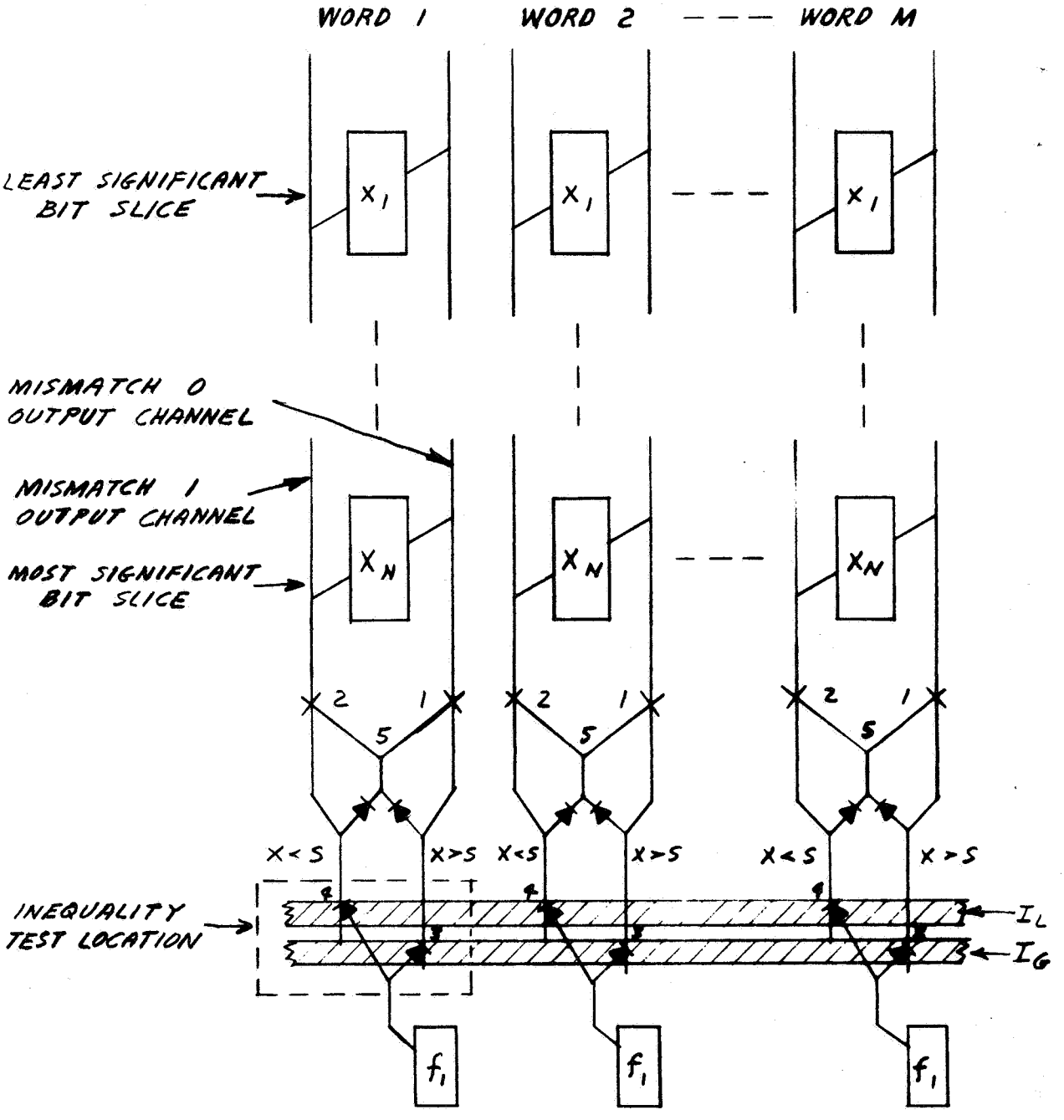


Figure 46 Memory array of type #2 cells and logic configuration pertinent to the inequality search operation.

The inequality search can be performed in the same cycle time as the equality search using the type #2 memory cell. Recalling the fact that approximately 50 equality searches are required using the type #1 cell, it is apparent that the implementation depicted in Figure 46 is the more suitable approach. Furthermore, the techniques which may be utilized to speed up an equality search (re-organization of the array, segmentation of bits, etc.) can be applied to the inequality search.

5.2.3 Maximum (Minimum) Search

The maximum (minimum) search is defined as the operation of finding the stored word which has the largest (smallest) magnitude. It is unique in that there is a dependency between words and no search word is required. The search must proceed in a bit-slice manner from the most significant end and requires that the output from a given bit slice comparison be used to operate logically on the succeeding lower-order bits. The following scheme, based upon a memory array incorporating a shifting capability within each word slice, has been conceived for performing the maximum (minimum) search operation.

To begin with, the contents of all memory cells are shifted, in parallel, one bit length per cycle, toward readout channels located at the most significant end of the words. A sense line interconnecting all words at that location performs an OR function of the outputs on a per-bit-slice basis, i.e., the sense line detects the presence of one or more 1's (domain tips) in successively lower-order bit slices as shifting operations progress.

When the bit slice containing the first 1 or 1's is sensed, a control line is energized. The latter performs the function of permanently inhibiting subsequent outputs in those words which do not contain a 1 in that particular bit slice. Each cycle in which 1 or more 1's are sensed results in a permanent inhibit (deletion from further consideration) of the words not containing a 1, but still "active" from the previous cycles. When no 1's occur, no inhibits result, and the active words

remain active. In this manner, the maximum word or words are those which are not inhibited, i.e., remain active after the least significant bit slice has been shifted to the readout channel and sensed.

To perform a minimum search, the complement of the information stored in each memory cell is operated on in the above manner. The word or words active at the end of the sequence are minimum, but appear as maximum as a result of the complementation.

Memory Array--Type #1 Cells. The word-slice shifting capability required for the maximum (minimum) search cannot be obtained using the type #1 memory cell. It is recalled (refer to section 4.3) that this design does not provide for a read-out of the stored information into the word channel within which the shifting operation would take place. The use of an additional control conductor to transform diode 4 shown in Figure 28 into a punch-through element would make this operation possible, but the availability of the complement remains a problem. For present purposes, modification of the type #1 cell will not be considered since it will only increase the complexity of the channel structure. Other methods of performing the search will be investigated.

Memory Array--Type #2 Cells. The type #2 memory cell is most convenient for performing the maximum (minimum) search since the stored bit and its complement are easily read out into the mismatch output channels. Furthermore, the latter are suitable paths for shifting this information to the sense location at the most significant end of the words. We recall that a stored bit is propagated into the mismatch 0 channel by energizing the I_0 interrogate conductor in conjunction with the general drive field, while the complement is introduced into the mismatch 1 channel by pulsing I_1 (refer to section 4.4).

The shifting operation described previously can be accomplished by any one of the several DTPL techniques developed for constructing shift register devices.

In particular, the DTPL implementation of the Broadbent type[5] shifting technique is useful for this purpose since no general drive fields are required. Unidirectional propagation of domains of reversed magnetization is obtained by successively energizing two sets of wide (approximately .100 inch) control conductors located behind the film plane with current pulses of alternating polarity. The fields produced by these conductors are oriented along the film easy axis and thus the word slice axis. During this sequence, the hold line which passes through all memory cells must be energized to prevent erasure by an erase-oriented shifting field.

Figure 47 schematically presents a portion of the memory configuration designed to implement the maximum (minimum) search operation. Shown in the figure are the sense line, control lines, and DTPL logic elements which are required to perform the inhibit function discussed at the beginning of this section. The stored information, or its complement, is shifted from top to bottom in the figure by the shift conductors. The length of a domain representing a 1 is indicated by L. A typical search operation is described next.

Referring to Figure 47, let us assume that a maximum search has begun, the contents of all cells have been written into the mismatch 0 channels, and the first shift cycle is in progress. Now assume that a 1 (domain) in word 1 and 0's in words 2 to M have been shifted across the sense line. When the readout signal occurs, control conductor I_R is energized and punch-through elements $2_1, 2_2 \ldots 2_M$ are enabled. This allows domain tips from the 1 generators to propagate towards gates $3_1, 3_2, \ldots 3_M$. In the case of word 1, the domain of length L in the readout channel will cause a tip to enter gate 4_1 via element 2_i and inhibit propagation to 3_1. Since no information is present in the readout channel of words 2 to M, no tip will enter gates $4_2 \ldots 4_m$. Gates $3_2 \ldots 3_M$ are switched and will remain as such due to the permanent hold line which prevents erasure only in the S channels. As a result, no information from the lower-order bit

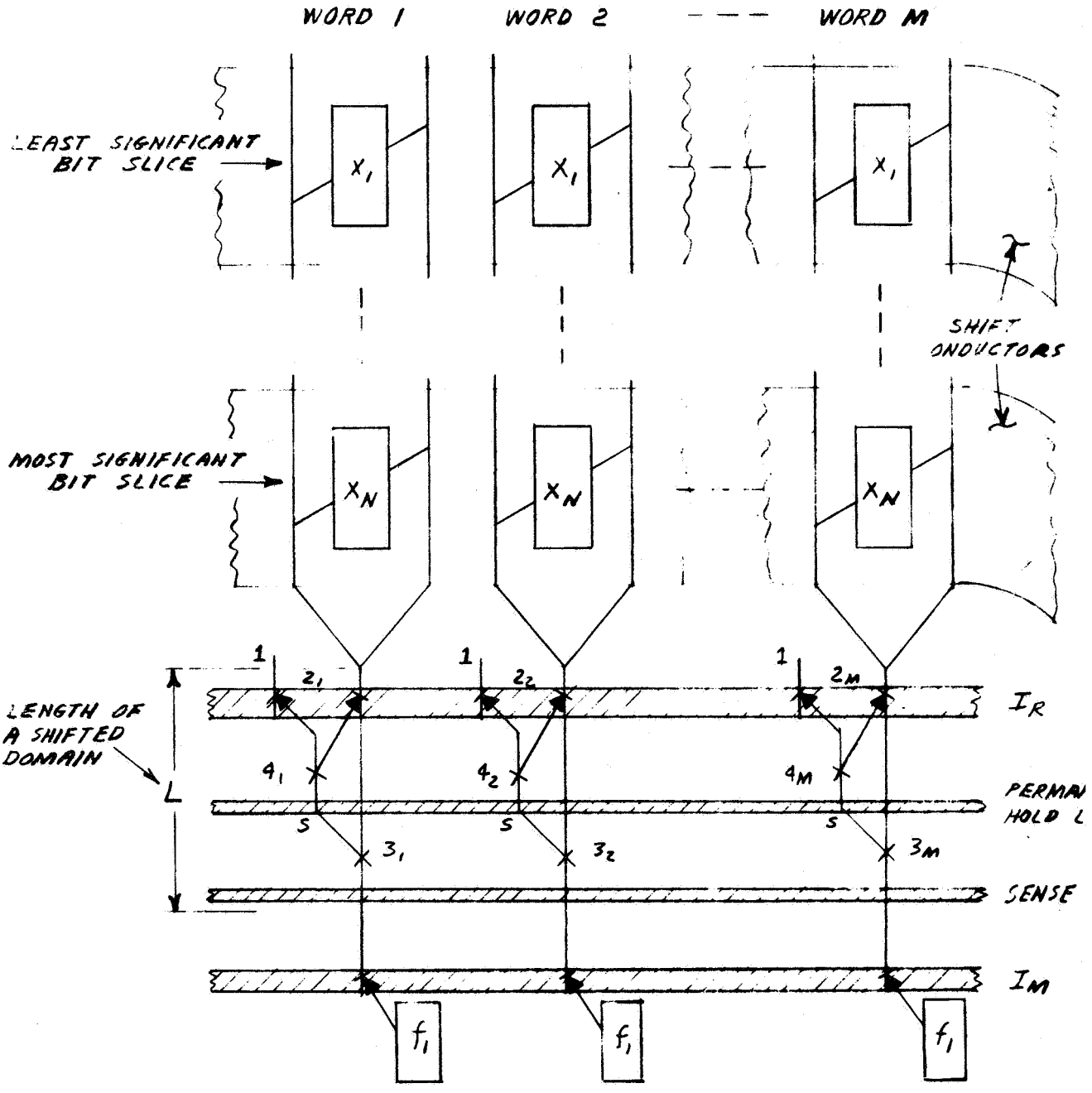


Figure 47 Memory array of type #2 cells and logic configuration pertinent to the maximum (minimum) search operation.

slices of words 2 to M will reach the sense as subsequent shifting operations take place.

Since the identity of the maximum (minimum) word or words cannot be determined until the least significant bit slice has been processed, and since this may contain all 0's, information representing the maximum (minimum) word or words is not conveniently obtained during the final shift sequence. The simplest solution to this problem is to insert a tag bit in each word following the least significant bit slice. When all processing is complete, one additional shift left is performed and the tag bit or bits in the active words (no domain in gates 3) propagate uninhibited past gates 3 to the flag bit memory cells f_1. At this time, line I_M is energized and the information is written into these storage cells. A general erase-hold completes the cycle.

The total time required for this search operation is approximately equal to one equality search cycle using the type #2 memory cells since the longest distance a tip must propagate is the same in both searches. Use of the shifting technique describes eliminates the normal erase-hold pulses common to the zig-zag and other shift register drive sequences.

The various techniques which can be employed to speed up previously-described search operations are suitable for the maximum (minimum) search. A problem exists, however, due to the dependency between words. Further study of this problem is planned.

5.2.4 Proximity Search

The proximity search is defined as the operation of finding the stored word which comes closest to matching a search word in terms of the number of matching bits.

Memory Array--Type #1 Cells. A modified type #1 memory cell with an "override mismatch" capability was described in section 4.3, "Improvements." An array of these cells can be used to implement a form of proximity search in which it is desired to find the word or words which differ from a search word in a particular bit position. The bit position, herein denoted as the proximity bit, is completely arbitrary and more than one can be selected during the search.

Let us consider the memory array depicted in Figure 48 composed of modified type #1 cells and associated override mismatch conductors I_p (refer to Figure 34b). The special proximity search operation is performed by doing an equality search on all bit slices in parallel and energizing the "inhibit match" control line. The latter causes a self-inhibit operation via punch-through elements 1 and gates 2 in all words satisfying the search. Those words containing one or more mismatches are characterized by a blocked tip in the word channel at the mismatch cell nearest the "nucleate test tips" control line. With the uniform drive field applied and the "inhibit-match" pulse terminated, the override-mismatch control conductor(s) corresponding to the proximity bit slice(s) being searched are then energized in conjunction with the interrogate lines which performed the initial equality search. In those words which differ from the search word only in the proximity bit position(s), the blocked tips will be punched through the mismatched cell(s) and an output tip obtained at the flag memory cell. On the other hand, words which contain one or more additional mismatches will produce no output. The operation is completed by writing the output tips into the flag cells f_1 and performing a general erase and hold on the entire array.

In this manner, only the word(s) containing the mismatch(es) in the specified bit position(s) can respond to the search. The operation requires approximately two equality search times, one to propagate match test tips through the entire word channel, and one to override the mismatches and produce output tips.

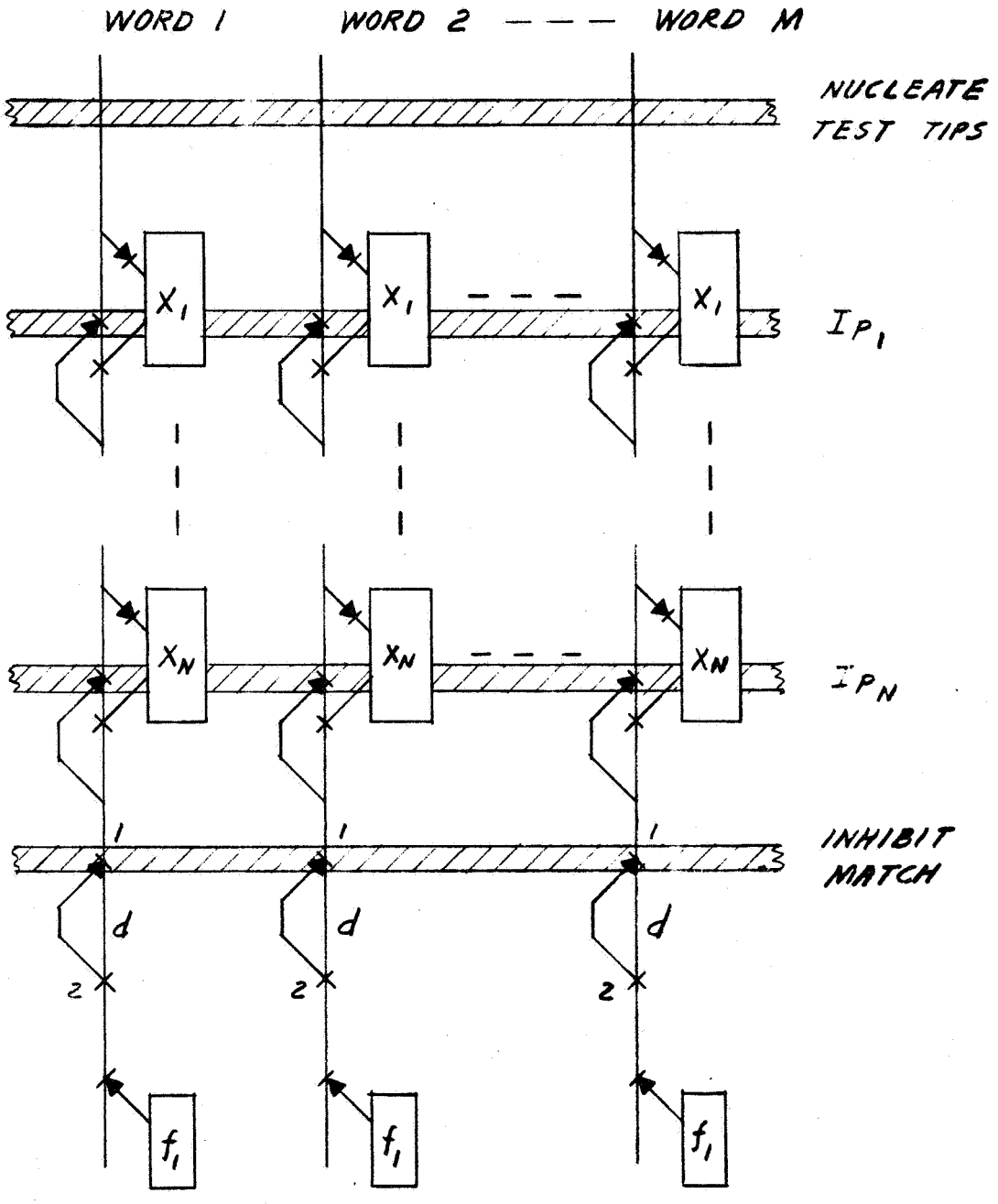


Figure 48 Memory array of modified type #1 cells and logic configuration pertinent to the proximity search operation.

A true proximity search according to the definition given previously would be more complex requiring a sequential search of each bit slice, a count of the number of mismatches and a minimum search on the contents of the counter. Techniques for performing this search in a simpler manner will be investigated.

Memory Array--Type #2 Cells. The specialized proximity search described in conjunction with the type #1 cell cannot be performed in an array of type #2 cells since the bit slice containing a mismatch cannot be identified during an equality search. Techniques for performing the standard proximity search are equally complex as in the case of the type #1 cell. Further study of this problem is planned.

5.2.5 Intersection of Searches

The intersection of two or more sets of words, each of which satisfies a basic search, is equivalent to a logical AND of the basic searches.

Memory Array--Type #1 Cells. To perform the intersection of searches in this type of array, the results of the first search are used as the input set to the next search. This mode of operation is possible due to the fact that test tips are normally required in the mechanization of a search. The configuration of memory cells and conductors to implement this function is similar to the basic array shown in Figure 42, except for the addition of hold conductors at the input and output ends of the words as depicted in Figure 49. These are required for shifting the results of a search back to the input for the subsequent search.

In performing the intersection of searches, the first search utilizes test tips written into all word channels by the appropriate nucleate conductor. At the end of the cycle, the output hold line is energized during the general erase-hold sequence, and the results of the search (domains of reverse magnetization) are

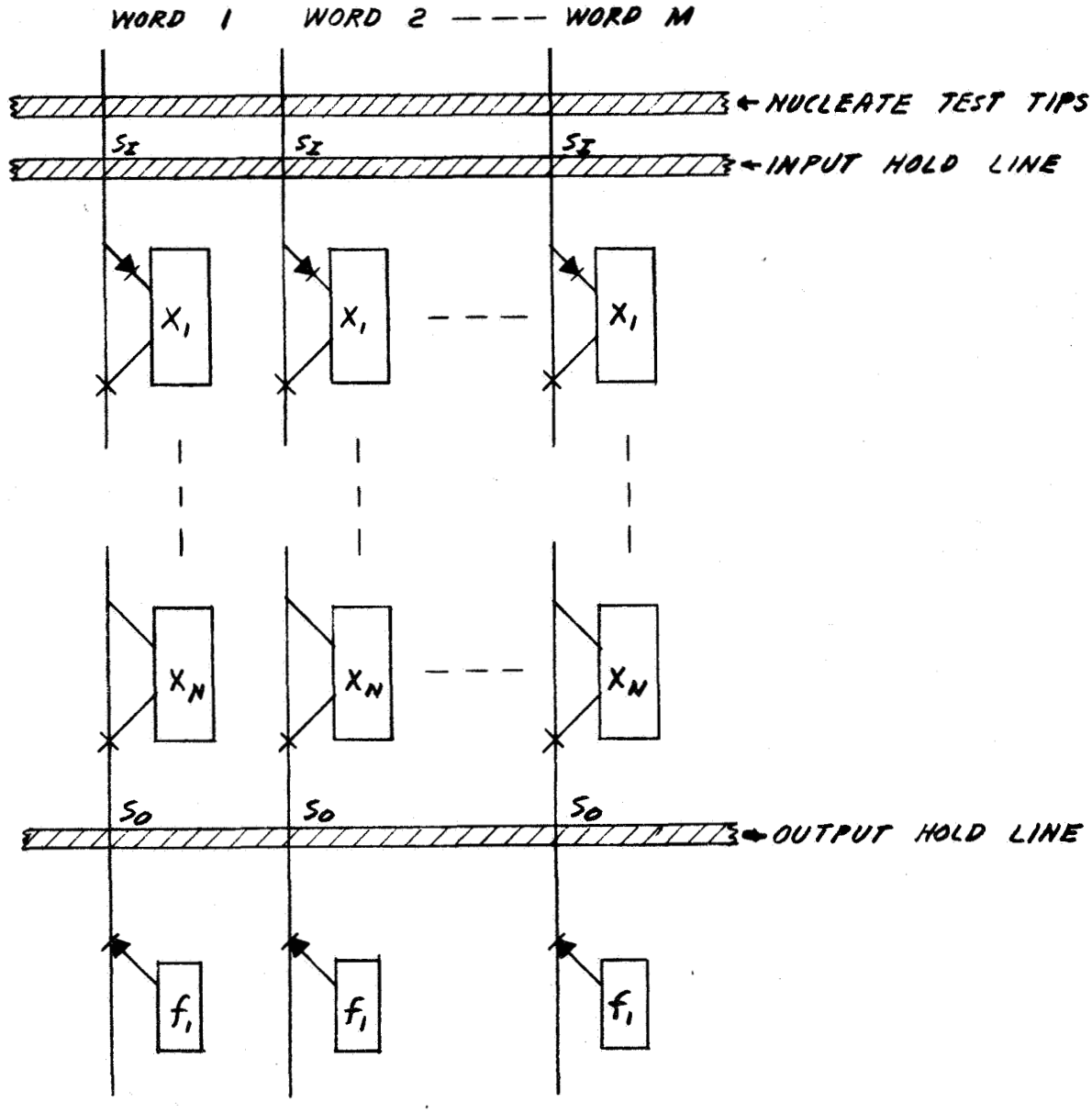


Figure 49 Memory array of type #1 cells and logic configuration pertinent to the intersection of searches operation.

stored at locations S_0 in the word channels. The general drive field is applied and the information in question propagates toward the input end. At this time, the input hold line is energized and the general erase-hold repeated. Domains now stored at S_I will function as the input set for the next search. These operations continue until the final search has been completed. The results remaining represent the intersection of the basic searches which are then written into the flag bit memory cells in the usual manner.

The total time required to perform the intersection of searches equals the sum of the basic search times plus the product of the number of searches and an equality search time.

Memory Array--Type #2 Cells. The previously-described technique for performing the intersection of searches is not suited to an array of type #2 memory cells because test tips are not required in search operations. A straightforward ANDing of the results of the basic searches would satisfy the intersection requirement, but this approach is cumbersome.

The most suitable scheme for mechanizing this search is to logically OR the mismatches from the basic searches in a "collect mismatch" storage cell on a per-word basis and use this result to inhibit a test tip propagating to a flag memory cell. In those words which satisfy all of the searches, the special storage cell remains erased since no mismatches are obtained. The test tip then propagates uninhibited to the flag cell and is stored therein for a subsequent on-match operation. In the case of the words producing one or more mismatches during the basic searches, the collect mismatch storage cell is switched and the test tip inhibited.

Figure 50 schematically depicts the memory array pertinent to the implementation of the intersection of searches. It is similar to the basic configureation shown in Figure 44, except for the additional hold line H which provides the

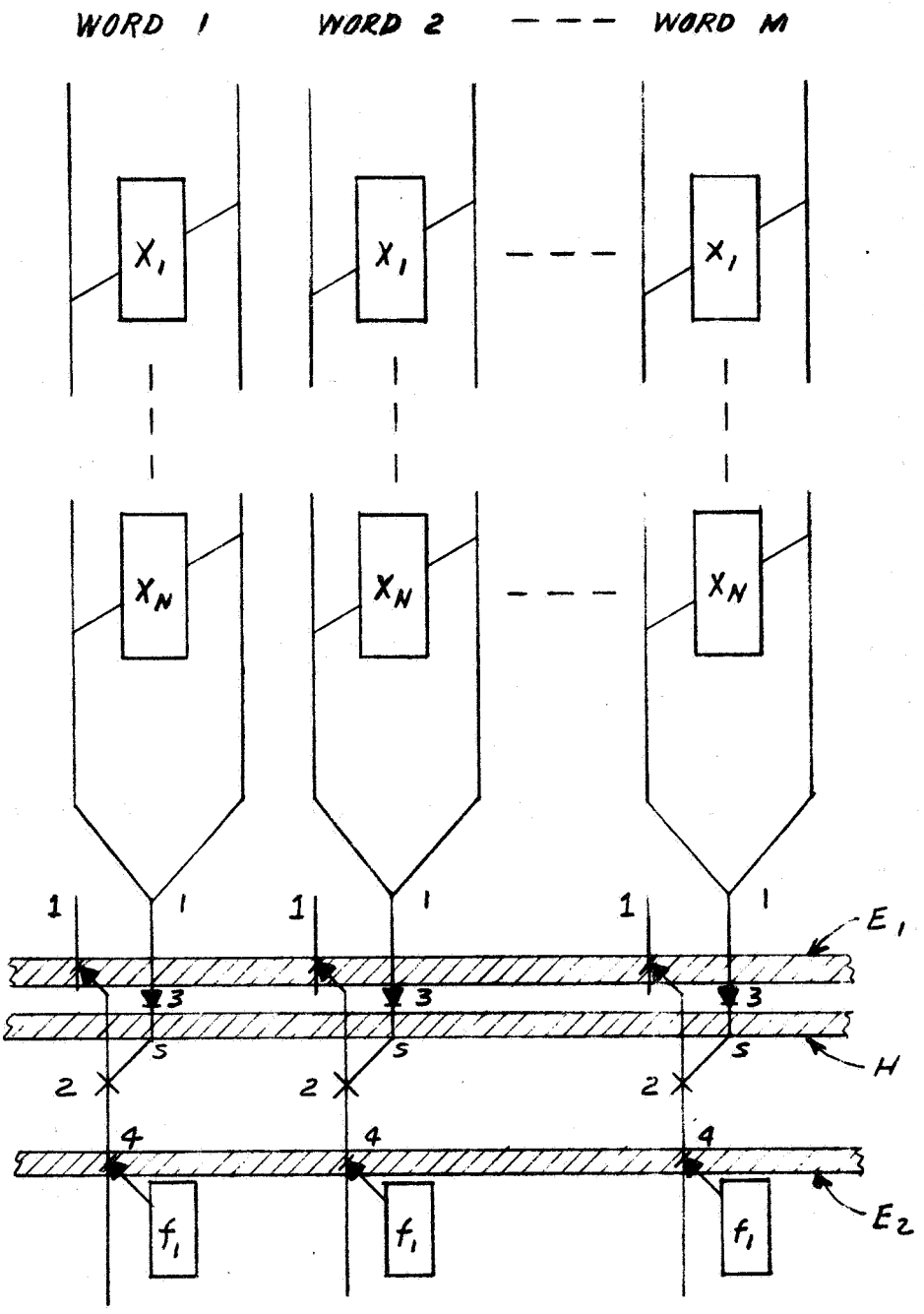


Figure 50 Memory array of type #2 cells and logic configuration pertinent to the intersection of searches operation.

channel leading to inhibit gates 2 with a storage capability. Diodes 3 prevent information stored at S from exiting this "collect mismatch" storage cell. Test tips are produced by the 1 generator and propagate to the flag memory cell via punch-through element 4 when line E_1 is energized.

If, for example, it were required to perform the intersection of several equality searches, following each test-for-match operation, the general erase-hold cycle would include a hold on line H to store the mismatches. When the searches are completed, E_1 is energized and the test tips propagated to the flag cells. A flag bit is then written in those words containing unswitched inhibit gates 2.

While the array in Figure 50 was designed primarily for equality searches, the intersection of different searches (inequality, maximum (minimum), etc.) can be performed quite readily. In these cases, it becomes necessary to invert the results (matches) from the searches in order to obtain the desired inputs (mismatches) to inhibit gates 2. Although this double-inversion operation appears redundant, it does reduce the number of logic operations required if the equality search is performed most frequently.

The memory time consumed in an intersection-of-searches operation performed in an array of type #2 cells is approximately equal to the sum of the individual search times. We recall that with the type #1 cell, additional time was required to shift the match tips between output and input hold locations.

5.2.6 Union of Searches

The union of searches is defined as the set of words satisfying one or more of a number of searches. This is obtained by logically ORing the results of the basic searches.

Memory Array--Type #1 Cells, Memory Array--Type #2 Cells. The union of searches is performed in the same manner in both of the memory arrays under

consideration. The operation consists of writing the results of each basic search into the same flag bit memory cell on a per-word basis and storing these results during the subsequent searches. In those searches where the match outputs are not immediately available at the flag cell, it then becomes necessary to temporarily store this information before shifting it to the flag cell. This is easily accomplished by means of a hold line located at the match output channel.

In general, the contents of all flag cells following a sequence of consecutive searches (no on-match operations) will always represent the union of these searches. The time required for this operation is approximately equal to the sum of the basic search times. It is assumed that the transfer of a match output described above constitutes a small portion of any search cycle.

5.3 Processing Operations

5.3.1 Field Addition $(X_1 + Y_1, X_2 + Y_2, \ldots, X_n + Y_n)$

This is the processing operation in which two quantities X and Y stored in the same word of the memory are added together and the result written back to replace either X or Y or to be stored in a third field. The most frequently-used type of field add is one in which the sum $Z = X + Y$ is stored in place of the quantity Y. It allows the use of a special algorithm[6] which reduces the number of search operations required per bit of addition as compared to the field add in which the sum Z is stored in a third field. That algorithm is intended for use in associative memories with an all-parallel equality search capability--a capability characteristic of DTPL memory-logic arrays.

In the discussion which follows, techniques for performing both types of field addition in the two basic memory arrays are described. The use of a DTPL serial adder in each word of memory for mechanizing these arithmetic operations will not be considered at this time due to the present size of the adder network. Improvements in the design of the latter are planned since their incorporation into a memory array would reduce processing time.

Memory Array--Type #1 Cells. To perform the field addition X + Y = Z→(third field), we consider the Boolean equations for the sum and carry bits given by:

$$Z_i = \bar{X}_i \bar{Y}_i C_i + \bar{X}_i Y_i \bar{C}_i + X_i \bar{Y}_i \bar{C}_i + X_i Y_i C_i \tag{16}$$

$$C_{i+1} = C_i X_i + C_i Y_i + X_i Y_i \tag{17}$$

In an array of type #1 memory cells, each of the above product terms $\bar{X}_i \bar{Y}_i C_i$, etc., can be generated by successive equality searches since the test-for-match operation is, in effect, an ANDing of the searched bits. For example, to generate $\bar{X}_i \bar{Y}_i C_i$, a test for match is performed on the bit slices corresponding to X_i, Y_i and C_i against the search word 001. If a match results, the test tip is then written into a Z_i memory cell contained in the third field. The operation continues in this manner with the remaining three sums being generated using search words 010, 100 and 111. Since the results of each search are effectively ORed in the Z_i cell, information contained in the latter at the end of the four searches is the desired sum bit.

The operation X + Y = Z →(Y) is carried out in the same manner, and uses a cell designated Z_t to temporarily store Z_i. When the addition is complete, Z_i is written into Y_i and the Z_t cell is erased.

The generation of C_{i+1} requires three equality searches. It is apparent that the contents of the C_i memory cell cannot be updated to C_{i+1} until at least the first two terms in equation (17) have been generated. The most convenient procedure is to logically OR the result of each search in a temporary storage cell. A general erase-hold is then performed without energizing the C_i hold line and C_i is erased. This is followed by a write operation and C_{i+1} is written into C_i. The cycle is completed with a general erase-hold in which the C_{i+1} temporary storage hold line is not energized. This erases the C_{i+1} cell in preparation for the next field addition.

In general, the field addition operation is performed in each word of memory in parallel. The equality searches required take place in the usual manner with test tips being introduced into all word channels simultaneously (refer to section 5.2.1) by means of a nucleate conductor. A selective field addition in one or more words is also possible. In this case, the aforementioned test tips are produced by the word selection network.

The configuration of type #1 memory cells and control conductors pertinent to the X + Y = Z→(third field, Y) processing operation is depicted in Figure 51. Cells designated Z_i are also type #1 with full memory-logic capability. Bits C_i, Z_t and C_{i+1} are modified storage structures. The former possesses a test-for-match capability, while the latter two can produce a readout into the word channel when I_{Z_t} or I_C is energized. Hold lines H_{Z_i}, H_{Z_t}, H_{C_i}, and $H_{C_{i+1}}$ function independently of the general hold line to control erasure on the Z_i, Z_t, C_i and C_{i+1} bit slices, respectively.

The step-by-step procedure for this field addition is outlined below. It is seen that seven equality searches, one or two writes and four additional general erase-holds are required. Steps 10 and 12 can be combined with 9 and 11 which normally end with a general erase-hold. Thus, approximately eight equality search times are required for this operation.

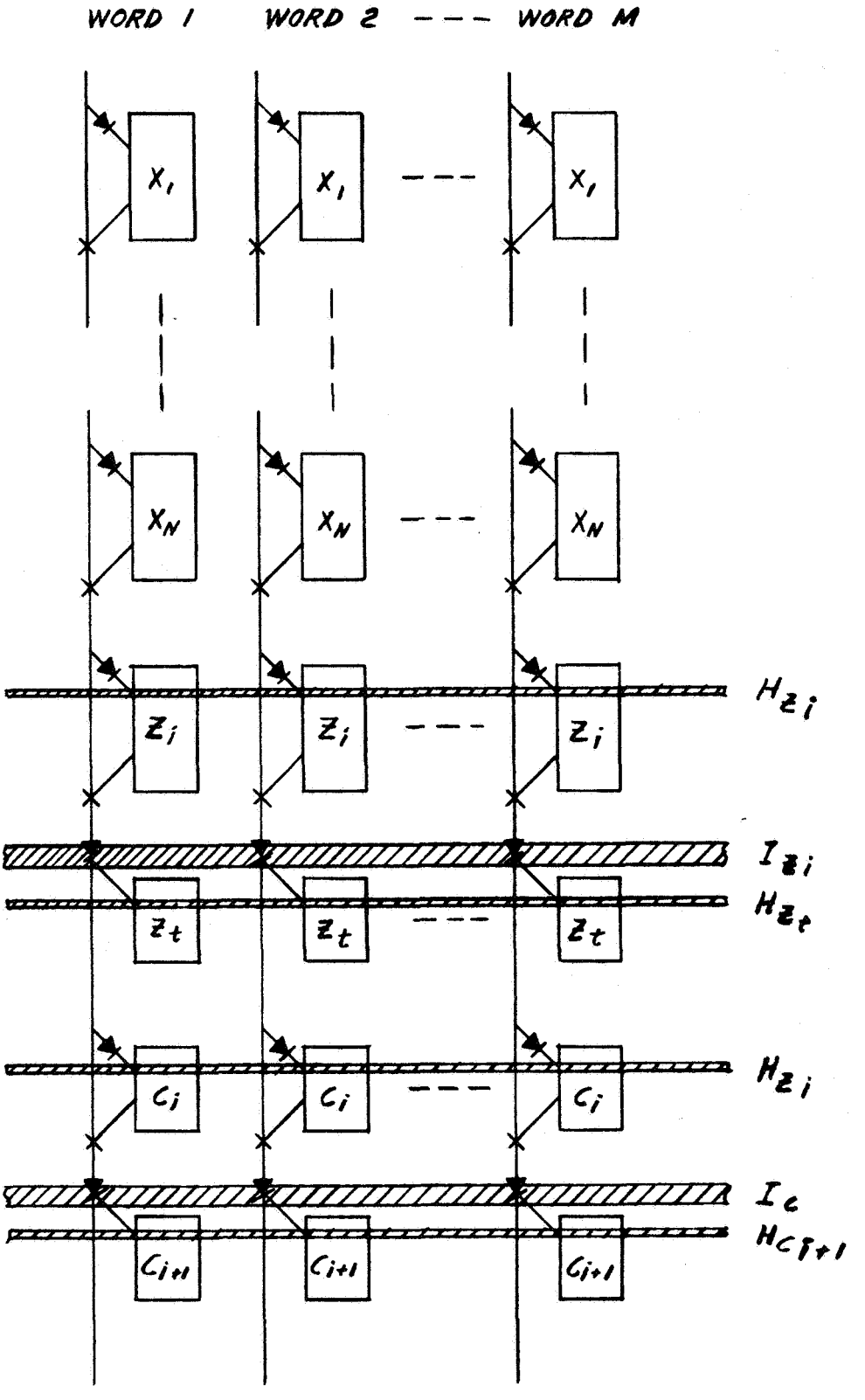


Figure 51 Memory array of type #1 cells and additional storage cells pertinent to the field addition X + Y = Z (third field, Y) processing operation.

Procedure for Field Addition

$X + Y = Z \rightarrow$ (Third Field, Y_t)

1. Erase all Z_i memory cells (required prior to first cycle)
2. Erase C_i bit slice (required prior to first cycle)

Start add; second and subsequent cycles

3. Equality search $X_iY_iC_i$ against 001, write Z_i
4. Equality search $X_iY_iC_i$ against 010, write Z_i
5. Equality search $X_iY_iC_i$ against 100, write Z_i
6. Equality search $X_iY_iC_i$ against 111, write Z_i
7. Equality search C_iX_i against 11, write C_{i+1}
8. Equality search C_iY_i against 11, write C_{i+1}
9. Equality search X_iY_i against 11, write C_{i+1}
10. Erase C_i bit slice
11. Write C_{i+1} bits into C_i cells
12. Erase C_{i+1} bit slice

To replace Y_i by Z_i, change Z_i to Z_t in above procedure and add

13. Write contents of Z_t (Z_i) into Y_i
14. Erase Z_t bit slice

The $X + Y = Z \rightarrow (Y)$ type of field addition can also be accomplished using a special algorithm as mentioned previously. To understand this operation, we consider the following tables for initial and final states of the X_i, Y_i and C_i storage cells where Z_i is stored in Y_i and C_{i+1} in C_i.

	Initial State			Final State		
	X_i	Y_i	C_i	X_i	Z_i	C_{i+1}
1	0	0	0	0	0	0
2	0	0	1	0	1	0
3	0	1	0	0	1	0
4	0	1	1	0	0	1
5	1	0	0	1	1	0
6	1	0	1	1	0	1
7	1	1	0	1	0	1
8	1	1	1	1	1	1

It is seen that initial states 1, 3, 6 and 8 generate identical final states. Thus, only 2, 4, 5 and 7 must be detected in order to modify the contents of the Y_i and C_i memory cells. Furthermore, it is noted that initial state 4 generates a final state which is the same as initial state 2, and initial state 5 generates a final state which is the same as initial state 7. To prevent errors, then, initial state 2 must be detected before 4, and 7 before 5.

To perform this operation, four equality searches are carried out on X_i, Y_i and C_i against search words 001, 011, 110 and 100, in that order. In those words satisfying a search, the match test tip is used to perform a local erase in the Y_i and C_i memory cells in preparation for the subsequent writing of Z_i and C_{i+1}. The information to be written is generated within the memory array using the stored match test tip according to the initial and final state tables, the pertinent portions of which are presented below.

X_i	Y_i	C_i
0	0	1
0	1	1
1	1	0
1	0	0

Z_i	C_{i+1}
1	0
0	1
0	1
1	0

It is noted that Z_i is the complement of C_{i+1} and C_{i+1} is equivalent to Y_i. Thus, if the search bit for the Y_i memory cell is also used to control writing into the C_i storage cell, a test tip is written into C_i, becoming C_{i+1} when a match occurs, $Y_i = 1$ and I_1 is energized. If a match occurs but $Y_i = 0$, no write occurs and C_i contains a 0. The correct Z_i is obtained by reading out C_{i+1} into a special output channel and writing its complement Z_i into the Y_i storage cell.

Figure 52 illustrates the memory array for this type of field addition. It consists of the basic configuration of type #1 storage cells, a carry storage cell C_i per word, a temporary hold location S_t and control lines for storing the results of an equality search and inverting gates 1 for writing Z_i. The C_i cells can perform write, local erase and readout into the C_i output channel. They are accessed by special control conductor I_{CY_i} which is energized during a "write C_{i+1}" operation if the Y_i search bit in the preceeding equality search was a 1. The I_{CR} control conductor is used to read out the carry bit C_{i+1} into the output channel leading to gates 1.

To write Z_i, the contents of the carry bit cell C_{i+1} are read out into the output channel and, by means of gate 1, inhibit the match tip, initially stored at S_t, from propagating to Z_i. If $C_{i+1} = 0$, no inhibit takes place and $Z_i = 1$. If $C_{i+1} = 0$ when no match tip is present, no Z_i is written and the Y_i cell remains unaltered for the next equality search.

The step-by-step procedure for this field addition is presented below. While only four equality searches are required, each must be followed with a local

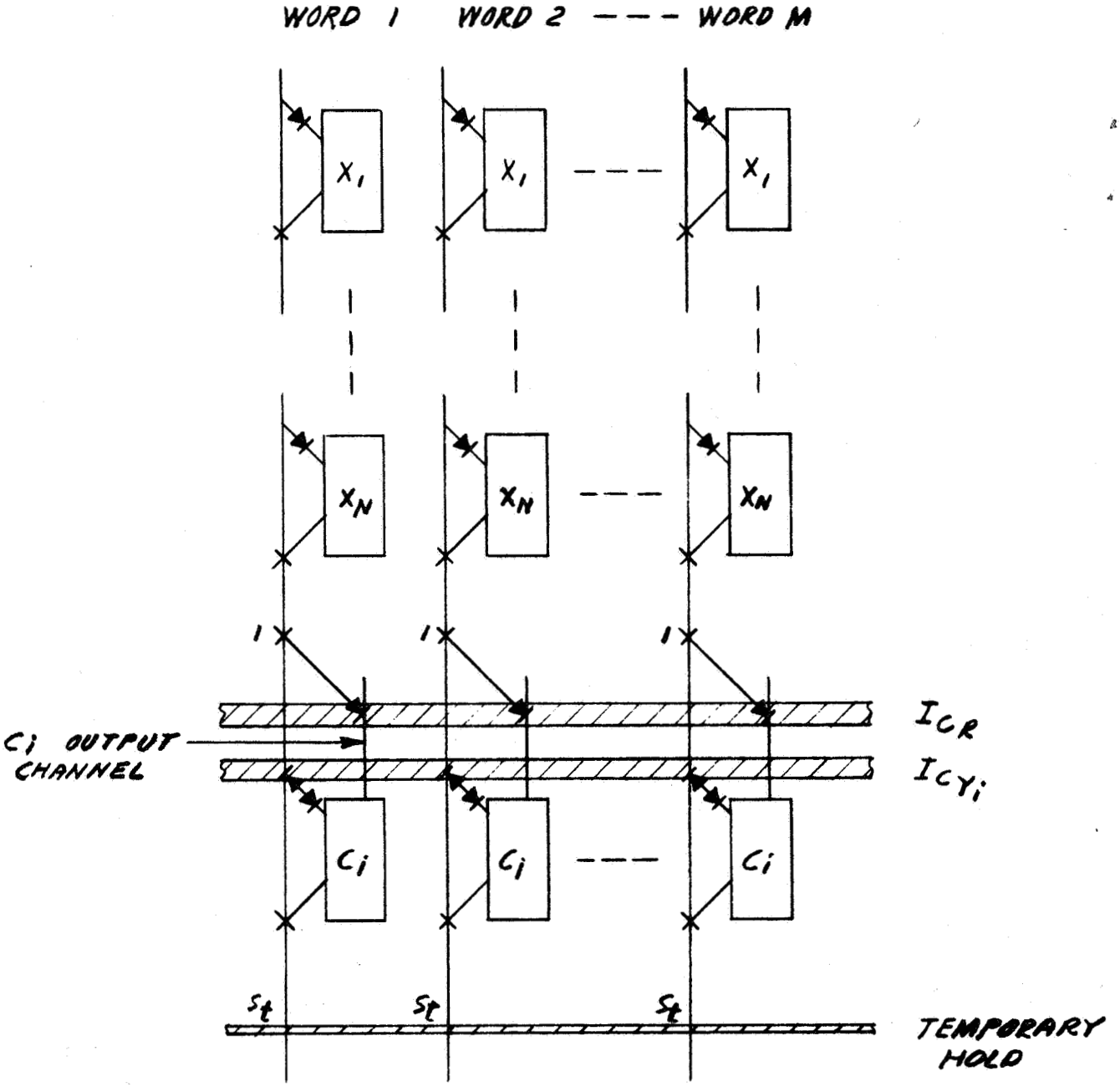


Figure 52 Memory array of type #1 cells and additional storage cells pertinent to the field addition X + Y = Z→(Y) processing operation.

erase on Y_i and C_i if a match results and two write sequences for C_{i+1} and Z_i. Thus, effectively sixteen equality search times are consumed in the arithmetic operation. Further investigation of this approach is planned to simplify and speed up the local erase and writing operations in order to realize the reduction in processing time possible when only four equality searches are required.

Special Procedure for Field Addition

$X + Y = Z \rightarrow (Y)$ ($C_i = 0$ prior to first cycle)

1. Equality search $X_i Y_i C_i$ against 001
2. Local erase Y_i and C_i on match
3. Write C_{i+1} into C_i storage cell on match
4. Write $Z_i = \overline{C_{i+1}}$ on match

5-8. Repeat 1-4 using search word 011

9-12. Repeat 1-4 using search word 110

13-16. Repeat 1-4 using search word 100

Memory Array--Type #2 Cells. Let us first consider the addition $X + Y = Z \rightarrow$ (third field). The Boolean expression for the sum and carry bits given by equations (16) and (17) can be rewritten in the form:

$$Z_i = \overline{(X_i + Y_i + \bar{C}_i)} + \overline{(X_i + \bar{Y}_i + C_i)} + \overline{(\bar{X}_i + Y_i + C_i)} + \overline{(\bar{X}_i + \bar{Y}_i + \bar{C}_i)} \quad (18)$$

$$C_{i+1} = \overline{(\bar{C}_i + \bar{X}_i)} + \overline{(\bar{C}_i + \bar{Y}_i)} + \overline{(\bar{X}_i + \bar{Y}_i)} \quad (19)$$

Each of the sum terms $\overline{(X_i + Y_i + \bar{C}_i)}$, etc., can be generated by successive equality searches since the test-for-match operation is, in effect, an ORing of the searched bits. Thus, in an array of type #2 cells, the term $\overline{(X_i + Y_i + \bar{C}_i)}$, for instance, is generated by performing a test for match on the bit slices corresponding to X_i, Y_i and C_i against the search word 001. A match yields no output, but the inversion operation which is part of the equality search (refer to section 5.2.1) produces the domain tip representing $\overline{(X_i + Y_i + \bar{C}_i)}$. This information is then written into the Z_i memory cell.

The complete field add operation $X + Y = Z \rightarrow$ (third field) is performed using the procedure developed for a memory array of type #1 cells described previously. Figure 53 depicts the type #2 cells and control conductors for implementing the required equality searches (seven) and storing the Z_i, Z_t, C_i and C_{i+1} bits.

The $X + Y = Z \rightarrow (Y)$ processing operation is equivalent to an $X + Y = Z \rightarrow$ (third field) add with the addition of a write cycle to transfer the sum bit stored in the temporary storage cell Z_t to the appropriate Y_i cell.

The special procedure described earlier for accomplishing $X + Y = Z \rightarrow (Y)$ in an array of type #1 cells (see Figure 52) can also be employed in this case. It is recalled that sixteen equality search times are required although only four equality searches are performed.

5.3.2 Operand Addition ($X_1 + S$, $X_2 + S$, ..., $X_n + S$)

The operation in which a quantity S located in the operand register is added to a set of stored quantities X where each X is contained in a different word of the memory is known as operand addition. As in the case of field addition, the sum $X + S = Z$ may either be written in place of X or be stored in another field of that word. From the standpoint of DTPL, $X + S = Z \rightarrow$ (second field) is the more general operation and is, therefore, the subject of the discussion which follows.

Memory Array--Type #1 Cells, Memory Array--Type #2 Cells. The algorithm developed for performing an operand addition is applicable to both types of DTPL memory arrays under consideration. In order to understand this operation, we refer to the truth table presented below.

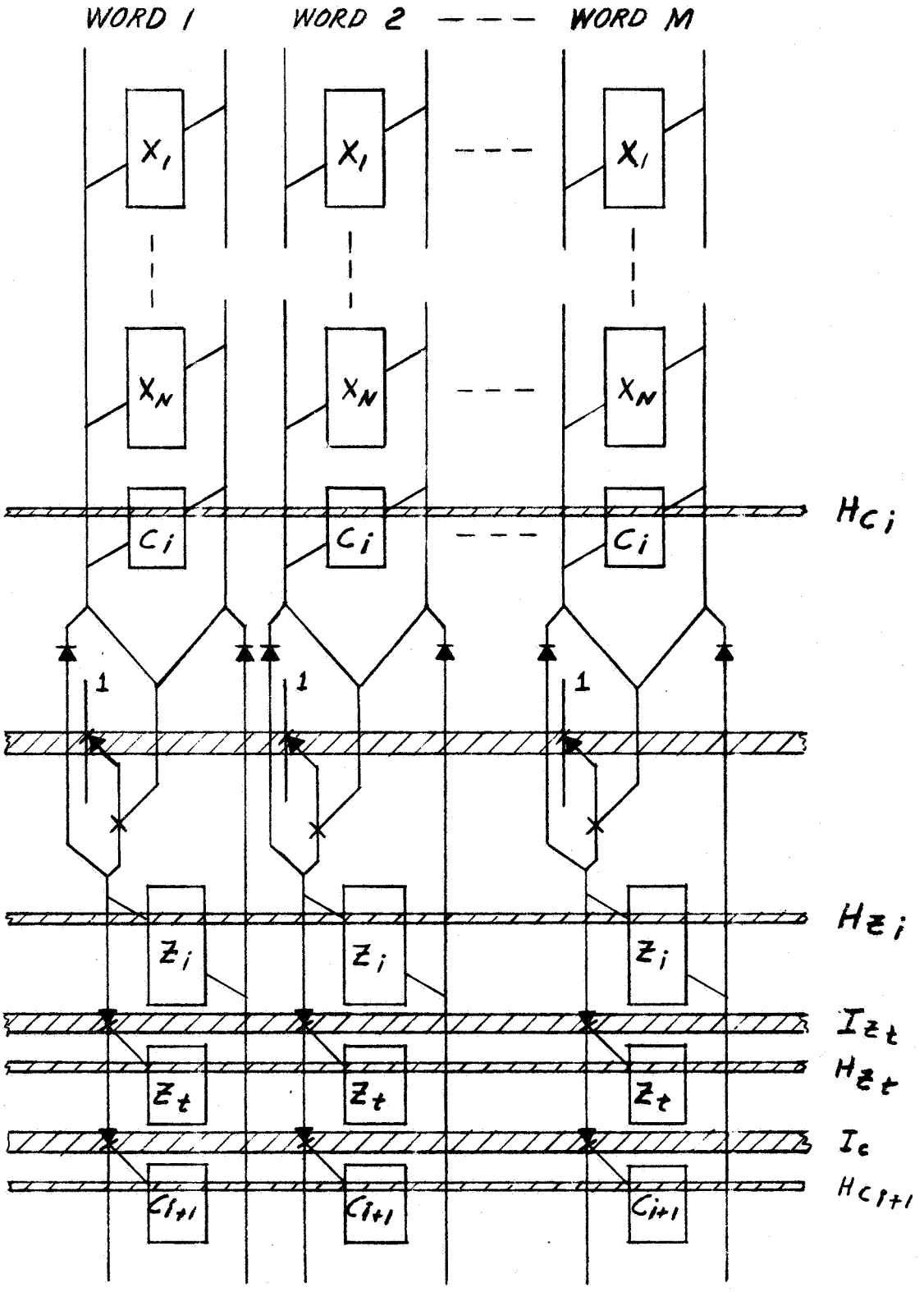


Figure 53 Memory array of type #2 cells and additional storage cells pertinent to the field addition X + Y = Z (third field, Y) processing operation.

X_i	S_i	C_i	Z_i	C_{i+1}
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Examining first the column of values for the sum bit, it is seen that Z_i depends on whether C_i and S_i match or mismatch and X is a 0 or a 1. More specifically, if $C_i \neq S_i$, $Z_i = 1$ when $X_i = 0$ and $Z_i = 0$ when $X_i = 1$. On the other hand, if $C_i = S_i$, $Z_i = 0$ when $X_i = 0$ and $Z_i = 1$ when $X_i = 1$. The value of Z_i can thus be obtained by doing an equality search on C_i against S_i and logically combining this result with a second bit of information representing the contents of the X_i cell. It will be shown that this second bit of information is equivalent to $\overline{X}_i$.

The DTPL logic structure required for the Z_i operation is presented in Figure 54. It consists of the following: (1) a temporary storage cell S C to store a match from the equality search on C_i against S_i, (2) a cell Z_i to store the sum bit, (3) a blocking conductor to synchronize tip propagation to gates 1, 2 and thus Z_i and (4) the appropriate gates 1, 2 and delay channels d to perform the logic. One such configuration would be located at the match output channel of each word of memory in either of the basic arrays.

To perform the addition, two equality searches are carried out--the first on C_i against S_i, the second on X_i against 0. If, for example, $X_i = 0$, $S_i = 0$ and $C_i = 0$, the equality search on C_i would result in a match and a bit stored in cell S C (SC initially erased). With the blocking conductor energized, the search on X_i takes place and the match output tip propagates to and comes to rest at location 4. Next, the blocking field is terminated and the SC cell outputs at 5 and **6** and

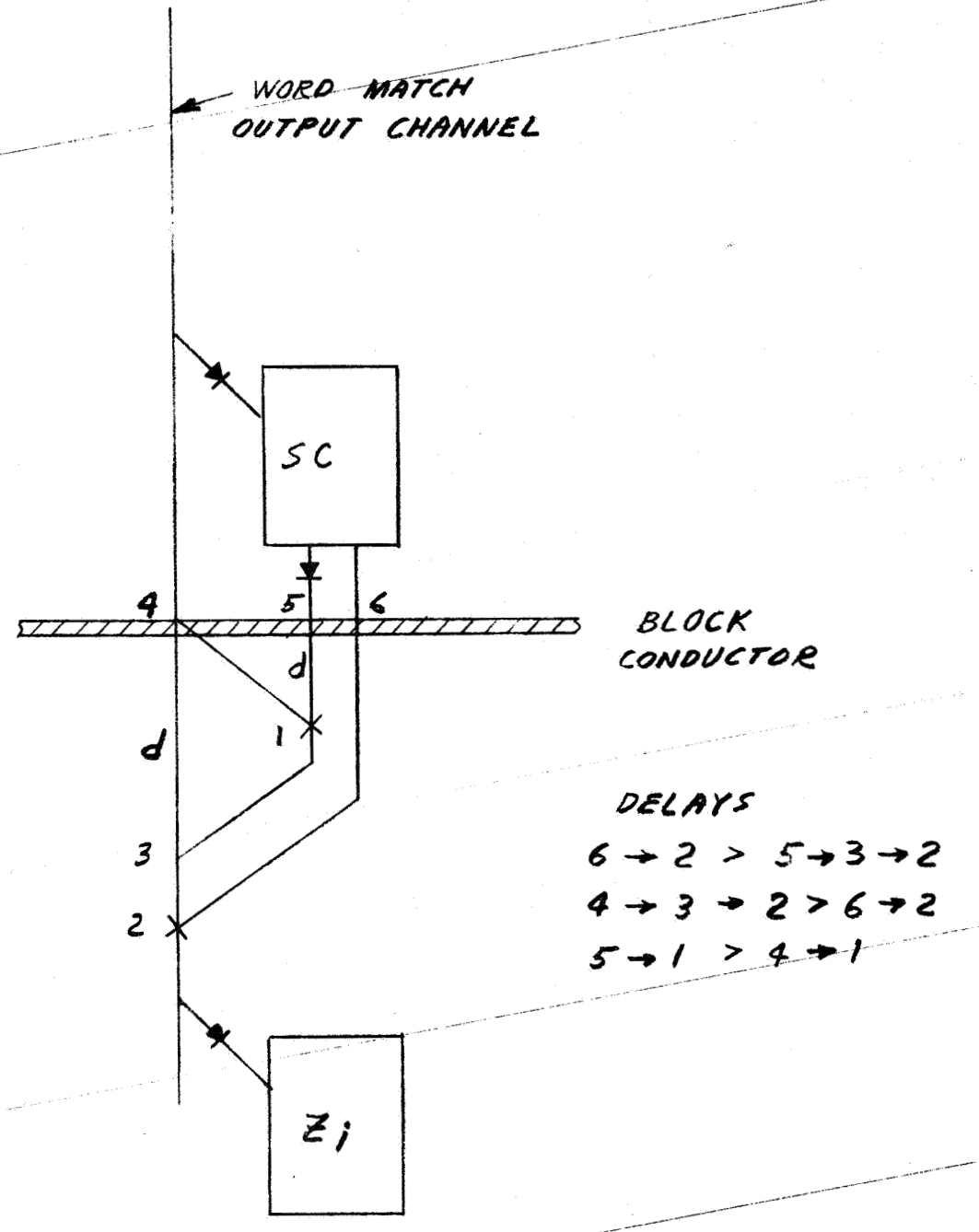


Figure 54 Storage cell and logic configuration used in operand addition processing operation.

the tip at 4 propagate in the direction of Z_i. As a result of the special delay channels (see Figure 54 for delays), inhibits occur at gates 1 and 2 and no information is written into Z_i (Z_i initially erased). Suppose, however, $X_i = 0$, $S_i = 0$ but $C_i = 1$, then the first search on C_i would produce a mismatch and cell SC would remain erased, i.e., SC = 0. The subsequent search on X_i would still provide a match tip at 4, which, when the blocking field terminates, propagates uninhibited to Z_i. The remaining input combinations for $X_i = 0$ are processed in the same manner as described above.

When $X_i = 1$, a given combination of S_i and C_i will produce a sum bit which is the complement of Z_i obtained for $X_i = 0$. Suppose $X_i = 1$, $S_i = 0$ and $C_i = 0$, the first search, C_i against S_i, results in a bit being stored in SC. Since the next search on X_i is against a 0, no output tip reaches location 4. The tips at 5 and 6 then propagate to OR gate 3 and inhibit gate 2 when the blocking field terminates, but no inhibit occurs since the delay from 6→2 is greater than from 5→3. A bit is then written into Z_i. If, however, $X_i = 1$, $S_i = 0$, but $C_i = 1$, no match occurs for either search and Z_i remains a 0.

The time required to generate a sum bit is thus approximately two equality search times. It is assumed that the time involved in performing the above logic operations is negligible in comparison with an equality search.

Referring next to the columns in the truth table corresponding to the carry bits C_i and C_{i+1}, it is noted that $C_i = C_{i+1}$ for all input combinations except 2 and 7. Furthermore, we note that when $X_i = S_i$, $C_{i+1} = X_i$, and when $X_i \neq S_i$, $C_{i+1} = C_i$. To generate C_{i+1}, then, an equality search is done on X_i against S_i as the first part of an intersection of searches operation. A local erase on C_i follows in those words satisfying the search. In the words where $X_iS_i = 01$ or 10, C_i is unchanged. Next, a second equality search is performed on X_i against 1 and the intersection of searches is completed. In the words satisfying both searches, i.e., words in which $X_iS_i = 11$, a 1 is written into the C_i cell becoming C_{i+1} (input combinations 7 and 8).

In summary, words containing $X_i S_i = 10$ or 01 are unchanged during the two search cycles. Where $X_i = S_i$, C_i is set to 0 by a local erase. The second search and then the intersection of searches operation find the words where $X_i = S_i = 1$ and a 1 is written into C_i. The time required to generate the carry bit is equal to an intersection of searches operation for two equality searches plus a local erase and write cycle. These depend upon the type of memory array utilized.

The procedure for obtaining Z_i and C_{i+1} is outlined below for the two basic memory arrays. An array of type #1 cells requires five equality search times as compared to four equality search times for an array of type #2 cells.

Procedure for Operand Addition

$X + S = Z \rightarrow$ (second field)

1. Equality search C_i against S_i, write SC
2. Equality search X_i against 0, write Z_i
3. Intersection of searches to obtain C_{i+1}
   a. Equality search X_i against S_i
   b. Local erase C_i on match
   c. Equality search X_i against 1
4. Write C_i in words satisfying 3

5.3.3 Summation $(X_1 + X_2 + \ldots + X_n)$

This operation produces the summation of a set of quantities X stored in separate words of memory. The results would either be written into one of the words or stored in an external register.

The mechanization of this summation is somewhat complex in comparison to the previously-described search and processing operations. Briefly, what is required is that the quantity X_i be read out and placed in the operand register. Using the word selection network, the word containing X_2 is selected for an operand addition and the latter performed between X_2 and $S(X_1)$. The result Z_{12}

is written back into the operand register and C_{12} stored in the word containing X_3. The operand addition is repeated between X_3 and $S(Z_{12})$ producing Z_{123} and C_{123}. This continues until all X's have been processed.

Memory Array--Type #1 Cells. A selected operand addition is easily accomplished in an array of type #1 cells since a test tip is utilized in the equality searches. This test tip, instead of being introduced into all words (a normal operand addition $(X_1 + S, X_2 + S, \ldots, X_n + S)$ is performed simultaneously in all words) would be produced by the word selection network. Thus, only the selected word would have its contents modified.

Memory Array--Type #2 Cells. While no test tips are utilized for search operations in this case, a word could be selected for operand addition by inhibiting the writing of the sum and carry bits Z_i and C_{i+1} in all words except the one to be modified.

One would also consider performing the summation by a series of field additions. As such, the quantity X_1 would be written into a second field of X_2 denoted as Y_2 and the field add $X_2 + Y_2 (X_1) = Z_2$ carried out. The sum Z_2 and carry C_3 would then be written into a second field of X_3 and the sequence repeated.

5.3.4 Counting $(X_1 + 1, X_2 + 1, \ldots, X_n + 1)$

In this operation, a set of quantities X stored in separate words of the memory are simultaneously incremented.

Memory Array--Type #1 Cells, Memory Array--Type #2 Cells. One method of performing this form of addition is to place a 1 in the least significant bit position of the operand register (0's in all other locations) and proceed with an operand addition in the usual manner.

A second technique uses a memory cell in each word to store the carry bit C_i. C_i is set to 1 at the start of the operation in those words to be incremented. An equality search is then performed on X_iC_i against 11 followed by an on-match local erase in the X_i bit slice. In words satisfying this search $X_i \rightarrow 0$. Another equality search is then done on X_iC_i against 01. An on-match local erase of C_i and simultaneous write in X_i occur next with $X_i \rightarrow 1$ and $C_{i+1} \rightarrow 0$ in the matching words. The operation continues until all bits of X have been processed. Approximately four equality search times are required in each of the basic arrays.

5.3.5 Shifting

A selected set of quantities located in the same field of different words in the memory are simultaneously shifted in one or two dimensions in this processing operation.

Memory Array--Type #1 Cells. Since the basic type #1 storage cell does not possess a word channel readout capability, no shifting can be performed in this array.

Memory Array--Type #2 Cells. The shifting operation is accomplished in a manner similar to a maximum (minimum) search. The contents of each memory cell are read out into a mismatch output channel and the shifting takes place by means of a set of conductors located beneath the film plane. The shifted information is written into the appropriate cells by a simple write operation. No more than one equality search is required since the cell readout and final write can be accomplished during the first and last shift cycles, respectively.

5.3.6 Complementing ($X_1 \rightarrow \overline{X}_1$, $X_2 \rightarrow \overline{X}_2$, ..., $X_n \rightarrow \overline{X}_n$)

This is the operation of simultaneously replacing each quantity X by its complement $\overline{X}$.

Memory Array--Type #1 Cells. In this case, the complementing operation is accomplished by performing the following in bit slice X_i during a single general drive cycle: (1) test for match 1, (2) write and (3) local erase. The first operation switches the entire word channel if $X_i = 1$ while the second writes a bit into the cell regardless of its contents. The local erase causes the entire cell to be erased if $X_i = 1$ (tip in word channel at shuttle level--refer to section 4.3), but leaves the cell in its new 1 state ($X_i = 1$ via the second step) if it originally contained a 0. This last condition results from the fact that a test for match 1 against $X_i = 0$ will result in an inhibit in the word channel. No tip reaches the shuttle level (refer to Figure 28a) and, therefore, no local erase occurs. The write does occur, however, and X_i is set equal to 1. In summary, the test for match 1 merely establishes the condition for a local erase on X_i if $X_i = 1$. If $X_i = 0$, no erase takes place and the 1 written into the cell in the second step is stored therein. The time required for a complementing operation per bit is equivalent to two equality searches.

Memory Array--Type #2 Cells. In order to complement the contents of type #2 memory cells X_i, that information is read out into the mismatch 0 output channel and temporarily stored in a special channel designated S_t via a punch-through element and conductor I_t. Subsequently, tips are introduced in the vicinity of S_t and propagation to X_i is gated by the contents of S_t. If $S_t = 1$, the new $X_i = 0$, while if $S_t = 0$, $X_i = 1$ is written.

To perform a complement operation in a particular word, a selection cycle is necessary. A general complement requires that the aforementioned tips be introduced simultaneously in all words of the memory.

Figure 55 schematically depicts the simple channel and conductor configuration located at the output of each word which is utilized in the complementing operation. Control conductor I_c is energized to write the cell output X_i into gate 3 via

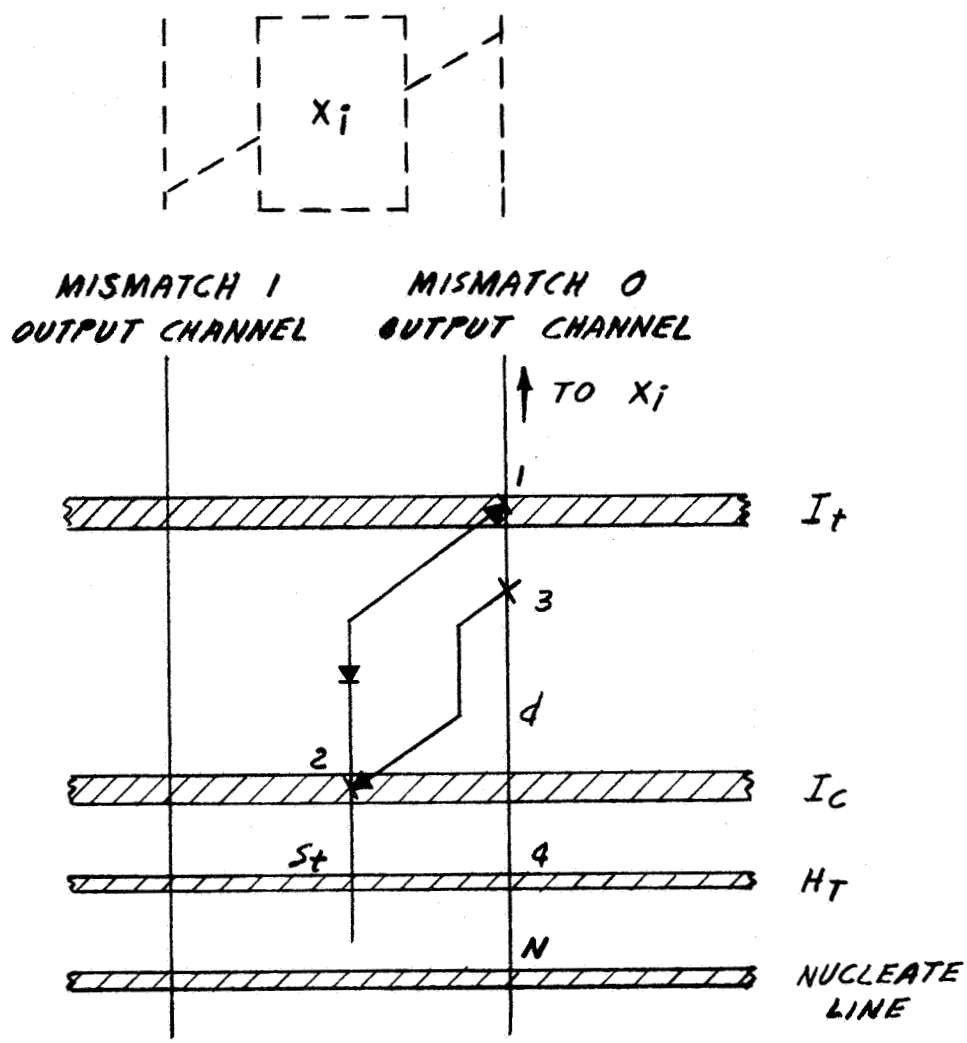


Figure 55 Channel and conductor configuration used in a memory array of type #2 cells for performing the complementing operation.

punch-through element 2; while H_T performs a temporary hold function in the storage channel S_t and channel 4. The nucleate line functions to write tips into all word channels at N if a general complement is desired. Otherwise, a tip is generated by the word selection network and held in 4. Gate 3 inhibits propagation back to X_i if X_i was originally a 1 during the next drive cycle. Two equality search times are then required for a general complement and three for a selected complement.

5.3.7 Logical Sum (X_1US, X_2US, ..., X_nUS)

The logical sum operation is a bit-by-bit ORing of the contents S of the operand register with quantities X stored in different words of memory. The result XUS = Z is written in place of X or stored in a second field.

Memory Array--Type #1 Cells. A simple algorithm has been developed for this operation. Consider the following truth table:

X_i	S_i	$Z_i = X_iUS_i$
0	0	0
0	1	1
1	0	1
1	1	1

To obtain Z_i in a second field, the storage cells for Z_i must be accessed by a control conductor I_1 which is energized when $S_i = 1$ to perform a write function. The logical sum operation begins by introducing domains in all word channels and propagating the tips to the Z_i cells. If $S_i = 1$, I_1 is pulsed and a 1 written in all cells. This satisfies input combination 2 and 4 in the above table. Then an equality search is performed on X_i against $S_i = 1$. In words satisfying the search, a 1 is written in the Z_i cells since I_1 would also be energized at this time. The second operation will make possible an output for $X_i = 1$ and

$S_i = 0$, input combination 3, which is not normally available in a search of X_i against S_i. Two equality search times are thus required for each bit to be summed.

Memory Array--Type #2 Cells. The first half of the procedure described above, i.e., the writing of test tips into Z_i cells if $S_i = 1$, is also required for the logical sum in this array. It is recalled that a write operation in a type #2 storage cell is performed by energizing the I_0 interrogate line ($S_i = 0$). Thus, if the Z_i storage cells are to be type #2, the first write procedure must be such that I_0 is pulsed if $S_i = 1$.

A second search is then carried out on X_i against S_i and I_0 is energized regardless of the value of S_i. This will detect the mismatch $X_i = 1$, $S_i = 0$ (also $X_i = 0$, $S_i = 1$, but this has already been accounted for in the first search) and cause a 1 to be written into Z_i. Again, two equality search times are consumed in the logical sum.

5.3.8 Logical Product ($X_1 \wedge S$, $X_2 \wedge S$, ..., $X_n \wedge S$)

This operation consists of a bit-by-bit ANDing of the operand register contents S and the stored quantities X.

Memory Array--Type #1 Cells. Consider the truth table for the logical product presented below:

X_i	S_i	$Z_i = X_i \wedge S_i$
0	0	0
0	1	0
1	0	0
1	1	1

It is seen that a 1 must be written in Z_i if $X_i = S_i = 1$. If the Z_i storage cells possess the same writing capability as required in the logic sum operation (see

memory array--type #1 cells), then an equality search on X_i against S_i followed by a write Z_i will cause a bit to be written into Z_i when $X_i = S_i = 1$. The mismatch conditions will produce no test tip for writing, while no write can occur for $X_i = S_i = 0$. A single equality search time is required for the logical product performed in this manner.

Memory Array--Type #2 Cells. The algorithm in this case considers the complement of the contents S in the operand register. Thus, we have the following table:

X_i	S_i	$\overline{S}_i$	Z_i
0	0	1	0
0	1	0	0
1	0	1	0
1	1	0	1

Recalling that a write operation in a type #2 memory cell occurs via the mismatch 0 output channel and that a test for match 0 when $X_i = 1$ produces a tip in the same output channel, then an equality search of X_i against $\overline{S}_i$ will produce the desired output for Z_i. That is, if $X_i = 1$ and $S_i = 1$, then $\overline{S}_i = 0$ and a test for match 0 on X_i causes an output in the mismatch 0 output channel from which it may be written in the Z_i cell. Input combinations 1, 2, 3 with S_i replaced by $\overline{S}_i$ either produce no output or a tip in the mismatch 1 channel which cannot be used for writing Z_i. This technique for accomplishing the logical sum then utilizes one equality search with the complement of the operand register.

5.4 Techniques for Processing Results

5.4.1 Introduction

The results of the various search operations such as the matches from an equality search, the words satisfying an inequality or maximum (minimum) search, etc., would normally be represented by a stored bit in one or more flag bit memory

cells associated with each word of memory. While the mechanization of all-parallel on-match operations, i.e., operations in which a bit slice write, local erase, or other function except read are performed simultaneously in all words satisfying a search, is relatively straightforward, the resolving of multiple matches to (1) provide readout in a word slice mode, (2) locate the first empty location for loading the memory, (3) generate an address for each word, (4) enable writing in a word slice mode, etc., represents a formidable problem.

The logic which makes possible sequential selection of the words satisfying a search and thus performs the resolve function is often referred to as a "word select ladder."[7] In this section, several DTPL word select ladder schemes are described and the trade-offs between sense electronics and resolve time considered. The technique for generating an address for "match" words is discussed and a comparison is made of the four methods for reading all match words.

5.4.2 Resolving Techniques

The "basic method" for resolving multiple matches (and the search for an empty memory location on loading) uses a single test tip which scans through the entire memory bypassing those words not containing a match and stopping at the first word on which a match exists. Figure 56 schematically depicts the simple scanning network located at each word and the test tip channel T interconnecting these networks in a serial manner. Channels designated F_1 and F_2 in the figure emanate from flag bit memory cells, while those designated W_1 and W_2 lead to the word or mismatch output channels, depending upon the type of memory array, for an on-match operation. Inhibit gates 1 and 2 in each network implement the required AND function between tips in the F and T channels, i.e., $W_i = F_i \cdot T$.

In performing the resolve operation, a test tip is introduced into the T channel by means of the "write test tip" control conductor and propagated to the first word with a general drive field. If there is a match on this word 1, i.e., if

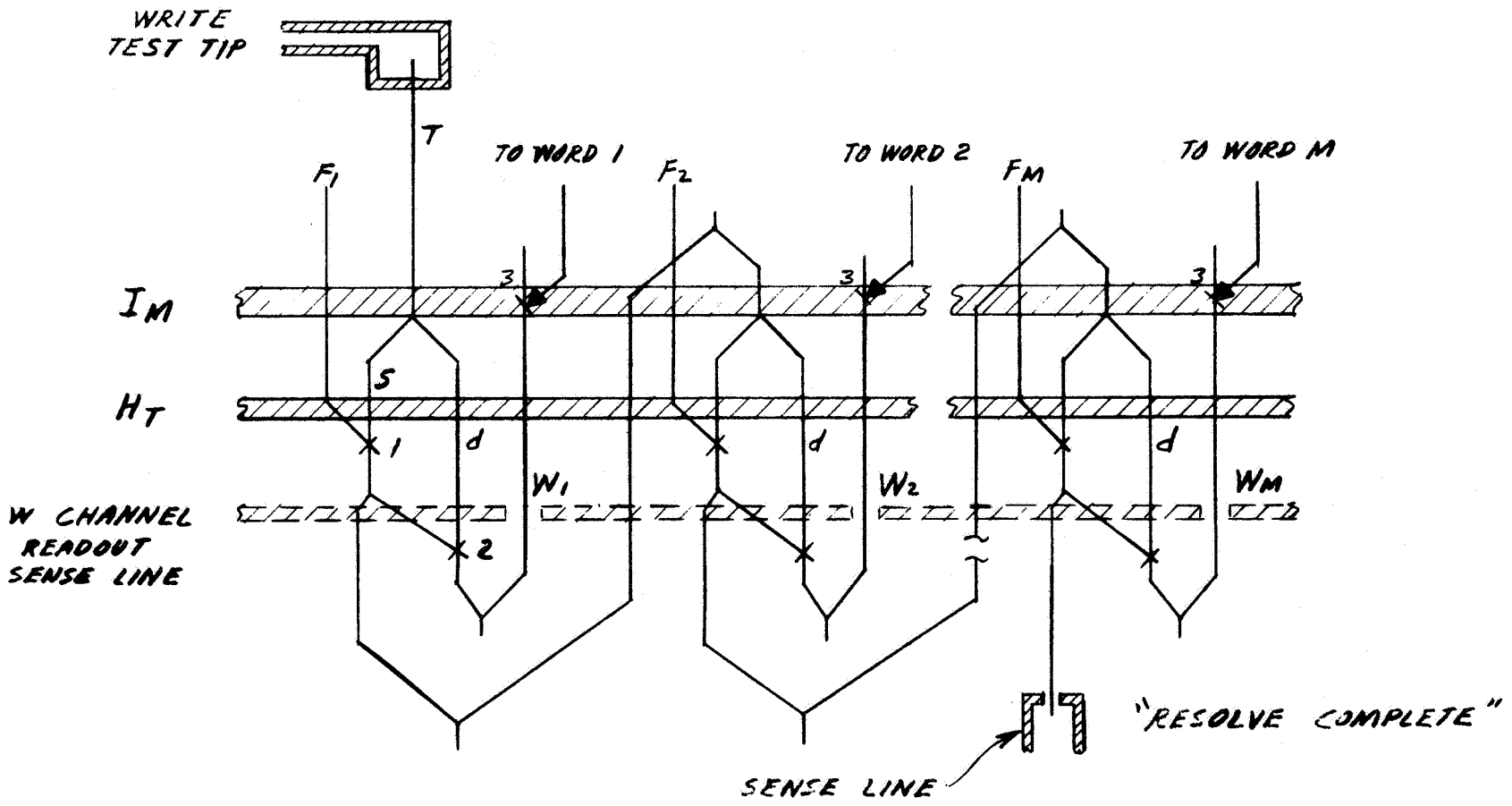


Figure 56 DTPL network for performing the match resolve operation by the "Tip Scan" technique.

there is a flag tip at F_1, the test tip enters channel W_1 and is blocked by punch-through element 3 until the subsequent on-match operation begins. At that time, control line I_M is energized, punch-through occurs, and the test tip performs the on-match operation. Upon completion of the latter by a general erase and hold, the domain stored at S by means of conductor H_T continues to propagate to the next memory word since no domain was present in gate 1 from F_1 of word 1 when this operation began. Now, if the flag tip is absent at word 2, indicating no match, the test tip continues uninhibited through the main channel of gate 1 to the next word. After the final match has been processed, the test tip is sensed at the readout channel designated "resolve complete" and the on-match resolve operations terminated. The same operation occurs if no matches exist in the entire memory. In this manner, a single sense amplifier is used to detect matches.

The basic scanning technique described evidently requires a great deal of tip propagation time since the minimum delay per scanning network would be of the order of 1 μsec. The time to resolve m matches (T_R) would then be equal to mM μsec where M is the number of words in the memory. This assumes that the duration of the propagate or general drive pulse in each resolve operation is equal to the time necessary to scan the entire memory regardless of the location of the first and subsequent matches. One method of reducing T_R is to detect the entrance of the test tip into a W channel, i.e., to obtain a readout when the first or next match word has been located, and use this signal to terminate the general drive pulse. The total time consumed in resolving m matches is designated T_{R_1} and T_{R_1} = M μsec since the sum of the scan times from the first match word to the second, and from the second to the third, and so on to the m^{th} match, is equivalent to a single scan of the entire memory. The W channel readout mentioned above would be accomplished by readout elements located at each of these channels and interconnected to form a single sense line as shown by the dotted line in Figure 56. An additional sense amplifier and logic to gate the general drive pulse would be required then to reduce T_R by a factor of m.

Another method of reducing T_R is to utilize additional sense amplifiers to detect matches separately within a number of segments of the memory. Each sense line would interconnect the readout elements located in the F channels of a segment of words as illustrated in Figure 57. The output of the sense amplifiers are sampled sequentially after the flag tips have been propagated to gate 1, and a test tip nucleated in the T channel corresponding to the first segment containing a match. The "write test tip" control conductor for each segment shown in Figure 57 is operated by a pulse driver which is gated by the output of the corresponding sense amplifier and a general sampling circuit. The scanning operation in the selected segment takes place in the manner described as "the basic method" for resolving multiple matches. It is recalled that, in this case, a sense amplifier was requiredto detect the test tip following the final on-match operation. In the network of Figure 57, this function is accomplished by the sense line interconnecting the "resolve complete" readout elements in each segment as illustrated in Figure 57. This requires an additional sense amplifier, the output of which is used to trigger the aforementioned sampling operation. The latter begins at the next unsampled segment.

In the straightforward implementation of this second variation of the basic resolve technique, the resolving of each match within a segment is performed using a fixed general drive pulse. The duration of this pulse is equal to the time required to scan a complete segment of m' words or m' μsec. Thus, if there are m_1 matches in segment 1, m_2 in segment, etc., the total time to resolve all segments T_{R_2} is given by $T_{R_2} = (m_1 + m_2 + \ldots + m_i)$. If $(m_1 + m_2 + \ldots + m_i) = m$, $T_{R_2} = mm'$ μsec which reduces to mM or T_R when all words are contained in a single segment. However, when the words are divided into i equal segments, this technique makes possible a reduction in T_R by a factor of i, i.e., $T_{R_2} = T_{R/i}$. There is obviously a tradeoff to be made in terms of the reduction in resolve time and the cost of additional sense amplifiers. A starting point for such considerations might be an increase in the number of sense amplifiers to obtain a resolve time equal to the basic equality search

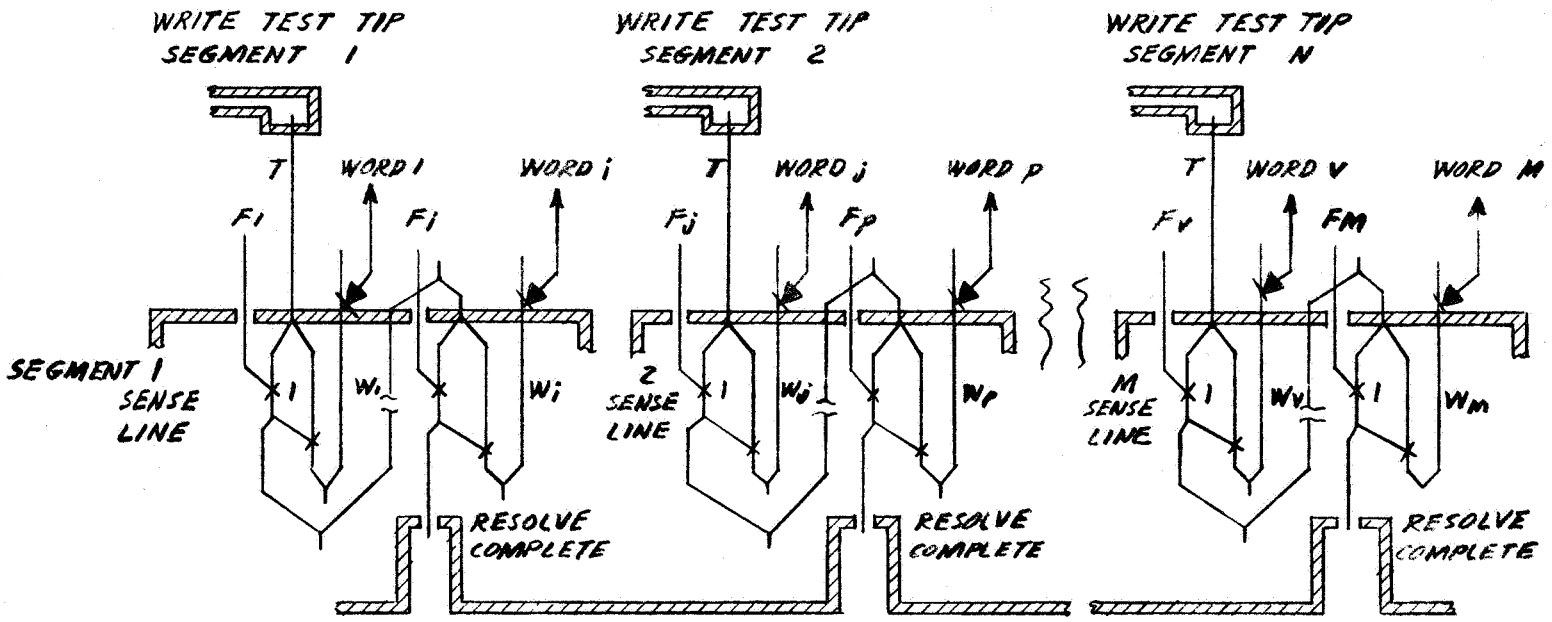


Figure 57 DTPL network used to resolve matches in segments of words.

time which, for a 100-bit per-word array of type #2 memory cells, would be approximately 250 μsec. This implies that an array of 1000 (M) words would be divided into 4 (i) segments of 250 words (m') and 4 additional sense amplifiers utilized.

The choice as to which of the two resolve schemes is most suitable for use in a DTPL associative memory depends upon the average number of matches (m) expected in search operations. We recall that the resolve time using the first method is independent of the number of matches, i.e., $T_{R_1} = M$ μsec, while the second approach depends upon the ratio of the number of matches to segments, i.e., $T_{R_2} = \frac{m}{i} M$ μsec. Thus, when $m/i < 1$, the second approach makes possible a shorter resolve time. Using the value i = 4 determined in the above manner, the inequality requires that the average number of matches be three or less. If M = 1000 words, m = 3 represents an extremely small number of matches. An average match rate of 5 per cent would require that i = 50 to satisfy the above inequality.

It would appear, from these figures, that the use of the segment scan technique is not practical if the number of matches on the average is more than a few per cent of M.

A combination of the two tip scan techniques described previously would considerably reduce the time required to resolve multiple matches. In this method, the words of the memory would be divided into i segments with the scanning of each segment taking place according to the first or W channel readout scheme which makes possible a variable match resolve time. The total time to resolve all matches within a segment (T_{RS}) would then be independent of the number of matches and equal to $\frac{M}{i}$ μsec. The total resolve time T_{R_3} is then dependent upon the number of segments containing matches (i_m). If $i_m = i$, $T_{R_3} = M$ μsec which is the same value obtained previously for T_{R_1}.

However, if one takes into consideration the statistical factor, that is the distribution of matches throughout the memory, it is apparent that $i_m < i$. In particular, as the number of segments increases, the probability of finding a given number of "empty" segments (contain no matches) increases. Since an empty segment is not scanned, the total resolve time is reduced correspondingly. A study of this aspect of the resolve problem is planned to determine the extent these probabilities affect the tradeoffs between resolve time and the cost of additional sense amplifiers for the segments.

An electronic scheme is also being considered as a possible solution to the problem of resolving multiple matches. The technique makes use of the sense amplifiers normally required in reading out of each bit slice and a small number of additional units to sense the outputs from blocks of words into which the memory would be divided. Two flag bit memory cells designated F_1 and F_2 are utilized in each word to store the results of a particular search. One of these special memory-logic networks (F_1) is located at the output end of the word, while the other (F_2) is contained within the word sharing a bit position with a standard type #1 or type #2 bit storage cell. The F_2 cells are located in successively higher or lower order bit positions from word to word in a given block such that the m^{th} word in each block contains an F_2 cell in the n^{th} bit slice. All F_1 cells within a block are interconnected by single sense line which is the input to the block sense amplifier.

A schematic representation of a memory array of type #2 cells organized in the above manner is depicted in Figure 58. It is seen that the F_2 cell in n^{th} bit slice of a word shares the readout channel of the n^{th} bit. Thus, no additional readout elements are required for the F_2 cells, proper isolation being obtained by the diodes D shown in the figure. A detailed description of the operation of the F_2 cells will not be given at this time. A cell design which incorporates the features and requirements of both flag bit and basic memory cells will be investigated.

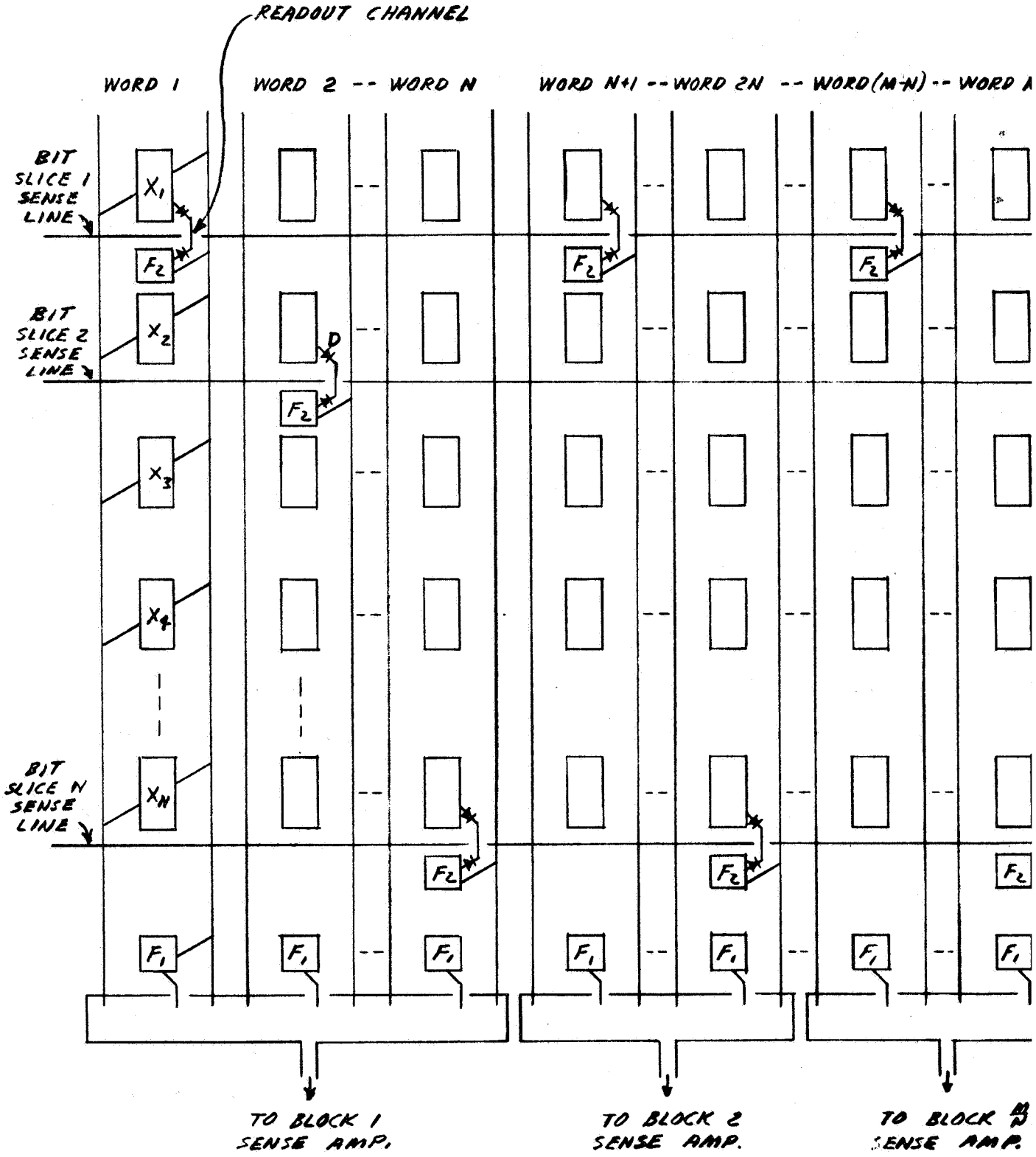


Figure 58 Modified memory array of type #2 cells for performing high speed resolve operation.

Using the configuration shown in Figure 58, the resolving of a match takes place in the following manner: A general drive field is applied and the contents of cell F_1 cells are propagated to their respective readout stations. The outputs of the block sense amplifiers are then sampled sequentially, starting with block 1. Upon obtaining an output, the sequence is terminated and a flip-flop which corresponds to that particular block is set. Next, the outputs of the bit slice sense amplifiers are sampled in the same manner, starting with bit 1. The flip-flop associated with the first bit slice containing a match is set and a general erase and hold operation restores the entire memory to its initial state.

The block and bit slice flip-flops set during this operation thus identify what may be considered as the "address" of the first match. To perform the subsequent on-match operation, this address could be decoded and the match word selected using the DTPL word selection logic. Another approach being considered is to read out the contents of the F_2 cell corresponding to the first match. This would be accomplished by means of two control conductors, one of which passes through all cells in a bit slice while the other passes through all cells in a block of words. The bit slice conductor would be driven by one of the interrogate line drivers, I_1 or I_0, but additional drivers would be required for the conductors which address the blocks. In mechanizing this readout, the output of the aforementioned flip-flops would be used to gate the corresponding bit slice and block drivers. Thus, no decoding or word selection would be required.

The resolve operation is initiated following each on-match operation. While some savings in time can be realized by starting the sampling sequences at the point where it was last terminated, a more straightforward approach would be to begin the procedure at the first block, i.e., utilize an identical resolve sequence for each operation. To this end, additional logic would be required in the F_1 and F_2 cell of each word to inhibit electrical readout from a word previously processed. This is readily accomplished.

The resolve time using the electronic scanning technique would be a few microseconds. This is but a fraction of the minimum time possible with the tip scan approach. The cost of the electronics necessary to implement the former may, however, be prohibitive. These costs will be determined in the second half of the program.

5.4.3 Technique for Generating a Word Address

The problem of generating the address of a word satisfying a search has been investigated and a suitable solution obtained. To perform the operation, it is first necessary to resolve the match by either the domain tip or electronic scanning technique and produce a domain in special readout channel of the word in question. This readout channel is coded with the binary address of the word in a manner which is dependent upon the readout elements utilized. A memory of 2^p words requires a p bit code and p additional sense amplifiers for this purpose.

A binary-coded channel structure is depicted schematically in Figure 59. It is assumed that magnetoresistance readout elements are utilized, although the basic approach is generally applicable to the planar-Hall and inductive readout techniques. Referring to the figure, the X's indicate points where the sense lines, shown as dotted lines, make contact with the magnetic film. The code is established by the presence (binary 1) or absence (binary 0) of these contacts which form the magnetoresistance elements in the p bit positions of the readout channels. The sense lines pass directly across those bits designated as 0's. Thus, when a domain is present in a readout channel, signals are obtained at the sense amplifiers in accordance with the channel code. No signal is obtained for the 0's or the 1's in the unswitched channels. From Figure 50, it is seen that the code for word 1 is (000...0), word 2 (100...0), word 3 (010...0) up to word 2^p which is given by (111...11). A 1000-word associative memory would then require p = 10 sense amplifiers to generate an address in the manner described.

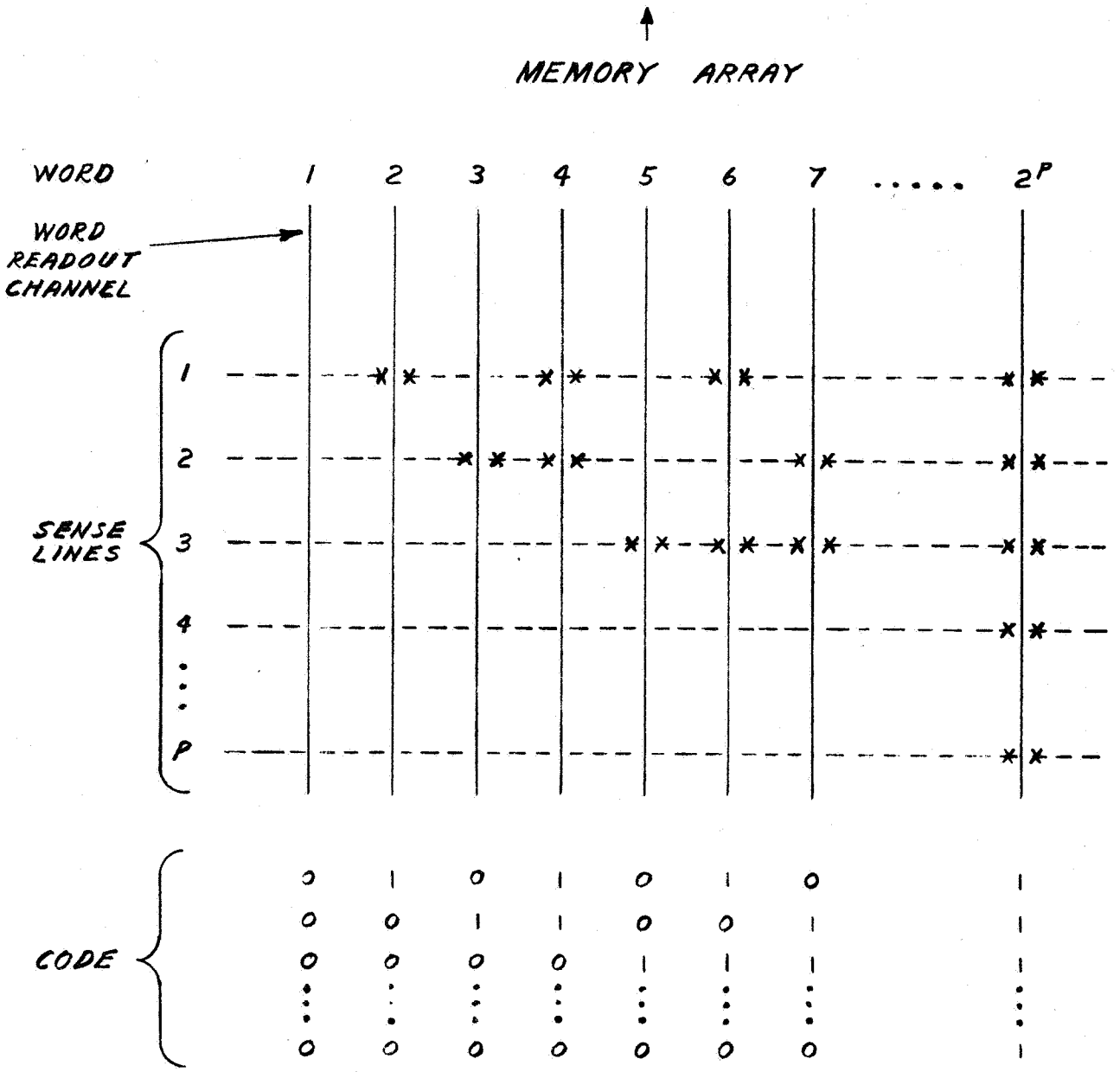


Figure 59 Coded channel structure used in generating a word address.

5.4.4 Methods of Reading All Match Words

Four methods have been considered for performing the operation of reading all match words. These are divided into two categories, one in which the match words are read sequentially, and the other in which an interlaced reading scheme is employed. The time to read all matches is determined for the case when no resolving is utilized, i.e., no selection of matches takes place, and for the case when the multiple matches are resolved. In the discussion which follows, T_p is defined as the propagation delay per bit and M, N and m are the number of words, bits per word, and matches, respectively.

The first technique does not require any selection of matches and words are read one by one. Letting T_1 be the time for the complete read operation, we have

$$T_1 = MNT_p. \tag{20}$$

In the second method, the matches are resolved, but the reading still takes place sequentially. The time for this operation T_2 is given by

$$T_2 = mNT_p + T_R \tag{21}$$

where T_R is the total resolve time. The third and fourth approaches utilize the interlaced reading scheme. In this procedure, the tips which perform the read operation are delayed from entering successive words by T_p, the net delay accumulating between the first and subsequent words. Each bit slice is sensed repeatedly as tips enter the word slices. The results for each word must be assembled by logic external to the array.

Thus, with interlaced reading, but no resolving, we obtain a read time T_3 expressed as

$$T_3 = NT_p + MT_p = (N + M)\, T_p. \tag{22}$$

When the matches are resolved, the interlaced reading technique requires that all matches be resolved before the reading commences. This does not modify the resolve time. In this manner, we obtain a time T_4 given by

$$T_4 = (N + m)\, T_p + T_R. \tag{23}$$

If we assume that T_R is equal to an equality search time, then $T_R = NT_p$.

The table below presents a comparison of the read times obtained by the four schemes. The ratio T_i/T_p is calculated since it is a constant factor in each case. The values M = 1000 and N = 100 have been chosen to represent a typical associative memory for spaceborne application [8] and m is considered as the variable factor.

			Sequential Read		Interlaced Read	
N	M	m	T_1/T_p	T_2/T_p	T_3/T_p	T_4/T_p
100	1000	10	100,000	1,100	1,100	210
100	1000	50	100,000	5,100	1,100	250
100	1000	100	100,000	10,100	1,100	300
			no resolve	resolve	no resolve	resolve

It is apparent that a considerable reduction in read time is possible by employing the interlaced read mode of operation in conjunction with the resolving of matches. The sequential read technique (T_2), although relatively slow, is much easier to implement, and may prove to be the only technique which is feasible. Additional study of the interlaced read approach is planned to determine the tradeoff between read time and the cost of external logic and storage required for this technique.

5.5 Summary

A summary of the times required to perform the various search and processing operations described in the preceeding sections is presented in the tables on the following pages and serves as a means of comparing the basic memory arrays under investigation. The techniques for processing the results of searches, i.e., resolving of multiple matches, generation of a word address and readout of match words, are independent of array type and will not be considered.

Referring first to the table for search operations, it is seen that in each array, one operation is described as "not presently possible." On the basis of the fact that the maximum (minimum) search is more widely utilized than the proximity search in spaceborne associative processors,[9] it would appear that an array of type #1 cells is not suitable for these purposes. The significantly greater time required to perform the inequality search in this array further substantiates the above conclusion. Although the remaining searches are carried out in approximately the same number of operations in each array, the basic unit of search time is smaller in array of type #2 cells. Taking all search operations into consideration, it is apparent that the second array type is definitely superior.

A similar conclusion is drawn when one considers the table for processing operations. The preliminary specifications for a DTPL associative processor presented in section 7 are based, therefore, upon an array of type #2 cells.

Times to Perform Search Operations - 100 Bits/Word

Basic Units of Time { T_{s_1} for array of type #1 cells; T_{s_2} for array of type #2 cells

Memory Array	Equality	Inequality	Max (Min)	Proximity	Intersection of K Searches	Union of Searches
Type #1 Cells	$T_{s_1} = 400\ \mu sec$	$50\ T_{s_1}$	Not presently possible	$2\ T_{s_1}$	$\sum$ Individual Searches $+ KT_{s_1}$	$\sum$ Individual Searches
Type #2 Cells	$T_{s_2} = 250\ \mu sec$	T_{s_2}	T_{s_2}	Not presently possible	$\sum$ Individual Searches	$\sum$ Individual Searches

Times to Perform Processing Operations

	Field Addition/Bit $X+Y=Z\rightarrow$(third field),	$X+Y=Z\rightarrow(Y)$	Operand Addition/Bit $X+S=Z\rightarrow$(second field)	Summation/Bit $X_1+X_2+X_N$	Counting/Bit $(X+1)\rightarrow X$	Shifting
Type #1 Cells	$8\ T_{s_1}$	$9\ T_{s_1}$	$5\ T_{s_1}$	$6\ T_{s_1}$	$4\ T_{s_1}$	Not possible
Type #2 Cells	$8\ T_{s_2}$	$9\ T_{s_2}$	$4\ T_{s_2}$	$5\ T_{s_2}$	$4\ T_{s_2}$	T_{s_2}

	Complementing/Bit $X\rightarrow\overline{X}$	Logical Sum/Bit $X \cup S$ (second field)	Logical Product/Bit $X \cap S$ (second field)
Type #1 Cells	$2\ T_{s_1}$	$2\ T_{s_1}$	T_{s_1}
Type #2 Cells	$2\ T_{s_2}$	$2\ T_{s_2}$	T_{s_2}

6. MATERIALS AND FABRICATION STUDIES

6.1 Introduction

During the first six months of the program, the materials and fabrication studies were concerned principally with the problem of fabricating multilayer DTPL associative memory structures on a single substrate and the investigation of laminated magnetic films. The improvements in the design of DTPL memory cells and arrays which are possible when these film-film logic networks are constructed as integrated devices has been described previously in section 4.3.4. Laminated films are of particular interest due to their characteristically low switching fields and high switching speeds in comparison to single magnetic layers. In terms of DTPL and an associative memory, their use would make possible a reduction in tip coercivity (power) and an increase in tip velocity (speed).

6.2 Multilayer Structures

The basic method of fabricating film-film DTPL memory logic structures is described as the superimposed-film technique. In this approach, separately prepared magnetic film elements, each containing a portion of the network channel pattern, are superimposed, registered to one another and bonded together with a suitable adhesive. A cross-sectional view of the completed structure is shown in Figure 60.

While this technique has been employed in the fabrication of small associative memory arrays (see section 4.3.3) of preliminary cell configurations for study purposes, it is not practical for constructing large arrays, nor can it be utilized with smaller cell structures. In the case of large arrays, the problem would be that of maintaining a uniform film-film separation of the order of .0002 ± .0001 inch. With respect to small cell structures, it is seen that the high density of DTPL logic elements would require concentrated fields from the control conductors located beneath the film element. This would not be achieved in a superimposed-film device as described in section 4.3.4 due to the relatively large film-conductor separation which exists under these circumstances.

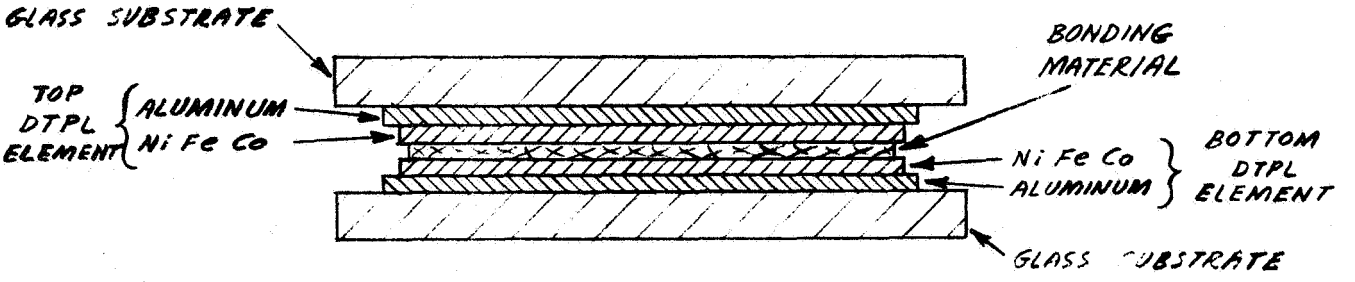


Figure 60 Cross-section view of multilayer structure fabricated by superimposed film technique.

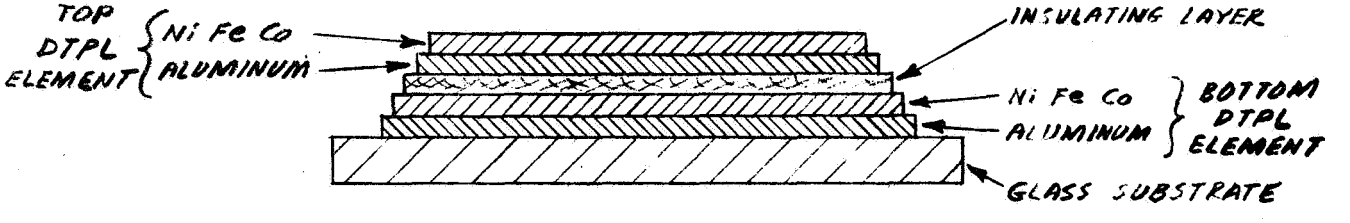


Figure 61 Multilayer structure fabricated on a single substrate.

The fabrication of two aluminum and magnetic layers on a single glass substrate would solve the second of the above problems, as it makes possible intimate contact between film elements and control conductors of the DTPL associative memory. This so-called multilayer structure is illustrated in Figure 61. The insulating layer located between the first magnetic and second aluminum films serves as a protective coating for the former during the photo-etching procedure involving the latter. Its other function is to smooth out any surface roughness which is present in the regions of the first magnetic layer deposited over aluminum. To be precise, the tip coercive force in a channel of the second magnetic film deposited over the insulating layer must be the same as the value obtained for that channel and film evaporated directly on a glass substrate.

In early multilayer DTPL structures, the insulating layer consisted of approximately 10,000 Å of silicon monoxide (SiO) prepared by vapor deposition. Although the evaporation of SiO is a reasonably straightforward procedure, problems exist in controlling its thickness and surface properties. Furthermore, the properties of an aluminum layer on SiO depend upon the thickness of the SiO and differ from those of a similar layer deposited on glass. Experiments have shown that the desired properties can be obtained by lowering the substrate temperature, but here again, control of the SiO thickness is required.

The effort to find a suitable insulating layer has continued during the first half of this program. Initial experiments were performed using an exposed layer of Kodak Thin Film Resist (KTFR) in place of the SiO. The resist is applied uniformly with a simple spinning apparatus. Its thickness is controlled by the amount of material utilized and the spinning speed.

In contrast to results of the work with SiO, it was found that the deposition of aluminum over photoresist must take place at higher substrate temperatures in comparison to an identical layer over glass in order to achieve a high coercive

force in an overlying magnetic film of normally low coercive force. First experiments produced sporadic behavior from sample to sample, i.e., some magnetic films possessed the desired high coercivity over the aluminum while others appeared as if they were deposited on glass. Incomplete baking out of the solvents contained in the resist was considered as a possible explanation for these variations. Subsequent experiments were performed in which the bake-out time was varied in a controlled manner. Improvements were noted, but the experimental results for the coercivity of a film on the aluminum could not be correlated.

The major problem with the photoresist is its susceptibility to cracking during the aluminum deposition which requires substrate temperatures in the vicinity of 260° C. These cracks would most likely cross channels in the photo-etched aluminum and behave as imperfections such as scratches, etc., which normally affect the propagation of channeled domain tips. Attempts to eliminate cracking have not been successful, and further study of the photoresist technique has been discontinued.

What appears as the solution to the problem of an insulating layer has been found in the form of duPont Pyre M. L. Pyre M.L. is a polymide solution which may be spun on a substrate like photoresist. Upon baking at 100° C for 30 minutes and another hour at elevated temperatures (about 250° C), it hardens and behaves as glass during the subsequent aluminum evaporation. The desired properties of the aluminum layer have been achieved experimentally without modifying the standard aluminum deposition procedure. Studies of Pyre M.L. coatings are still required, however, to insure proper uniformity of pinhole-free thin layers about .0001 inch thick. Additionally, techniques must be developed to obtain imperfection-free surfaces. Work in these areas is planned for the second half of the program.

6.3 Laminated Magnetic Films

Clow[10] and other workers have reported that very low domain wall coercivities of approximately .2 oe are obtained in laminated, 1000 Å thick, 80-20 nickel-iron films. These films consist of ten magnetic layers, each 100 Å thick, interleaved with silicon monoxide layers of comparable thickness deposited alternately in the same vacuum. It is recalled that a single layer, 1000 Å thick film of the above composition normally exhibits a wall coercivity of 1.5 to 2.5 oe.

An explanation of the effect proposed by Clow is that the domain wall energy is reduced in the laminated structure. Figure 62a shows diagrammatically a cross section through a Néel wall in which exchange interaction causes the whole of the magnetization inside the wall to lie in essentially the same direction. A large free pole energy results. In a laminated film, no exchange interaction exists through the SiO layers, and the magnetization can align itself as shown in Figure 62b in order to reduce its magnetostatic energy. This energy reduction may account for the very low coercivity.

In addition to the low wall coercivity obtained in multilayer films, an increase in the switching speed (inverse switching time) has also been observed[11] which is directly proportional to the number of laminations. In a ten-layer film, the inverse switching time is ten times greater than in a single film of the same thickness. Behavior of this type finds direct application in DTPL associative memory arrays where tip propagation velocity is the factor which limits the speed at which most searches can be performed. A reduction in tip coercivity, and thus drive field requirements, would also be possible with laminated magnetic films leading to an even greater reduction in power requirements.

With these potential improvements in mind, the study of laminated DTPL films was initiated. Film samples containing propagation channels were fabricated

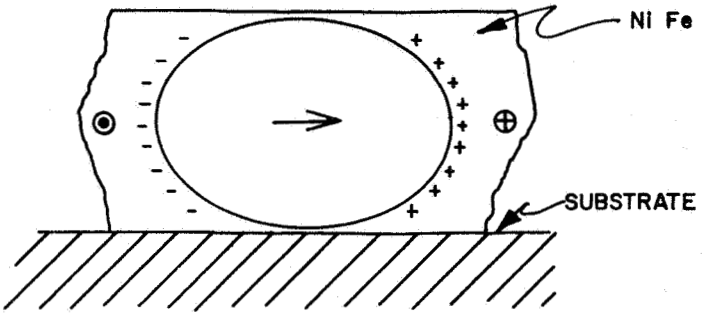


Figure 62 (a) Néel Wall in a Single Magnetic Layer

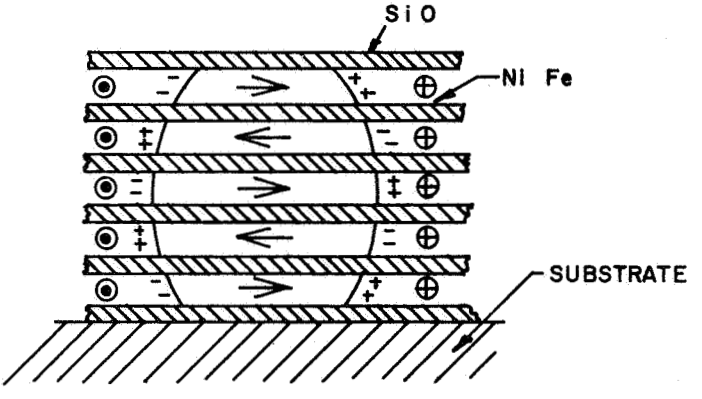


Figure 62 (b) Domain Wall Magnetization Configuration in Laminated Magnetic Film

with from two to ten layers using SiO and NiFeCo evaporants and a special shutter arrangement in the same vacuum system. Tip coercivity was reduced from 2 oe to .5 oe and velocity nearly doubled at a given value of applied field. The nucleation threshold normally 12 to 15 oe in single-layer, 13 per cent Co films was, however, only 5 oe with 10 laminations and approximately 8 oe in a three-layer structure.

In all cases, the net flux of the film over aluminum was less than that for the laminated films deposited directly on glass as measured using the BH loop tracer. It is believed that the first layer in these films, which may be 150 to 500 Å thick, is of very high coercivity over the aluminum and is not being switched or contributing to the net flux of the film. Such layers are characterized by a high dispersion in the magnetization which may be the cause of the low nucleation fields measured. Experiments are in progress to determine the aluminum necessary to obtain high anisotropic coercivity and a high nucleation field in a single magnetic film 300 Å to 500 Å thick. Additional laminations will be tried with the goal of maintaining the desired characteristics for the film on aluminum while obtaining a low coercivity and high nucleation field within the channels.

7. PRELIMINARY DESIGN AND SPECIFICATIONS FOR DTPL ASSOCIATIVE PROCESSOR

7.1 Introduction

It is the intention of this section to present a general description of a DTPL associative processor designed on the basis of the first six months' study effort, the specific areas of which have been discussed in sections 2 through 6. A preliminary memory array organization is described and the power requirements of typical film-control conductor-drive coil assemblies calculated. The electronics requirements for a typical system are then considered in the final subsection.

7.2 Memory Plane--Storage Cells and Logic Configurations

The type #2 DTPL memory cell has been shown to be most suitable for performing both the storage and logic functions required in an associative processor. This configuration will, therefore, be utilized as the basic storage element in the proposed memory array.

In section 5, it was stated that the bits of a word could be divided into segments to reduce search time by a factor of two or more. The physical separation between these segments or their outputs which exists in most cases under these conditions necessitates the use of galvanomagnetic, rapid information transfer elements (see section 2.2) in order to fully realize the savings in time that segmentation makes possible. Although the feasibility of these transfer elements has been demonstrated, additional experimental work is required to improve their operating margins. Thus, at this time, a preliminary memory array design based on the above technique would not be practical.

An equivalent approach is to organize the word structure such that the outputs from all segments are available at the same location on a film plane with the

additional provision that the outputs from successively higher (lower) order bit slices be delayed with respect to each other. The latter is a necessary condition for performing the inequality and maximum (minimum) searches (see sections 5.2.2 and 5.2.3).

An array organization which meets the aforementioned requirements is depicted schematically in Figure 63. It is seen that the bits of a word are contained in two columns in a "staggered" arrangement. In this manner, all interrogate lines can be located in one layer, the local erase conductors in a second layer, and a physical separation between cell outputs achieved. While the array density remains at 280 bits per square inch for these type #2 memory cells fabricated using a multilayer structure, the linear density parallel to the word axis (vertical in the figure) is increased from 11 to 22 bits per inch. As a result, the basic unit of search time, T_{s_2}, is reduced from 250 to 125 μsec. The linear density perpendicular to the word axis is now only 12.5 words per inch.

The proposed processor will consist of 1000 words with 100 bits per word. Taking into consideration the additional space required for (1) word selection logic, (2) search and processing control and flag bits and (3) word slice logic (resolve logic, address generation structure, etc.), the total length of a word slice would be approximately 6 inches. Based upon present magnetic film deposition technology, one might assume a typical memory plane size of 3 square inches. Thus, a given word would require two film planes and a total of 37 words would be contained in this film pair. A preliminary layout of the storage cell and logic structures is depicted in Figure 64. The small film element described as the "transfer element" is used to magnetically interconnect the corresponding mismatch output channels of each word in the two memory planes. With such an organization, a complete 1000-word system would consist of 27 film pairs, or a total of 54 planes.

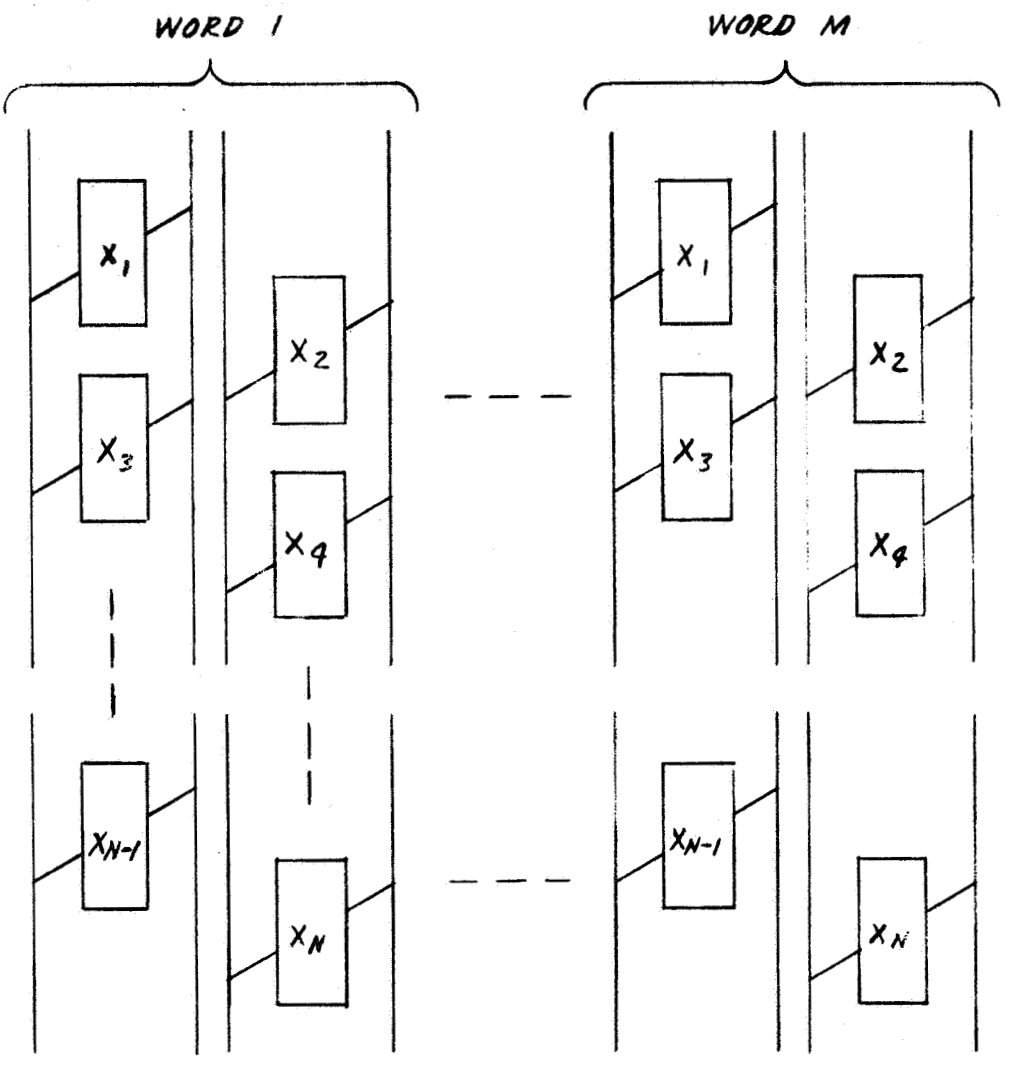


Figure 63 Memory array of type #2 cells organized to reduce search time.

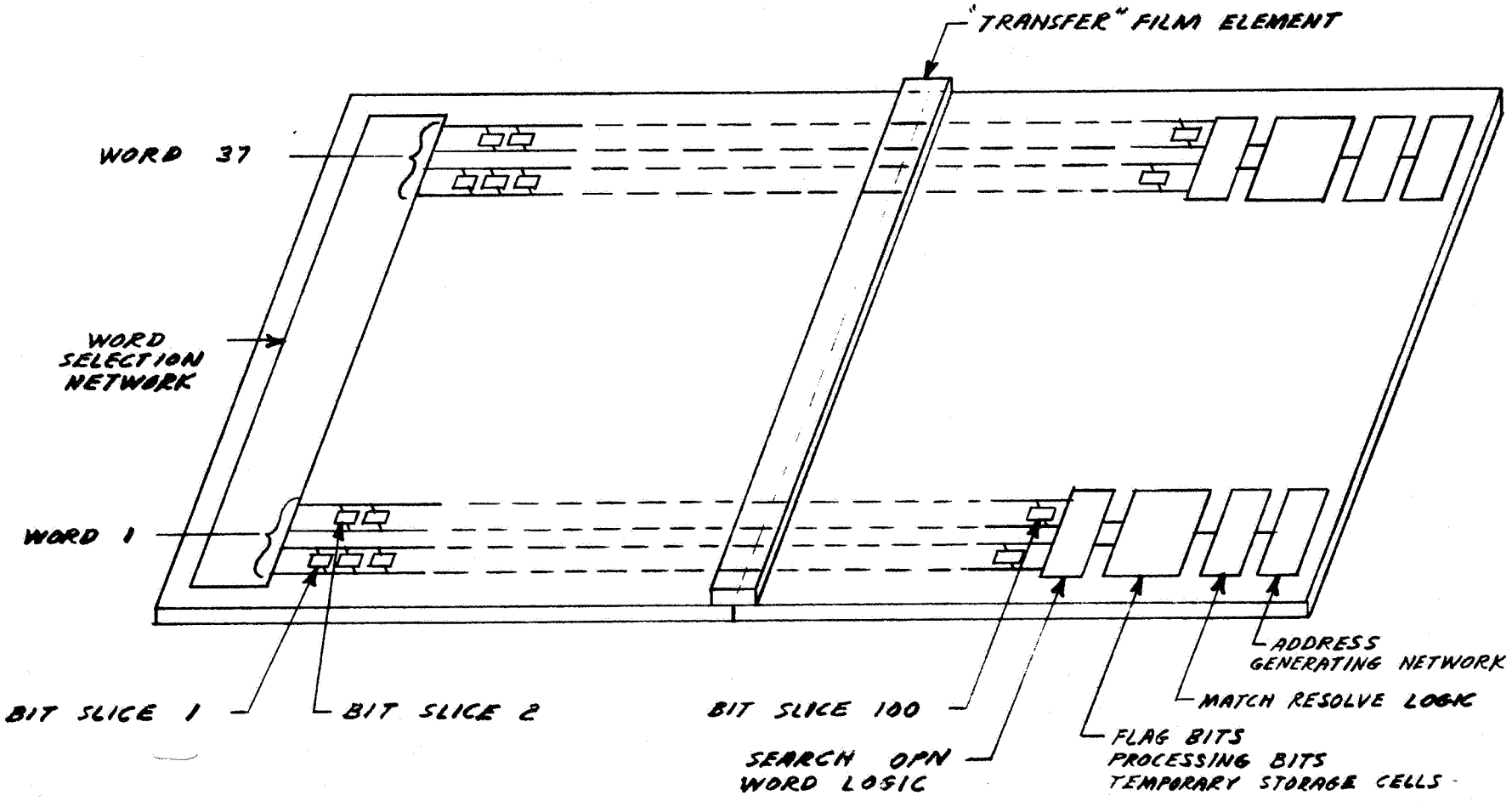


Figure 64 Preliminary layout of type #2 memory cells and logic structures on a film plane of a DTPL associative processor.

7.3 Memory Plane--Control Conductor--General Drive Coil Assembly

The determination of the optimum number of memory planes per drive coil assembly depends upon the relative tradeoffs between the cost of several low-power, .5-to-1-ampere pulse driver circuits and a small number of high-power units. At one extreme, we have the case of a single 3-inch-square magnetic film element per coil, while at the other extreme, one would consider all 54 planes driven by a single general drive coil. Let us choose the former as a reference and calculate typical voltage and power requirements for this configuration.

To begin with, a coil wrapped around a 3-inch-square film element and capable of producing 10 oersteds per ampere of drive current would be characterized by an inductance L_c of approximately 5 μh and resistance R_c of approximately 1.7 ohms. The voltage (V_c) required to achieve a .75-ampere pulse (I_c) with a 1 μsec risetime (t_R) is then equal to $L_c I_c/t_R + IR \approx 5$ volts. Assuming an additional 5 volts for current regulation, we obtain a power supply voltage requirement of $V_s = 10$ volts. The total power supplied by the source for a single coil assembly is approximately equal to $V_s I_c$ or 7.5 watts for a 100 per cent duty cycle. A complete system would then consist of 54 of these coil assemblies which yields a total power requirement of over 400 watts for most search and processing operations. If one chooses to drive each half of the pair shown in Figure 64 for half of the total drive cycle, i.e., for the time required to propagate tips across a given plane, a 50 per cent reduction in system power is obtained. Further segmentation of the drive coils and proper sequencing of drive pulses would make possible greater power savings at the expense of increased electronics cost.

In order to decrease power and electronics cost, the number of film planes per drive coil assembly must be increased. As an example, consider the case of 4 planes per coil. Under these conditions, the drive coil inductance would be 20 μh

(coil cross-sectional area is increased by a factor of 4) with the resistance remaining relatively unchanged at 1.7 ohms. The voltage requirements for the aforementioned current pulse I_c is given by (20) (.75) + (1.7) (.75) volts, or 16.25 volts. With regulation, we have a new V_s of 21.25 volts. Power supplied by the source to drive the four film plane coil assembly is now equal to 15.9 watts. In this manner, then, 4 planes can be driven with only twice the power necessary for a single plane. The total system power using the simple drive coil segmenting scheme described previously is then reduced from 200 watts to ~ 110 watts since only seven coils are driven at a time (duration $\approx \frac{\text{general drive cycle}}{2}$).

A simple expression for determining the total system power as a function of the number of planes per coil assembly (n) can be derived as follows: First we assume that the drive coil inductance (L_T) is directly proportional to n, i.e., $L_T = nL_c$, and the resistance (R_T) is relatively independent of n, i.e., $R_T = R_c$. The supply voltage required for each coil assembly V_s is then given by $V_s = (nL_c/t_R + I_c R_c + 5)$ volts, where t_R is the drive pulse risetime and 5 volts is utilized for regulation. With the number of coil assemblies required (N) equal to 27/n, the total system power (P_T) is expressed as $P_T = 27/n\ V_s I_c$. Letting I_c = .75 amperes, t_R = 1 μsec, L_c 5 μh, and R_c = 1.7 ohms, we obtain $P_T = 27/n\ [\ n(5)\ (.75) + (.75)\ (1.7) + 5]\ (.75)$ watts, which produces to P_T = (76 + 129/n) watts. If the n = 27 (all planes in a single drive coil assembly), a minimum P_T of 81 watts is obtained. Further reduction of P_T will necessitate dividing the drive coil(s) into more than the two segments considered in the above derivation. The tradeoffs involved in optimizing the drive coil assembly will be investigated during the second half of the program. Other approaches, e.g., use of a drive field which is "on" at all times, to limit the voltage and thus power requirements will also be considered.

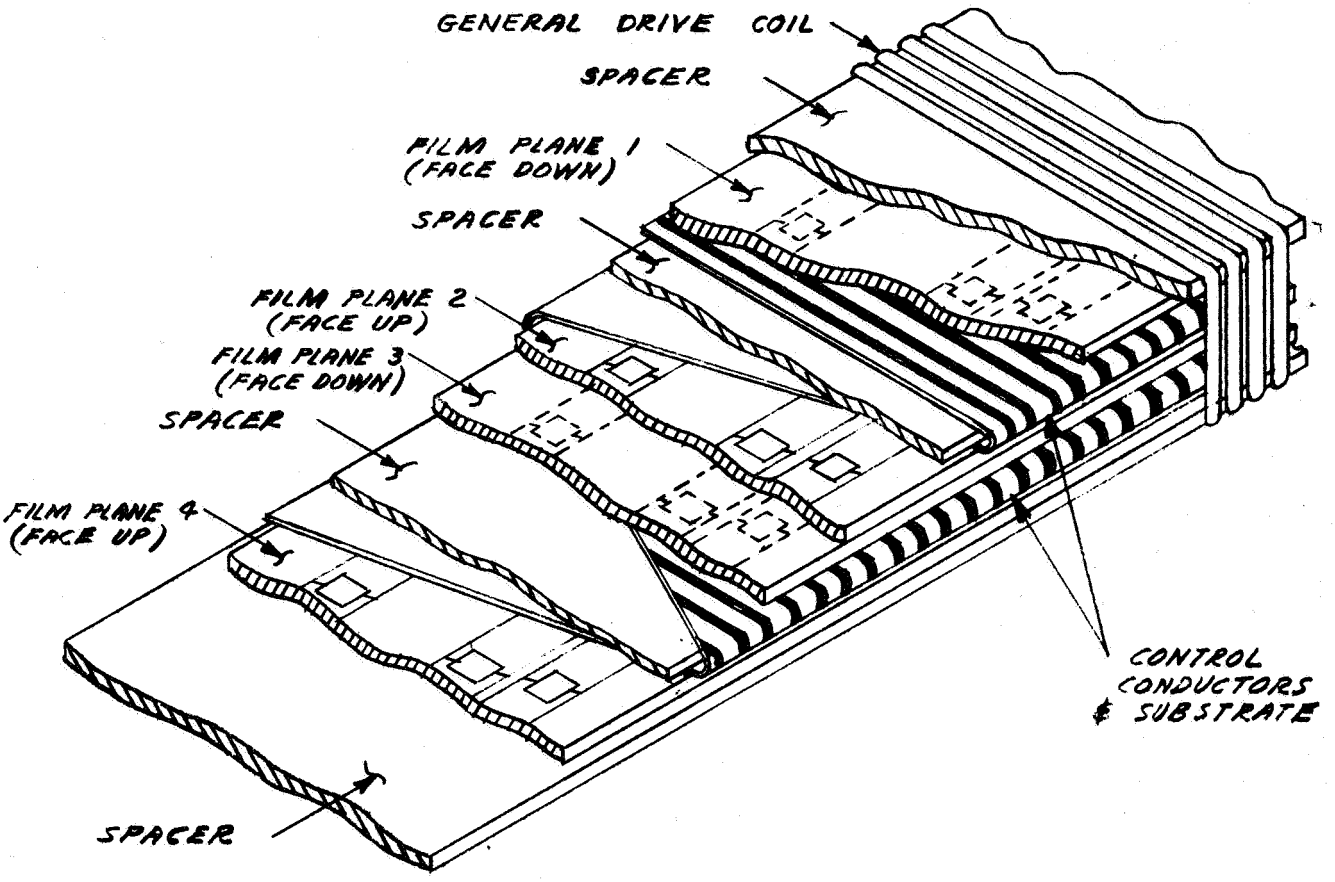
As an illustration of the configuration of memory planes and control conductors in a coil assembly of the type under discussion, let us consider the four-plane

structure depicted in Figure 65. Part a of the figure shows a cut-away view of what may be described as a "memory stack" with the cross-sectional view presented in part b. The film planes are fabricated using multilayer techniques (see section 6.2) and positioned face down on the control conductors. The latter are contained on a single mylar or epoxy bond substrate which passes through the stack in such a way that all planes face the same side. In this manner, registration and bonding of film planes to this substrate may be easily performed prior to a folding procedure which produces the final configuration. The spacers indicated in the figure provide the separation between adjacent control lines required to minimize stray control fields. The substrates of the two center film planes function as the spacer in that region. Methods of interconnecting the control conductors of the different stacks are not shown in the figure. It is assumed that a simple scheme employing "plug-in" type cards and connectors would be utilized.

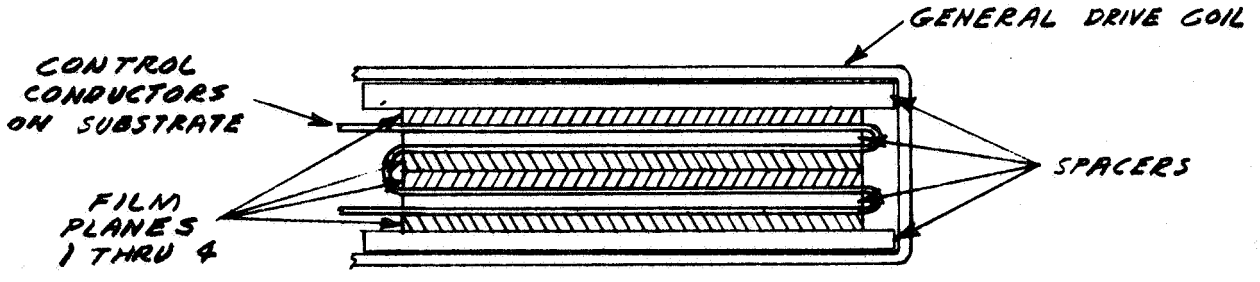
7.4 Electronics Requirements

The electronics required in a DTPL associative processor can be divided into the following four categories: (1) general drive, (2) control, (3) logic and (4) sense. The general drive circuitry will depend upon the number and size of the coil assemblies. Although considerable savings can be realized through the use of multiple plane stacks, the problem of field uniformity becomes a factor under these conditions. A possible system configuration would be the 4-plane stack illustrated in Figure 65. It is recalled that each stack is composed of two general drive coils. Thus, a total of 14 bipolar drivers would be required to produce the general drive and erase fields in the seven memory stacks.

The control electronics would be comprised of: (1) 300 interrogate and local erase line drivers for the 100 bit slices, (2) 14 hold line drivers (2 per stack), (3) approximately 12 control conductor drivers for flag bits and control operations, (4) 11 drivers for the DTPL word selection logic, (5) 14 drivers for the



a.



b.

Figure 65 Configuration of memory planes and control conductors in a coil assembly (stack) of a DTPL associative processor.

shift conductors required in the maximum (minimum) search, and (6) 7 nucleate line drivers for the resolve logic networks. Most of these circuits would be low power since the duty cycle is approximately 10 per cent for control functions.

Logic circuitry in the proposed associative processor would consist of all of the devices and networks required for the command and control of the system electronics. Search and mask registers are included in this category in addition to the flip-flops for the resolving of multiple matches (see section 5.4.2).

The sense electronics would consist primarily of 100 bit slice sense amplifiers for the readout of stored information. An additional 100 drivers would be required to supply the magnetoresistance readout element drive currents. The DTPL address generation logic described in section 5.4.3 would utilize 10 sense amplifiers with the associated current drivers, while the resolve logic would necessitate another 14 sense amplifiers and drivers.

A more thorough analysis of the electronics requirements is planned for the second half of the program when the various tradeoffs between speed, power and cost and stack assemblies have been determined.

8. PROGRAM PLAN FOR SECOND HALF

The general work plan for the second half of the program is presented in Figure 66. It consists of many individual study efforts, each of which is concerned with a basic problem in the design of a DTPL associative processor. The specific plan for each task is as follows.

Final Memory Cell Design.

It is the intention of this task to finalize the design of the basic type #2 DTPL memory cell presently under investigation. New and improved type #2 memory-logic structures will be sought with the goal of reduced size and propagation delay.

Final Evaluation--Memory Cell Structures

The final memory cell designs resulting from the preceeding task will be implemented, tested and evaluated. Multilayer techniques will be utilized in fabricating these networks to minimize film-control conductor separation.

Final Evaluation of Selection Network

The improved selection network described in section 3 which utilizes the DTPL punch-through elements will be constructed and tested. A final design suitable for use in the proposed processor is the goal of this effort.

Search Techniques

Improved methods of performing the inequality and maximum (minimum) searches will be investigated. Accurate propagation velocity techniques are required specifically for the inequality search.

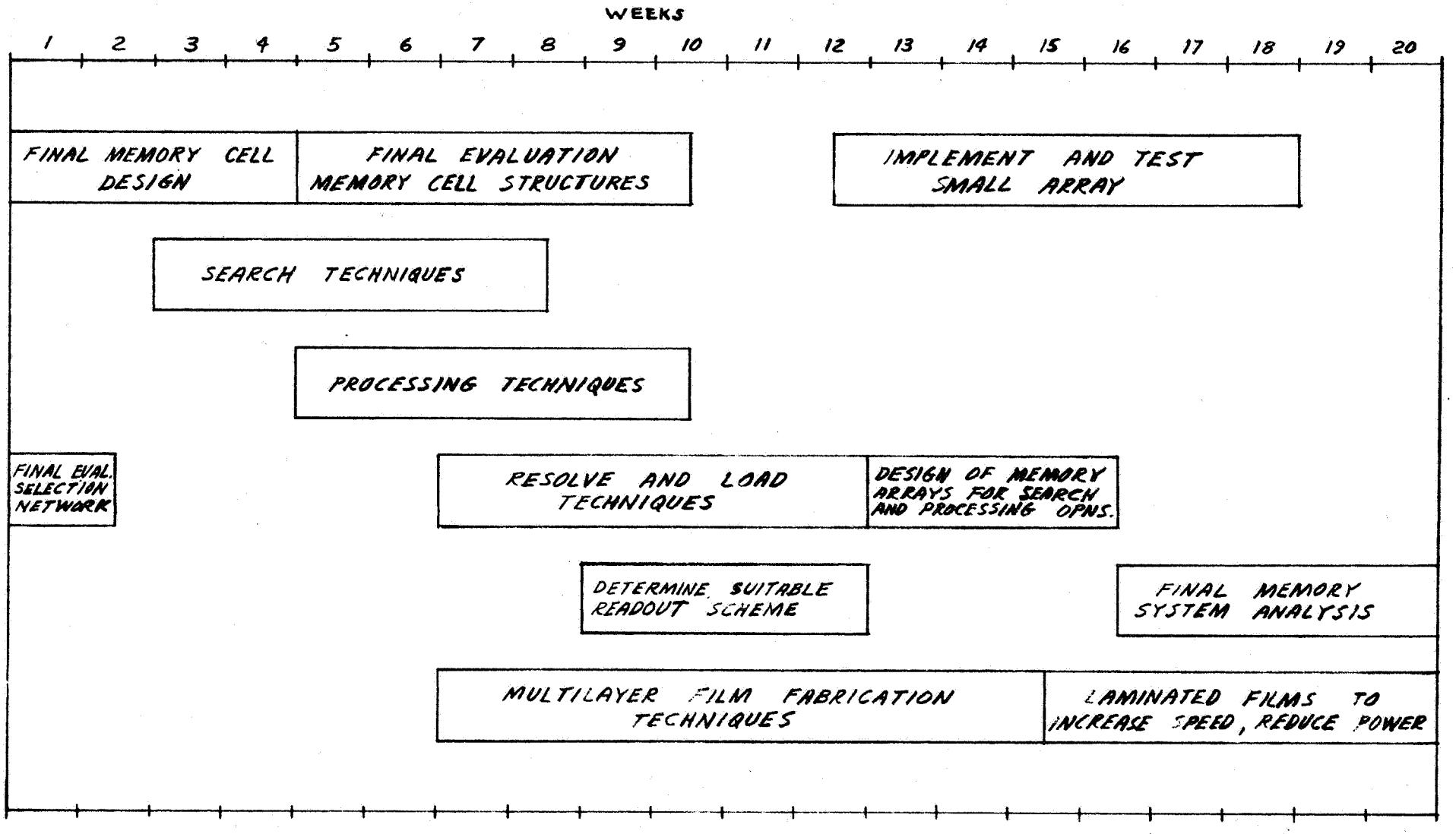


Figure 66 Work plan for second half of program.

Processing Techniques

Techniques for reducing the number of operations required in performing a field addition, operational addition, etc., will be sought. The use of multi-purpose control bits to minimize the number of these structures is of particular interest.

Resolve and Load Techniques

The tradeoffs between the cost of electronics and reduced resolve and load time will be considered. Techniques for performing these critical functions will be finalized.

Determine Suitable Readout Scheme

The various techniques for reading out of a DTPL channel will be evaluated on the basis of signal amplitude and complexity of readout element fabrication. This will require a study of long sense lines which interconnect many substrates.

Implement and Test Small Array

A small memory array incorporating the final memory cell design and capable of performing selected search and processing operations will be constructed and evaluated. This structure will serve to demonstrate the feasibility of the DTPL technique for implementing the functions of an associative processor.

Design of Memory Arrays for Search and Processing Operations

Memory array organization will be investigated in an effort to reduce the basic search time. Various techniques of segmenting the bits of a word would be considered and word structures finalized.

Final Memory System Analysis

Memory plane-drive coil assemblies will be studied and tradeoffs established. With the final configuration chosen, an analysis of the speed, power, cost and size of a 1000-word, 100-bits-per-word associative processor would then be performed.

Multilayer Film Fabrication Techniques

The techniques for fabricating multilayer DTPL memory planes on a single substrate will be studied experimentally. Uniformity of the insulating layer (see section 6.2) is of particular importance.

Laminated Magnetic Films to Increase Speed, Reduce Power

The improvements possible through the use of laminated magnetic layers are significant. Experiments will, therefore, be performed to determine the feasibility of this approach and the extent to which these improvements can be realized.

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NEW TECHNOLOGY APPENDIX

It is the opinion of the writer that most, if not all, of the material in this interim report should be classified as New Technology as it applies to the design of an associative processor. This report describes the first study effort inwhich DTPL techniques have been developed expressly for use in advanced associative processors.

Personnel

The NASA Project is under the direction of H. I. Jauvtis. Dr. R. J. Spain, Manager of the Applied Research Department, until his departure from LFE, made major contributions to the work reported here. Significant contributions were also made by J. Veronelli.