FINAL REPORT

STUDY OF STATE-OF-THE-ART STATIC INVERTER DESIGN

PREPARED FOR

NATIONAL AERONAUTICS and SPACE ADMINISTRATION

JUNE 16, 1966
CONTRACT NAS 9-5580

VARO
STATIC POWER DIVISION
BIOMETRICS INSTRUMENT CORP.
1600 DALLAS NORTH PARKWAY,
PLANO, TEXAS 75074

VARO-VSPER 0005

FINAL REPORT

STUDY OF STATE-OF-THE-ART STATIC INVERTER DESIGN

BY

C. L. PAYNE, M. G. WARFORD, D. C. NIPPER,
J. P. SMITH, AND J. D. GILLETT

PREPARED FOR

NATIONAL AERONAUTICS and SPACE ADMINISTRATION

JUNE 16, 1966
CONTRACT NAS 9-5580

TECHNICAL MANAGEMENT, NASA - MANNED SPACECRAFT CENTER

INSTRUMENTATION AND ELECTRONICS SYSTEMS DIVISION, F. E. EASTMAN

STATIC POWER DIVISION
BIOMETRICS INSTRUMENT CORP.
1600 DALLAS NORTH PARKWAY,
PLANO, TEXAS 75074

TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

SUMMARY

This document is the final report covering work performed in the study of state-of-the-art static inverter designs under Contract NAS9-5580. This report covers the time from January 6, 1966, to June 6, 1966.

It presents the research of the state-of-the-art inverter designs and the selection of a design approach to fulfill the objective for the proposed inverter. As part of this report the recommended design is analyzed, the primary circuit is developed, and recommendations for design objectives and design requirements are made.

I. INTRODUCTION

In aircraft, satellite, or spacecraft applications the source of power is generally derived from some DC source such as a battery or fuel cell. This raw DC power must be conditioned by static inverters and/or static converters to a useable form before it reaches the utilizing equipment.

Since the utilizing equipment may consist of radar, altitude control, communication and other life support or operation equipment, the inverter or converter must be most reliable. Also these units must have an efficiency as high as possible, while keeping their weight as light as practical. These objectives (reliability, efficiency, weight) may be specified but, in general, the specified values are minimum quantities and it is desirable that they be exceeded whenever possible.

In the design of an inverter the approach chosen has a direct bearing on each of the above design objectives, as well as on the ability of the inverter to meet general specification requirements. In this phase of the program, research of the state of the art in inverter design has led to development of an advanced design for a multiple-purpose inverter.

The first section of this report is devoted to the state-of-the-art study. In this study, basic inverter design concepts are reviewed. The ability of each design concept to develop an inverter which can meet the design specifications is discussed. To aid in these discussions, a simplified circuit diagram and waveshapes are illustrated for each design.

The selected design is explained in detail. Operation of the individual circuits is explained. The relationship between design requirements and circuit functions is also covered. The circuit is analyzed and basic circuit components are selected. The waveforms of this design and similar designs are compared and analyzed for optimum circuit design and component selection. The requirement of "switching-speed-of-transistors vs. frequency-of-operation-for -transformer-and-filter-design" is discussed. Preliminary quantative reliability analysis is made to weigh redundancy considerations. Other reliability considerations are also discussed.

The preliminary circuit diagram and a proposed bill of material is developed. To establish system performance and physical characteristics, a detailed loss, or efficiency-and-weight, study is made. The possible design configuration is outlined for evaluation.

Design specifications are reviewed and recommendations made for the final design. These recommendations are made on a basis of possible trade-offs between various performance parameters and design goals.

II. STATE-OF-THE-ART STUDY

A. INTRODUCTION

The main purpose of the study phase of this program has been to search the state of the art in inverter design for a design that can produce an inverter to meet the design requirements of the proposed multiple-purpose inverter. Many excellent designs have been used often to produce a number of well-engineered inverters. Since most of these basic designs have been analyzed at different times in detail, only a brief description of the circuit of each and its major disadvantage is given. This report cannot be considered complete in that rapidly advancing state of the art in design and components brings about new concepts continually. It is the intent of this report to include those designs considered feasible at this time.

The basic function of an inverter is to transform input DC power to usable AC power of the correct voltage and frequency. This transformation requires two basic functions in the inverter: (1) a switching device to convert the DC voltage to an AC voltage; and (2) a scaling device, such as a transformer, to convert the AC voltage to the proper level.

Most solid-state inverters are designed around two basic types of switching devices; i.e., a power transistor and a silicon-controlled rectifier (SCR). The SCR, in general, has a much higher voltage range than the transistor; however, the SCR suffers from two basic problems -- turnOFF control and switching speed. In most inverter designs the SCRs must be forced to turn OFF, thus they require more circuits than transistor designs. The transistor, in turn, has lower current-carrying ability and requires more drive power than the SCR. For the expected power level and operating conditions, the transistor is considered the best device for this application. Thus, the various circuits are explained on the basis of using power transistors for the major switching devices. Most of these circuits would work equally well, however, using SCRs and with only slight circuit modifications.

The transformer (which scales the voltage) and the filter (which shapes the voltage) together form the major weight-determining elements in an inverter.

The transformer is not only used to scale the output voltage, but is also utilized to isolate various DC and AC circuits -- a prime requirement of many systems.

Inductors and capacitors utilized in the output filter for waveshaping are also used in various input filter configurations to form AC impedance barriers between the DC power source and the inverter. Since these items make up a large part of the inverter weight, it is of paramount importance that their use be kept to a minimum. Filtering can be reduced through linear operation of the transistor; however, losses are prohibitive in most power inverter applications. Investigation of the various inverter designs attempted to evaluate such problems in conjunction with the overall design requirements.

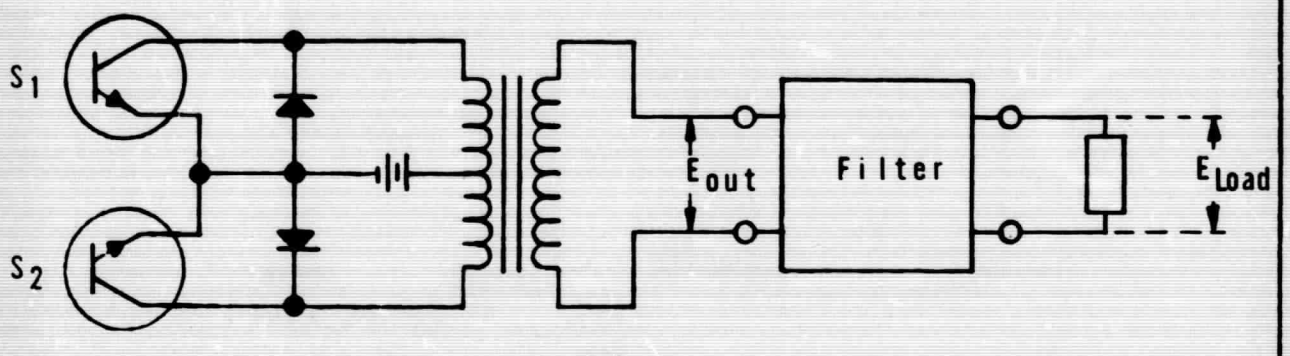
B. DISCUSSION OF INVERTER TYPES

This discussion of inverter designs covers not only the more complex state-of-the-art designs but also the simpler basic designs. The simpler designs are used as an introduction to the more complex designs. Discussion of the simpler circuit is held to a minimum since these circuits have been studied in previous reports and are well known to the industry. Circuits discussed:

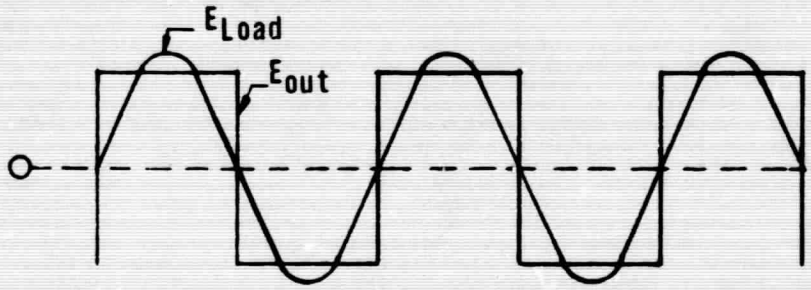
1. PARALLEL INVERTER
2. CHOPPER REGULATED PARALLEL INVERTER
3. PULSE-WIDTH REGULATED PARALLEL INVERTER
4. SERIES CONNECTED PARALLEL INVERTER
5. BRIDGE INVERTER
6. STEP-WAVE INVERTER
7. HIGH-FREQUENCY STEP-WAVE INVERTER
8. HIGH-FREQUENCY DC-DC CONVERTER-INVERTER
9. PULSE-WIDTH MODULATED INVERTER
10. PHASE-DEMODULATED INVERTER

1. Parallel Inverter (Figure 1)

The first design to be considered and one of the most basic designs is the parallel inverter. The schematic for this circuit is illustrated in Figure 1a. The main switching elements are power transistors S1 and S2. These transistors are operated as switches; i.e., they are either OFF or ON, and are operated in a



(a)



(b)

FIGURE 1
PARALLEL INVERTER

push-pull mode. This process produces a squarewave voltage (E_{out}) as illustrated in Figure 1b. This squarewave voltage is filtered to produce a low-distorted sine wave, also illustrated in Figure 1b. The filter requirements are determined by the maximum harmonic of this waveform - approximately 48 percent.

2. Chopper Regulated Parallel Inverter (Figure 2)

To be of use, the output voltage must be regulated by some means because a change in input DC voltage or load causes a change in the output AC voltage. One method of achieving this is to regulate the input DC voltage before it goes to the inverter. This regulation can be accomplished by using a series regulator or a chopper regulator. Due to the excessive power dissipation of a series regulator, only the chopper regulator is discussed.

A simple chopper regulator circuit is illustrated in Figure 2a. The chopper regulator consists of OFF-ON switch-transistor S1 and an L-C filter. S1 is turned OFF and ON as a function of the output DC level. The voltage out of S1 is illustrated in Figure 2e. As the input voltage, Figure 2b, changes levels, the OFF-ON time ratio of S1 changes. Choke L, in the filter, is designed for a minimum load current and a maximum OFF time of transistor S1. To provide a current path for load current when the transistor is OFF, fly-back diode D1 is provided. Typical currents for the transistor and the diode are illustrated in Figures 2c and 2d.

Output regulation of the inverter is a direct function of the DC voltage out of the chopper regulator. If the inverter output must be well regulated, output of the chopper is made a function of the AC output by connecting the AC output to the regulator. Any change in the AC output is reflected as a DC error signal to the regulator which causes a change in the DC output of the chopper.

3. Pulse-Width Regulated Parallel Inverter (Figure 3)

A second method of regulation for a parallel inverter is termed pulse-width control. This type of control produces a quasi-squarewave. Output sine wave voltage E is a direct function of the width of the quasi-squarewave and can be expressed mathematically by the Fourier Series:

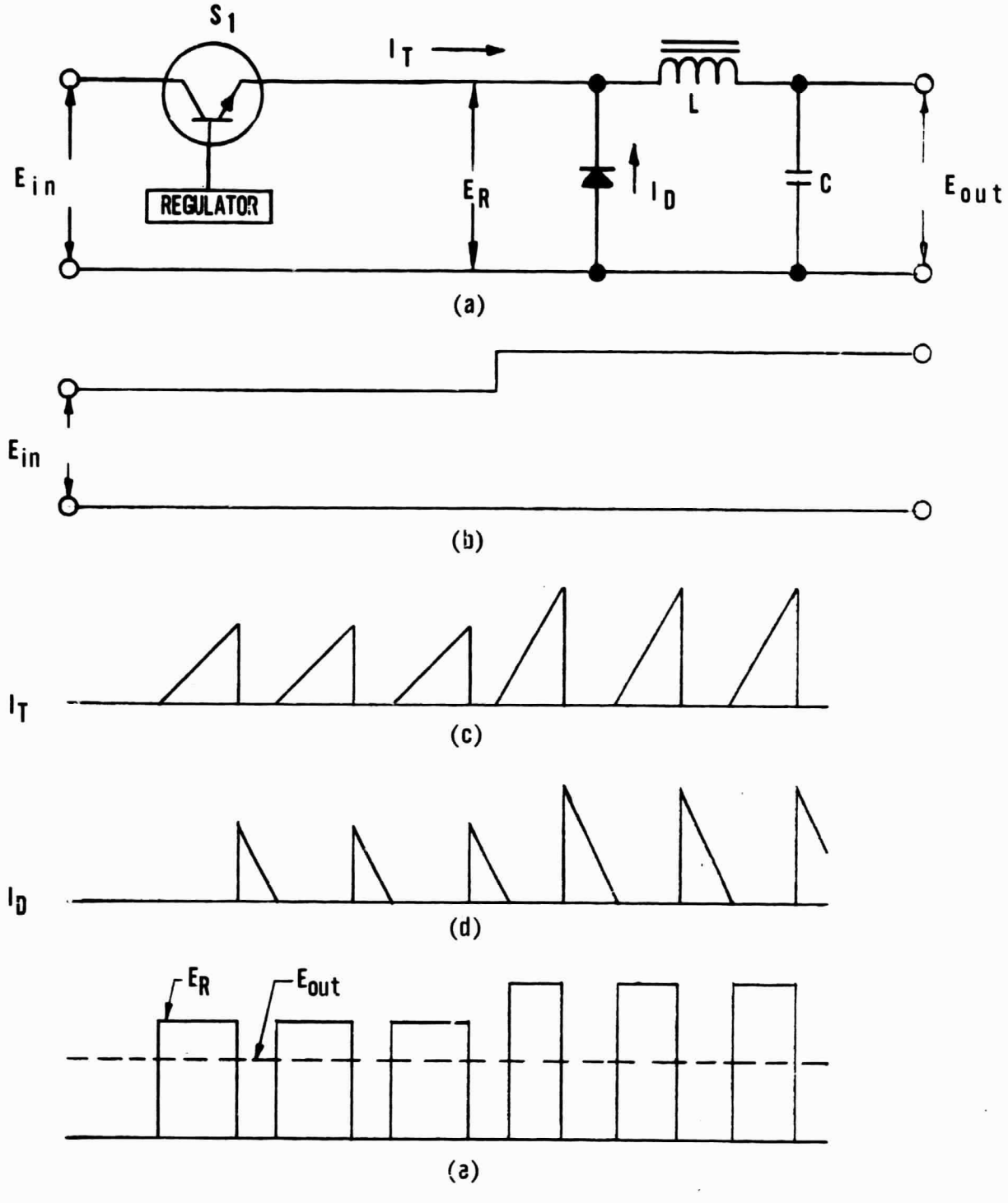
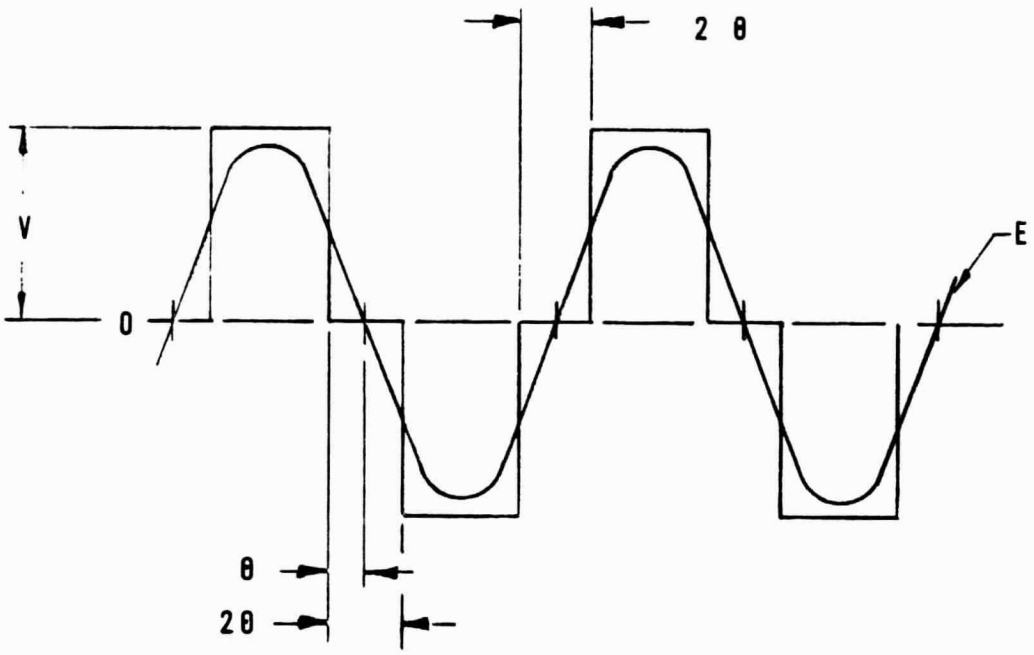


FIGURE 2
CHOPPER REGULATOR



$$E(wt) = \frac{4V}{\pi} (\text{SIN } wt \text{ COS } \theta - 1/3 \text{ SIN } 3wt \text{ COS } \theta + 1/5 \text{ SIN } 5wt \text{ COS } 5\theta - 1/7 \text{ SIN } 7wt \text{ COS } 7\theta + 1/9 \text{ SIN } 9wt \text{ COS } 9\theta \text{ ----------})$$

FIGURE 3
QUASI-SQUARE WAVE
VOLTAGE WAVEFORM

$$E(\omega_t) = \frac{4\,V}{\pi}\left(\sin \omega_t \cos \theta - \frac{1}{3} \sin 3\,\omega_t \cos 3\,\theta + \frac{1}{5} \sin 5\,\omega_t \cos 5\,\theta - \frac{1}{7} \sin 7\,\omega_t \cos 7\,\theta + \frac{1}{9} \sin 9\,\omega_t \cos 9\,\theta - \text{ - - }\right).$$

Inspection of this equation shows that the function θ controls the amplitude of the harmonic voltages as well as the fundamental voltage. A plot of this equation is shown in Figure 4. As seen in the plot, as θ varies then the amount of total harmonic content varies. This variation places additional requirements on the harmonic filter because it has to be designed to handle higher voltages and to block out more of the harmonic as compared with the fundamental.

Much of the information presented on the parallel inverter is well known to the inverter field; however, it is the basic design for almost all inverters and a general discussion of its operation is prerequisite to the later design discussions. This discussion of the parallel inverter should not be considered complete, however, in any way since many of the basic design problems, such as reactive currents, are not covered at all.

The basic disadvantage of the parallel inverter is the weight of the transformer and filter. For this reason this basic approach in itself is not given further consideration.

4. Series Connected Parallel Inverter (Figure 5)

A second basic design to be considered is the series connected parallel inverter. The basic schematic for this design is illustrated in Figure 5a. Inspection of this schematic shows it to be two parallel inverters connected in series, just as the name implies. Output voltage E_1 of the first inverter is considered to be the reference for the second inverter. By phase shifting output voltage E_2 of the second inverter and adding it to the first inverter, a quasi-squarewave voltage is developed. The advantage of this design is that it offers a low impedance current path for current flow when there is no voltage. In the

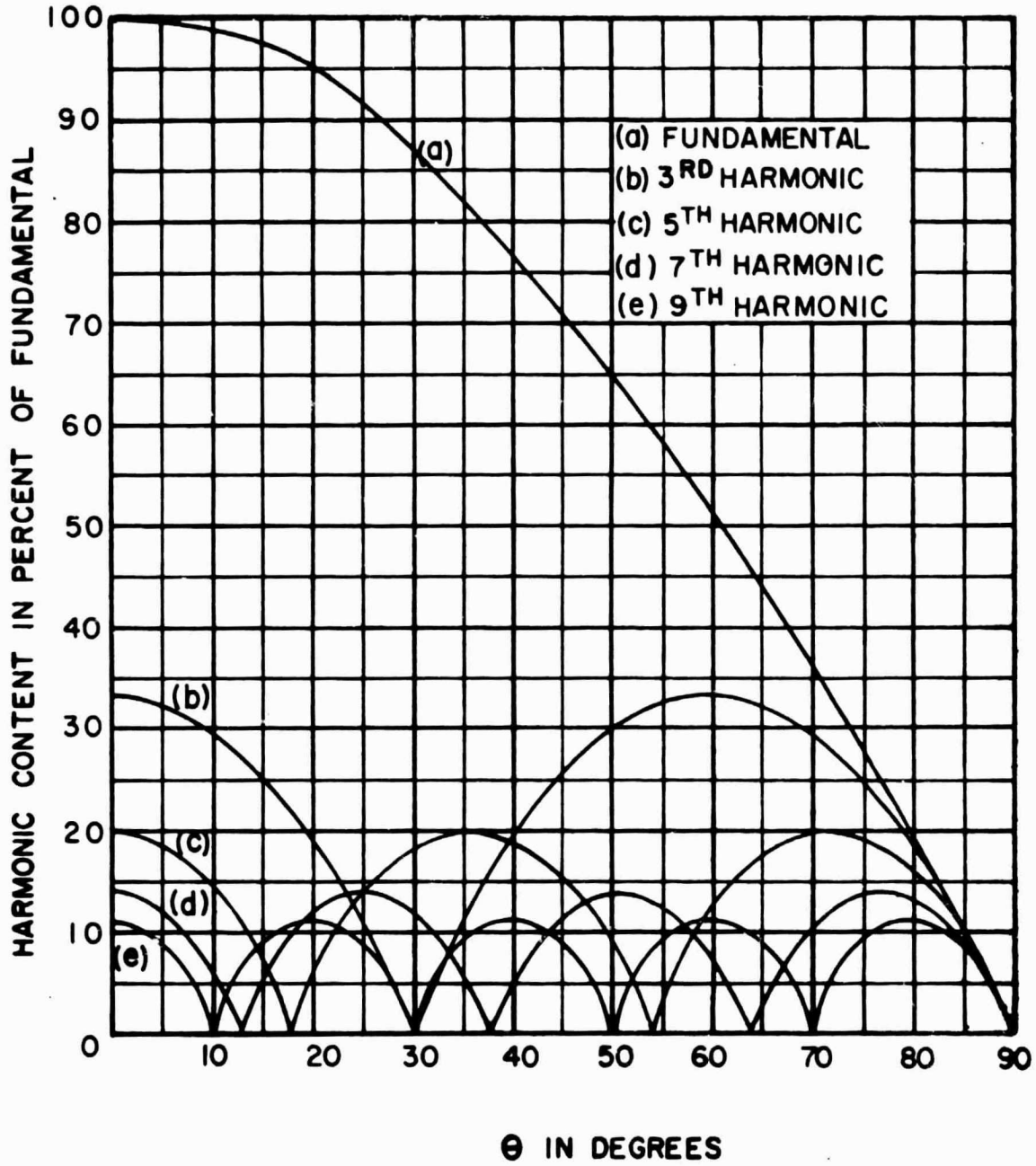
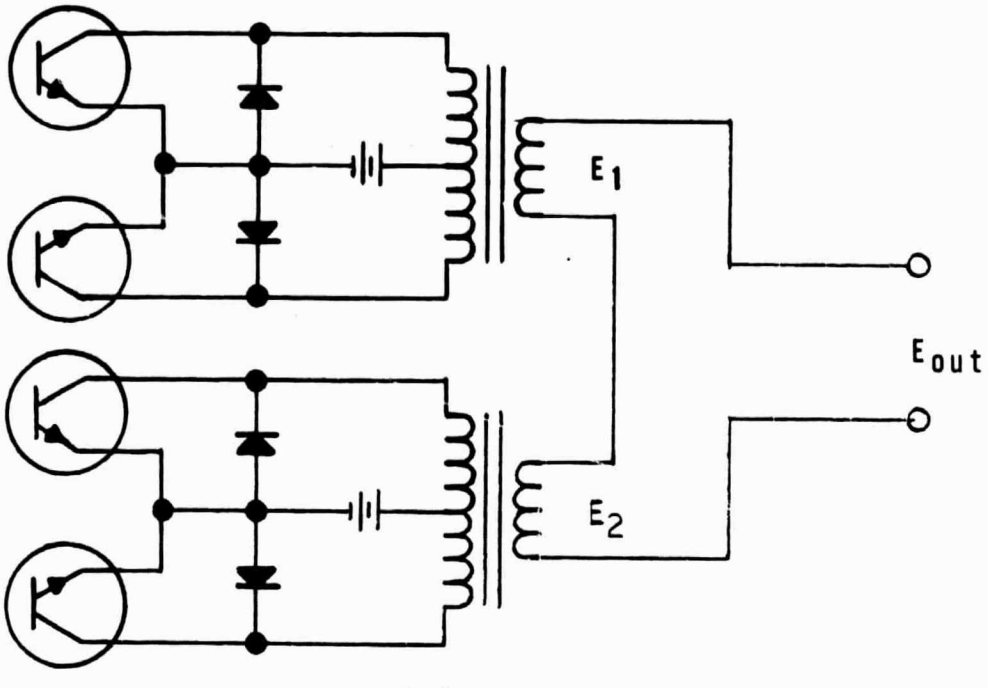
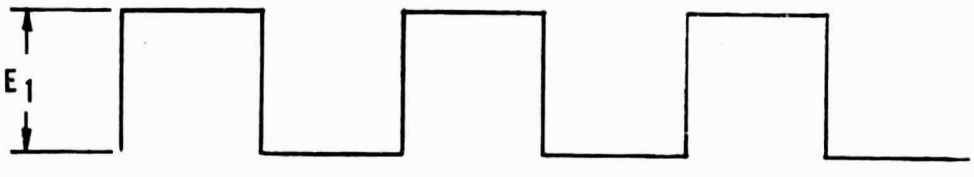


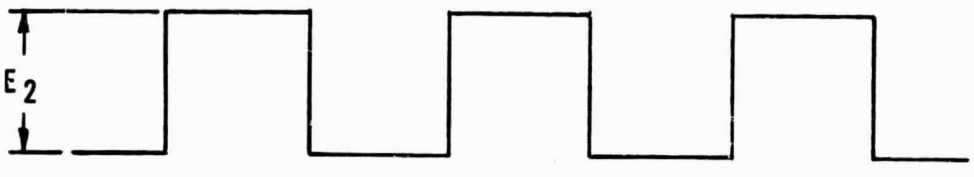
FIGURE 4
HARMONIC DISTRIBUTION



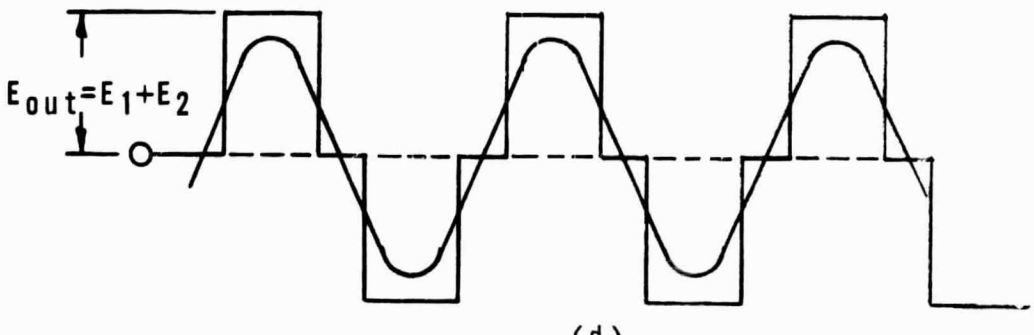
(a)



(b)



(c)



(d)

FIGURE 5
SERIES-CONNECTED
PARALLEL INVERTER

quasi-squarewave parallel inverter this presents a problem and causes additional problems for the filter. Although the low impedance of this circuit reduces the filter size, it makes poor utilization of the power transformer and power transistors. The increased size and weight of the power transformer more than makes up for the reduced filter weight, thus ruling out use of this design.

5. Bridge Inverter (Figure 6)

A design which overcomes the disadvantage of transformer size and still has a low impedance source is the bridge inverter. (Design schematic, Figure 6a.) The voltage waveforms of Figure 6b and 6c illustrate the output of two drive transformers used to drive power transistors S1 through S4. When the voltage of Figure 6b is positive, transistor S1 is ON and S2 is OFF, when it is negative, S2 is ON and S1 is OFF. When the voltage illustrated in Figure 6c is positive, S3 is ON and S4 is OFF; when it is negative, S4 is ON and S3 is OFF.

The output waveform, Figure 6d, may now be developed through the use of the switching action of the transistors shown in Figure 6b and 6c. During the first time period, T_1, transistors S1 and S4 are ON while transistors S2 and S3 are OFF, which, in effect, shorts out the input to the transformer, providing a current through transistor S1 and diode D4 or transistor S4 and diode D1. At time period T_2, transistor S3 turns ON while transistor S4 turns OFF, connecting the transformer to the battery through transistors S1 and S3, and producing the output voltage as illustrated. During time period T_3, transistors S2 and S3 are ON while S1 and S4 are OFF, again shorting out the primary of the transformer. During time period T_4, transistor S2 and S4 are ON, placing the battery across the transformer but with an opposite polarity from that experienced during time period T_2.

This approach is much better than the previous designs; however, it does not provide any major weight advantage since the transformer must carry fundamental voltage. The major disadvantage is that each time a set of power transistors switch conduction states, a short circuit is placed across the input power source. A second disadvantage is the requirement of two transistors in series, thus increasing overall losses. This design is very good, but will not fulfill requirements of the proposed inverter.

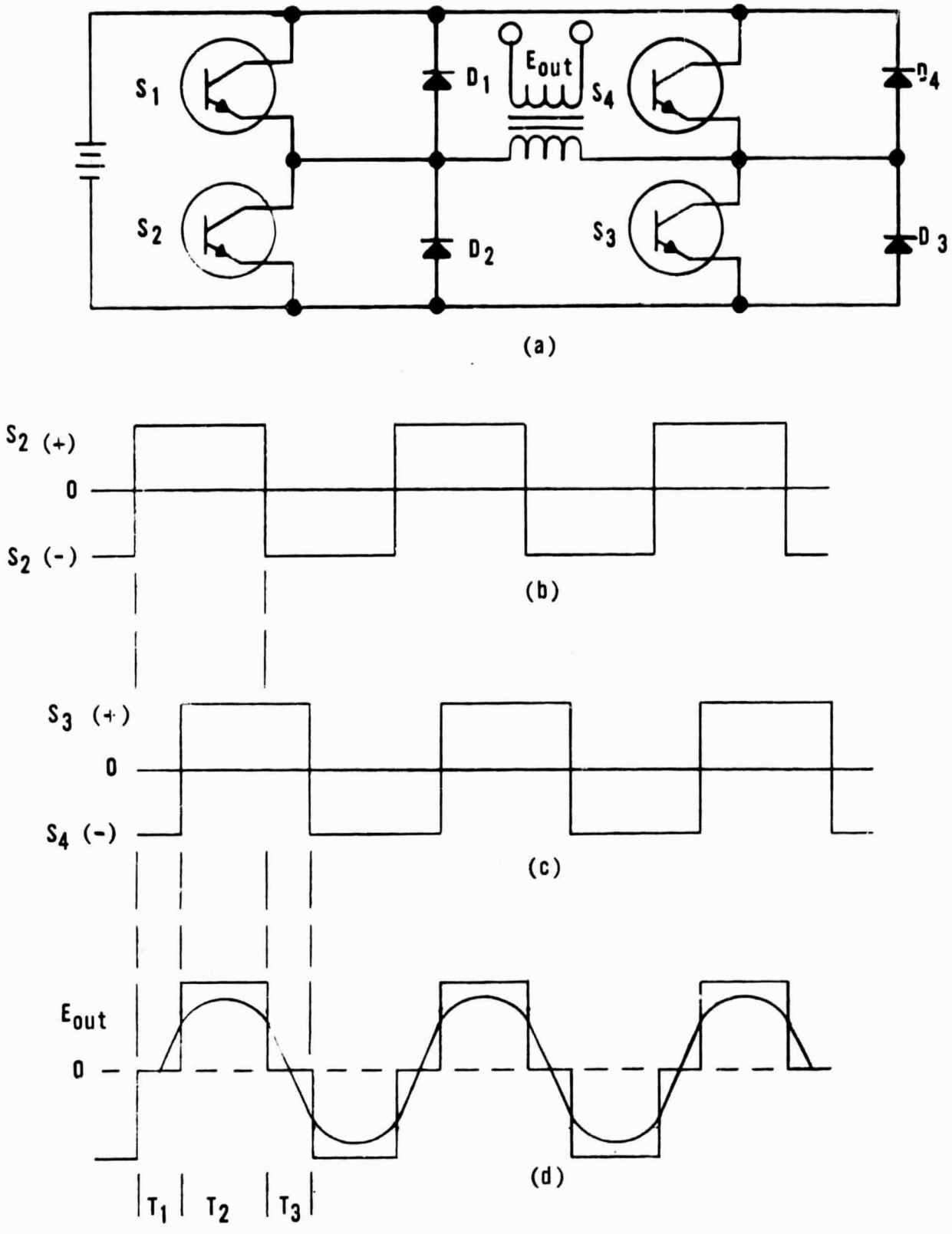


FIGURE 6
BRIDGE INVERTER

6. Step-Wave Inverter (Figure 7)

The step-wave inverter is the first design to offer a major advantage over the previous designs. For the purpose of discussion the simplest type of step-wave inverter is used. A schematic of this design is illustrated in Figure 7a. In this circuit the power transformer primary is tapped to provide intermediate levels of output voltage. Illustrated in Figure 7f is the output voltage before and after filtering, termed a six-step equal-time equal-height step-wave output with a total fundamental value of 1.35 E, and a total harmonic content of 31 percent of the fundamental. This simple design used for discussion does not provide minimum distortion vs. number of steps, however.

The output of the parallel inverter illustrated in Figure 1b is considered a two-step equal-time output. The value of the fundamental for this wave is 0.9 E and total harmonic content is 48 percent. Thus, by varying the number of steps, the value of the harmonic can be varied. If the height of the steps is varied, distortion is also varied. The height of the steps is not difficult to change since it requires only a change in the transformer turns ratio. The more steps taken, however, the more complex the control circuit becomes. Thus, as the number of steps is increased to reduce the filter requirement, the control circuit becomes more complex. In the large power unit where the control circuit weight and size is small, compared with the power stage, more steps can be taken with a greater advantage than in smaller VA units.

Table I lists a few of the basic step-wave designs with the approximate total harmonic content as a percent of the fundamental voltage. Inspection of this table shows that as the number of steps are increased, the total distortion decreases. The biggest drop in distortion is between the two-step and the six-step waveform. It is also noted that there is an optimum harmonic content depending upon the step width and step height chosen.

This type design has the advantage of a lightweight filter, but the power transformer must still carry the fundamental output voltage. A second disadvantage is no direct means of control of the output voltage. The output is generally controlled by a chopper regulator on the input as previously discussed.

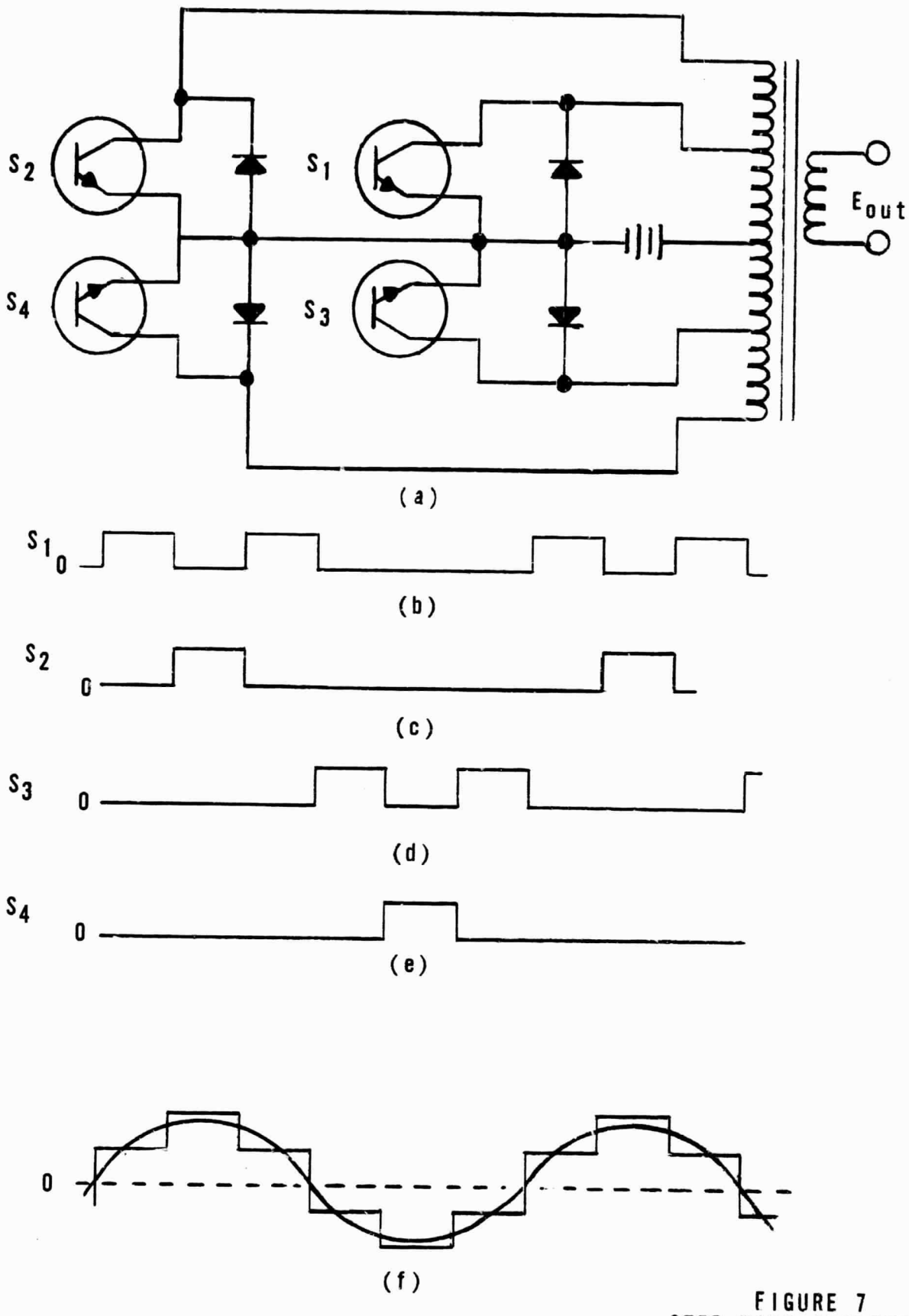


FIGURE 7
STEP-WAVE INVERTER

TABLE I

STEP-WAVE OUTPUT STEPS VS DISTORTION

WAVE TYPE	% TOTAL DISTORTION
TWO STEP-EQUAL TIME	48.
FOUR STEP-EQUAL TIME	48.
FOUR STEP-UNEQUAL TIME -1	31.
FOUR STEP-UNEQUAL TIME -11	29.
SIX STEP-EQUAL TIME-EQUAL HEIGHT	31.
SIX STEP-UNEQUAL TIME-UNEQUAL HEIGHT	23.
EIGHT STEP-EQUAL TIME-UNEQUAL HEIGHT	23.
EIGHT STEP-UNEQUAL TIME-EQUAL HEIGHT	17.
EIGHT STEP-UNEQUAL TIME-UNEQUAL HEIGHT	18.
TEN STEP-UNEQUAL TIME-UNEQUAL HEIGHT	15.
TWELVE STEP-EQUAL TIME-UNEQUAL HEIGHT	15.
TWELVE STEP-UNEQUAL TIME-UNEQUAL HEIGHT	12.
SIXTEEN STEP-UNEQUAL TIME-UNEQUAL HEIGHT	10.
EIGHTEEN STEP-EQUAL TIME-UNEQUAL HEIGHT	10.

7. High-Frequency Step-Wave Inverter (Figure 8)

The high-frequency step-wave inverter is a further improvement of the basic concept of the step-wave inverter.

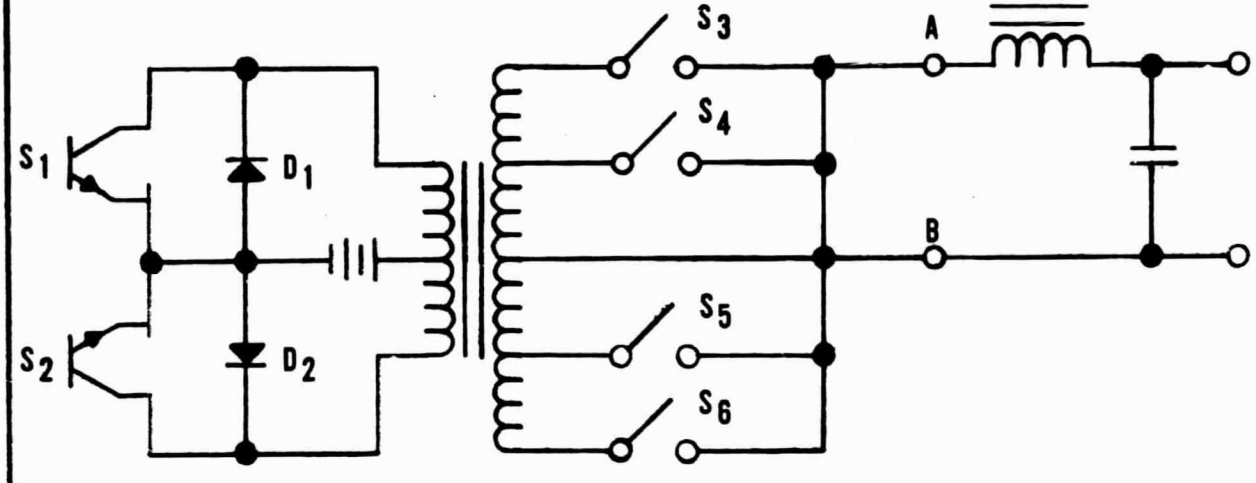
The high-frequency step-wave inverter reduces not only filter requirements by waveshaping, but reduces transformer size through the use of a high-frequency power stage. A simplified schematic is presented in Figure 8a.

Comparison of Figure 8a with 7a shows that the basic stepping switches have been moved from the primary of the power transformer to the secondary. The power stage consists of a standard parallel inverter operating at some predetermined high-frequency switching rate. Its frequency is determined by the number of steps and is some multiple of the output frequency. The voltage out of this type inverter is a squarewave (Figure 8c) and for the purpose of discussion is 2800 cycles.

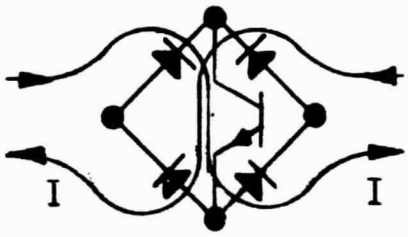
The output is stepped or steered by bilateral switches S3 through S6. A typical circuit diagram for a bilateral switch is shown in Figure 8b. The bilateral switch consists of four diodes and a power transistor, and allows current to flow in either direction whenever the transistor is turned ON.

The output of this inverter (Figure 8d) is easily developed by following the switching actions and time periods as illustrated.

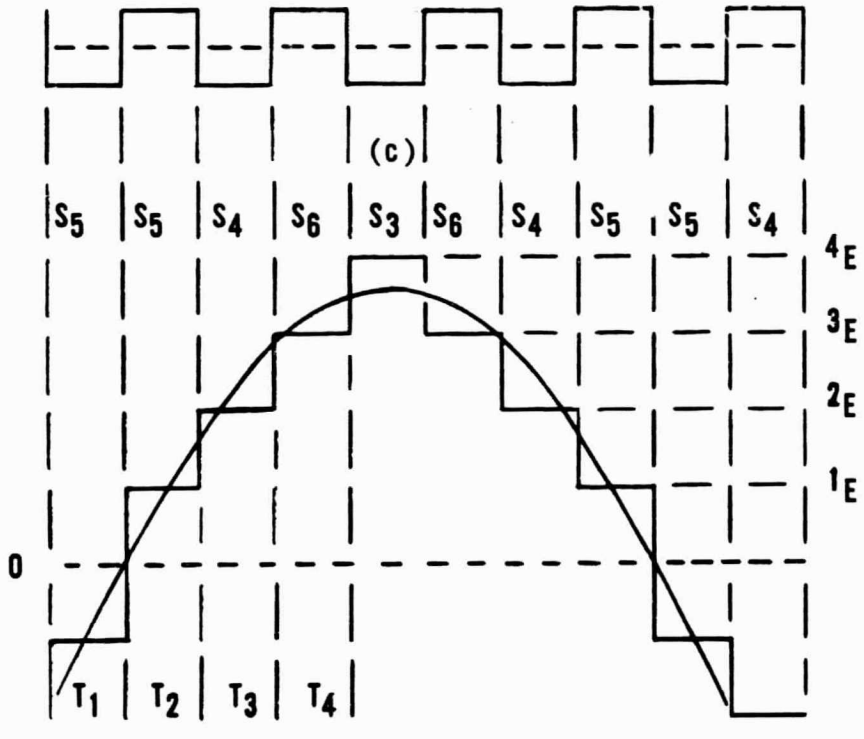
Figure 8c represents the basic polarity out of the power transformer and is used as a reference. At time period T_1, bilateral switch S5 is ON and a negative voltage is impressed at point A of the filter. At time period T_2, bilateral switch S5 is still ON, but the output of the power transformer has reversed polarity. A positive voltage is now imposed at point A of the filter. At time period T_3, the output of the transformer again reverses polarity; however, switch S5 was turned OFF and switch S4 turned ON, applying a positive voltage of 2E to point A of the filter. At time period T_4, the polarity reverses, switch S4 is turned OFF, switch S6 is turned ON, and a positive voltage of 3E is applied to point A. By continuing this process, the 14-step step-wave illustrated in Figure 8d is generated.



(a)



(b)



(d)

FIGURE 8
HIGH-FREQUENCY
STEP-WAVE INVERTER

This method not only has the advantage of low filter requirement for the output filter, but also the power transformer which does not carry the fundamental output voltage can be designed for the carrier frequency. This arrangement allows the transformer to be small, thus bringing about a further reduction in weight over the standard step-wave inverter.

Again, the disadvantage of this system is that it provides no direct method of output voltage regulation. This regulation may be accomplished, however, by use of the input chopper regulator discussed previously. A second disadvantage is the logic circuit required for correct operation of the bilateral switches. Even with these disadvantages, this design is considered to be one of the better designs for a low-weight inverter. It has one major advantage over many other high-frequency type inverters -- a low output impedance; that is, it allows current flow from the load back into the primary.

8. High-Frequency DC-DC Converter-Inverter (Figure 9)

The high-frequency DC-DC converter-inverter is basically a DC-DC converter with an inverter attached to its output. The converter output is double ended; that is, it has a positive and a negative output with a common ground. The converter is followed by an inverter stage which converts the high-voltage DC to the proper AC voltage and frequency. The circuit for this design is shown in Figure 9a. If the inverter is of the self-regulating quasi-squarewave type, then the converter output can be unregulated. If the inverter has a square-wave output or if it has a fixed output phase angle (θ), then the converter output must be regulated. Figure 9b shows the high-frequency voltage waveform of the converter power stage. Figure 9c shows the inverter output with a fixed phase angle, before and after filtering.

This approach offers a design advantage in that the converter can be operated at an optimum high-frequency, thus reducing the power transformer weight. The converter frequency can be selected independent of the output frequency. The self-regulating type inverter is less complex than the fixed output type inverter because the converter does not require a preregulator; however, the fixed output inverter may be designed with a phase angle fixed for

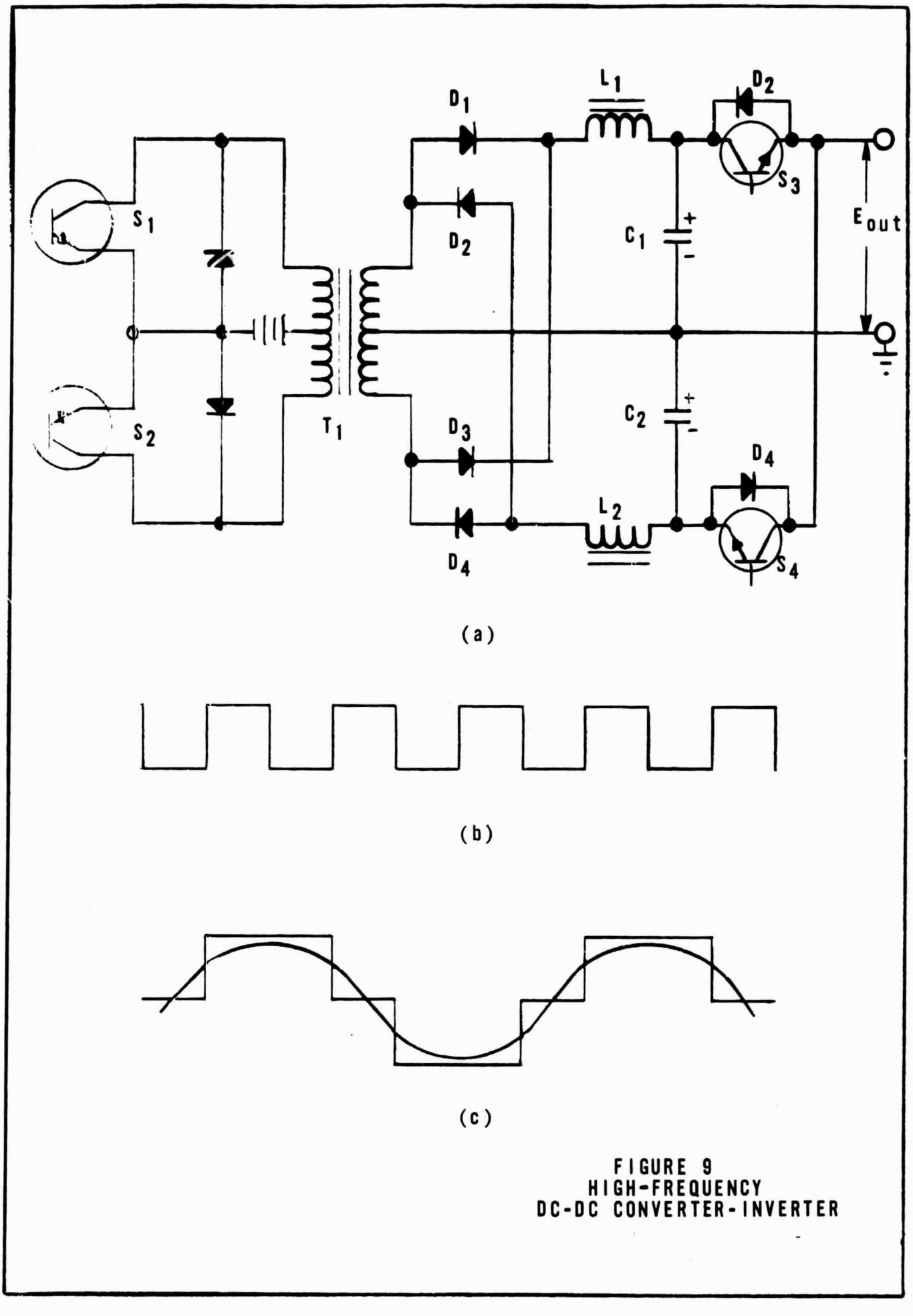


FIGURE 9
HIGH-FREQUENCY
DC-DC CONVERTER-INVERTER

minimum distortion. The reduced inverter output filter requirements may overcome the additional weight of the DC regulator for the converter input.

The major disadvantage of this system is the DC filter requirements for the converter output. If the inverter operates into a reactive load, the DC filter capacitor must be large enough to store the reactive current to prevent the DC voltage from being modulated - the major problem area of this design.

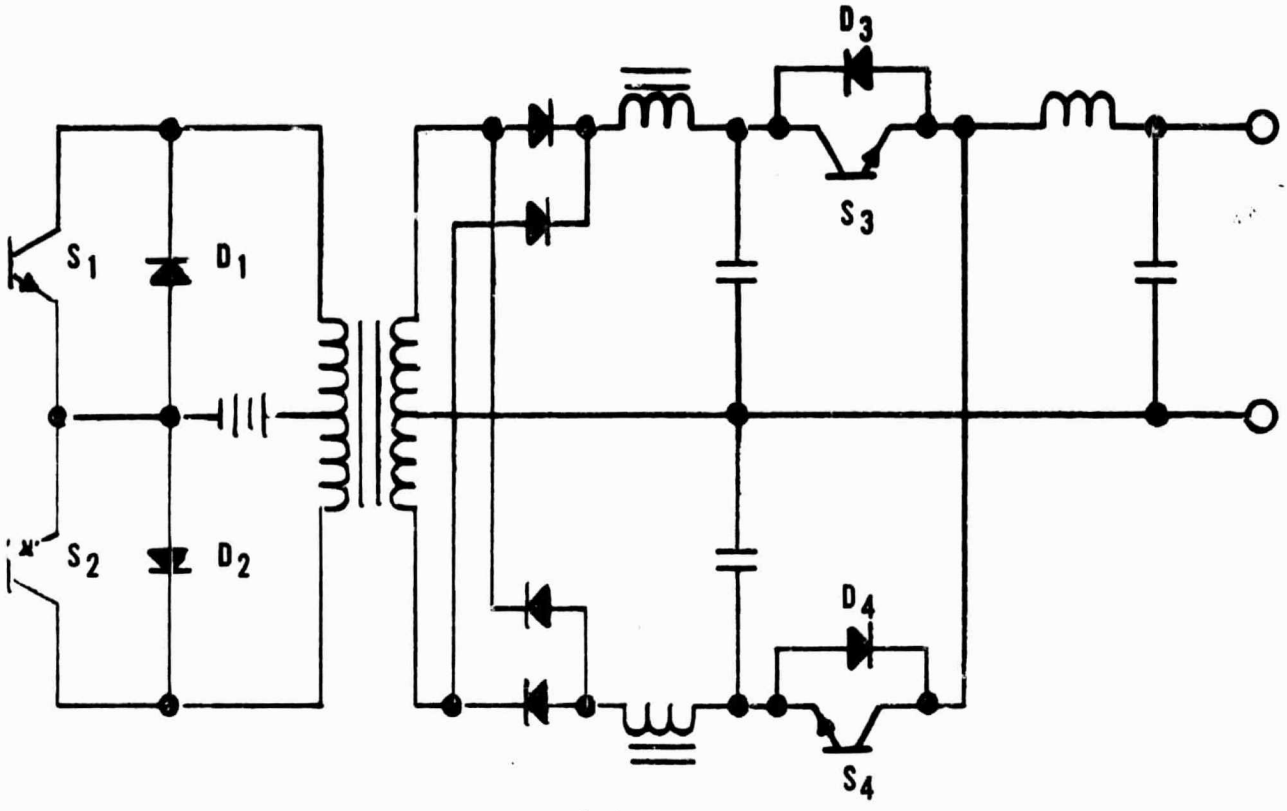
9. Pulse-Width Modulated Inverter (Figure 10)

The pulse-width modulated inverter is one of the more advanced state-of-the-art designs for inverters. This design combines the advantage of a high-frequency transformer with that of a low-pass AC output filter. The schematic for the pulse-width modulated inverter (Figure 10a) is very similar to that of the high-frequency DC-DC converter-inverter (Figure 9a). The basic difference is in how the inverter transistors (S3 and S4) are controlled.

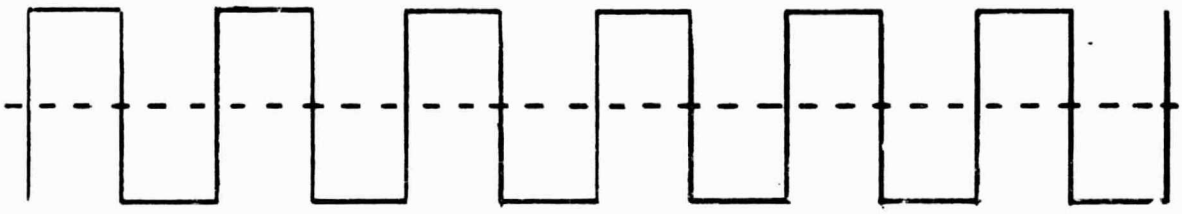
In the pulse-width modulated inverter, the inverter transistors are switched at a high frequency to produce a modulated output at the required inverter output frequency. This modulated voltage is illustrated in Figure 10c along with the output sine wave.

By using the time periods of Figure 10c and the schematic of Figure 10a, basic operation of this circuit can best be explained. The positive bus, or B+ bus, is connected to the output filter through transistor switch S3 while transistor switch S4 connects the negative bus to the output filter. When switch S3 is ON, the filter has a positive voltage applied to its input terminals. When S4 is ON, it has a negative voltage applied to its input. Transistors S3 and S4 are never ON at the same time, one is turned ON as the other is turned OFF. Transistor S4 is ON during time period T_1, producing a negative voltage at the input of the filter at point A. At time period T_2, S4 turns OFF and S3 turns ON, applying B+ to the filter. For time period T_3, S4 is again ON, while for time period T_4, S3 is ON. This switching produces a series of voltage pulses at the input of the filter.

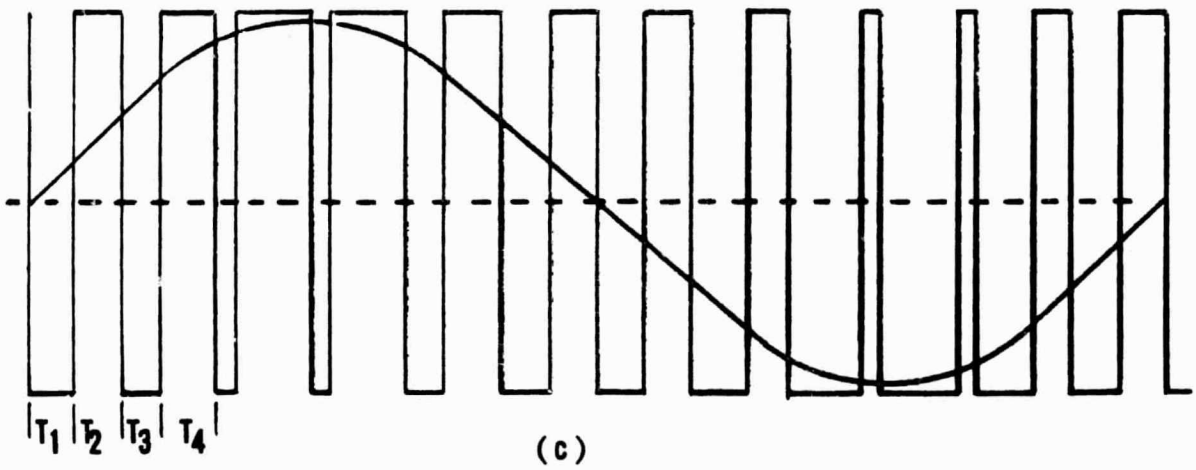
Inspection of these pulses shows that positive pulses are wider



(a)



(b)



(c)

FIGURE 10
PULSE- WIDTH
MODULATED INVERTER

than negative pulses for this group of time cycles. Further, inspection of Figure 10c shows that there is a burst of wide pulses and then a burst of negative pulses. Since the widths of the pulses are controlled as a function of a sine wave, the modulated waveform of Figure 10c produces a sine wave when passed through a low-pass filter.

Design of the filter is a function of the ratio of the high-frequency carrier to the low-frequency output. The upper limit of this ratio is limited by the switching frequency of transistor switches S3 and S4. In determining the operating frequency, some tradeoff must be made between transformer and filter size and inverter efficiency.

Output voltage amplitude and frequency are determined by the sine wave which modulates switches S3 and S4. If the sine wave is fixed, then the output may be regulated by controlling the DC input voltage.

A second more direct method of regulation is to make the modulating sine wave a direct function of the output sine wave. When there is a change in output voltage it is reflected to the sine wave reference directly, making regulation time a function of the carrier frequency and not the output frequency.

A complete description is not given for this waveform as it is covered in the main body of the report.

The basic disadvantage of this circuit is reactive current flow. The DC filters on the output of the converter must be designed to take care of the reactive current flow from the inverter. If this flow is very large, then the size and weight become increasingly larger, reducing the size and weight advantage of the design.

10. Phase-Demodulated Inverter (Figure 11)

The phase-demodulated inverter is a new and unique state-of-the-art inverter developed by Varo in early 1965. The basic design concept was tested and proved in a 200-VA variable-frequency inverter. The basic circuitry for this design is illustrated in Figure 11a. Input DC power is amplified by a square-wave parallel inverter at some high frequency predetermined by the design

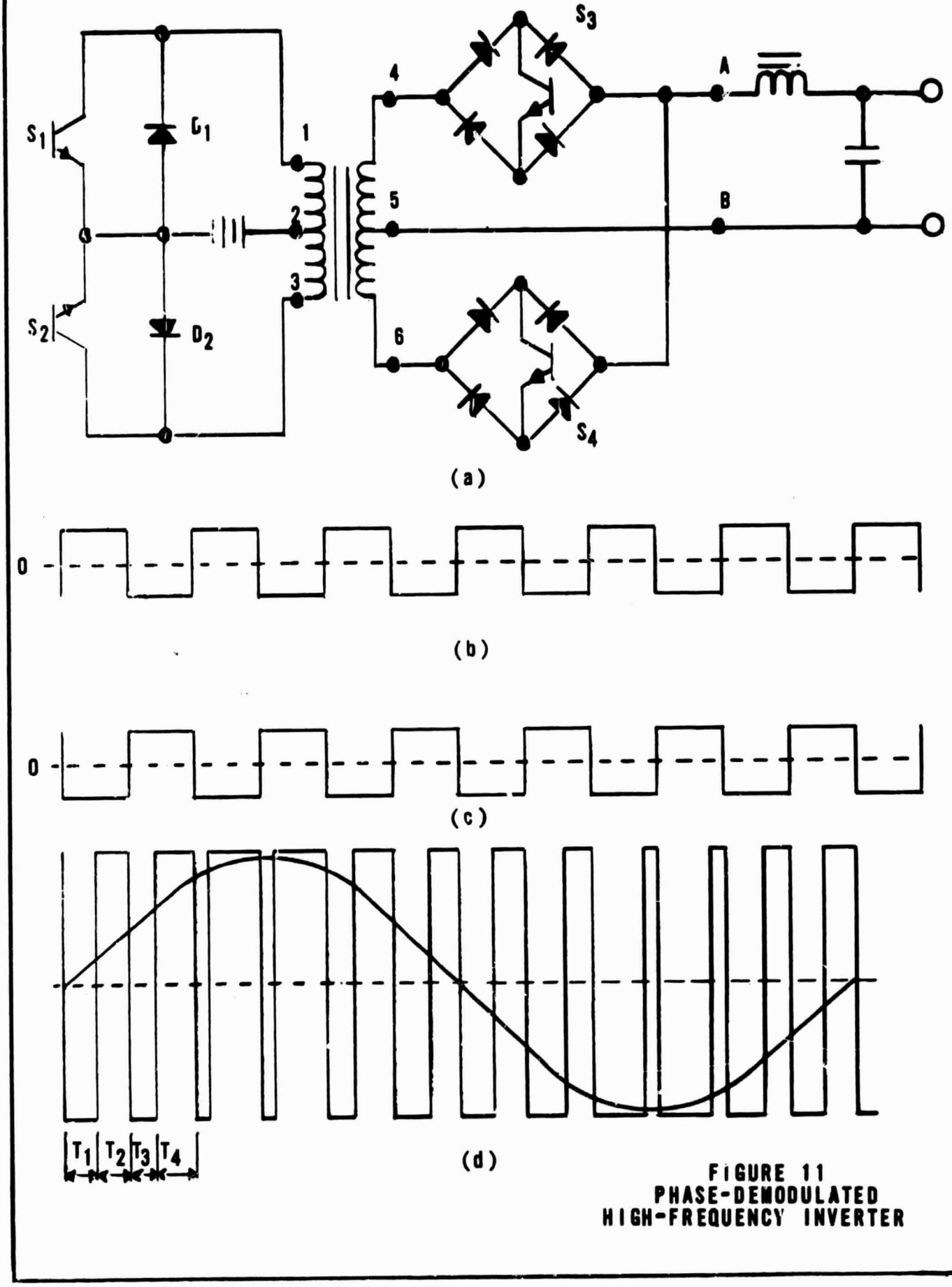


FIGURE 11
PHASE-DEMODULATED
HIGH-FREQUENCY INVERTER

requirements. The output of the power transformer is push-pull and is illustrated in Figure 11b and 11c. Figure 11b illustrates the voltage as it appears at terminals 4-5 of power transformer T_1. Figure 11c illustrates the voltage that appears at terminals 5-6 of T_1.

Terminals 4 and 6 are connected to the output filter by bilateral switches S3 and S4. By phasing the operation of switches S3 and S4 correctly, the high-frequency squarewave out of the power transformer is phase-demodulated to produce a pulse-width modulated voltage with a sine wave envelope. By the use of a simple low-pass filter, the modulated high-frequency wave is smoothed out to form a low-distorted sine wave.

The output AC voltage and frequency is controlled by varying the phase-demodulation of the high-frequency squarewave. Figures 11b, 11c, and 11d show the basic phase relationship of the power transformer output and switches S3 and S4. At time period T_1, switch S4 is ON, connecting the negative voltage of terminal 6 to point A of the filter. At time period T_2, switch S3 is turned ON and switch S4 is turned OFF, applying the positive voltage of terminal 4 to point A of the filter. At time period T_3, the power stage reverses output voltage; however, transistor S3 stays ON, applying a negative voltage to point A for time period T_3. Switches S3 and S4 again switch ON-OFF states at time period T_4, again applying a positive voltage to point A. This switching is continued to produce the pulse-width modulated voltage waveform illustrated in Figure 11d.

Output voltage and amplitude are a direct function of the modulating sine wave controlling the action of switches S3 and S4. This sine wave is an error signal developed by comparing the output voltage with a fixed sine wave reference voltage of the correct amplitude and frequency. This design provides an optimum in weight reduction since the power transformer is designed for the high-frequency carrier, the filter is of the low-pass design, and the required control circuit is not overly complex

A complete description of the operation of this circuit is provided in this report.

C. DESIGN SELECTION

All of the designs presented have innate advantages and disadvantages. Selection of the best design weighed the basic design against the operational requirements of the inverter. Since a reduction of weight and space is a primary objective of the program, the first five basic designs can be removed from consideration. This leaves the following designs to be considered:

6. STEP-WAVE INVERTER
7. HIGH-FREQUENCY STEP-WAVE INVERTER
8. HIGH-FREQUENCY DC-DC CONVERTER-INVERTER
9. PULSE-WIDTH MODULATED INVERTER
10. PHASE-DEMODULATED INVERTER

Of the five remaining designs only the step-wave inverter is of the low-frequency type inverter designs. All of the remaining four designs utilize high-frequency power amplification in some means. Since the high-frequency step-wave inverter includes the basic advantage of the step-wave inverter, the step-wave will not be given further consideration.

One additional consideration to be given is the fact that all of the high-frequency units require high-voltage transistors. This problem has become less important than it was a year ago because most major device manufacturing companies are working on high-voltage devices and rapid advancements are being made in this field.

Of the four remaining designs, a basic separation of ability and desirability may be made. Reinspection of Figure 9a and Figure 10a shows that the high-frequency DC-DC converter-inverter and the Pulse-Width Modulated Inverter have the same basic circuit diagram. The pulse-width modulated inverter has two basic advantages: lighter weight, due to less filtering, and a basic ability to be paralleled. The converter-inverter approach should prove to be more efficient since the inverter transistor switch is at a much lower frequency.

The high-frequency step-wave inverter is an excellent design, except for the input DC regulation requirement. Also, the gating circuit to step and phase lock the output switches would be more complex than desired when weighed with

the paralleling and three-phase requirements.

The Phase-Demodulated-High-Frequency Inverter is the most desirable of the designs considered. It offers a maximum weight reduction with a minimum of power and control circuitry. The output regulation is a function of the high-frequency carrier and not the output frequency. The resulting fast response allows units to be paralleled with a minimum of additional circuitry. Use of the output sine wave as part of the regulation loop provides for minimum phase shift of the output with respect to the reference, which, in turn, provides for good phase angle control when units are connected in three-phase configurations. These and many other advantages are more apparent from the detailed circuit description.

To provide a basic guide line for inverter selection, the best five designs are listed in Table II with a few of their evaluating factors. A 1-5 rating consideration was used for evaluation, where 1 is the most desirable. These ratings are provided only as a basic guide since a circuit modification could result in the re-evaluation of any of the individual ratings.

TABLE 2
INVERTER DESIGN EVALUATION

INVERTER TYPE	WEIGHTING FACTORS											
	TRANSFORMER	OUTPUT FILTER	CONTROL CIRCUIT	INTERMEDIATE DC FILTER	POWER FACTOR	EFFICIENCY	PARALLEL	THREE PHASE	COMPLEXITY	SIZE	WEIGHT	TRANSIENT RESPONSE
STEP-WAVE INVERTER	5	3	4	NA	2	1	4	4	2	5	5	5
HIGH-FREQUENCY STEP-WAVE INVERTER	2	3	5	5	1	3	3	3	4	2	2	4
HIGH-FREQUENCY DC-DC CONVERTER-INVERTER	1	5	2	5	5	3	4	4	3	4	4	5
PULSE-WIDTH MODULATED INVERTER	1	1	2	5	3	3	2	1	3	3	3	3
PHASE-DEMODULATED INVERTER	1	1	2	NA	1	2	1	1	2	1	1	1

NOTES: 1-5 RATING USED, 1 MOST DESIRABLE,
NA - NOT APPLICABLE

III. ELECTRICAL DISCUSSION

A. GENERAL CIRCUIT DESCRIPTION

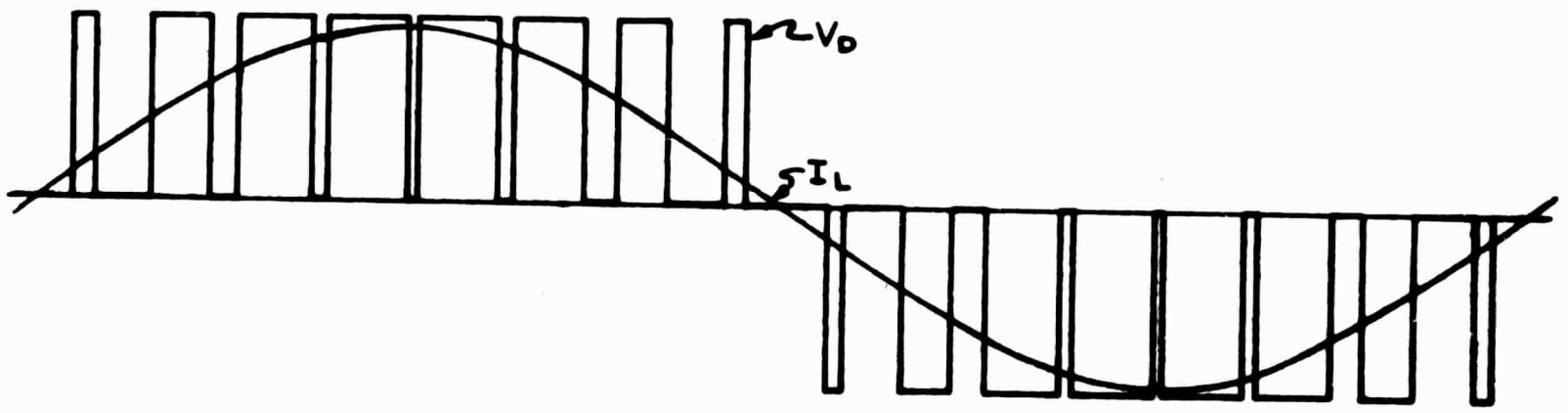
The Phase-Demodulated High-Frequency Inverter was selected not only for its general design advantages, but also for its overall versatility. This versatility is being demonstrated in several lightweight, multiple-frequency inverters being furnished to the U. S. Army Engineer Research and Development Laboratories. A list of these units is provided in Appendix B. The inverters furnished have utilized several basic design configurations, the best of which has been selected for use in the development of this inverter.

In the state-of-the-art study, only the basic Phase-Demodulated High-Frequency Inverter concept was described; however, the design to be utilized for this application is termed a Phase-Demodulated High-Frequency Bridge Inverter and has been used in the development of a 250-VA multiple-frequency inverter.

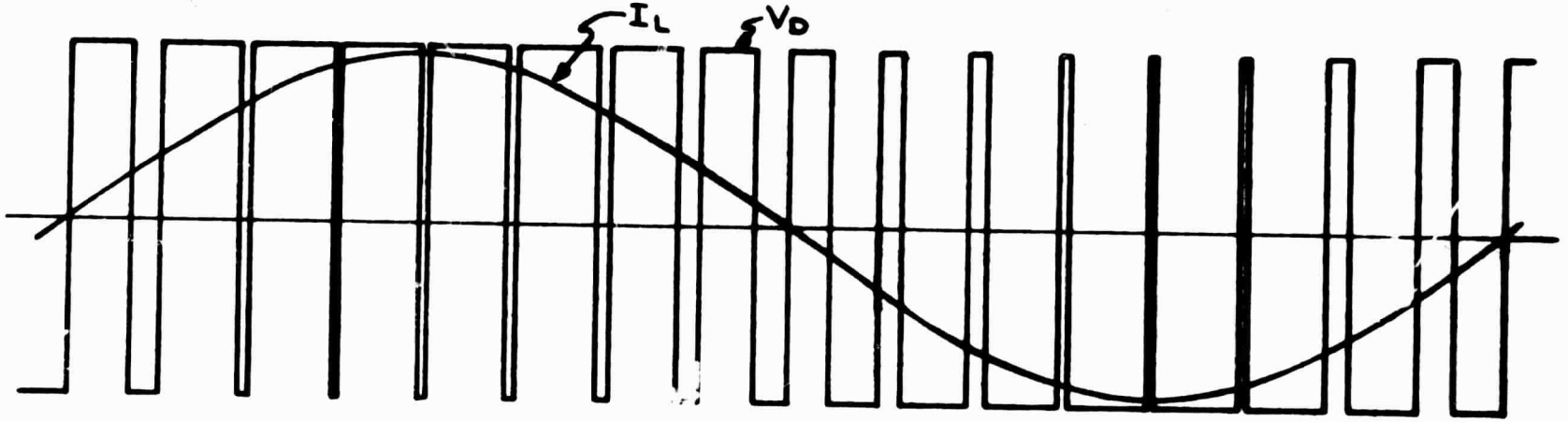
The advantage of the improved design is apparent in the comparison of output waveforms of the two designs. The output of the Phase-Demodulated High-Frequency Inverter is illustrated in Figure 12b, while the output of the improved design is illustrated in 12a. The modulated waveform of Figure 12a requires less output filtering and also results in less volt-ampere loading of the power transformer.

This improvement in design is brought about with a minimum of additional circuitry. Figure 13 is a block diagram for a Phase-Demodulated High-Frequency Inverter which fulfills the basic design requirements. Figure 14 is the block diagram for the Phase-Demodulated High-Frequency Bridge Inverter. The basic difference in the two designs is the addition of an extra reference comparator circuit and a demodulator drive circuit.

Figure 14 includes all of the basic functions for single-phase, three-phase, and parallel operation of the inverter. The connection illustrated is for single-phase operation. Blank connections F, K, and L are for three-phase and/or parallel operation which is covered in a later section. A step-by-step discussion of Figure 14 provides a good understanding of the design concept of the Phase-

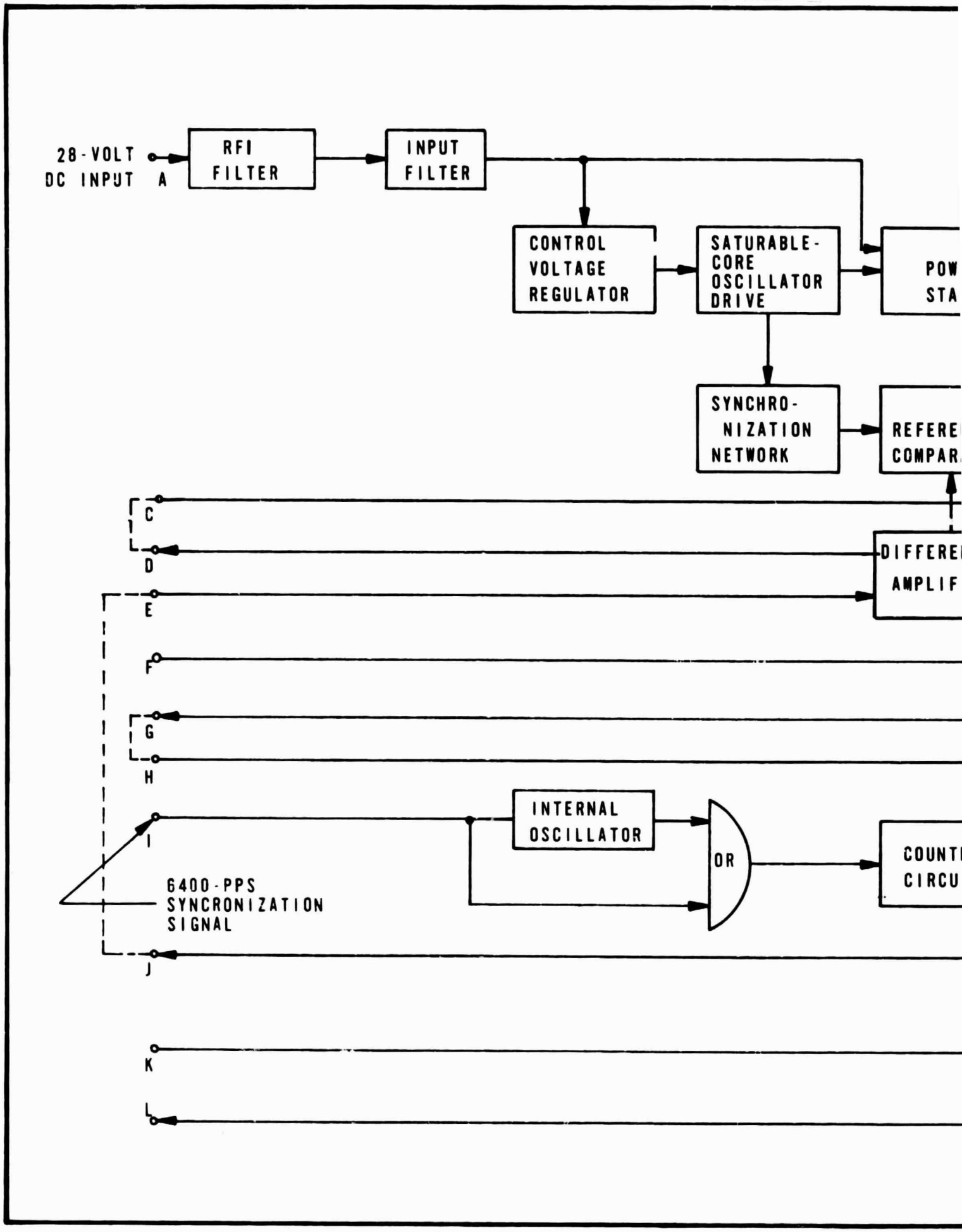


(a)



(b)

FIGURE 12
MODULATED WAVEFORMS



FOLDOUT FRAME 1

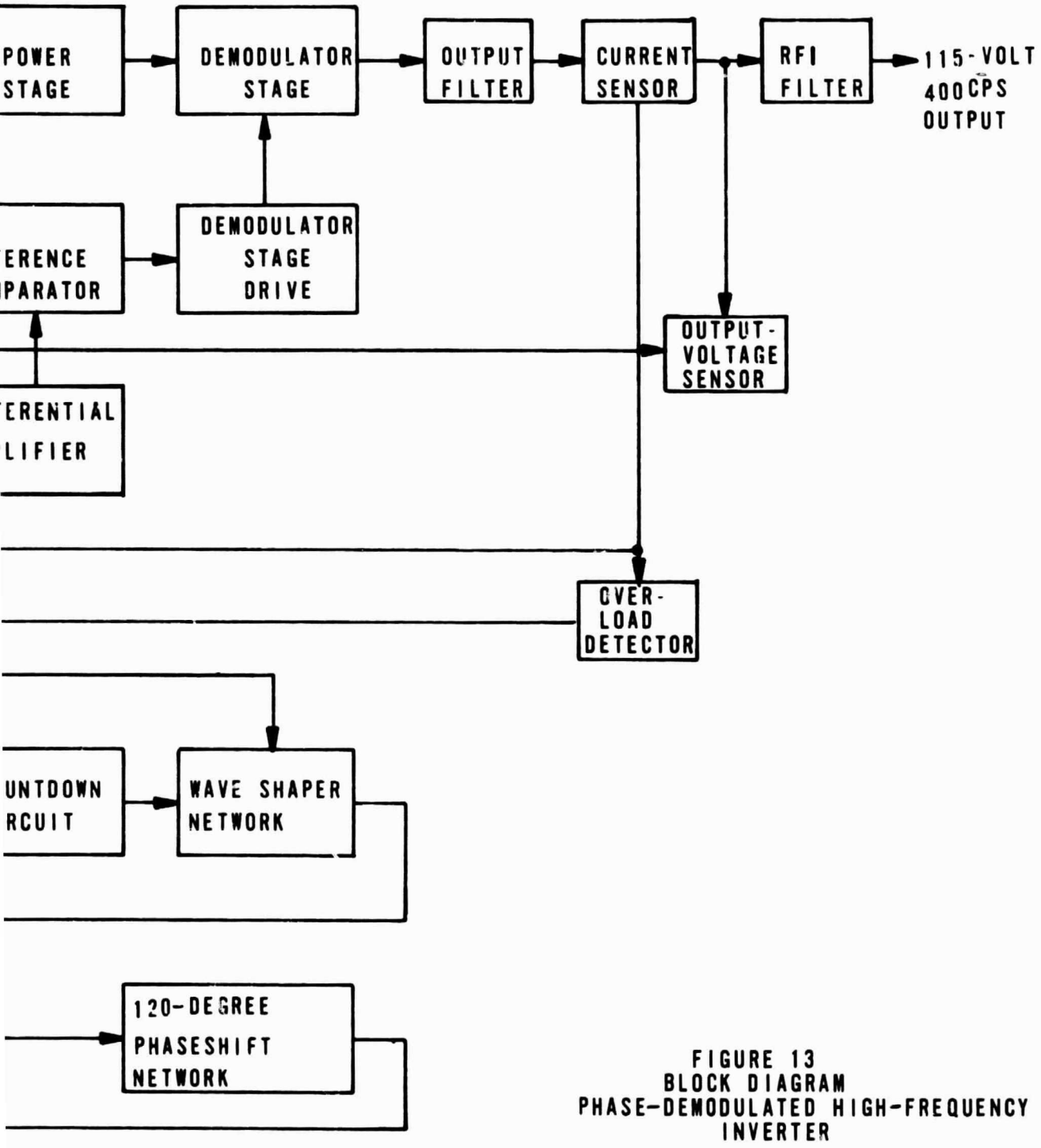
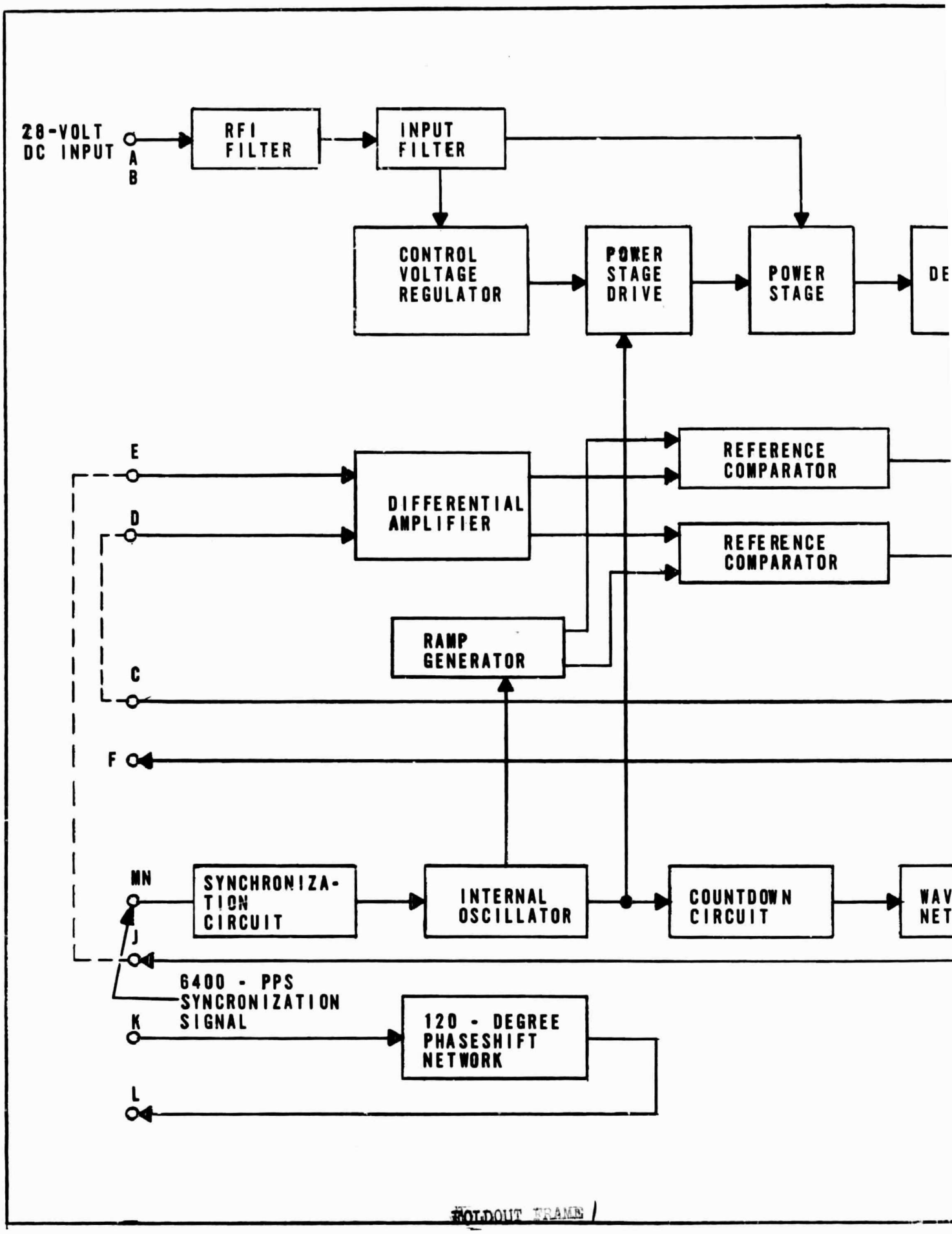


FIGURE 13
BLOCK DIAGRAM
PHASE-DEMODULATED HIGH-FREQUENCY
INVERTER



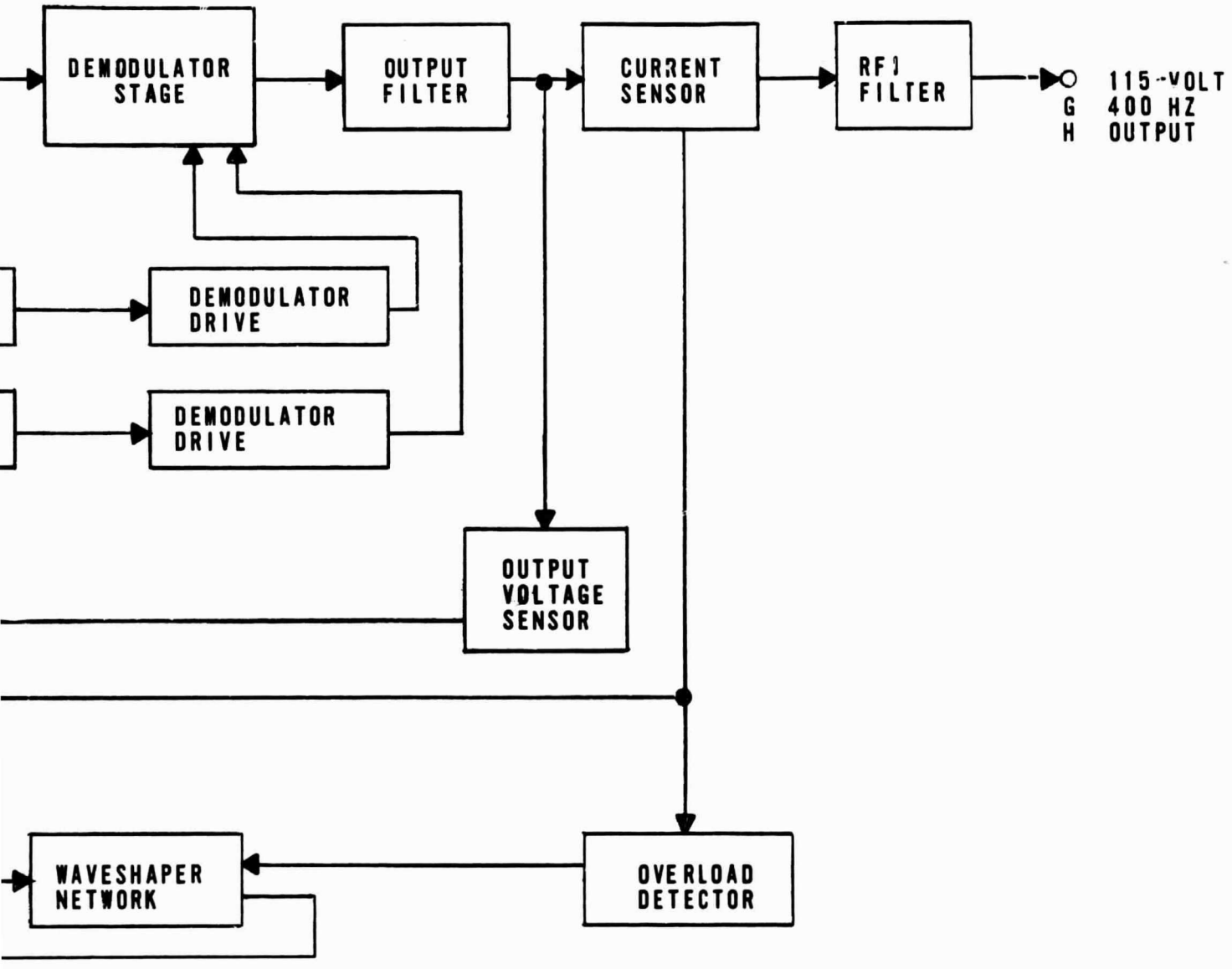


FIGURE 14
PHASE-DEMODULATED HIGH-FREQUENCY
BRIDGE INVERTER

FOLDOUT FRAME 2

Demodulated High-Frequency Bridge Inverter.

To protect the input DC line from RFI and line modulation due to the inverter, appropriate RFI and power filtering is provided. The RFI filtering is minor since the input filter suppresses RFI conduction in the input lines.

Power for the various control functions is provided by the control voltage regulator. This regulator provides all the proper level and degree of regulation.

Operation of the control functions and their relationships to the power stage and phase demodulator can best be explained through the use of waveforms illustrated in Figure 15. Figure 15a is a simplified schematic of the power stage and the demodulator, and is used to show the proper phase relationships between the various waveforms.

The 6400-Hz output of the internal oscillator is illustrated in Figure 15b. This output is frequency locked to the external signal through the synchronization circuit. The output of the oscillator provides the reference trigger for the power stage drive, the reference comparators. and the countdown circuit.

The power stage drive consists primarily of a flip-flop and several power amplifier stages. The pulse of Figure 15b triggers the flip-flop which is in turn amplified to produce the 3200-Hz push-pull drive voltage as illustrated in Figure 15c and 15d. This voltage is used to drive the power transistors illustrated as simple switches S1 and S2 in Figure 15a. Power transformer T_1 amplifies this voltage to the proper level (Figure 15h).

The 6400-Hz signal is reduced to a 400-Hz squarewave voltage by the countdown circuit. The waveshaper network is an active filter which produces a precise 400-Hz sine wave from this squarewave voltage. This differential amplifier compares the output voltage of the inverter with the sine wave reference to produce a pair of sine wave error signals. These error signals (Figures 15e and 15h) control the output of the inverter. A change in the reference voltage or the output voltage causes an opposite change in the error signal.

Also illustrated in Figures 15e and 15h is a 3200-Hz ramp waveform which represents the control voltage of the two reference comparators. These

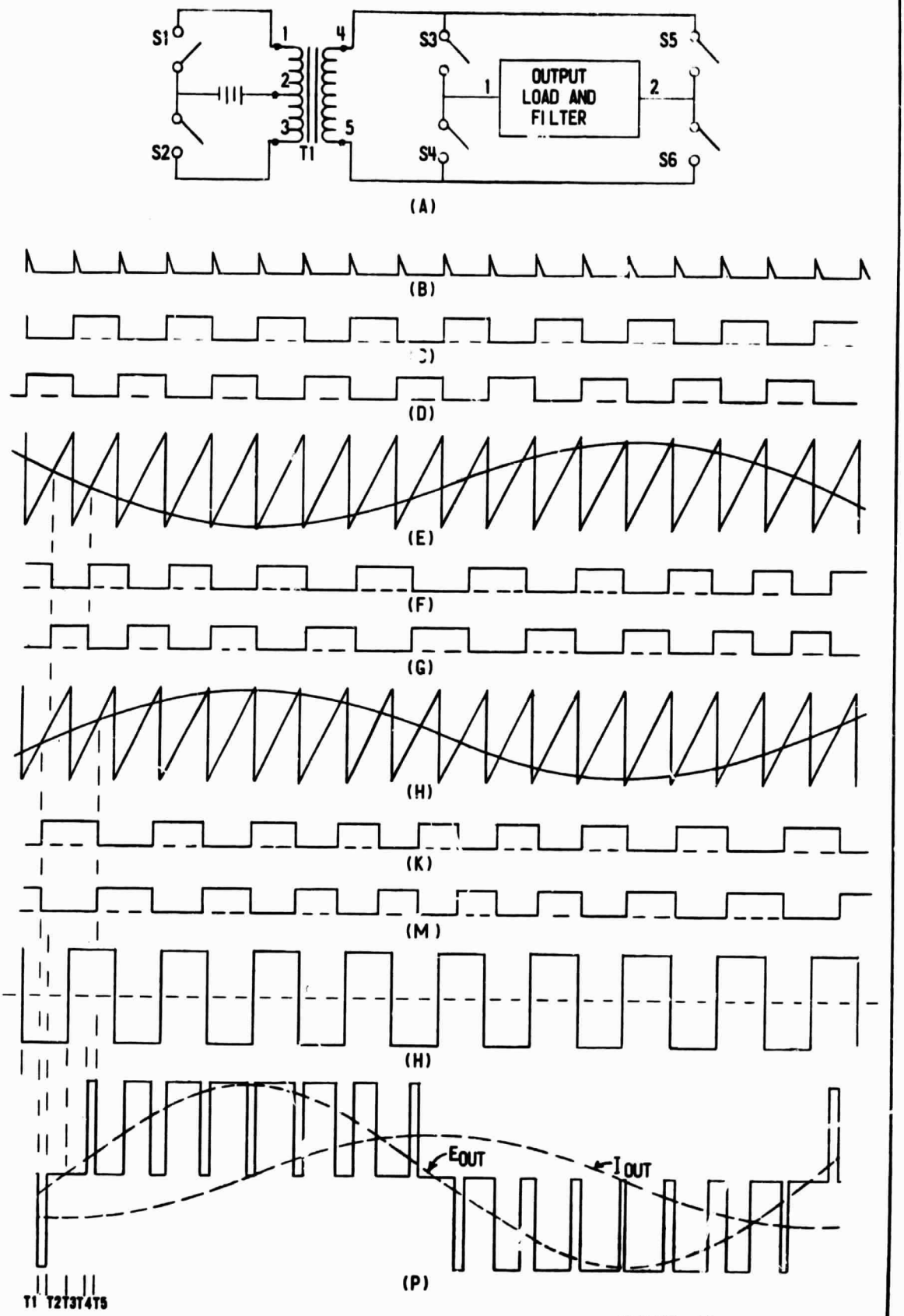


FIGURE 13
WAVEFORM DEVELOPMENT

ramp voltages are frequency and phase locked to the output of the power stage. When the sine wave of Figure 15e crosses the ramp, a pulse is generated at the output of reference comparator (A). This pulse triggers a flip-flop in the demodulator drive (A) to produce a push-pull drive signal as illustrated in Figures 15f and 15g. Signal 15f drives bilateral switch S3 while signal 15g drives bilateral switch S4. The sine wave and ramp of Figure 15h, in turn, produces the drive signals of Figures 15k and 15m. Signal 15k drives bilateral switch S6 while 15m drives bilateral switch S5.

By using the time periods illustrated in Figure 15p, the relationship between the control function is shown as the output-modulated voltage waveform is developed. At time period T_1 the sine wave signal and ramp signal of Figure 15h intersect, causing a change in the output of demodulator drive (B) which is reflected in the drive voltages shown in Figures 15k and 15m. This change in drive voltage turns switch S6 ON and switch S5 OFF, connecting terminal 2 of the output filter to terminal 5 of the power transformer. Terminal 1 of the output filter, connected to terminal 4 of the power transformer, did not change states at time period T_1. Negative output voltage, Figure 15h, is applied to the filter as shown in Figure 15p.

The next time period T_2 shows the sine wave and ramp signal of Figure 15e intersecting, causing switch S3 to turn OFF and switch S4 to turn ON. This action disconnects terminal 1 of the filter from the power transformer and connects it to terminal 2 of the filter, shorting out the input to the filter, and open circuiting the secondary of the power transformer.

At time period T_3 the output of the power transformer reverses, as illustrated in Figure 15h. Also, at this time the ramps are reset; however, there is no switching action of the demodulator switches during the resetting action. Since the demodulator did not change states, the input to the filter is still short circuited.

At time period T_4, demodulator switches S3 and S4 again reverse states: switch S3 is turned ON and switch S4 is turned OFF. This action again connects terminal 1 of the filter to terminal 4 of the transformer. The short from the

filter is removed and the positive voltage of the transformer is connected to the filter input.

By following the action of the two control ramps and their error sine waves throughout a complete cycle of the output frequency, it is seen that the modulated voltage is passed through a low-pass filter to produce the low-distorted sine wave output voltage.

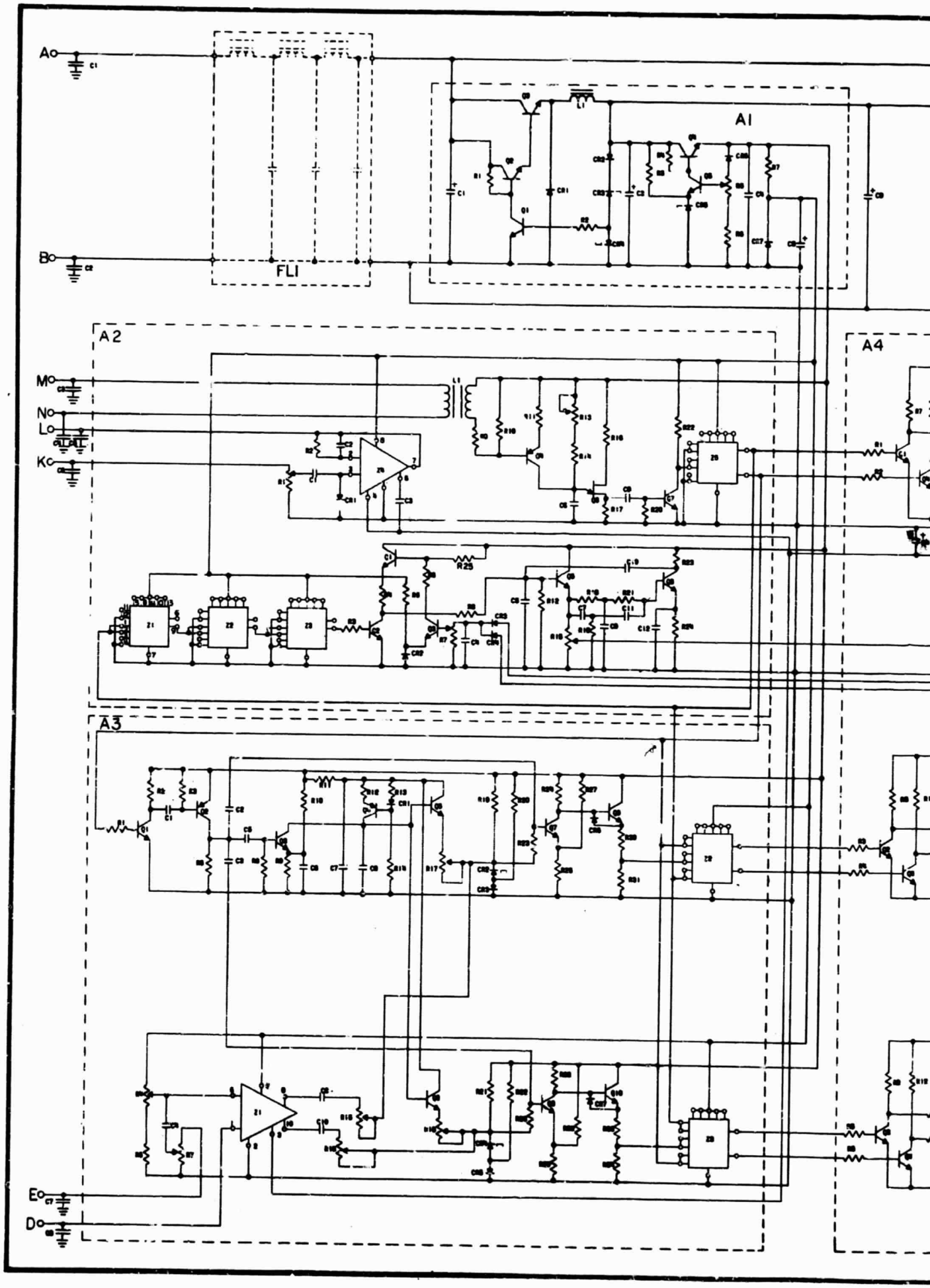
The inverter is protected from overloads by the output voltage sensor. When the output exceeds a predetermined level, a voltage signal to the waveshaper network causes the output reference sine wave to decrease, in turn, reducing the output voltage.

B. DETAILED CIRCUIT DESCRIPTION (Figure 16)

The completed schematic diagram for the High-Frequency Phase-Demodulated Bridge Inverter (Figure 16) includes not only the components required for single-phase operation but also those required for parallel operation, three-phase operation, and parallel-three-phase operation. To ensure complete understanding of the inverter design concept as well as the operation of each of the modules, a detailed description of the operation of each module is provided. The schematic is divided into five major sections, the first three sections A1, A2, A3, are control functions, and the last two, A4 and A5, are power functions. Control sections A1, A2, and A3 represent three possible printed circuit board arrangements. Section A4 represents the amplifier or drive stages (this function could be one or three separated modules as determined by the final mechanical design). Section A5 is all hardware normally connected to the main chassis because of size or heatsink requirements.

Discussion of various circuits is not necessarily in the order of their location on the schematic, but is in logical sequence of their operation and relationship to each other:

1. Control Voltage Regulator
2. Synchronization Circuit and Internal Oscillator
3. Power Stage Drive and Power Stage



FOLDOUT FRAME

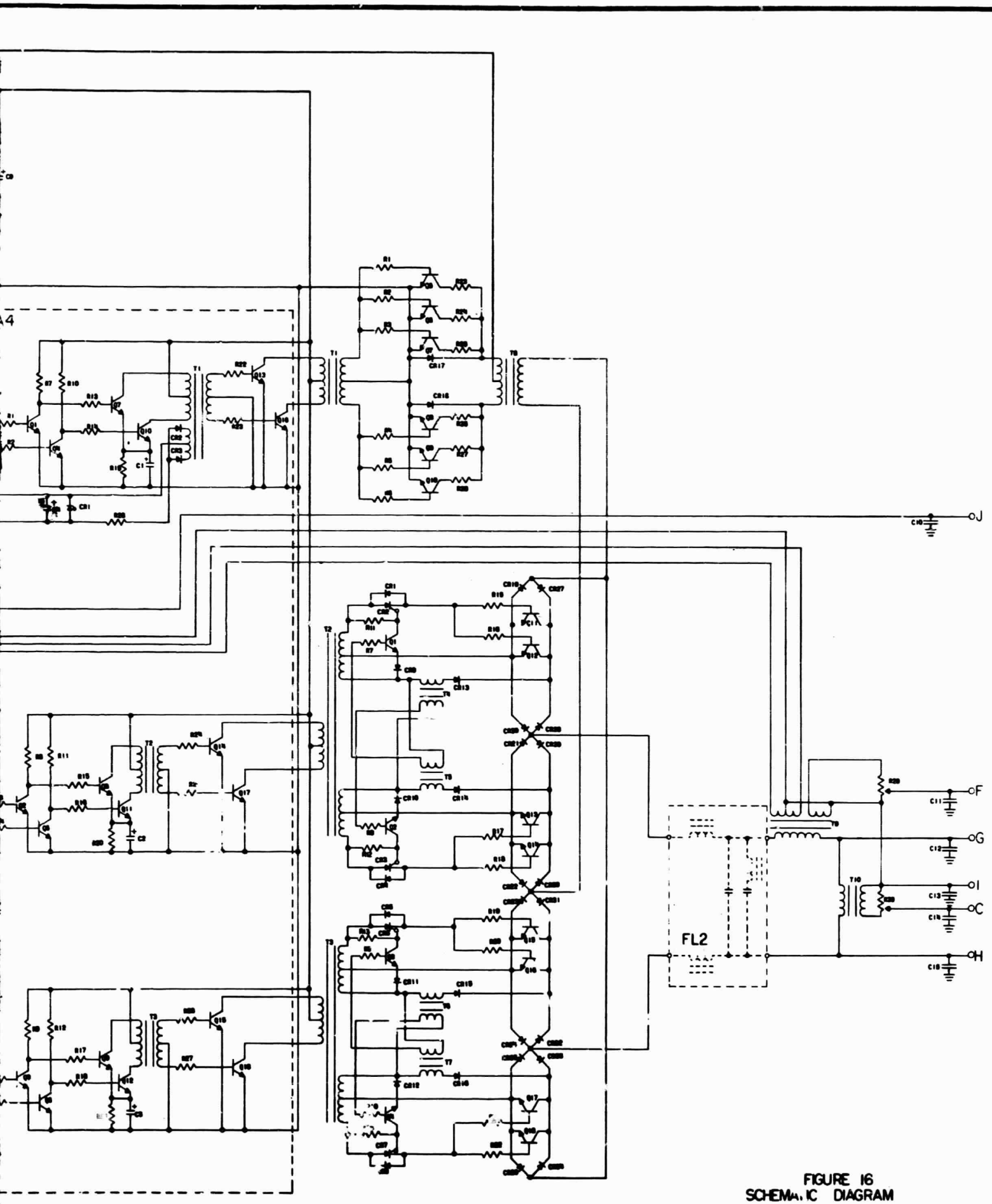


FIGURE 16
SCHEMATIC DIAGRAM

FOLDOUT FRAME 2

4. Countdown Circuit and Filter Network
5. Ramp Generator Differential Amplifier and Reference Comparators
6. Demodulator Drives and Demodulator
7. Filtering Output and Input and RFI
8. Voltage and Current Sensing
9. Three-Phase and Parallel Interconnection

1. Control Voltage Regulator (Figure 17)

The control voltage regulator contains a chopper regulator, a series regulator, and a zener regulator. The combined use of several types of power controls was selected to achieve maximum efficiency with maximum performance of the control sections.

The chopper regulator is the most efficient, acts as preregulator for the other regulator circuits and provides all power for the drive circuits. Through the use of this preregulator, the losses normally associated with series regulator circuits, zener circuits, and base drive circuits are greatly reduced. The chopper regulator circuit is illustrated in Figure 18.

Transistors Q1, Q2, and Q3 are operated in a saturated switching mode; that is, they are either ON or OFF. Their ON state is made a direct function of the output DC level and is controlled by constant current diode CR2, zener diode CR3, and tunnel diode CR4.

The DC output voltage level is established by the zener diode CR3. The constant current diode CR2 limits the current through the zener, thus allowing a low power zener to be utilized as a reference. The tunnel diode CR4 performs the actual regulation of the period of oscillation determined by the current through the tunnel diode. When there is an increase in the output voltage, there is a corresponding increase in the current through CR2, thus causing the tunnel diode to go into a low impedance state. At this time the voltage across the tunnel diode increases, turning transistor Q1 ON, turning OFF transistor Q2; Q3 in turn causes a drop in the output voltage which reduces the current through the tunnel diode, returning it to its original state.

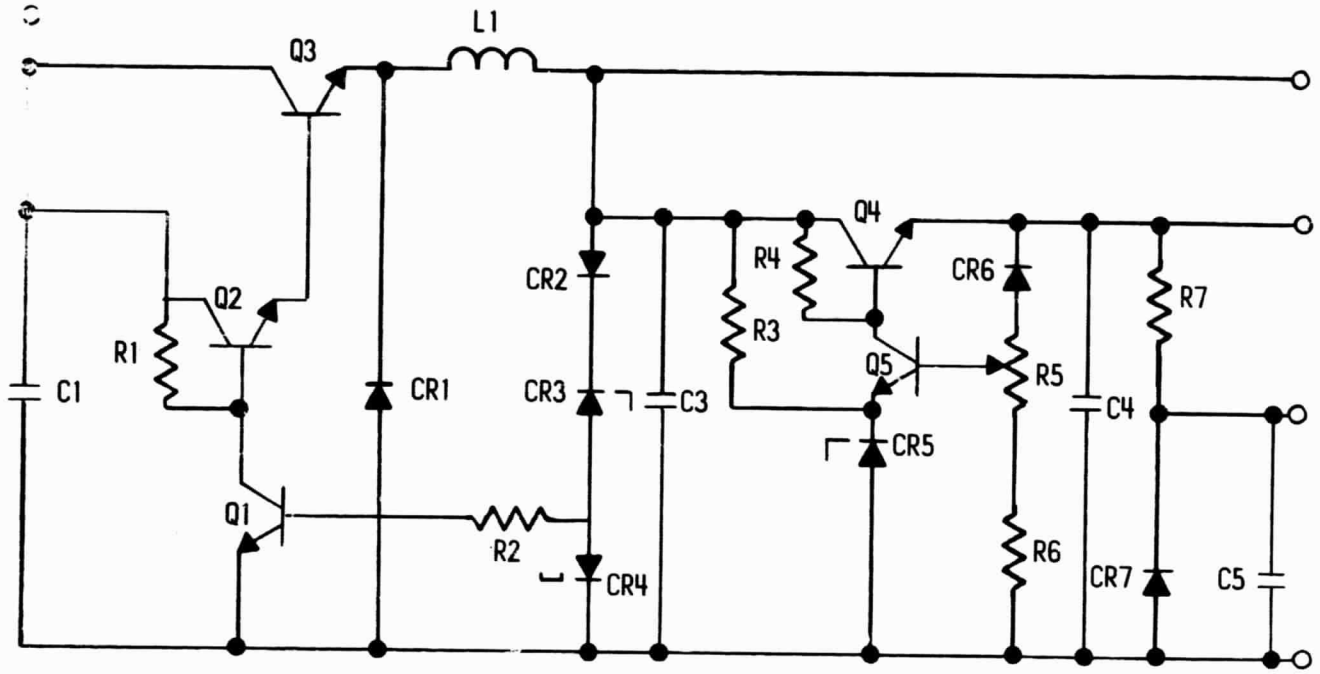


FIGURE 17
CONTROL VOLTAGE REGULATOR

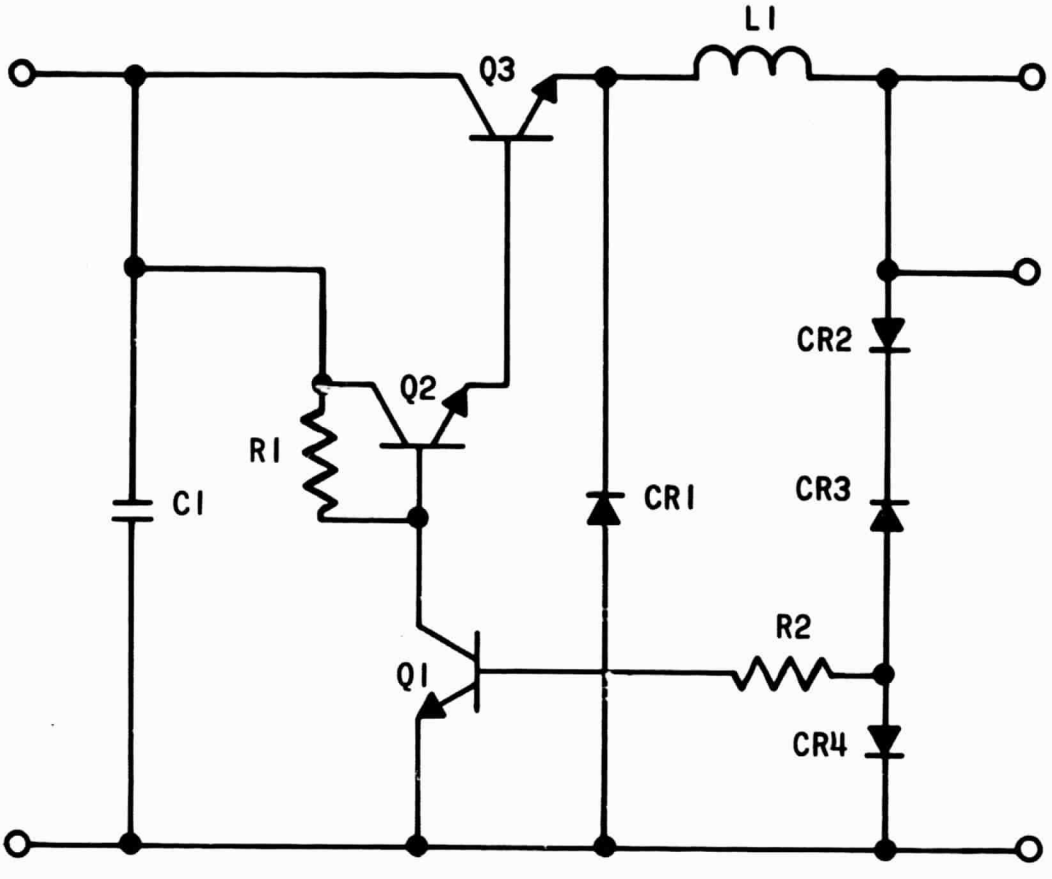


FIGURE 18
CHOPPER REGULATOR

The frequency of oscillation is determined by the LC circuit and load current which in turn varies the current through CR4. Since the current through the tunnel diode is a direct function of the voltage out of the regulator, the tunnel diode regulates the output voltage by controlling the OFF-ON condition of transistor Q1. The output regulation and ripple is a function of the zener diode and the tunnel diode. Regulation runs about 2 percent with the 2 percent ripple voltage and an overall efficiency of about 95 percent.

Since many of the control functions cannot tolerate the voltage variation and ripple of the chopper regulator circuit while maintaining the desired output requirements, a separate DC source must be established for these functions. The series regulator provides the precise power requirements of the control circuits. Since it operates off the chopper regulator output, its power dissipation is at a minimum.

The series regulator circuit (Figure 19) is a standard series regulator in which the output voltage is compared with a reference voltage established by zener diode CR5. The voltage change of the output is compared through transistor Q5 and voltage sensing network R6, R5, and CR6. Zener diode CR6 was added to the sensing network to increase the amount of the error signal appearing at the base of transistor Q5.

Also illustrated in Figure 19 is the zener diode circuit consisting of R7 and CR7. This circuit establishes required bias levels for the integrated circuit networks.

The various capacitors illustrated in the various regulator circuits are used for filtering and to help decouple the different regulator circuits.

2. Synchronization Circuit and Internal Oscillator

The internal oscillator circuit is a 6400-Hz relaxation oscillator designed around unijunction transistor Q6 in Figure 20. In the free-running mode, capacitor C6 is charged through resistors R13 and R14 and discharged through emitter base one junction of transistor Q6 as the firing point of the unijunction transistor is reached. At this point the current through resistors R13 and R14

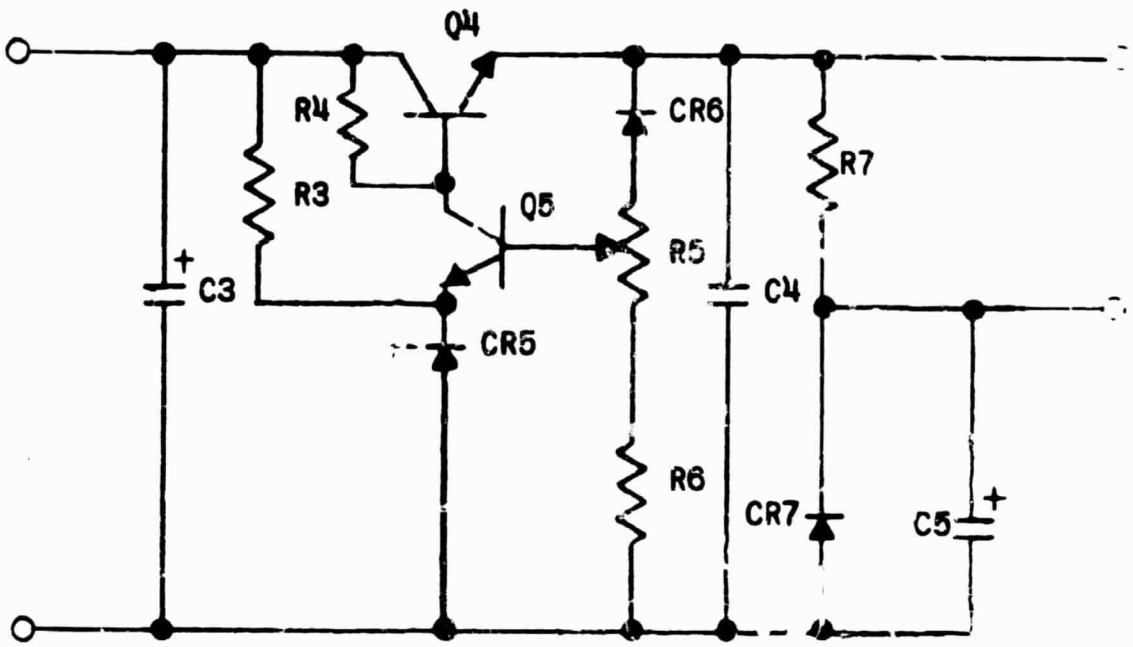


FIGURE 19
SERIES REGULATOR

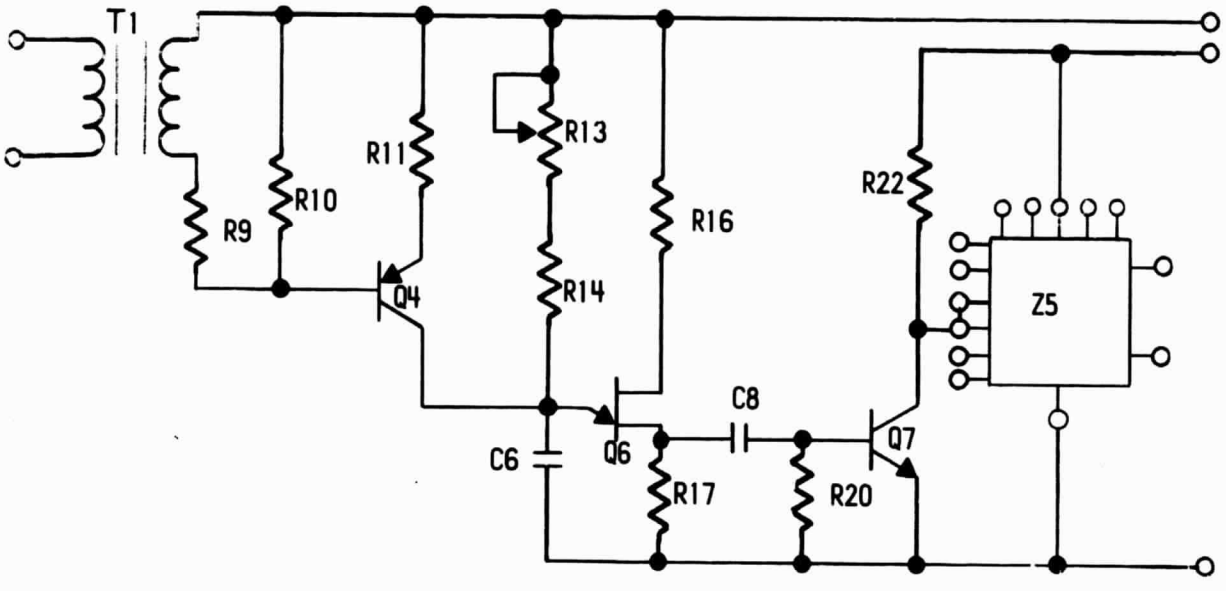


FIGURE 20
OSCILLATOR NETWORK

is insufficient to maintain the ON condition in transistor Q6, thus the cycle is repeated.

The positive voltage-pulse developed across resistor R17 when transistor Q6 turns ON is amplified and inverted by transistor Q7, providing a negative pulse to trigger bistable multivibrator Z5. Multivibrator Z5 then develops a 3200-Hz squarewave.

In the synchronized mode, the input squarewave is transformer coupled to the base of switching transistor Q4, turning Q4 ON and OFF on alternate half-cycles. This feature is used to synchronize the unijunction transistor oscillator to the input signal. Resistor R11 is of sufficiently low value so that when transistor Q4 is turned ON, capacitor C6 is abruptly charged and transistor Q6 turns ON. Transistor Q6 remains ON as long as Q4 is ON because the current through resistor R11 is greater than the holding current for transistor Q6. After one half-cycle, transistor Q4 and, in turn, transistor Q6 turn OFF. Then capacitor C6 again starts charging through resistors R13 and R14. Thus, transistor Q6 is actually locked in phase with transistor Q4, and with the input squarewave.

3. Power Stage Drive and Power Stage

The power stage drive is primarily a power amplifier which amplifies the two squarewave voltages produced by the internal oscillator flip-flop. This amplifier, or drive circuit, is illustrated in Figure 21. The voltage at the base of transistor Q1 is illustrated in Figure 22a, while Figure 22b illustrates the voltage at the base of transistor Q2. When the voltage of Figure 21a is positive, transistor Q1 is ON, turning transistor Q7 OFF. Transistor Q10 is ON at this time, producing a positive voltage at the base of transistor Q13 and turning it ON. The collector voltage of Q13 is illustrated in Figure 22c, while Figure 22d illustrates the collector voltage of transistor Q16. Thus, Figure 22 illustrates the input and output voltages of the drive stage with the proper phasing.

The drive stage also has a secondary function of providing negative voltage requirements to the differential amplifier and phase-shift network. This function is accomplished by adding an additional secondary winding to

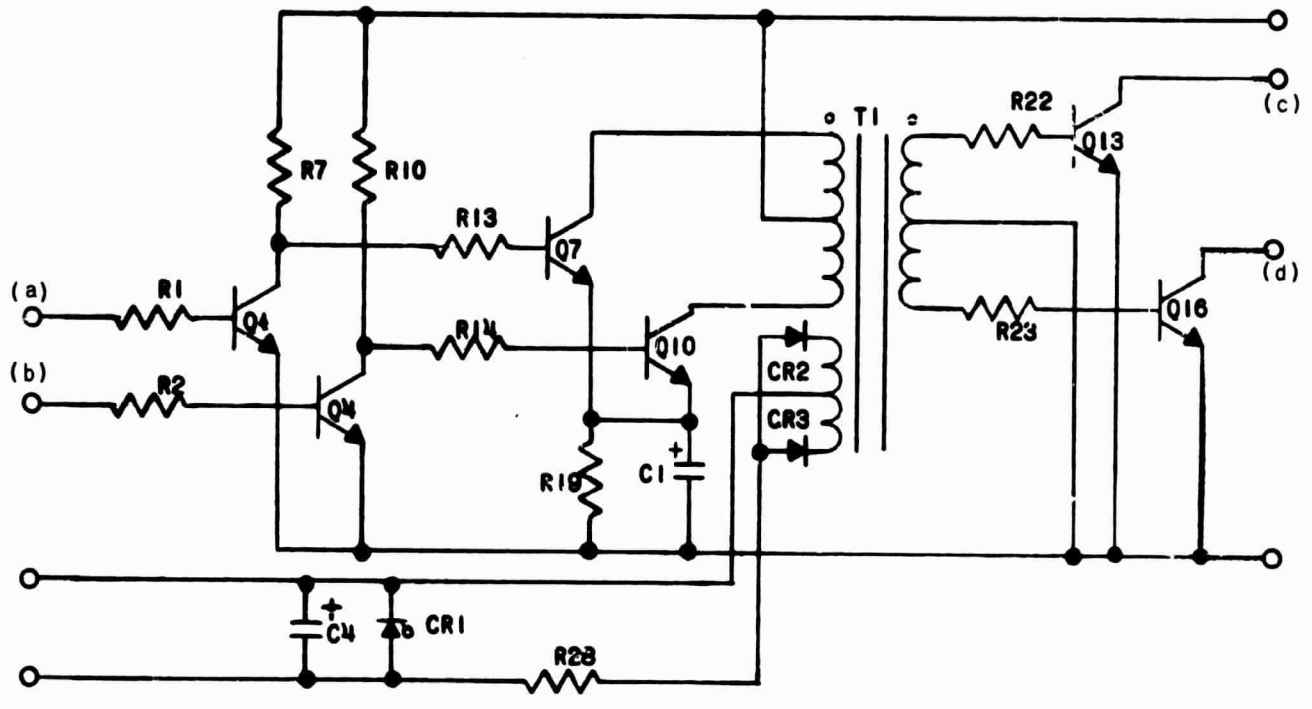


FIGURE 21
POWER STAGE DRIVE

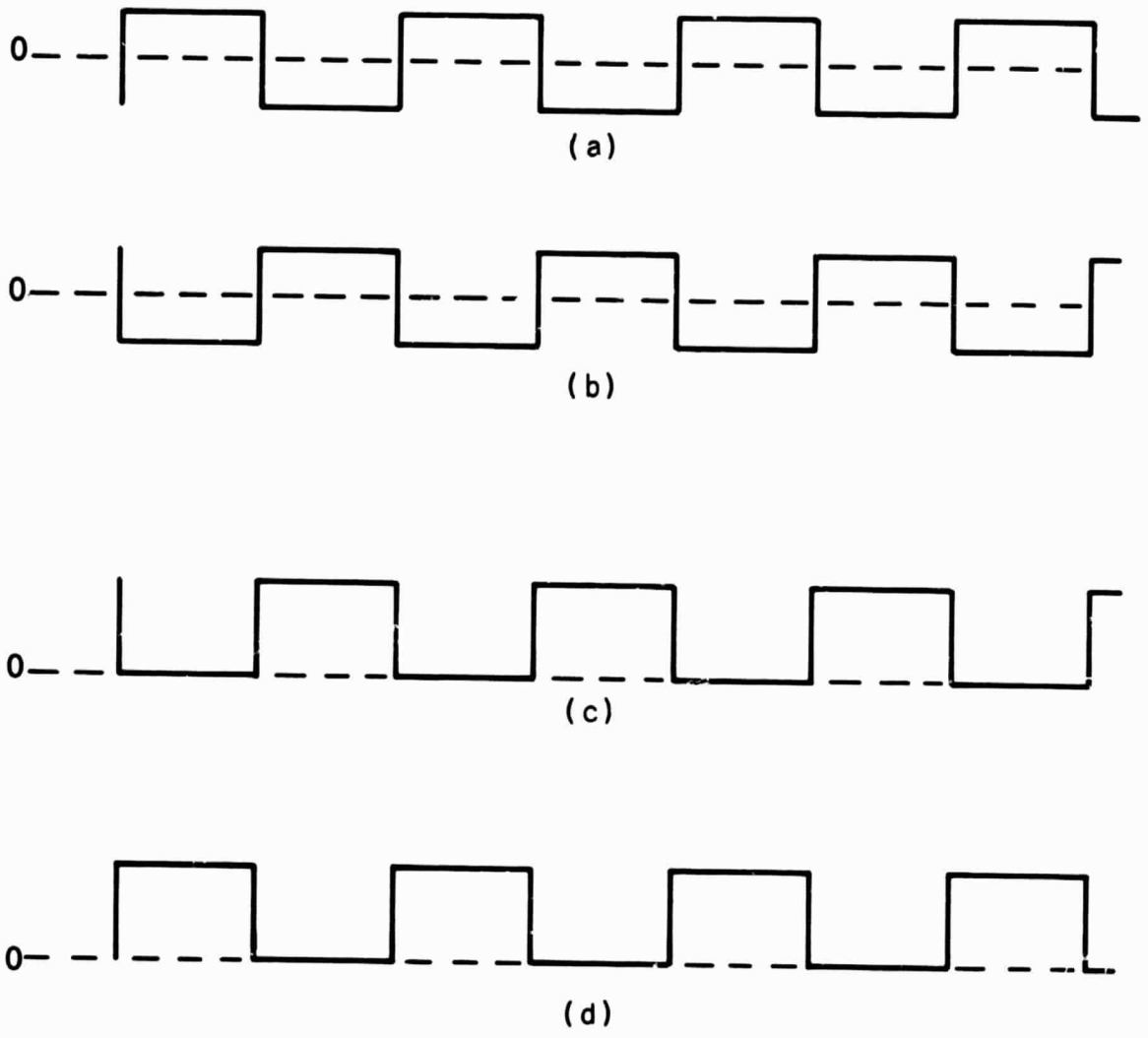


FIGURE 22
DRIVE STAGE WAVEFORMS

transformer T1. The output of this winding is rectified, filtered, and zenered to provide precise voltage level.

The primary function of the power stage is to convert the input DC voltage to an AC voltage and amplify this AC voltage to the proper level for use by the demodulator stage. The power stage is illustrated in Figure 23 and consists primarily of a drive transformer, power transistors, and a power transformer.

Drive transformer T1 is used for impedance matching between the power transistor and the drive stage. The push-pull input to the drive transformer is illustrated in Figure 24. The voltage at terminal 1 of T1 is illustrated in Figure 22a while Figure 22b illustrates the voltage at terminal 3. The voltages of terminal 4 are shown in Figure 24c while the inverse of this voltage appears at terminal 6, Figure 24d. These voltages drive power transistors Q5 through Q10. By using fast-rising squarewave drive voltages, switching losses are kept to a minimum. Resistors R1 through R6 are current-sharing resistors used to equalize the drive voltages and currents of the power transistors.

Transistors Q5 through Q7 are turned ON when the drive voltage, Figure 24c, is positive. Transistors Q8 through Q10 are biased OFF at this time by their drive voltage (Figure 24d). The push-pull action of the power transistors produces an AC voltage at the primary of power transformer T8 which is amplified, producing the 3200-Hz squarewave voltage illustrated in Figure 24e.

4. Countdown Circuit and Filter Network

A 400-Hz squarewave is developed by binary countdown from the 3200-Hz squarewave. Three bistable multi-vibrators are diagrammed in block form as Z1, Z2, and Z3 in Figure 25, along with the 400-Hz filter circuit.

Transistor Q2 is used as a saturating amplifier to isolate Z3 from the filter. The filter itself is of the active type, designed around a twin-tee network which is tuned to 400 Hz. Transistor Q5 is an emitter follower input stage. The twin-tee passes all frequencies except 400 Hz to the base of inverting

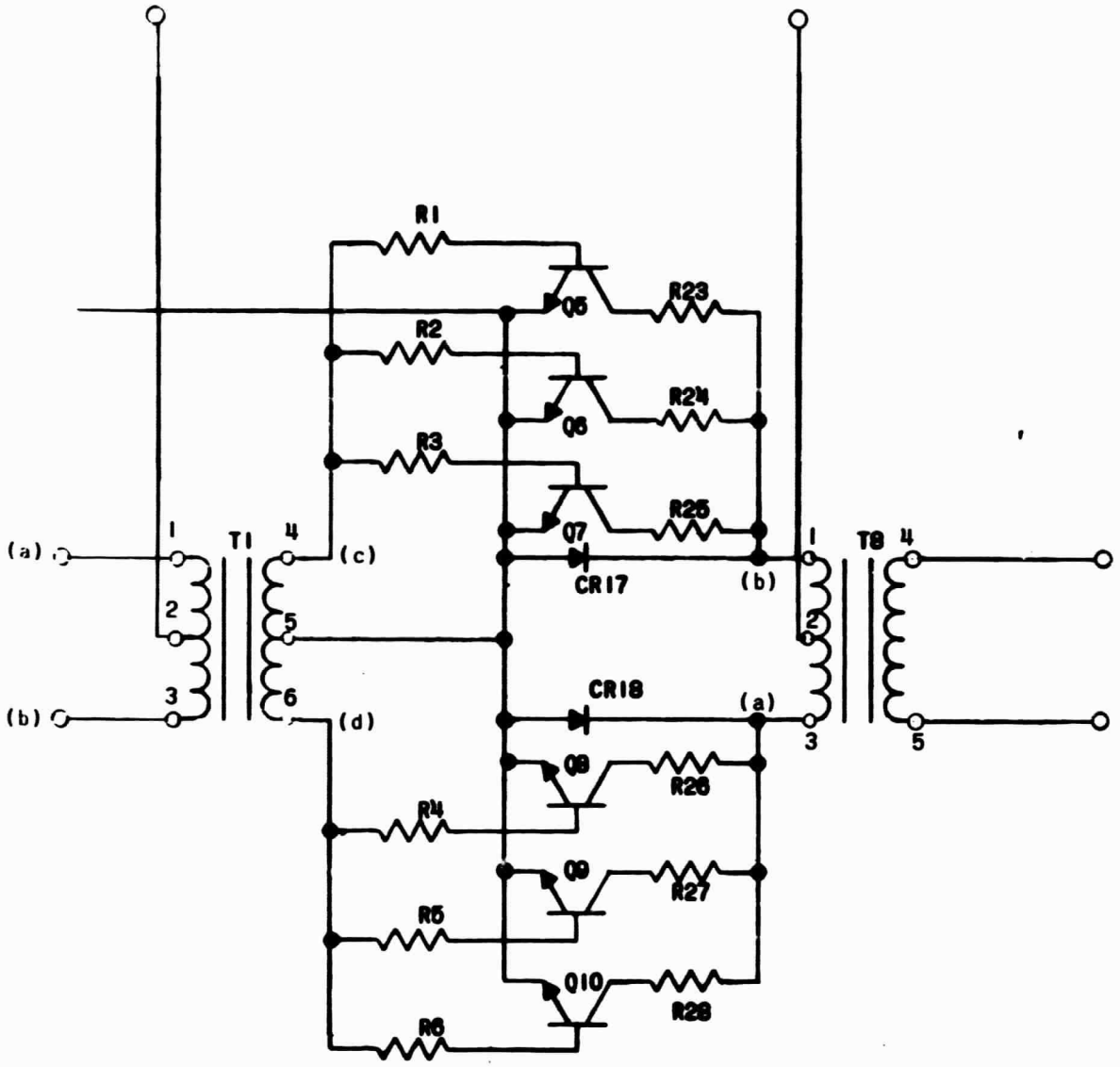


FIGURE 23
POWER STAGE

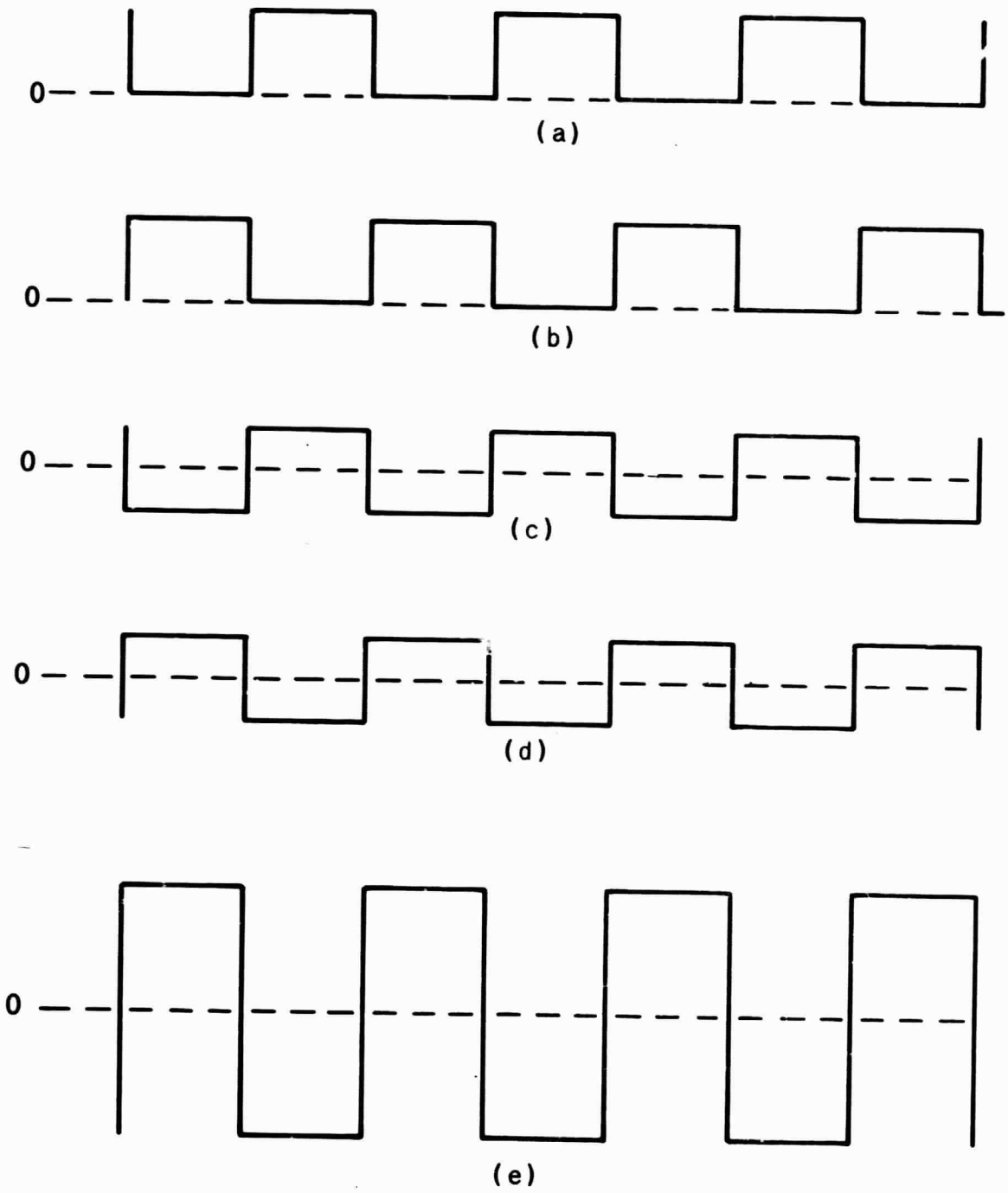
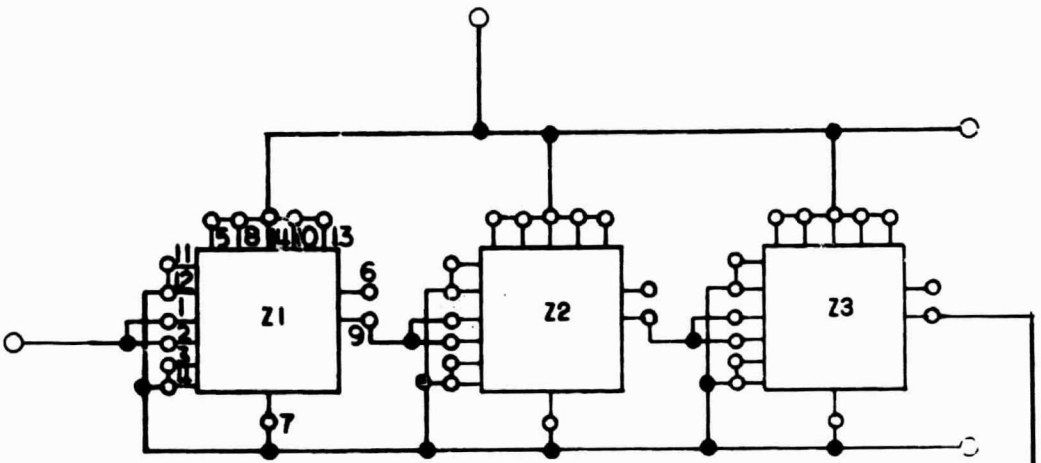


FIGURE 24
POWER STAGE WAVEFORMS



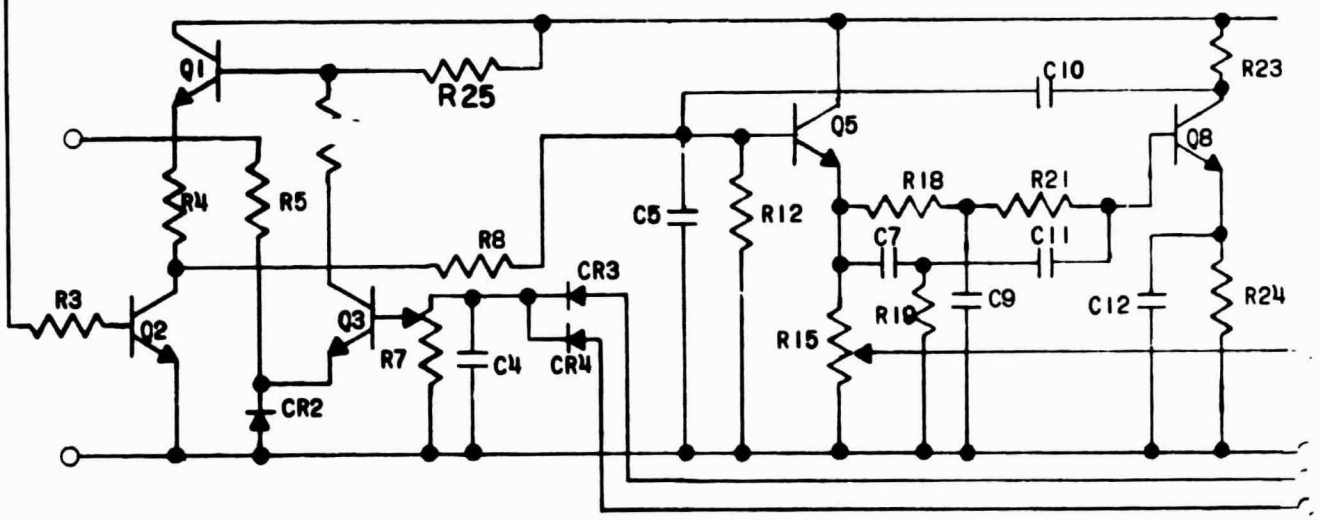


FIGURE 25
COUNTDOWN AND FILTER NETWORK

amplifier stage Q6. Then feedback capacitor C10 provides negative feedback for all frequencies, except 400 Hz. Thus, the odd harmonic content of the 400-Hz squarewave is filtered out, leaving a 400-Hz low-distorted sine wave.

5. Ramp Generator, Differential Amplifier, and Reference Comparators (Figure 26)

These four circuits represent the basic feedback or regulator loop of the inverter. They are illustrated as a group, showing the interrelationships.

The ramp generator (Figure 26) is basically what its name implies; a circuit that generates a linear ramp function. To provide a detailed understanding of the operation of the ramp generator, various voltage and current waveforms are illustrated (Figure 27) along with discussion of how they are obtained.

If transistor Q4 were ON and a voltage applied to resistor R12, a voltage would develop at point A, Figure 27a. This is the charging potential that appears across a capacitor as it is charged through a resistor from a DC source. The 3200-Hz squarewave output voltage of the internal oscillator is integrated to form a 3200-Hz synchronizing pulse, Figure 27b, at point B. As this pulse turns transistor Q3 ON, point A is clamped to ground, forcing capacitor C8 to discharge. The voltage now appearing across capacitor C8, point A, is illustrated in Figure 27c.

To make the ramp more linear, the charging current must be held constant. This is done by holding the voltage across R12 constant. Resistors R13 and R14 form a voltage divider network to which the base of transistor Q4 is connected. Diode CR1 is for temperature compensation. Since the base current is small compared with the fixed current of R13 and R14, the voltage at point C remains fixed. This, in turn, holds the voltage across resistor R12 constant, producing the sawtooth voltage illustrated in Figure 27d. Transistors Q5 and Q6 act as emitter followers to produce the ramp currents (Figure 27e) used by the reference comparator circuits.

The key to the operation of this circuit is the synchronizing

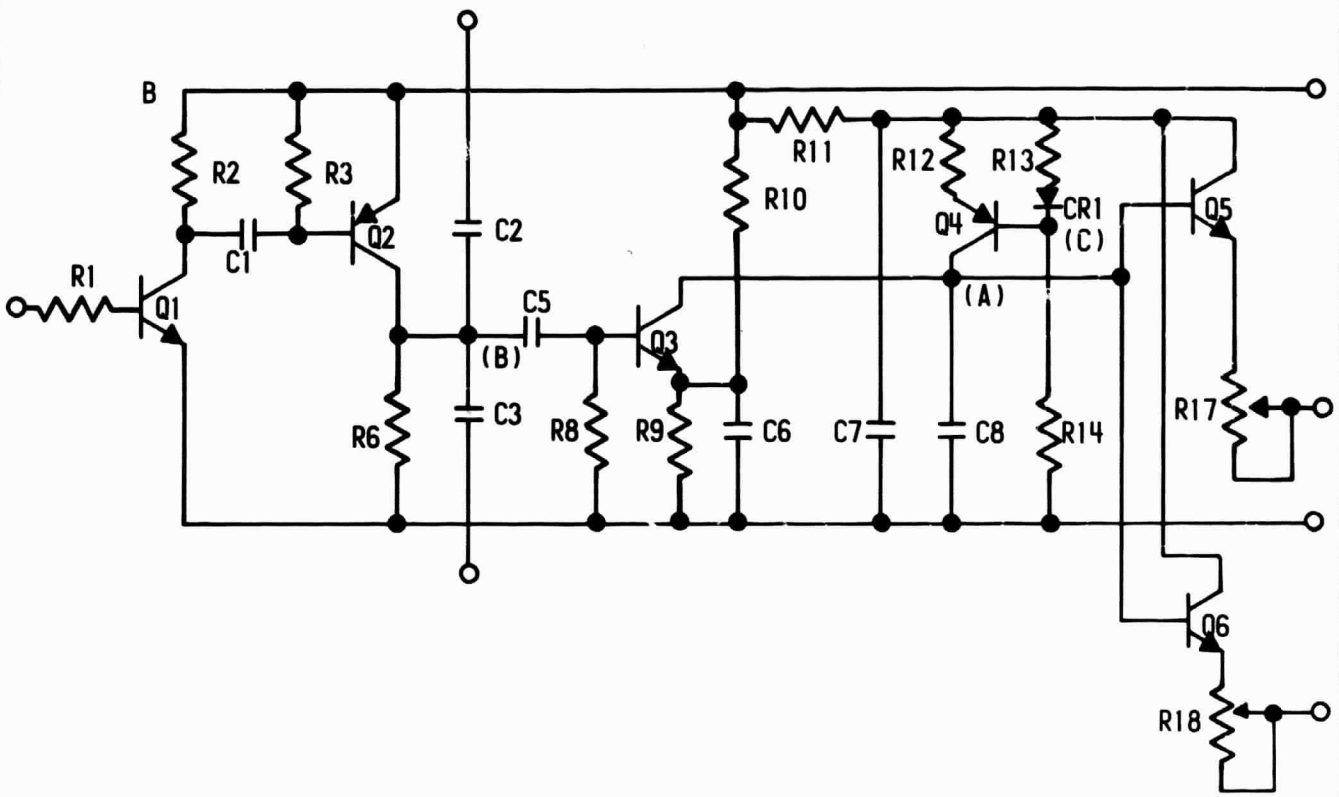


FIGURE 26
RAMP GENERATOR

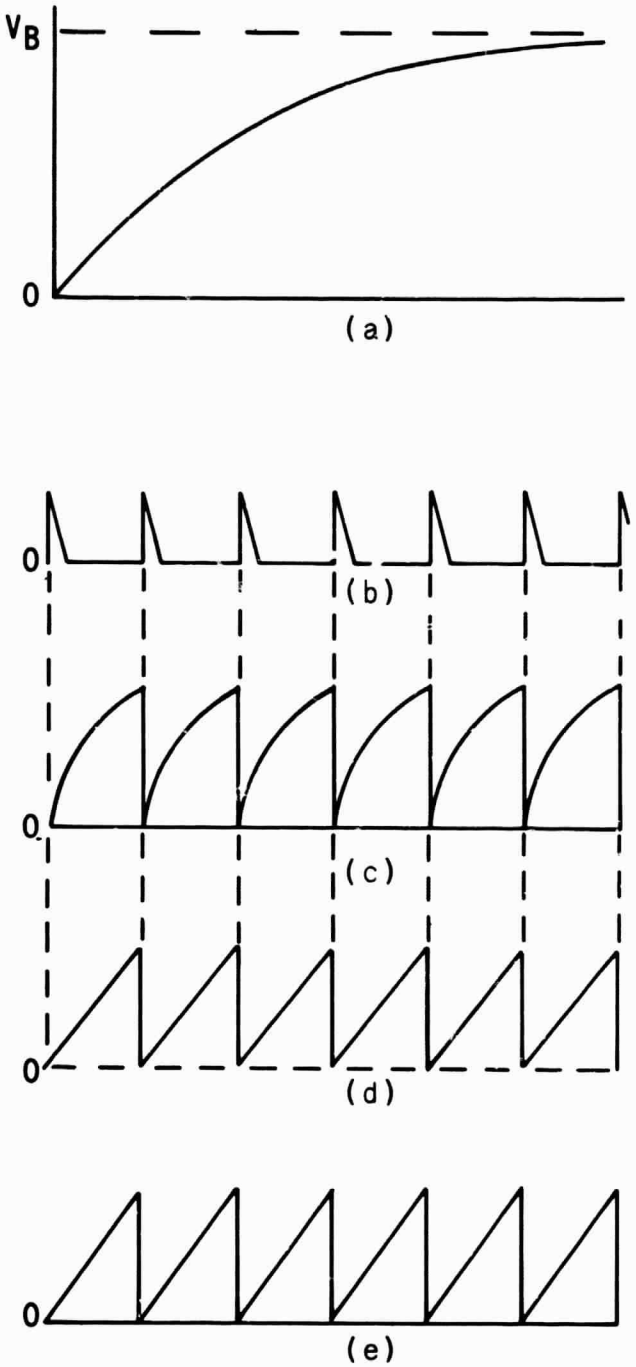


FIGURE 27
SAWTOOTH WAVEFORMS

pulse which prevents transistor Q4 from operating out of its active region. (If Q4 becomes saturated, the voltage waveform becomes nonlinear.) The synchronizing pulse also synchronizes the reference comparator circuits to be explained later.

The differential amplifier is a high-gain amplifier used to compare the output voltage with a fixed reference voltage established by the filter network. The amplifier circuit is illustrated in Figure 28. So that the inverter meets the paralleling and three-phase interconnection requirements, the amplifier is designed to provide the correct error signals at points C and D with predetermined signals at points A and B. This is necessary so that the inverter may be connected in parallel or three-phase without readjustments.

The amplifier compares the feedback sine wave with the reference sine wave and produces two sine wave error signals. One error signal is in phase with the output while the other error signal is 180 degrees out of phase. An increase in the output voltage of the inverter causes a decrease in the two error signals, thus causing the output voltage to be reduced in proportion to the change in the error signal. This relationship becomes more obvious in the discussion of reference comparators.

The function of the reference comparator circuits is to furnish two sets of 3200-Hz modulated squarewave drive voltages for the demodulator stage. Modulation of the squarewave voltages is a function of the sine wave error signals and is determined by the reference comparator. Since operation of both reference comparators is identical, a detailed explanation of only one comparator is given. Waveforms for both circuits are illustrated in Figure 30, while the schematic diagram for the comparators is illustrated in Figure 29.

The heart of the comparator is tunnel diodes CR2 and CR4. As is well known, a tunnel diode has a negative resistance region which is a function of the current through the diode. When current through the diode reaches a predetermined level, known as Ip, voltage across the diode takes an immediate step jump to some higher value determined by the load line of the device. This increase in voltage across the tunnel diode is in the order of

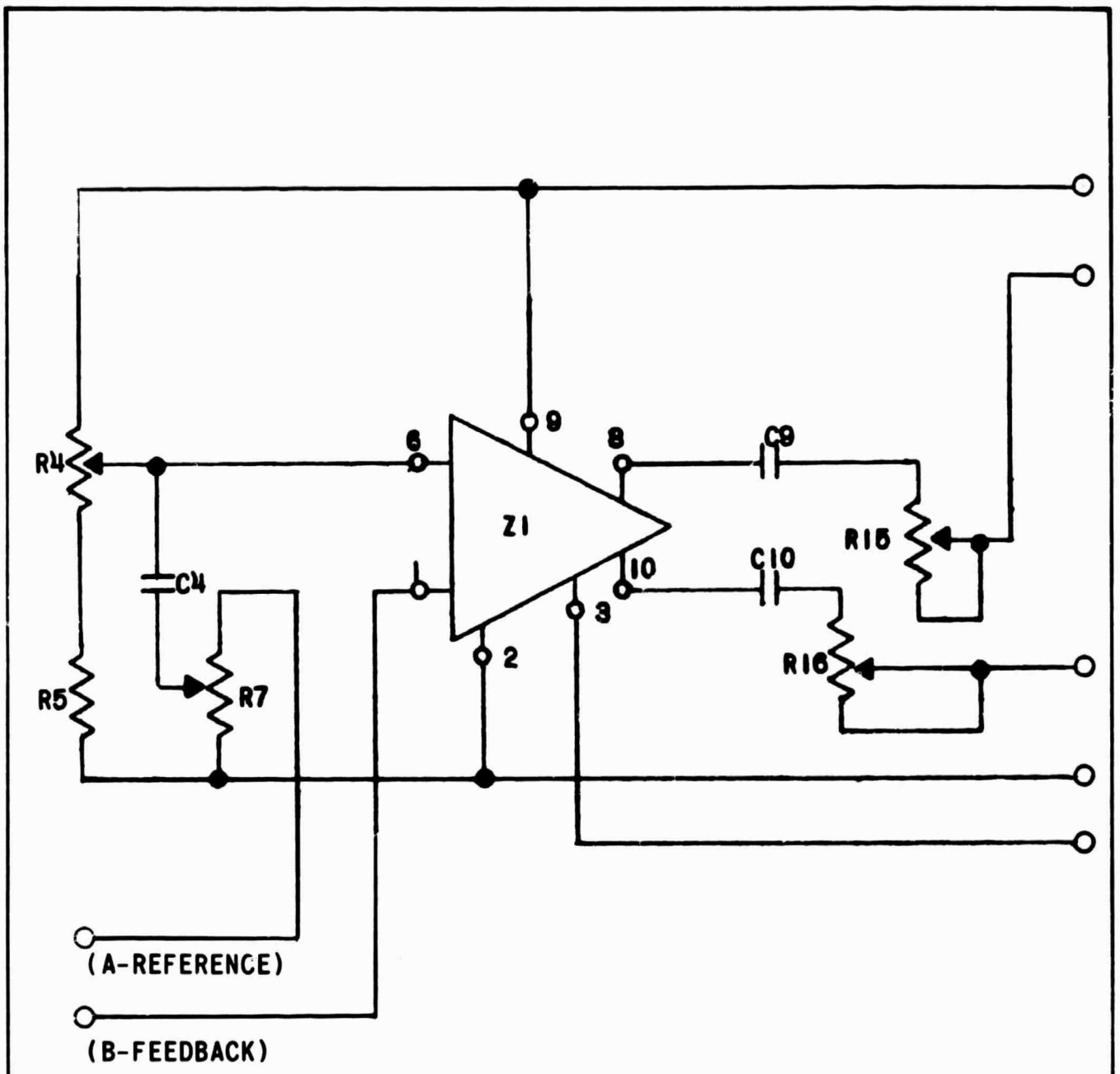


FIGURE 28
DIFFERENTIAL AMPLIFIER

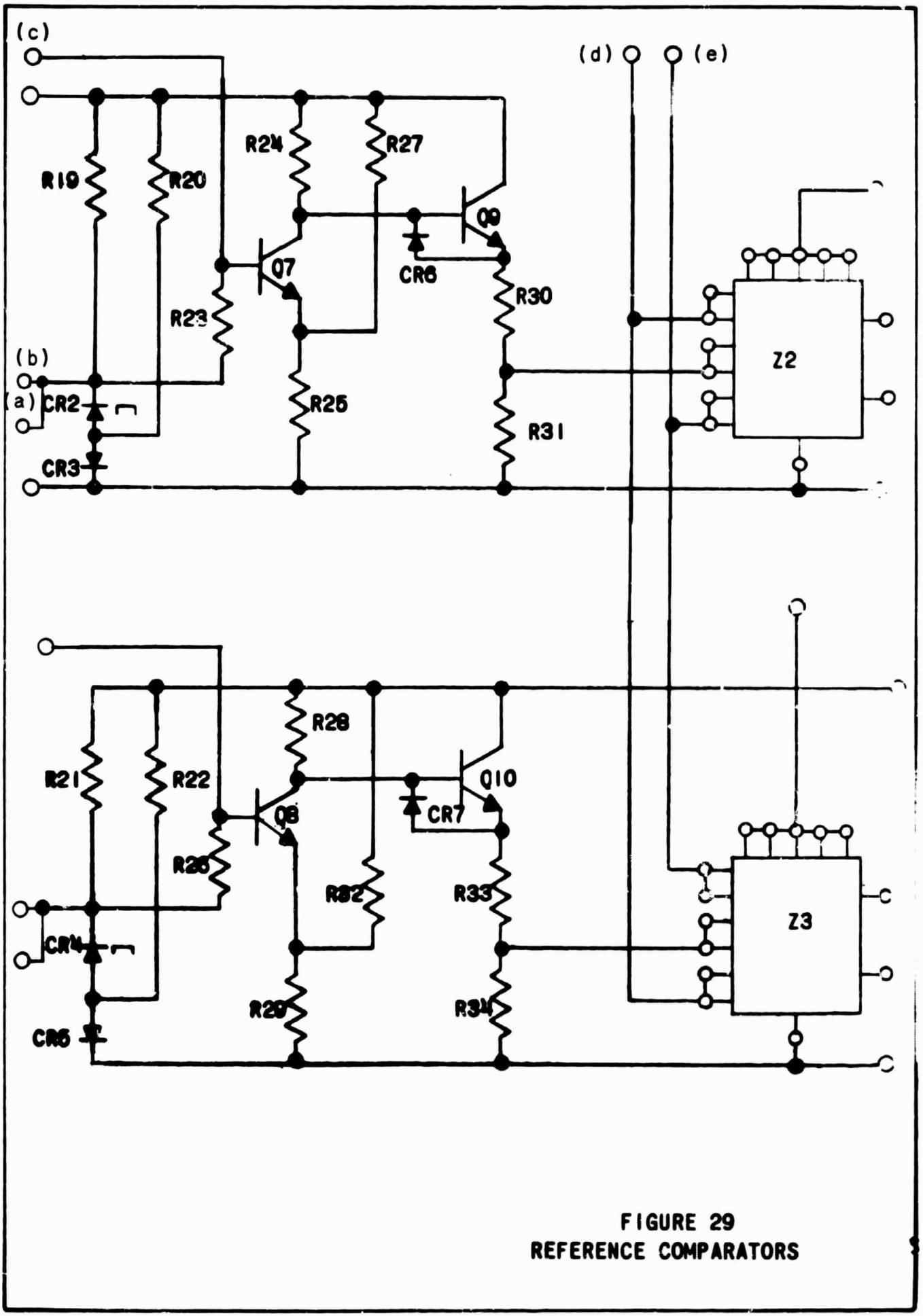


FIGURE 29
REFERENCE COMPARATORS

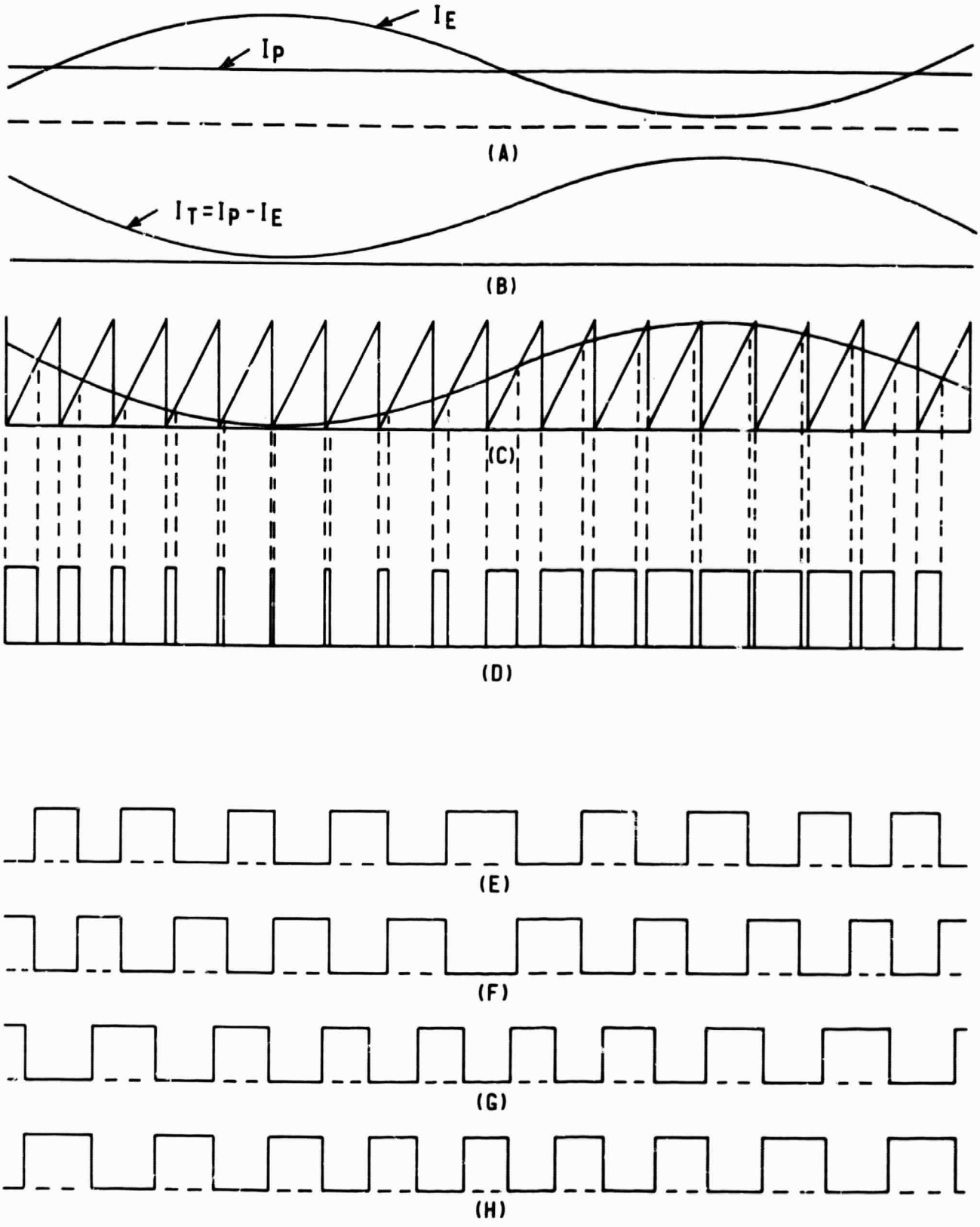


FIGURE 30
REFERENCE COMPARATOR WAVEFORMS

magnitude of five. Corresponding with this increase in voltage, there is a decrease in current through the tunnel diode due to its negative resistance characteristics. This characteristic is utilized to obtain a step voltage without a corresponding increase in current. Again referring to Figure 29, it is seen that the step voltage appearing across tunnel diode CR2 turns transistor Q7 ON.

The waveforms of Figure 30 further illustrate the regulating action of the tunnel diode. The Ip, or trigger level, of the tunnel diode is illustrated in Figure 30a. Now, if sinusoidal error current I_E from the reference comparator is superimposed over Ip, then the locus of a new trigger point, I_T, may be plotted (Figure 30b). Trigger point I_T of tunnel diode CR2 is now a sinusoidal function of error signal I_E.

By combining sawtooth current I_S with trip current I_T, transistor Q7 may be driven in a modulated form. Figure 30c shows that each time ramp current I_S of the sawtooth crosses trip point I_T of the tunnel diode, the tunnel diode changes states, turning transistor Q7 ON. This, in turn, turns transistor Q9 OFF. Each time the ramp is reset the tunnel diode is reset and transistor Q7 is turned OFF through Point C which is connected to capacitor C2 in the ramp generator circuit.

The output of transistor Q9 (Figure 30d) drives flip-flop Z_2. When this voltage (Figure 30d) goes negative, the flip-flop reverts states (Figures 30e and 30f).

Operation of the second reference comparator is identical to that of the first, except that tunnel diode trip point I_T is phase shifted 180 degrees from that of the first reference comparator. The output of transistor Q10 is the same as illustrated in Figure 10d, except inverted. This output, in turn, drives flip-flop Z3, which has an output (Figures 30g and 30h).

To ensure proper phasing between the demodulator stage and the power stage, flip-flops Z2 and Z3 are phase locked to the output of Z5 of the oscillator circuit through connections d and e.

6. Demodulator Drive and Demodulator (Figure 31)

Demodulator drive stage operation is the same as the power stage drive operation, thus a detailed discussion is not furnished.

The demodulator drive stage amplifies the signal from the flip-flop of the reference comparator to a level usable by the demodulator stage

The object of the demodulator stage is to convert the 3200-Hz squarewave voltage to a pulse-width modulated voltage. Half of the demodulator stage is illustrated in Figure 32. The complete demodulator (Figure 16) is made up of four bilateral switches and four base drive impedance-matching networks. The impedance-matching networks form the same function as the power stage, except that they have been modified to improve switching characteristics. This function is described more fully in the Design Analysis section of the report.

The bilateral switches, consisting of transistors Q11 through Q18 and diodes CR19 through CR34, convert the 3200-Hz squarewave voltage to a pulse-width modulated voltage. A simplified version of the bilateral switch showing possible current flow is shown in Figure 33.

The simplified schematic of Figure 34 along with the waveforms of Figure 35 are used to show the phase and modulation operation of the demodulator stage. Figure 34a is the 3200-Hz squarewave out of the power stage. Figure 34b is the push-pull voltage from a reference comparator which controls the operations of the bilateral switches. When the voltage (Figure 34b) is positive, switch S1 is closed and S2 is open. The output of the other reference comparator (Figure 35c) drives switches S3 and S4. When it is positive, S3 is ON and S4 is OFF. The demodulator stage output, a 6400-Hz pulse-width modulated voltage waveform (Figure 35d) may now be developed. To help in the explanation, a set of reference points (1-8) are added to Figure 35d.

At point 1, the power stage output reverses so that it is negative. Also, at this time switch 1 and switch 4 are ON due to the voltage condition illustrated in Figures 35b and 35c. This condition places a short circuit on the input of the filter. Since switches S2 and S3 are OFF, or open, the secondary of the power transformer is unloaded and there is no voltage at the input of the filter.

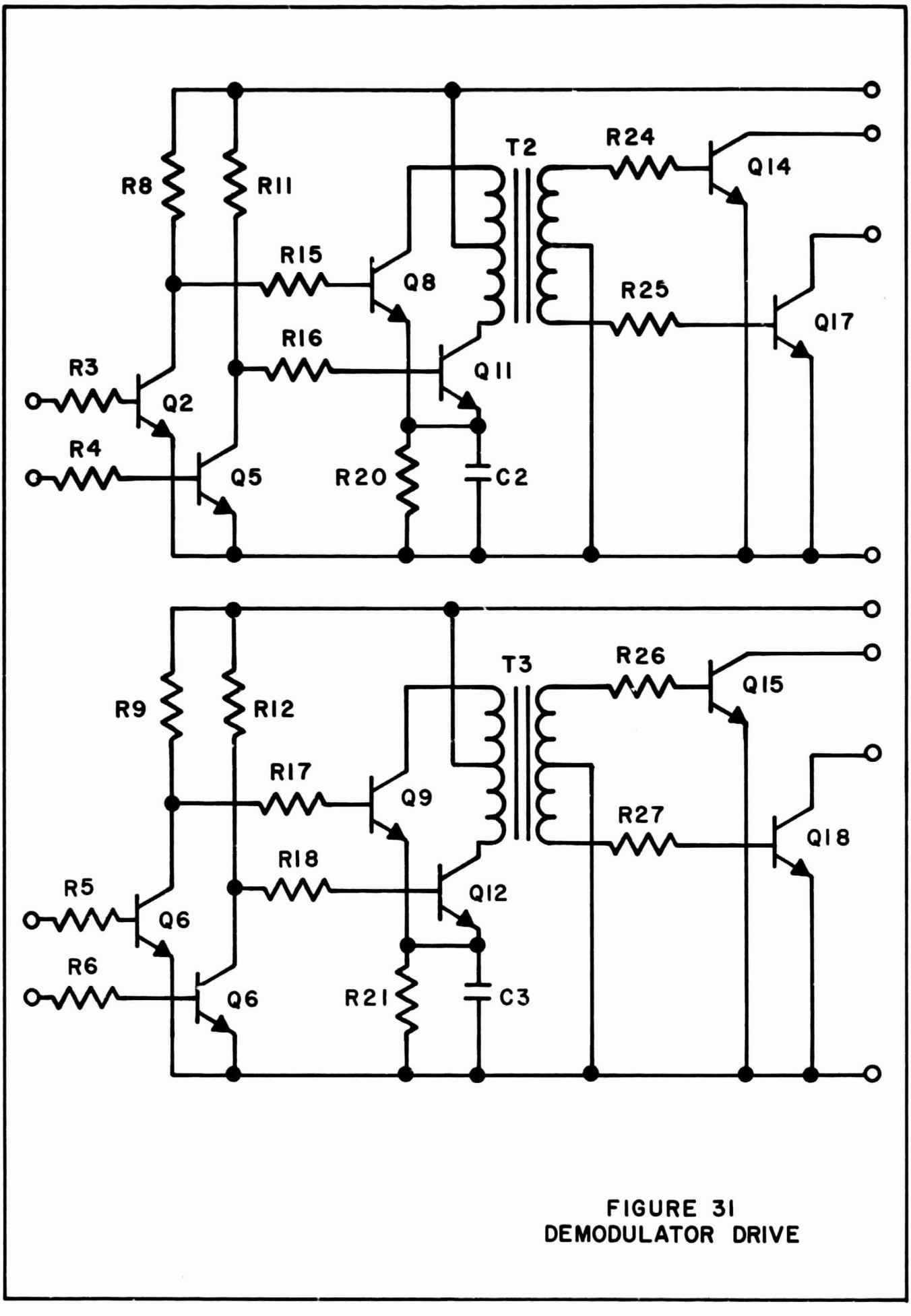


FIGURE 31
DEMODULATOR DRIVE

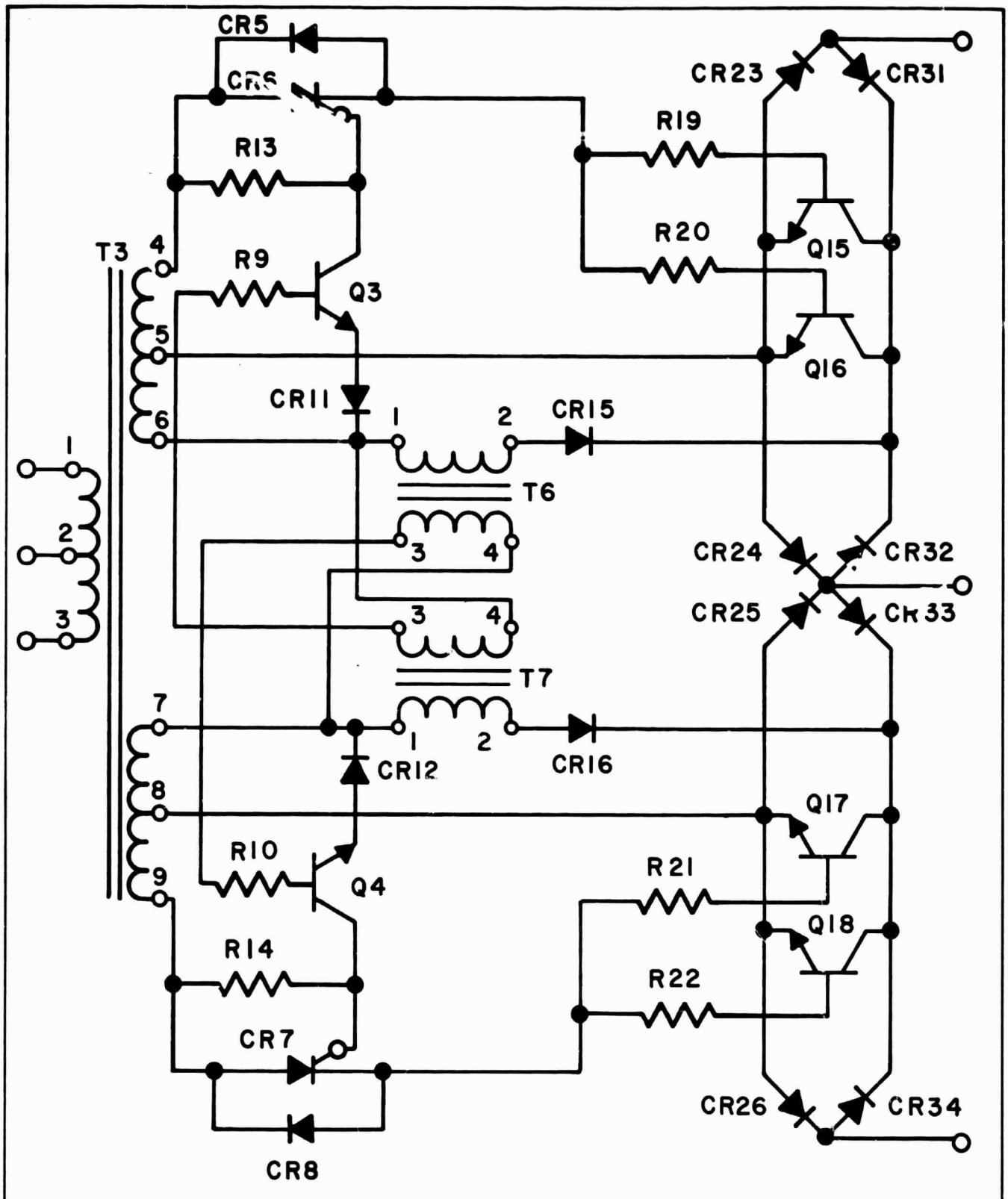


FIGURE 32
DEMODULATOR STAGE

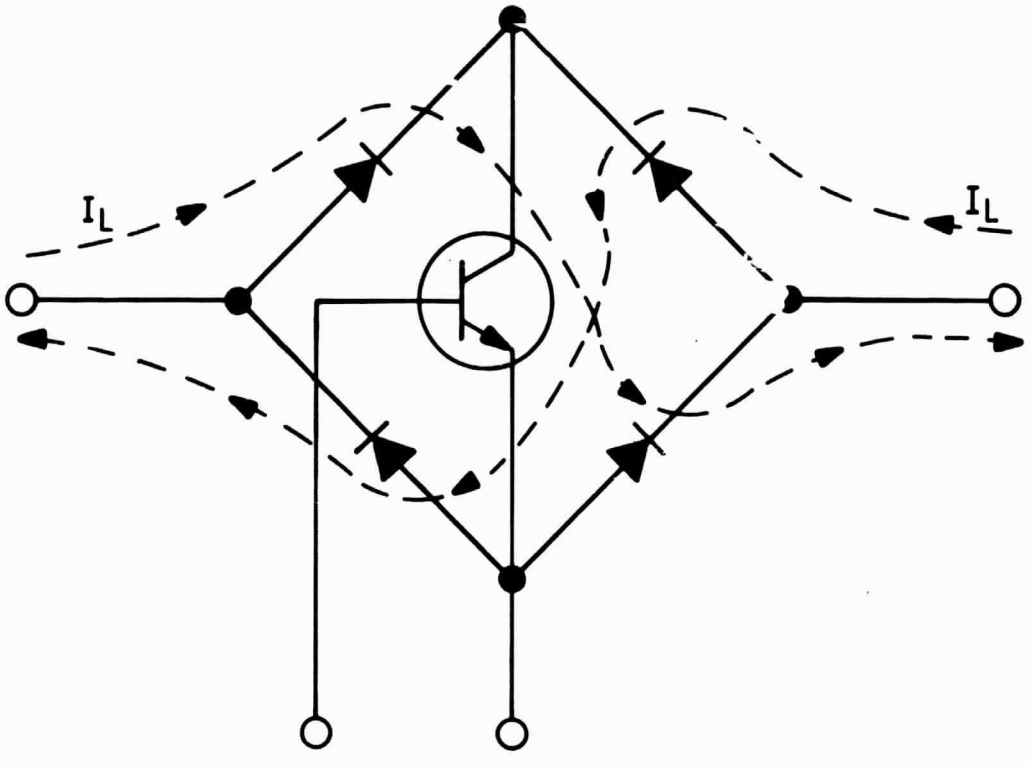


FIGURE 33
BILATERAL SWITCH

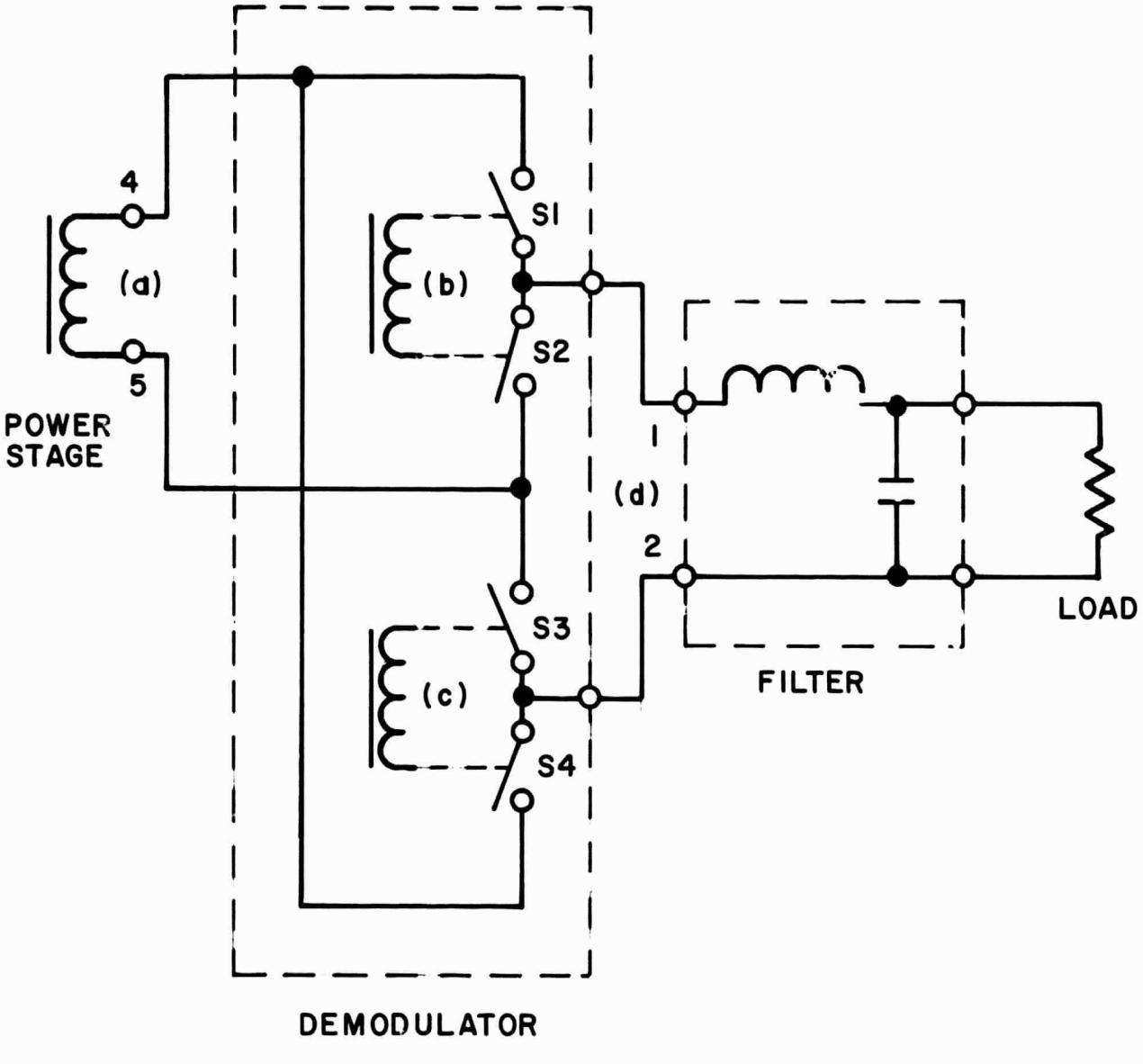


FIGURE 34
SIMPLIFIED SCHEMATIC

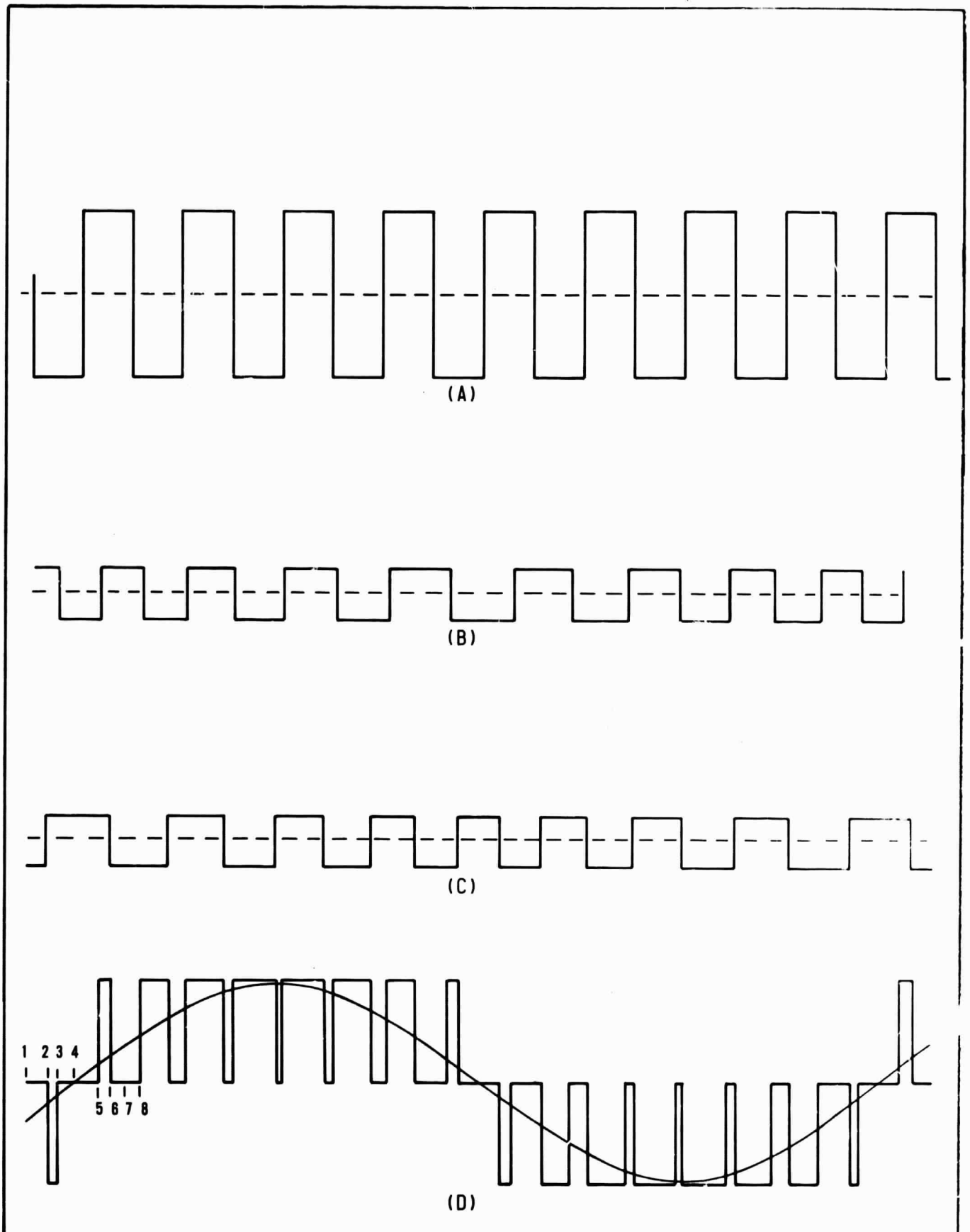


FIGURE 35
DEMODULATOR WAVEFORMS

This condition is illustrated in simplified form in Figure 36a.

At point 2, the voltage to switches 3 and 4 reverses, turning switch 4 OFF and turning switch 3 ON. Inspection of Figure 34 shows that under this condition terminal 1 of the filter is connected to terminal 4 of the power stage and terminal 5 of the power stage is connected to terminal 2 of the filter. Since the output of the transformer (4 to 5) is negative, then a negative voltage appears at the input of the filter. This circuit is illustrated in Figure 36b, and its waveform in Figure 35d, points 2 to 3.

At point 3, the drive (Figure 35b) for switches 1 and 2 reverses, turning switch 1 OFF and switch 2 ON. This again shorts out the input to the filter (Figure 36c).

At point 4, the output of the power stage reverses polarity as in Figure 35a; however, there was no action by the demodulator switches, thus the input to the filter does not change (Figure 35d).

At point 5, the drive (Figure 35b) again reverses, turning switch S2 OFF while turning switch S1 ON. This action connects the transformer to the filter (Figure 36d). Since the output of the transformer is positive, a positive voltage appears at the input to the filter.

By following the switching action of the power stage and the controlling action of the demodulator switches, the pulse-width modulated voltage (Figure 35d) is developed. Pulse-width modulation is a function of the operation of the modulator switches which are controlled by the reference comparators. The amount of modulation, or the pulse width, of the pulses determines the amplitude of the output sine wave (Figure 35d).

7. Filtering Output, Input, and RFI

The output of the demodulator consists primarily of a group of positive going and negative going pulses with a basic frequency of 6400 Hz (Figure 35d). The primary function of the output filter is to waveshape this modulated voltage to form a sine wave containing a minimum amount of distortion. It is also desirable that the filter achieve this function without producing any

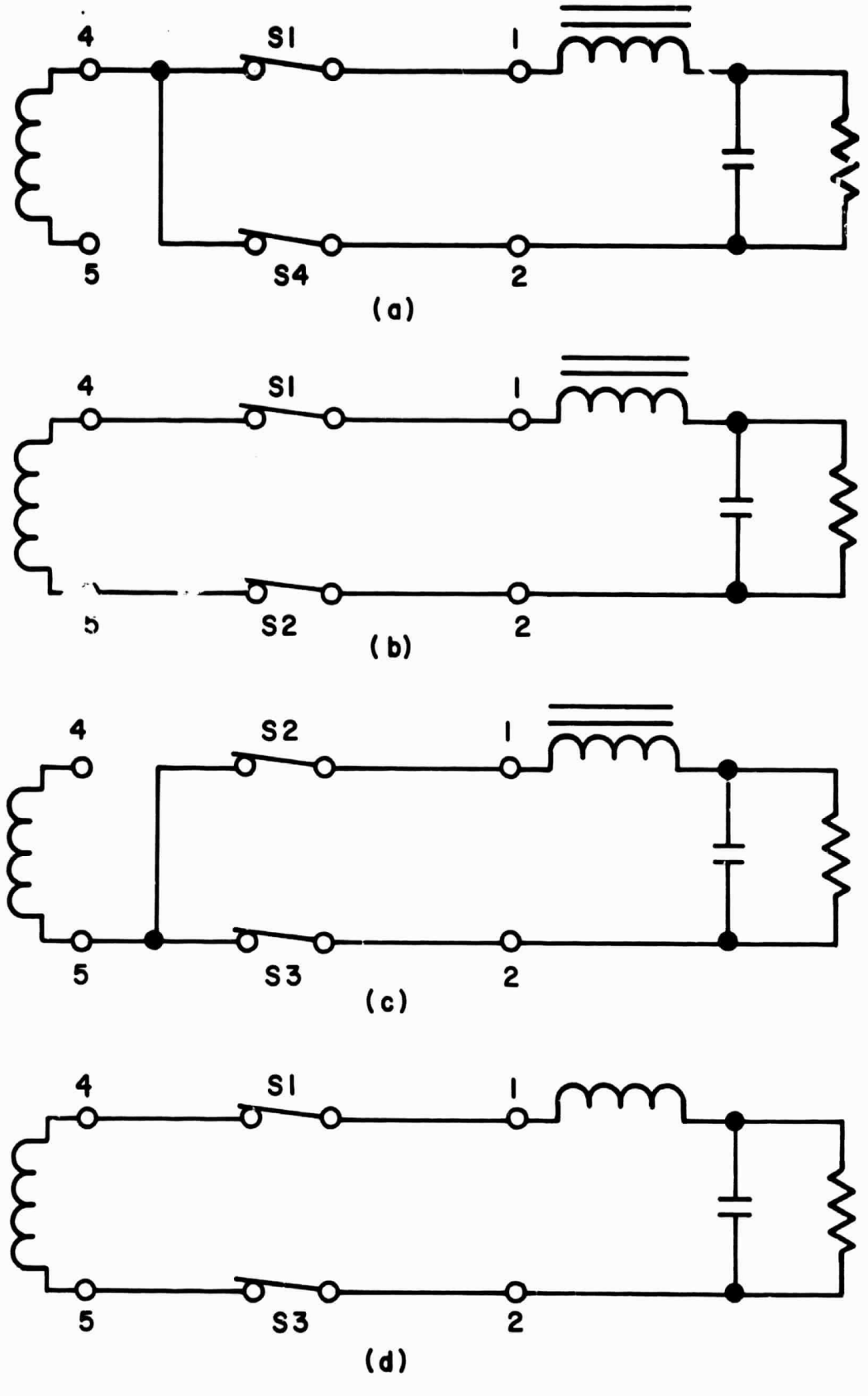


FIGURE 36
DEMODULATOR OPERATION

unnecessary voltage-ampere burden on the demodulator or power stage. It is further desired that the filtering operation be independent of the inverter load.

Figure 35d shows that fundamental voltage is a direct function of the amount of modulation; however, the major requirement for the filter design is a knowledge of the harmonic voltages present and their respective frequencies. Figure 37 is a plot of the frequency spectrum of the pulse-width modulated waveform shown in Figure 35d. This spectrum is for a modulation index of one and reveals that the four major harmonic voltages present are located at 5200 Hz, 6000 Hz, 6800 Hz, and 7600 Hz. These four harmonic voltages represent the major harmonics that must be filtered by the filter while passing the fundamental 400-Hz frequency.

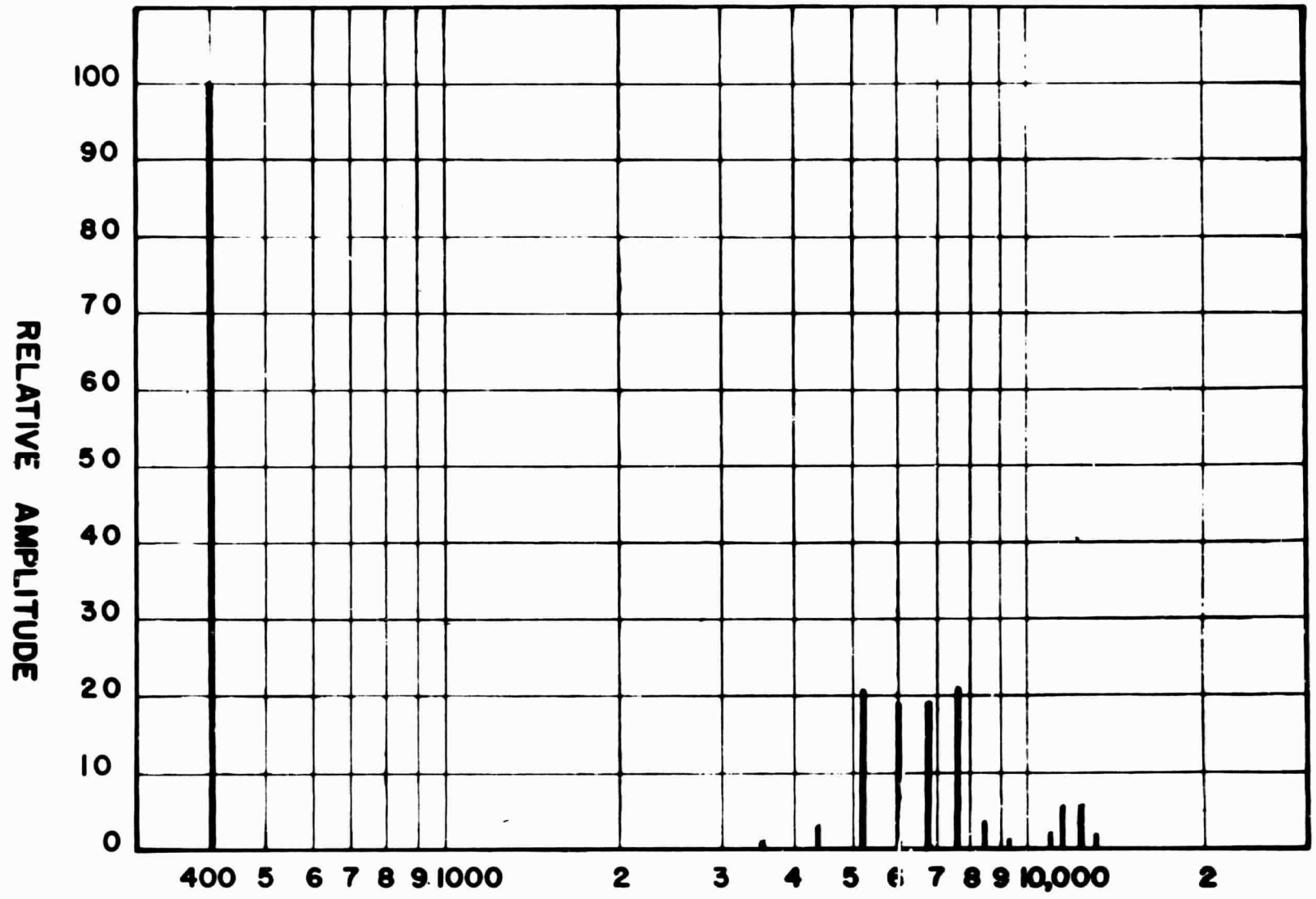
The design which offers the maximum design advantage is presented as FL2 in Figure 38. This is a simple low-pass filter designed for the specific 400-Hz load conditions. To further attenuate the four basic harmonic frequencies, a series-tuned 4600-Hz trap is added.

To reduce the RFI requirements, the parallel inductor, normally one device, is split into two separate inductors (L_1 and L_2). Since this is a low-pass filter, simple bypass capacitors reduce the RFI to the desired level.

The input filter shown in Figure 39 as FL1 isolates the input DC line from modulation and ripple generated by the inverter. It also isolates the inverter from high-voltage surges on the DC line.

The filter design is based primarily on the modulation requirement -- the governing factor. A 400-Hz inverter modulates the input at an 800-cycle rate; therefore, filter requirements are basically those of a 400-cycle rectified sine wave with the load current and source impedance determining the filter requirements. One additional requirement of the phase-demodulated inverter is that the input current is a combination of 6400-Hz pulses and a 400-Hz rectified sine wave.

(Final design will be determined through test and evaluation of the waveforms generated by the prototype inverter. This determination is necessary for maximum efficiency with minimum weight. This filter will also act as



$f_c = 400$
$f_v = 6400$
$M = 1.0$

FIGURE 37
FREQUENCY SPECTRUM
DOUBLE EDGE MODULATION

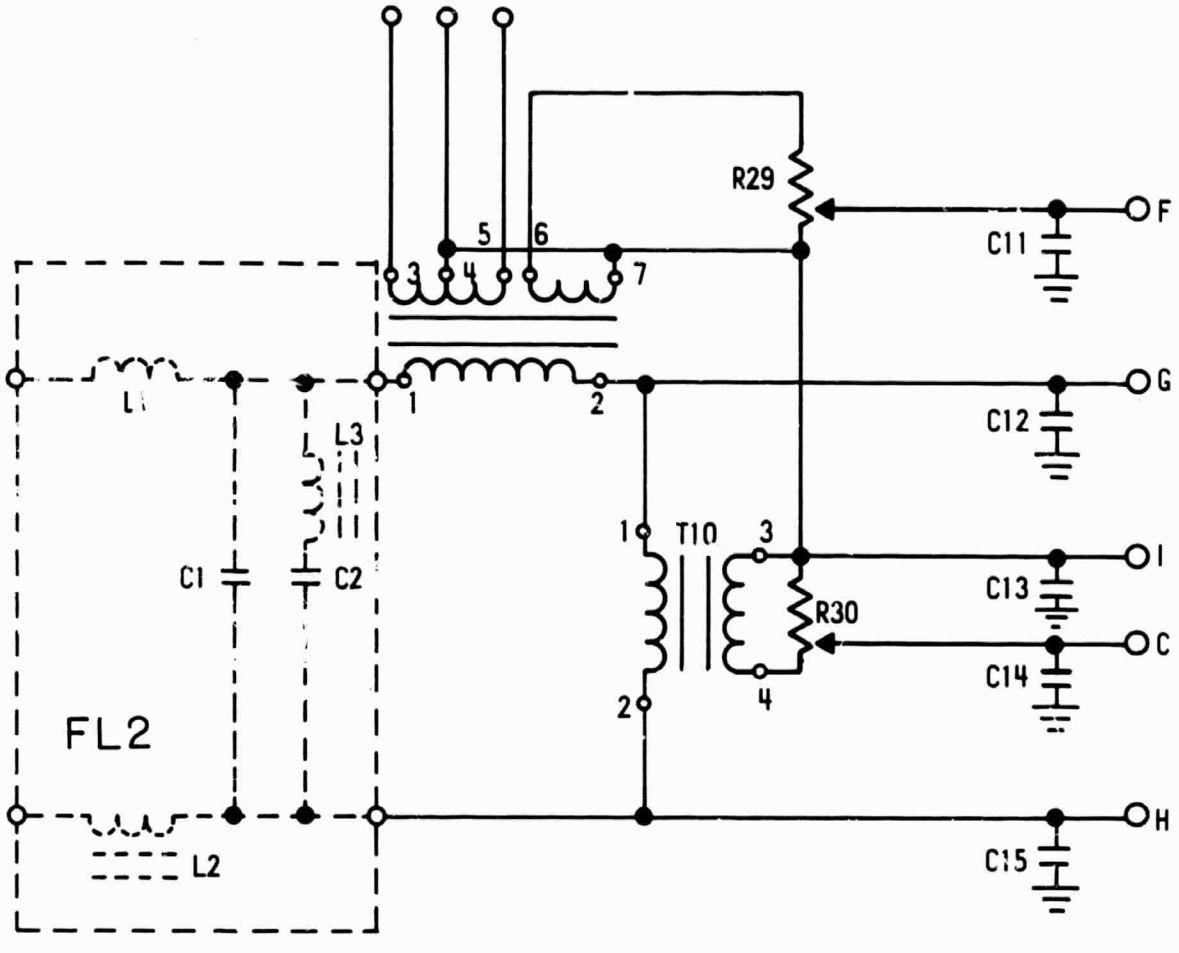


FIGURE 38
OUTPUT NETWORK

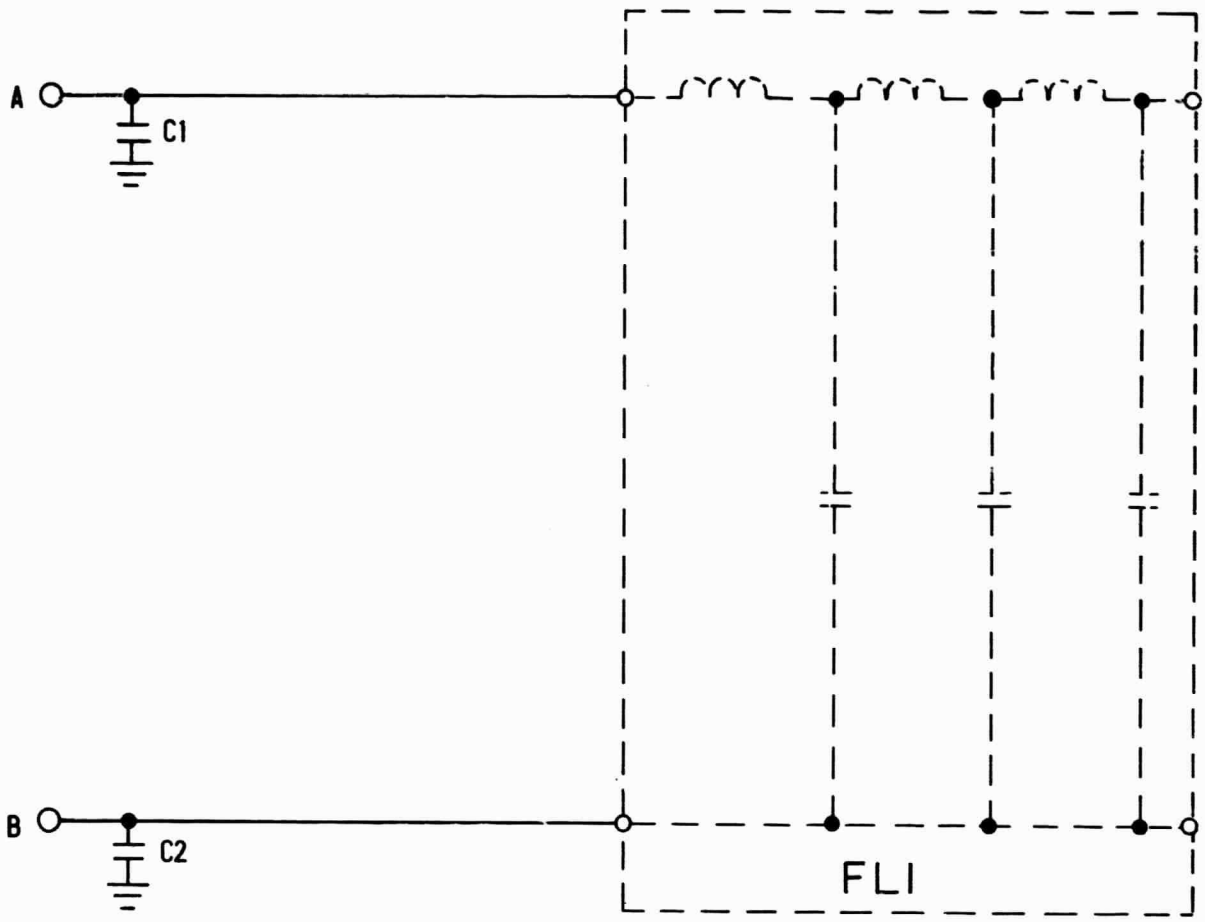


FIGURE 39
INPUT FILTER

the primary RFI filter with bypass capacitors for additional safety. The input, as well as the output, filter must be located as close as possible to the connector to provide maximum efficiency in the reduction of RFI.)

8. Voltage and Sensing

Sensing functions are performed by a set of transformers to provide isolation between input and output. Voltage transformer T10 and current transformer T9 are shown in Figure 38.

The voltage sensing transformer is a 400-Hz step-down transformer. Output of the transformer is connected to output terminals I and C through voltage adjustment resistor R30. The output of terminal I and C is set at 2.5 volts peak-to-peak with 115 volts from the inverter. This setting is a requirement for the three-phase operation to be discussed later. In normal operation this output signal is fed directly back into the inverter at terminal D. Since terminal I is the internal control ground lead, it does not require reconnecting.

The current-sensing transformer has two secondary windings. Windings 6-7 is used for parallel operation which is discussed in the next section.

Windings 3-4 and 4-5 provide overload protection for the inverter. Terminal 4 is connected to ground line while terminals 3 and 5 are connected to the overload circuit (Figure 25). Diodes CR3 and CR4 rectify the AC voltage to form a DC level proportional to the output current level. Zener diode CR2 in the emitter of transistor Q3 keeps the transistor biased OFF in normal operation. When the output current exceeds the predetermined level set by R7, however, transistor Q2 turns ON, turning transistor Q1 OFF and reducing the supply voltage to the 400-Hz reference amplifier transistor, Q2. This action reduces the output of the filter which forms the sine wave reference for the differential amplifier and, in turn, controls the reference comparators. Reduction in the reference sine wave reduces the output voltage of the inverter proportionately.

9. 120-Degree Phase Shift

For three-phase operation, the desired phase shift is obtained by use of an operational amplifier with reactive feedback. Figure 40a shows the

basic circuit.

Because of the high open-loop gain of the operational amplifier, Ig, the amplifier input current can be assumed to be zero, and the junction of R_1, R_2 can be assumed to be at ground potential.

The gain of the overall circuit is $\frac{eo}{ei}$ and, by Kirchoff's current, low:

$$I_i = I_f \tag{1}$$

therefore, $$\frac{ei}{Z_i} = - \frac{eo}{Z_f} \tag{2}$$

and $$\frac{eo}{ei} = - \frac{Z_f}{Z_i} \tag{3}$$

where Z_i is the total input impedance

Z_f is the total feedback impedance.

For the circuit in Figure 40a

$$Z_f = \frac{\frac{R_2}{jwc}}{R_2 + \frac{1}{jwc}} = \frac{R_2}{1 + jwR_2C} \tag{4}$$

$$Z_i = R_1 \tag{5}$$

and $$\frac{eo}{ei} = \left(\frac{R_1}{R_2}\right) \frac{1}{\sqrt{1 + w^2R_2^2C^2}} \angle - \tan^{-1} WR_2C \tag{6}$$

Let $$\left(\frac{R_1}{R_2}\right) \frac{1}{\sqrt{1 + W^2R_2^2C^2}} = 1 \tag{7}$$

$$\angle - \tan^{-1} WR_2C = 60^\circ \tag{8}$$

If the conditions of equations (7) and (8) are met, the 180-degree phase shift of the amplifier and the feedback network give a total phase shift for 120 degrees and an absolute gain of 1 for the circuit.

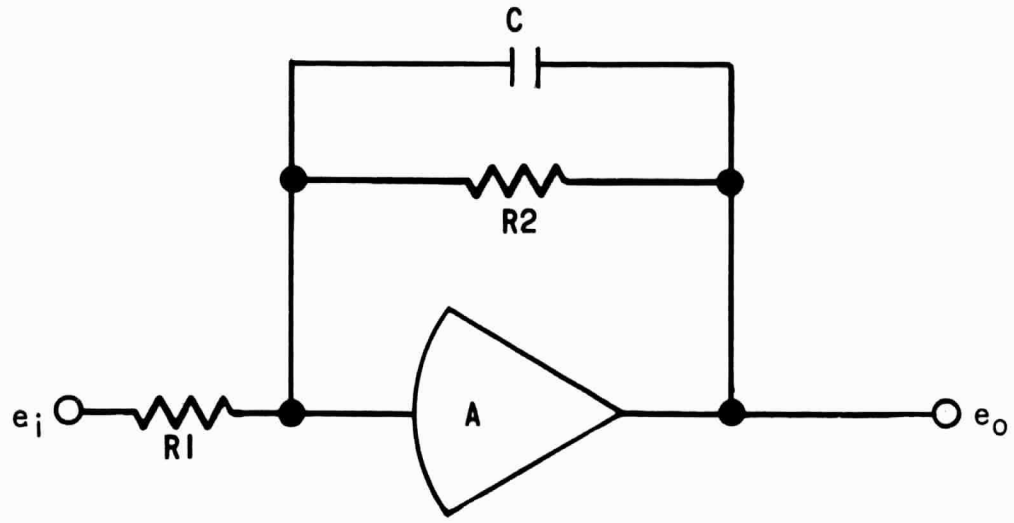
The circuit of Figure 40b is a 120-degree phase-shift circuit which operates on the above principle. It is utilized in the inverter to generate the required 120-degree phase shift for three-phase operation.

C. THREE-PHASE AND PARALLEL OPERATION

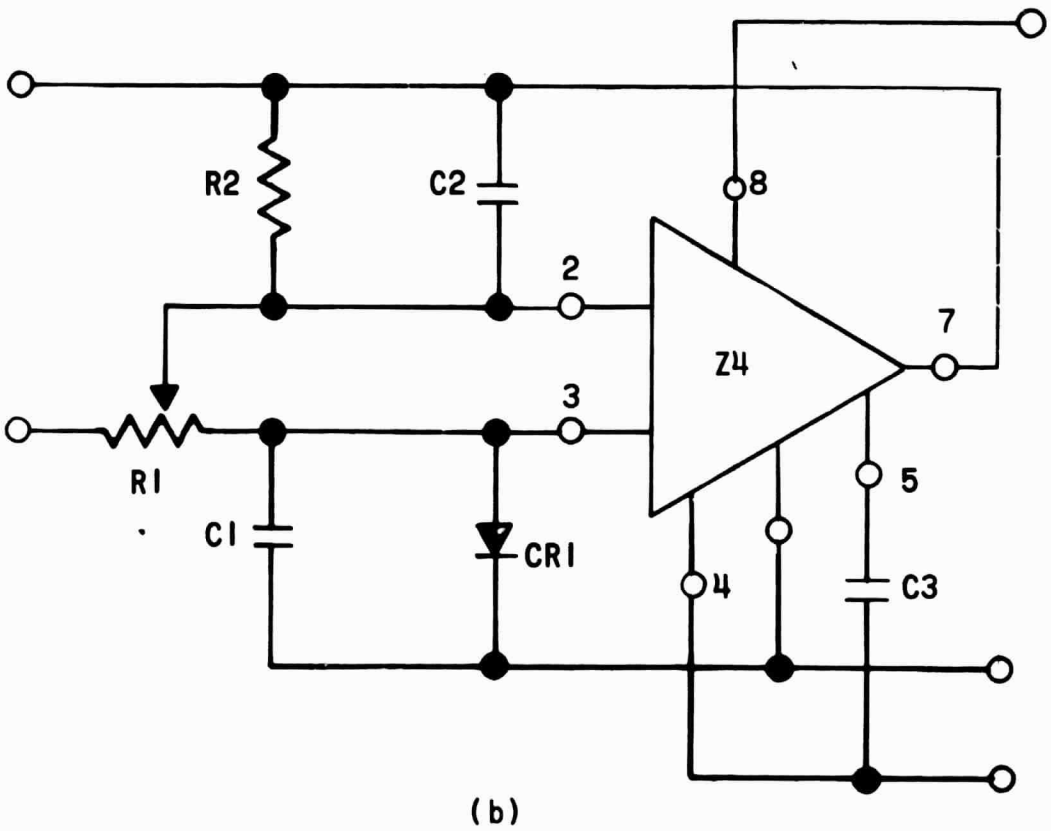
The high-frequency operation of the reference comparator and the simple low-pass filter makes three-phase and/or parallel operation of the inverter a simple task. The inverter acts in many ways like a low-frequency linear amplifier. The differential amplifier compares the output voltage to the reference voltage to ensure that the output has the same form as the reference voltage. The output can only be as good as the reference voltage and has the same form as the reference. If a squarewave is used as a reference, then the inverter puts out a squarewave, or if the reference is a triangular wave then the output is triangular.

To show how this reference is utilized in three-phase operation, three inverters are used. Inverter A supplies the A-phase voltage; Inverter B, the B-phase voltage; and Inverter C, the C-Phase voltage. In inverter A, the output of the filter network, terminal J, is connected to the input of the differential amplifier, terminal E. Terminal J is also connected to the input of the phase shift circuit, terminal K. The output of the phase-shift circuit, terminal L, is connected to terminal E and to terminal K of inverter B. The output of inverter B's phase-shift circuit, terminal L, is connected to terminal E and to terminal K of inverter C. The input reference voltage to each of the differential amplifiers, terminal E, is illustrated in Figure 41. The phase angle between these three waveforms determines the output phase angle. Terminals I of all three inverters are connected together. Terminal C of each inverter is connected to terminal D of that inverter. These basic connections for three-phase operation are illustrated in Figure 42.

With the connections as described and illustrated, inverter A produces what is termed phase-A output, and is at zero degrees. Interconnection I is a ground connection for the control sections. The output of terminal L of inverter A is a reference voltage for inverter B and has a phase angle of 120 degrees with respect to inverter A. This 120-degree reference signal is used by the inverter



(a)



(b)

FIGURE 40
PHASE-SHIFT CIRCUIT

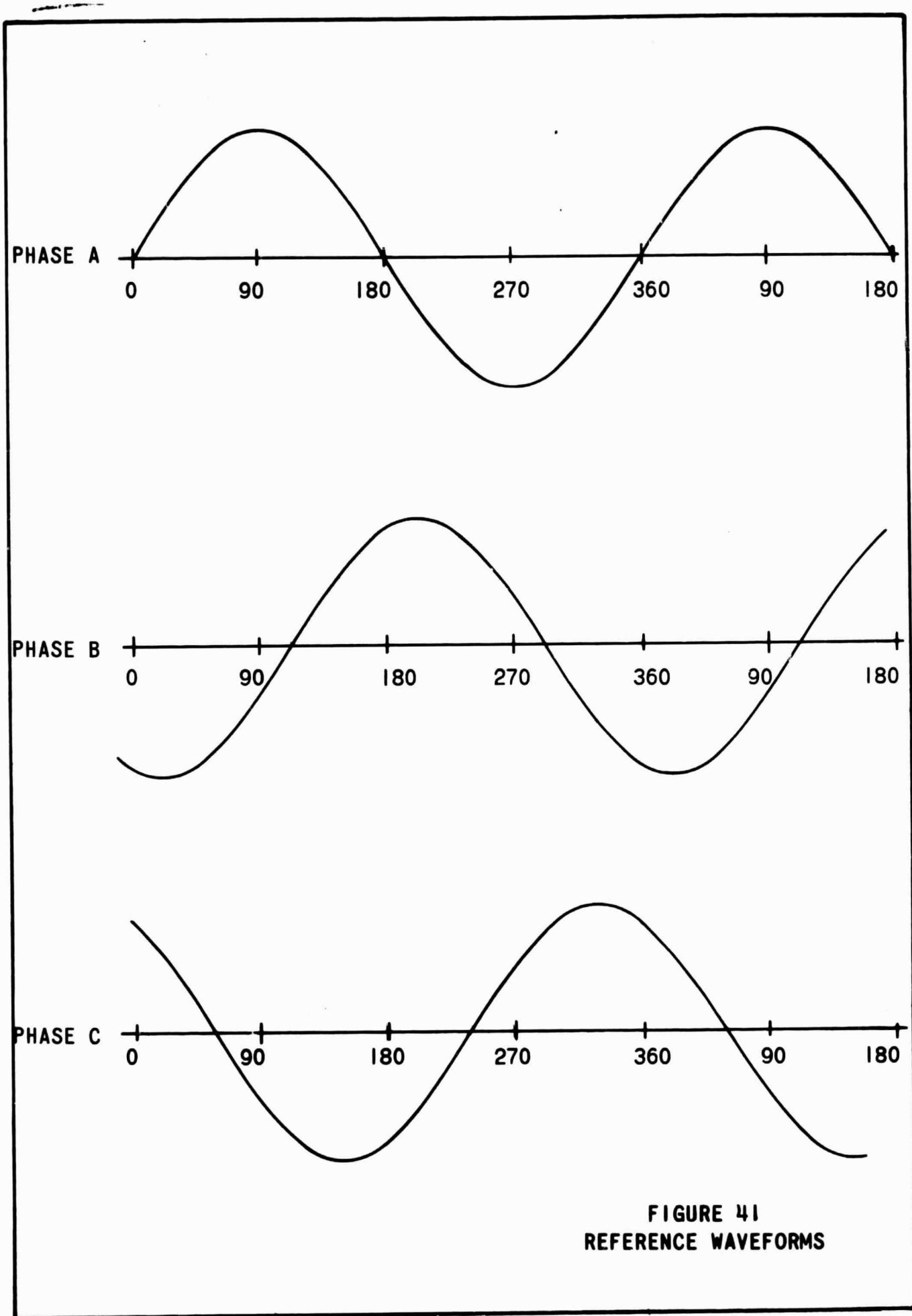


FIGURE 41
REFERENCE WAVEFORMS

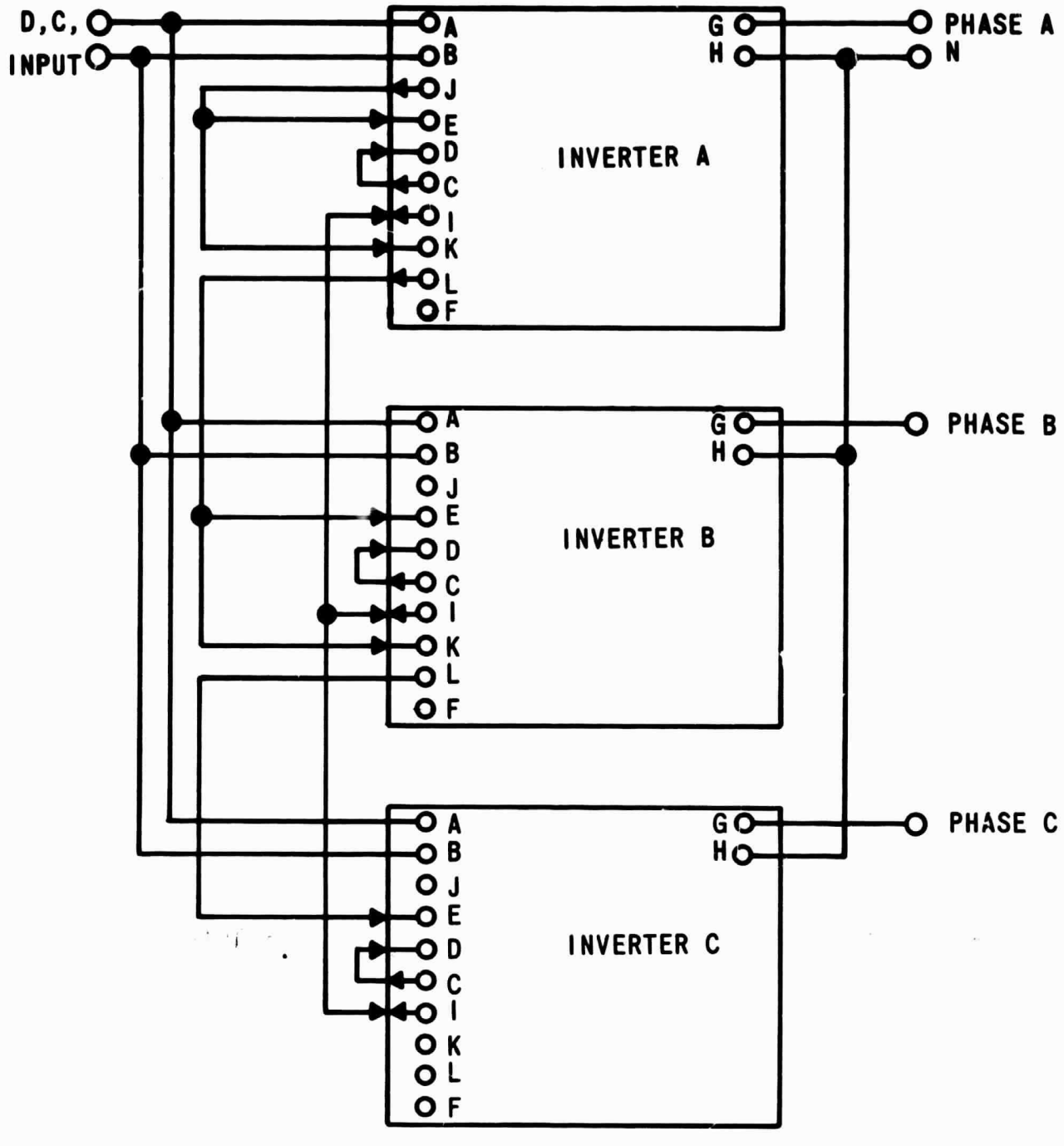


FIGURE 42
THREE-PHASE INTERCONNECTIONS

B reference comparator, terminal E, to produce phase B. The phase-shift circuit of inverter B, terminal L, produces a reference voltage for inverter C and has a phase angle of 120 degrees with respect to inverter B, or 240 degrees with respect to inverter A.

Paralleling of inverters is accomplished in a similar manner. The required interconnections are illustrated in Figure 43. For this discussion, two inverters are used. Inverter A is connected for standard single-phase operation. Inverter A produces a reference voltage, terminal F, for inverter A-1. This reference voltage is a function of the output current of inverter A as developed by current transformer T9. This reference voltage is the input to the differential amplifier of inverter A-1. The output current of inverter A-1 is then sensed by transformer T9 and a feedback voltage is developed which is a function of its output. This voltage is used for the second input of the differential amplifer. Thus, inverter A is a voltage source while inverter A-1 is a current source with its output current determined by the output current of inverter A.

The output power of the three-phase system (Figure 42) could be doubled by paralleling each of the phase inverters with a second inverter as illustrated in Figure 43. A three-phase parallel system is illustrated in Figure 44. To accomplish the described interconnections without readjustment of the various control functions in the inverters has required several additional components. Figure 16, shows that the voltage-sensing transformer T10 and current transformer T9 have output voltage adjustments in the form of variable resistors R29 and R30. Outputs of these two circuits are adjusted to provide 2.5 volts peak-to-peak under normal load voltage conditions. This voltage output matches that of the output of the sine wave reference terminals -- also 2.5 volts peak-to-peak. The differential amplifier is set up through R7 so that the inverter provides the correct output voltage when 2.5 volts are applied to its dual inputs. The 120-degree phase-shift network output is adjusted through R1 so that its output amplitude is the same as its input amplitude except that it is phase shifted 120 degrees. By having all the basic outputs and inputs set at a predetermined condition for all inverters, then the control signal between inverters may be mixed readily. This arrangement makes paralleling and three-phase operation possible without readjustment of the control circuits.

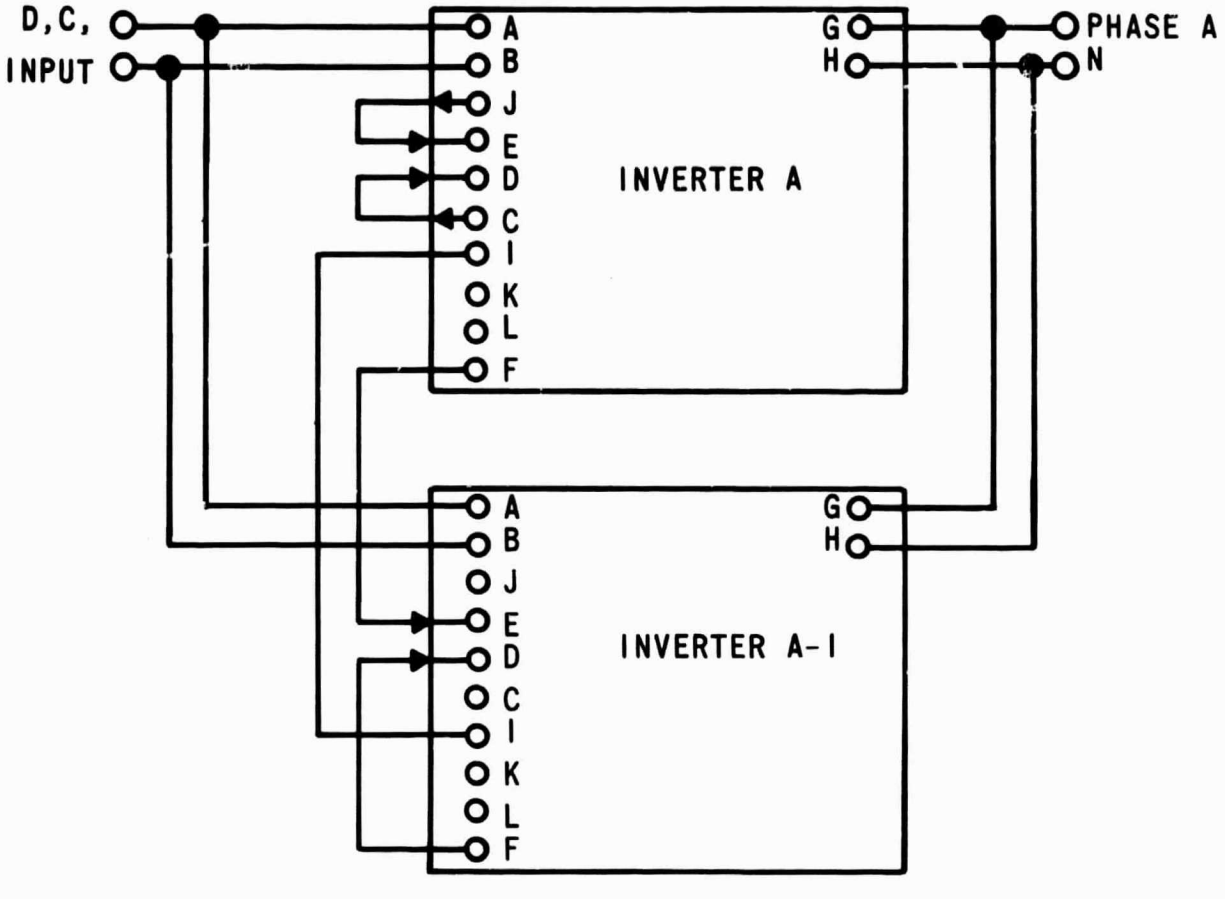


FIGURE 43
PARALLEL INTERCONNECTIONS

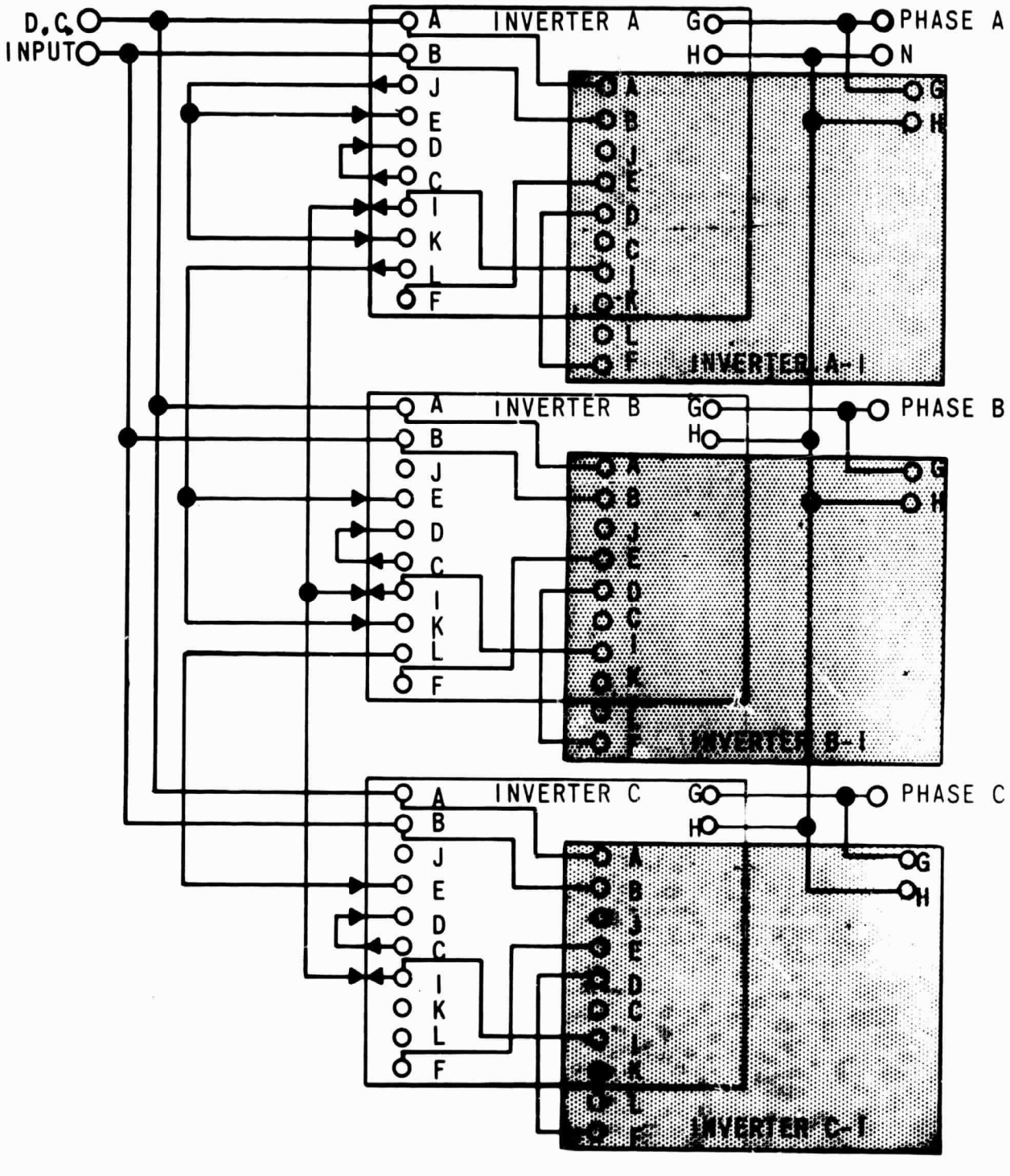


FIGURE 44
THREE-PHASE
PARALLEL INTERCONNECTIONS

IV DESIGN ANALYSIS AND CONSIDERATIONS

This section of the report covers major design and circuit considerations given in the selection of the final configuration as illustrated in the Schematic Diagram, Figure 16. It is not intended to be a complete and detailed design analysis, but only a guide to various design and components considerations.

A. BASIC DESIGN CONSIDERATION

The versatility of the Phase-Demodulated High-Frequency Inverter offers several basic designs which could have been utilized in the final design. Several are presently being used in other hardware development programs (Appendix B).

The first design given consideration is the Phase-Demodulated High-Frequency Inverter-- the basic design as outlined in the state-of-the-art study. It is one of the simpler approaches, but has two basic disadvantages: it has a much higher harmonic content that the other designs, and voltage stresses on the demodulator transistors require them to be series connected to overcome these stresses.

The second design considered reduces harmonic content and filter requirements. The Phase-Shifted Phase-Demodulator High-Frequency Inverter design uses two standard Phase-Demodulator Inverters which have the outputs of their power-switching stages series connected, and one phase shifted 90 degrees with respect to the other. This arrangement produces a wave similar to that of Figure 12a except that the frequency of the modulated pulse is four times the power-switching stage and not two times as in the standard unit. The basic disadvantage of this arrangement is the requirement for two inverters to obtain one output, thus making the unit much more complex. In the higher power units the disadvantage of the more complex control section may be minor when compared with the weight-saving made through reduced filtering requirements.

The third design considered is the Phase-Demodulated High-Frequency Bridge Inverter. The basic advantage of this circuit is the improved modulated waveform illustrated in Figure 12a. This waveform only doubles the power stage switching frequency; however, it is much simpler than the phase-shifted circuit.

Also, the method of regulation provides the same response as the phase-shifted circuit. As will be described in the waveform analysis, this waveform has both edges modulated vs. only trailing edge modulation for the 90-degree phase-shifted circuit. At the same modulation frequency, a double edge modulated waveform has fewer harmonics present than the single edge modulated waveform. Also, the amplitude of the harmonics voltages present is less.

The fourth design considered is a combination of the second and third. This design is recommended only because of its extremely high power inverters. In this concept, the power stage of two series-connected Phase-Demodulated Bridge Inverters are phase shifted. The output of this design is a double edge modulated waveform that more closely approximates a sine wave as illustrated in Figure 45. Inspection of Figure 45 shows the improvements gained with this circuit. The pulses present are at a frequency rate four times that of the power stage. The disadvantage is that of complex and added circuitry which must be weighed with each power level and application.

B. PULSE-WIDTH MODULATION ANALYSIS

This is one of the most important sections of the report, although it does not relate to the detailed circuit design. The analysis provides a fundamental understanding of the Phase-Demodulated Inverter concept. The analysis is on a waveform basis and not an inverter design basis. Analysis of this waveform is difficult and can be very complicated if not approached correctly. One of the most important steps is the development of the basic equations. If the equations are not developed correctly and do not describe the pulse-width modulated waveform, then incorrect data will result. A very practical approach which may be used to analyze this type waveform is explained by H. S. Black [208]. An expansion of this basic approach is utilized in the waveform analysis.

In pulse-width modulation a train of pulses is modulated by the value of each instantaneous sample of the continuously varying modulating wave which produces a pulse of proportional width. The modulating wave may vary the position with time of the leading edge, the trailing edge, or both edges of the pulses. There are two types of sampling associated with pulse-width modulation—uniform and natural.

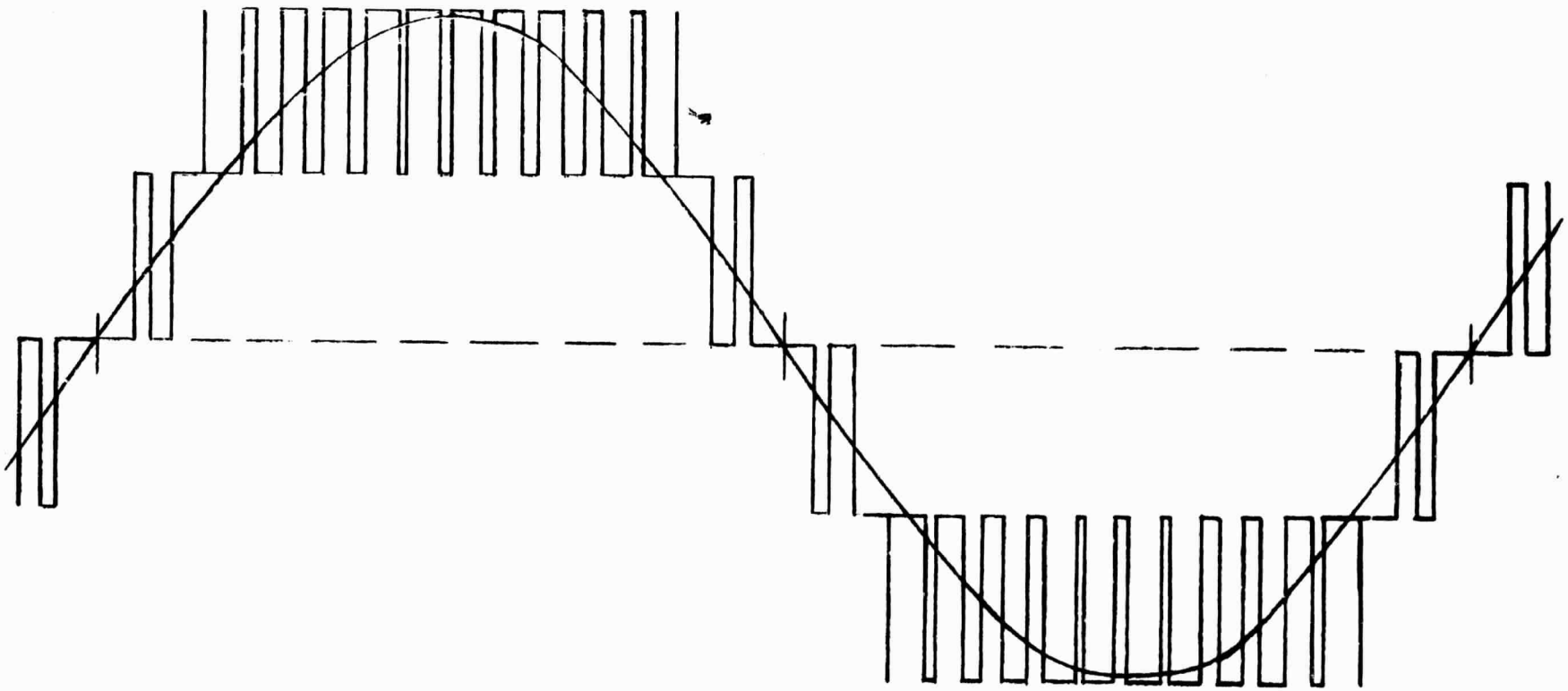


FIGURE 45
OUTPUT WAVEFORM OF TWO SERIES-CONNECTED PHASE-DEMODULATED BRIDGE INVERTERS

In uniform sampling, the modulation is such that the pulse width is proportional to the instantaneous value of the modulating wave at equally spaced sampling times.

With natural sampling, the pulse width is proportional to the average value of the modulating waveform during the sampling interval. Natural sampling, as used in the the Phase-Demodulated High-Frequency Inverter, is illustrated and developed in the waveforms of Figure 30.

The difference between natural and uniform sampling is that natural sampling yields a spectrum that has no lower harmonics of the modulating frequency (fv). This means that the spectra of a pulse-width modulated waveform employing natural sampling is void of lower harmonics (2fv, 3fv, 4fv, etc.) and the lowest harmonics are sidebands of the carrier frequency. An inverter using natural sampling has a distinct advantage due to the lessened filtering requirements; therefore, only natural sampling is discussed in detail.

In literature on modulation, pulse-width modulation is often called pulse-duration or pulse-length modulation. In this disucssion of the subject the term pulse-width modulation is adhered to.

Natural sampling may be divided into two groups or methods of modulation: single edge modulation and double edge modulation. In single edge modulation only one edge of a pulse, leading or trailing, is modulated by the modulating signal. In double edge modulation both the leading edge and trailing edge are modulated. The frequency spectrum of the two types of natural sampling are as different as natural sampling and uniform sampling.

Single edge modulation is discussed first because development of its equation helps in development of the equation for double edge modulation. A single edge modulated waveform is illustrated in Figure 12b, page 30. This waveform can be analyzed by a double Fourier series method and is covered in detail by Black.[208] In Black's discussion, Chapter 17, two equations are derived that describe the spectra of a pulse-width modulated waveform - one for natural sampling and the other for uniform sampling. The double Fourier series for pulse-width modulated pulses of unit height with trailing edges modulated by natural samples of a sinusoidal modulating wave is

$$F_1(t) = K + \frac{M}{2} \cos w_v t + \sum_{m=1}^{\infty} \frac{\sin m w_c t}{m\pi} \sum_{m=1}^{\infty} \frac{Jo(mM\pi)}{m\pi} \sin(mw_c t - 2mK\pi)$$

$$- \sum_{m=1}^{\infty} \sum_{m=\pm 1}^{m=\pm \infty} \frac{Jn(mM\pi)}{m\pi} \sin(w_c t + nw_v t - 2mK\pi - \frac{m\pi}{2})$$

where K is the DC component of the pulses

M is the modulation index $0 \leq M \leq 1$

w_v is the angular modulating frequency $w_v = 2\pi f_v$

w_c is the angular carrier frequency $w_c = 2\pi$ (Number of pulses/sec.)

n is the number of the harmonic of the modulating frequency

m is the number of the harmonic of the carrier or pulse frequency

Jo(mMπ) and Jn(mMπ) are bessel functions of the first kind.

The major problem in developing this equation is relating the modulating frequency to the output frequency. A procedure developed by W. R. Bennett[210] and explained by Black is outlined through the use of Figure 46. The modulating wave is represented by A cos $w_v t$ traveling in the Y axis of Figure 46a. The high-frequency wave travels the X axis, a leading edge at 2π intervals at a frequency of w_c.

If line OZ is passed through the modulating wave and the modulating wave is repeated at w_c (Figure 46a), the modulated wave of Figure 46b may be developed by projecting from Figure a to b the leading edge of high-frequency wave w_c and the intersecting point of A cos $w_v t$ and the line OZ. The equation for the pulses in Figure 46b may be written

$$X' = B + A \cos Y.$$

To represent the complete train of pulses, the basic dimension X and Y and A and B must be related to time, and the above basic equation expanded to include the train of pulses. The basic time equations are

$$X = w_c t$$
$$Y = w_v t$$
$$B = 2K$$
$$M = A/\pi$$

The slope of line OZ is Y/X or w_v/w_c and relates the two frequencies. Function K is the ratio in the absence of modulation, of the pulse width to the pulse rate. In this example $K = \pi/2 = 1/2$ such that $B = \pi$. M is the modulation index and represents the limit of the amplitude of the modulating wave in Figure 46a. In the equation $A \cos w_v t$, A has a maximum limit of π, so that M has a maximum value of one.

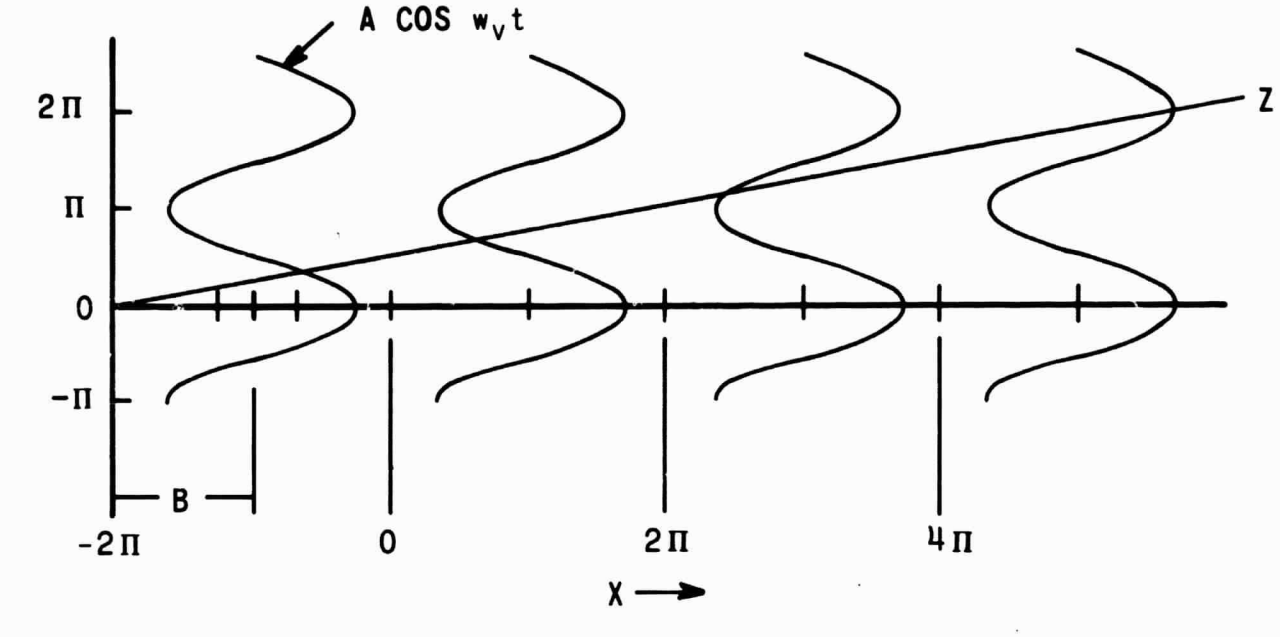
Figure 46 and the above discussion are presented only to illustrate how terms in the modulation equation were defined. Complete derivation of the single edge modulation equation is presented by Black; however, the above discussion helps in the evaluation below of the equation.

From Figure 46 it is seen that the DC component of the waveform is one-half when K is one-half and the pulse is of unit height. The equation for the spectra of width modulated pulses with trailing edges modulated by natural samples of a sinusoidal modulating wave then becomes

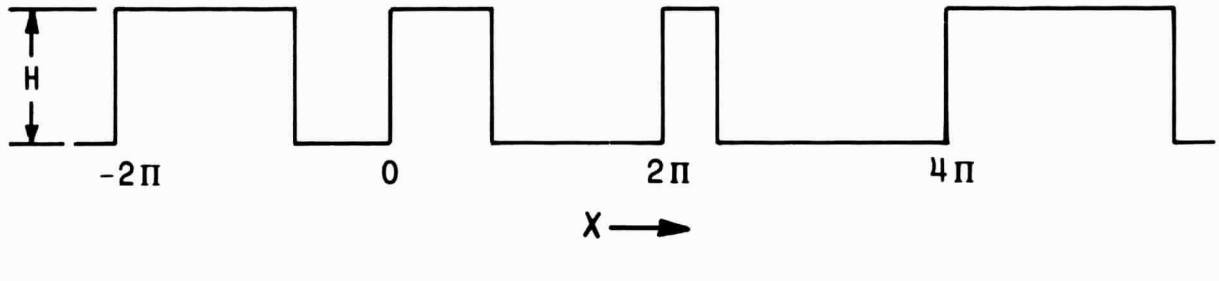
$$F(t) = \frac{1}{2} + \frac{M}{2} \cos w_v t + \sum_{m=1}^{\infty} \frac{\sin (m w_c t}{m\pi} - \sum_{m=1}^{\infty} \frac{Jo(mM\pi)}{m\pi} \sin (m w_c t - m\pi)$$

$$+ \sum_{m=1}^{\infty} \sum_{n=\pm 1}^{n=\pm\infty} \frac{Jn(mM\pi)}{m\pi} \left[\begin{array}{l} \sin(mw_c t + nw_v t) \cos m\pi \cos \frac{n\pi}{2} \\ -\cos(mw_c t + nw_v t) \cos m\pi \sin \frac{n\pi}{2} \end{array} \right]$$

The first term is the modulation or power component and is directly proportional to the value of the modulation index. The second and third terms are the dundamental and harmonics of the carrier frequency. The carrier frequency is defined as 2π times the number of pulses per second. The fo ı term is the sideband components formed by the beating of the fundamentals and harmonics of the carrier and power frequencies. The following sample calculations illustrate the use of this equation.



(a)



(b)

FIGURE 46
SINGLE EDGE MODULATION

SAMPLE CALCULATIONS:

The equation is multiplied by 2 to give the power frequency component a peak value of one unit.

$$M = \frac{\text{Maximum pulse width-change in pulse width}}{\text{Maximum pulse width}}$$

For M = 1

$m = 1 \quad f_v = \frac{w_v}{2\pi} = 400 \text{ cps}$

$n = 1 \quad f_c = \frac{w_c}{2\pi} = 6400 \text{ cps}$

$fw_c = M \cos w_c t$

$fw_v = f400 \text{ cps} = 1$ (This is the peak amplitude relative to the peak magnitude of the pulses.)

$$fw_c = 2\sum_{m=1}^{\infty} \frac{\sin (mw_c t)}{m\pi} - 2\sum_{m=1}^{\infty} \frac{Jo(mM\pi)}{m\pi} \sin (mw_c t - m\pi)$$

$$f6400 \text{ cps} = \frac{\sin w_c t}{3.14} - \frac{Jo\,(3.14)}{3.14} \sin (w_c t - 180)$$

Let $w_c t = 90^\circ$ (This assumption will result in maximum amplitude of the harmonics.)

f6400 cps = 0.444 (This is the peak amplitude relative to the peak magnitude of the pulses.)

$$fmw_c \pm nw_v = 2\sum_{m=1}^{\infty} \sum_{n=\pm 1}^{n=\pm\infty} \frac{Jn(mM\pi)}{m\pi} \left[\begin{array}{l} \sin(mw_c t + nw_v t) \\ \quad \cos m\pi \cos \frac{m\pi}{2} \\ -\cos (mw_c t + nw_v t) \\ \quad \cos m\pi \sin \frac{n\pi}{2} \end{array} \right]$$

Let $w_c t + w_v t = 90^\circ$

$$f6Kc,\ 6.8Kc = 2\,\frac{J_1\ (3.14)}{3.14} = 0.192$$ (This is the peak amplitude relative to the peak magnitude of the pulses.)

Table 3 illustrates data calculated for a pulse-width modulated waveform with the trailing edge modulated by natural samples of a sinusoidal wave. The calculated data is compared with data measured in the laboratory for a modulation index of 0.9 (Table 4.) This data correlation demonstrates that the relative amplitudes of the power frequency, carrier frequency and sideband frequencies are independent of the modulating frequency and the carrier frequency. This is true for a power frequency of 60 cps or 400 cps.

Increasing the ratio of the carrier frequency to the power frequency shifts the relative amplitudes of the carrier and sideband frequencies farther up the frequency scale. Generally speaking, the carrier frequency should be made as high as the circuitry permits to reduce the output filtering problem.

The frequency spectrum of a pulse-width modulated waveform with the trailing edge modulated and a modulation index of unity is illustrated in Figure 47. This data, along with Table 3, provides the detailed information necessary for a comprehensive output filter design. It not only lists the harmonics present, but also gives their amplitude relative to the amount of modulation. Comparison of the amplitude of fundamental frequency fv with harmonic amplitude fc shows that at a modulation index of 0.7 the amplitude of the harmonic is as large as the fundamental. This comparison is illustrated in Figure 48 for a few of the major harmonics. If the two frequencies, fv and fc, are not well separated, the output filter design becomes very difficult.

The preceding equation becomes the double Fourier series for width modulated pulses with leading edges modulated by natural samples of a sinusoidal modulating wave if a negative sign is put in front of the t. The negative sign in front of the t reverses the time scale and the modulated trailing edges become the modulated leading edges. The equation then becomes:

$$F_2(-t) = K + \frac{M}{2}\cos(-w_v t) + \sum_{m=1}^{\infty} \frac{\sin(-mw_c t)}{m\pi} \sum_{m=1}^{\infty} -\frac{Jo(mM\pi)}{m\pi} \sin(-mw_c t - 2mK\pi)$$

$$-\sum_{m=1}^{\infty} \sum_{n=\pm 1}^{n=\pm\infty} \frac{Jn(mM\pi)}{m\pi} \sin(-mw_c t - nw_c t - 2mK\pi - \frac{n\pi}{2}).$$

TABLE 3

CALCULATED AMPLITUDE DISTRIBUTION OF A TRAILING EDGE MODULATED WAVEFORM VS MODULATION INDEX

FREQUENCY	RELATIVE AMPLITUDE MODULATION INDEX (M)					
	1.0	0.9	0.8	0.7	0.6	0.5
f_v	100.0	90.0	80.0	70.0	60.0	50.0
$1f_c$	44.4	51.4	60.4	70.6	82.0	93.4
$2f_c$	24.8	29.8	37.6	42.6	44.4	41.0
$3f_c$	17.4	23.0	26.6	26.8	22.4	15.5
$4f_c$	13.4	17.6	20.0	16.6	11.7	12.5
$5f_c$	11.0	13.5	14.6	10.5	10.4	15.2
$f_c \pm f_v$	19.2	20.0	31.8	35.6	37.0	36.2
$f_c \pm 2f_v$	31.2	30.6	28.6	25.4	21.0	16.5
$f_c \pm 3f_v$	21.0	16.2	14.0	10.2	7.0	4.64
$f_c \pm 4f_v$	9.2	6.8	4.72	9.55	1.78	0.94
$f_c \pm 5f_v$	2.74	2.74	2.74	0.44	-----	-----
$2f_c \pm 1f_v$	6.68	10.2	10.5	6.46	0.42	9.6
$2f_c \pm 2f_v$	7.64	8.26	1.5	7.96	13.0	15.8
$2f_c \pm 3f_v$	3.6	7.32	11.7	13.7	13.4	10.5
$2f_c \pm 4f_v$	11.5	11.8	12.4	10.8	7.96	4.76
$2f_c \pm 5f_v$	11.4	9.86	8.26	5.72	3.5	1.58
$2f_c \pm 6f_v$	8.0	6.04	4.14	2.6	1.27	0.44
$3f_c \pm 1f_v$	3.82	5.72	2.86	2.76	6.8	5.92
$3f_c \pm 2f_v$	4.04	2.54	4.24	5.9	3.4	3.18
$3f_c \pm 3f_v$	1.92	5.1	4.88	3.1	3.8	8.7
$3f_c \pm 4f_v$	5.1	4.04	2.54	3.82	7.84	7.84
$3f_c \pm 5f_v$	2.76	1.49	5.72	7.42	7.0	5.53
$3f_c \pm 6f_v$	2.54	5.72	7.0	7.2	5.0	2.76

$f_v = 400$
$f_c = 6400$

TABLE 4

CALCULATED VS MEASURED AMPLITUDE DISTRIBUTION
OF A TRAILING EDGE MODULATED WAVEFORM

FREQUENCY	RELATIVE AMPLITUDE				
	CALCULATED M = 0.9 f_v = 400 f_c = 6400	MEASURED M = 0.9 f_v = 400 f_c = 6400	MEASURED M = 0.9 f_v = 400 f_c = 4800	MEASURED M = 0.9 f_v = 400 f_c = 9600	MEASURED M = 0.9 f_v = 60 f_c = 9600
f_v	100.0%	100.0%	100.0%	100.0%	100.0%
f_c	57.2	56.	53.	63.	53.
$2f_c$	33.1	33.	32.	37.	32.
$3f_c$	25.6	24.	23.	27.	17.
$4f_c$	19.6	18.	18.	20.	21.
$5f_c$	15.0	15.	--	18.	20.
$f_c \pm f_v$	28.8	26.	25.	30.	24.
$f_c \pm f_v$	28.8	26.	27.	31.	24.
$f_c \pm 2f_v$	34.0	35.	32.	33.	33.
$f_c \pm 2f_v$	34.0	35.	27.	35.	33.
$f_c \pm 3f_v$	18.0	20.	20.	19.	21.
$f_c \pm 3f_v$	18.0	20.	20.	18.	21.
$2f_c \pm f_v$	11.3	10.	10.	10.	8.
$2f_c \pm f_v$	11.3	10.	10.	11.	8.

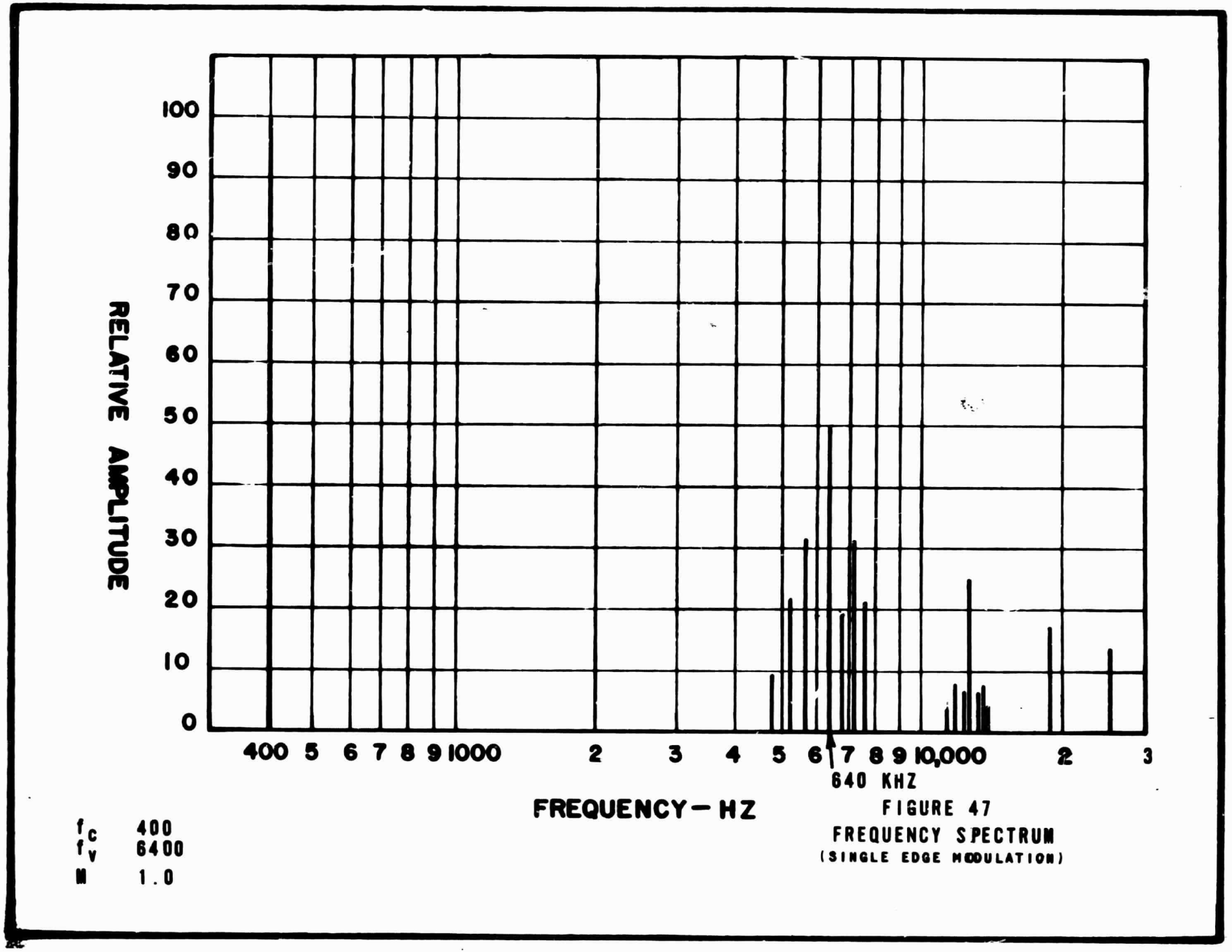
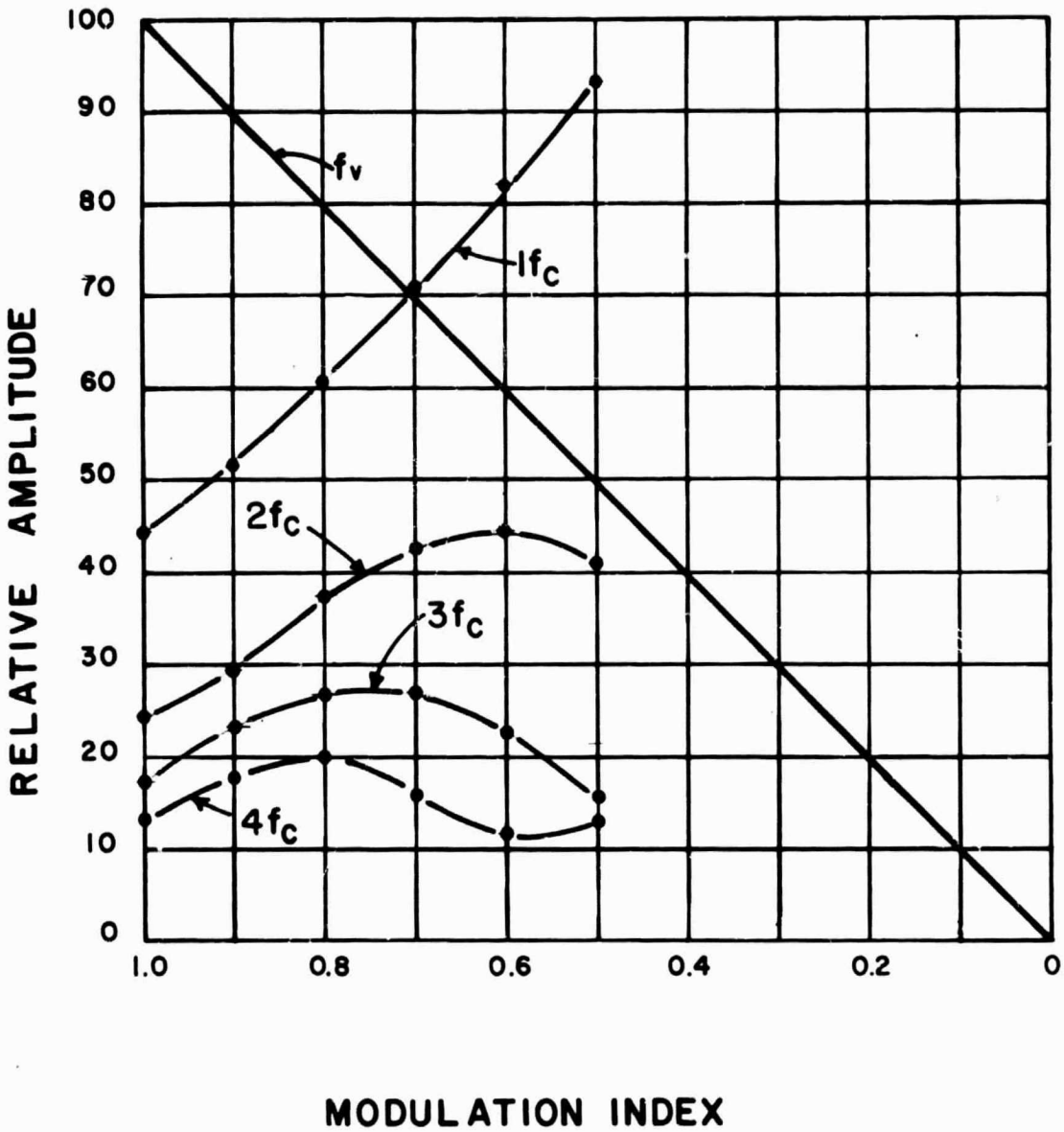


FIGURE 47
FREQUENCY SPECTRUM
(SINGLE EDGE MODULATION)



f_v = 400 HZ

f_c = 6400HZ

FIGURE 48
RELATIVE AMPLITUDE VS
MODULATION INDEX
(SINGLE EDGE)

For pulses with both edges modulated, the two preceding double Fourier series are added together because both series have the proper time relationship. The double Fourier series for width modulated pulses with both edges modulated becomes

$$F_3(t) = F_1(t) + F_2(-t).$$

Substituting in the equations for $F_1(t)$ and $F_2(-t)$ gives

$$F_3(t) = K + \frac{M}{2}\cos w_v t + \sum_{m=1}^{\infty}\frac{\sin m w_c t}{m\pi} - \sum_{m=1}^{\infty}\frac{Jo(mM\pi)}{m\pi}\sin\overset{(mw_c t,}{(-2mK)}$$

$$-\sum_{m=1}^{\infty}\sum_{n=\overset{+}{-}1}^{n=\overset{+}{-}\infty}\frac{Jn(mM\pi)}{m\pi}\sin\left(mw_c t + nw_v t - 2mK\pi - \frac{n\pi}{2}\right) + K$$

$$+\frac{M}{2}\cos(-w_v t) + \sum_{m=1}^{\infty}\frac{\sin(-mw_c t)}{m\pi} - \sum_{m=1}^{\infty}\frac{Jo(mM\pi)}{m\pi}\sin(mwct-2mK\pi)$$

$$-\sum_{m=1}^{\infty}\sum_{n=\overset{+}{-}1}^{n=\overset{+}{-}\infty}\frac{Jn(mM\pi)}{m\pi}\sin\left(-mw_c t - nw_v t - 2mK\pi - \frac{n\pi}{2}\right).$$

Using $\cos(w_v t) = \cos(-w_v t)$ and $\sin(1mw_c t) = -\sin(mw_c t)$

and combining terms gives

$$F_3(t) = 2K + M\cos w_v t - \sum_{m=1}^{\infty}\frac{Jo(mM\pi)}{m\pi}\left[\begin{matrix}\sin(mw_c t - 2mK\pi) \\ +\sin(-mw_c t - 2mK\pi)\end{matrix}\right]$$

$$-\sum_{m=1}^{\infty}\sum_{n=\overset{+}{-}1}^{n=\overset{+}{-}\infty}\frac{Jn(mM\pi)}{m\pi}\left[\begin{matrix}\sin\left(mw_c t + nw_v t - 2mK\pi - \frac{n\pi}{2}\right) \\ +\sin\left(-mw_c t - nw_v t - 2mK\pi - \frac{n\pi}{2}\right)\end{matrix}\right].$$

Using $\sin(A \overset{+}{-} B) = \sin A\cos B \overset{+}{-} \cos A\sin B$

simplifies to

$$F_3(t) = 2K + M \cos w_v t + 2 \sum_{m=1}^{\infty} \frac{Jo(mM\pi)}{m\pi} \cos mw_c t \sin 2mK\pi$$

$$+2 \sum_{m=1}^{\infty} \sum_{n=\pm 1}^{n=\pm\infty} \frac{Jn(mM\pi)}{m\pi} \cos (mw_c t + nw_v t) \sin (2mK\pi + \frac{n\pi}{2}) .$$

The DC component is zero; therefore, K = 0.

The equation then becomes

$$F_3(t) = M \cos (w_v t) + 2 \sum_{m=1}^{\infty} \frac{Jn(mM\pi)}{m} \cos (mw_c t + nw_v t) \sin (\frac{n\pi}{2})$$

$$n = \pm 1, \pm 3, \pm 5, \text{ etc.}$$

This equation could have been derived, as was the original equation, through the use of Figure 49. Inspection of this figure further illustrates the effect of double edge modulation. In this series of pulses the leading edge is being modulated as well as the trailing edge. Also, due to the method of defining the leading and trailing edge, the modulated waveform has a series of positive pulses and a series of negative pulses at the output frequency. Since double modulation is affected by the same basic waveform, the negative portion equals the positive, thus there is no DC or k factor.

It should also be noted that the positive and negative pulses have unit heights, thus the fundamental is twice that of the previous equation with the same input.

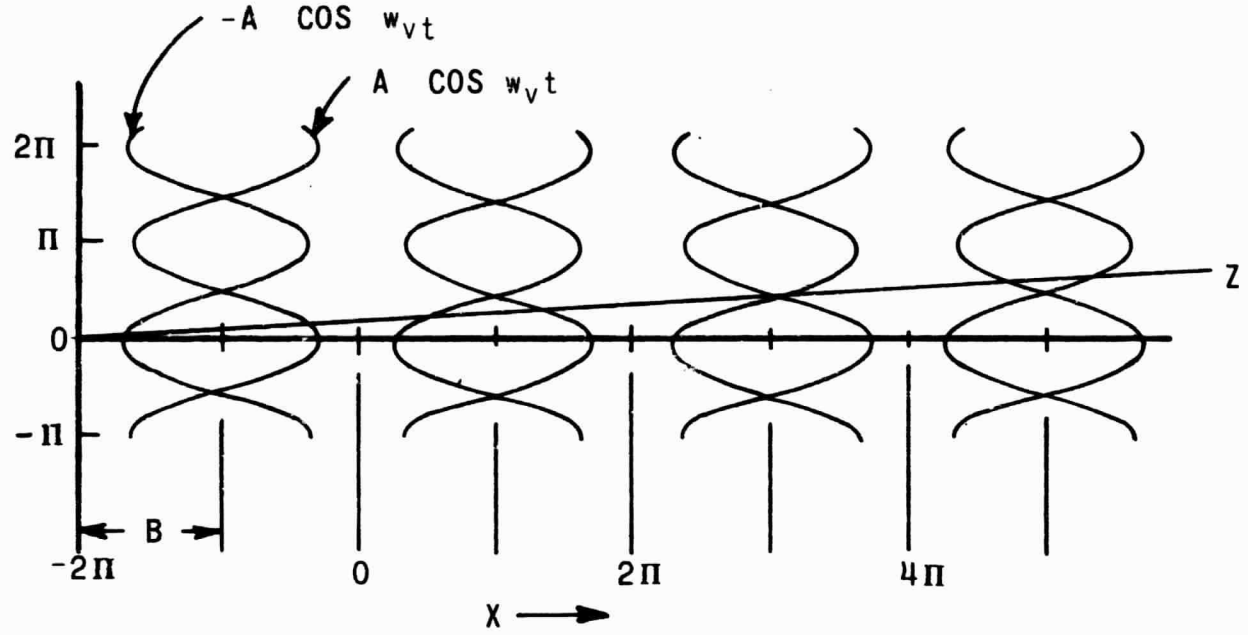
To further clarify this, the basic equation is written for Figure 49 as for Figure 46. Inspection of Figure 49 shows that the center of the pulse is not necessarily at the center of the carrier. The reason for this is more obvious from an inspection of line OZ and its intersection points into the two modulating waves. Since the leading edge is no longer fixed, a new equation must be written for the modulated waveform of Figure 49b. In general form this equation is:

$$X' = X_1' - X_2'$$

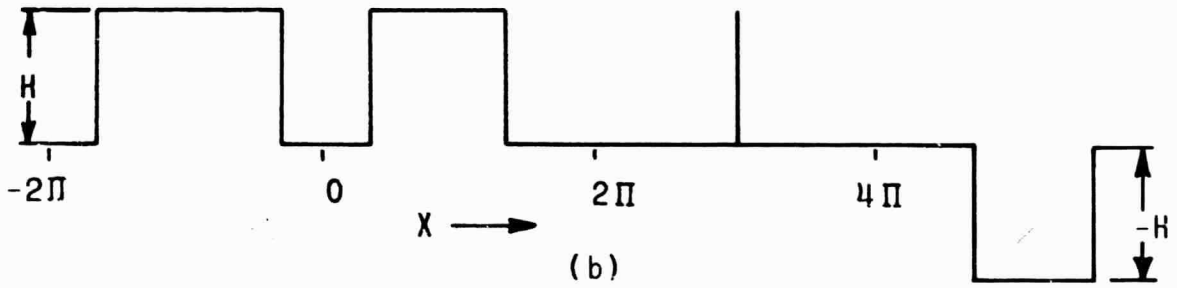
where X_1' defines the trailing edge and X_2' defines the leading edge and each can be defined by its own equation as

$$X_1' = B + A \cos w_v t$$

$$X_2' = B - A \cos wvt$$



(a)



(b)

FIGURE 49
DOUBLE EDGE MODULATION

therefore

$$X' = X_1' - X_2'$$

$$X' = B + A \cos w_v t - (B - A \cos w_v t)$$

$$X' = 2 A \cos w_v t.$$

Comparison of this equation for pulse width with that of the equation for single edge modulation helps to illustrate the basic differences in Black's derived equations. A sample calculation also illustrates the differences in the types of modulation. Also, inspection of Figure 49b shows that double edge modulation results in twice the frequency response as that of single edge modulation.

The first term is the modulating voltage, and it could be a sine or cosine term because the relative phase of the modulating signal affects only the relative phases of the components of the spectrum, not their magnitudes which are of chief interest here. The frequency components of the last term are given by the combination of all possible pairs formed by taking the sum and difference of integral multipliers of w_v and w_c. The absolute value of n gives a relative amplitude for both sidebands. When n is positive, an upper sideband component is defined such as $mw_c t + nw_v t$. When n is negative, a lower sideband component is defined such as $mw_c t - nw_v t$.

SAMPLE CALCULATION:

$$M = \frac{\text{Maximum pulse width - Change in pulse width}}{\text{Maximum pulse width}}$$

$M = 0.9$ $\qquad f_v = \frac{w_v}{2\pi} = 400$ cps

$$f_c = \frac{w_c}{2\pi} = 6400 \text{ cps}$$

$fw_v = M \cos w_v t$

f400 cps = 0.9 (This is the amplitude relative to the unit height of the pulses.)

$$fmw_v t \pm nw_v = 2 \sum_{m=1}^{\infty} \frac{Jn(mM\pi)}{m\pi} \cos (mw_c t + nw_v t) \sin\left(\frac{n\pi}{2}\right)$$

$n = \pm 1, \pm 2, \pm 3,$ etc.

$$fwc \pm w_v = 2\left[\frac{J_1(.9X3.14)}{3.14}\right] = 2\left[\frac{J_1(2.82)}{3.14}\right] = 0.637\left[0.4097\right] = 0.26.$$

This is the peak amplitude relative to the unit height of the pulses for the upper sideband $w_c + w_v$ and the lower sideband $w_c - w_v$.

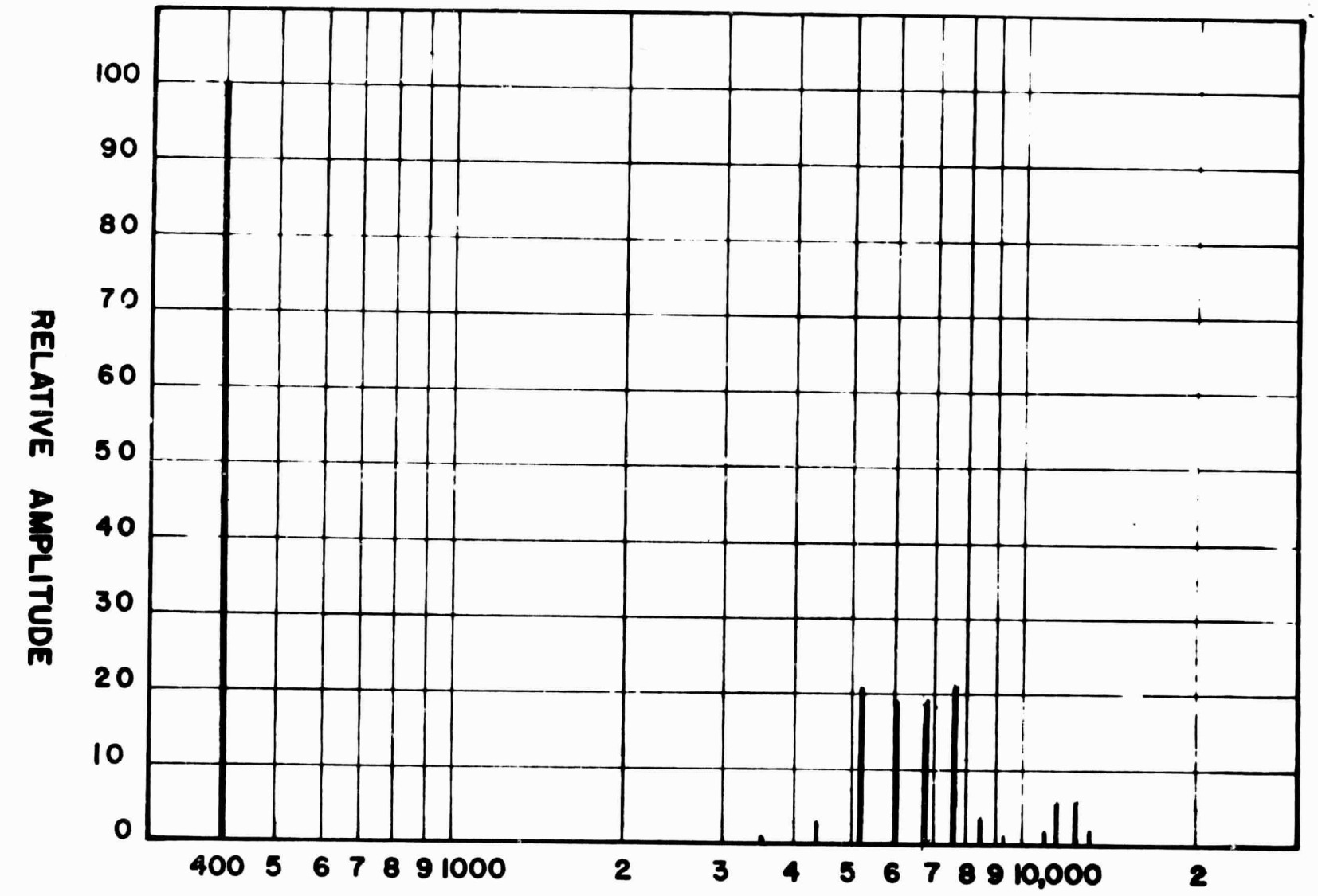
The waveform for the above equation is illustrated in Figure 12a. The data shown in Table 5 was calculated for pulse-width modulated pulses with both edges modulated by natural samples of a sinusoidal wave. In Table 6, the calculated data is compared with data measured in the laboratory. Notice that for pulse-width modulation of both edges of the pulse, the carrier and its harmonics are not present in the spectrum. This is an advantage because only the low-amplitude sideband components need to be filtered out to obtain the sine wave output.

The frequency spectrum for pulse-width modulation with both edges modulated and a modulation index of unity is illustrated in Figure 50. To further illustrate the effects of modulation the frequency spectrum for various modulation indexes are illustrated in Figures 50 through 55. Figure 56 shows the fundamental frequency relative amplitude and the first four major harmonic frequencies relative amplitude as a function of the modulation index. Comparison of Figure 56 with Figure 48 shows the tremendous advantage of the double edge modulated waveform over the single edge modulated waveform. Verification of this calculated data (Table 5 and Table 6) further stresses the requirement for use of double edge modulation.

The type of double edge modulation is also important. If the method of modulation is established differently from that of Figure 49 such that the modulated waveform of Figure 46 or 12b is generated in a double edge modulated method, many of its advantages are lost. To illustrate this, the frequency spectrum of a double edge modulated waveform in which the K factor does not vanish is illustrated in Figure 57. Inspection of this figure shows not only the increased harmonics but also the increase in their amplitudes.

C. DEMODULATOR STAGE AND DRIVE

Design of the demodulator and demodulator Drive has a major bearing on the efficiency, size, and weight of the inverter. The function of the demodulator is to convert the 3200-Hz squarewave to a 6400-Hz double edge modulated wave in as efficient manner as possible. In the demodulator there are three major areas of power dissipation, the diodes, the power transistors, and the drive circuit.



$f_c = 400$
$f_v = 6400$
$M = 1.0$

FIGURE 50
FREQUENCY SPECTRUM
DOUBLE EDGE MODULATION

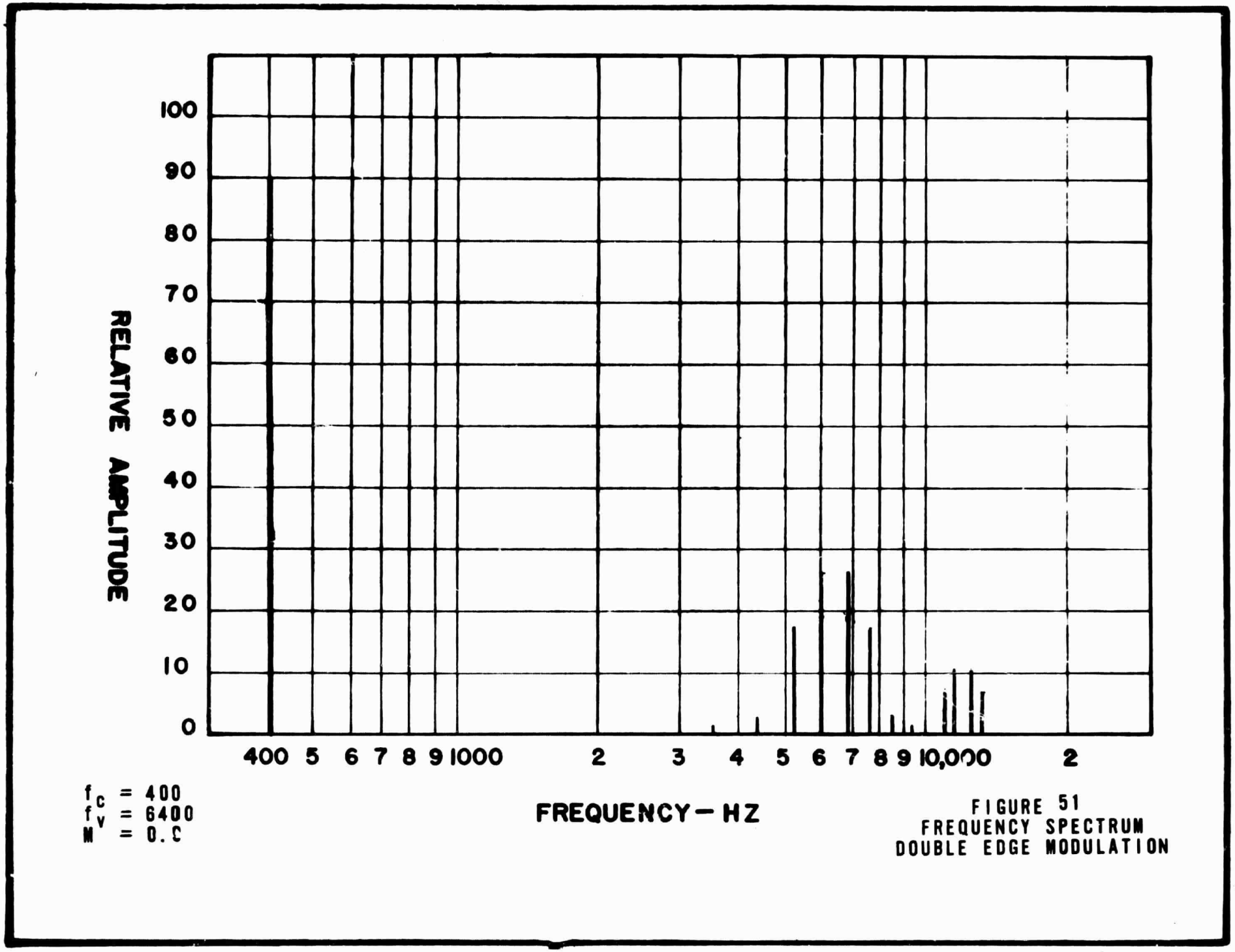


FIGURE 51
FREQUENCY SPECTRUM
DOUBLE EDGE MODULATION

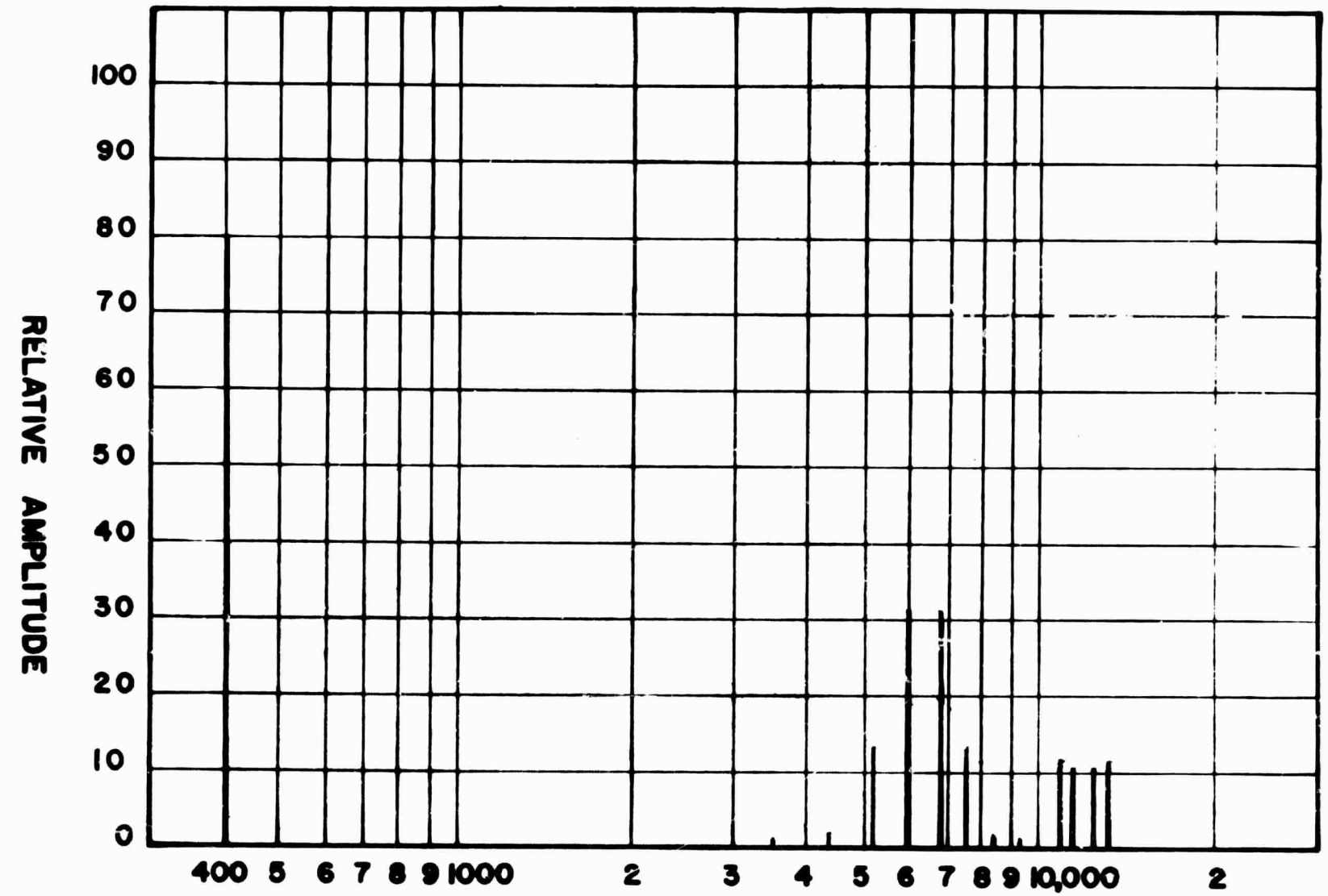


FIGURE 52
FREQUENCY SPECTRUM
DOUBLE EDGE MODULATION

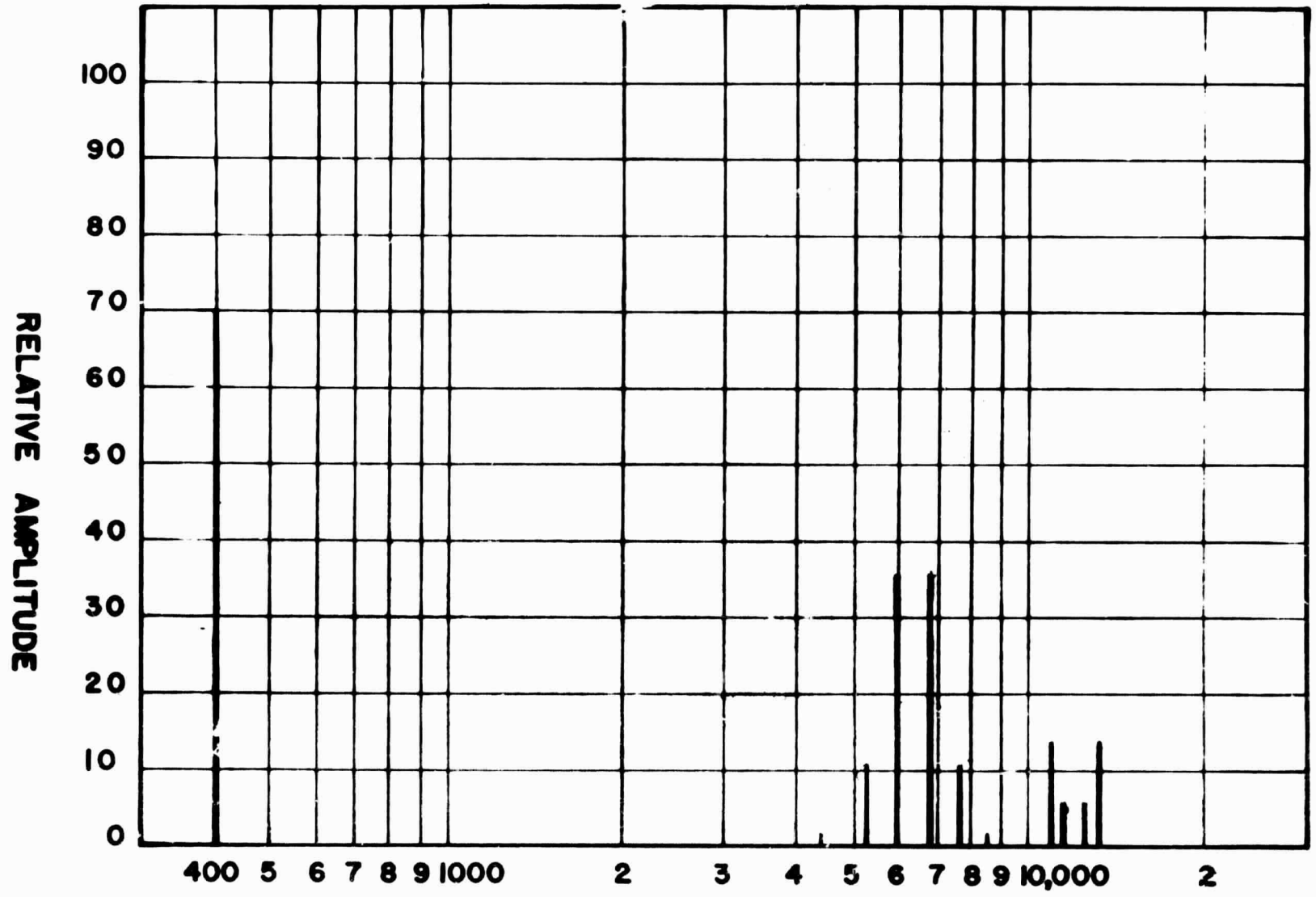


FIGURE 53
FREQUENCY SPECTRUM
DOUBLE EDGE MODULATION

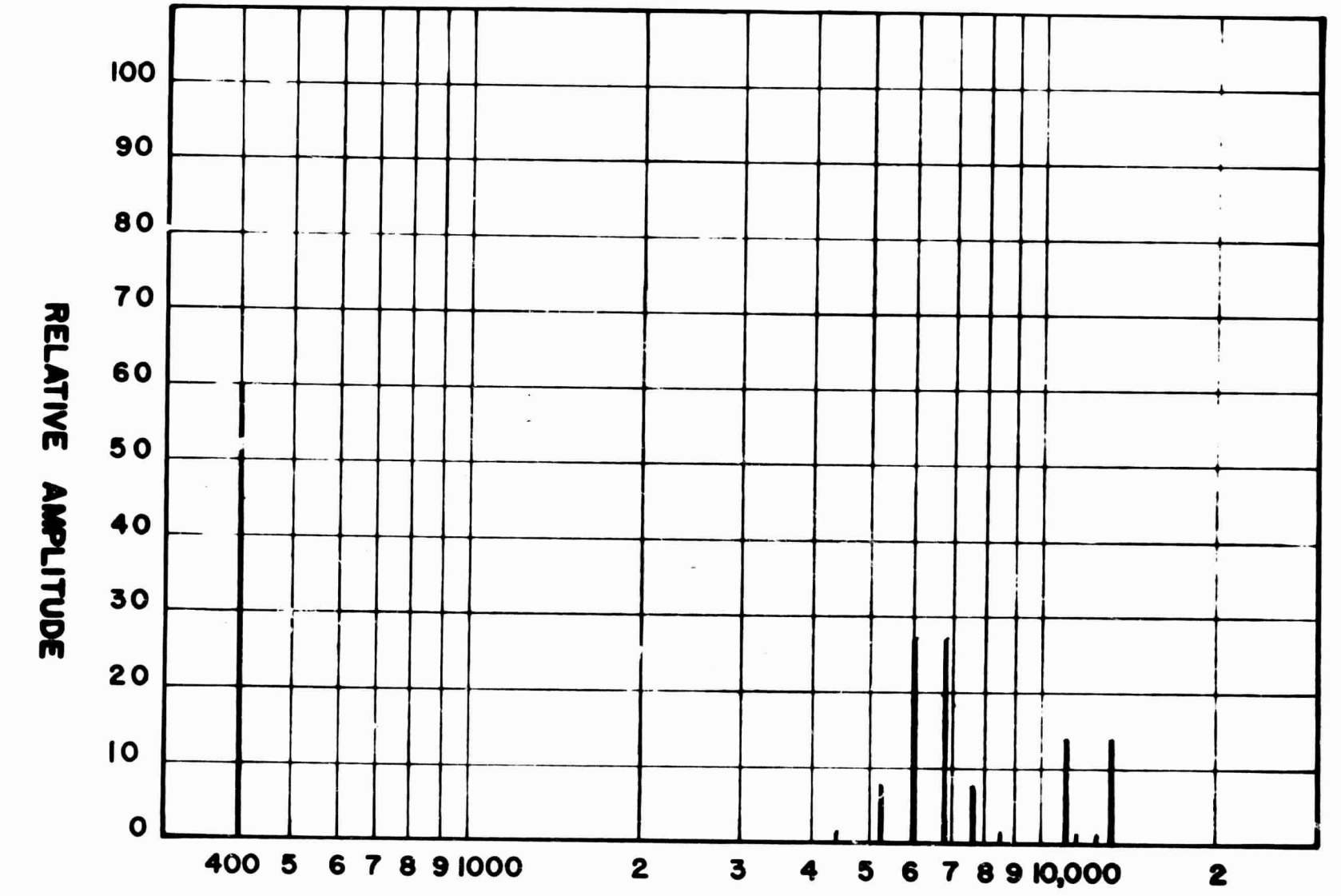
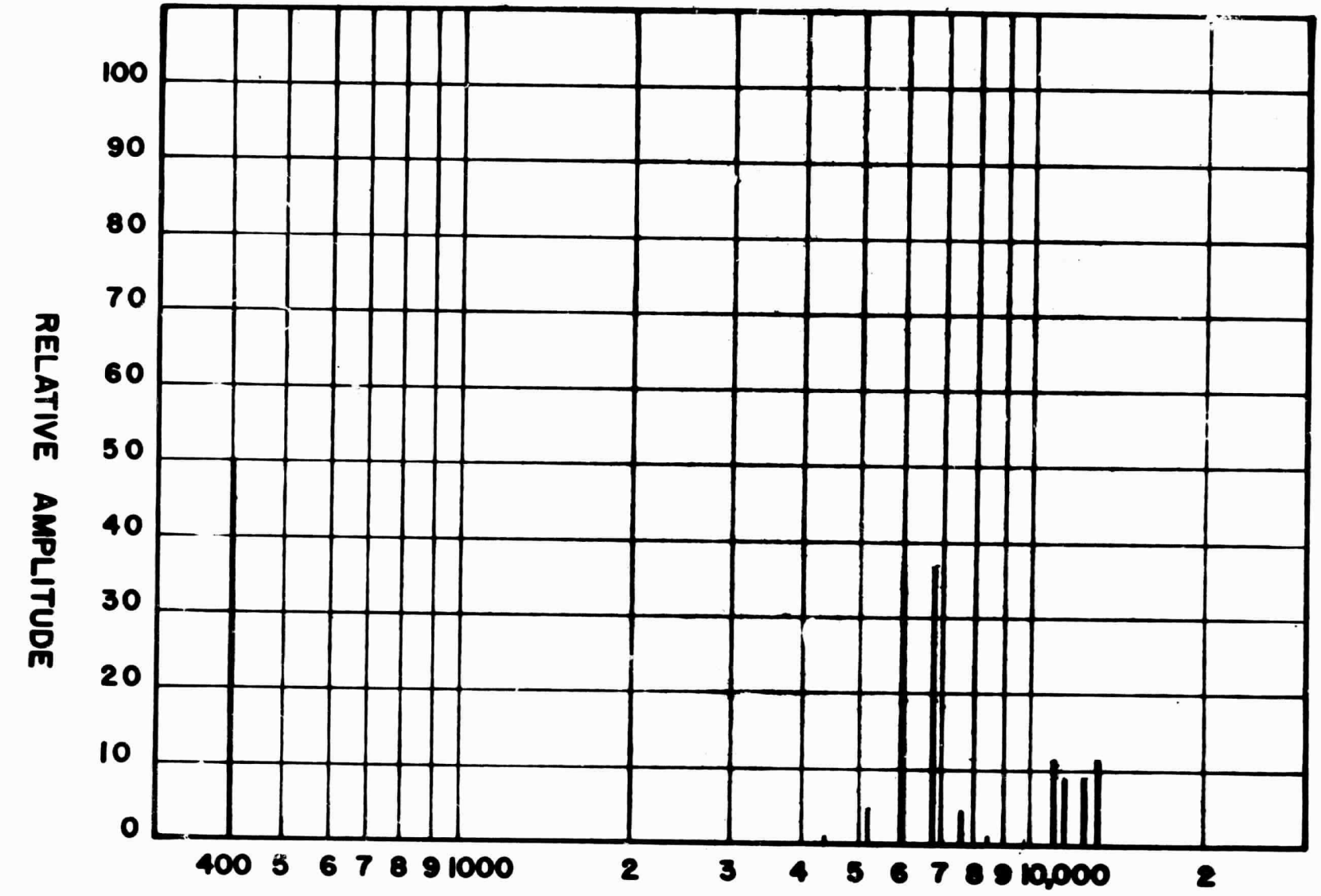
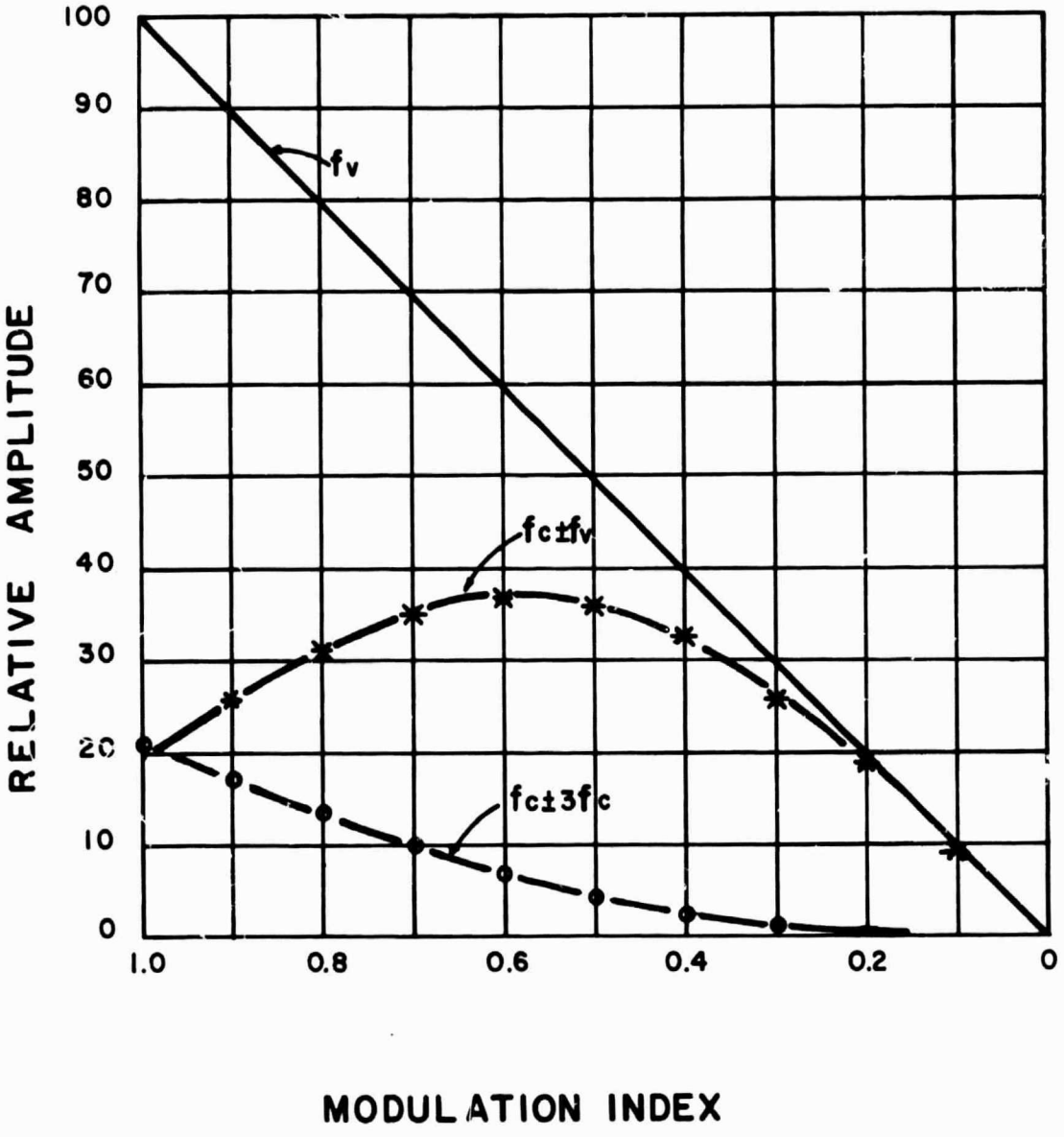


FIGURE 54
FREQUENCY SPECTRUM
DOUBLE EDGE MODULATION



$f_c = 400$
$f_v = 6400$
$M = 0.5.$

FIGURE 55
FREQUENCY SPECTRUM
DOUBLE EDGE MODULATION



fv = 400 HZ

fc = 6400HZ

FIGURE 56
RELATIVE AMPLITUDE VS
MODULATION INDEX
(DOUBLE EDGE)

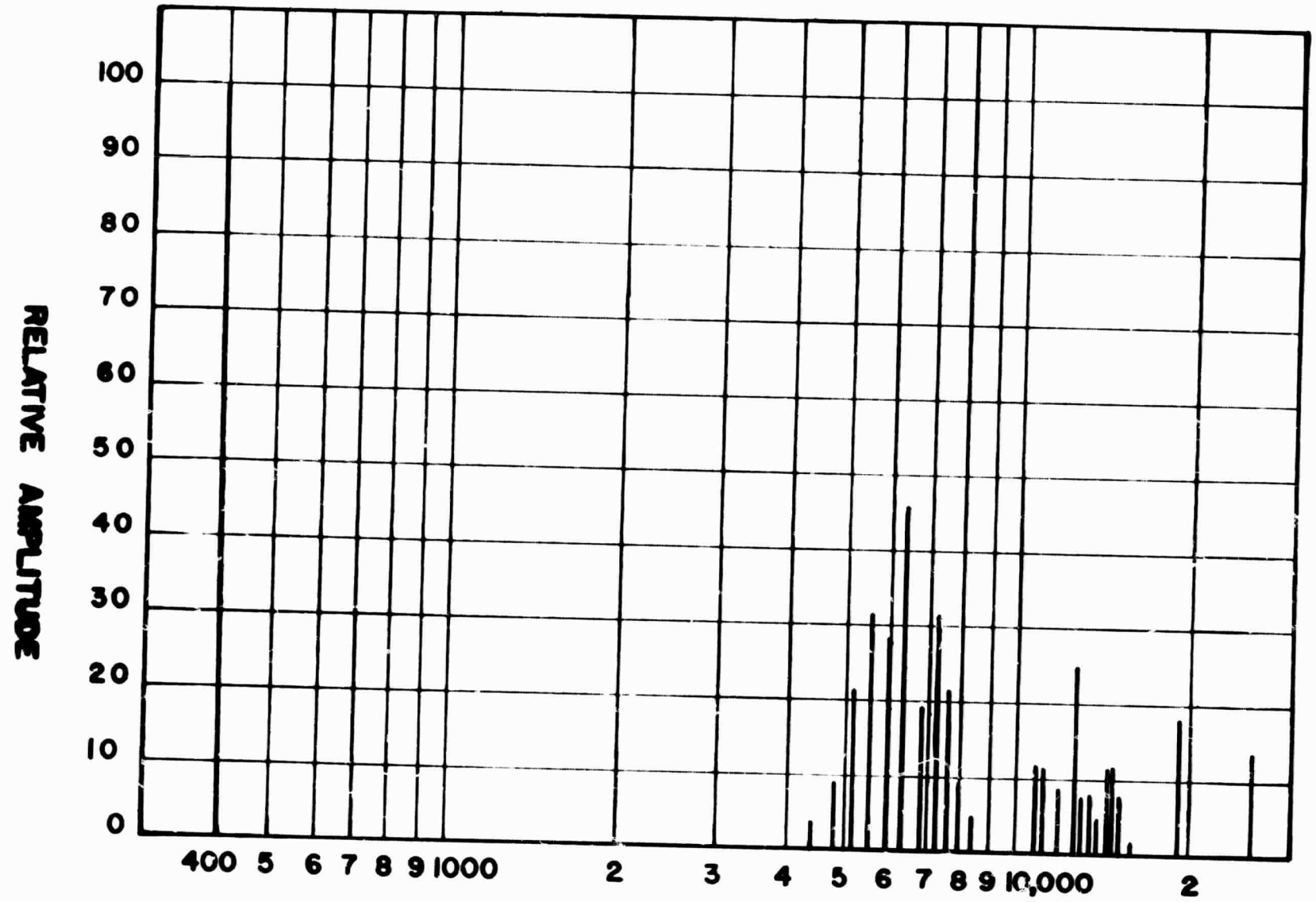


FIGURE 57
FREQUENCY SPECTRUM
(DOUBLE EDGE MODULATION)

TABLE 5
CALCULATED AMPLITUDE DISTRIBUTION OF A DOUBLE EDGE MODULATED WAVEFORM VS MODULATION INDEX

FREQUENCY	RELATIVE AMPLITUDE MODULATION INDEX (M)					
	1.0	0.9	0.8	0.7	0.6	0.5
f_v	100.0	90.0	80.0	70.0	60.0	50.0
$f_c \pm f_v$	19.2	26.0	31.7	35.4	37.0	36.3
$f_c \pm 3f_v$	20.8	17.4	13.8	10.3	7.3	4.62
$f_c \pm 5f_v$	2.7	2.39	1.3	0.96	0.45	0.45
$f_c \pm 7f_v$	0.16	0.16	0.17	0.01	0.01	0.01
$2f_c \pm f_v$	6.62	10.2	10.4	6.5	0.41	9.6
$2f_c \pm 3f_v$	1.19	6.36	11.6	13.7	13.7	10.4
$2f_c \pm 5f_v$	11.9	10.7	8.3	5.1	4.2	1.4
$2f_c \pm 7f_v$	4.7	3.18	1.7	0.6	0.5	0.08
$2f_c \pm 9f_v$	1.02	0.67	0.18	0.03	0.03	0.0
$3f_c \pm f_v$	3.86	5.79	2.86	2.65	6.87	5.92
$3f_c \pm 3f_v$	2.12	5.0	4.87	3.12	4.03	8.64
$3f_c \pm 5f_v$	2.69	1.59	5.66	7.42	7.04	4.71
$3f_c \pm 7f_v$	6.0	6.95	5.87	4.1	2.27	0.91
$3f_c \pm 9f_v$	5.23	3.62	1.95	0.93	0.35	0.09

$f_v = 400$
$f_c = 6400$

TABLE 6
CALCULATED VS MEASURED AMPLITUDE DISTRIBUTION OF A DOUBLE EDGE MODULATED WAVEFORM

CALCULATED $M = 0.9$, $f_v = 400$, $f_c = 6400$		MEASURED $M = 0.9$, $f_v = 400$, $f_c = 7200$	
FREQUENCY	AMPLITUDE	FREQUENCY	AMPLITUDE
f_v	100.0%	f_v	100.0%
$f_c \pm f_v$	29.0	$f_c \pm f_v$	30.0
$f_c \pm 3f_v$	19.4	$f_c \pm 3f_v$	18.0
$f_c \pm 3f_v$	19.4	$f_c \pm 3f_v$	16.0
$f_c \pm 5f_v$	2.66	$f_c \pm 5f_v$	4.88
$f_c \pm 7f_v$	0.18	$f_c \pm 7f_v$	0.6
$2f_c \pm f_v$	11.3	$2f_c \pm f_v$	13.0
$2f_c \pm 3f_v$	7.1	$2f_c \pm 3f_v$	9.0
$2f_c \pm 5f_v$	11.9	$2f_c \pm 5f_v$	11.0
$2f_c \pm 7f_v$	3.54	$2f_c \pm 7f_v$	4.4
$2f_c \pm 9f_v$	0.75	$2f_c \pm 9f_v$	4.0
$3f_c \pm f_v$	6.4	$3f_c \pm 1f_v$	7.8
$3f_c \pm f_v$	6.4	$3f_c \pm 1f_v$	7.3
$3f_c \pm 3f_v$	5.6	$3f_c \pm 3f_v$	7.0

The diode losses are a direct function of the type diode used in the bilateral switch and are based on the forward conduction losses and on the leakage current under reversed bias conditions. The diodes conduct in groups of four, series connected. The loss for a group under normal operating conditions is approximately 17.3 watts. This is the total power dissipated by all 16 diodes, so to determine the average power dissipation by a diode, total power must be divided by the total number of diodes, 16. This gives an average power dissipation of 1.1 watt per diode. It is clear the diodes are selected on a basis of peak currents and peak voltages and not on the basis of power dissipation.

Selection of power transistors for the demodulator is a much more complex problem. As with the design of any power-switching stage, each transistor parameter must be evaluated for optimum operating and circuit conditions as well as maximum stress levels. The most desirable characteristics of the demodulator transistor are fast switching speeds and high voltage ratings. The voltage across the demodulator when it is OFF or switching, varies between 180 volts to 275 volts. The variation in voltage is due to input voltage changes and load changes. Under abnormal or input transient conditions, the transistors could go to 311 volts. The load current seen by the transistor would be 4.4 amperes at 500 VA and 6.5 amperes at 750 VA. As with the diodes, however, the transistors must be selected to carry the peak current of 9.3 amperes (6.5 X 1.414) without coming out of saturation. Also, the 14-ampere short-circuit current must also be given consideration. It is also desirable that the transistors have switching times in the order of 2.0 microseconds, and that the saturation losses be in the order of 0.0[illegible] ohm. It should be noted that the frequency multiplication inherent in this design makes it possible to operate at half the frequency of other circuits while maintaining the same basic frequency ratio between the low output frequency and the desired high modulation frequency.

Table 7 gives a comparison of a few of the high-voltage transistors that could be considered for use in the demodulator stage. This table does not include all transistors available but only those given consideration. The development of these devices has been extensive and the outlook is good for future devices of higher voltage and current levels.

TABLE 7
HIGH-VOLTAGE SWITCHING TRANSISTORS

	DELCO 423	DELCO 431	DELCO 2N2582	DELCO 2N2583	T.I. 2N3847	T.I. 2N3849	SOLITRON* MHT 7805
COLLECTOR VOLTAGE	400	400	500	500	300	300	325
COLLECTOR CURRENT (AMPS)	3.5	5.0	10.0	10.0	20.0	20.0	10.0
POWER RATING (WATTS)	100	125	150	150	150	150	50
TURN-ON-TIME (U sec.)	0.3	0.4	2.1	2.1	4.0	4.0	-
TURN-OFF-TIME (U sec.)	1.2	0.9	3.2	3.2	7.0	7.0	-
SATURATION RESISTANCE (OHMS)	0.3	0.12	0.14	0.10	0.07	0.07	0.1
CURRENT GAIN h_{fe}/I_c	10/2.5	10/3.5	10/5	10/10	10/10	10/15	20/5

*PRELIMINARY SPECIFICATIONS

For this application the Delco 2N2583 transistor was considered to be the optimum choice. All of the devices with the exception of the Solitron Unit have been tested in inverters using the phase demodulated design. The Texas Instruments device has presently been removed from the market due to yield problems; however, this is expected to clear up in the near future. The Delco 423 and 431 have been used extensively and with good results in our 250-VA multiple - frequency inverter. They were given consideration for use in this application and indicated a slight power savings; however, the additional circuitry requirement was not considered worth the small increase in efficiency. The improvement in efficiency was due to the much faster switching times of the 423s and 431s.

By paralleling two 2N2583s, the overload currents can easily be met while providing an ample safety factor for current as well as voltage . In paralleling the two 2N2583s, it was not considered necessary to provide paralleling resistors to force current sharing. Current sharing networks are generally needed where the unbalance in current cannot exceed ten to fifteen percent. In this design, however, an unbalance of fifty to seventy-five percent under overload conditions would not exceed the current rating of the device. Tests have indicated that in the proposed circuit the transistor carrying the heavier current loads tends to switch faster than those carrying the least current. This situation causes the lightly loaded transistors to carry a larger share of the switching losses. This effect tends to balance the total losses between the two devices. Illustrated in Figure 58 is the switching losses and saturation losses as a function of load current. As load current increases, the saturation losses go up as expected; however, at the same time, switching losses decrease since the transistor is not over driven as much in the higher current region. When two transistors are paralleled and one of the transistors carries most of the current due to higher gain or lower saturation resistance losses, then it tends to switch faster than the other. This transistor then has higher saturation losses, but lower switching losses than the transistor with the light load. We have paralleled six Delco DTS 423s in the same basic demodulator circuit with very good results. The 2N2583 was chosen for this application because of the reduced circuitry and slight weight advantage.

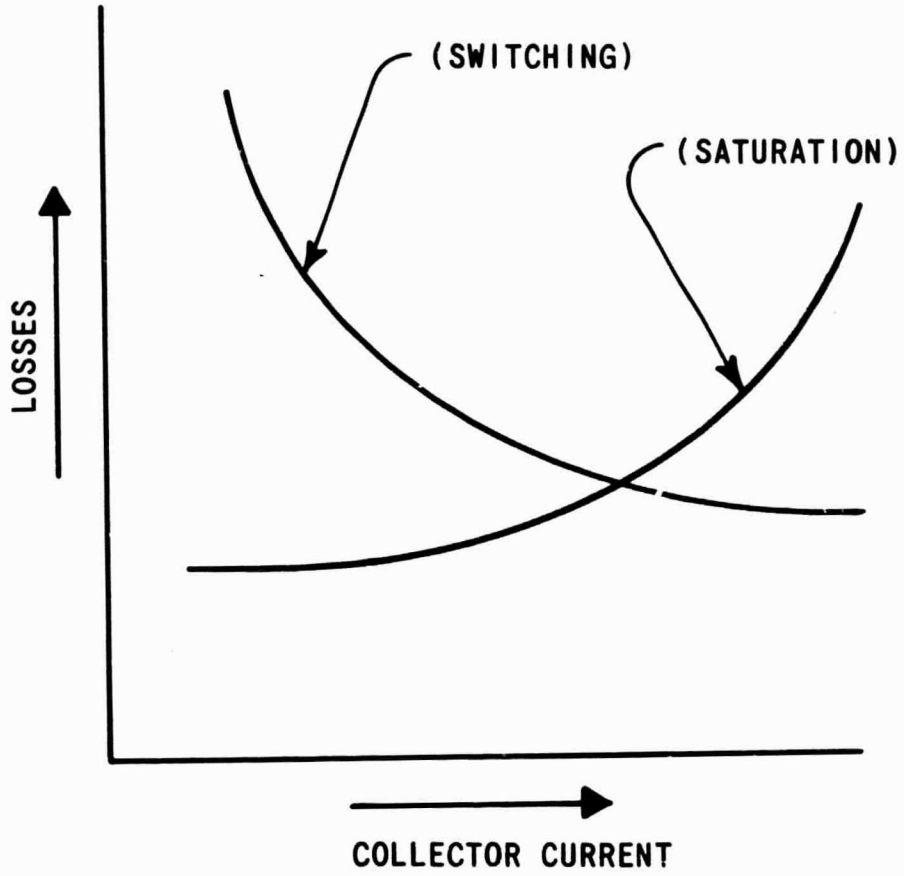
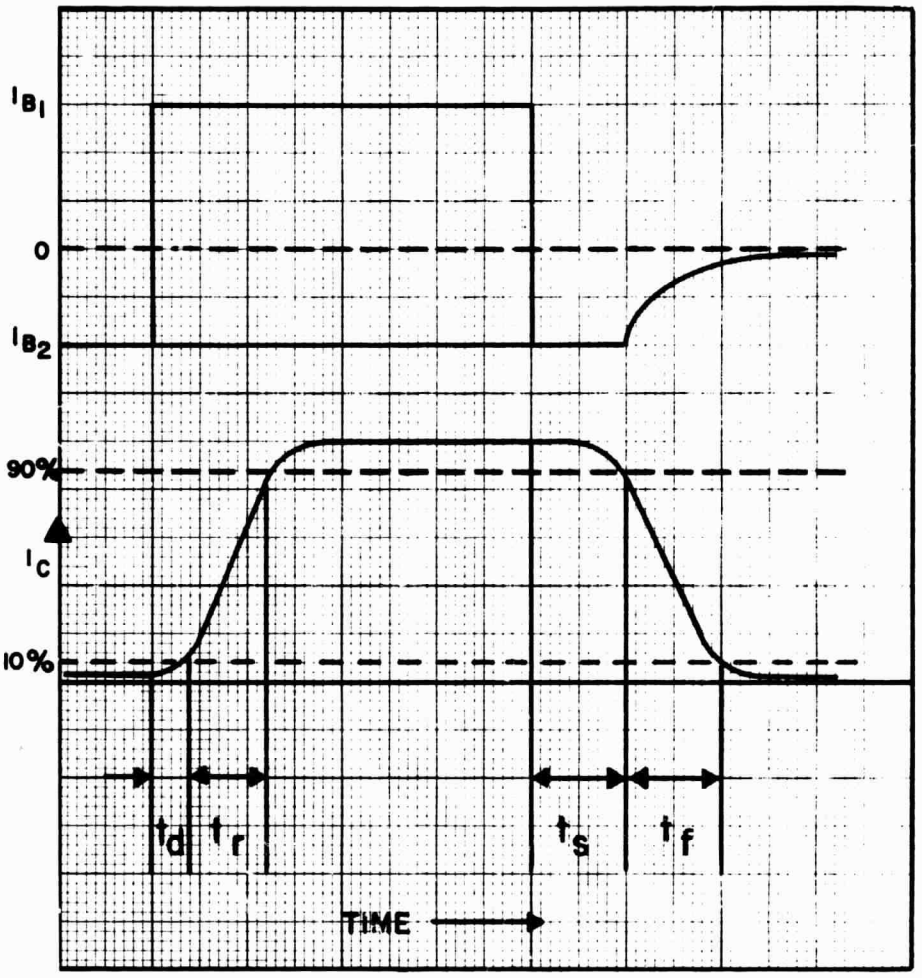


FIGURE 58
LOSSES VS COLLECTOR CURRENT

INPUT AND OUTPUT CURRENT PULSES OF
SATURATED COMMON EMITTER SWITCH



$T_{ON} = t_d + t_r$ = DELAY TIME PLUS RISE TIME
$T_{OFF} = t_s + t_f$ = STORAGE TIME PLUS ALL TIME

FIGURE 59
SWITCHING TIMES

The power dissipated by the transistors may be calculated from the following equation:

Total power dissipation =

$$P(\text{switching ON}) + I_c(\max)\ V_{ce}(\text{sat}) + I_B\ V_{BE}(\text{sat}) +$$

$$P(\text{switching OFF}) + V_{ce}(\max)\ I_{cex}\ .$$

This equation shows that there are five contributing factors in the power dissipation of a transistor. In a high-voltage device, the time required to change states from an OFF to ON or from an ON to OFF condition becomes a primary design factor. The switching power may be calculated from

$$P(\text{switching}) = \frac{1}{2} (I_c(\max)) (V_{ce}(\max)\ (\text{duty cycle}).$$

Switching at a 3200-Hz rate gives a period of 312 μsec. If the total switching time to go from OFF to ON was 3.12 μsec and the collector current was 10 amperes at 200 volts, then the power loss would be (duty cycle= $\frac{3.12}{312}$ = 0.01)

$$P_s = \frac{1}{2} (10) (20) (.01) = 1.0 \text{ watts.}$$

It is obvious that if the switching time were reduced, the switching losses would go down accordingly. Total switching time is determined by four basic factors as illustrated in Figure 59. Turn ON time is composed of delay time Td and rise time T_r while the turn OFF time is composed of storage time Ts plus fall time T_f. Rise time and fall time are fixed factors, that is they are determined entirely by the device design. The delay time and storage time are also limited by the device design to some extent; however, the basic driving circuit affects these parameters a great deal. For this reason, considerable effort was spent in designing a drive circuit which reduces the affect of the delay or storage time.

The delay times in most devices is small and is normally included with the rise time as turn ON time. Storage time is as great or greater than fall time, however, and can equal the total turn ON time. The following switching times for the 2N2583 illustrate this:

Turn ON time ($T_D + T_r$) = 2.1 microseconds

Storage time (Ts) = 2.2 microseconds

Fall time (T_f) = 1.0 microseconds.

Since the demodulator transistors operate in push-pull pairs (Figure 34) such that one transistor is turning ON as the other is turning OFF, both transistors can be on at the same time. When both transistors conduct simultaneously for this turn ON-OFF period, the output of the transformer is shorted. The magnitude of the short-circuit current is limited by the source impedance and by the gain of the demodulator transistors. As the short circuit current goes above the point for which there is sufficient gain, then the transistors pull out of saturation. This tends to help turn off the ON transistor and hold off the OFF transistor. Also, as the transistor comes out of saturation, large voltages appear across the transistor. This generates large power dissipation in the transistors during these switching conditions.

One method of reducing these switching losses is illustrated in Figure 32. This design was considered the best of many given consideration. This circuit locks the OFF transistors off until the ON transistor has come out of forced saturation and is approaching the starting point of its fall time, the 90-percent point of Figure 58. Refer to Figure 32: if transistor Q17 and Q18 are ON and drive transformer T3 reverses voltage and attempts to turn Q17 and Q18 OFF, the storage time holds it ON and the positive voltage now at terminal 7 causes current to flow through transformer T7 and transistor Q17. This action produces a voltage at terminal 3-4 of T7 which biases ON transistor Q3. Since transistor Q3 is ON, the gate of SCR CR6 is held at a negative voltage and does not turn ON. This action prevents the drive current from reaching demodulator transistors Q15 and Q16, thus they remain OFF.

As transistors Q17 and Q18 come out of saturation and the collector voltage matches the voltage of terminals 7-8, current stops flowing in transformer T7. This permits transistor Q3 to turn OFF, thus turning ON SCR CR6 which turns ON demodulator transistor Q15 and Q16. The overlap of switching times is the rise and fall times of the devices. This circuit has proved more successful than some other circuits considered.

One common method is to use a diode in the base-to-collector circuit. This diode prevents the transistor from going into complete saturation. This method did not prove out since it did not slow down the turn ON.

Another attempt made to slow down turn ON was a base-to-emitter capacitor to reduce the rise time of the voltage at the base of the transistor. This method

did not provide reduction in short-circuit currents required for good operation.

Several other methods were tried in the design of the drive stages for the 3-KW and 250-VA inverters without success. The design, as illustrated in Figure 32, has proved to be the best approach to the problem.

The calculated power dissipation for the demodulator stage is 29.0 watts at nominal loads. This power is divided between eight transistors, giving an average power dissipation of 4.0 watts each. As pointed out in the previous discussion, the demodulator transistor carried less than half its rated current at nominal loads, but must be designed for the overload and short-circuit current conditions.

D. POWER STAGE AND DRIVE

The power stage is a basic push-pull parallel inverter operated at a switching frequency of 3200 Hz. Design of the power stage is made simpler by the number of devices available. Table 8 lists a few of the devices given consideration for use in the power stage. The Solitron devices 2N3151 and MHT 8923 were not analyzed for use in the design due to the lack of information on the switching speeds. If their switching times are as fast as the MHT 8923, however, they may be given consideration in the development stage due to the possible reduction in components and circuits requirements. As with any new device, it is desirable to see how well they are going to work out.

The RCA device is considered to be the best choice for use at this time. This decision is based on optimum losses without undue circuit complexity. Power dissipation for the paralleled RCA 2N3265 is 20.8 watts, divided between six transistors for an average dissipation of four watts per transistor. Again, the design is based on a maximum value of current and on voltage conditions under worst-case conditions.

Drive for this stage is designed for maximum switching speed and minimum circuitry. Addition of a delay circuit such as in the demodulator was not considered necessary. Switching losses are not as severe at the lower voltages of the power stage.

TABLE 8
HIGH-POWER SWITCHING TRANSISTORS

	RCA 2N3265	T.I. 2N4003	SOLITRON* 2N3599	SOLITRON* 2N3151	SOLITRON* MHT 8923
COLLECTOR VOLTAGE	90	100	80	150	120
COLLECTOR CURRENT (AMPS)	25	40	20	30	90
POWER RATING (WATTS)	125	100	100	300	350
TURN-ON-TIME (U sec.)	0.5	1.0	0.7	--	--
TURN-OFF-TIME (U sec.)	2.0	2.0	2.7	--	--
SATURATION RESISTANCE (OHMS)	0.05	0.04	0.06	0.03	0.02
CURRENT GAIN h_{fe}/I_c	20/20	15/30	10/20	10/50	10/75

*NEW DEVICES

E. FILTERING

1. Input Filter

Input filter FL1, shown in the schematic diagram, is designed to meet four specific requirements of the related specifications. These are:

1. Ripple generation
2. Turn ON transient
3. Input transient
4. Electromagnetic interference

Of the above requirements, the ripple generation specification appears most difficult to meet. The following discussion indicates the general approach taken to reduce ripple generation.

Based on an 80-percent efficiency, input power to the inverter is 625 watts at full load. Assuming the input voltage is a minimum of 24 volts at full load, input current is 26 amperes. Allowing a 1.0-volt drop across the input filter, input voltage at the power stage is 23 volts.

Input current for the power stage is composed of a 400-Hz full-wave rectified envelope at 3200-Hz switching frequency superimposed on a DC current level for control and drive circuitry power. Assuming a 3.0-ampere steady-state current for control and drive circuitry, peak input current to the power stage is $(26-3) \times \sqrt{2}$ volts = 32.5 amperes. Total peak current is (32.5 + 3) amperes = 35.5 amperes. The waveform is shown in Figure 60.

This envelope must be filtered to prevent superimposing a 0.5-volt peak into the 0.5-ohm input impedance of the source. The input current variation from source to inverter is 1.0-ampere maximum.

The choke-input filter is designed to store energy during the valley period of the envelope and supply energy during the peak periods of the envelope. To optimize filter design, small values of inductance have been chosen to reduce iron weight and copper loss. Thus, a large amount of capacitance is required to store and deliver energy.

The first filter to be considered is shown in Figure 61. The

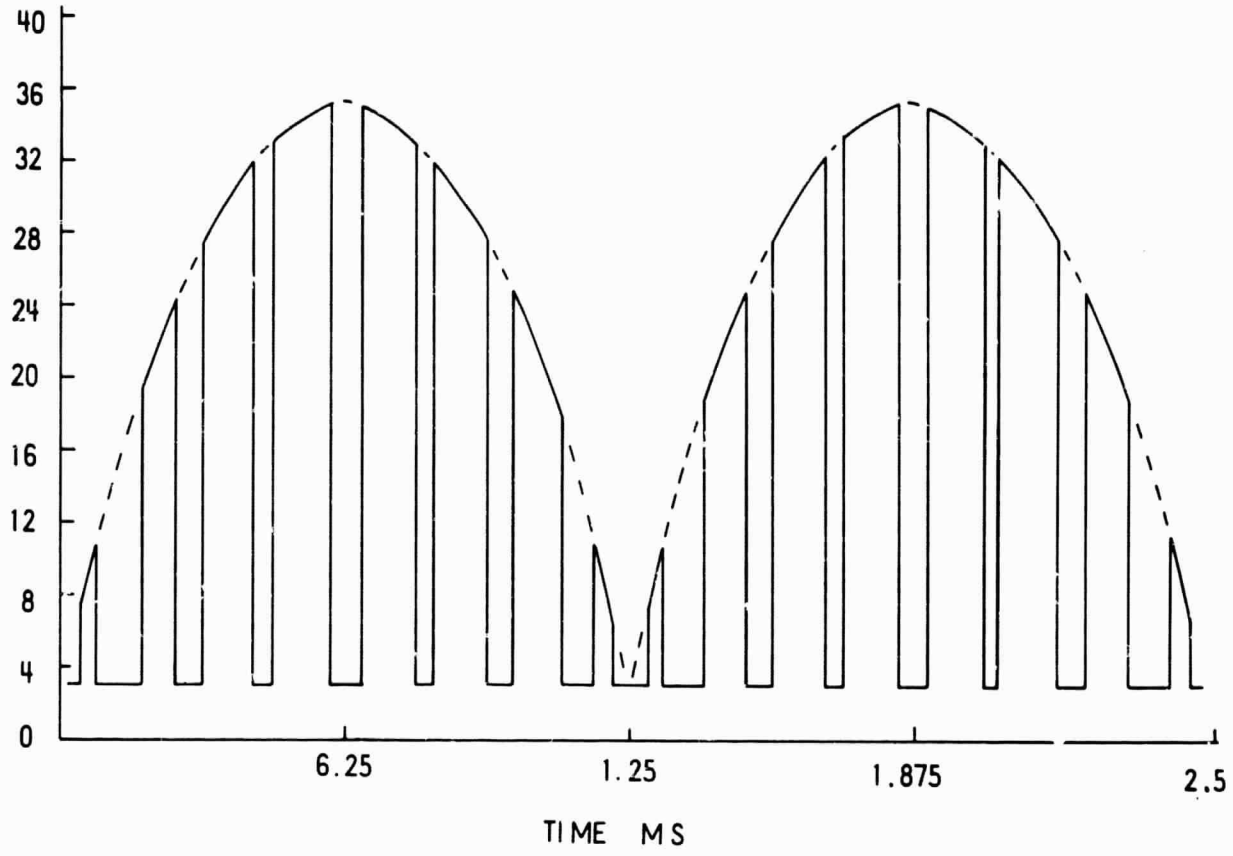


FIGURE 60
INPUT CURRENT WAVEFORM

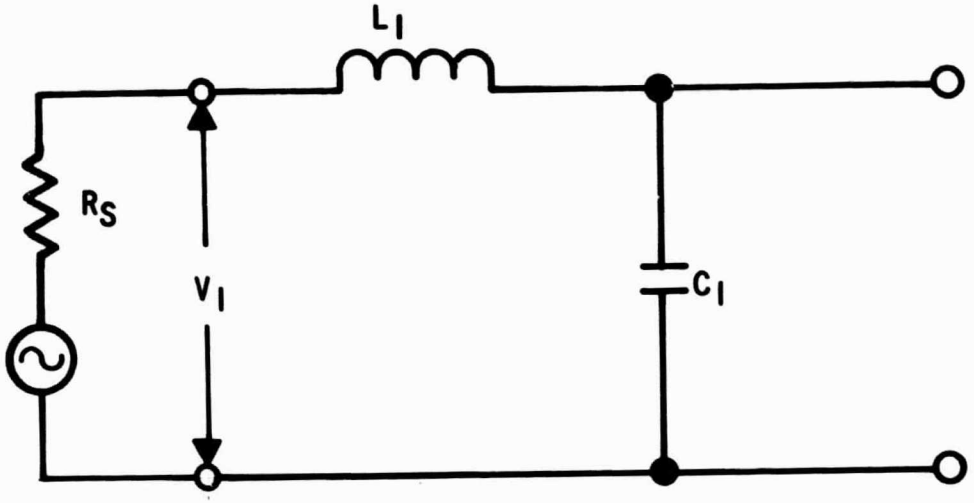


FIGURE 61
BASIC INPUT FILTER

capacitance was calculated using $C = i_c \frac{dt}{dec} = 4250\ \mu f$. The inductance was calculated using

$$L = E_L \frac{dt}{di_L} = 250\ \mu h.$$

This filter is impractical because of the size of L and C and the 8.5-ampere current that the capacitor must carry.

Next, a six-element filter was designed as shown in Figure 62. The capacitance values are 2350 μf, 1775 μf, and 1420 μf. The inductance values are 50.0 μh, 26.2 μh, and 15.0 μh. Paralleling of capacitors in a cordwood manner is utilized to minimize volume. The inductor may consist of tapped windings on a single core to reduce volume and weight as compared with the three inductors. The finalized component values must be determined by test data from breadboard models.

The proposed choke input filter limits the inrush current to the inverter. By using the filter value of Figure 2, for simplicity, input current from source to filter can be calculated from Figure 63. The loop equation is

$$E = Ri + \frac{Ldi}{dt} + \frac{1}{C}\int idt.$$

The LaPlace transform is

$$E = (1L + R + \frac{1}{pC})\, i_t$$

$$Is = \frac{E}{Ls^2 + Rs + \frac{1}{C}} = \frac{E/L}{S^2 + \frac{R}{L}s + \frac{1}{LC}} = \frac{E/L}{(s + \frac{R}{2L})^2 + \frac{1}{LC} - (\frac{R}{2L})^2}.$$

Solution for i is:

$$i_t = \frac{E\ e^{-\frac{Rt}{2L}} \sin \sqrt{\frac{1}{LC} - (\frac{R}{2L})^2}\ t}{L \sqrt{\frac{1}{LC} - (\frac{R}{2L})^2}}.$$

Resonant frequency of the filter is $f = \frac{1}{2\pi\sqrt{LC}} = 154.0$ Hz and the period is 6.5 ms. Assuming E_{in} is 28 volts, Figure 64 shows a plot of damped waveform

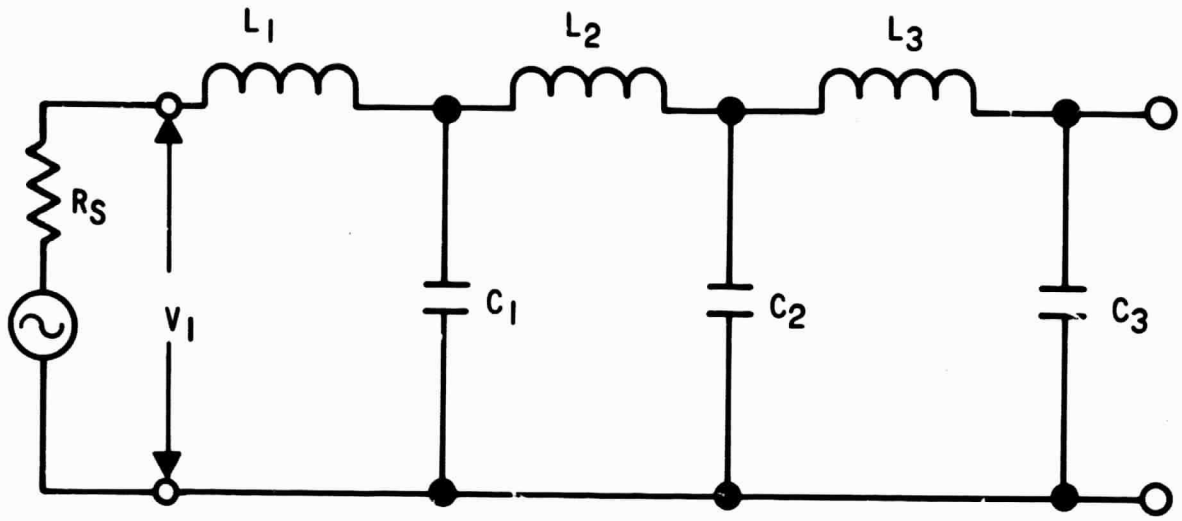


FIGURE 62
CASCADE INPUT FILTER

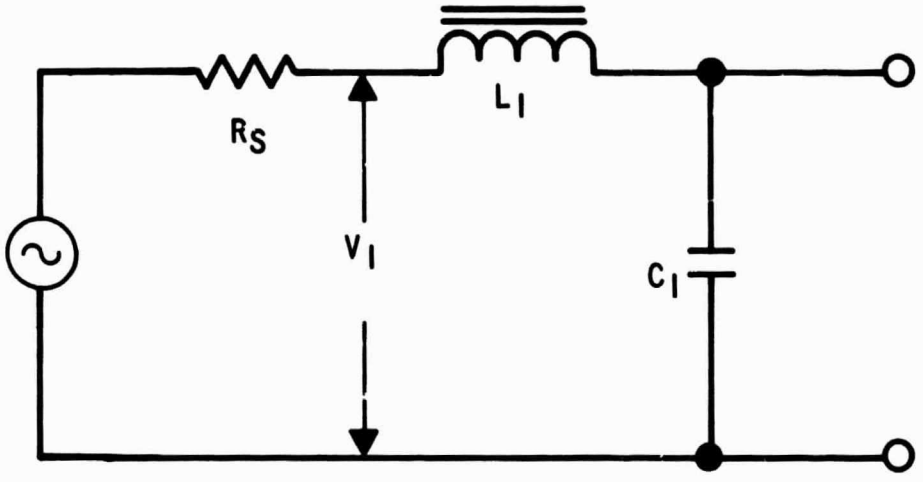


FIGURE 63
SIMULATED INPUT FILTER

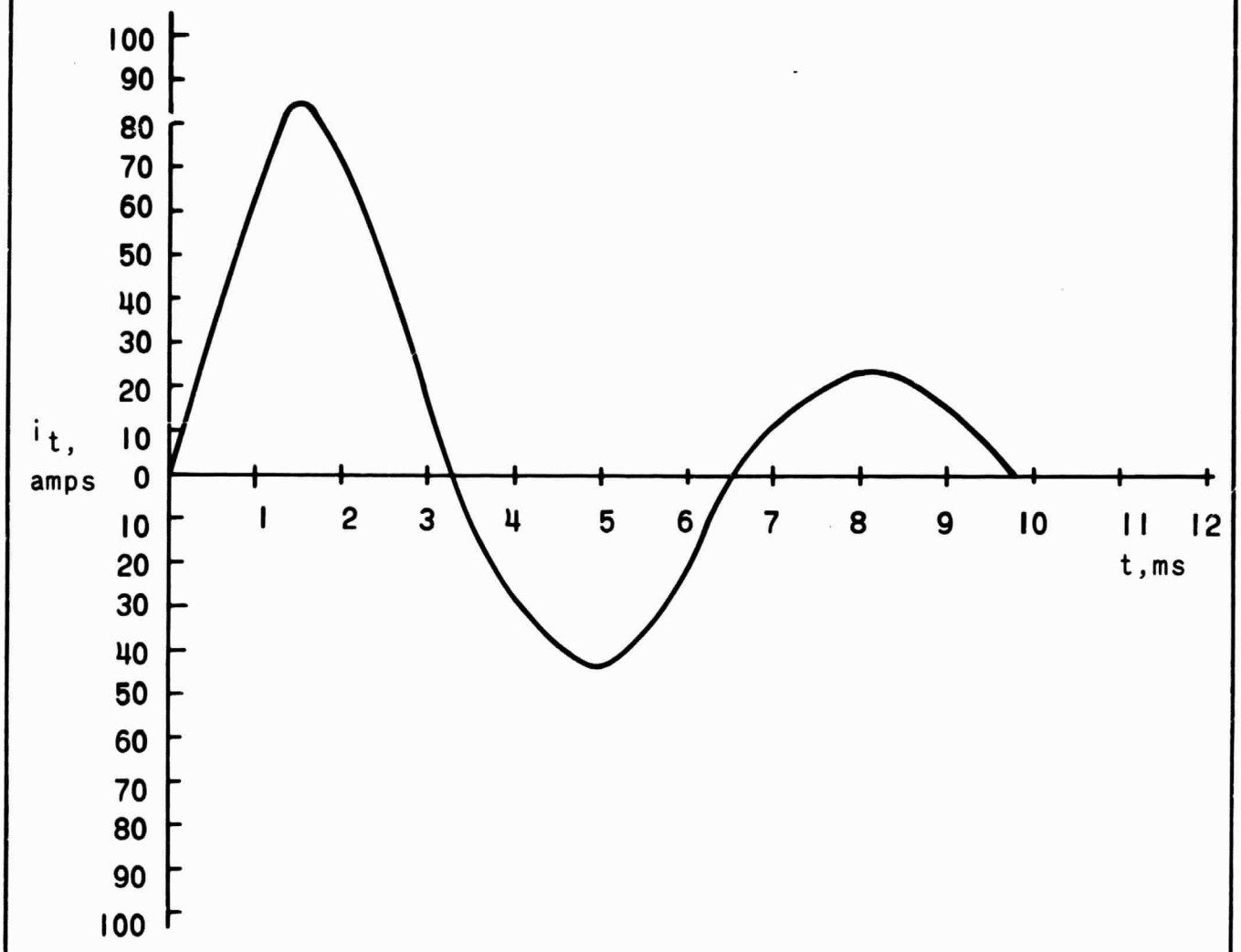


FIGURE 64
INPUT CURRENT TO FILTER

i_t. At t = 2 ms, input current is 74 amperes, which is below the 300-percent peak rating of nominal input current (or 300 percent X 26 amperes = 78 amperes). At 100 ms, sufficient damping has occurred to limit the input current to the milliampere range.

The input filter is sufficient to absorb energy produced by the 80-volt transient for 10μsec and limit transient input voltage to the power stage to a safe level. The transient of 40 volts for 1 sec must not damage the inverter components.

Feedthrough capacitors, as shown in the schematic diagram shall be used to reduce electromagnetic interference and shall be located at the input connector. Due to the design of the input filter, extensive RFI filtering is not necessary to meet the RFI requirement of the specification.

2. Output Filter

Discussion and data developed in the Pulse-Width Modulation Analysis section is of great value in designing the output filter. It provides an understanding of the waveform to be filtered and a knowledge of the power stress on the filter. The basic function of the output filter is to shape the output of the demodulator stage into a sinusoidal voltage with minimum distortion. It is desirable that the filter achieve this function without introducing any unnecessary voltage-ampere burden on the power stage and that the filter characteristics be relatively independent of the load.

Examination of the output waveform of the power stage, Figure 35d, which is similar to the waveform illustrated in Figure 49b, reveals the requirements of the transfer characteristics desired. The pulse repetition rate of this wave is approximately 6400 Hz, which is a compromise between the desirable high frequency dictated by the filter consideration and the low frequency required by the switching components in the power stage. Again, it is pointed out that the modulation frequency, 6400 Hz, of the modulated waveform is twice that of the power switching stage, 3200 Hz. This data, taken in the laboratory, indicates that the maximum modulation index (M) that can be achieved for a similar power

stage operating at full load is better than 0.95. The pulse-width modulation spectrum for a modulation index of 0.9 illustrated in Figure 52 will be used to design the output filter. The major frequency components of this spectrum are tabulated for easy reference in Table 5. The filter is to be designed to provide 2-percent maximum rms distortion. Examining Figure 52 reveals that the lowest sideband frequency of 6 KHz is the predominate frequency that must be suppressed. A reduction to 2 percent or less of the fundamental requires an approximated reduction of 28.9-to-2 or about 15-to-1 in an amplitude of this frequency. This reduction is expressed in db by using the formula 20 log V_1/V_2 and equals about 24 db.

Various low-pass filters are analyzed on four basic requirements: first, does the filter have enough attenuation to provide minimum distortion? second, is phase shift a minimum so as not to affect the feedback control loops? third, is the voltage-ampere burden a minimum to reduce unnecessary load on the power stage? last, but not least, are the components of a practical size and rating?

The first low-pass filter configuration considered is illustrated in Figure 65. The series L_1C_1 is tuned to the fundamental frequency of 400 Hz. The impedance of the series L_1C_1 passes the fundamental but is a high impedance to the other frequency components. Let C_1 be 40 μf and use $L_1 = 1/w^2C_1$ to calculate an inductance of 4 mh to resonant at 400 Hz. The shunt LC is tuned to 6.4 KHz to attenuate higher-frequency components. Let C_2 be 6 μf and use $L_2 = 1/w^2C_2$ to calculate an inductance of 100 μh. The voltage transfer ratio for this low-pass filter is

$$\frac{V\ out}{V\ in} = \left| \frac{(X_{L_2} - X_{C_2})}{(X_{L_1} + X_{L_2}) - (X_{C_1} + X_{C_2})} \right| .$$

Decibels of attenuation for this low-pass filter is equal to

$$20 \log \left| \frac{V\ in}{V\ out} \right| = 20 \log \left| \frac{(X_{L_1} + X_{L_2}) - (X_{C_1} + X_{C_2})}{(X_{L_2} - X_{C_2})} \right|$$

where $X_L = 2\pi fL$, $Xc = \frac{1}{2\pi fC}$.

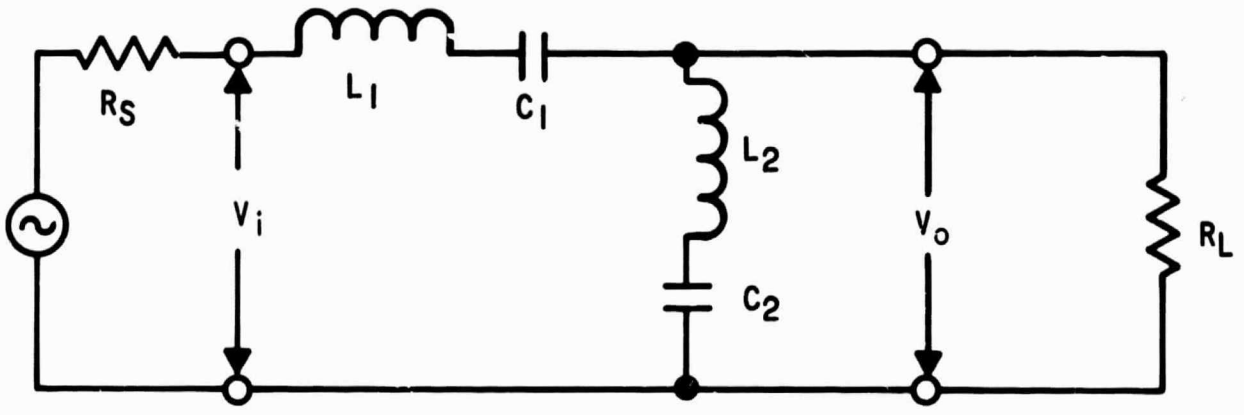


FIGURE 65
SERIES TUNED FILTER

Current for full load is given by the ratio of 500 VA/115 volts, which is 4.35 amperes. The resistance of the load is the ratio of 115 volts/4.35 amperes, which is 26 ohms. The phase angle can be calculated and is given as

$$\phi = \tan^{-1} \frac{(X_{L_1} - X_{C_1}) \left[(X_{L_2} - X_{C_2})^2 + (R_L)^2\right] + X_{L_2} - X_{C_2})(R_L)^2}{(X_{L_2} - X_{C_2})^2 R_L} .$$

Next, the voltage-ampere burden is calculated based on the 400-Hz fundamental voltage which can attain a maximum of 211 volts peak for this condition. The 400-Hz circulating current, with no load on the output of the filter, is

$$I = \frac{E}{Z} \qquad \frac{E}{\left|(X_{L_1} + X_{L_2}) - (X_{C_1} + X_{C_2})\right|} ,$$

$$I_{400\ Hz} = \frac{211}{\left|(9.5 + 0) - (10 + 8)\right|} = \frac{211}{8.5} = 24.8 \text{ amperes rms} .$$

The 5.2-KHz component is 20 percent of the 400-Hz component, or 42 volts.

$$I_{5.2\ KHz} = \frac{42}{\left|(120 + .5) - (.25 + .4)\right|} = \frac{42}{120} = 0.35 \text{ amperes.}$$

The 6-KHz component is 29 percent of the 400-Hz component, or equal to 62 volts.

$$I_{6\ KHz} = \frac{62}{\left|(140 + .5) - (.35 + .47)\right|} = \frac{62}{140} = 0.443 \text{ A} .$$

Figure 66 illustrates the attenuation and phase angle respectively of a typical 400-Hz filter for a pulse-width modulated system. The ideal filter has a minimum loss, or attenuation, at the basic 400-Hz to which L_1 and C_1 of Figure 65 are tuned. From 400 Hz to 1200 Hz the gain of the output filter is notched out by a twin-tee filter in the feedback network. The filter has a maximum attenuation at 6.4 KHz, and sufficiently attenuated sidebands of 6.0 KHz and 6.8 KHz.

The second low-pass filter configuration considered is shown in Figure 67. This filter must be designed to attenuate the 6-KHz sideband frequency component from 28.9 percent to 2 percent of the 400-Hz voltage.

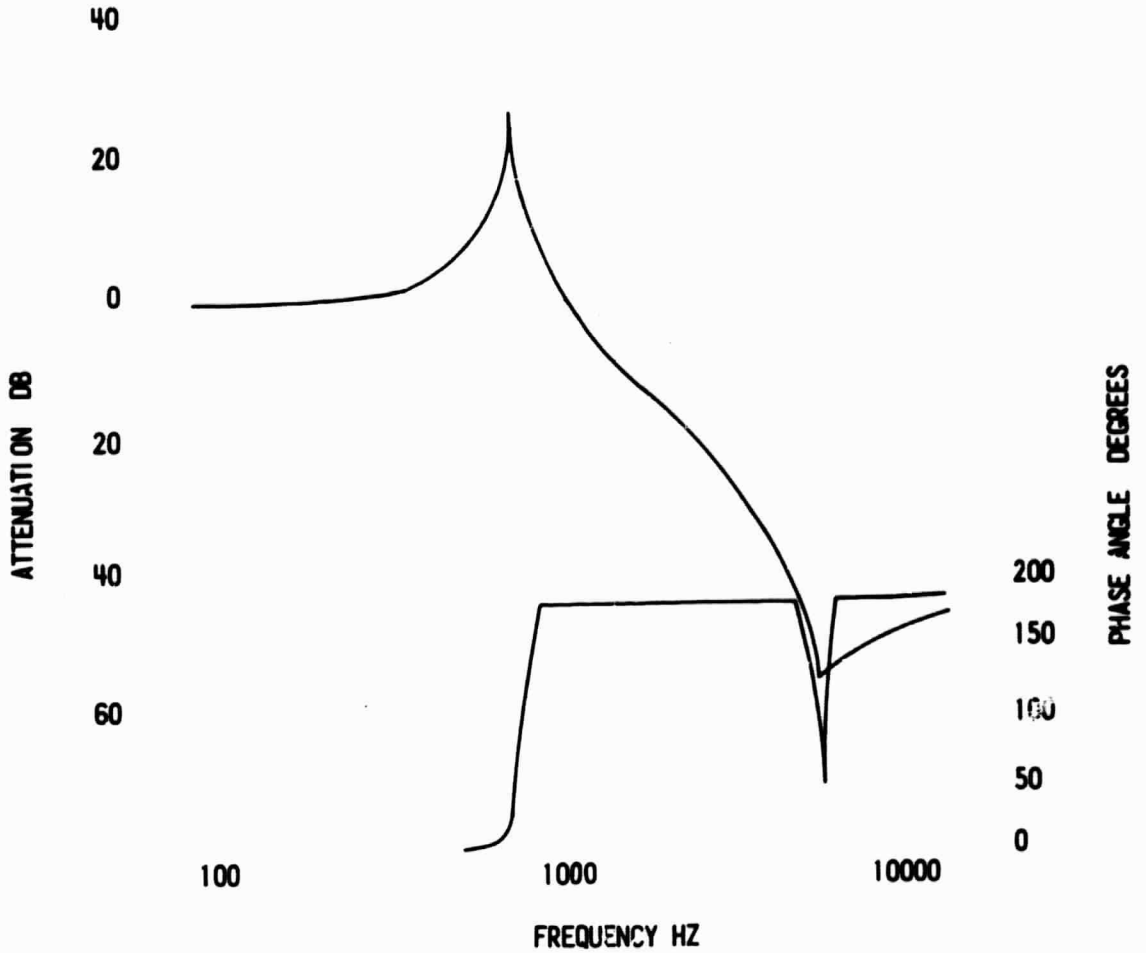


FIGURE 66
FILTER ATTENUATION AND
PHASE ANGLE

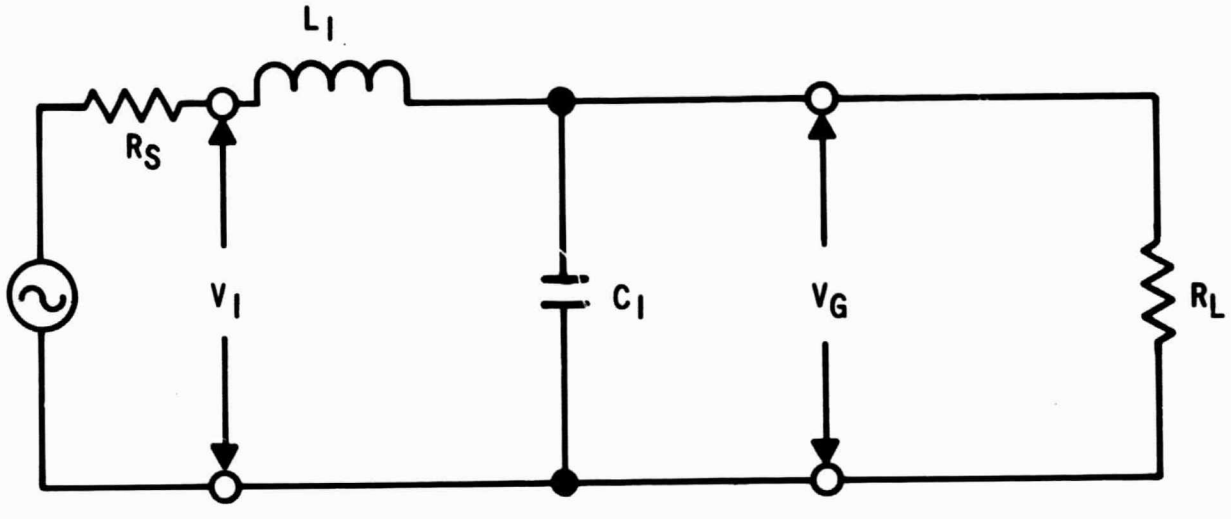


FIGURE 67
SINGLE SECTION FILTER

To perform this reduction, an impedance ratio of 14-to-1 between the inductor and capacitor at this frequency (6 KHz) is required. Allowing a 5-percent voltage drop at a full load current of 4.35 amperes rms requires an inductance of $L_1 = 560\ \mu h$. For an impedance ratio of 14-to-1 at 6-KHz requires a $C_2 = 20\ \mu f$. The voltage transfer ratio for this low-pass filter is

$$\frac{V\ out}{V\ in} = \frac{X_{C_1}}{X_{L_1} + X_{C_1}} .$$

The decibels of attenuation for this low-pass filter is equal to

$$20 \log \left| \frac{V\ in}{V\ out} \right| = 20 \log \left| \frac{X_{L_1} + X_{C_1}}{X_{C_1}} \right| .$$

The phase angle for unity power factor is calculated from

$$\phi = \tan^{-1} \frac{X_{L_1} (R_L^2 + X_{C_1}^2) - (R_L)^2}{(X_{C_1})\, R_L} .$$

Next, the voltage-ampere burden is calculated:

$$I_{400\ Hz} = \frac{E}{\left| X_{L_1} - X_{C_1} \right|}$$

$$I_{400\ Hz} = \frac{211}{\left| 1.3 - 20 \right|} = \frac{211}{18.7} = 11.3 \text{ amperes rms}$$

$$I_{5.2\ KHz} = \frac{42}{17 - 1.5} = \frac{42}{15.5} = 2.71 \text{ amperes rms}$$

$$I_{6\ KHz} = \frac{62}{20 - 1.3} \qquad \frac{62}{18.7} = 3.32 \text{ amperes rms} .$$

The last filter to be considered is a simple LC followed by a shunt trap. This filter is illustrated in Figure 68. The shunt trap is tuned to resonance at 6 KHz to attenuate the sideband components adjacent to 6 KHz. To minimize

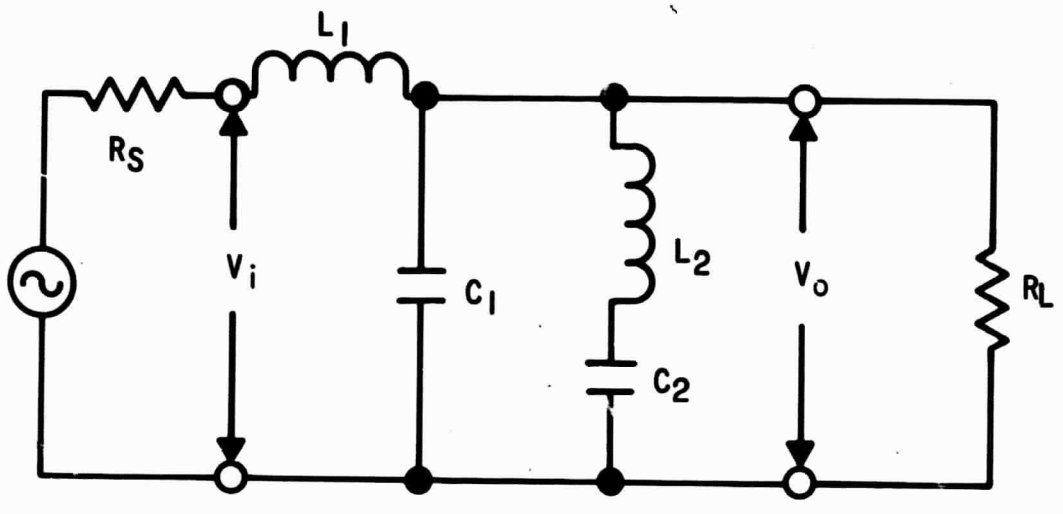


FIGURE 68
SHUNT SERIES FILTER

the circulating currents, choose L_1 to equal 1.5 mh. The reactance of C_1 is chosen to attenuate frequency components above 10 KHz. To attenuate these higher-frequency components by 10-to-1 requires the capacitive reactance of C_1 to be 1/9 the inductance reactance of L_1 at 10 KHz. Therefore, C_1 = 1.5 μf. The attenuation of this filter is expressed as

$$\text{attenuation in db} = 20 \log \frac{X_{L_1}X_{C_1} + (X_{L_1} + X_{C_1})\, X_{L_2} - X_{C_2}}{X_{L_1} \left| (X_{L_2} - X_{C_2}) \right|} .$$

F. CONTROL FUNCTIONS

The various control functions are designed for maximum size and weight reduction. To accomplish this, microcircuits have been used where possible and when they fulfill circuit requirements. Since the control circuits used are of a standard nature, it is felt that a detailed analysis of the various circuits does not add to the report. The control circuits as well as the power circuits are designed to provide maximum efficiency. It is stressed that if any advance designs are generated in the other programs they should be utilized in development of the prototype inverters. Any design changes that add to the overall operation of the inverter should be included in the final design of prototype inverters.

V. MECHANICAL DESIGN

In the design of inverters the design goal is to increase efficiency and reduce size. Inverter efficiency determines the amount of heat generated, a major factor in package design for the inverter. Package weight is a function of the volume of heat to be dissipated and the cooling means used. Package configuration is another factor which determines the overall weight of the inverter. Physical stress requirements also influence final design weight and must be considered with the configuration.

The package configuration illustrated in Figure 69 is not considered to be a final design, but is offered as a starting point for a possible final design. The final design will be developed in conjunction with NASA when detailed requirements have been fully resolved.

Figure 69 offers one possible design that is strong, lightweight and has good heat transfer to the cold plate. It is felt that the weight of this design can meet the 15-pound maximum by balancing construction techniques and materials against heat-dissipation requirements. Any input and output connector arrangement can be used according to the application. The connector shown is for illustrative purposes only.

Modular construction has been shown in this package for ease of maintenance. This type of potted or sealed construction also provides local containment of any spark or fumes that might be caused by a component failure. Modular construction also lends itself to a wide variety of configurations, depending upon space requirements. For truly lightweight unitized construction, however, the components are assembled to the base plate and the whole inverter is foamed to exclude free air. This foaming minimizes difficulties by extremely low pressure environment. Circuitry is still in a modular layout pattern as in Figure 69 and accessible by removing and repouring foam in the area affected.

A lightweight cover of aluminum that has been cased into an exo-skeletal configuration, as shown, provides good protection for components. It also helps to keep the base plate within flatness tolerances while saving weight. This cover, or a similar one, affords a high degree of accessibility and can

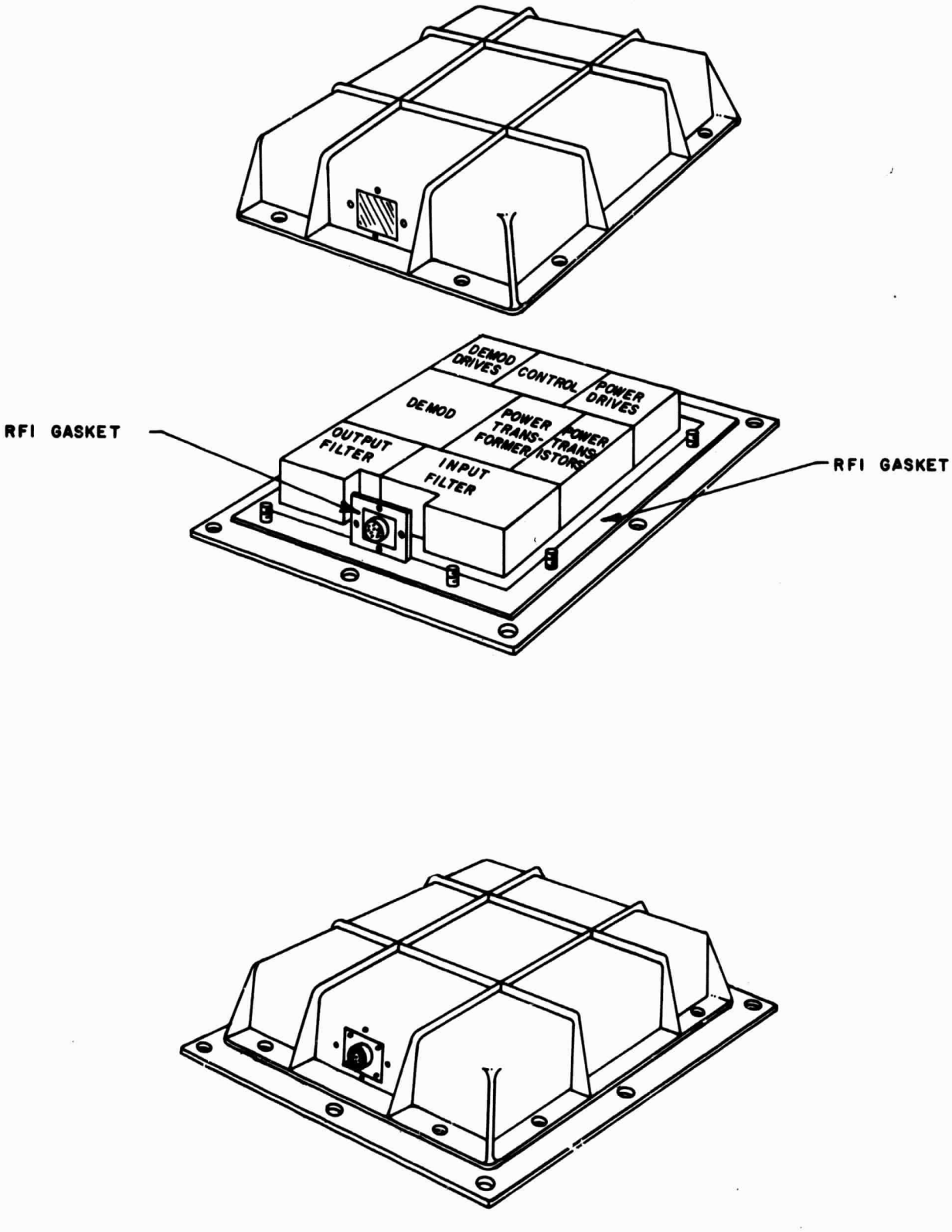


FIGURE 69
500-VA INVERTER

be designed to be removed after the inverter is installed. All components or modules are mounted to the base plate. Heat-producing parts are attached in such a manner that their heat is efficiently transferred to the base and to the cold surface. This relationship can be quite important since there is no air to carry off the slight amount of heat that some components, such as resistors, generate without this convection cooling. If these parts are bonded to a heatsink by a good conductive insulator, this problem is avoided. Cooler components last longer and are more reliable. Modules can be mounted so that they can be removed without exposing the machined surface of the base plate after installation, if this adds to the inverter design.

The heat-transfer surface of the base plate has a finish of 32 micro-inches rms maximum and is flat within 0.010 total indicator runout. The thermal conductivity of aluminum and that of the base plate are approximately 130 BTU/HR/Ft^2/F^o. Assuming that the cold plate can absorb 3 watts of heat flux per square inch and that the base plate is one square foot, then

$$3.0 \text{ watts}/1N^2 + 10.22 \text{ BTU/HR}/1N^2 + 1475 \text{ BUT/HR}/Ft^2 .$$

Thus, the heatsink is capable of absorbing 1475 BUT/HR/Ft^2 from the base plate. Assuming a full 50-percent overload of the inverter, or 185 watts dissipation, then

$$185 \times 3.4144 + 630 \text{ BTU/HR} .$$

If we dissipate this amount through one square foot of area, we have 630/1 Ft^2 + 630 BTU/HR/Ft^2, or less than half the capability of the cold plate. At the rated load the heat dissipation is 130 watts, or less than one-third the capacity. This is one area where weight reduction may be possible. Reduction of base plate area could contribute a significant weight loss.

A listing is shown in Table 9 indicating power dissipation of various circuit portions, and total power dissipation both at the 500-VA level and at the 750-VA (or 50-percent overload) condition. Inverter efficiency is also shown. It can be seen by comparing this listing with Table 10 that the heat load has been evenly distributed over the base plate. Uniform heat distribution improves thermal efficiency.

TABLE 9
POWER DISSIPATION

	500 VA	750 VA
OUTPUT FILTER	13.5	20.0
DEMODULATOR - DIODE	17.3	25.7
- TRANSISTORS	28.6	38.6
POWER STAGE - TRANSFORMER	10.6	19.1
- TRANSISTORS	20.8	34.4
DRIVES - DEMODULATOR	4.5	4.5
- POWER	7.8	7.8
CONTROL	13.6	13.6
INPUT FILTER	13.5	21.7
	130.2 WATTS	185.4 WATTS

$$\text{EFF.} = \frac{500}{630.2} = 79.5\% \text{ @ } 500 \text{ VA}$$

$$= \frac{750.0}{935.4} = 80.1\% \text{ @ } 750 \text{ VA}$$

TABLE 10
WEIGHT ANALYSIS

VOLTAGE SENSING TRANSFORMER	.25 lbs.
POWER STAGE DRIVE TRANSFORMER	.35 lbs.
SUB DRIVE TRANSFORMER	.25 lbs.
SUB DRIVE TRANSFORMER	.25 lbs.
POWER TRANSFORMER	2.25 lbs.
CURRENT TRANSFORMER	.0625 lbs.
DEODULATOR DRIVE TRANSFORMER	.25 lbs.
ILLUSTRATED COVER & BASEPLATE ASSY.	4.50 lbs.
INPUT FILTER ASSY.	4.00 lbs.
OUTPUT FILTER ASSY.	1.20 lbs.
TRANSISTORS - CIRCUITRY	2.00 lbs.
TOTAL	15.36 lbs.

ABOVE BASEPLATE IS 144 SQUARE INCHES IN AREA.

The final weight cannot be calculated until the ultimate configuration is known; however, an approximate figure can be reached by examining Table 10 which lists the magnetic components, case, and other components and their weights. The package design given in this discussion offers a good reference until the final design is determined; however, the weight listing indicates that other configurations would also fall into this weight range.

VI. RELIABILITY ANALYSIS

A. Preliminary Reliability Analysis

A preliminary reliability analysis, summarized in Table 11 indicates a MTBF of 10,542 hours for the inverter. MIL-HDBK-217A, dated December, 1965 was used for the analysis calling for a temperature of 71°C and stress levels normally employed. Application K factors for "ground" were used to adjust generic failure rates since MIL-STD-756A depicts orbit and ground environmental stress as being equal. Launch stress was not considered in the preliminary analysis due to the short duty cycle and relative insignificance. This design represents a reliability improvement over the state of the art of approximately 10 percent to 15 percent, attributed primarily to the employment of integrated circuits in the control circuitry.

B. Reliability Discussion

Review of the preliminary design indicates that parts are conservatively rated and applied in accordance with good reliability practices. At this stage of the design, proper parts selection is possibly the most important reliability consideration. For this reason, NASA Publication PPD-600 was consulted as the primary source of part selection due to the thorough screening of semiconductors required and careful consideration of other parts, and vendor selection. Most of the part requirements not included in PPD-600 were selected from the MIL-R-38100A series (established reliability parts). Recently developed parts required for state-of-the-art performance are employed on a trade-off basis. Design techniques such as chopper regulation and digital circuitry application are employed in an effort to reduce stress level and reduce failures due to parameter drifts. Redundancy formulas were derived by summing the appropriate number of terms of the binomial expansion of $(R + q)^2$ (R = reliability of a single component or system, q = unreliability, and n = number of redundant components or systems in the configuration). Example:

TABLE 11
RELIABILITY ANALYSIS SUMMARY

COMPONENT TYPE	QUANTITY (Q)	GENERIC FAILURE RATE FAILURES/10^6HOURS (GFR)	APPLICATION FACTOR (K)	TOTAL ADJUSTED FAILURE RATE FAILURES/ 10^6 HOURS (Q X GFR X K)
SECTION A1				
COMPOSITION RESISTORS	6	0.006	6	0.216
POTENTIOMETER	1	1.470	1.0	1.470
POWER TRANSISTORS	2	0.820	1.0	1.640
SIGNAL TRANSISTORS	3	0.195	1.5	0.876
DIODES	5	0.195	1.0	0.975
ZENER DIODES	2	0.580	1.0	1.160
INDUCTOR	1	0.250	1.5	0.338
TANTALUM CAPACITORS	5	1.200	0.5	3.000
				9.675
SECTION A2				
INTEGRATED CIRCUIT (MIC)	5	0.400	1.0	2.000
COMPOSITION RESISTORS	21	0.006	6.0	0.756
POTENTIOMETER	4	1.470	1.0	6.960
TANTALUM CAPACITORS	2	1.200	0.5	1.200
CERAMIC CAPACITORS	10	0.010	1.0	0.100
SIGNAL TRANSISTORS	8	0.195	1.5	2.340
ZENER DIODES	2	0.580	1.0	1.160
DIODES	3	0.195	1.0	0.585
				15.010
SECTION A3				
MIC	3	0.400	1.0	1.200
COMPOSITION RESISTORS	28	0.006	6.0	1.008
POTENTIOMETER	6	1.470	1.0	8.820
CERAMIC CAPACITORS	10	0.010	1.0	0.100
DIODES	7	0.195	1.0	1.365
SIGNAL TRANSISTORS	10	0.195	1.5	2.925
				15.418
SECTION A4				
COMPOSITION RESISTORS	27	0.006	6.0	0.972
CERAMIC CAPACITORS	3	0.010	1.0	0.030
DIODES	2	0.195	1.0	0.390
SIGNAL TRANSISTORS	12	0.195	1.5	3.510
POWER TRANSISTORS	6	0.820	1.0	4.920
TRANSFORMERS	3	0.250	1.5	1.125
				10.947
SECTION A5				
COMPOSITION RESISTORS	28	0.006	6.0	1.008
POWER TRANSISTORS	14	0.820	1.0	11.480
SIGNAL TRANSISTORS	4	0.195	1.5	1.170
SIGNAL DIODES	14	0.195	1.5	4.095
POWER DIODES	18	0.900	1.0	16.200
TRANSFORMERS	10	0.250	1.5	3.750
INDUCTORS	3	0.250	1.5	1.125
TANTALUM CAPACITORS	2	1.200	0.5	1.200
INDUCTORS	3	0.250	1.5	1.125
TANTALUM CAPACITORS	3	1.200	0.5	1.800
CERAMIC CAPACITORS	9	0.010	1.0	0.010
TRANSFORMERS	2	0.250	1.5	0.750
				7.713
			TOTAL	94.854

Develop redundancy formula for system employing six redundant components, requiring four components for mission success:

$$R_s = \sum_{n=0}^{n=2} (R_s + q)^6 = \underset{\text{Oth Item}}{R^6} + \underset{\text{1st Item}}{7R^5 q} + \underset{\text{2nd Item}}{\frac{30}{2!} R^4 q^2} + \text{-----} q^6.$$

Summing through the second team:

$$R_s = R^6 + 6R^5 q + 15 R^4 q^2.$$

Substituting $q = 1-R$

$$R_s = R^6 + 6R^5 (1-R) + 15R^4 (1-R)^2$$

$$= R^6 + 6R^5 - 6R^5 + 15R^4 - 30 R^5 + 15 R^6$$

$$R_s = 10 R^6 - 24 R^5 + 15 R^4.$$

Since the versatility of the unit allows a number of failure-detection and switching techniques to be employed in a redundant system, the worse-case situation of operating redundancy is depicted in all cases. Detection and switching circuitry is not considered. In most cases of multiple redundant systems, failures of more than the allowed number of units would not constitute a catastrophic failure but only inadequate power which could be compensated. The probability of complete loss of power in any one of the examples is extremely remote.

The primary virtue of the proposed inverter is its versatility. Considering only the attributes to the reliability consideration, a few of the redundance schemes which could be employed are discussed:

1) Paralleling single units for single-phase high-power requirements. Units could be paralled for power requirements with additional units added in a redundance configuration to meet reliability requirements. Simple circuitry could be employed to detect a failure (such as high or low voltage, phase shift, and high distortion) and remove it from service.

Example:

If 2KVA of power is required with a reliability of .999 for a fourteen-day mission, six 500-VA units in a synchronized, redundance configuration would meet the requirement. Reliability of a single unit for fourteen days (336 hours) :

$R_s = e^{-\lambda t}$ -.9686

λ = 94.854 failures / 10^6 hours

t = mission time fourteen days.

Reliability of six units in operational redundance with four units being required for mission success (neglecting detection and switching):

$$R_p = 10\,R_s^6 - 24\,R_s^5 + 15\,R_s^4 = 9994.$$

2) Paralleling single units for three-phase operation. Units could be paralleled for three-phase operation with additional single units added in a redundancy configuration to meet reliability requirements.

Conventional redundance in a three-phase system would require a completely redundant three-phase power supply and complex failure-sensing and switching circuitry for a workable system. Redundance may be effected, however, with the proposed three-phase system by the addition of single units and simple failure-detection and switching circuitry. Quantitative examples are discussed:

Example: For a fourteen-day (336 hours) mission:

Reliability of a single unit:

$$R_s = 3^{-\lambda t} - .9686.$$

Reliability of a three-phase system employing three single units:

$$R_3 = e^{\lambda 3t} = .9087.$$

Reliability of a three-phase system employing four single units:

$$R_4 = 4\,R_s^3 - 3\,R_s^4 = .9942.$$

Reliability of a three-phase system employing five single operating units (neglecting detection and switching):

$$R_5 = 6R_s^5 - 15R_s^4 + 10R_s^3 = .994.$$

3) **Paralleling units for three-phase operation with higher power requirements. Single units could be paralleled for three-phase operation where additional power is required with single units added on for redundancy.**

Example:

If 3-KVA of three-phase power is required for a fourteen-day (366 hrs) mission:

Reliability of a single unit:

$$R_s = .9686.$$

Reliability of a three-phase, 3-KVA system employing six single units:

$$R_6 = R_s^6 = .8258.$$

Reliability of a three-phase, 3-KVA system employing seven single operating units (neglecting detection and switching) :

$$R_7 = 7R^6 - 6R^7 = .9814.$$

Reliability of a three-phase, 3-KVA system employing eight single operating units (neglecting detection and switching)

$$R_8 = 21\ R^8 - 48R^7 = 28R^6 = .9984.$$

VII. DESIGN RECOMMENDATIONS

The available information developed in the state-of-the-art study shows that Phase-Demodulated High-Frequency Inverters offer a basic design which fulfill the design requirements of the proposed multi-purpose inverter. Some of the basic requirements are more difficult than others, but it is felt that by proper care in the final design stages, the objective can be met. The following design recommendation is basically a step-by-step presentation of the design specification (Section 5 of the Work Statement for Static Inverter Development). Each paragraph is covered and changes or recommendations are made when it is felt that the changes or recommendations result in an improved inverter design.

The following recommendations are based on a single-phase inverter with a 500-VA full-load rating. The single-phase units are capable of parallel, three-phase, and parallel three-phase operation through external interconnection with no readjustment of internal controls. The recommendations are divided into two sections:

1. Design Goals
2. Design Requirements .

1.2.0 Design Goals

The following limits are submitted as goals which appear possible and can most likely be accomplished or exceeded. Also, listed with each goal is the design limit which must be met in the event the design goal is not accomplished.

1.2.1 Efficiency

a. At full-rated load

-design goal 80 percent
-design requirement 75 percent

b. At 40-percent full-rated load

-design goal 60 percent
-design requirement 50 percent.

NOTE: Full rated load 500 volt ampere

$$\text{Efficiency} = \frac{\text{Power out (watts)}}{\text{Power in (watts)}\ (100)}$$

Efficiency calculation should be based on unity PF at light load conditions and on 0.85 PF at full load.

1.2.2 Weight

-design goal 14.0 pounds
-design requirement 17.0 pounds maximum.

1.2.3 Dimensions

The final assembly configuration is to be determined by NASA and the contractor during the development programs (Phase II). It is noted that the design configuration is the determining factor in the final weight; however, it is felt that the design goal of 15 pounds can be met.

1.2.4 Acoustic Noise

The generated acoustic noise must be below the following design goals:

a. Sound Pressure Level : 65 db max broadband noise from 20-10,000 cps.

b. Speech Interference Level: 40 db max.

1.2.5 Reliability

The inverter must be designed to achieve a minimum reliability of 0.960 based on 400 hours of operation at the environments specified herein.

2.1.0 Design Requirements

2.1.1 Mission Life

The inverter must be designed to have a total mission life of 1200 hours of operation.

2.1.2 Factor of Safety

Each electrical element within the inverter must be rated to withstand abnormal parameter variations up to 1.5 times normal rated levels.

2.2.0 Electrical Characteristics

2.2.1 Input Voltage - 28 volts DC plus or minus 4 volts.

2.2.2 Input Ripple

Less than 1.5 volts rms as per MIL-STD-704, Paragraph 5.2.2.

2.2.3 Input Transients

Inverter shall withstand 80 volts DC for 10 microseconds, and 40 volts DC for 1 second without damage.

2.2.4 Turn-ON Transient

The turn-ON transient after two milliseconds from turn ON with the input voltage as specified in 5.3.3.1 and full rated load and power factors can not exceed 300 percent of the steady-state value for the same conditions. Stabilization to within 10 percent of the steady-state values of input current and output voltage must occur within 100 milliseconds. The inverter must stabilized to the performance conditions of this specification within 5 seconds after turn ON under all rated combinations of line, load, and environment.

NOTE: The input filter discussed in Section IV E is designed to block the 80-volt DC transient and to limit the inrush current not to exceed 300 percent full load current.

2.2.5 Loss of Input Power

It is recommended that this be restated as follows:

The unit shall be designed so as not to be damaged by removal of input voltage or reduced input voltage. The inverter design

does not contain the required circuitry to accomplish this; however, it is felt that this should be included to protect the inverter from low input voltage.

2.2.6 Three-Phase Output Voltage

115 volts rms plus or minus 1 percent line to neutral (3-phase, 4-wire systems) over rated load, input, and environmental conditions.

2.2.7 Output Voltage Transient

The output voltage shall remain within 115 Vrms plus or minus 10 percent for any step load or line change within the specified normal limits. Recovery to steady-state limits must be within 2.5 m-seconds. Transient voltage in excess of 225 volts peak must not appear at the output under any condition.

2.2.8 Output Voltage Modulation

As per MIL-STD-704, paragraph 5.1.3.6 except that maximum amplitude must not exceed 2.0 volts peak.

2.2.9 Output Frequency Modulation

The output frequency modulation must not exceed 0.5 cycles per second under any load and power factor combination specified herein.

2.2.10 Load

0-500 volt amperes (VA) per module based on three modules per each three-phase inverter.

2.2.11 Power Factor

a. All load levels: 0.65 lagging to 0.80 leading.
b. 0 to 30 percent of rated load: 0.8 to 0.1 leading.

2.2.12 Overload

The inverter must be capable of withstanding a 150-percent overload for a 10-minute period while supplying an output voltage within the limits of paragraph 2.2.6. The inverter will be protected from a 20-second overload or short circuit condition and must return to normal operation automatically upon the removal of the overload or short circuit. It is recommended that the 14-ampere reference be removed, unless it is necessary, to allow more freedom in design.

2.2.13 Frequency

a. External Synchronization: 400 cps, plus or minus 1 percent. Signal Characteristics:

1. Frequency: 6400 pps.
2. Duty Cycle: 50 percent, plus or minus 1 percent.
3. Amplitude: Pulse ON: +3.0 volts, plus or minus 0.5 volts.
   Pulse OFF: 0 volts, plus 0.5 minus 0 volts.
4. Frequency Stability: 10 parts per million.
5. Source and inverter impedances: 100 ohms, plus or minus 10 percent.
6. Rise Time: 1.0 microsecond.
7. Decay Time: 1.0 microsecond.

b. Free-Running Mode: 400- cps, plus or minus 2 percent.

2.2.14 Waveform

As specified in MIL-STD-704, Paragraph 5.1.3.5.

2.2.15 Isolation

The AC output and DC input must be electrically isolated from each other and from the case except for Radio Frequency Interference feed-through capacitors which may be grounded to the case. No breakdown shall occur when 400 volts DC is applied between the input power terminals and the inverter case, and 750 volts DC between the AC output terminals and the case.

2.2.16 Ripple Generation

The inverter must not superimpose onto the DC input line any voltage in excess of 0.5 volts peak between DC and 15 KC when measured across an input source with an impedance of 500 milliohms. (This requirement can be met, however, weight and size can be reduced if the source impedance is reduced or the ripple voltage raised. The source impedance should be related to frequency, if possible, to make it possible to design an input filter that provides optimum performance with a minimum weight.)

2.2.17 Motor Starting

The inverter must be capable of starting an induction motor load while simultaneously supplying 60 percent of its rated output. The motor load shall be simulated by connecting two fans (Rotron Manufacturing Company Type AXIMAX-3, single-phase, motor series 528YS) in parallel across the output and disconnecting one of the fans after 5 seconds. The fans start simultaneously.

2.2.18 Parallel and Three-Phase Operation

The individual single-phase inverters must be capable of being interconnected for any combination of parallel and/or three-phase operation. (It has been assumed that parallel and three-phase operation must be through external connection only and that no control or power readjustments are required or permitted. This is not stated and should be if it is a requirement. If it is not, then the proposed design could be simplified.)

2.2.19 Electromagnetic Interference

The equipment must meet the design, quality assurance testing, and documentation requirements of MIL-I-26600 and MSC addendum ASPO-EMI-10A. In case of a conflict in specification, the tests and requirements specified in MIL-I-26600 and MSC addendum ASPO-EMI-10A can not be superseded by any other test or requirement included in these specifications. (This requirement does not pose the normal problem due to nature of the design. The recommended design does not have the problems associated with low-frequency ripple due to the nature of its design (illustrated in Appendix B).)

2.2.20 Dielectric Strength

Electrical parts and subassemblies prior to being wired must be capable of withstanding an electrical potential of 1500 volts rms, 60 cps in accordance with MIL-STD-202, Method 301 between insulated points and case, without electrical breakdown. Criterion of Failure:

a. Breakdown, or
b. Current flow in excess of 500 microamps.

All items which cannot be tested for dielectric strength will be subject to approval.

2.2.21 Protective Devices

Protective devices which require replacement or manual resetting are not to be used.

2.3.0 Mechanical Characteristics

2.3.1 Thermal Requirements

a. The major heat-dissipating elements of the power inverter must be mounted on a heatsink, one surface of which must be exposed on the module for external conduction cooling. For design purposes the inverter assembly is considered thermally isolated from all conducting structures. Spacecraft mounting surface must have at least 200 square inches of contact area.

b. Heat Flow - Maximum allowable heat flux in any portion of the inverter: 3.0 watts per square inch.

c. Thermal Conductivity - Heatsink to cold plate: 100 BUT/HR/Ft^2/^oF.

d. Heatsink surface:
   Finish: 32 microinches rms max.
   Flatness: Within 0.010 inches total indicated run out.

2.3.2 Sealing

The inverter must be designed such that those portions of the circuit that will burn, spark, or outgas because of electrical overload or short circuit are hermetically sealed or potted. Potting must be of the closed-cell foam type which does not support combustion.

2.3.3 Vibration Isolators

The inverter must be designed such that vibration isolators are not required.

2.4.0 Environmental

2.4.1 Temperature Limits

a. Operating Ambient: 0-160°F
b. Cold Plate Coolant Temperature: 35°F min to 135° F max.

2.4.2 Temperature Sensors

Temperature sensors must be incorporated at critical points to provide an external indication of excessive temperature conditions. The temperature sensors must be provided as shown necessary by the reliability and maintainability studies to be performed during the Development Stage.

2.4.3 Thermal Vacuum

The inverter will be exposed to a vacuum of 1.0×10^{-5} millimeters Mercury. The unit must be operated at full load over the ambient temperature range given in 5.3.5.1a.

2.4.4 Shock

The unit must be capable of withstanding a peak acceleration of 20g. The shock pulse waveform will be a sawtooth with an 11 millisecond rise time and a 1 millisecond decay. The unit will be operating during this test and must remain within specified tolerances.

2.4.5 Vibration

a. Sinusoidal: 5-100 cps - Linear increase from 0.3g at 5 cps to 8.5g at 100 cps.
100 - 300 cps - 8.5g.
300 - 2000 cps - Linear decrease from 8.5g at 300 cps to 5g at 2000 cps.
Sweep Rate: 1/2 octave per minute for 2 cycles in each of three mutually perpendicular axes.

b. Random: 20-85 cps - 0.041 g^2/cps
85 - 100 cps - 12db/oct rise.
100 - 1000 cps - 0.078g^2/cps.
1000 - 1200 - 12 db/oct roll-off.
1200- 2000 - 0.041g^2/cps.
Vibration in three mutually perpendicular axes, 17 minutes in each axis.
Ambient temperature: 160°F.
Inverter will be operated and must remain within specified tolerances.

2.4.6 Acoustic Susceptibility

The inverter must be capable of withstanding a sound pressure level of 140 db overall with a frequency range of 4.7 to 9,600 cps.

2.4.7 Test Points

An adequate number of test points must be provided for each sub-assembly to facilitate isolation of faults in the inverter.

APPENDIX A

BIBLIOGRAPHY

Reference No.	Title	Author
1	"Commutation Analysis"	
2	"A High-Power DC/DC Static Converter . . . Electrical Engineering, Nov. 1963	D. L. Duff A. Ludbrook
3	"A New Frequency Multiplier" . . . . . Electrical Engineering, Sept. 1962	Marvin Camras
4	"Filters in Electronics" . . . . . Westinghouse Engineer, March 1963	Anatol I. Everev
5	"Square Waves Produce Sine Waves". . . . . EDN Design Ideas (RS 770), Dec. 1963	J. A. Rose
6	"Static Magnetic Frequency Multiplier" . . Patent #2,911,582, Nov. 3, 1959	H. L. Kellogg
7	"Magnetic Frequency Converter" . . . . . Patent #2,913,596, Nov. 17, 1959	Hugh M. Ogle
8	"Cyclo Converter Frequency Converters" . . (For F. Eastman, USN)	Louis Allis Co.
9	"Overload Protection for Transistor Voltage Regulators". . . . . Electronics, Dec. 23, 1960	Allan G. Lloyd
10	"RFI-Less Switching with SCRs" . . . . . EEE, March 1964	F. W. Gutzwiller
11	"Effect of Operating Frequency on Missile Alternators" . . . . . Electrical Engineering, August 1959	R. E. Turkington
12	"Switching Circuits Using the Gate Turn-Off Controlled Rectifier" . . . . . EEE, March 1963	J. W. Motto, Jr.
13	"Phase Control of SCRs with XFMR and Other Inductive AC Loads". . . . . Application Note (200.31, 3/63)G.E.	F. W. Gutzwill J. D. Meng
14	"How to Design Practical SCR Circuits" . . Electronic Design, May 24, 1962	D. A. Pisarcik

Reference No.	Title	Author
15	"Power Control with Semiconductor Devices". Control Engineering, Sept. 1961	B. Mokrytzki R. Murray R. Putkovich D. A. Pisarcik T. E. Ebert
16	"Circuit Design and Application of High Power Silicon Rectifiers" . . . . . Semiconductor Diode Source Book	N. A. Forbes
17	"Selecting the Proper High Voltage Rectifier" . . . . . Electronic Design, Sept. 13, 1963	Chet Schuler
18	"Capacitors for SCR Commutation Applications". . . . . Product Data, G.E. ((GC-1556A)	
19	"Now the Gate Turn Off Switch Speeds VP D-C Switching". . . . . Electronics, March 23, 1964	Dennis R. Graff
20	"Peak Current Considerations for RCA Silicon Controlled Rectifier Applications" Application Note SMA-19, RCA	J. Neilson
21	"Characteristics of the Gate Controlled Turn-Off Transistor Controlled Rectifier . IEEE Conference Paper #CP63-510	J. W. Motto,Jr.
22	"Increasing Power and Frequency with General Electric's New Line of High-Speed SCRs and Power Diodes" . . . . . Application Note #200.37 (3/64) - G.E.	Neville Mapham
23	"Extending the Upper Frequency Limit of SCR Inverters by Using the Time-Series Circuit" . . . . . Application Note - (2/63) - G.E.	Neville Mapham
24	"Adjustable Speed A-C Drive with SCR Frequency Inverters" . . . . . Electro-Technology, August 1963	Thomas E. Usher Charles D. Beck
25	"Design of a Silicon Controlled Rectifier High Frequency Inverter" . . . . . Semiconductor Products, Sept. 1962	Neville Mapham
26	"A High-Voltage SCR Pulse Inverter". . . . Electro-Technology, June 1962	A. A. Vagge

Reference No.	Title	Author
27	"Series Transistor Controls SCR" . . . . . EDN	
28	"A Semiconductor Variable-Speed A-C Motor Drive" . . . . . Electrical Engineering	D. C. Griffith R. M. Ulmer
29	"A 50 KVA Adjustable Frequency 24-Phase Controller Rectifier Inverter" . . . . . IRE Transactions on Industrial Electronics May 1962	C. W. Flairty
30	"Replacing Sine Wave Sources with Solid-State Inverters"	Donald Levy
31	"A High Frequency Power Generator Using SCRs". . . . . Solid State Design, April 1963	Neville Mapham
32	"Three-Phase Static Inverters Power Space-Vehicle Equipment" . . . . . Electronics, May 5, 1961	Raymond J. Kearns Joseph J. Rolfe
33	"A High Power DC-AC Inverter with Sinusoidal Output" . . . . . Electronic Engineering, Sept. 1961	George Salters
34	"Transistor Controlled Rectifier, Single-Phase DC to AC Static Power Inverter Application" . . . . . Report AR4, Issue 2, Westinghouse	
35	"A Semiconductor Converter of Direct Current Into Three Phase Current". . . . . ASTIA #FTD-TT-61-43 Oct. 4, 1961	P. O. Azbelev
36	"An Audio-Frequency High-Power Generator Employing Silicon Controlled Rectifiers" . AIEE Paper #3889 E, May 1962	R. Thompson
37	"Static AC Adjustable Frequency Drives". . Control Engineering, April 1964	H.K. Hulstrand
38	"SCR Phase Control of Inductive Loads" . . Electro-Technology, April 1964	F. W. Gutzwiller
39	"How To Use Silicon Controlled Rectifiers In Series Or Parallel" . . . . . Control Engineering, May 1964	A. R. Mulica

Reference No.	Title	Author
40	"Developing True Solid-State Static Alternators" . . . . . Electronics, May 24, 1963 pp 58-61	R. H. Murphy
41	"Frequency-Changer Systems Using the Cycloconverter Principle". . . . . AIEE Trans. Applications and Industry May, 1963	R. A. Van Eck
42	"Switching Power Supply Regulators for Greater Efficiency". . . . . Electronic Design, June 22, 1964	Seymour Levine
43	"Static Inverter with Neutralization of Harmonics". . . . . AIEE Conference Paper EP 61-891	Andress Kernick J. L. Roof T. M. Heinrich
44	"Selected Harmonic Reduction in Static DC-AC Inverters" . . . . . IEEE Transaction Paper No. 63-1011	F. G. Turnbull
45	"How to Trigger SCRs Sequentially" . . . . Electronic Design, Sept. 27, 1963	R. Thompson
46	"Optimization Study of High Power Static Inverters & Converters". . . . . NASA Report-TRW Electromech Div. Contract No. NAS3-2785 Thompson Ramo Wooldridge, Inc. (3 Qtrly Reports)	NASA (Arthur B. Larsen) (James E. Murray)
47	"Step-Up Frequency Changer". . . . . AIEE Transaction Paper 60-1043	R. J. Wurm L. J. Stratton
48	"Single-Phase to Polyphase Converters" . . Electronic Technology, Oct. 1961	F. Butler
49	"A Static Electronic Frequency Changer". . IRE Int Conventional Rec v9 pt5 (Aerospace & Navigational Electronics,etc.) 1961 P 342-8	R. M. Ulmer D. C. Griffith
50	Self-Locking Polyphase Transistor-Magnetic Inverter" . . . . . AIEE Conference Paper T121	J. A. Bennett C.H.R. Campling

Reference No.	Title	Author
51	"A Silicon-Controlled Rectifier Inverter With Improved Commutation" . . . . . AIEE Conference Paper 61-718	W. McMurray D. P. Shattuck
52	"Half-Bridge Inverter Provides Economical Three-Phase Power" . . . . . Electronic, Sept. 15, 1961	Allan G. Lloyd
53	"Three-Phase Inverter with Feedback Loops" Electronics, March 23, 1962	Temple J. Gilliam
54	"Static Inverter Delivers Regulated Three-Phase Power" . . . . . Electronics, July 8, 1960	Manfred Lilienstein
55	"Frequency Septupler Provides Stable 420-cps Voltage" . . . . . Electronics, May 3, 1963	Wm. A. Geyger
56	"Adjustable-Frequency Power Inverter Systems for Industry". . . . . Westinghouse Engineer, Nov. 1963	C. G. Helmick K. Lipman
57	"What's Available Today in Frequency Changers". . . . . Product Engineering, Dec. 24, 1962	Ante Lujic Michael S. Inove
58	"Static Inverter Design Considerations". . Electrical Engineering, April 1963	Charles B. Brahm
59	"Artificial Commutation of Static Converters" . . . . . AIEE Conference Paper #62-1392	J. R. Toth J. D. Schoeffler
60	"Static Inversion Based on Duty Cycle Modulation". . . . . IEEE Transaction	Bobo Kruger D. J. Hancock
61	"Transistor Converters for the Generation of High-Voltage Low-Current DC Supplies" . AIEE Conference Paper #2929E	C. A. Yarrow
62	"Designing Series SCR Inverters" . . . . . Electronic Design, June 7, 1963	R. Thompson

Reference No.	Title	Author
63	"Transistorized Three-Phase Power Supplies". . . . . Electronic Industries, Jan. 1959	Wm. Brannian
64	"How To Use SCRs in Power Supplies". . . . Electronic Design, Oct. 1, 1961	A. C. Leenhouts
65	"Transistorized SCR Firing Circuits" . . . Mullard Technical Communications, Vol. 7, No. 75, June 1963	T. J. Jarratt
66	"Switch-Off Circuits for SCRs Operating on DC" . . . . . Mullard Technical Communications Vol. 7, No. 65, June 1963	R. A. Payne
67	"Precise Phase Angle Control of SCRs". . . Mullard Technical Communications Vol 7, No. 65, June 1963	R. A. Payne
68	"New High Power DC Converter Circuits" . . Mullard Technical Communications Vol. 5, No. 43, April 1960	
69	"Electronic Three-Phase Wave Generator". . Patent #2,916,687	D. L. Cronin
70	"Solid State Power Stage Amplifier Employing Silicon Rectifiers and Half-Cycle Response Magnetic Amplifiers" . . . . . Patent #25,574, May 12, 1964	E. W. Manteuffel
71	"Semiconductor Inverter Circuit with Means to Preset the Core Flux of the Transformer" Patent #3,133,241, May 12, 1964	J.R. Cole etal (Joe W. Walton)
72	"Signal Controlled Inverter Power Amplifier" Patent #3,103,616, Sept. 10, 1963	J. R. Cole etal (Joe W. Walton)
73	"Inverter Circuit Utilizing Silicon Controlled Rectifiers and Modulating the Output with a Derive Difference Voltage" . Patent #3,124,740, March 10, 1964	P. D. Corey etal (Armistead L. Wellford)
74	"Apparatus for Converting DC Power to AC Power". . . . . Patent #3,125,725, March 17, 1964	J. B. McCarthy Clifton

Reference No.	Title	Author
75	"Regulated Voltage Converter Circuit". . . Patent #3,135,909, June 2, 1964	R.E.D.Anderson (R.J. Projain)
76	"Inverter Circuit" . . . . . Patent #3,047,789, July 31, 1962	H. R. Lowry
77	"Electrical Apparatus" . . . . . Patent #2,470,975, May 24, 1949	W. H. Bussey
78	"Inverter" . . . . . Patent #2,872,635, Feb. 3, 1959	F. Lawn
79	"Static Power Inverter". . . . . Patent #3,024,373, March 6, 1962	H. I. Seike
80	"Controlled Rectifier Inverter Circuit". . Patent #3,034,015, May 8, 1962	H. E. Schultz
81	"Three-Level Inverter Circuit" . . . . . Patent #3,060,330, Oct. 23, 1962	K. M. Trampel
82	"DC to AC Converter" . . . . . Patent #3,051,914, Aug. 28, 1962	J. H. Brown
83	"Voltage Regulator". . . . . Patent #3,018,432, Jan. 23, 1962	M. Palmer
84	"Motor Control Systems". . . . . Patent #2,939,064, May 31, 1960	J. W. Momberg etal (Edward W. Taylor)
85	"Magnetic Amplifier Control Circuitry for Gated Electronic Switches and Application to Lighting Loads" . . . . . Patent #2,998,547, Aug. 29, 1961	B. Berman
86	"Self-Regulated Static Frequency Converter" . . . . . Patent #3,088,065, Apr. 30, 1963	E.W. Manteuffel
87	"Static Inverter Circuit". . . . . Patent #3,096,472, July 2, 1963	L. J. Elliott etal (Thomas C. Ward)
88	"Frequency Multiplier" . . . . . Patent #3,099,784, July 30, 1963	H. E. Forsha etal (Sidney M. Kapell)
89	"High Frequency Power Supply System" . . . Patent #2,623,203, Dec. 23, 1952	G. W. Demuth

Reference No.	Title	Author
90	"Magnetic Pulse Doubling Circuit". . . . . Patent #2,814,737, Nov. 26, 1957	J. E. Sunderlin etal (Roy E.Lee)
91	"Three Phase Power Supply" . . . . . Patent #2,899,572, Aug. 11, 1959	C. W. Skelton etal Wm. T. Donnell
92	"Three Phase Power Supply System". . . . . Patent #2,898,412, Aug. 4, 1959	J. S. Lin.
93	"Static Frequency Converter" . . . . . Patent #2,820,942, Jan. 21, 1958	M. Depenbrock
94	"Frequency Multiplier" . . . . . Patent #2,666,178, Jan. 12, 1954	W. Kramer
95	"Frequency Changer". . . . . Patent #2,418,640, Apr. 8, 1947	H. M. Huge
96	"Transistor Converter with Self-Starting Circuit" . . . . . Patent #3,145,348, Aug. 18, 1964	R. P. Massey
97	"DC Power Supply for Isolated Loads" . . . Patent #3,145,305, Aug. 18, 1964	L. Levy
98	"AC Static Switching Circuit". . . . . Patent #3,145,266, Aug. 18, 1964	J. D. Owen
99	"Control Circuitry". . . . . Patent #2,910,641, Oct. 27, 1959	J. L. Boyer
100	"System for Supplying Controlled Frequency Power" . . . . . Patent #2,967,252, Jan. 3, 1961	R. F. Blake
101	"Signal Frequency Converter" . . . . . Patent #2,963,660, Dec. 6, 1960	G. H. Towner
102	"Signal Frequency Converter" . . . . . Patent #2,816,062, Dec. 17, 1957	G. H. Towner
103	"Electric Valve Frequency Changer" . . . . Patent #2,288,363, June 30, 1962	E. D. McArthur
104	"Electric Valve Converting System" . . . . Patent #1,957,230, May 1, 1934	C. A. Sabbah etal
105	"Electric Valve Frequency Changer" . . . . Patent #2,319,072, May 11, 1943	E. D. McArthur

Reference No.	Title	Author
106	"System for Supplying Controlled Frequency Power" . . . . . Patent #2,899,566, Aug. 11, 1959	C. C. Ware etal
107	"Frequency Converter". . . . . Patent #2,481,132, Sept. 6, 1949	M. A. Lissman
108	"Variable Pulse Width Parallel Inverters". Patent #3,075,136, Jan. 22, 1963	D. V. Jones
109	"Phase and Frequency Converter Device" . . Patent #3,109,976, Nov. 5, 1963	G. Sichling
110	"High Frequency Power Supply". . . . . Patent #3,054,940, Sept. 18, 1962	K. M. Chirgwin etal
111	Static Power Converters, Performan. and Application	Robert Wells
112	Mercury-ARC Current Convertors, 2nd Ed., Ser Isaac Pitman & Sons, Ltd, London 1941	H. Rissik
113	SCR Manual, 3rd Edition. . . . . General Electric	
114	Silicon Controlled Rectifier Designers Handbook - 1st Edition . . . . . Westinghouse Corp., Semicond. Div.	
115	"Transistor Frequency Multiplier". . . . . Patent #3,030,566, Apr. 17, 1962	J. T. Collins
116	"Phase Regulated Inverters". . . . . Patent #3,050,674, Aug. 21, 1962	D. W. Moore
117	"Frequency Doubling Circuit" . . . . . Patent #3,044,004, July 10, 1962	J. P. Sicard
118	"Frequency Multiplying System" . . . . . Patent #3,048,765, Aug. 7, 1962	R. Weppler
119	"Frequency Multiplier" . . . . . Patent #3,025,448, March 13, 1962	R. B. Muchmore
120	"Multi-Stage Frequency Conversion Transmitter Adapted for Tuning Within an Extended Frequency Range". . . . . Patent #3,146,398, Aug. 25, 1964	M. Schnadelbach
121	"Frequency Control System" . . . . . Patent #3,036, 258, Jan. 2, 1959	K. R. Freidrich

Reference No.	Title	Author
122	"Frequency to Simulated Synchro Output Converter" . . . . . Patent #3,044,003, July 10, 1962	G. Stavis et al (Robert Grossman)
123	"Electric Power Translation System". . . . Patent #3,036,258, Jan. 2, 1959	K. R. Freidrich
124	"Electric Power Translation System". . . . Patent #3,026,467, March 20, 1962	D. K. Barnes
125	"Electric Power Translation System". . . . Patent #3,026,466, March 20, 1962	K. F. Freidrich
126	"Self-Balancing Power Supply System Having A Single Phase Output Energized by A Multiphase Source". . . . . Patent #3,040,231, June 19, 1962	P. P. Biringer
127	"Single Phase Power Supply System Having A Multiphase Source" . . . . . Patent #3,040,230, June 19, 1962	P. P. Biringer
128	"Crystal Frequency Stabilization". . . . . Patent #3,020,423, Feb. 6, 1962	E. A. Gerber
129	"Current Supply Apparatus" . . . . . Patent #3,041,523, June 26, 1962	R. E. Kuba
130	"Voltage Regulator Circuit Arrangement". . Patent #3,038,111, June 5, 1962	
131	"Frequency Transducer" . . . . . Patent #3,067,376, Dec. 4, 1962	V. B. Kwast
132	"Transistorized Power Supply". . . . . Patent #3,064,177, Nov. 13, 1955	A. Bender
133	"Inverter Having Amplitude Regulation" . . Patent #3,027,508, March 27, 1962	A. L. Johnson
134	"Voltage Regulated Power Supplies" . . . . Patent #3,046,466, July 24, 1962	P. C. Tyrrel etal (W.F. Wiley, Jr.)
135	"Synchronized Power System". . . . . Patent #3,056,077, Sept. 25, 1962	E. R. McCarter
136	"Frequency-Doubling Microwave Cavity". . . Patent #3,054,042, Sept. 11, 1962	N. Karayiansis etal (Clyde A. Morrison)

Reference No.	Title	Author
137	"Gyromagnetic Harmonic Generator". . . . . Patent #3,054,042, Sept. 11, 1962	M. T. Weiss
138	"Harmonic Generator" . . . . . Patent #3,060,365, Oct. 23, 1962	P. A. Crandell
139	"Serrodyne Frequency Shifters" . . . . . Patent #3,058,049, Oct. 9, 1962	F.J.O'Hara etal
140	"Polyphase Static Inverter". . . . . Patent #3,052,833, Sept. 4, 1962	J. E. Coolidge etal
141	"Solid State Power Inversion Techniques" . Semiconductor Products March 1960 and April 1960	Dr. D. A. Paynter B. D. Bedford J. D. Harnden,Jr.
142	"Handbook of Industrial Electronic Control Circuits" 1st Ed . . . . . McGraw-Hill Book Co., Inc., New York, 1956	John Markus Vin Zeluff
143	"Handbook of Electronic Control Circuits" 1st Ed. . . . . McGraw-Hill Book Co., Inc., New York 1959	John Markus
144	"Three-Phase Static Inverter". . . . . Patent #3,144,599, Aug. 11, 1964	C. B. Brahm
145	"The Widening World of the SCR". . . . . Electronics, Sept. 21, 1964	John C. Hey
146	"Choosing An AC Supply". . . . . Electro-Technology, Sept., 1964	Paul F. Swain
147	"Electronic and Radio Engineering, Fourth Ed. . . . . McGraw-Hill Book Co., New York, 1955, p.6	F. E. Terman
148	"Solid State Inverters Suppress Harmonics" Electronic Design, Sept. 28, 1964, p. 42	Bengt G. Olsson
149	"Controlled Frequency Power Supply System" Patent #3,148,323, Sept. 8, 1964	R. F. Blake etal Wm. J. Spaven
150	"System for Providing a Range of Determinate Frequencies from a Variable Speed Source". . . . . Patent #3,148,324, Sept. 8, 1964	L. R. Peaslee etal S. C. Caldwell

Reference No.	Title	Author
151	"Improvements Relating to the Conversion of Single Phase Alternating Electric Currents". . . . . Patent Specification (British) #518632, March 4, 1940	A. Stevens A.H.B. Walker
152	"An Improved DC to AC Inverter with Silicon Controlled Rectifiers" . . . . . Communications presented at Colloque International; Paris, France, Feb. 20-25, 1961	A. C. Stumpe
153	"Transistor Ring Counter". . . . . Patent #204081 (Australia); Nov. 14, 1956	E. R. Alschul
154	Steverbare Silizium-Gleichrichter und inre Anwendung.	R. Swoboda
155	"Tunnel-Diode Circuits Invert Direct to Alternating Current" . . . . . Electronics, Sept. 21, 1964	F. M. Carlson
156	"Static Frequency Converter" . . . . . Proceedings, 16th Annual Power Sources Conference, 21-23 May, 1963, pp 170-73	F. M. Carlson
157	"Activated Commutation for SCR Power Inverters" . . . . . Proceedings, 16th Annual Power Sources Conference, 22-24 May, 1962, pp. 150-54	G. P. Underbrink
158	"Static Inverters Using SCR with Pulse-width Control" . . . . . Ibid, pp. 154-56	F. Lawn
159	"Phase Control of Polyphase Static Inverters" . . . . . Ibid, pp. 156-59	B. Wilkinson
160	"Methods for Optimizing the Waveform of Stepped-Wave" . . . . . AIEE Conference Paper No. CP62-1147	P. D. Corey
161	"Analysis of a Three-Phase Inverter with Resistive Load" . . . . . AIEE Transactions - Vol 70, 1951, pp. 1055-1061	R. E. Turkington
162	"Parallel Inverter with Resistance Load" . Electrical Engineering, Nov. 1935, pp. 1227-1235	C. F. Wagner
163	"Parallel Inverter with Inductive Load". . Electrical Engineering, Sept. 1936, pp. 970-980	C. F. Wagner

Reference No.	Title	Author
164	"Design of an Electronic Frequency Changer" . . . . . AIEE Transactions - Vol. 63, 1944, pp. 1070-1078	C. H. Willis etal
165	"Fundamentals of Electronic Frequency Conversion". . . . . Power Plant Engineering, May 1946, pp. 58-65	M. M. Morack
166	"Design Techniques for Static Inverters" (Part 1) Electrical Manufacturing, Jan. 1960, pp. 79-87	A. A. Sorensen
167	"Design Techniques for Static Inverters" Electrical Manufacturing, Feb. 1960, pp. 84-94	A. A. Sorensen
168	"An Investigation of the Suppression of Commutation Oscillation in a Static Power Converter" . . . . . Direct Current, April 1962, pp. 98-103	R. Feinberg etal
169	"Filter Design for High Power Static Inverters" . . . . . Elteknik, 1964, pp. 121-124	Lennert Brandquist
170	"Design of DC-DC Converters for High Efficiency at Low Power" . . . . . Defense Documentation Center Bulletin AD443899	John A. Higgins
171	"Apparatus for Obtaining the Sum or Difference of the Frequencies of Two Alternating Signals" . . . . . Patent #3,151,915	T. D. Graybeal
172	"Frequency Converter". . . . . Patent #3,152,297	L. R. Peaslee
173	"Electric Apparatus for Controlling the Charging and Discharging of a Capacitor. . Patent #3,154,732	J. L. Jenson
174	"High Power Thyratron with a Low Value Resistor Bypass" . . . . . Patent #3,156,846	H. J. Wilms, Jr.
175	"Synchronous and Induction Motor Operation From a DC Source by Means of a Solid State Inverter Integral with the Motor". . Patent #3,156,858	
176	"Direct Current to Alternating Current". . Patent #3,156,877	S. L. Merkel

Reference No.	Title	Author
177	"Transistor Inverter Utilizing an Impedance Directly Connected Between Base and Collector to Prevent Saturation". . . . . Patent #3,157,795	A. I. Pressman
178	"Frequency Spectrum Generator Utilizing Diode and RC Combination to Effect Amplification and Harmonic Generation. . . Patent #3,158,752, Nov. 24, 1964	D. A. Strief
179	"Starter Protector for DC-AC Inverter" . . Patent #3,159,799, Dec. 1, 1964	K. W. Cooper, Jr.
180	"Converter with Series Load in Feedback" . Patent #3,159,800, Dec. 1, 1964	R. P. Massey
181	"Current Source Transducer High-Voltage Low-Current Power Supply System" . . . . . Patent #3,160,809, Dec. 8, 1964	G. F. Vanderschmidt
182	"Rectifier Circuit". . . . . Patent #3,160,806, Dec. 8, 1964	D. G. McDaniel
183	"Alternating Current Voltage Regulator". . Patent #3,160,808, Dec. 8, 1964	K. W. Kruse, Jr.
184	"Starting Circuit for Transistor Converter" Patent #3,160,829, Dec. 8, 1964	E. W. Mahland
185	"Inverter Starting Circuitry". . . . . Patent #3,160,830, Dec. 8, 1964	D. F. Murphy
186	Three Level Converter" . . . . . Patent #3,155,845, Nov. 3, 1964	A. J. Groudis
187	"Voltage Stabilizing Systems". . . . . Patent #3,155,894, Nov. 3, 1964	G. M. Bell
188	"Circuit for Protecting a Load Circuit From Initial Power Supply Voltage Transients". . . . . Patent #3,155,847, Nov. 3, 1964	T. M. Kirchmier
189	"Frequency Synthesis System for Multi-Frequency Transmitter-Receiver" . . . . . Patent #3,155,907, Nov. 3, 1964	A. H. Wulfsberg
190	"Pulse-Width Modulator". . . . . Patent #3,155,838, Nov. 3, 1964	C. B. Brahm
191	"Regulated Power Conversion System". . . . Patent #3,152,296	G. W. Mezaros

Reference No.	Title	Author
192	"An All Solid State Cycle Converter" . . .	G. J. Hoolboom
193	"The Frequency Converter Approach to A Variable Speed Constant Frequency System". . . . . AIEE Paper, 60-1076	L. R. Peaslee etal
194	"Precise Frequency Generation From an Unregulated Shaft" . . . . . AIEE Transactions, Applications and Industry, Vol. 79, pp. 442-451, Jan. 1961	K. M. Chirgwin L. J. Stratton J. R. Toll
195	"A Filter for Silicon-Controlled Rectifier Commutation and Harmonic Attenuation in High Power Inverters". . . . . Communications and Electronics May 1963, pp. 259-262	R. R. Ott
196	"Protection Circuit for Transistor Power Supply". . . . . Patent #3,161,834, Dec. 15, 1964	A. Noyes, Jr.
197	"Self-Oscillatory DC to AC Inverters with Magnetic Amplifier Controls" . . . . . Patent #3,161,837, Dec. 15, 1964	A. G. Lloyd
198	"Transistor Oscillator Inverter with Series Load in Feedback Circuit" . . . . . Patent #3,164,786, Jan. 5, 1965	D. G. Wilson
199	"Isolating and Frequency Multiplying Circuit Employing Varactor Diodes" . . . . . Patent #3,163,781, Dec. 29, 1964	J. M. Barringer
200	"Transistor Converter Circuit" . . . . . Patent #3,048,764, Aug. 7, 1962	J. E. Murphy
201	"Specifying the Best Transistor for Power Inverters" . . . . . Electronic Equipment Engineering, Oct. 1964, pp. 55-56	Robert Bolvin
202	"Sweep Test Picks Best Transistors to Bar Inductive Load Damage" . . . . . Electronic Design, Oct. 26, 1964	Jerry Miller
203	"Controlled Frequency Alternating Current System". . . . . Patent #3,170,107, Feb. 16, 1965	R. D. Jessee
204	"Voltage to Frequency Converter" . . . . . Patent #3,169,233, Feb. 9, 1965	S. A. Schwartz

Reference No.	Title	Author
205	"Frequency-Dividing Circuit" . . . . . Patent #3,170,069, Feb. 16, 1965	R. A. Kaenel
206	"Automatic Electric Power Regulator" . . . Patent #3,161,819, Dec. 15, 1964	A. R. Perrins
207	"Handbook of Noise Control". . . . . McGraw-Hill Book Co., Inc.	C.M. Harris, PhD
208	"Modulation Theory". . . . . D. Van Nostrand Co., Inc. 1953	H. S. Black
209	"Distortion in Pulse-Duration Modulation". Proceedings of the IRE, New York, Vol. 35, 1947, pp. 1230-1235	E. R. Kretzer
210	"New Results in the Calculation of Modulation Products" . . . . . The Bell System Technical Journal, New York, Vol. 12, April 1933, pp. 228-243	W. R. Bennett
211	"Parallel Inverter and Converter Operation and Improvements in Transformers . . . . . NASA Report - Westinghouse Electric Corp. Contract No. NAS 3-2792	NASA (G.W. Ernsberger) (H.R. Howell) (A.R. Baker)
212	"Optimization Study of High Power Static Inverters and Converters" . . . . . NASA Report - TRW Inc. Contract No. NAS 3-2785	NASA (R. G. Kline, etal)
213	"5KW Pulse Width Modulated Static Inverter NASA Report - TRW Inc. Contract No. NAS 3-6475	NASA (W.V. Peterson) (R.J. Resch)
214	"A Handbook on Electrical Filters" . . . . White Electromagnetics, Inc. 1963	White Electro-Magnetics, Inc.
215	"Pulse Width Modulated Inverters for AC Motor Drives" . . . . . IEEE International Convention Record, Part 8, IEEE International Convention, New York, N.Y., March 1966	B. Mokrytzki

APPENDIX B

PHASE-DEMODULATED HIGH FREQUENCY INVERTER DESIGNS

The following list of Phase-Demodulated High-Frequency Inverter designs is furnished to provide a reference as to what additional design work is and has been done in this area.

The basic design concept was proved out in a 200-VA, single-phase, variable-frequency inverter. This inverter operated like a low-frequency (DC to 400 Hz) amplifier in that the output reference voltage was taken from a function generator. The design did not include a feedback circuit so the output (voltage and frequency) was a direct function of the reference signal. This design was used to prove the basic Phase-Demodulated High-Frequency Inverter concept.

The second design is a three-phase, 3-KVA, 60-Hz inverter presently being evaluated by Varo and the U.S. Army Engineering Research and Development Laboratories under Contract DA-44-009-AMC-992(T). A photograph of this inverter is shown in Figure 70. The inverter input is 28 volts DC nominal. The output voltage is 115 volts rms line-to-neutral, three-phase, wye. The unit has an efficiency at 3 KW of 73 percent. The no-load to full-load regulation is 2 percent. The inverter was initially subject to noise pickup in the control stage which resulted in 10 percent output distortion at 60 Hz. A redesign has reduced this distortion to less than 4 percent. Additional redesigns are being considered to up the output power to 3750 VA and make the output frequency selectable between 50, 60, and 400 Hz.

The third inverter being developed under ERDL Contract No. DA-44-009-AMC-137 (T) is a 4-KVA Thermionic Silent Running Power Supply. The input power is 4 volts DC derived from a thermionic fuel cell. The output is to be two high-frequency squarewaves phase shifted 90 degrees capable of being phase-demodulated to produce a 115-volt, 50, 60, or 400-Hz output. This is a feasibility study to determine if a 2400-Hz Phase-Demodulator Power Stage can be constructed to operate off of the 4 volt thermionic fuel cell.

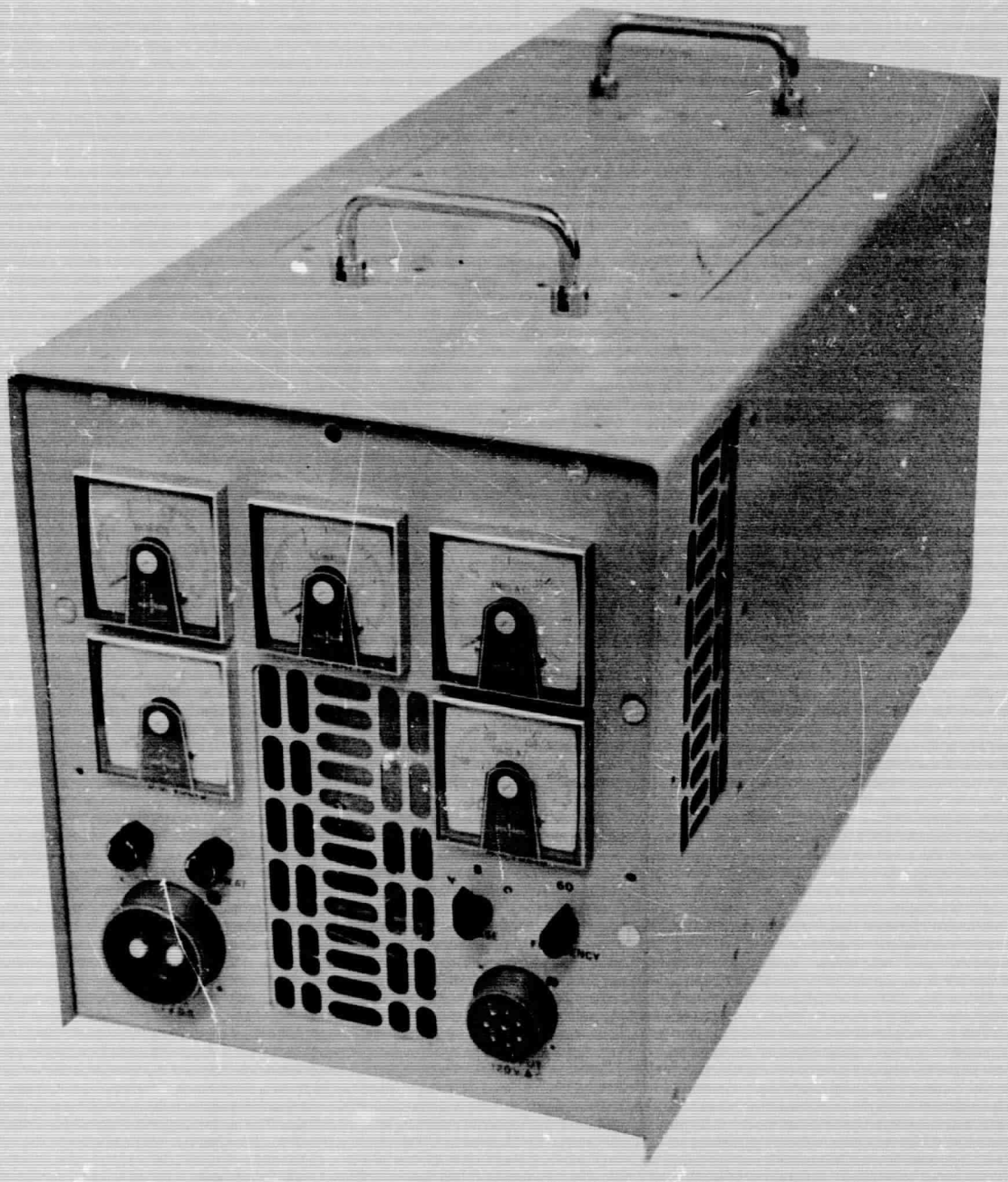


Figure 70. Three-Phase, 3-KVA, 60-Hz Inverter.

The fourth design, Model 4367, is a 250-VA, single - phase multiple-frequency inverter. The output of this inverter can be selected to provide 28 volts DC, 125 watts, or 115 volts AC at 50, 60, or 400 Hz. The output voltage regulation of this unit is ± 2 percent. The frequency regulation is ± 0.25 percent. The weight of this inverter is 12 pounds. A picture of this inverter is provided in Figure 71.

This inverter as well as the other inverters already described has provided extensive information for this design. A few of the various output waveshapes from the inverter are illustrated in Figures 72 through 82.

Figures 72 and 79 show the output voltage of this inverter at an output frequency of 400 Hz. Figure 74 illustrates the unfiltered waveform out of the demodulator at an output frequency of 400 Hz. It is very interesting to note how closely this corresponds with the calculated or constructed waveform of Figure 15p.

Figure 75 illustrates the output voltage and output current at 400 Hz. Figure 76 shows the output current at a different power level.

Figure 77 through 79 show the input voltage being modulated and the effects of this modulation on the output. These different figures are for different modulation rates, 1 Hz to 10 Hz. The low frequency was used since this is where this type problem shows up the most. The 250-VA inverter does not have an input filter, only 750 μfd of capacitance on the input of the unit. It is also noted that the output variation or modulation peak to peak is about the same or slightly less than the input modulation. The amount of output modulation is a function of the regulation of the unit. If this unit had a better regulation loop or required better regulation, then the output modulation would decrease as a function of the improvement in regulation.

Figure 83 illustrates the circuit used to modulate the input line. Inspection of this circuit shows that the source impedance is fairly high during modulation due to the modulator. The high-frequency noise on the input line is noise generated by the inverter and reflected to the source. Use of an input filter as illustrated in the proposed design reduces this noise to the required level.

Figure 80 illustrates the affect of a step load (0-150 VA) on the inverter when the input is being modulated at a 5-Hz rate. The only change is a drop in output voltage at the point of the application of the load. It is felt that the high input impedance affected the output regulations somewhat. The effect of the same load is illustrated in Figure 81 at a slower sweep rate and without the input modulator in the circuit. The point of load application is hard to locate on the trace since it only appears as a bump in part of a quarter of a cycle. The picture illustrated has two traces as the first sweep did not catch the load change.

Figure 82 illustrates the starting ability of the 250-VA inverter. The sweep illustrated shows the inverter starting a 1/4-inch (Ramp) Black and Decker Drill.

Figures 72 through 76 illustrate the 250-VA, 400-Hz operation while Figures 77 through 82 illustrate its operation at 60 Hz. Additional tests and data have been taken from this design as well as the other designs and applied to this program. Any additional design data generated will be used in the prototype design of Phase II.

Figure 71. 250-VA, Single-Phase Multiple-Frequency Inverter.

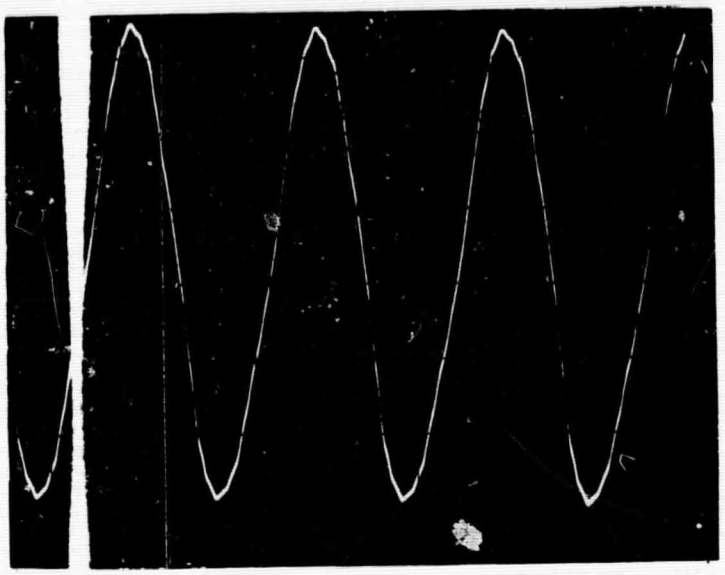


FIGURE 72
OUTPUT VOLTAGE

115 VOLTS RMS
50 VOLTS/CM
1.0 M SEC/CM
NO LOAD

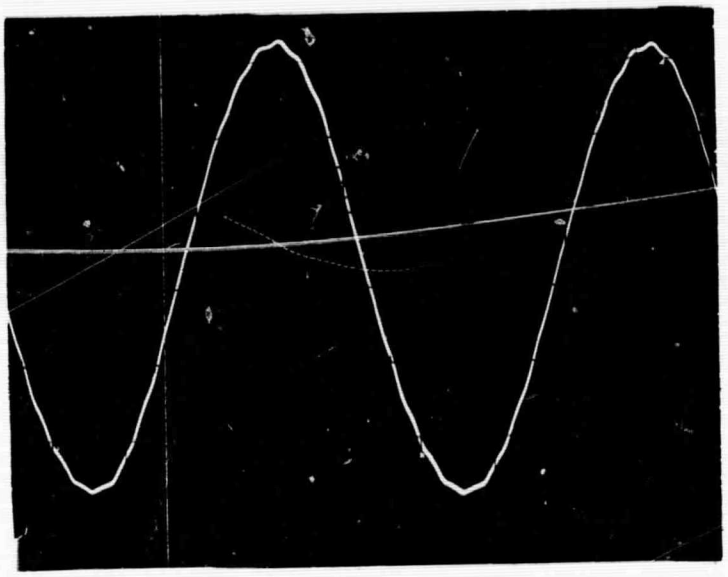


FIGURE 73
OUTPUT VOLTAGE

115 VOLTS RMS
50 VOLTS/CM
0.5 M SEC/CM
NO LOAD

FIGURE 74
UNFILTERED DEMODULATED VOLTAGE

200 VOLTS/CM
0.5 M SEC/CM

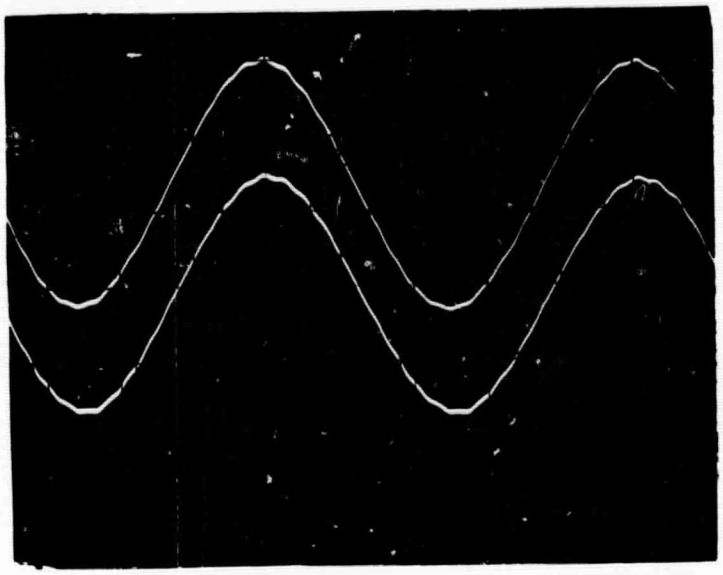


FIGURE 75

TOP: OUTPUT VOLTAGE
115 VOLTS RMS
100 VOLTS/CM
0.5 M SEC/CM

BOTTOM: OUTPUT CURRENT
1.1 AMPERE RMS
1.0 AMPERE/CM
0.5 M SEC/CM

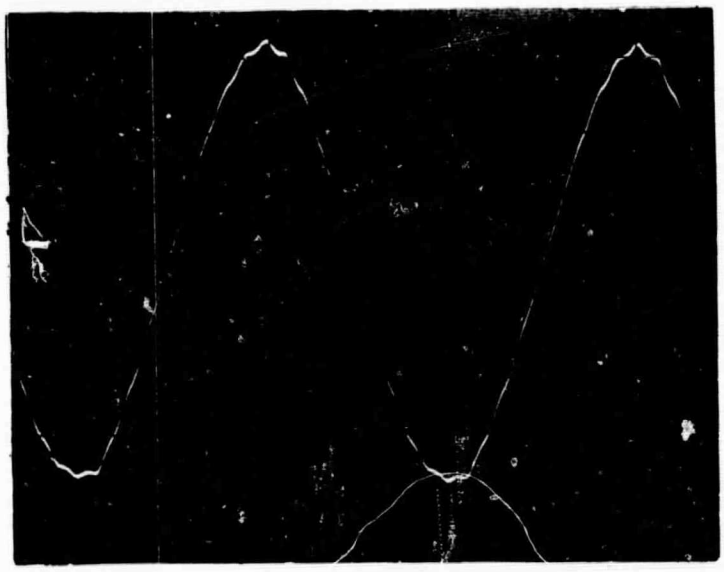


FIGURE 76

OUTPUT CURRENT
2.0 AMPERES RMS
1.0 AMPERE/CM
0.5 M SEC/CM

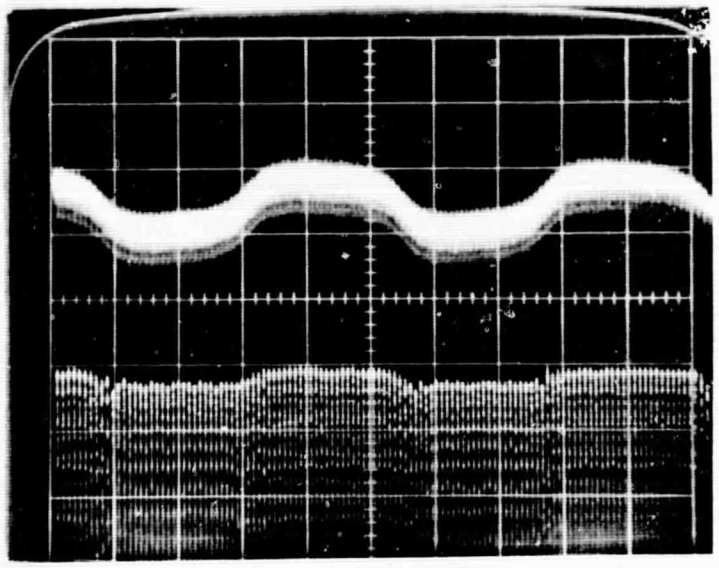


FIGURE 77

UPPER TRACE:

INPUT MODULATED D.C. VOLTAGE

MODULATING FREQ -1Hz

SCALE -5 V/cm

LOWER TRACE:

OUTPUT A.C. VOLTAGE
SCALE -10 V/cm

SWEEP:

200 M sec/cm

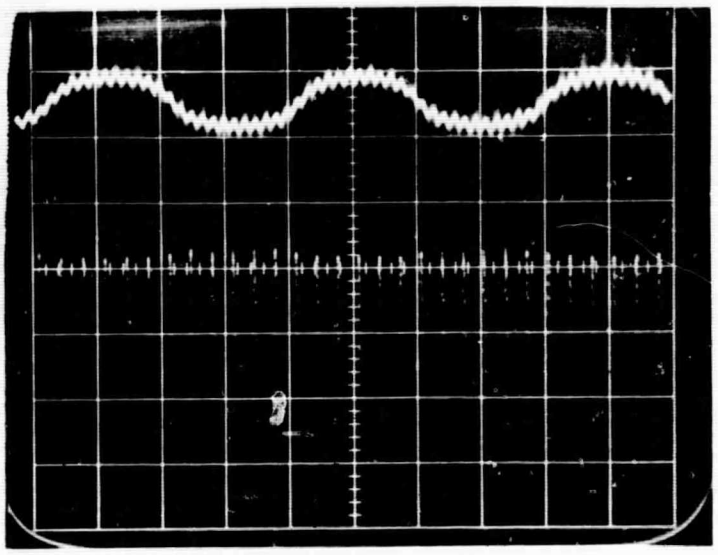


FIGURE 78

UPPER TRACE:

INPUT MODULATED D.C. VOLTAGE

MODULATING FREQ -5Hz

SCALE -5 V/cm

LOWER TRACE:

OUTPUT A.C. VOLTAGE
SCALE -10 V/cm

SWEEP:

50 M sec/cm

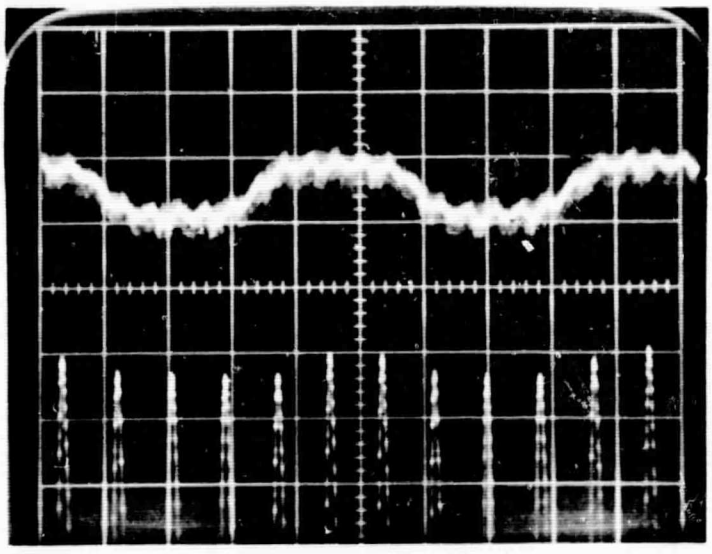


FIGURE 79

UPPER TRACE:

INPUT MODULATED D.C. VOLTAGE

MODULATING FREQ -10Hz

LOWER TRACE:

OUTPUT A.C. VOLTAGE

SWEEP:

20 M sec/cm

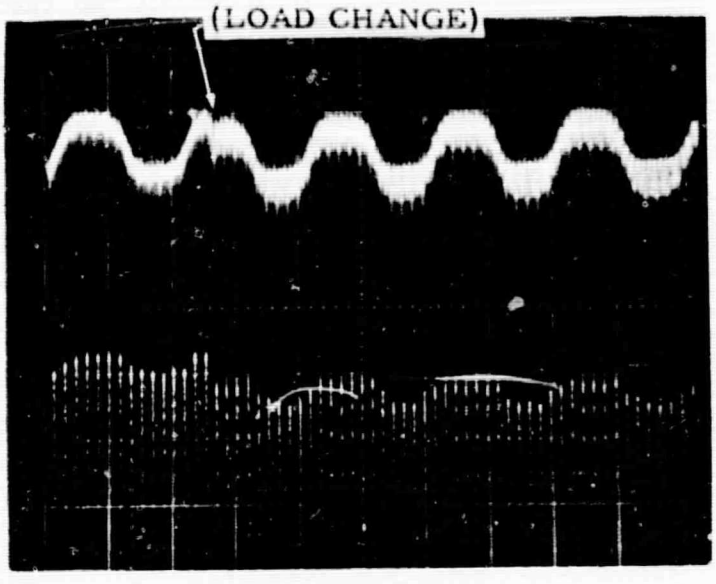


FIGURE 80

NO LOAD TO 150 VA LOAD

UPPER TRACE:

INPUT MODULATED D.C. VOLTAGE

MODULATING FREQ -5Hz

SCALE _5 V/cm

LOWER TRACE:

OUTPUT A.C. VOLTAGE

SCALE -10 V/cm

SWEEP:

100 M sec/cm

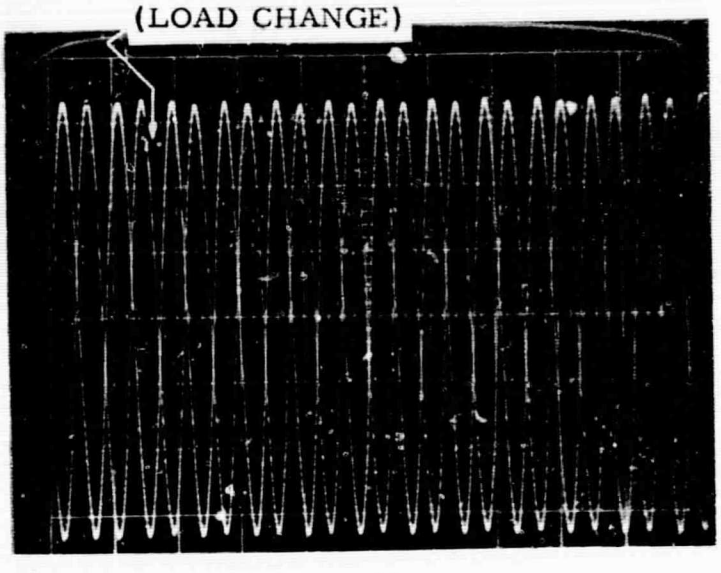


FIGURE 81

115 VOLTS RMS

0-150 VA LOAD CHANGE

VERTICAL SCALE: 50 V/cm

SWEEP: 20 M sec/cm

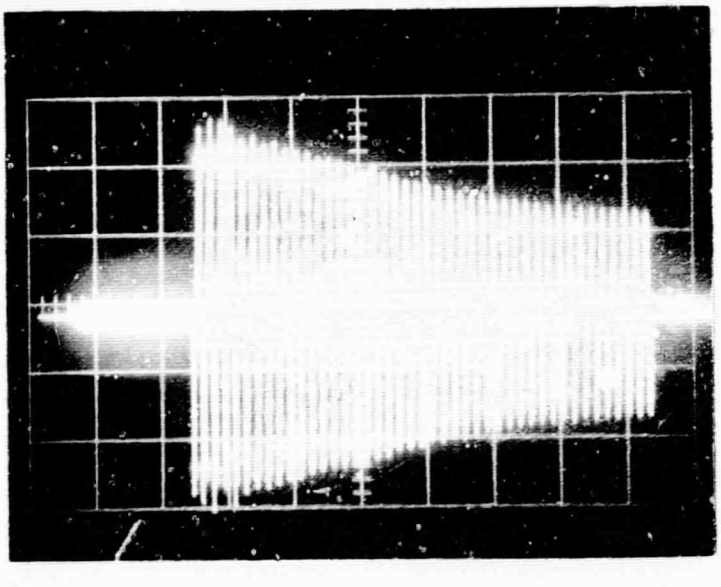


FIGURE 82

OUTPUT: STARTING CURRENT

LOAD: BLACK & DECKER 1/4 (2 AMP) DRILL

VERTICAL: 2 AMP/cm

SWEEP: .2 sec/cm

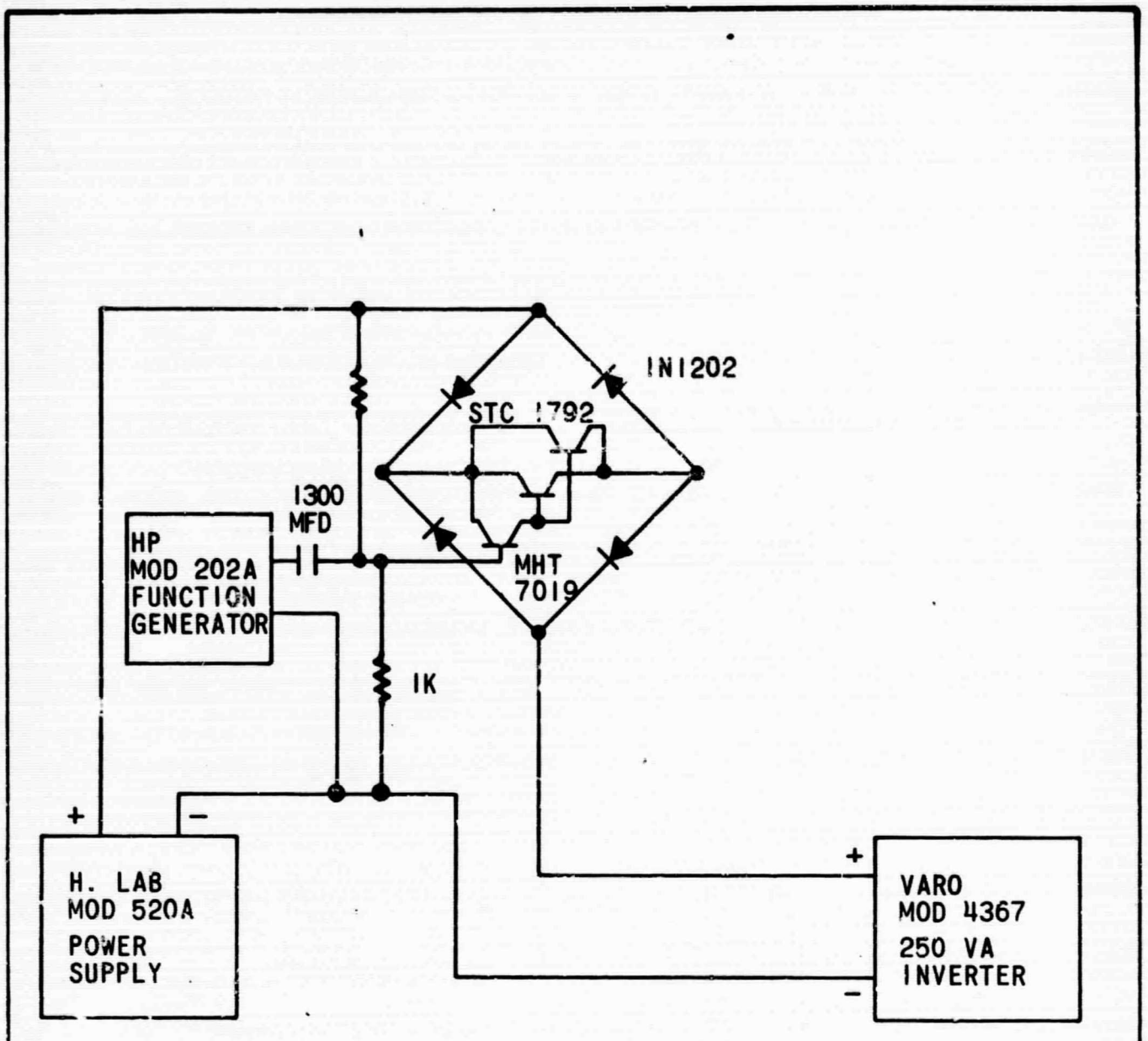


FIGURE 83
MODULATION CIRCUIT

APPENDIX C

DETAILED PARTS LIST

SECTION A1

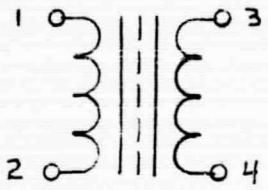
PART	VALUE	TOLERANCE
R1	3.9K ½ W	± 5%
R2	100 ½ W	± 5%
R3	6.2K ½ W	± 5%
R4	100 ½ W	± 5%
R5	500 ½ W Potentiometer	±10%
R6	1.62K ½ W	± 1%
R7	620 ½ W	± 5%
C1	47 ufd 50 WVDC	±10%
C3	60 ufd 35 WVDC	±10%
C4	22 ufd 35 WVDC	±10%
C5	22 ufd 20 WVDC	±10%
L1	4 mhy	± 1%
CR1	UTR11	
CR2	CL1302	
CR3	1N968	
CR4	1N2929	
CR5	1N754A	
CR6	1N758	
CR7	1N750A	
Q1,Q5	S2N930	
Q2	2N696	
Q3	2N3879	
Q4	S2N2034A	

SECTION A2

PART	VALUE	TOLERANCE
R1	52K ½ W Potentiometer	±10%
R2	68.8K ½ W	± 1%
R3,R20	2.7K ½ W	± 5%
R4,R25	2.2K ½ W	± 5%
R5,R16	390 ½ W	± 5%
R6,R17	100 ½ W	± 5%
R7, R13	10K ½ W Potentiometer	±10%
R8	68K, ½ W	± 5%
R9,R10	51 ohm ½ W	± 5%
R11	620 ohm ½ W	± 5%
R12	47K ½ W	± 5%
R14	33K ½ W	± 5%
R15	10K 1 W Potentiometer	±10%
R18,R21	7.96K ½ W	± 1%
R19	39K ½ W	± 1%
R22	1K ½ W	± 5%
R23	33K ½ W	± 5%
R24	15K ½ W	± 5%
C1	47 ufd 20 WVDC	± 1%
C2	.01 ufd 20 WVDC	± 1%
C3	.33 ufd 35 WVDC	±10%
C4	10 ufd 20 WVDC	± 1%
C5	390 uufd 35 WVDC	±10%
C6	5000 uufd 35 WVDC	± 1%
C7	.005 ufd 35 WVDC	± 1%
C8	.1 ufd 35 WVDC	±10%
C9,C10	.01 ufd 35 WVDC	± 1%
C11	.005 ufd 35 WVDC	± 1%
C12	39 ufd 10 WVDC	±10%
CR1	1N914	
CR2	1N746	
CR3,CR4	1N4001	
Q1,Q2,Q3	S2N697	
Q4	S2N2412	
Q5,Q7,Q8	S2N930	
Q6	S2N491	
Z1,Z2,Z3,Z5	CD2203	
Z4	NA702	

CURRENT SENSING TRANSFORMER

A2 - T1



CORE	-	6T-5340-D1
TURNS	-	N_{1-2} 30T #35 H.F.
		N_{3-4} 32T #35 H.F.
SIZE	-	3/4" X 3/4" X 1/2"
WEIGHT	-	.1 lbs.

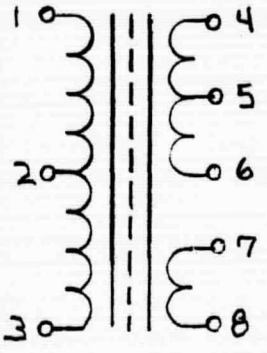
SECTION A3

PART	VALUE	TOLERANCE
R1	5.6K ½ W	± 5%
R2	2.2K ½ W	± 5%
R3	3.9K ½ W	± 5%
R4	5K ½ W Potentiometer	±10%
R5	2K ½ W	± 5%
R6	470 ½ W	± 5%
R7,R15,R16,R17,R18	10K ½ W Potentiometer	±10%
R8	10K ½ W	± 5%
R9	330 ½ W	± 5%
R10	2.7K ½ W	± 5%
R11	220 ½ W	± 5%
R12	5.6K ½ W	± 5%
R13	3.3K ½ W	± 5%
R14	16K ½ W	± 5%
R19	6.2K ½ W	± 5%
R20	5.6K ½ W	± 5%
R21,R33	2.2K ½ W	± 5%
R22,R30	5.6K ½ W	± 5%
R23	820 ½ W	± 5%
R24,R28	10K ½ W	± 5%
R25,R29	91 ½ W	± 5%
R26	820 ½ W	± 5%
R27	4.7K ½ W	± 5%
R31,R34	270 ½ W	± 5%
R32	4.7K ½ W	± 5%
C1	4 0 uufd 20 WVDC	±10%
C2,C3	120 uufd 50 WVDC	±10%
C4	10 ufd 15 WVDC	±10%
C5	.0068 uf 20 WVDC	±10%
C6	5 ufd 20 WVDC	±10%
C7	35 ufd 20 WVDC	±10%
C8	.015 ufd 50 WVDC	± 1%
C9, C10	10 ufd 15 WVDC	±10%
CR1,CR3,CR5,CR6,CR7	S1N916B	
CR2,CR4	1N2929	
Z1	CA3000	
Z2,Z3	CD2203	
Q1,Q3,Q9,Q10	S2N697	
Q2	S2N1132	
Q4	2N3250	
Q5,Q6,Q7,Q8	S2N930	

SECTION A4

PART	VALUE	TOLERANCE
R1,R3,R5 R2,R4,R6 R7,R9	7.5K ½ W	± 5%
R10,R12	2.7K ½ W	± 5%
R13,R15,R17 R14,R16,R18	1.8K ½ W	± 5%
R19,R21,R20	100 1 W	± 5%
R22,R24,R26 R23,R25,R27	27 2 W	± 5%
C1,C2,C3	10 uf, 20 WVDC	±10%
CR2, CR3	1N4001	
CR1	1N821	
Q1,Q2,Q3 Q4,Q5,Q6	S2N930	
Q7,Q8,Q9 Q10,Q11,Q12	S2N697	
Q13,Q14,Q15 Q16,Q17,Q18	2N3897	

SUB DRIVE TRANSFORMER



A4 - T1

Core - 6T-5958-D2

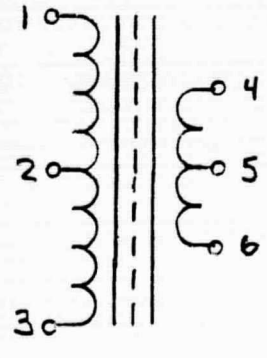
Turns - N_{1-2} - 195T #30 H.F. } Bifilar
N_{2-3} - 195T #30 H.F. }

N_{4-5} - 31T #21 H.F. } Bifilar
N_{5-6} - 31T #21 H.F. }

N_{7-8}

Weight - 0.25 lbs.

Size - 1-1/2 X 1-1/2 X 3/4



A4 - T2, A4 - T3

Core - 6T-5958-D2

Turns - N_{1-2} - 195T #30 H.F. } Bifilar
N_{2-3} - 195T #30 H.F. }

N_{4-5} - 31T #21 H.F. } Bifilar
N_{5-6} - 31T #21 H.F. }

Weight - .25 lbs.

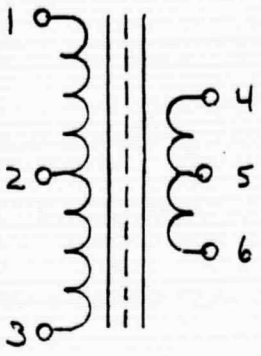
Size - 1-1/2 X 1-1/2 X 3/4

SECTION A5

PART	VALUE		TOLERANCE
R1,R2,R3			
R4,R5,R6	.75 5 W		1%
R7,R8,R9,R10	330 $\frac{1}{2}$ W		5%
R11,R12,R13,R14	100 $\frac{1}{2}$ W		5%
R15,R16,R17,R18			
R19,R20,R21,R22	1 5 W		1%
R23,R24,R25			
R26,R27,R28	.025 ohm 10 W		1%
C9	100 ufd 100 V		10%
C1,C2,C12,C15	.005 ufd 3 KV	disc. ceramic	10%
C3,C4,C5,C6	1000 uufd	feedthrough	1.5% Erie 2499-003
C7,C8,C10,C11			
C13,C14	5000 uufd	feedthrough	1.5% Erie 2499-003

POWER STAGE DRIVE TRANSFORMER

A5 - T1



Core - 6T-5504-D2 Toroid

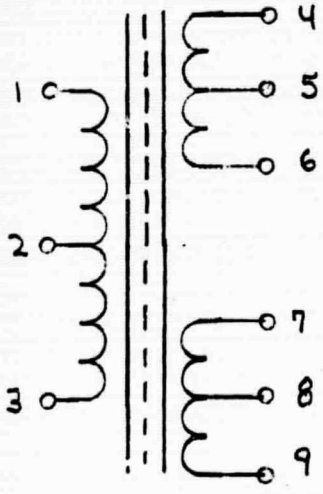
Turns - N_{1-2} - 159T #22 H.F. } Bifilar
N_{2-3} - 159T #22 H.F. }

N_{4-5} - 18T #17 H.F. } Bifilar
N_{5-6} - 18T #17 H.F. }

Weight - .35 lbs.

Size - 1-1/2 X 1-1/2 X 3/4

A5 - T2, A5 - T3



Core - 6T-5958-D2

Turns - N_{1-2} - 195T #31 } Bifilar
N_{2-3} - 195T #31 }

N_{4-5} - 317T #25 H.F. } Bifilar
N_{7-8} - 317T #25 H.F. }

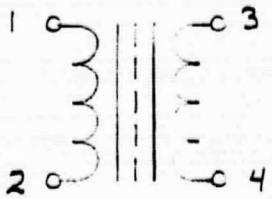
N_{5-6} - 317T #40 H.F. } Bifilar
N_{8-9} - 317T #40 H.F. }

Weight - .25 lbs.

Size - 1-1/2 X 1-1/2 X 3/4

CURRENT TRANSFORMER

A5 - T4,T5,T6,T7



Core - A206068-2 (Arnold) Toroid

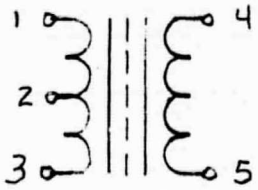
Turns - N_{1-2} 100 #22 H.F.

N_{3-4} 5 #20 H.F.

Weight - 1 oz.

Size - 1.00" X .450"

A5 - T8



Core - 2 ea. 50001-2A Toroid

Turns - N_{1-2} - 9T #12 } Bifilar

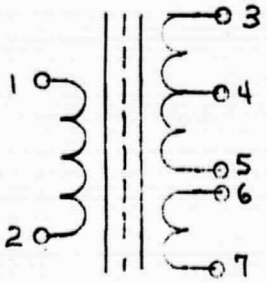
N_{2-3} - 9T #12 }

N_{4-5} - 70T #13 Single

Weight - 2-1/4 lbs.

Size - 2-1/2 X 3-1/2 X 3-1/2

ISOLATION TRANSFORMER



A5 - T9

CORE - EE-24-25

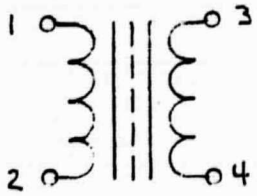
TURNS - N_{1-2}- 2 turns #16 H.F.

N_{3-4}- 50 turns #35 H.F. } Bifilar

N_{4-5}- 50 turns #35 H.F. }

N_{6-7}- 30 turns #35 H.F.

SIZE - 1"" X 1" X 1"



A5 - T10

CORE - E1-375 - Silicon

TURNS - N_{1-2} - 900T #40 H.F.

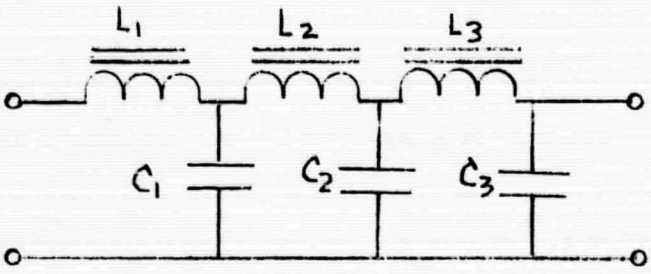
N_{3-4} - 50T #35 H.F.

WEIGHT - .25 lbs.

SIZE - 1-1/2 X 1-1/2 X 1-1/2

INPUT FILTER

A5 - FL1



L1

Core - 55252-A2

Turns - 10T #10

Weight - .5 lbs.

Size - 1-3/4 X 1-3/4 X 3/4

L2

Core - 55583-A2

Turns - 5T #10

Weight - .25 lbs.

Size - 1-1/2 X 1-1/2 X 3/4

L3

Core - 55583-A2

Turns - 4T #10

Weight - .25 lbs.

Size - 1-1/2 X 1-1/2 X 3/4

C_1

2350 mfd. Tantalum wet slug
Similar to GE CL55CN441MP3
Special package to achieve weight reduction

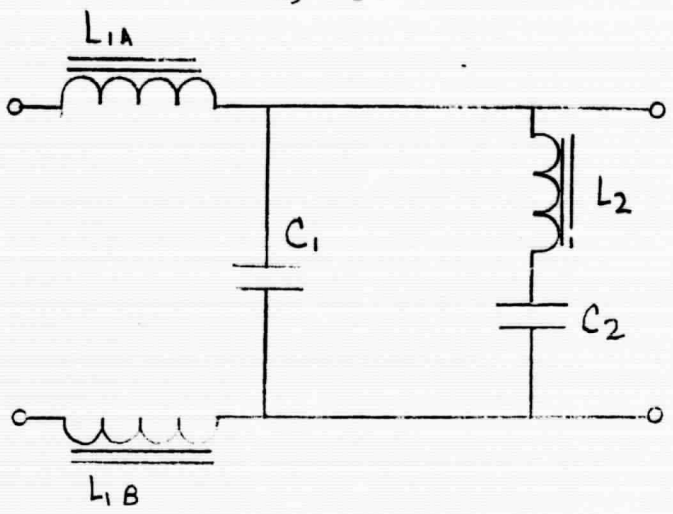
C_2

1775 mfd. (Packaged with C_1)

C_3 1420 mfd. (Packaged with C_1)

OUTPUT FILTER

A5 - F[illegible]



L_{1A}, L_{1B}

Core - 55928-A2 - Toroid

Turns - 61T #16 H.F.

Weight - .3 lbs.

Size - 1.5 X 1.5 X 1

L_2

Core - 55908-A2 - Toroid

Turns - 59T #18 H.F.

Weight - .25 lbs.

Size - 1.5 X 1.5 X .75

C_1

1.5 mfd. Dg-155

Metallized Mylar

Size: 1.68" X .73" X .92"

C_2

2 mfd. Dg-205

Metallized Mylar

Size: 1.68" X .84" X 1.06"