RELIABILITY IN DIGITAL SYSTEMS WITH ASYMMETRICAL FAILURE MODES *

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ABSTRACT

Most present day reliability schemes using redundancy to mask the failure of individual logic modules employ majority voting with the assumption that the replicated modules have symmetrical failure characteristics. This paper presents an analysis of such schemes when the modules exhibit asymmetrical failure modes; that is, the probability that a module fails with a 0 output is not equal to the probability that it fails with a 1 output. Fail-safe logic systems (discussed by other authors) fall in this category. A general expression is presented which gives the reliability of a network consisting of n identical modules feeding a k-out-of-n voter. It is shown that a simple majority element does not always represent the optimal choice. Plots for selecting the optimal k for n = 3, 4, 5 when the individual module reliability parameters are known are presented. Also included are graphs of network reliability in terms of individual module reliability and the degree of asymmetry.

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INTRODUCTION

Most reliability schemes for digital systems assume that a given module (gate, flip-flop, sub-system) has an equal probability of failing with output 0 as with output 1. In particular, some majority voting schemes (deriving from Von Neumann [3]) make such an assumption. The assumption is not always valid; Mann has discussed this point [1].

Further, one may intentionally design circuits to fail almost certainly in either the 0 or 1 state. These have been termed "fail-safe" logical systems [2].

This paper considers systems such as that illustrated in figure 1 where the modules are identical. If there are no failures, the logic is such that

$$f_1 = f_2 = \cdots = f_n = f ,$$

and is so chosen that at least one module failure may be tolerated. With symmetrical module failures, the best choice is a majority element, a logic element whose output is equal to the majority of its inputs. Assuming the majority element and modules have sufficiently high reliability, the composite system will be more reliable than a single module.

If the modules have asymmetrical probabilities of failure, it is not obvious what logic element is best. For example, in the extreme case that the modules always fail with zero outputs, an OR gate is a better choice for the logic element than a majority gate. The present paper is concerned with the problems of choosing the optimal logic element given the failure probabilities of the modules and of deriving the system reliability.

ANALYSIS

We assume that a module will fail stuck at 0 or 1 and that the following module parameters are available:

p_0 = the probability that the module will fail and fail at 0,

p_1 = the probability that the module will fail and fail at 1.

If a given collection of modules are tested for a given period of time, some will fail at 1, some will fail at 0, and some will not fail at all. In these terms,

$$p_0 = \frac{\text{number of modules failed as 0}}{\text{number tested}}$$

$$p_1 = \frac{\text{number modules failed as 1}}{\text{number tested}}$$

Not all logical functions need be considered. Since the modules are identical, only symmetric functions need be considered. Since the system output is to be identical with the module outputs, only positive functions need be considered. Further, out of the class of positive symmetric functions, only those of the following type will be considered:

(1) $$S_{k/n} = \begin{cases} 1 \text{ if k or more of the n inputs are 1} \\ 0 \text{ if not} \end{cases}$$

The function $S_{k/n}$ can be realized by a single threshold element with unity weights and a threshold k. $S_{1/n}$ is an n-input OR gate, and $S_{n/n}$ is an n-input AND gate.

The reliability of the output gate will be considered unity for the sake of the computations which follow. This is a matter of convenience since the reliability of this gate enters as a multiplicative factor and may be taken into account at a later point.

The system will be considered to have failed when it no longer follows the behavior of the working modules. Then the system will fail when k or more modules fail as a 1 or n-k+1 or more modules fail as a 0. Since these two events are disjoint, we have for a logic element realizing $S_{k/n}$

$$P_{k/n} = \text{probability of system failure}$$

(2) $$= \sum_{i=k}^{n} \binom{n}{i} p_1^i \left(1 - p_1\right)^{n-i} + \sum_{i=n-k+1}^{n} \binom{n}{i} p_0^i \left(1 - p_0\right)^{n-i}$$

where

$$\binom{n}{i} = \frac{n!}{(n-i)!\,i!} .$$

The reliability of the system is $V_{k/n} = 1 - P_{k/n}$.

Note that

$$(3) \qquad V_{k/n}(p_0, p_1) = V_{(n-k+1)/n}(p_1, p_0) \ .$$

Figures 2-8 are plots of $V_{k/n}$ through $n = 5$ in terms of the parameters

P = reliability of each module

$= 1 - p_0 - p_1$

α = probability of failing as a zero given a failure has occurred

$$= \frac{p_0}{p_1 + p_0} \ .$$

By applying equation (3), the missing plots may be read off the existing plots; for example, $V_{3/3}$ may be read from the plot for $V_{1/3}$ by interpreting the horizontal axis as

$$\alpha' = \frac{p_1}{p_1 + p_0} \ .$$

These curves allow rapid estimation of the system reliability.

The curves of figures 2-8 may be used to determine when the system becomes less reliable than a single module. Since P represents the module reliability, the intercept of the curve for $P = x$ with the horizontal line $V_{k/n} = x$ yields the value of α for which the system breaks down. If the reliability of the logic element $S_{k/n}$ is not assumed unity but takes some value β, the curves of figures 2-8 are correct if the values on the vertical scale are multiplied by β.

Given n modules and the associated p_0 and p_1, which function $S_{k/n}$

is optimal? Figures 9-11 answer this question for n = 3, 4, 5. These curves were obtained by numerical solution (on a general-purpose digital computer) of the equations in two unknowns

$$V_{k/n} = V_{(k+1)/n} .$$

If the number of modules is not determined otherwise, one is free to choose both k and n. The choices which maximize $V_{k/n}$ through n = 5 are indicated in figures 12, 13, and 14 with increasing detail. The boundaries between regions are approximated by staircase functions.

REFERENCES

[1] Mann, W. C., "Restorative Processes for Redundant Computing Systems," In Redundancy Techniques for Computing Systems, Wilcox and Mann (eds.), Spartan Books, 1962.

[2] Mine, H., and Y. Koga, "Basic Properties and a Construction Method for a Fail-Safe Logical System," IEEE Trans. on Electronic Computers, Volume EC-16, No. 3 (June 1967).

[3] Von Neumann, "Probablistic Logics and the Synthesis of Reliable Organisms from Unreliable Components," Automata Studies (edited by C. E. Shannon and J. McCarthy), Princeton University Press, 1956.

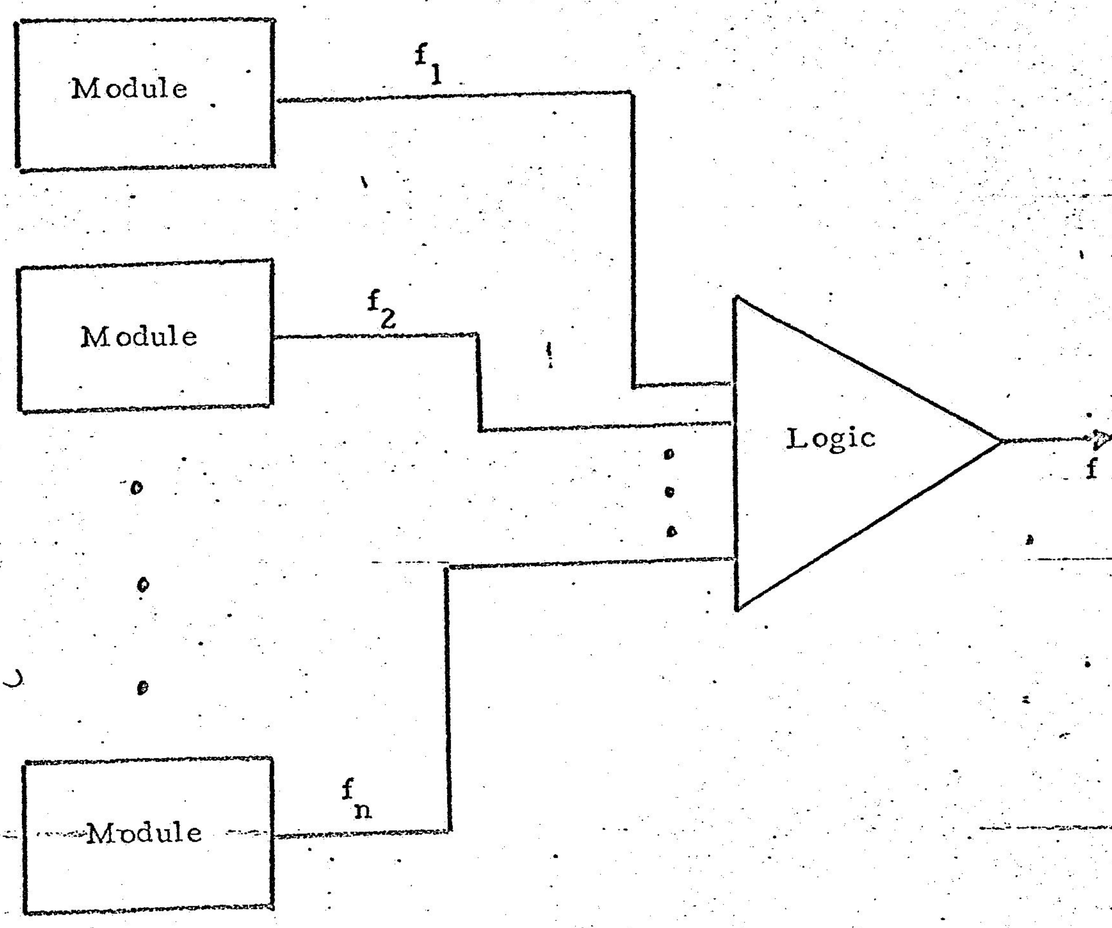
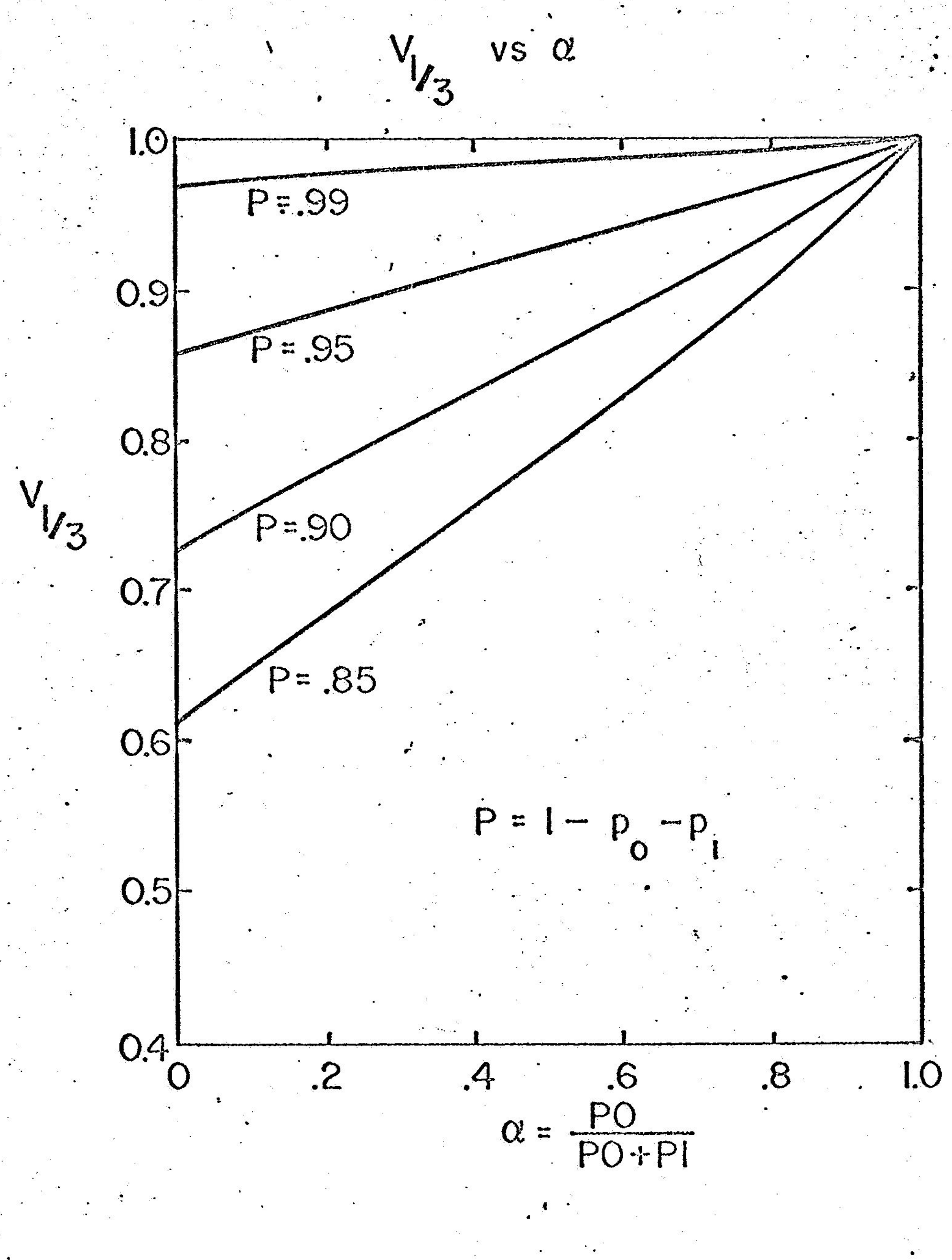
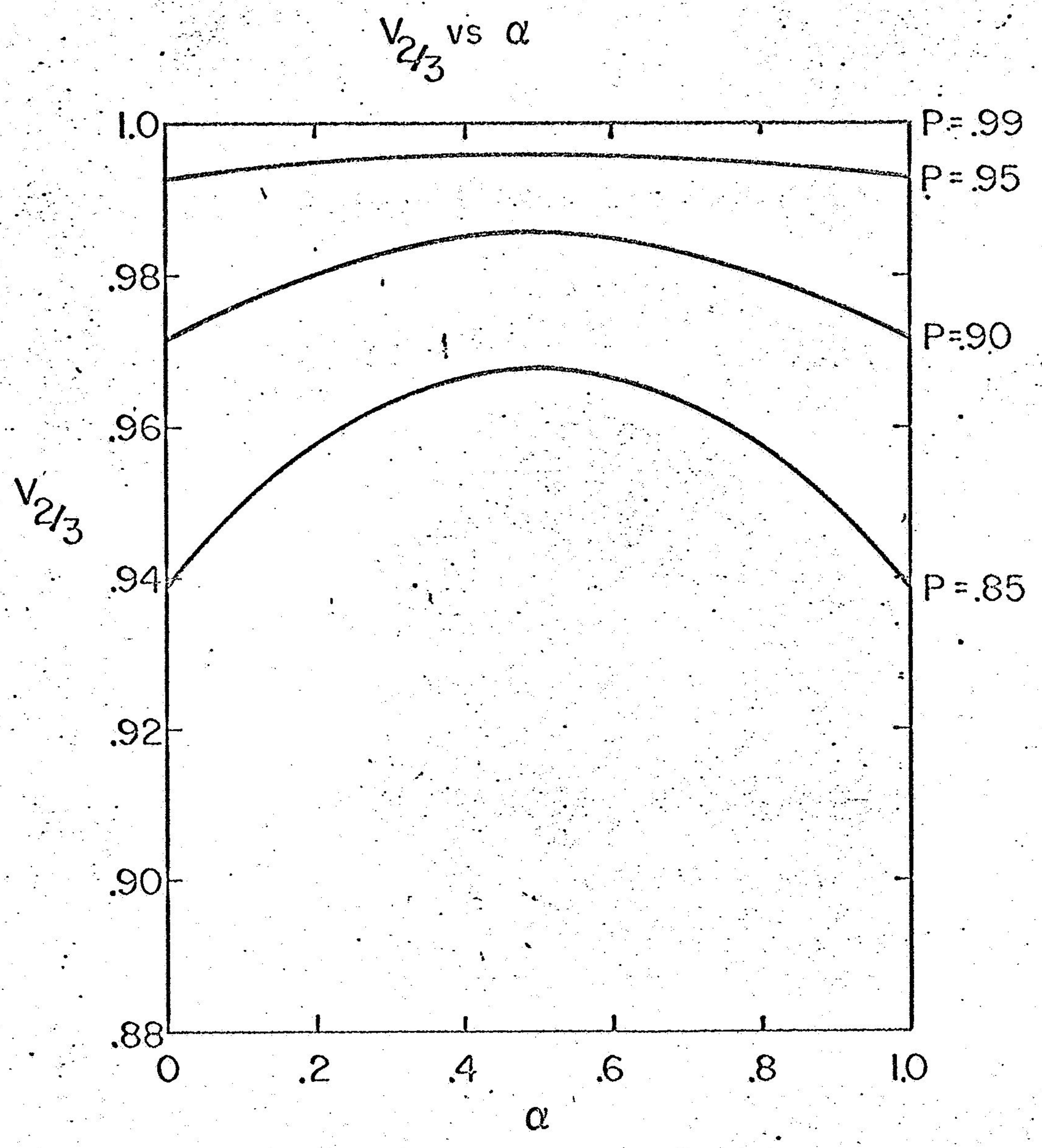


Figure 1

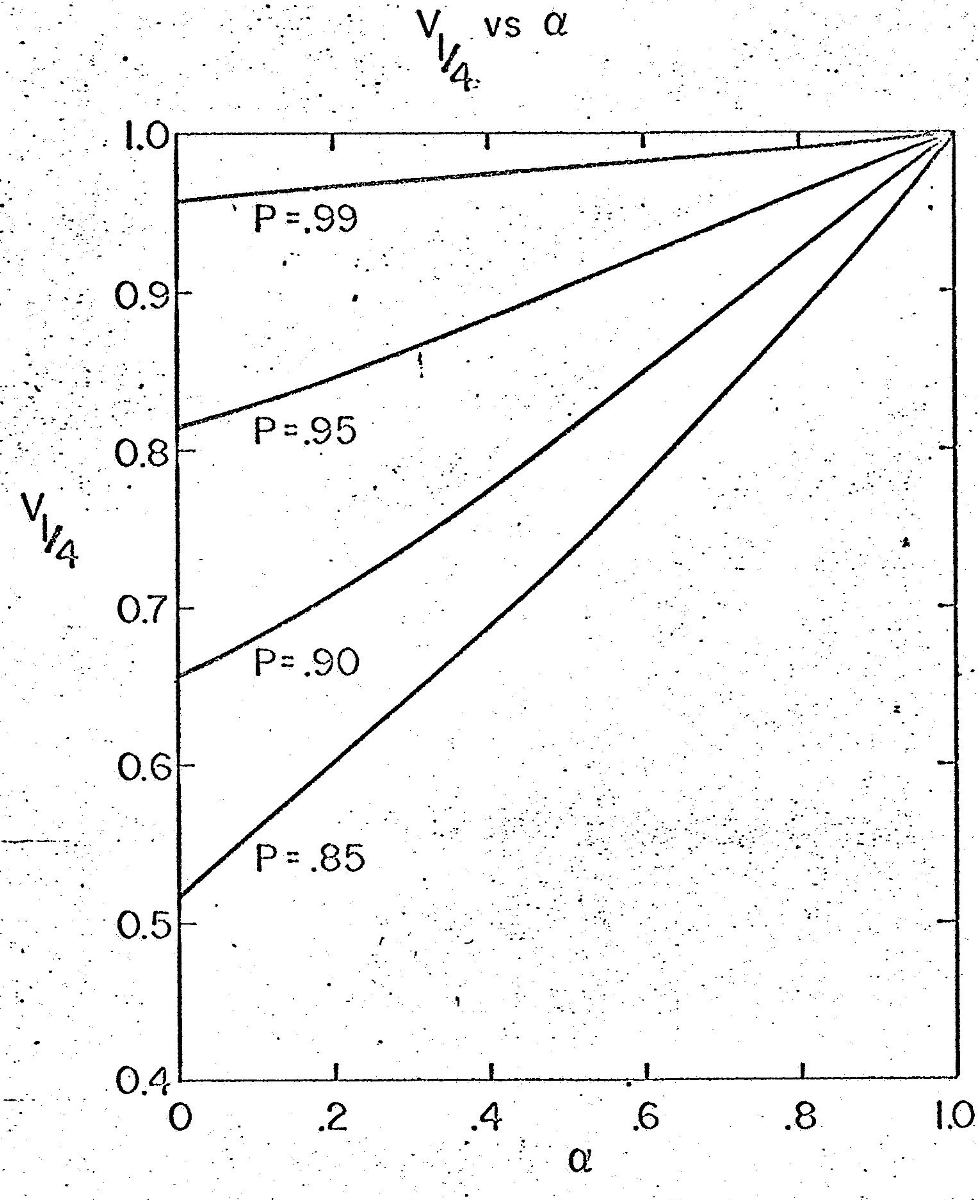


V1/3 vs α
1.0
0.9
0.8
0.7
0.6
0.5
0.4
V1/3
P = .99
P = .95
P = .90
P = .85
P = 1 − p0 − p1
0
.2
.4
.6
.8
1.0
α = PO / (PO + PI)

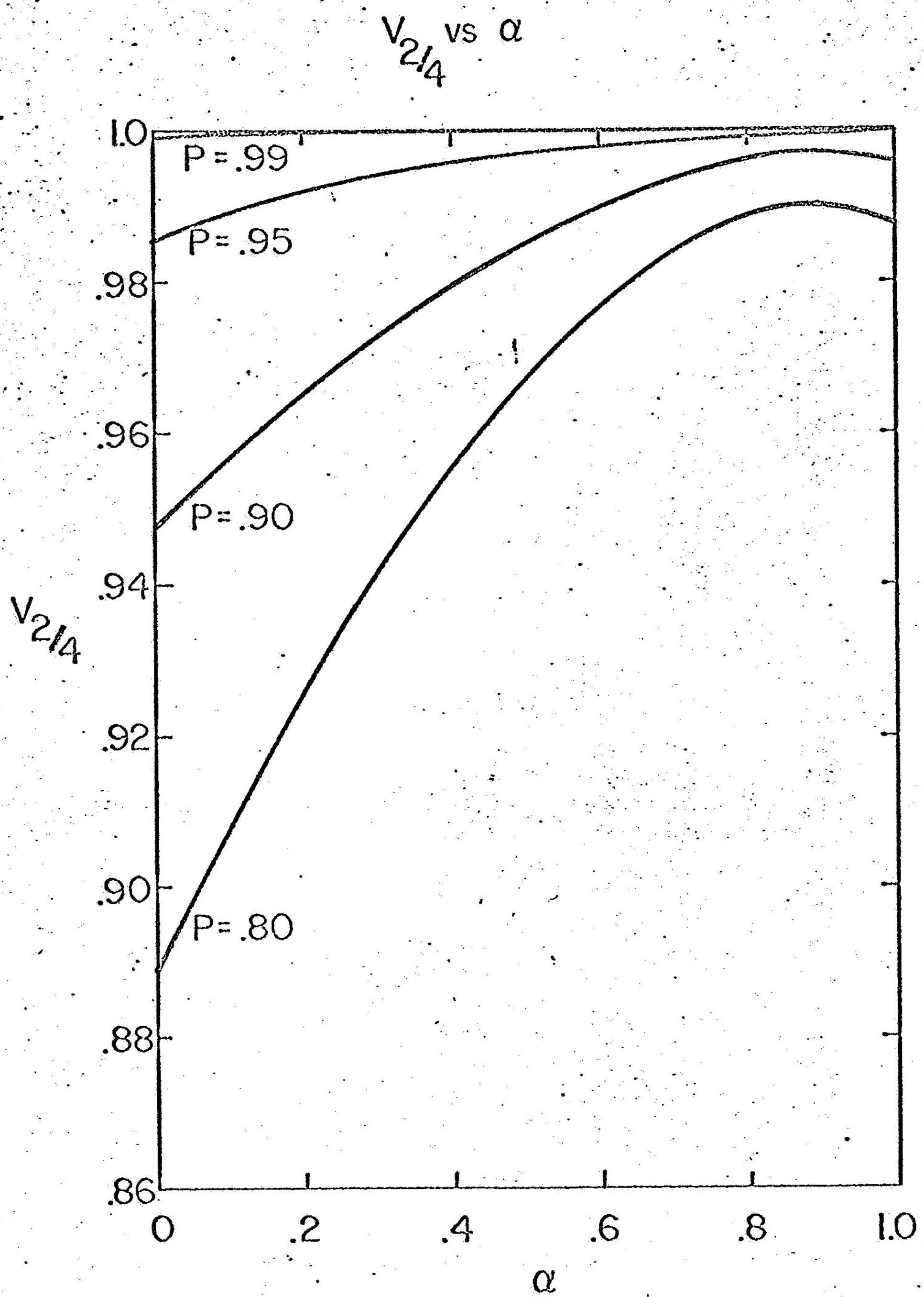
Fig. 12



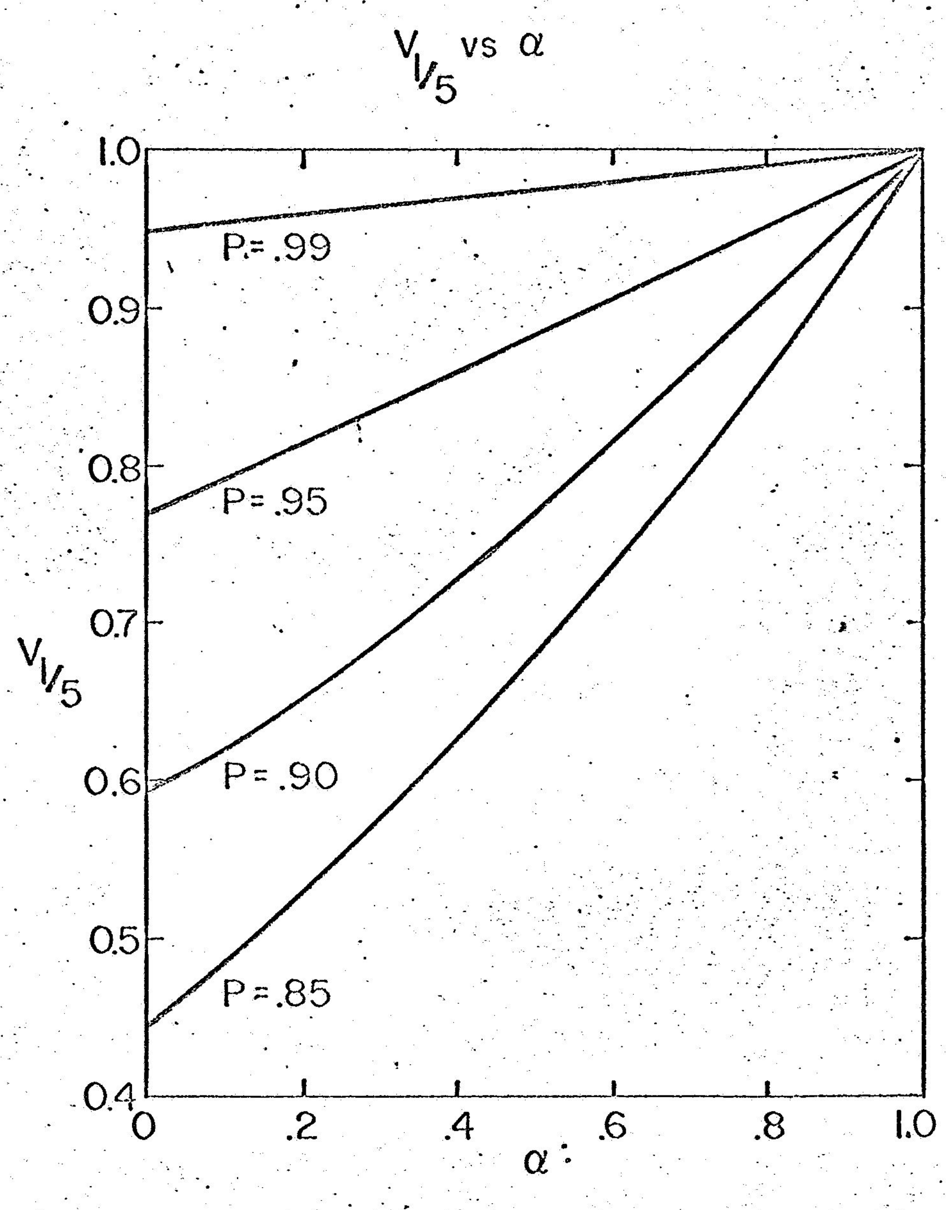
$V_{2/3}$ vs α
$V_{2/3}$
1.0
.98
.96
.94
.92
.90
.88
0
.2
.4
.6
.8
1.0
α
P = .99
P = .95
P = .90
P = .85



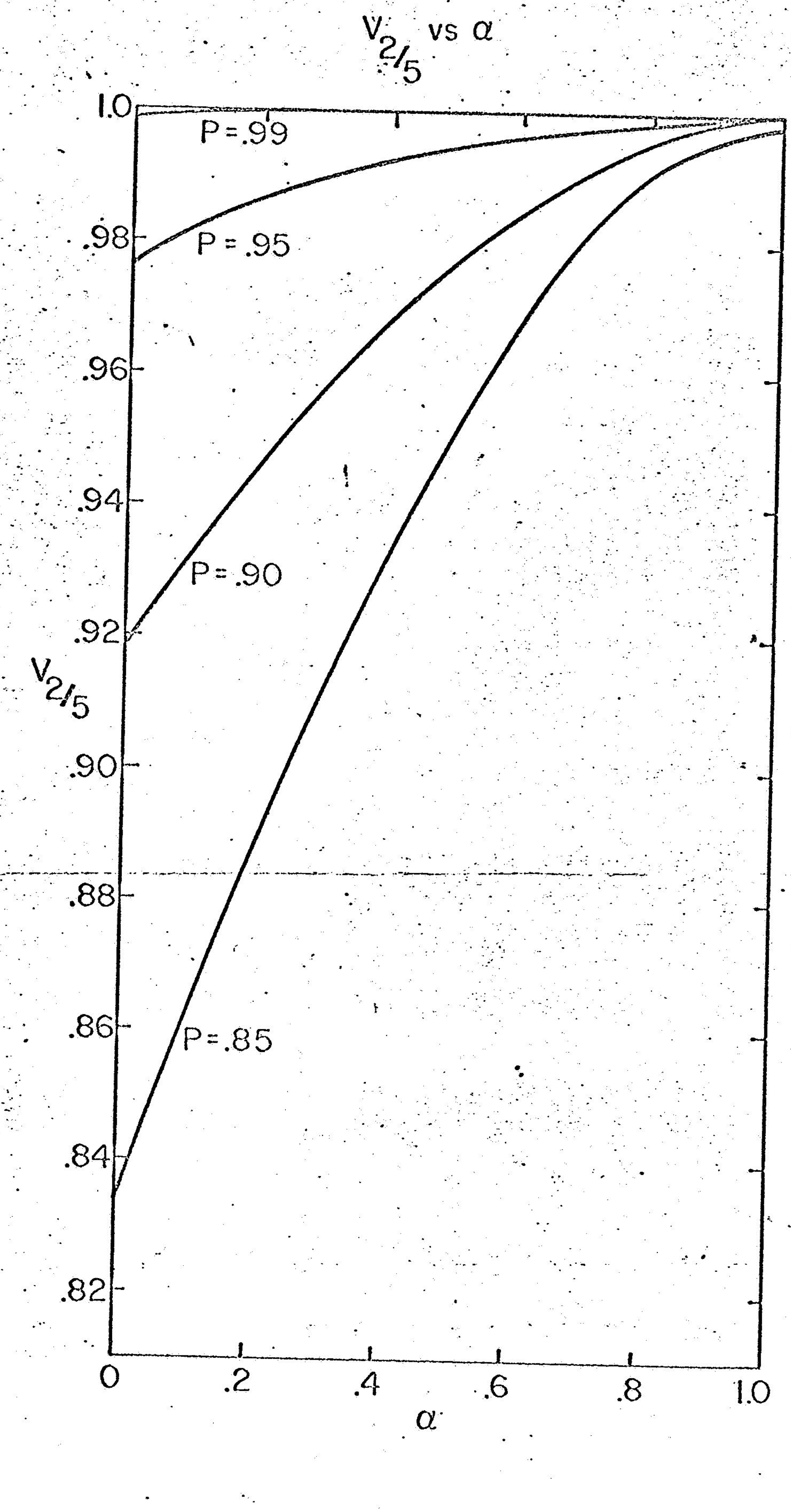
$V_{1/4}$ vs α
$V_{1/4}$
1.0
0.9
0.8
0.7
0.6
0.5
0.4
P = .99
P = .95
P = .90
P = .85
0
.2
.4
.6
.8
1.0
α

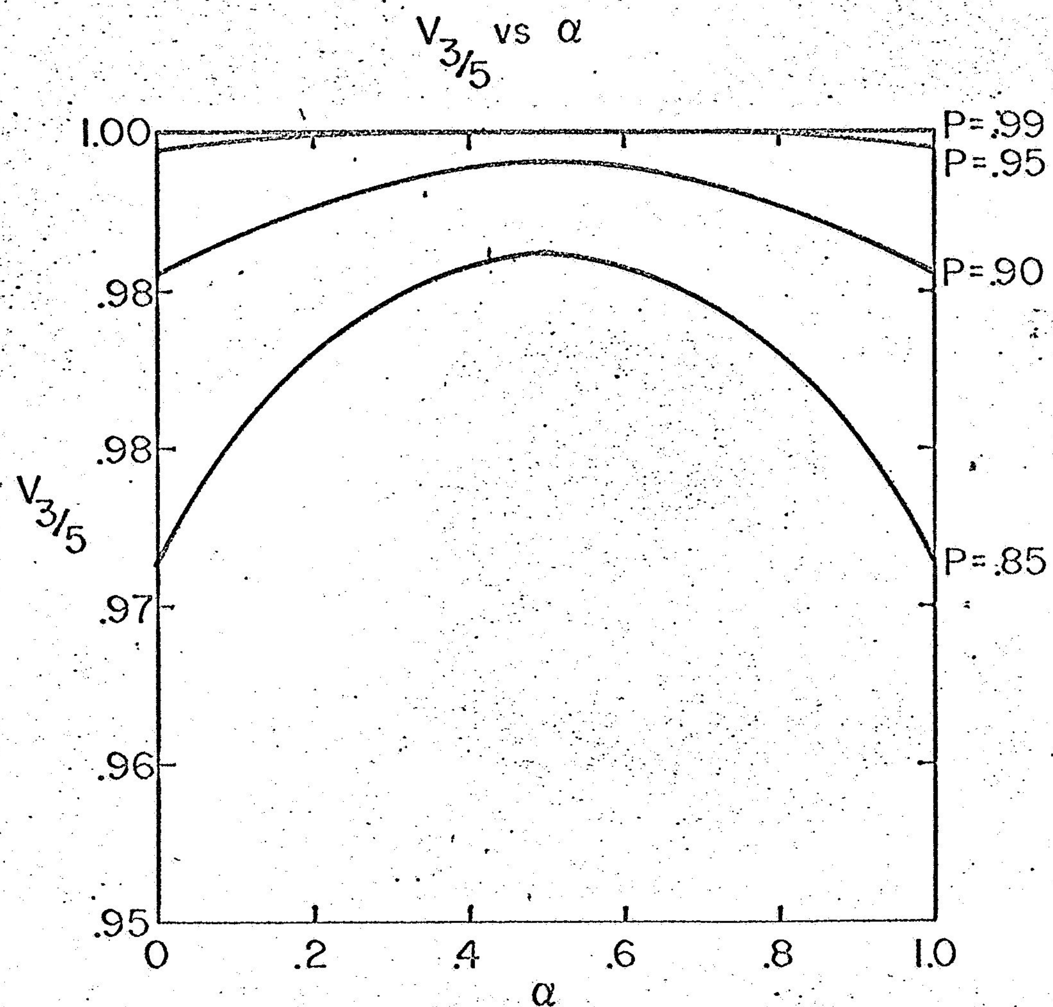


V2/4 vs α
1.0
.98
.96
.94
.92
.90
.88
.86
V2/4
P = .99
P = .95
P = .90
P = .80
0
.2
.4
.6
.8
1.0
α

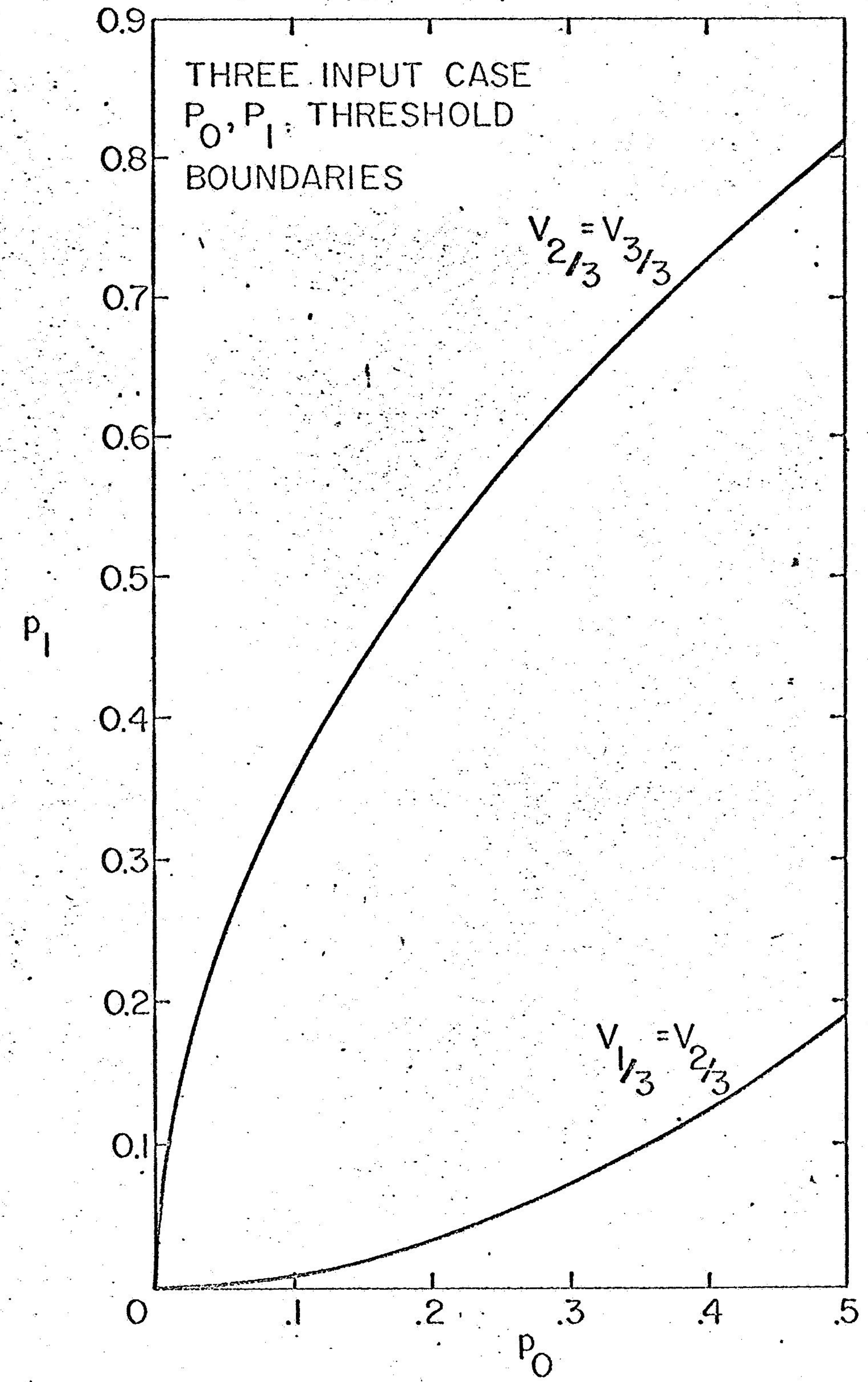


$V_{1/5}$ vs α
1.0
0.9
0.8
0.7
0.6
0.5
0.4
$V_{1/5}$
P=.99
P=.95
P=.90
P=.85
0
.2
.4
.6
.8
1.0
α

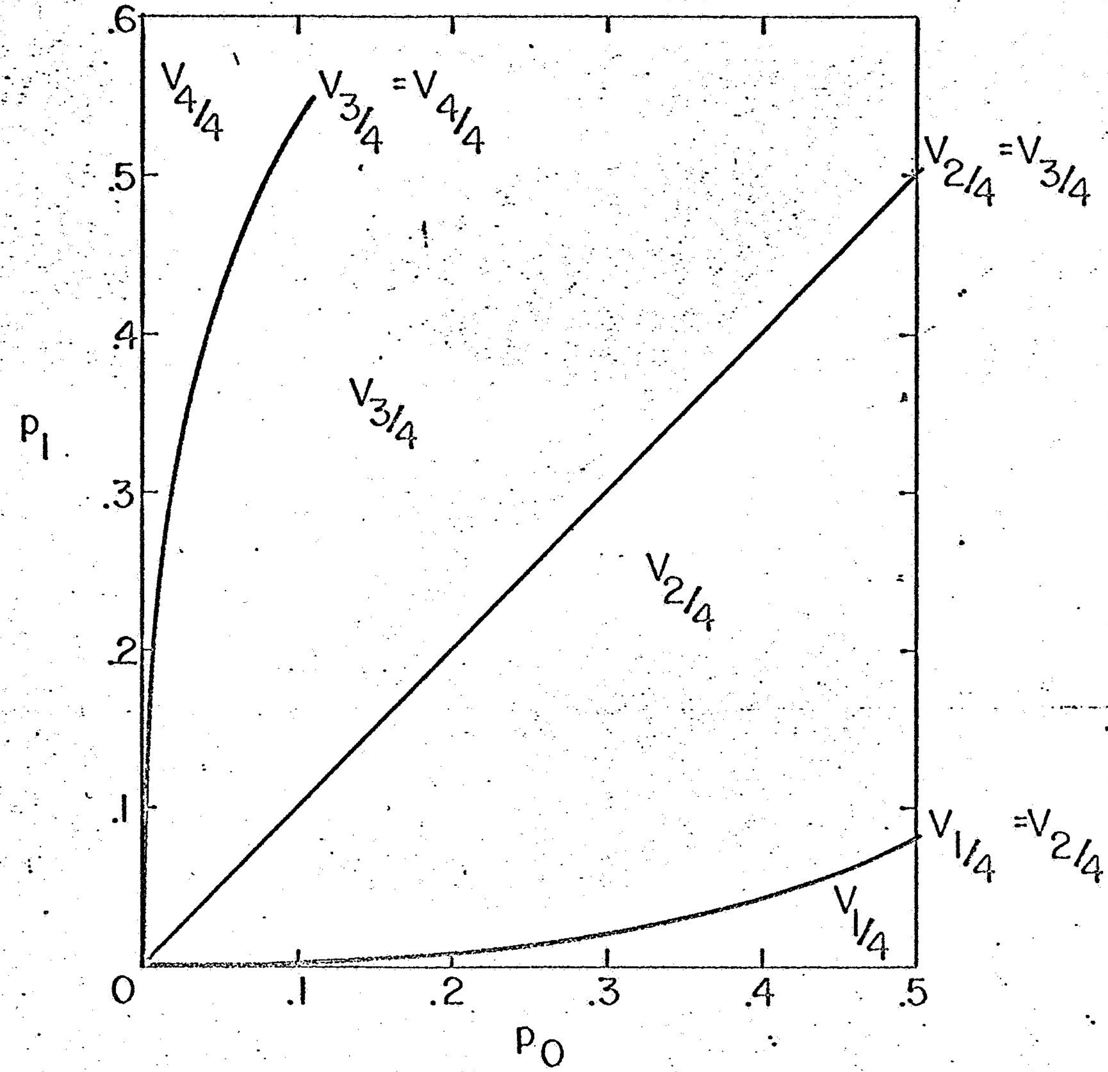

$V_{2/5}$ vs α
1.0
.98
.96
.94
.92
.90
.88
.86
.84
.82
$V_{2/5}$
P = .99
P = .95
P = .90
P = .85
0
.2
.4
.6
.8
1.0
α



V3/5 vs α
1.00
.98
.98
.97
.96
.95
V3/5
0
.2
.4
.6
.8
1.0
α
P=.99
P=.95
P=.90
P=.85

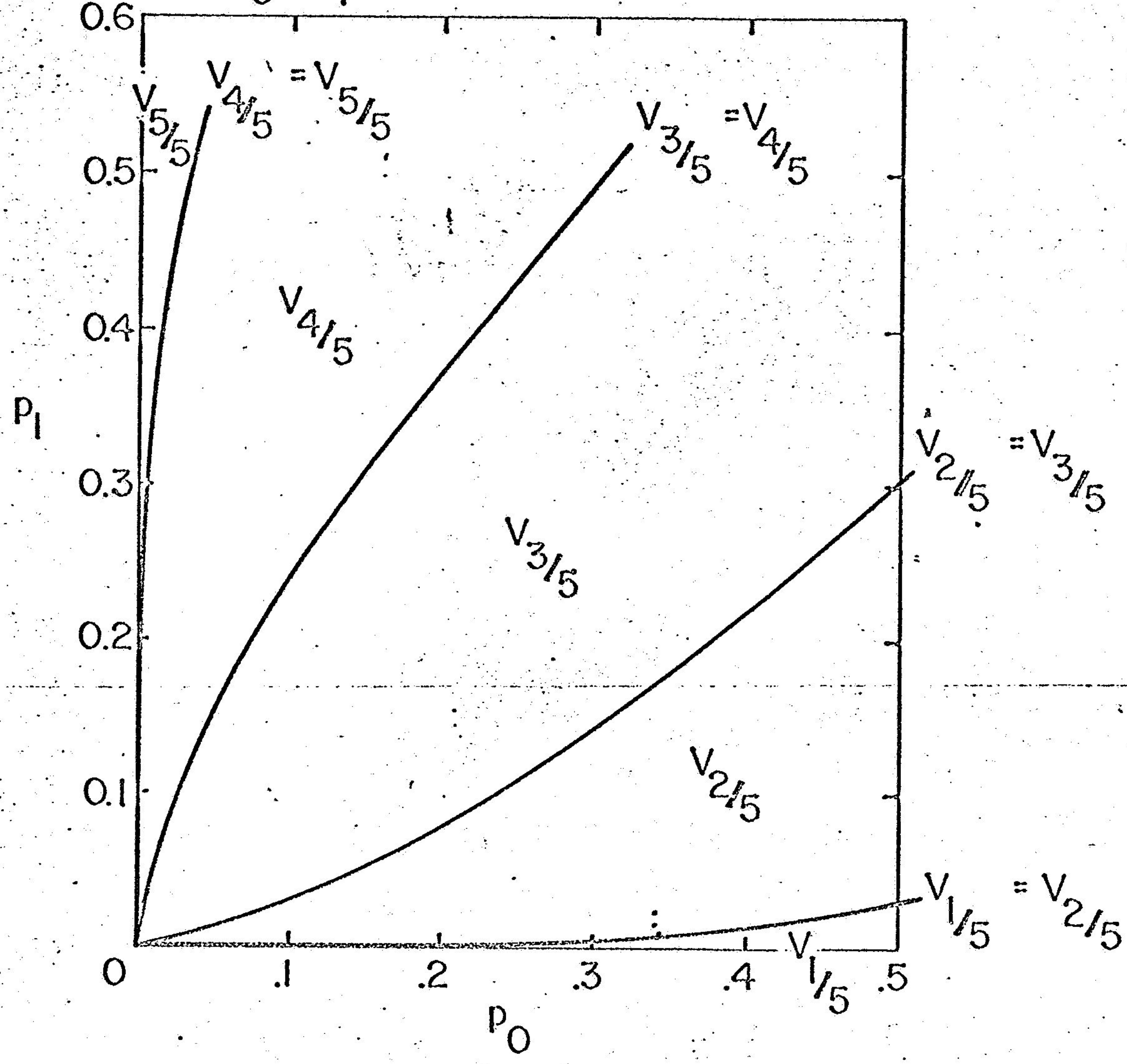

THREE INPUT CASE
P_0, P_1: THRESHOLD
BOUNDARIES
$V_{2/3} = V_{3/3}$
$V_{1/3} = V_{2/3}$
0.9
0.8
0.7
0.6
0.5
0.4
0.3
0.2
0.1
0
.1
.2
.3
.4
.5
p_1
p_0

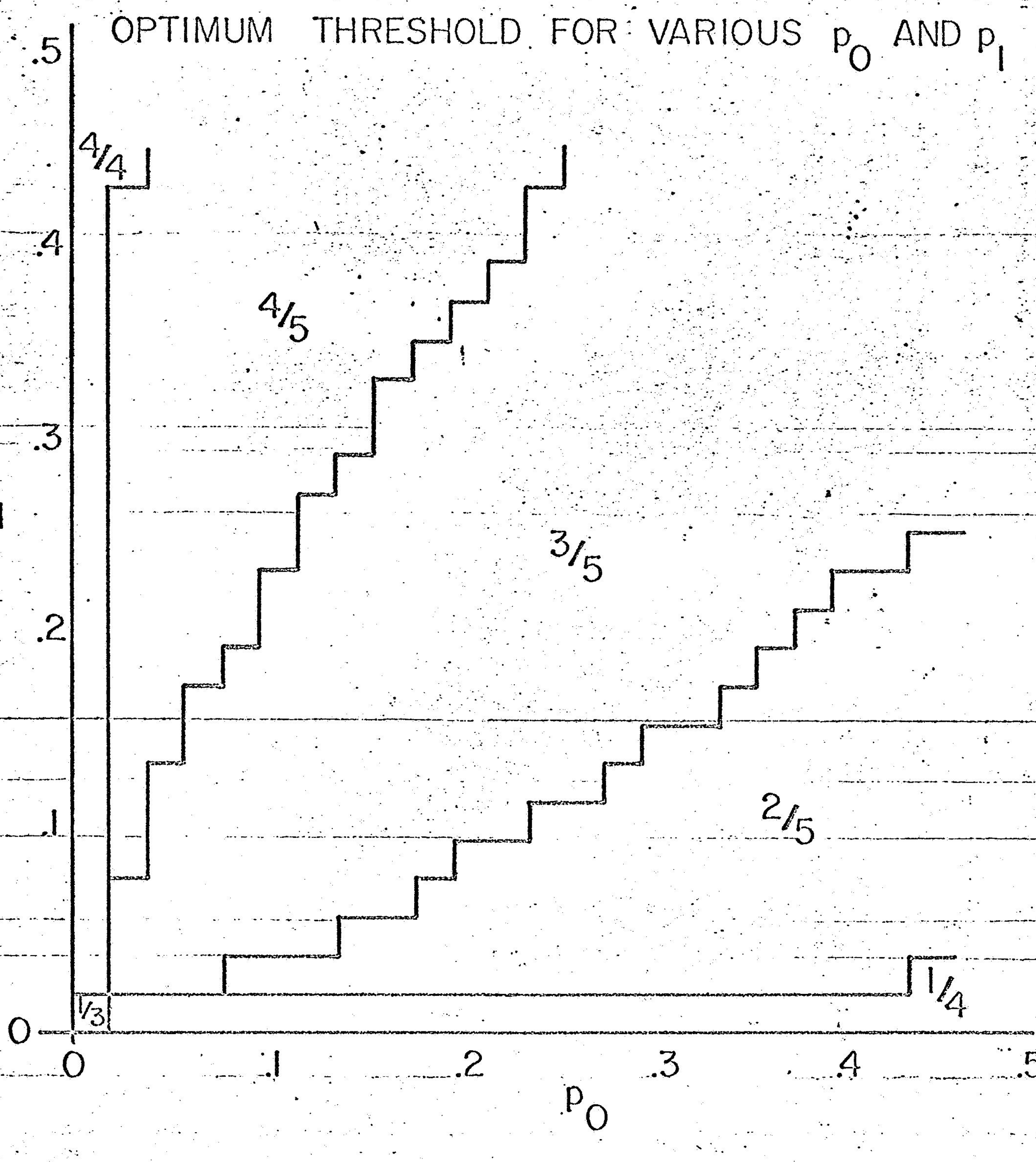
P_0, P_1 THRESHOLD BOUNDARIES



FIVE INPUT CASE

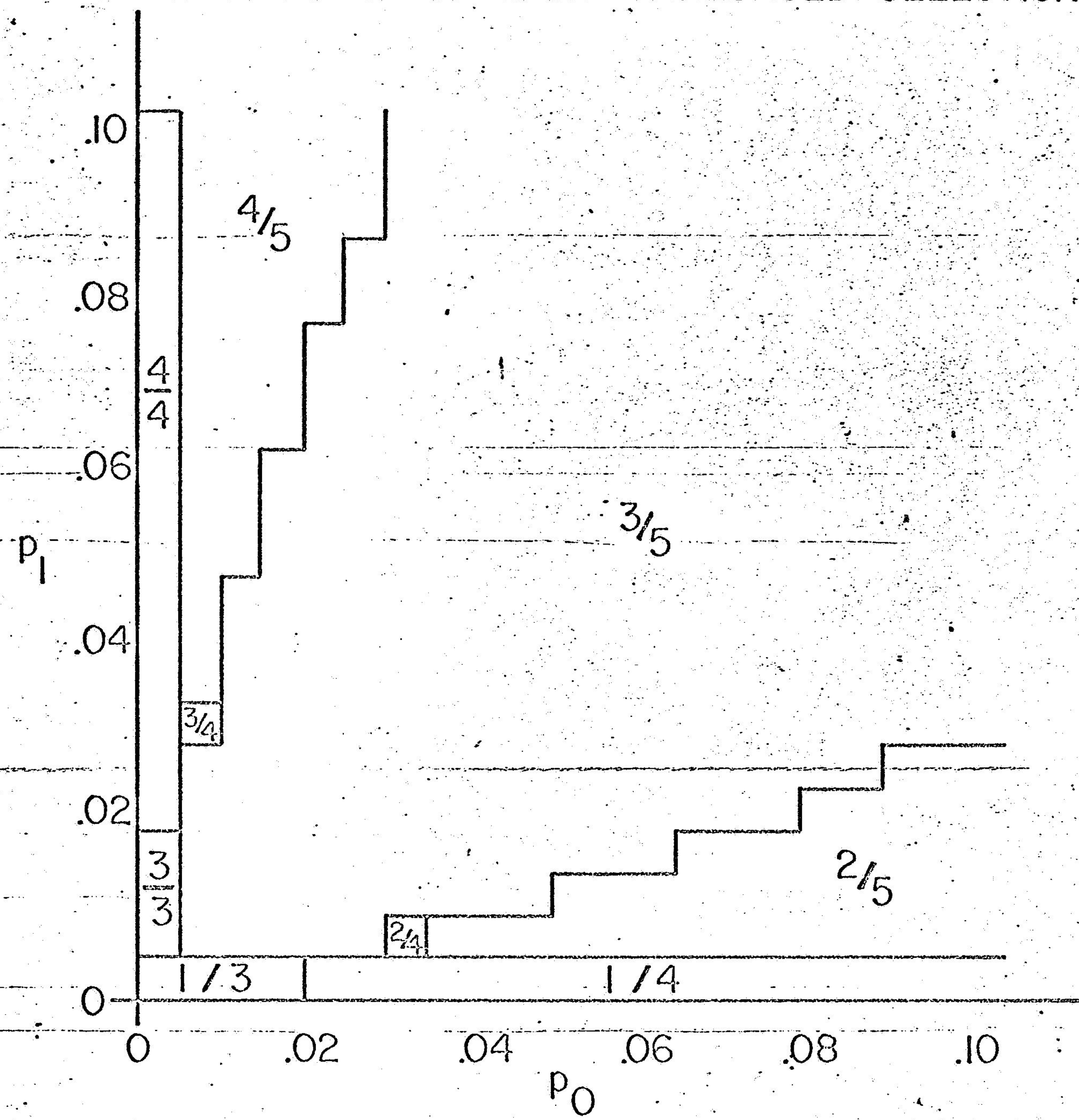
P_0, P_1 THRESHOLD BOUNDARIES

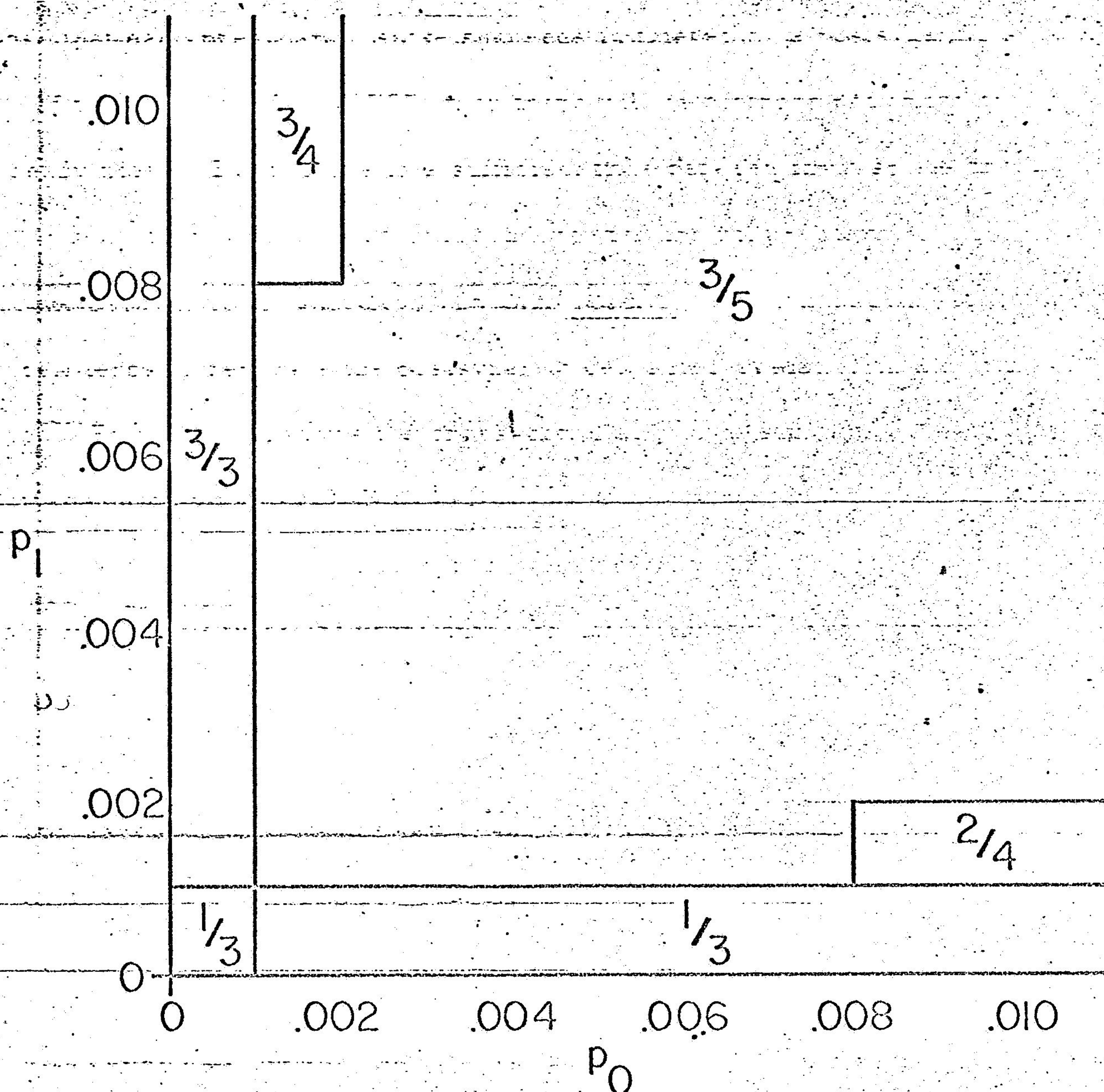




OPTIMUM THRESHOLD FOR VARIOUS p_0 AND p_1
.5
.4
.3
.2
.1
0
p_1
4/4
4/5
3/5
2/5
1/4
1/3
0
.1
.2
.3
.4
.5
p_0

MAPPING OF OPTIMUM THRESHOLD SELECTION





.010
.008
.006
.004
.002
0
p_1
3/4
3/5
3/3
2/4
1/3
1/3
0
.002
.004
.006
.008
.010
p_0