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FINAL REPORT

for

THE DEVELOPMENT OF ANALOG PROBABILITY SWITCHES UTILIZING FERRIELECTRIC TRANSPOLARIZERS

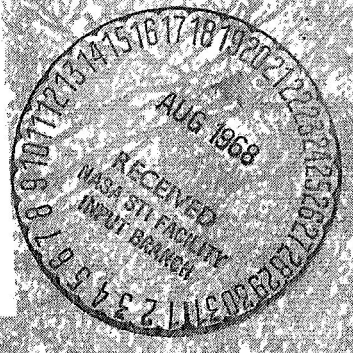
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Prepared by

Electrocrystal Corporation, Inc.

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ABSTRACT

The formation of invariant features and their use in recognition, decision and control processes is a crucial problem. In this connection, the question arises what type of signal processing could bring us closer to a solution of this problem. An attempt was made to develop a new signal processor which is believed to hold considerable advantages over existing processors. The fact that signals coming from the environment, normally do not provide information in a digitized form, and the transformation, storage as well as processing of such signals requires a sizable addition of electronic hardware strongly suggests that the direct processing of such signals of non-digital nature represented by multilevel samples offers considerable savings in electronic gear and provides advantages over digital processing

The aim of this contrast was to explore the possibility and lay the ground work for a new information processor which would respond to analog input signals, and which would be able to process such information without an analog to digital conversion. According to this new concept, the environment would be characterized by a number of internal models, which are represented by analog distribution functions describing environmental states having affine or similarity features, which have been derived and established by past experience. For deriving

various characteristic distributions for a given list of properties, an analog type signal transformation logic was conceived.

For storing these characteristic analog distribution functions represented by multilevel samples, a small analog associative memory was developed. In order to increase the probability of response, a floating analog storage register was conceived. For comparing and re-adjustment of sensed and learned features, a simple processor (Flag) was constructed.

Finally, an attempt was made to develop a trainable multilevel storage element.

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I. INTRODUCTION

Recent developments in ferrioelectrics and the ELECTRO-CRISTAL TRANSPOLARIZER* have suggested the possibility of a new approach to the development of statistical or probability switches for use in adaptive controls, learning devices, and feature-extraction equipment. ELECTROCRISTAL personnel have been observing, with keen interest, the advances made during the past several years by industry and the Government in the fields of bionics and adaptive controls. ELECTROCRISTAL's investigations with new ferrielectric materials, which parallel these studies, disclose the interesting use of solid state or switching circuits in which logic and memory properties are united. With such new components, large studies could be made in the fabrication of new and basic hardware for self-organizing adaptive devices.

To consider for a moment the final objective of the program, we would like to state our expectation of a new family of computers becoming available for NASA applications through this work. This family of devices will be a radical departure from conventional computation equipment and will provide multi-level non-destructive memory and the ability of self-organization. Future space-born computers will find considerable benefit in their ability of self-adaption and self-repair.

It has been known for some time that biological neuro-networks have revealed no evidence of the separate existence of memory and logical switching functions. In other words, a physiological network seems to be trainable and can alter its operational parameters. This does not require actual structural changes but merely probability (impedance or threshold) changes in an essentially invariant structure. As a consequence, it seems most likely that these two properties are united so that they are available for performing the function of an adaptive switching network which is dependent upon a characteristic distribution for a given list of properties. Such an operation may involve:

(1.) The reduction of the sensed information to invariant features utilizing an analog type signal transformation logic.

(2.) The storage of extracted features.

(3.) The comparison and re-adjustment of sensed and learned features.

(4.) The control and utilization of stored analog reference functions for recognition and decision.

With reference to (1.), it is proposed to utilize a composite distribution function derived from typical signal patterns or a family of analog reference distribution functions, which are discussed in more detail in Section II under the title "Signal Transformation Logic".

With reference to (2.), the storage of extracted features in form of

distribution functions requires storage of analog functions. This is accomplished in such a manner that a particular derived distribution function is represented by multilevel samples (1) (see Section III and IV, B).

With reference to (3.), the development of hardware has just reached the state that work on the comparison and re-adjustment of sensed and learned features became possible. A brief discussion of this phase of the work is presented in Section IV, B8.

With reference to (4.), no work was contemplated at this initial stage.

The most recently developed ferrielectric TRANSPOLARIZER* possesses several unique features which make it an outstanding candidate for adaptive controls. These features would include:

(1.) The possible coexistence of logic and memory.

(2.) Analog (multilevel) storage.

(3.) Low switching voltage.

Important advances in the development of ferrielectric materials have recently been made, rendering possible the preparation of a two-section TRANSPOLARIZER* having a total switching voltage of only 10 volts. This device then becomes readily compatible with transistors.

Electrocristal Corporation is pleased to report that the three novel ideas first proposed have been realized in a small scale laboratory analog associative memory. The concepts, which have been fully examined, were

the following:

(1.) The first involves the theory and logic of a multilevel logic-memory element.

(2.) The second involves the utilization of these elements to develop floating memory units, capable of storing whole analog functions.

(3.) The third involves the conceptual development of systems and the means of modifying either or both the reference and sensed distributions stored in the element, as a unit, to the environmental information.

II. SIGNAL TRANSFORMATION LOGIC

The use of multilevel samples for characterizing an event in the form of one or more distributions of various properties necessitated the clarification as to how such distributions can be processed from such events, for example, from voice or video type signals.

Without entering into a lengthy discussion of details, it can be briefly stated that human recognition processes simplify information in such a manner as to recognize, for example, a voice information regardless of how phase relationships develop due to reverberations, or in a video information, apparently without the need of scanning or search operations, etc. Although much more could be said about these physiological recognition processes, let us examine what kind of preprocessing methods could lead to similar transformations of an incoming signal. Since any sort of a learning system is based on a recognition process, the first step must be to develop a recognition process which could presumably operate in a fashion similar to the brain.

Corresponding to what has been said, theoretical work was initiated in three directions:

1. The characteristic features of the various distribution functions were established and tabulated so as to have a guidance toward electronic implementation of such density distribution functions.

2. Study was extended to develop an orderly mathematical process to break down an arbitrary distribution function

into the sum or product of simple distribution functions.

3. Effort was made to determine those types of simple distribution functions which are best suited for synthesizing composite distribution functions.

Besides studying the various distribution functions which have been compiled by Frank A. Haigho (2) and Marvin Felen and Norman C. Levers (3), the previous state of art on curve analyzers and graphical computers has also been studied. Some of the more significant of these works are listed below:

C. S. French (4) developed an analog electro-mechanical device which synthesizes a complex distribution curve by the summation of normal probability curves only, each of which is easily adjustable in position, width, and height.

M. Rogoff (5) developed a digital machine which fulfils a somewhat different function. Its mode of operation is the linear combination of whole spectra to fit the spectrum of a mixture of substances other than the resolution of a single spectrum into its component bands.

F. W. Noble (6) developed an electronic analog computer which analyzes a given distribution curve by synthesizing a number of Gaussian or Lorentzian distribution functions, each with adjustable parameters, and presenting, on an oscilloscope, the sum of these functions for comparison with the experimental curve being analyzed.

DuPont Co., Inc. (7) introduced the DuPont 310 Curve Resolver, a special purpose analog computer for resolving overlapping peaks in various analytical curves. This resolver is based on the device developed by V. W. Noble, which utilizes transistorized electronic circuitry.

In addition, information was accumulated on techniques and circuitries which were already in an experimental state for processing Gaussian, Rayleigh, Poission, Exponential and Lorentzian distributions. It appears, however, that little or no work has been done on the electronic processing of these distributions. The concept conceived for the processing of information transforms signals, images, or events (briefly referred to as a "pattern") to be recognized, into more than one discriminant function, each of which represents a distribution of a particular property of the pattern to be characterized. Accordingly, various property distributions would be processed from a particular pattern. Each one of these property functions would be a composite (not elementary) distribution function.

As a result of this research, three tables of probability (density) functions have been compiled, and their characteristic features have been tabulated. (Hereafter these functions will be referred to simply as "distribution functions".)

(a) Table I contains the more significant distribution functions, each of which can be electronically processed.

(b) Table II contains discrete distribution functions. Of those enumerated, the Poisson is the only one for which we have found an electronic method of processing.

#	Distribution	Probability Density Function $\phi(x)$	Distribution Function $\Phi(x)$	Mean Value $E\{x\}$	Variance $Var\{x\}$	Skewness v	Remarks
1	Gaussian	$\frac{1}{\sqrt{2\pi}} e^{-x^2/2}$ $(-\infty < x < \infty)$	$\frac{1}{2}\left[1 + \operatorname{erf}\left(\frac{x}{\sqrt{2}}\right)\right]$	0	1	0	$\operatorname{erf} z = 2\,\Phi_x(z/\sqrt{2}) - 1$
2	Rectangular or Uniform Distribution	$\begin{cases} \frac{1}{2\alpha} & (\lvert x-\xi\rvert < \alpha) \\ 0 & (\lvert x-\xi\rvert > \alpha) \end{cases}$	$\begin{cases} 0 & (x \le \xi-\alpha) \\ \frac{1}{2\alpha}(x-\xi+\alpha) & (\xi-\alpha \le x \le \xi+\alpha) \\ 1 & (x \ge \xi+\alpha) \end{cases}$	ξ	$\frac{\alpha^2}{3}$	0	x is uniformly distributed over the interval
3	Raleigh	$\begin{cases} 0 & (x<0) \\ \frac{x}{\sigma^2} e^{-x^2/2\sigma^2} & (x \ge 0) \end{cases}$	$1 - e^{-x^2/2\sigma^2}$	$\sqrt{\frac{\pi}{2}}\,\sigma$	$0.43\sigma^2$		The envelope of a band of normally distributed noise approaches a true Raleigh distribution as the bandwidth approaches zero.
4	Exponential	$\begin{cases} \frac{1}{\beta} e^{-\left(\frac{x-\xi}{\beta}\right)} & (x>0) \\ 0 & (x<0) \end{cases}$	$\begin{cases} e^{-\frac{\lvert x-\xi\rvert}{\beta}} & (x \le \xi) \\ 1 - e^{-\frac{\lvert x-\xi\rvert}{\beta}} & (x \ge \xi) \end{cases}$	$\xi + \beta$	β^2	2	Useful when the random variable is the length of an interval without the occurrence of a particular event where the average rate of occurrence of the event is β.
5	Causal or Dirac Delta	$\delta(x-\xi) = \begin{cases} 0 & (x=\xi) \\ \infty & (x=\xi) \end{cases}$	$U(x-\xi)$	ξ	0	Not defined	x is almost always equal to ξ. Note that the rectangular and Cauchy approximate a causal distribution as $\alpha \to 0$ or $\beta \to 0$
6	Lorentzian	$\frac{\alpha}{\beta^2 + x^2}$	$\frac{\alpha}{\beta} \arctan \frac{x}{\beta}$	0	1	0	An LC resonance curve describes a Lorentzian distribution.

TABLE I.
Continuous Probability Distributions

Distribution	Point Probabilities	Restrictions on Parameters	$E\{x\}$ Mean Value	$Var\{x\}$ Variance	ν Skewness	Remarks
Poisson	$e^{-\xi}\frac{\xi^x}{x!}$	$0 < \xi < \infty$	ξ	$\xi^{-\frac{1}{2}}$	ξ	Domain: $x = 0, 1, 2, \ldots \infty$; $\xi > 0$
Geometric	$\nu(1-\nu)^x$	$0 \le \nu \le 1$	$\frac{1-\nu}{\nu}$	$\frac{1-\nu}{\nu^2}$	$\frac{2-\nu}{\sqrt{1-\nu}}$	Domain: $x = 0, 1, 2, \cdots \infty$
Binomial	$\binom{n}{x}\nu^x(1-\nu)^{n-x}$	$0 \le \nu \le 1$	$n\nu$	$n\nu q$	$\frac{q-\nu}{\sqrt{n\nu q}}$	$q = 1-\nu$ Domain: $x = 0, 1, 2, \ldots, n$
Polya's or negative binomial	$p(x) = \left(\frac{\xi}{1+\beta\xi}\right)^x \frac{1(1+\beta)\ldots[1+(x-1)\beta]}{} p(0)$ $p(0) = (1+\beta\xi)^{-\frac{1}{\beta}}$ $(\xi>0, \beta>0)$ $(x \ge 0)$		ξ	$\xi(1+\beta\xi)$	See (2)	1) Polya's distribution reduces to the Poisson distribution for $\beta = 0$, and to the Geometric distribution for $\beta = 1$ 2) $\upsilon = \frac{(1+\beta\xi)+\xi/n}{\sqrt{\xi(1+\beta\xi)}}$ $(n \ge 0)$

TABLE II.
Discrete Probability Distributions

(c) Table III contains those distribution functions which Medgyessy (8) has found suitable for superposition and which he has tested mathematically.

In this processing operation, one of the most important considerations is the speed by which such a distribution can be processed. Another important consideration in selecting distribution functions for characterizing a pattern is whether or not it is suitable for the decomposition of composite distribution functions into elementary distribution functions. Medgyessy was the first who systematically treated this problem of the decomposition of superpositions of distribution (density) functions of one variable.

The representation of a composite distribution function in terms of elementary distribution functions seems to be a very sophisticated mathematical task. Medgyessy gives in his book the mathematical criteria for those elementary distribution functions which are suitable for the representation of composite distribution functions by superpositions. According to his findings, there are about eight distribution functions (see Table III) which can be used. (The characterization of those distribution functions already given in Tables I and II are not repeated in Table III). The reader should be mindful that most of the electronic distribution processors so far developed did not consider the importance of speed by which a particular distribution should be processed, and therefore, the electronic implementation of such processors should be regarded at this writing as an unsolved problem. Although this work actually constitutes only a beginning step towards

#	Distribution	Probability Density Function $\phi(x)$	$\Phi(x)$ Distribution Function	$E\{x\}$ Mean Value	$\mathrm{Var}\{x\}$ Variance	υ Skewness	Remarks
1	Cauchy	$\frac{1}{\pi\alpha}\,\frac{1}{1+\left(\frac{x-\xi}{\alpha}\right)^2}$	$\frac{1}{2}+\frac{1}{\pi}\arctan\frac{x-\xi}{\alpha}$	$E\{x\}$ and $\mathrm{Var}\{x\}$ do not exist; the Cauchy principal value of $E\{x\}$ is ξ.		Not defined	Distribution of $x=\xi+\alpha\tan y$ if y is uniformly distributed between $y=-\pi/2$ and $y=\pi/2$ (rectangular distribution). Cauchy's distribution is symmetric about $x=\xi$. Half width and interquartile range are both equal to 2α.
2	Beta	$0 \quad (x\le 0, x\ge 1)$ $\frac{\Gamma(\alpha+\beta)}{\Gamma(\alpha)\,\Gamma(\beta)}\,x^{\alpha-1}(1-x)^{\beta-1}$ $(0<x<1)$ $(\alpha>0,\ \beta>0)$	$0 \quad (x\le 0)$ $I_x(\alpha,\beta) \quad (0\le x\le 1)$ $1 \quad (x\ge 1)$	$\frac{\alpha}{\alpha+\beta}$	See (1)	$\frac{2(\alpha-\beta)}{(\alpha+\beta+2)}$	1) $\mathrm{Var}\{x\}=\frac{\alpha\beta}{(\alpha+\beta)^2(\alpha+\beta+1)}$ 2) $I_x(\alpha,\beta)$ is the complete beta function ratio; unique mode $(\alpha-1)/(\alpha+\beta-2)$ for $\alpha>1,\ \beta>1$.
3	Gamma	$0 \quad (x\le 0)$ $\frac{1}{\beta^{\alpha}\Gamma(\alpha)}\,x^{\alpha-1}e^{-x/\beta}$ $(x>0)$ $(\alpha>0,\ \beta>0)$	$0 \quad (x\le 0)$ $\frac{1}{\Gamma(\alpha)}\,\Gamma_{x/\beta}(\alpha)$ $(x\ge 0)$	$\alpha\beta$	$\alpha\beta^2$	$2/\sqrt{\alpha}$	$\Gamma_x(\alpha)$ is the incomplete gamma function.
4	Logarithmic Normal	$0 \quad (x\le\alpha)$ $\frac{1}{(x-\alpha)\sigma\sqrt{2\pi}}\,e^{-\frac{1}{2}\left[\frac{\log_e(x-\alpha)-u}{\sigma}\right]^2}$ $(x>\alpha)$	$\int\phi(u)\,du$ $u=\frac{\log x-\log\xi}{\sigma}$ $(0<x<\infty)$	See (1)	σ^2	$\sigma\log x$	1) $E\{x\}=\xi\times 10^{\frac{\sigma^2}{2\log e}}$

Note: The Gaussian, Poisson, Binomial, and Polya distributions are also suitable for superposition.

TABLE III.

Continuous Probability Distributions Suitable for Superpositions

the characterization of electrical signals by some of their composite (not elementary) distribution functions, it serves, however, the purpose of offering a more realistic approach to the design requirements of a multilevel-logic memory.

With reference to Tables I, II, and III some work has been done to determine what property of an electrical signal can best be described by a particular type of distribution function. The focal point of this study was to determine the conditions which must be met by an electronic processor to extract the distribution of a particular property, such as frequency spectrum or zero crossings, from an electrical signal. In investigating, for example, the mathematical properties of a Poisson distribution, it becomes clear from both the extraction of sets of samples and the organization of these sets into a distribution, that the Poisson distribution is well suited to describe a process such as the one present in an electrical signal known as zero crossings. More generally speaking, it is well suited to describe processes, phenomena, etc., in which the distribution of events is weakly coupled or weakly interrelated; and this coupling or interrelation is not of a long range type. In contrast, a pure normal distribution describes events having no coupling or which are not interrelated. This characterization of the various distribution functions will later permit the specification of various electronic devices which are suitable for the extraction of some particular features from an

electrical signal. Table IV of this report gives examples of properties the distribution of which may be most aptly described by a particular distribution function.

At this point, a question could arise as to what benefits are to be derived from this mathematical study.

First, it is one of the new concepts of this work to characterize a pattern representing a signal by its characteristic features. These characteristic features are represented in the form of distribution functions.

Second, depending upon how closely a particular pattern representing intelligence is to be specified, particular numbers of characteristic properties have to be used for the description of that pattern. Accordingly, if the distribution of the various properties of a given pattern is known, such a specification becomes possible. It is evident that one type of distribution function could specify a particular pattern only loosely: depending upon how close the specification is desired, additional distribution functions need to be invoked.

Thus it is clear that if we want to specify the various properties of, let us say, a sine wave, or any other pattern, the distribution of the various properties of such a pattern must be known - in other words - we must be able to process the distribution of a particular property.

Normal Distribution	The statistics of peaks of a random signal over the amplitude range. It is suitable to characterize the amplitude features of a signal. Composite normal distributions would have the same features.
Rayleigh Distribution	The statistics generated by the linear (envelope) detection of a narrow band of Gaussian noise. It is characterized by the distribution of the envelope of the peaks and represents modulation intensity properties.
Poisson Distribution	The statistics of zero crossings of band-limited white noise. It is suitable to characterize the frequency of a signal without obtaining the intensity of the signal.
Frequency Distribution	The statistics of one countable number of possible values of a random signal such as frequency of occurrence. It is suitable to characterize spectral density.

TABLE IV
Examples for the Characterization of Some Properties of Electrical Signals by Probability Distributions

A. Conceptual Example of a Pattern Discriminator using Analog Distribution Functions as stored Prototype Functions

As an example of a pattern discriminator using analog statistical switches, which in another terminology may also be called an analog associative memory, FIGURE 1 is included. An analog statistical switch may be defined as a switch which responds to a particular distribution of analog signals. Such a switch may sometimes be regarded as a special filter. It may also be looked upon as a pattern discriminator. The property distribution processors $\Phi_i(x)$ give the distribution of the various properties of a particular pattern, such as frequency spectrum, zero crossing, density distribution of peaks with amplitude, etc. The output of each distribution processor feeds into a set of statistical switches $g_j[\Phi(x)]$ comprising typical distribution functions stored in the form of multilevel samples within a particular (i) class of properties. The outputs of the various groups of statistical switches are discriminated in a "Flag", and the outputs of the "Flag" are further processed in the response device (shown schematically). FIGURE 2 represents a preliminary concept of such an analog associative discriminator denoted by $g_1[\Phi(x)], g_2[\Phi(x)], \ldots g_n[\Phi(x)]$ having a flexible internal distribution function stored in the form of discrete samples of the just described distribution functions and by the settings of the TRANSPOLARIZERS* in Column 1b, while the incoming signal can be simulated by the settings of the TRANSPOLARIZERS* in Column 1a. However, before

FIGURE 1: Conceptual Example of an Analog Pattern Discriminator

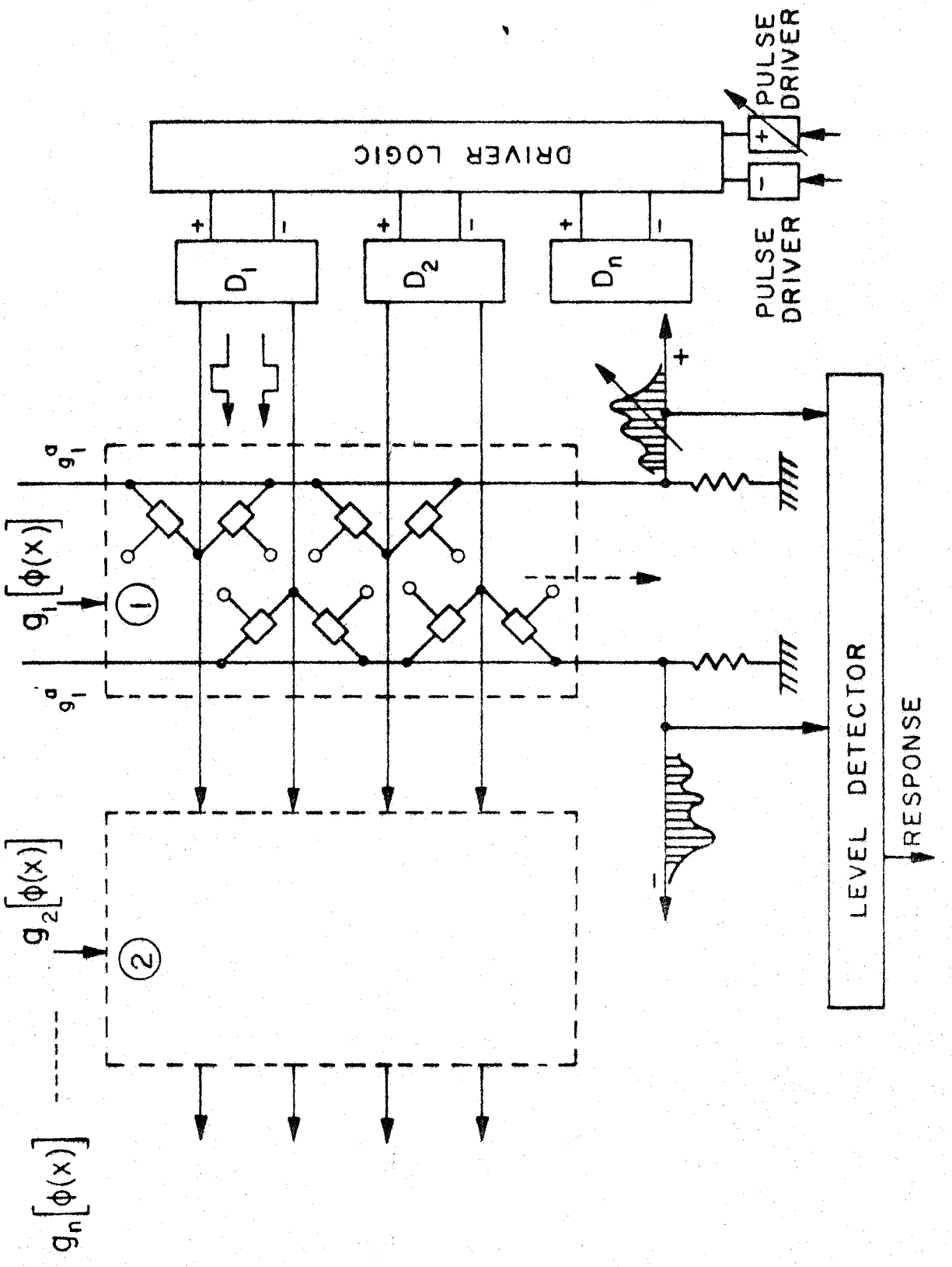


FIGURE 2: An Element of an Analog Associative Discriminator

the operation of an analog associative memory, which is the core of such a discriminator, can be discussed in more detail, an introductory presentation on the proposed analog associative memory and the TRANSPOLARIZER* is given in Section III, B, and C.

III. THE ANALOG STORAGE OF EXTRACTED FEATURES

From the foregoing, it is apparent that the core of this new pattern recognition and learning system is a type of memory which, instead of storing digital words stores "whole analog functions" represented by semi-continous multilevel samples. Furthermore, it is also evident that all of the stored analog functions must be simultaneously interrogated in order to eliminate time consuming search operations and obtain an instantaneous response. Since, according to our present concept, the human brain seems to operate in a similar manner, this type of memory may be appropriately called an "analog associative memory". It should be noted here that according to our knowledge, this is the first of this kind of memory and it is hoped that it may open a large field of applications. The implementation of this novel memory concept has been our main concern in this first phase of work.

A. Previous History

Von Steinbuch and Frank (1) show that the use of analog techniques offers extraordinary possibilities for the formation of invariants. They suggest the use of an impedance matrix as a learning element. In this impedance matrix, various types of resistors and transfluxors were utilized to represent a set of models of the external world, with the properties that these models should be alterable, so as to be able to fit them to the

experience gained externally, and then use them as invariant features for comparison. In this learning method, the stored and learned characteristics, represented by vector components, are cross-correlated. A selection gate with a response to the maximum sum of the vector products gives a response on only one of the rows representing the closest property function. Each row connects to a set of impedances, each of which represents one vector component describing the model. This implies that the individual impedances must be able to assume analog values. In this connection, it is noted that if a set of impedances represents the sampled analog information, the information storage capacity of such a system is enormous as compared to a digital storage system. For example, a ten digit memory with the capability of n stored levels within each digit affords a storage capacity of n^{10}. The possible savings in actual hardware with such a combined analog-digital learning system appears to be quite significant. FIGURE 3 presents a ferrielectric analog-digital learning matrix of this type. The conductances of the TRANSPOLARIZER* Y_{11}, Y_{12}, Y_{13}, - - - Y_n represent the stored features of a particular model which are set through inputs 1, 2, 3, ---n. These inputs, being of high impedance character, may be directly controlled by small photocells arranged in a pickup matrix. The learned features are another set of vector components represented by the voltages e_1, e_2, e_3, --- e_n. The vector products of $Y_{1j}\ e = i_{1j}$ and the $\sum_j i\ j$ is invariant at their maxima's provided the model represented

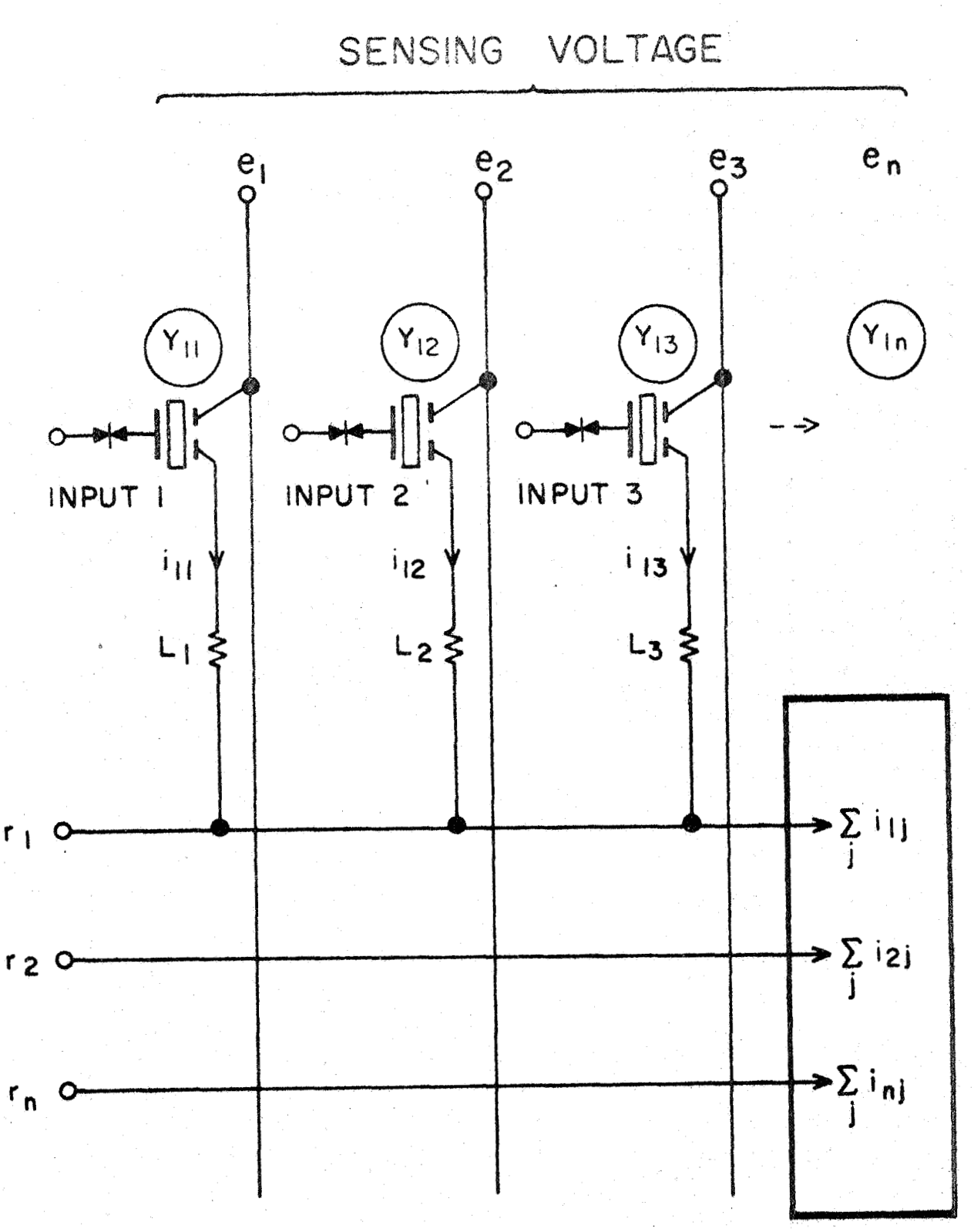


FIGURE 3: Ferrielectric Analog-Digital Learning Matrix

by the Y_{ij} components on a particular row is in a good correlation with the learned components. The sum of currents i_{ij} actuate a selection gate with a single output on that row at which the $\sum_j i_{ij}$ is maximum. This concept was studied since it became evident that the TRANSPOLARIZER* is uniquely suited to implement an analog storage system.

B. The Proposed Analog Associative Memory

According to ELECTROCRISTAL's concept, a particular piece of information would be presented by a statistical distribution of a particular property of said information in the form of voltage amplitudes or impedance levels, derived from the information by various types of distribution function processors and would be stored in a set of TRANSPOLARIZERS* for further processing.

The processing would essentially be directed toward eliminating redundancies and information elements which are not invariant. The elimination of grey or non-essential information would leave a substantially reduced distribution, which should then approach the invariant learned features of the initial distribution.

The extraction of invariant features of a pattern must be produced by the property distribution processors utilizing appropriate transformation logic. Since, however, such processors were at this writing not available, both stored prototype distribution function as well as the interrogating distribution function were simulated by arbitrary settings of two sets of

memory registers (see FIGURE 2). The analog associative memory comprises a larger number of such analog prototype functions representing models of the environment and are stored in lumped multilevel TRANSPOLARIZER* memory registers denoted by (1), (2), n. The interrogation distribution function is presented to all prototype functions simultaneously for comparison or correlation purposes. The number of prototypes depend on the type of pattern to be recognized, such as acoustic or video, etc. The prototype functions in the matrix can also form a number of groups depending on the type of properties stored in them. In the past, the conventional approach to pattern recognition was based on the utilization of the minimum distance between derived and stored prototype functions which were, during the recognition process, essentially not variable, and provided rather narrow decision regions. In contrast, the proposed learning matrix involves the concept of processing "whole functions" stored in the matrix, which are, however, flexible and can be altered or floated around their initial state so as to conform as close as possible to the interrogating distribution.

The fluctuations may represent any sort of linear or non-linear transformations and afford the producing of desired similarity distribution functions in a clustered manner around a typical distribution. Although the fluctuating reference function may not become identical with the interrogating functions, the fact, however, that the similarity functions so generated are planned to remain within the boundaries of the decision

regions, would increase the probability in obtaining a proper minimum distance, and a more correct decision could be achieved.

The desired fluctuation is obtained by altering the driver logic, which can be done by changing the rate, amplitude, etc. of the pulse drivers shown in FIGURE 2. Each TRANSPOLARIZER* column can be sequentially driven by the drivers D_1 , D_2 , D_n. The drivers are driven by a driver logic, which generates sequential outputs as a clock pulse input drives the logic. This driver logic is constructed in such a manner that after a single sequence of driving pulses has switched the sixteen TRANSPOLARIZERS* through a complete cycle, an additional seventeenth driving board is activated. This driving board sends out an opposite polarity restoring pulse, and switches all sixteen TRANSPOLARIZERS* back to their original stand-by position. More details will be given in Section IV. This process may be compared in a loose sense with a synchronization process utilized in the television and other electrical fields.

Due to the interesting properties of the TRANSPOLARIZER*, the prototype function can be directly trained onto the lumped multilevel TRANSPOLARIZER* memory registers utilizing the error correcting training technique. The implementation of this principle was attempted and the results were very promissing. This adaptive training of multilevel TRANSPOLARIZER* memory registers may become an important feature if the prototype functions are to be derived directly from the

environment and be used later as references. Conditioning or motivation is accomplished by using the error signal as a negative feedback on the inputs of the TRANSPOLARIZERS* which may act like a "kinesthetic feedback". (see Section IV, B. 8)

C. The TRANSPOLARIZER

The discovery of man-made ferrielectrics and their favorable technological properties (9) (10) opened up a large field of applications in which the unique ferroelectric properties of these new materials can be utilized. In ferrielectric devices, similar to ferroelectric devices, switching storage properties are simultaneously present. They have, however, similar to ferrite cores, a switching threshold field. The simultaneous presence of these three features, namely, switching, storage, and threshold field properties, make ferrielectric devices extremely useful. It is noted that these devices are voltage devices, and therefore the current requirements are far less severe than in their magnetic counterpart, the transfluxor (11).

One of the most interesting recent achievements in the semiconductor field is the utilization of ferrielectric materials in an electrostatically controlled circuit impedance with stored settings called the TRANSPOLARIZER.

FIGURE 4 represents a two-path transpolarizer comprising two identical ferrielectric storage cells connected in series. FIGURE 5 is a photograph of a transpolarizer mounted in a transistor socket. When the polarization of both crystal sections is identical, a sensing pulse opposing

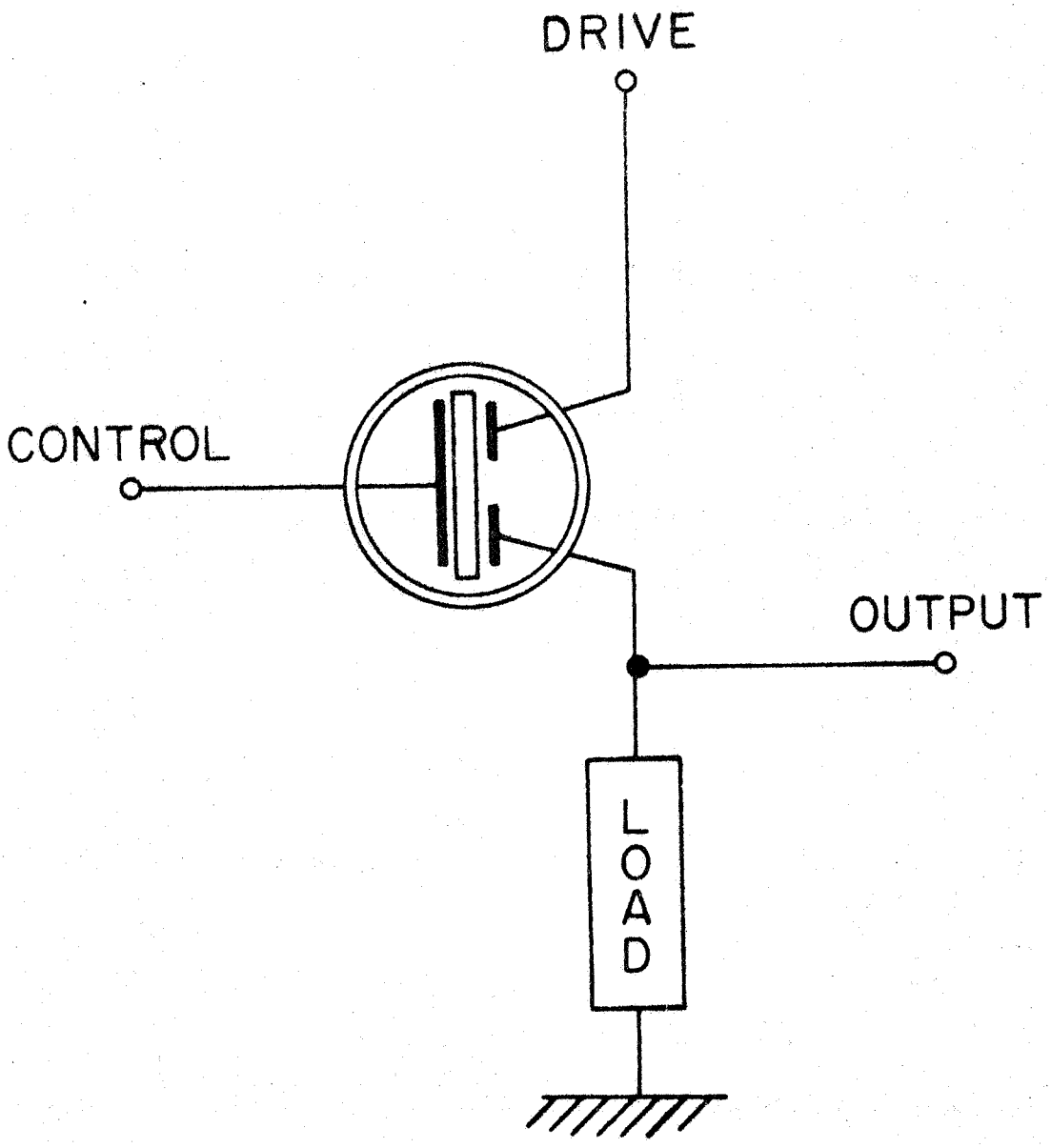


FIGURE 4: Schematic Representation of a Two-Path Transpolarizer

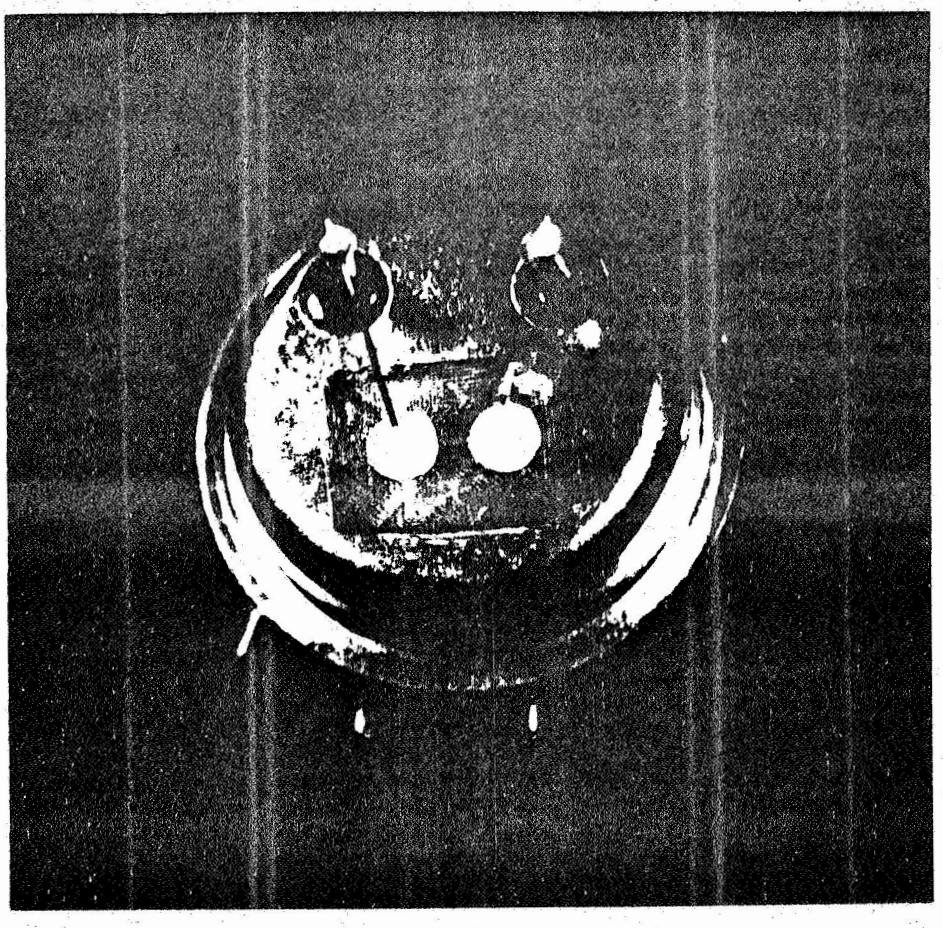


FIGURE 5: Transpolarizer Mounted in a Transistor Rocket

these polarization directions can switch both storage cells, or if a sine wave is applied as a sensing signal, it will find a low impedance since each half period can switch both condensors. If, however, the polarization of the two crystals is opposite, for either polarity of a sensing pulse or sine wave, one of the two storage cells will be driven increasingly in saturation where dielectric constant is small and therefore represents a small capacity, i. e., high impedance, and neither of the storage cells can be switched. When both cells are polarized in the same direction, a binary "1" is stored and when the polarization in the two cells is opposite, a binary "O" is stored. The set, block, and unblock pulses are supplied through magnetic reed relays, gas discharge tubes, photoelectric cells or double anode saturation diodes to the control terminal in order to isolate these pulse sources from the circuit itself.

The transpolarizers initially developed possessed an adverse feature, namely, regardless of the pulse applied to the control point, both polarity pulses caused a blocked state. This feature of the earlier transpolarizers required a quite complicated circuitry for setting the blocked and unblocked states. A description of these early devices is given in a final technical report (12), in Section IV, A and B. In order to simplify the set or write-in operation of the transpolarizers, a new transpolarizer was developed which could be blocked by a positive polarity pulse, and unblocked by a negative polarity pulse. A complementary device was also

developed. This novel type of transpolarizer was used in this work. The underlying principle of this new type of transpolarizer is that if asymmetrically biased ferrielectrics are properly oriented and electrically connected in series, as indicated in FIGURE 6, they establish a net hysteresis loop which is symmetric in all respects. If a d-c field is applied to the center point between the two ferrielectric elements, the effect on the bias is the same in both elements, i.e., it either adds to or reduces the internal field; thus when elements are connected in series, so long as the magnitude of the internal field of both is the same, complete hysteresis loop symmetry remains, and the net polarization will change as a function of the field applied to the center point "X", and will depend on the state of polarization in the series sections of the ferrielectric elements; as a consequence, multilevel storage is possible.

The practical use of ordinary ferroelectrics until now was limited because of fatigue effects and lack of a threshold field. These problems have been resolved because these new ferrielectric materials, having ferroelectric properties, possess a threshold switching field. The basic element in all of these devices is a condenser with a dielectric exhibiting ferrielectric properties. When two or more ferrielectric capacitors are in a common path or paths and polarization of the condensers can be individually controlled, interesting new switching and storing functions can be achieved.

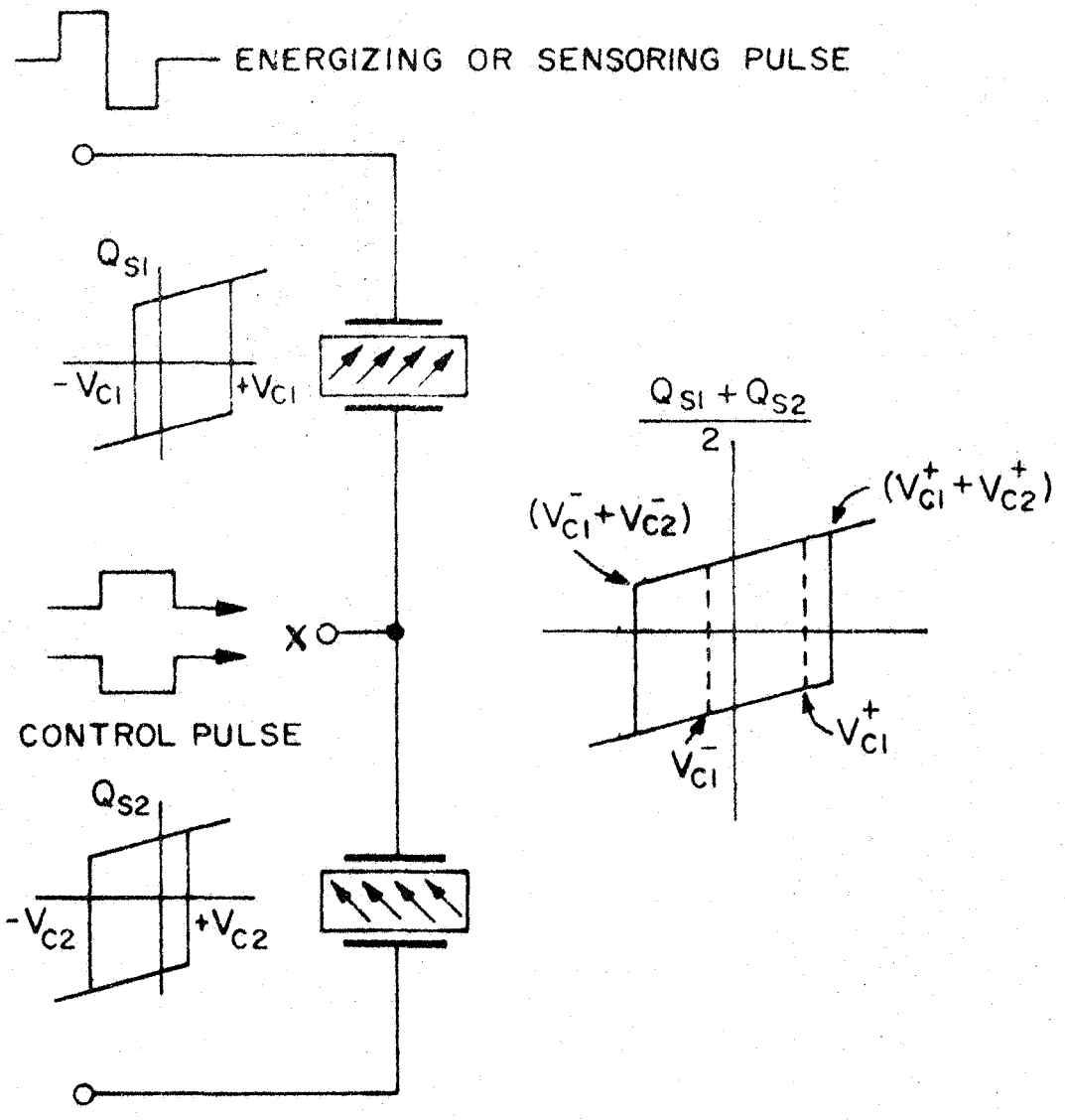


FIGURE 6: Transpolarizer Comprising Two Internally biased Crystal Sections

An important feature of the transpolarizer is that any level of unblocked polarization can be set, affording the storage of sampled analog signals also. FIGURE 7 is a photograph showing a family of hysteresis loops, each pertaining to a different setting, including the completely blocked and unblocked maximum settings. When a low polarization level is set, repetition rate can be increased up to a megacycle or higher. Since any appreciable hysteresis is sufficient for a transpolarizer action, it is apparent that very little power is required for control purposes. As an illustration, a transpolarizer using as a ferrielectric dielectric Mixed Bismuth Oxides of the type (MBO) with layered structure whose polarization is about $3. \times 10^{-6}$ coulomb/cm^2 with an area of $42 \times 10^{-4} cm^2$ and a coercive voltage of about 15 volts needs only about 4×10^{-8} watt-second, or less, for setting.

D. Recent Improvements

At the time this project started, the voltage level of these new transpolarizers was 35 volts for a two-section transpolarizer. Although these transpolarizers performed very well, their high switching voltage did not make the transpolarizer compatible with transistor technology. It should be remembered that a transpolarizer having a 35 volt switching voltage must be driven at least twice the coercive voltage which, in device terminology, means twice the switching voltage. For this reason,

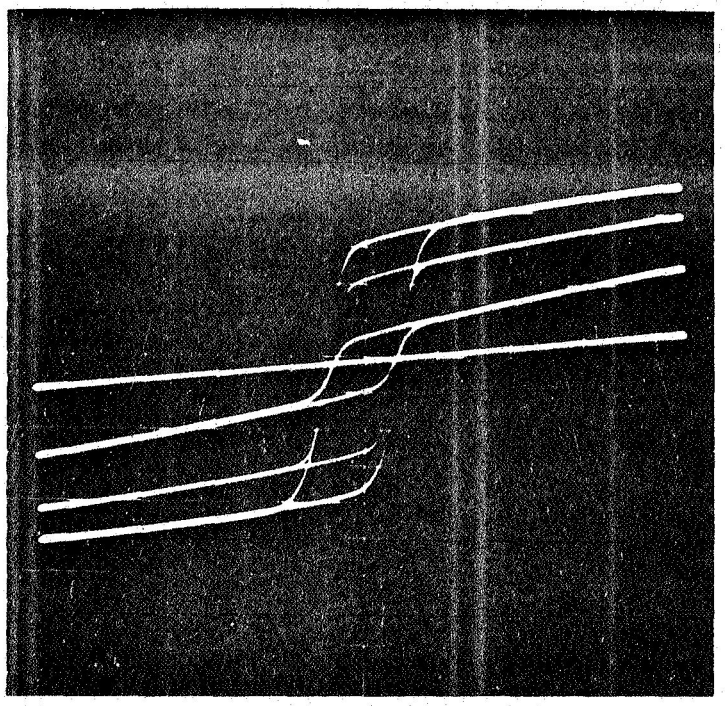


FIGURE 7: A Family of Hysteresis Loops

a driving voltage of 70 volts was required at these initial times. This and additional problems, necessitated a nearly one order of magnitude improvement over those electrical parameters which existed previously. In the following, those points are briefly listed on each of which a great deal of improvement was required.

(a) reduction of switching voltage to a least 10 volts

(b) crystal machining

(d) reduced conductivity of crystals

(e) electroding

(f) element fabrication

With reference to (a), it is noted that a number of factors are responsible for the switching voltage.

(1) crystal thickness

(2) crystal growth

(3) the amount of dope used during crystal growth

(4) electroding

The effect of these factors will be discussed separately. One of the most time consuming portions of this work was the preparation of uniform crystal thickness. Considering the coercivity (4.2KV/cm) of these crystals, a crystal thickness of one mil is required. To lap and polish a crystal to such a thin flake-like dimension requires an extremely high skill in the art. It took over one and one-half years of work to determine the condition under which this work can be properly accomplished.

Three lapping and polishing machines were required to process the crystals down to one mil thickness and obtain a flawless, clean, optically polished surface. Electric measurements clearly indicated that if the polishing was not perfect, the coercivity increased considerably. Five and one mil grit sizes were used for lapping purposes; while the final polish was obtained with a polishing cloth and a 0.05 grit size polishing component of zirconium which was received through the courtesy of the National Lead Company. The slurry viscosities, as well as circulation temperature, etc. were closely controlled.

In addition to the lapping and polishing problems, it was also important that the crystal surfaces be parallel. This was accomplished by letting the lapping blocks ride on three diamond pins which are set with the crystals, giving an interference pattern the topology of which was indicative of the quality of flatness.

The next most important factor in the reduction of the switching voltage was crystal growth itself. It was found that some crucibles and furnace configurations, as well as the thermal history of growth, have a considerable effect on the coercivity. The best crystal growth conditions for a given equipment and furnace topology must be determined. Essentially, the method described by Van Uitert (13) was used. In addition to the growth condition, a particular type of impurity addition also had a profound effect on descreasing the switching voltage. The effect of various dopants is described in detail in a final report (14).

The electroding procedure had an equally important effect on the switching voltage of the crystals. The best electrodes found so far were acid electrodes. However, these have not become practical. They were used extensively during laboratory measurements. ELECTRO-CRISTAL CORPORATION, Inc. has developed a special graded electroding process which utilizes a thin semiconductor layer between dielectric and metal electrodes and involves a diffusion process also. A patent was applied for this electrode and is described in more detail in a dissertation in partial fulfillment for a Doctoral Degree at Catholic University by Joseph Srour. It was found that the coercivity of elements electroded by this new process exhibited only one-half of the coercive voltage of those elements electroded by vacuum deposits or silver paste.

It should be noted that if the crystals were lapped and polished to a very thin dimension, the conductivity of these thin crystals storage elements increased and this effect is conflicting with the aims to achieve lower switching voltage by thin crystals. In order to improve on these conflicting effects, more work would be needed to improve on the doping procedure and employ higher purity materials for the crystal growth. These two aspects would require considerable additional work and could not have been accomplished within this contract period.

One mil thick crystals were prepared for the element fabrication, and we found that it was extremely difficult to cut these crystals to exactly uniform sizes. A number of methods were tested, such as, diamond wheel

cutting, ultrasonic cutting and scribing. It was found, however, that the only method which worked reliably was the airbrasive method. Using this method, the already electroded crystals were readily and easily cut to a fairly uniform size. A great deal of automation would be required to obtain higher precision and uniformity in production. This work could not be pursued further because there was no provision made for this type of work within the scope of this contract.

The element fabrication itself was done conventionally and was described earlier in a number of papers. However, it should be noted that the packaging and mounting required a very good insulation from the case of the header, and based on experience, it was found that an insulation between leads and header case of 10^{14} ohms was required. For this reason, headers were used which satisfy this requirement. The leads were gold plated, flat ribbons of 5 mil wide and based silver paste. This lead attachment was very reliable and never caused any serious difficulties. The headers were capped, using a Raytheon type welder. A header in which the crystals and lead attachments were mounted is shown in Photograph 4.

IV. TRANSPOLARIZER MATRIX

In general, a topological adaptive system requires three operations:

(1.) Modeling,

(2.) Evaluation,

(3.) Entailment (implication).

The modeling portion will involve the processing storage of distribution functions and the adjustment of these functions. The evaluation portion produces a "MATCH" or "MISMATCH" signal depending on a particular input signal. The entailment or implication operation would involve the normal output function and the resulting deductions that can be produced from the whole process.

A complete system utilizing an analog associative memory requires a lumped analog memory which employs TRANSPOLARIZERS* as the storage elements. Each storage unit may store as many as 16 to 48 multilevel samples.

During the first phase of Contract No. 12-136, ELECTROCRISTAL undertook the study of statistical switch concept which could be employed in learning adaptive control systems. As a result of these investigations, the need for an analog associative memory developed as one of the primary areas of interest. Basically, an analog associative memory permits one to compile and interrogate complex information by handling whole functions

in the computational process. The multilevel storage feature of the ELECTROCRISTAL storage memory allows the storing of more than two levels of information (conventional systems) at any one discrete memory point.

Although the advantages of an associative memory are well known to those who are actively seeking new data processing techniques, little or no work has been done on analog associative memories since no suitable device was available for the storage of an analog signal. Some of the more notable problems associated with such a memory may be listed as follows:

(1.) Multilevel storage.

(2.) An associative memory inherently requires the use of a non-destructive memory element.

(3.) The simultaneous switching of a large number of multilevel words or simple functions, even with extremely low power per storage element, would lead to a high switching power requirement.

(4.) The high power requirement is even more apparent if no modularity in switching is permitted.

(5.) Even if an excellent signal-to-noise ratio is obtainable from the storage element, it is apparent that a high degree of noise compensation is required in order to achieve successful operation.

(6.) The search for equality, proximity (within the decision region), and inequality requires a comparison of every stored word with the interrogating signal and if a large number of words is considered, the power requirement for producing the interrogating code provides a problem in itself.

(7.) It is also quite apparent that a simple matrix would require a complex flag, and with a more sophisticated matrix, the flag complexities could be reduced.

(8.) From all these considerations, it becomes evident that one is inherently led to the requirement of developing a storage element which performs some logical operations also.

(9.) In connection with the logic-storage element, it should also be noted that if high-speed switching is to be obtained, a high switching field must be applied. Since the "READ" and "WRITE" operation of an associative memory is not based on the usual coincidence process, it is possible to obtain higher switching fields in this case because higher switching field than twice the coercivity can be applied. It is known, however, that if a high switching field is used, the switching time decreases and the switching current increases. The problems then exist of limiting the switched current in order to keep the power requirement low, as required.

ELECTROCRISTAL can now make available storage elements with the following unique features:

(1.) A solid state crystal device can be produced having a small area and being capable of processing extremely low-level switching current transients (about one milli-ampere).

(2.) Non-destructive read-out.

(3.) Storage elements can perform certain logic-functions and thus combine the logic-storage capability into an associative memory.

(4.) The driving voltage can be as low as 30 to 40 volts.

(5.) The switching times of one element can be set between four and five microseconds, with the low driving voltages.

A number of matrix configurations were considered for the storage of analog signals. The analog associative discriminator described in Section II A and the analog-digital learning matrix described in Section III A have already exemplified ferroelectric analog storage matrices.

In this study other matrix configurations were also considered, and a detailed consideration was given to noise elimination techniques. ELECTROCRISTAL studied matrix noise cancellation methods, and new sensing techniques. As a radical departure from conventional memory matrices, a system was devised to permit every element to function both as a logic and as a memory cell. The double memory cells operate on the analog word line as "OR" gates, and as a result provide an excellent signal to noise ratio for equality matches.

In considering the various possible sensing techniques, it was determined that matches for "PROXIMITY" and "INEQUALITY" may be obtained by interrogating the entire logic matrix with a multilevel driving voltage code, representing a particular analog function. This technique essentially compares the output of each stored analog word with that of a particular compensating interrogating word. Such a matrix is shown in FIGURE 8. This matrix is essentially sort of a modified Steinbuch-Frank matrix including the elastic noise transient cancellation technique developed by ELECTROCRISTAL. A thorough investigation

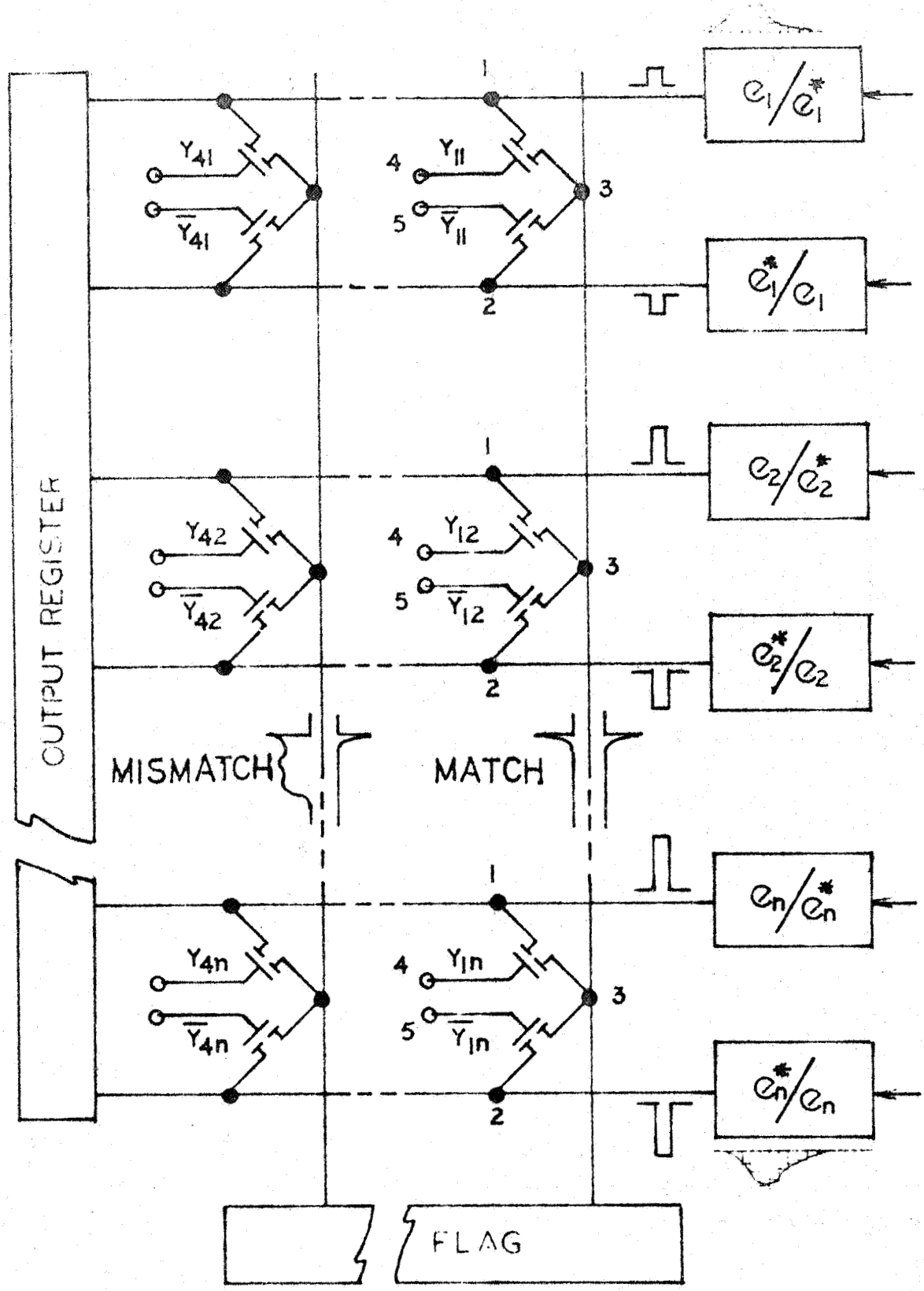


FIGURE 8: A Logic-Storage Type Learning Matrix

showed that if a single TRANSPOLARIZER* was used for each memory bit, similar to the learning matrix of Steinbuch and Frank, it would have been very difficult to solve some of the problems discussed earlier, and the flag would be excessively complex. In addition, in this case, the only method by which the response of the matrix could be detected is the correlation method, and as a result, for detecting a "MATCH ", only maximum indicators could be employed, which in a large matrix would not necessarily give a unique answer. Furthermore, the "MATCH" of each function would correspond to a different level and in the case of, let us say, a matrix containing 5,000 stored functions, most likely a large number of maximum levels may be identical, and an extremely fine level discriminating device would be required to discriminate the thousands of levels within a few volts. For this reason it is believed that the Steinbuch-Frank type matrix described earlier could only be useful for discriminating a small amount of multilevel words, and even then the level sensing accuracy must be extremely high.

To circumvent these difficulties, it was imperative to find a matrix solution which responds in case of a "MATCH" on the output of the appropriate multilevel word with a zero, or nearly zero output. Such a matrix solution would give a unique answer in the instance of a "MATCH" even if the memory matrix has a large number of stored functions. It was expected that such a matrix response could be obtained

only if one interlaces two identical matrices in such a manner that every memory bit consists of two elements, i.e., two TRANS-POLARIZERS* which are driven counter-clockwise during the sensing operation. As a consequence, one obtains an interlaced Wheatstone-bridge network in which the word lines with their loads in the flag, as shown in FIGURE 8, are the outputs between the bridge center of the twin memory elements and ground. FIGURE 8 also shows that by using a twin TRANSPOLARIZER* configuration, and particularly defined TRANSPOLARIZER* states, i.e., levels describing a function, it is possible with the counter-clockwise pulse drive to achieve a nearly complete cancellation of the output in the case of a "MATCH". Furthermore, it becomes evident that this type of matrix configuration, with its counter-clockwise pulse drive in the "READOUT" step, also has a cancellation effect on all stray capacitances and elastic transients.

Referring now to FIGURE 8, a small section of a matrix is shown. The twin TRANSPOLARIZERS* denoted by Y_{11} and $\overline{Y}_{11}$, etc., represent one storage element and also an "OR" gate. A function is stored in a set of TRANSPOLARIZERS* such as Y_{11}, Y_{12}, --- Y_{1n}. Other words are stored in the matrix elements having subscripts of 2, 3, ---K. In FIGURE 8, for simplicity, every column contains the matrix elements of a stored function, while the complementary matrix elements denoted by the Y's represent the elements of the interrogating matrix. The stored functions and the interrogating matrix are driven counter-clockwise as

indicated by e_i and e_i^* in the driver circuits shown in FIGURE 8. The interrogating or the complementary matrix is driven by the $e^{*'}s$, which represent the interrogating function, signified by a set of pulses having amplitudes which approach the function to be interrogated, while the property matrix, in which the property functions store the TRANSPOLARIZER* conductances (Y), is set to appropriate values in order that their conductance values approximate a property function. If the proper conductances and driver voltages are set and applied to the matrix, the interrogating matrix will present the interrogating function for comparison to every multilevel property function. Because the stored property matrix is simultaneously switched with the interrogating matrix, the output of that word line will become "ZERO", or nearly "ZERO", at which the stored properties "MATCH" with the interrogating matrix. This clearly shows that the twin elements of the matrix comprising a particular Y and Y represent an "OR" gate. There will always be an output, unless both of the twin TRANSPOLARIZERS* are simultaneously energized and contain the same signal, or simply when the interrogating signal and stored property signals match. The suggested sensing technique allows the flag to determine the following conditions:

(1.) An "EQUALITY" will be represented by no, or minimum, switching transients on the output line.

(2.) A "PROXIMITY" will be represented by the sum of a specified minimum number of switching transients on the output line closest to the matched level.

(3.) An "INEQUALITY" will be represented by a specified number of switching transients on the output line.

This noise cancellation technique was developed by ELECTROCRISTAL personnel and a signal-to-noise ratio for a single "MISMATCH" on the order of 80:1 was obtained. A load resistor of at least one kilohm, was chosen in order that a switching transient of 1 milliampere should produce at least an output signal of one volt. Such a system alleviates the necessity of any stringent requirements or tolerances to be placed on the "FLAG" circuitry.

It is noted that the interrogating matrix could be made of an evaporated resistance matrix, which would make this double-matrix system much less expensive. ELECTROCRISTAL CORPORATION is now in the process of developing a new adaptive element, which can be briefly denoted by the key words "ferrielectrically controlled resistors". These devices will be essentially electrically controlled resistors, the resistivity of which will be affected in a manner similar to the operational principles of the TRANSPOLARIZERS*.

A. Design Considerations of an Analog Memory

Before the design of an analog associative memory was undertaken, a number of questions had to be answered. These included:

(1) In what form will an analog signal be presented to the associative memory ?

(2) Will the analog signal presented be phase sensitive ?

(3) Will the interrogating signals have some deviation from the distribution functions stored in the analog associative memory ?

(4) If there should be a deviation from the stored discriminant function, what would be the nature of this deviation ? Is it a random deviation ? And, regardless of the nature of the deviation, what type of flexibility could be built into the associative memory so as to compensate for such a spread within the decision region ?

(5) Is the normalization of the input signal required ?

(6) How should the structure of the matrix be organized ?

(7) What type of sensing "FLAG" should be used to detect a response ?

(8) Should the interrogation of the memory matrix be parallel and/or sequential ? The word "parallel" used in this sense means that all analog stored words are simultaneously interrogated in a sequence, level by level.

It should be mentioned here that the representation of an electrical signal by composite distribution functions appears to have one distinct advantage, and that is that, generally, distribution functions are phase insensitive. As a consequence, the construction of an analog memory, represented by samples, is more feasible than if a phase sensitive system were needed. In addition, in most cases it may be possible to derive a synchronization signal from the input, which then could be synchronized with one of the flexible stored discriminant functions.

B. Experimental Model of the Analog Storage and Interrogating Matrix

A schematic diagram of the actually built experimental prototype matrix and interrogating matrix is shown in FIGURE 9 along with the

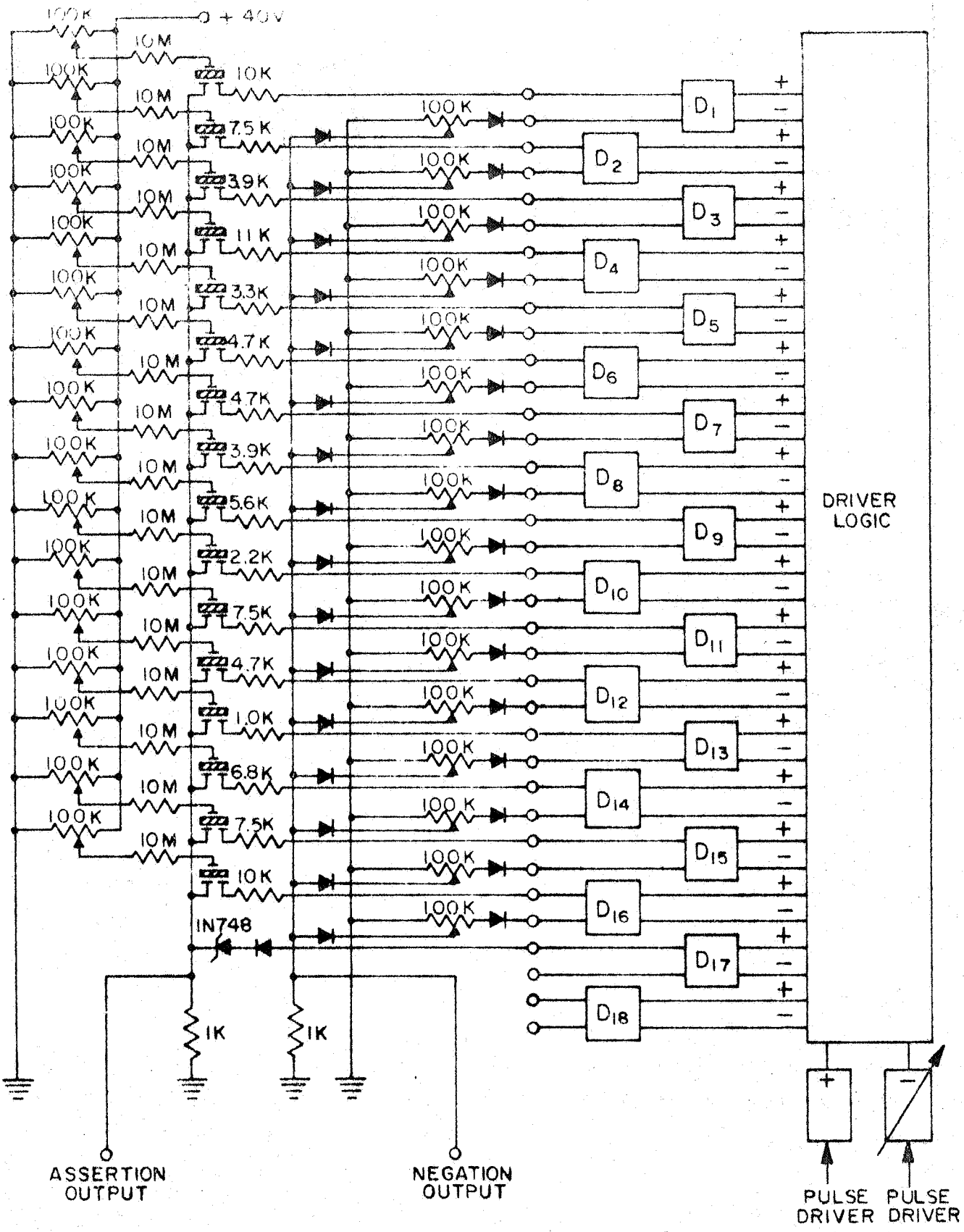


FIGURE 9: The Experimental Storage and Interrogation Matrix

driver logic section and the prototype matrix drivers D_2, D_4, --- D_{18}. Although the statement of work calls for the implementation of only four memory units, it was thought that in developing and testing the concept of an analog associative memory, a distribution function represented by 16 multilevel bits would be more adequate. For this reason, the prototype matrix consists of 16 TRANSPOLARIZERS*, each representing one bit of the analog word. The outputs from the prototype driver were resistively coupled to the TRANSPOLARIZERS*. The control points of the TRANSPOLARIZERS* were variably set through a 100 K potentiometer. The TRANSPOLARIZERS*, serving as analog storage elements, could be sequentially switched into the 1 K load due to the sequential pulses produced by the driver logic driven by the pulse drivers as indicated in FIGURE 9. The 17th sequential pulse from the prototype driver pulses was designated as the "RESET" pulse to the memory elements. This "RESET" pulse is coupled through a zener diode IN 748 to the common 1 K output of the analog memory elements. This "RESET" pulse serves to readjust the polarization of the TRANSPOLARIZERS* to the original state. The transients from the memory elements are in the order of 1 or 2 volts, while the "RESET" pulse has the magnitude of 40 volts. This large reset pulse provided a serious problem. This becomes more clearly evident later when the sampling is to be carried out. FIGURE 10, trace #1, pictorially displays the output from the prototype matrix. The transients along with the "RESET" pulse are clearly visible. The frequency

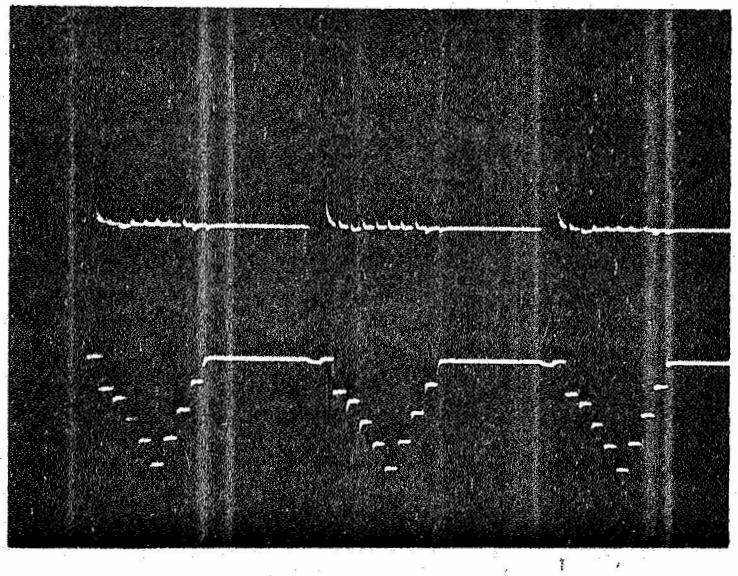


FIGURE 10: Output Signals from the Prototype and Interrogating Matrix

of operation is 60 KHz. The scale is 1 v/cm and the time 0.1 ms/cm.

The interrogating matrix is purely resistive. This amplifies the matrix functions. The interrogation driver pulses are coupled to 100 K potentiometers through a diode. The output of the potentiometers are coupled through a diode to a common load. The diodes at the input and the output provide isolation to the negation output. The interrogation matrix is shown schematically in FIGURE 9 with the interrogation logic and the pulse drivers which are driven in a similar way as the prototype section. FIGURE 10, trace #2, pictorially displays the variable output from the interrogation matrix. The frequency of operation is 60 KHz. The scale is 1 v/cm and the time is 0.1 ms/cm.

As previously stated, there is one 16-bit analog word represented by sixteen samples, and one 16-bit interrogating word, which can be compared with the stored word. The interrogating word is represented by sixteen small variable potentiometers, and permits the setting of any sort of analog function represented by sixteen samples. In order to produce a proper displacement of the analog samples on a scope, the ripple-counter operates the driver cards in such a manner, that after the sixteen samples have been switched, a seventeenth pulse is generated, which drives a "RESET" card. This resets the sixteen TRANSPOLARIZERS* and permits the re-cycling of a stored word indefinitely. The interrogating word, as stated before, produces the analog samples on a resistive network, the value of which can be varied. As a result, the samples appear as

pulses having different heights. Since these pulses follow in succession and each pulse has a constant height for the time-on, this arrangement permits the sampling of the interrogating pulses at any instant of time within a pulse, without affecting the height of the pulse. This is a very important advantage, since the transients from the switched TRANS-POLARIZERS* can now be sampled on any portion of the transients, preferably around the maximum current position. In this manner, it is possible to eliminate the need of a compensating matrix.

1. The Driver Logic

The prototype drive is initiated from one of the "Sync out" connections of the two pulse generators used, and is a +7v/spike sent directly to a minimum delay inverter. Since the flip-flops of the ripple-counter in the driver logic are triggered by negative pulses, the positive pulses of the generator were inverted. The trigger voltage of the ripple-counter is ~ -4v. It is important that the inverter be of the minimum delay type since it affects the synchronization of the prototype function with the interrogating function. The inverter is capacitively coupled to the prototype drive generator in order to reduce the switching time of the transistor used. The transistor is biased to a point just before saturation in order to increase the turn-on time, which is important in preventing delay. The $V_{ce(SAT)}$ of the transistor used is 1v to prevent noise, which in turn would trigger the prototype drive generator from triggering the inverter. The output from the inverter is then directly

coupled to an emitter-follower. Here again, the 2N 869 PNP transistor is used, thus keeping the saturation voltage at -lv. The emitter-follower is used strictly for impedance-matching purposes. The inverter and emitter-follower used are shown in FIGURE 11. It is important that the overall delay of the inverter and emitter-follower should be small. On FIGURE 12, trace #1 pictorially shows the "SYNC OUT" pulse from the prototype drive generator which is sent to the inverter. FIGURE 12, trace #2 shows the inverted "SYNC OUT" pulse which is used to trigger the prototype ripple-counter. The frequency of operation is 60 KHz. The magnification is 2, and the scale is 5v/cm. The time is 0.1 ms/cm.

The output from the inverter and emitter-follower is then used as a "CLOCK" pulse to drive nine RST flip-flops arranged to form a ripple-counter. The ripple-counter, having been previously set through terminals "r" (see Fig. 13), begins operation as the first "CLOCK" pulse arrives. The "CLOCK" pulse is provided simultaneously to all flip-flops on terminal 18 (see Fig. 15). The "1" state of the first flip-flop is sent directly to the "S" terminal of the second, and so on down through each until the ninth flip-flop is reached and here it is fed-back to the first, and an iterative operation is in process. The "O" state of the first flip-flop is sent directly to the reset or "R" terminal of the second and this continues and is again fed-back from the last to the first. FIGURE 13 shows the schematic of the RST flip-flops used. Note that the flip-flop can be reset at any time through terminal "r". Here a 2N706A transistor is used to discharge the "1" state to ground.

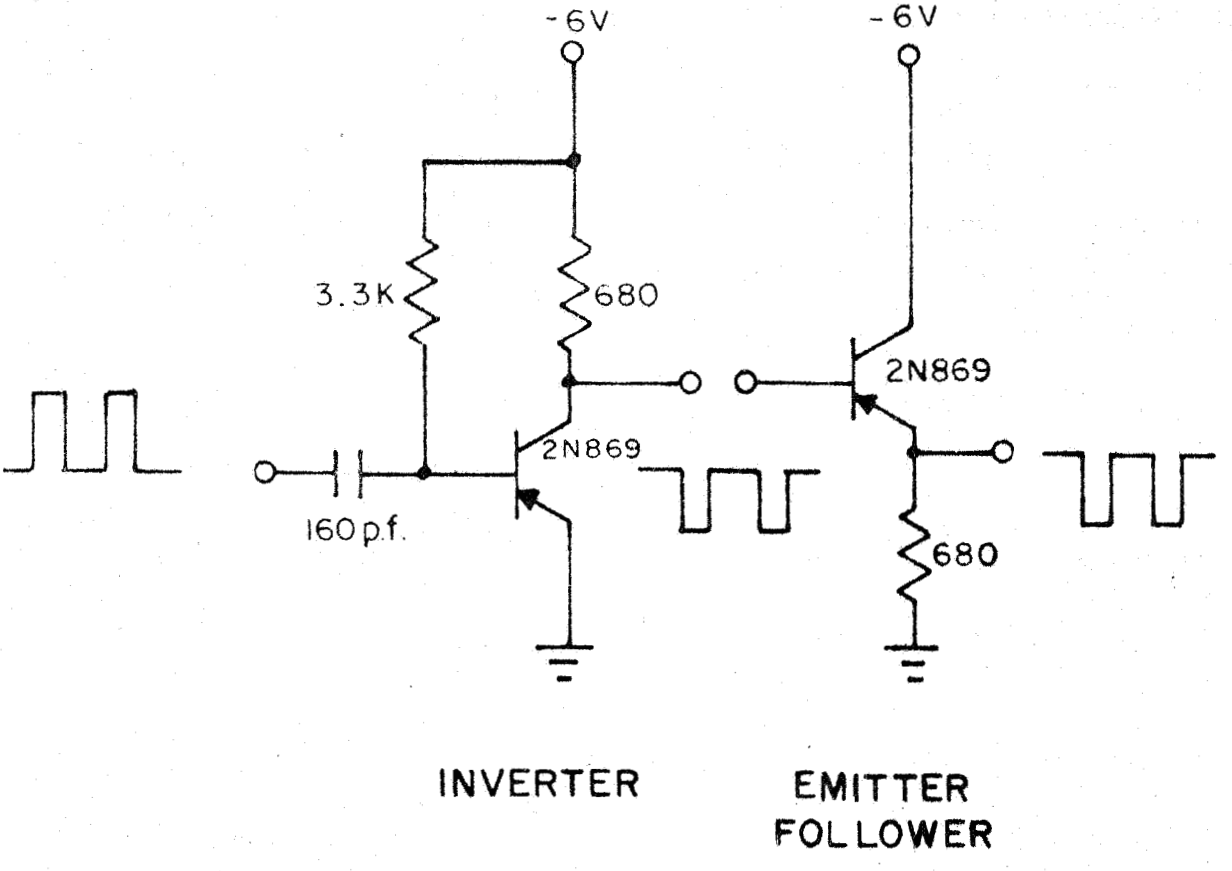


FIGURE 11: Inverter and Emitter Follower used for Matching the Pulse Driver and Driver Logic

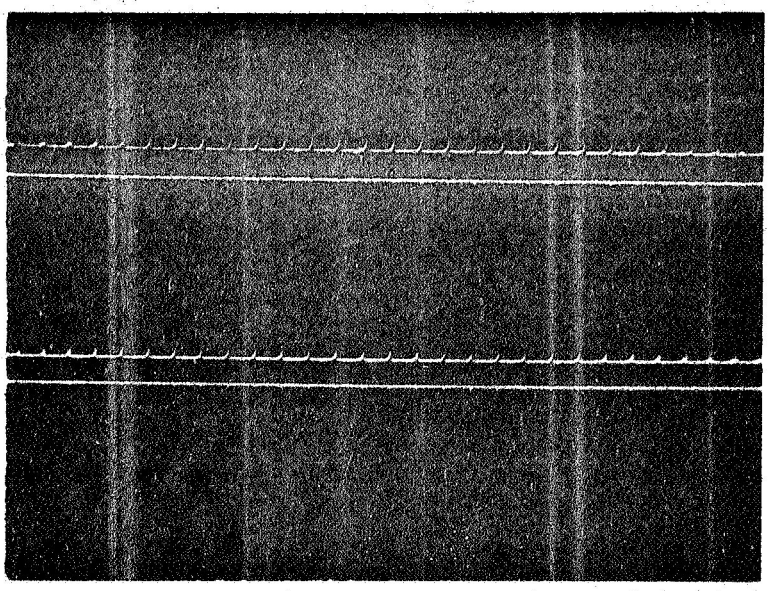


FIGURE 12: Various Driving Pulses of the Clock Generator

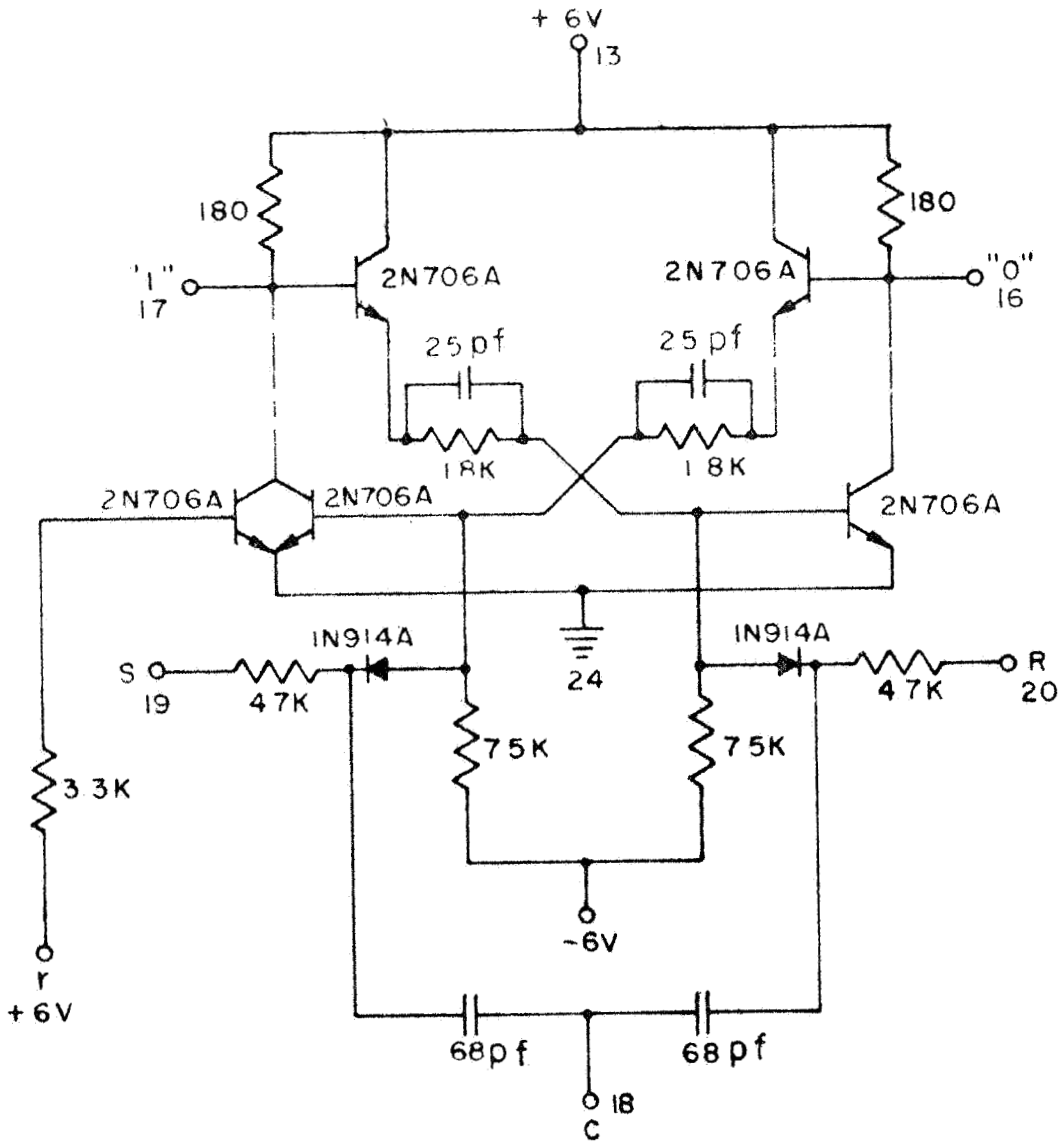


FIGURE 13: RST Flip-Flop

This method of resetting the ripple-counter has proven very effective. From the prototype ripple-counter , the outputs are then sent to 18 "AND" gates where a sequential logic operation is performed, and 18 sequential pulses are developed. The "AND" gate consists of diode-transistor logic and is shown schematically in FIGURE 14. The block diagram of the prototype driver logic is shown in FIGURE 15. The output waveforms of the ripple-counter and the "AND" gates are shown in FIGURE 16. FIGURE 17, traces #1, #2, #3, #4, shows 4 of the 18 sequential pulses, which are generated from the ripple-counter and the "AND" gates, to be used in the prototype drive. The frequency of operation is 60 KHz. The magnification is 2, and the scale is 5 v/cm. The time is 0.1 ms/cm.

The interrogation drive is initiated from the other of the two pulse generators used. It functions similar to the manner in which the prototype drive was generated. That is, the "SYNC OUT" pulse from the interrogation pulse generator is sent to the inverter and emitter-follower. This is the same as that shown in FIGURE 11. FIGURE 12, traces #3, and #4 , shows the "SYNC OUT" pulse from the interrogation drive generator and the inversion which has been carried out. The frequency of operation is 60 KHz. The magnification is 2, and the scale is 5 v/cm. The time is 0.1 ms/cm.

The output from the inverter and emitter-follower is likewise used as a "CLOCK" pulse to drive the nine RST flip-flops in the interrogation

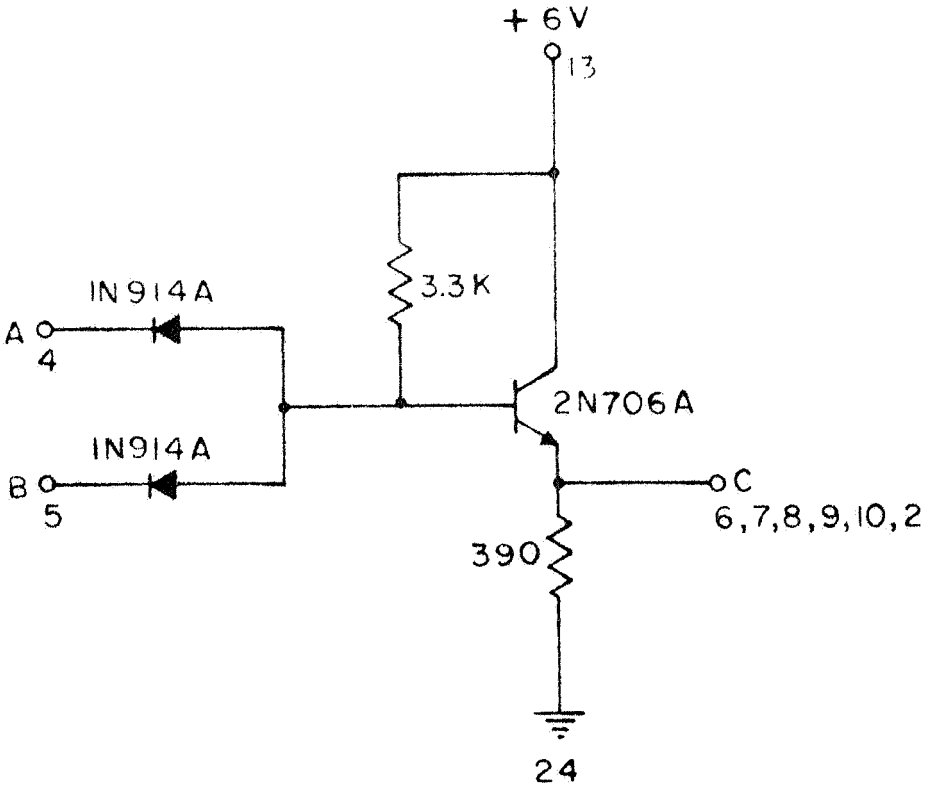


FIGURE 14 "AND" GATE

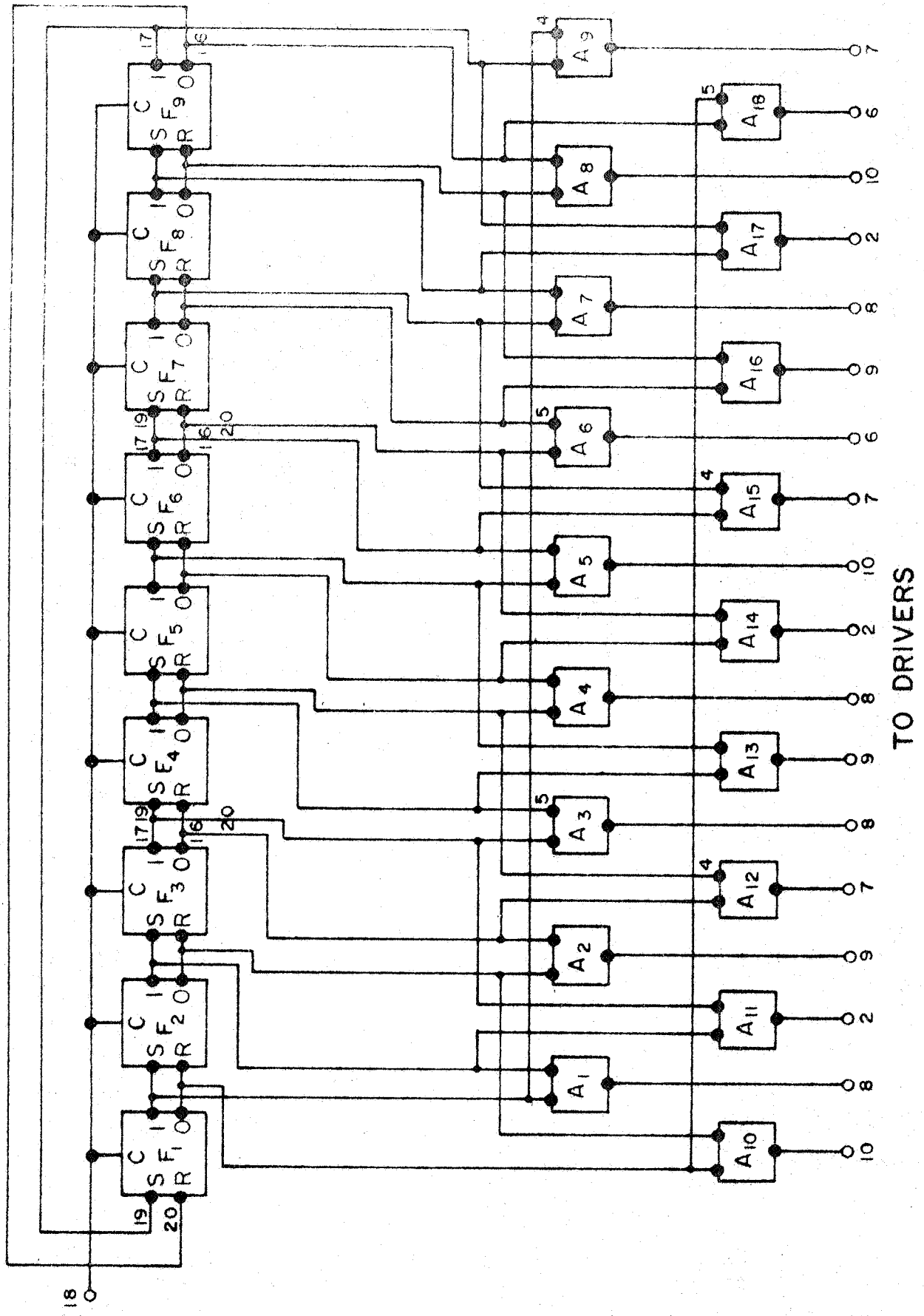


FIGURE 15: Driver Logic

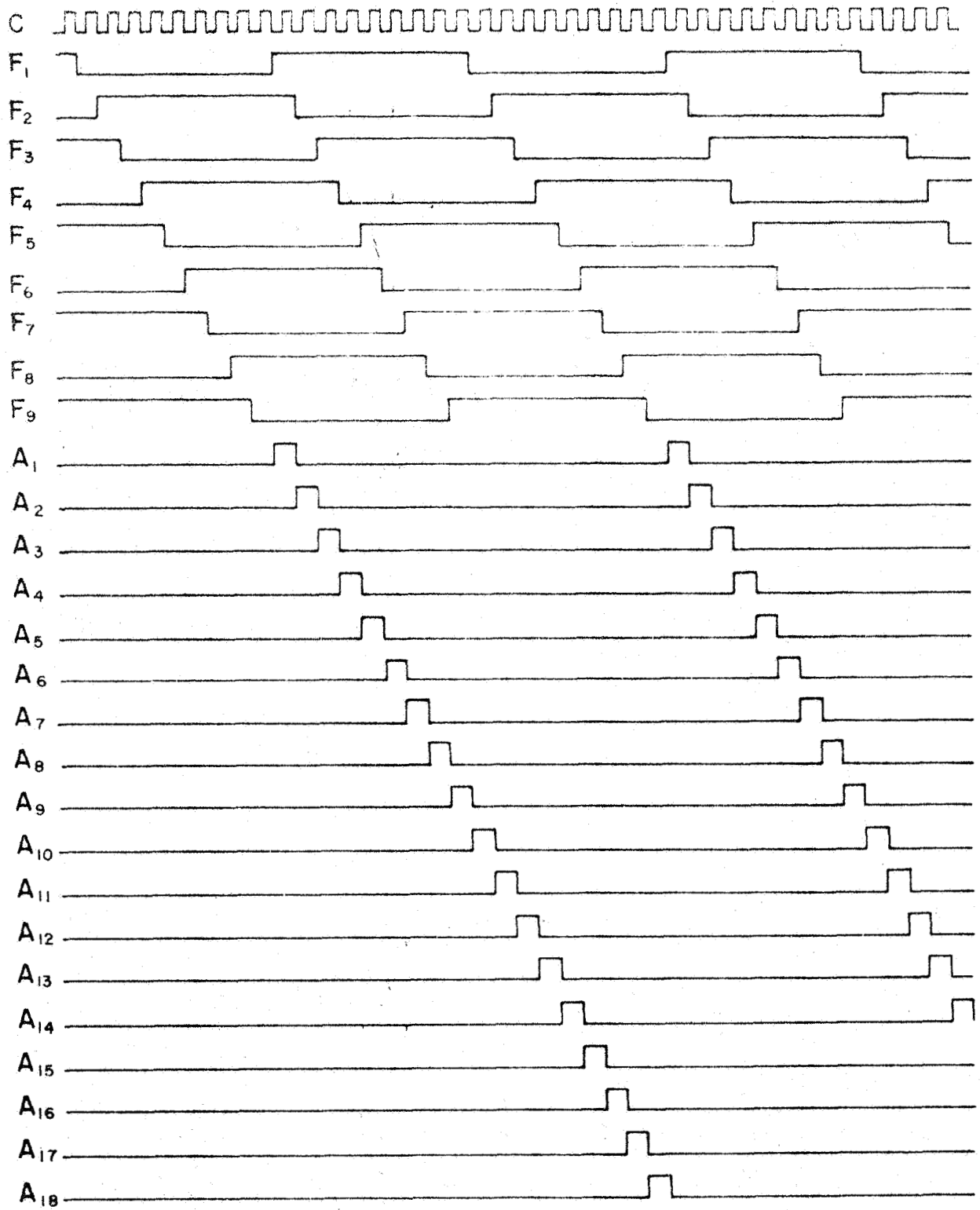


FIGURE 16: Input -Output Waveforms of the Driver Logic

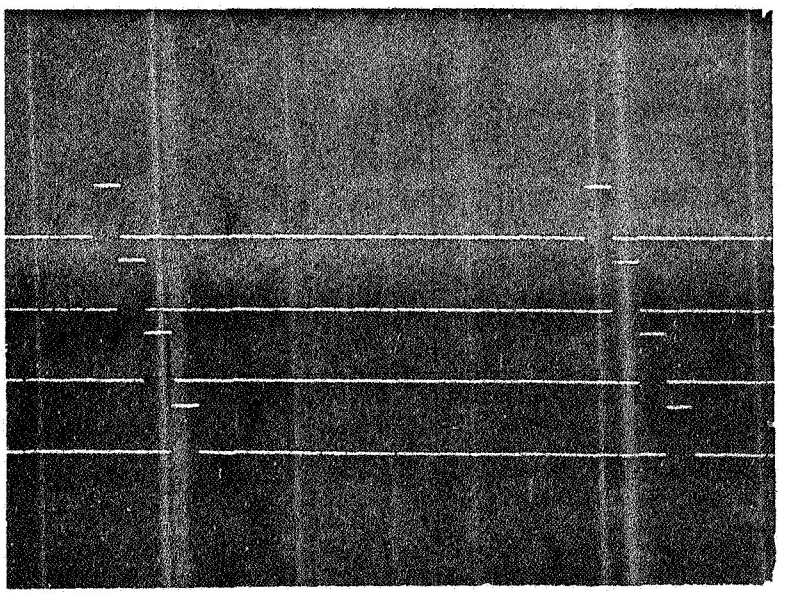


FIGURE 17. Pulse Outputs from the Driver Cards to the Prototype Function

ripple-counter. The operation of the ripple-counter is similar to that used in the prototype drive. Again, the outputs of the flip-flops are gated and 18 sequential pulses are generated for the interrogation drive. The flip-flops and "AND" gates used are those shown previously in FIGURES 13 and 14. The block diagram of the interrogation driver logic is the same as that shown in FIGURE 16. FIGURE 18, traces #1, #2, #3, and #4, show four of the eighteen sequential pulses which are generated from the ripple-counter and the "AND" gates to be used in the interrogation drive. The frequency of operation is 60 KHz.. The magnification is 2, and the scale is 5 v/cm. The time is 0.1 ms/cm. The eighteen sequentail pulses having been generated from the prototype logic are now sent directly to the driver cards D_1, D_3, ---D_{17} (see Fig. 9).

2. The Driver Cards

Each driver card contains four pulse drivers, two positive and two negative, which can be combined into two switching pulse pairs, each pair comprising a plus and a minus pulse. The repetition rate of the generated pulses can be continously varied from DC to 2 MHz with negligible effect on the rise and fall times. This high frequency was built in the first experimental model in order to have a sufficient universal system for further expansion. The circuit diagram of the switching pulse driver (D) is given in FIGURE 19. The outputs can be loaded down to a small output impedance without damaging the driver.

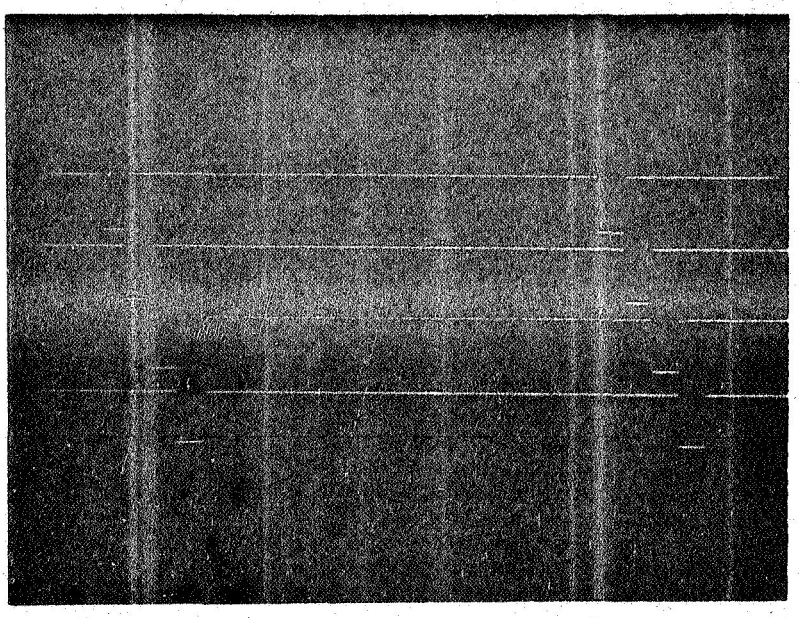


FIGURE 18: Pulse Outputs from the Driver Cards to the Interrogating Function

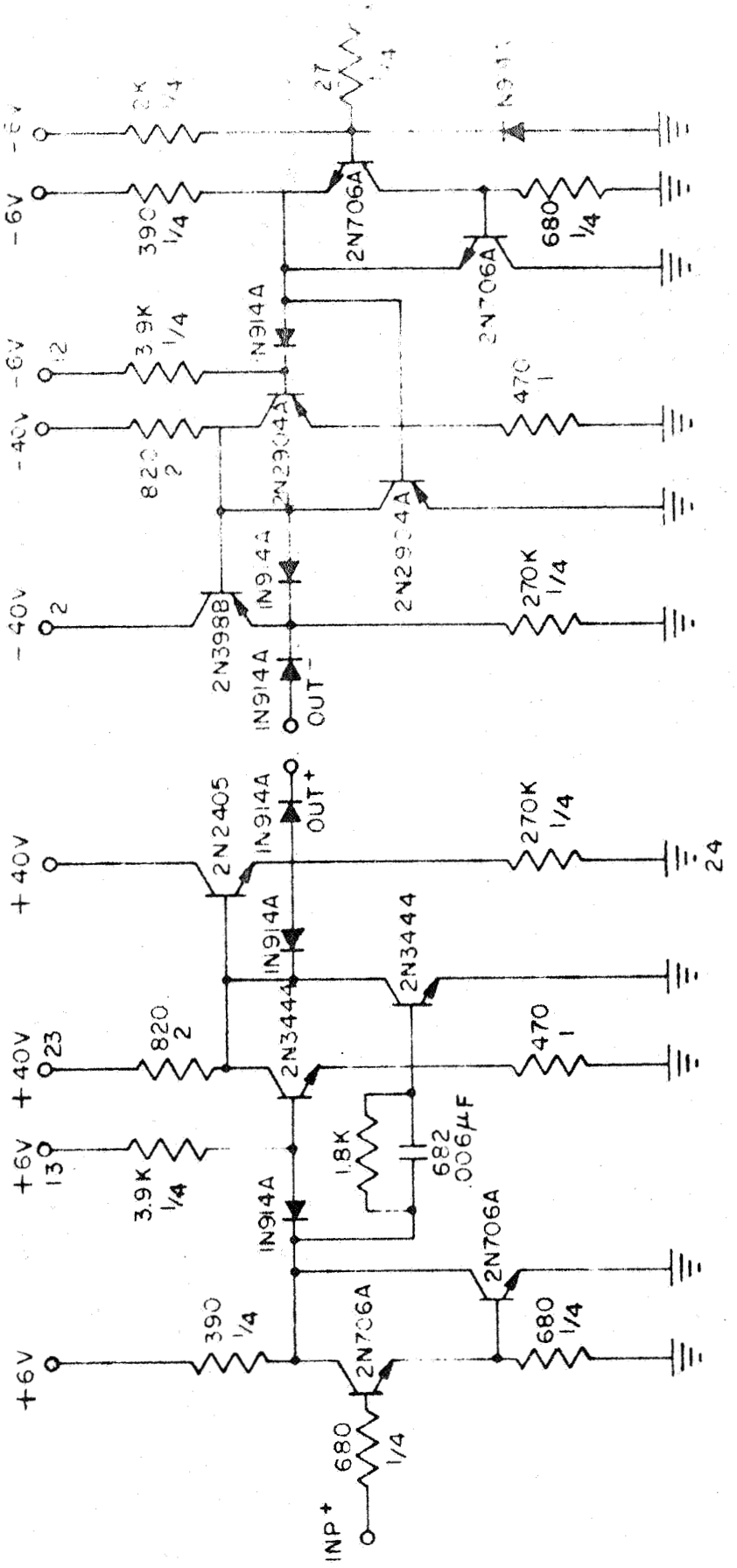


FIGURE 19: The Driver Card

Each sequential pulse from the prototype logic enters a separate driver. The trigger voltage of the driver is 1.5v minimum. Again, this allows for a good noise rejection ratio. The assertion pulse of the driver is triggered and the new prototype driver pulse becomes a -40v pulse. Through this sequential pulse pattern, 18 assertion drivers are used to generate the drive to be used in the prototype matrix. The schematic of the driver is shown in FIGURE 19, which shows both the assertion and the negation drivers. FIGURE 17 pictorially displays 4 of the 18 sequential prototype driver pulses. The prototype matrix will use 16 of the sequential pulses as a drive, one for resetting the matrix, and one for a synchronization pulse, after which a recycling process will begin. The frequency of operation shown in FIGURE 17 is 60 KHz. The magnification is 2, and the scale is 50 v/cm. The time is 0.1 ms/cm.

In a similar manner, the 18 sequential pulses from the interrogation logic are sent directly to the negation section of the driver. Here again, 18 negation drivers are used. Each of the interrogation driver pulses is generated. The negation driver is shown schematically in FIGURE 19 . FIGURE 18 shows pictorially 4 of the 18 sequential interrogating driver pulses used to drive the interrogation matrix. The frequency of operation is 60 KHz. The magnification is 2, and the scale is 50 v/cm. The time is 0.1 ms/cm. The interrogation matrix uses 16 of these sequential pulses, while one is used for gating purposes later in the development, and one is used for a synchronization pulse, after which a recycling process begins.

3. The Flag

With reference to FIGURE 9, the learning matrix has two outputs: an assertion output, which presents the prototype function, and a negation output, which presents the interrogation function. These two outputs are fed in the flag for further processing purposes. A number of different flags could be developed depending on what type of recognition process is to be adopted. In the following, a few flag types are mentioned:

(a) Comparator or Correlator type.

(b) A flag processing the product of the prototype and interrogation functions utilizing a minimum or maximum switch which could work within the limits of the decision region and thereby perform a simple minimum distance recognition.

(c) A flag processing the quadratic product of the prototype and interrogation function which would lead then to a minimum distance decision.

(d) A flag which, besides the various decision responses, could produce any desired type of error function which could be used for training in the TRANSPOLARIZER* matrix prototype functions directly from the sensed signal of the environment or use the same error functions for adjusting already existing prototype functions.

Since this was the first time that an analog associative memory was developed, a type of flag was chosen which was essentially a comparator or correlator type and which would be suitable for producing an error function which could then be used for training-in prototype functions using signals from the environment only, or utilizing this error function for the re-adjustment of already existing prototype functions.

4. The Experimental Flag

FIGURE 20 is a block diagram of the experimental flag actually built. As stated before, this flag was a comparator type of flag, mentioned under (a) in the previous paragraph. The reader is reminded that although the matrix shown in FIGURE 9 presents a one word matrix only, matrices comprising a number of such words corresponding to various requirements are envisioned. Each word comprises a different prototype function, while the interrogation function is simultaneously presented to all prototype words. Each word has a processing flag of one of the types mentioned. In this work, only a matrix comprising one prototype function and interrogation function was constructed. For this reason, only one flag of the type mentioned was built. Every flag on the outputs of the various prototype is, in principle, identical. However, they could be also of any of the types mentioned, or groups of the different types of flags which could also be employed throughout the matrix (12). Both the prototype or assertion outputs as well as the interrogating or negation outputs are essentially fed into a comparator through two operational amplifiers as shown in FIGURE 20.

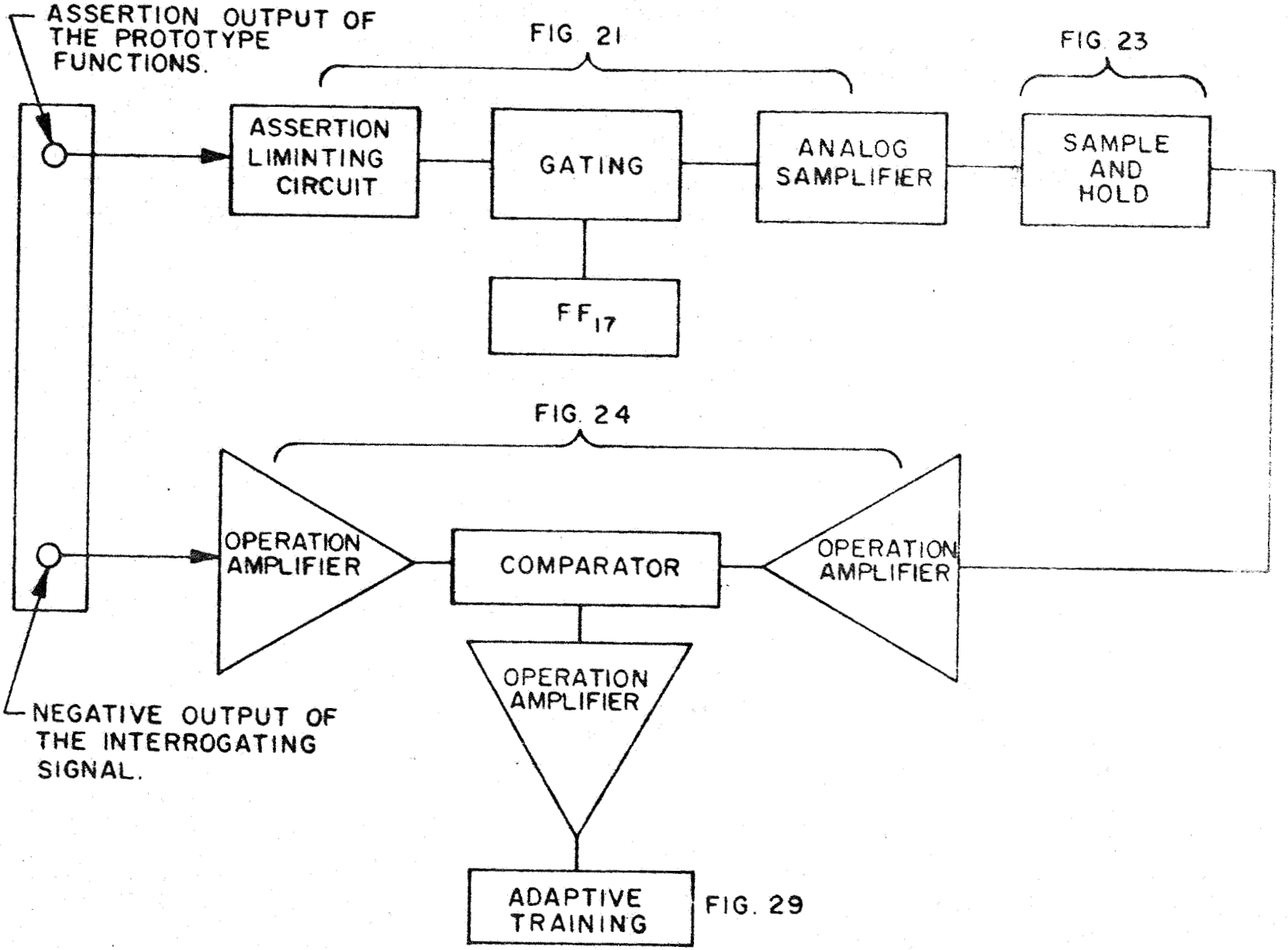


FIGURE 20: The Experimental Flag

THE FLAG OF THE ANALOG ASSOCIATIVE MEMORY.

The output of the comparator is the signal which can be utilized for various purposes such as switching a gate, or for adaptive training, etc. This comparator is described in more detail in connection with FIGURE 24. As shown in FIGURE 21, the assertion output signals require a preprocessing for a number of reasons as follows:

(a) The 40v reset generated by driver D_{17} which resets the TRANSPOLARIZER* into their initial state, requires the application of a limiting circuit.

(b) Since the limiting circuit still leaves a fairly strong portion of the reset pulse in the prototype function, this needed to be gated out for which purposes a gate and a pulse derived from flip-flop 17 is used. Thereafter, an amplitude normalization is inserted using an analog amplifier. The limiting, gating and analog amplifier circuitries are described in detail in FIGURE 21.

Since the so obtained prototype function consists of the sequential appearance of ferroelectric switching transients, these switching transients are sampled around the vicinity of the maximum value of the switching transients. As a result, every TRANSPOLARIZER* amplitude is now represented by the narrow sample of the switching transient. A sample and hold circuitry is then employed to obtain a comparable signal with the interrogating signals. The sample and hold circuitry is discussed in FIGURE 23. Finally, the differential signal, or error signal produced by the comparator, is again amplified in an operational amplifier and in our particular case, it is fed in the adaptive training circuitry described in FIGURE 29.

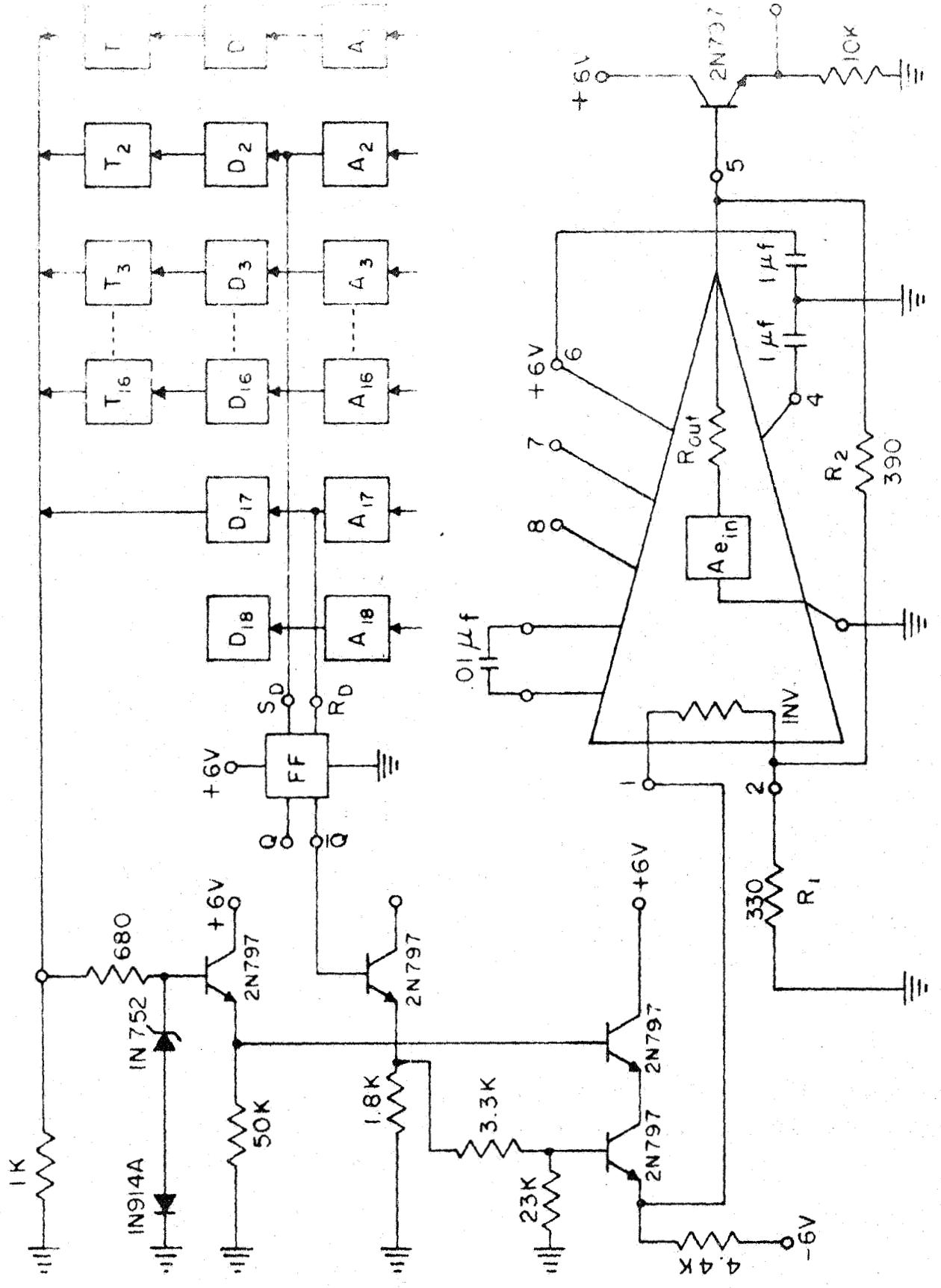


FIGURE 21: Limiting, Gating and Amplifying Circuitry

5. Limiting, Gating, and Amplifier Circuitry

Before the sampling circuit design could be carried out, one problem became evident. This problem stemmed from the fact that the sampling of pulses in the magnitude of 2 volts from the prototype matrix required the sampling to be very sensitive in the range between 0 and 2 volts. However, on the sample output where the transients appear, a 40 volt pulse is also present. This pulse is used as the "RESET" pulse for the analog memory elements. Here it becomes obvious that it is impossible to design a sampling circuit which is ultra-sensitive between 0 and 2 volts and which is concurrently able to process a 40 volt "RESET" pulse. A solution to this problem can only be accomplished by either minimizing the "RESET" pulse or, alternatively, eliminating it at some point in the circuit at which the resetting of the prototype matrix would not be affected. The ideal situation would be to eliminate the "RESET" pulse completely from the prototype matrix output, and this was accomplished by a process of gating the prototype function.

The output from the prototype function line was resistively coupled into a Zener-limiter (see Fig. 21). The transients, being of magnitudes between 0 and 2 volts, were not affected, but the 40 volt "RESET" pulse was limited to a value of 5.6 volts by the Zener diode. Afterwards, the Zener limiter was followed by an emitter-follower, which serves as a "FAIL-SAFE" device. The reasoning behind this is that if something should happen to the Zener limiter and it no longer functions as it should, the transistor of the

emitter-follower will "BURN OUT" preventing further damage in the "FLAG" section. This is important since this is where the most expensive circuitry is located.

For the purpose of creating a "GATE" pulse at the exact time when the "RESET" pulse is present, an IC RST flip-flop is used. The output of the seventeenth "AND" gate is sent to the direct set "S_D" of the flip-flop. This provides a "1" on the output line. This process provides a "GATE" pulse for the first 16 sequential prototype driver pulses, but is absent for the last 2 sequential pulses. This "GATE" pulse is then sent to an emitter follower, after which it proceeds onto the base of one of the transistors of the double transistor "AND" gate, as shown in FIGURE 21. The signal from the Zener-limiter where the "RESET" pulse has been limited to 5.6 volts is sent to the base of the other transistor in the "AND" gate. Since the gate is only conducting during the period of the first 16 sequential pulses from the prototype logic section, the "RESET" pulse is removed from the output line of the prototype function, and a complete elimination has been achieved. It is important that a transistor with a high speed and a low $V_{ce(SAT)}$ be used, since the outputs of the prototype function are of small amplitude. FIGURE 21 schematically shows the Zener-limiter, the origin of the "GATE" pulse, and the double transistor "AND" gate. In FIGURE 21, trace #1 pictorially displays the "GATE" pulse from the IC RST flip-flop. Trace #2 displays the "GATE" pulse as it enters the double transistor "AND" gate. Trace #3 displays the output from

the double transistor "AND" gate, whereby it can be seen that the 40 volt "RESET" pulse is almost entirely eliminated from the prototype function. The frequency of operation is 60 KHz. The scale on trace s #1 and #2 is 5v/cm and the time is 0.1 ms/cm.

As mentioned earlier, the minimization and complete elimination of the "RESET" pulse from the signals of the prototype function having been accomplished, the final result was that the signals from the prototype matrix were now too small in amplitude for sampling. Therefore a linear amplification was needed. This amplification was performed through the use of a Motorola MC 1530 high performance integrated operational amplifier. Some of the advantages provided by this operational amplifier were low offset voltages and currents, small size and reduced spacing, increased reliability, and excellent temperature tracking. Another and probably the most important feature of this IC operational amplifier was that an internal pin connection permitted the shaping of the open loop response. The noise rejection ratio was excellent.

The prototype signal from which the "RESET" pulse was eliminated is now fed directly into the operational amplifier. The input offset voltage is between 1 and 5 millivolts, which provides excellent triggering for the prototype function. The gain of the amplifier was determined by the ratio of the feedback resistance to the ground-leak resistance and was set to provide a gain of 2, thus making it possible for each discrete bit of the analog word to vary between 0 and 4 volts. The bandwidth provided no limitation, in that it was possible to operate in the video range at 2 MHz.

The output impedance was 25 ohms, providing a good prototype function to be sampled. The differential input signal was limited to ± 5 volts. The DC bias was capacitively stabilized and operation was set between + 6 and − 6 volts. This eliminated the need for new power supplies or limiting circuitry. The operational amplifier was lag-compensated through the use of oscillation information provided by Bode, Nyquist, and Pole-Zero plots. The operational amplifier was then followed by an emitter-follower for the purpose of impedance matching and isolation. It is to be noted here that this emitter-follower eliminated most of the noise and overshoots which passed through the operational amplifier because most of the undesired noise and overshoots were negative, and consequently did not trigger the positively biased emitter-follower. It is of importance that the transistor used here be of a very high speed type, and have a very low $V_{ce(SAT)}$. The prototype signal from this operational amplifier is now the signal which is to be sampled. The schematic diagram of the operational amplifier is shown in FIGURE 21. FIGURE 22, trace #4 displays the prototype function, having been amplified, and the "RESET" pulse completely removed. The frequency of operation is 60 KHz. The scale is 2 v/cm and the time is 0.1 ms/cm.

6. Sample and Hold Circuitry

The next step was to develop a sampling circuit for the 16-bit stored analog word, which would be a better representation of the prototype function.

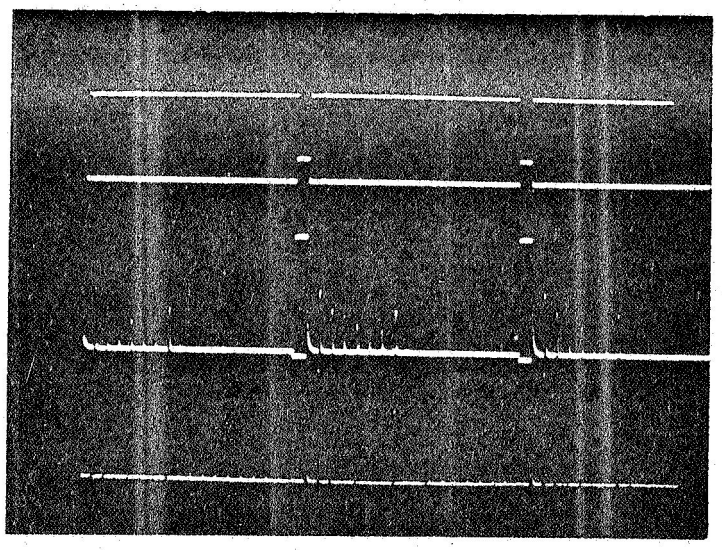


FIGURE 22: Oscillograms Showing the Ellimination Steps of the 40 V Resetting Pulse

It became evident that there is a basic difference between sampling binary signals and analog signals. In the case of binary signals, it is possible to shape the pulse by using clipping diodes, or another flip-flop , and consequently it becomes relatively easy to eliminate any undesired overshoots, transients, and other such unwanted phenomena. However, this is not possible with a sampled analog signal, and for this reason, it was imperative to design a sampling circuit which produces relatively clean samples. At a later time, the samples representing the analog functions, may be integrated into a continous function, and this will aid in the smoothing-out of small residual overshoots.

The sample-hold circuit was designed to sample the prototype matrix and then to hold this sample until the next sample was presented. Most of the sample-hold circuits which were studied are quite complex, while others were overly simpled. One of the problems which we encountered with most of these circuits was that the hold-capacitor was capable of charging and discharging simultaneously. To overcome this problem, a resistor was placed in one of the loops to limit the discharge current. This, however, created a new problem, namely, that the speed with which the output responded to the new input levels was substantially reduced. This is especially true if the sampling time is short.

The schematic diagram of the sample-hold circuit is shown in FIGURE 23. This circuit does not have the limitation mentioned above because charge and discharge do not occur simultaneously, and thus there

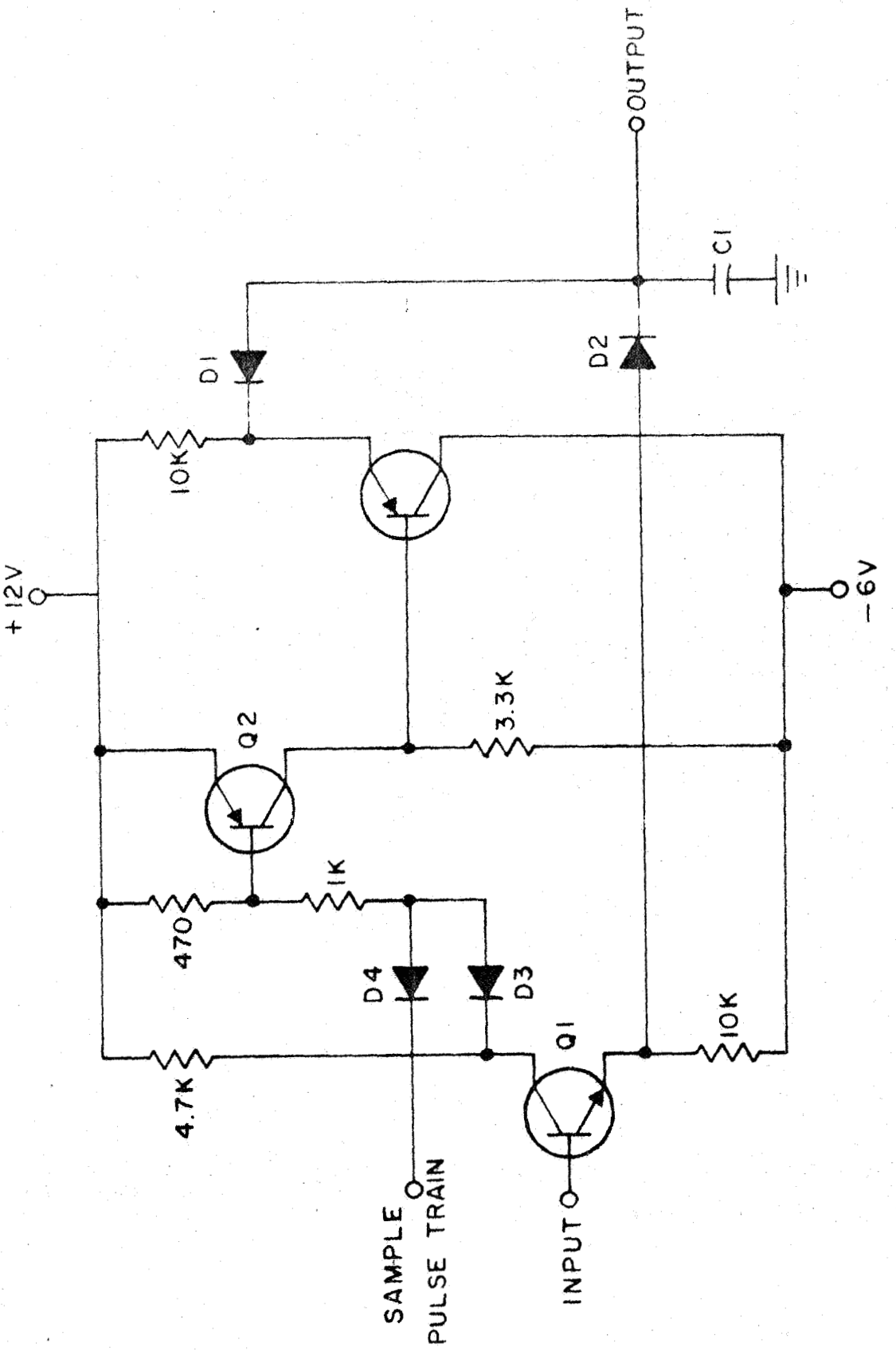


FIGURE 23: Sample and Hold Circuitry

is no need for a current-limiting resistor. The circuit has two inputs: the signal from the prototype matrix whose amplitude is being sampled, and a positive sampling pulse train. The sampling operation of the circuit calls for the sampling pulse train to be at ground potential between sampling pulses, which in turn holds Q_2 in saturation. The collector voltage of Q_2 approaches +12v, which then turn off Q_3, causing its emitter to also be at a potential of 12v. This has the effect of back-biasing diode D_1 which then does not permit the holding capacitor C_1 to discharge between pulses. At exactly this point, Q_1 is also shut down causing its emitter to be a -6v. This causes D_2 likewise to be back-biased, thus preventing any charging of the hold-capacitor between pulses. During the sampling process, if the new signal is more positive then the previous signal, the hold-capacitor C_1 charges through emitter-follower Q_1 and low leakage diode D_2. Due to this charging of C_1, the collector voltage of Q_1 drops below +12v. This voltage drop through D_3 drives Q_2 into saturation, cuts off Q_3, and back-biases D_1, and the process is again repeated as explained earlier. If the new input signal is less than the previous one, Q_1 remains cut off as does Q_2, but emitter-follower Q_3 becomes higher conductive providing a very low impedance path for C_1 to discharge through D_1. The hold-capacitor C_1 continues to discharge until it reaches the amplitude of the new input pulse less the diode drops in Q_1 and D_2. At this particular point Q_1 again turns on, stopping the discharge of C_1, and the process again repeats itself. The time required to hold the sampled pulse is dependent upon the value of the hold-capacitor. The larger

the value of C1, the larger will be the value of the rise and fall times of the sampling pulse which is being held.

7. The Comparator

Since most of the comparators on the market today have a digital output, the design of an analog comparator was necessary. Efforts were directed into designing an analog comparator with medium gain, large bandwidth, small input offset current and voltage requirements, and a low input impedance. Fundamentally, the Wheatstone Bridge appears to be the simplest device for the implementation of an analog comparator. One of the first models designed made use of high speed switching transistors. But the preliminary work revealed some problems, one of which was that by using transistors, the $V_{ce}(SAT)$ was 200 mv at best, which is a rather high value, if small signals are to be precisely compared. This would mean a loss of 5 % in the error signal to be used in the adaptive training process. Another problem was the voltage drop across the transistor junctions, which could cause a further loss in the ability of the error signal to readjust the prototype matrix. And finally, due to the high output impedance of the discrete component transistor comparator, the bridge resistance would be rather high.

To eliminate these problems, operational amplifiers instead of transistors were used (see Figs. 20 and 24). The signal from the prototype matrix, having passed through the gating circuit and the samplehold circuit, is now sent directly into a Motorola MC 1530 IC operational amplifier of the

same type as used previously in the gating circuit. The input impedance was kept rather high, in order that the operational amplifier might sense minute input signals and amplify them for the correlation process. Through the use of Bode, Nyquist, and Pole Zero plots, the operational amplifier was lag-compensated to retain it from the region of oscillation. The gain was set to give the maximum output voltage swing. The power supply voltages were capacitively decoupled through the use of small non-polarized capacitors.

Likewise, the interrogation matrix signals from the resistive network were sent directly into another operational amplifier. The input impedance of the operational amplifiers was matched. Similarly, the power supply voltages were capacitively decoupled, the amplifier was lag-compensated, and the gain of the operational amplifier was set to give the maximum output voltage swing possible. Since the output impedance of the operational amplifiers was in the order of 25 ohms, it was then these two impedances that were used to serve as half of the Wheatstone Bridge. This half of the bridge remained fixed, while the other half consisted of two small variable potentiometers, used in this instance to establish the "ZERO" level between the two matrices. The bridge was then calibrated to give a "ZERO" output when an exact "MATCH" existed between the prototype and interrogation matrices. The bridge was then followed by a third operational amplifier, in order that isolation of the two signals could be obtained. It also served as an amplifier for the generated error signal, which is to be used in the adaptive training process. Again, the power supply voltages were capacitively

decoupled, the amplifier was lag-compensated to prevent oscillation, the input impedance was kept high for greater sensitivity, and the gain was set to provide maximum output voltage swing in either direction, due to the fact that the error signal may be positive, zero, or negative.

This analog comparator has been fully analyzed and exhibited the following characteristics. The input offset current I_{io} can be varied between 0.2 and 2 ma, thus providing a very high sensitivity for the comparator. The input offset voltage $/V_{io}/$ can vary from 1 to 5 mv. The input common mode voltage swing V_{icm} may reach a maximum of 2.7v peak. The output voltage swing V_o may reach a maximum of 5.2v peak. The bandwidth of the analog comparator may be as high as 2 MHz. This comparator has been subjected to the processing of different distribution functions from the two matrices and excellent results have been obtained. Error signals with distinct characteristics have been generated, and the comparator is capable of performing the following functions:

(1.) A "MATCH" condition

(2.) A positive error signal

(3.) A negative error signal

(4.) A bi-polar error signal

The schematic diagram of the analog comparator is shown in FIGURE 24. FIGURE 25, trace #1, pictorially displays the sampled prototype function from the output of the sample-hold circuit. Trace #2 displays the amplified

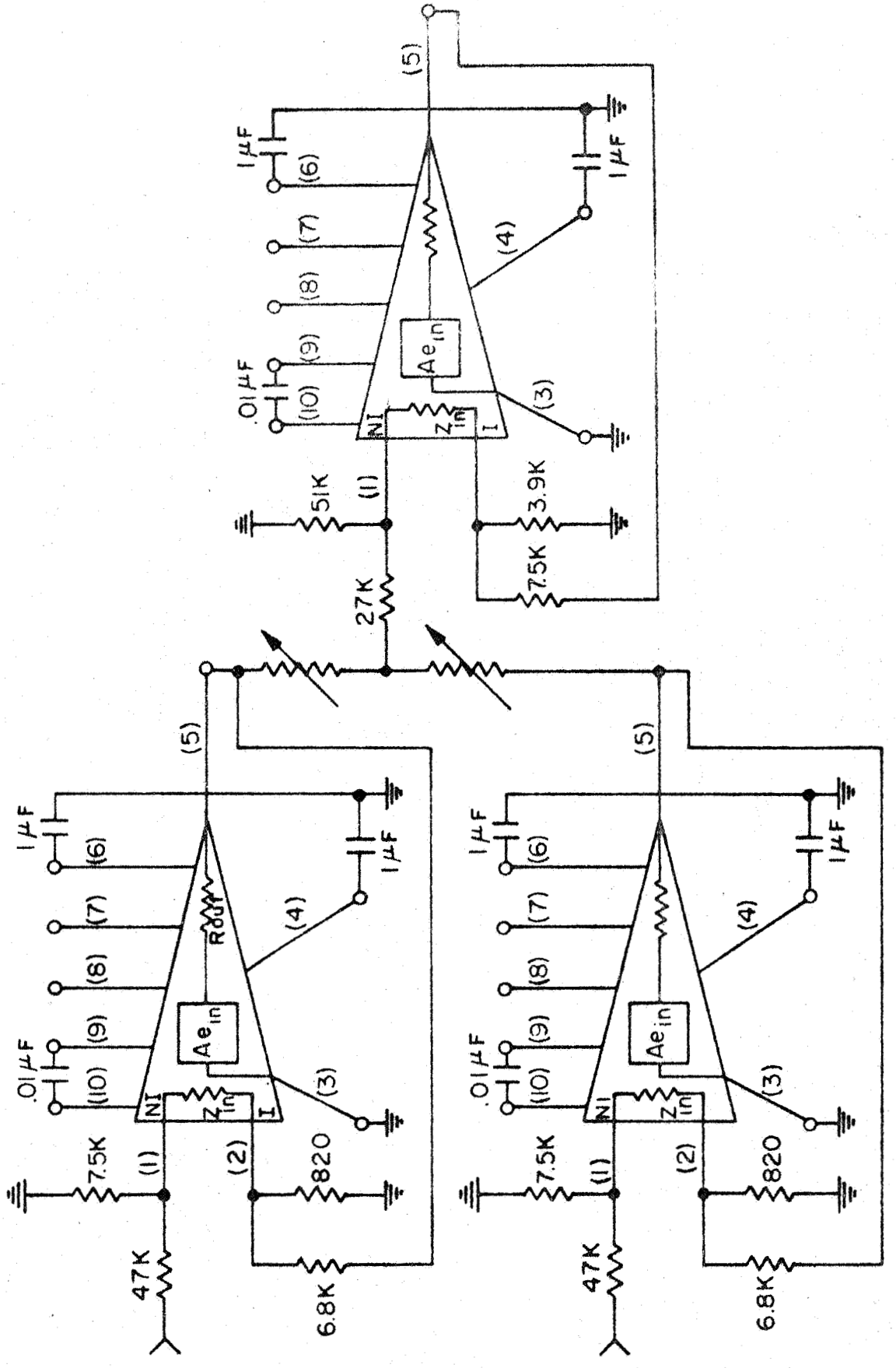


FIGURE 24: The Comparator

interrogation function. Trace #3 displays the amplified prototype function. Trace #4 displays the output from the analog comparator which is the generated error function to be used for adaptive training. The frequency of operation is 60KHz. The scale is 5 v/cm, and the time is 0.1 ms/cm.

FIGURE 26, trace #1, displays some arbitrary function set on the interrogating matrix. Trace #2 displays some arbitrary function set on the prototype matrix. Trace #3 displays the comparator output which has correlated the two functions. It is interesting to note the resemblance of this waveform to a sine function. It is now possible to integrate the waveform for a better representation, if necessary. Trace #4 displays the error function which has been amplified for the training process. The frequency of operation is 60KHz. The scale is 5 v/cm, and the time is 0.1 ms/cm.

FIGURE 27, trace #1, displays another arbitrary function set on the interrogation matrix. Trace #2 displays an aritrary function set on the prototype matrix. Trace #3 displays the comparator output, exhibiting the correlation which has taken place between the two functions. Trace #4 displays the error function which has been amplified for the training process. The frequency of operation is 60 KHz. The scale is 5 v/cm, and the time is 0.1 ms/cm.

FIGURE 28, trace #1, displays still another arbitrary function set on the interrogation matrix. Trace #2 displays again an arbitrary function set

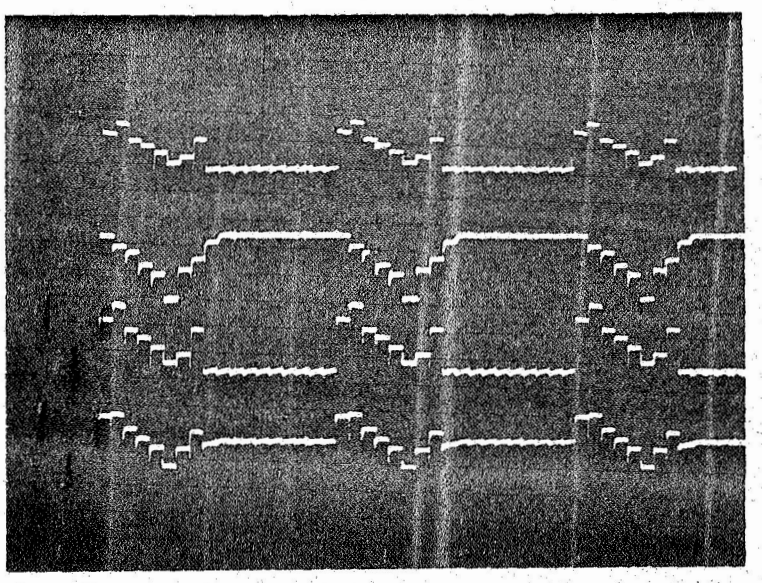


FIGURE 25: Oscillogram Showing the Process of Generating an Error Function between a Prototype and an Interrogating Function

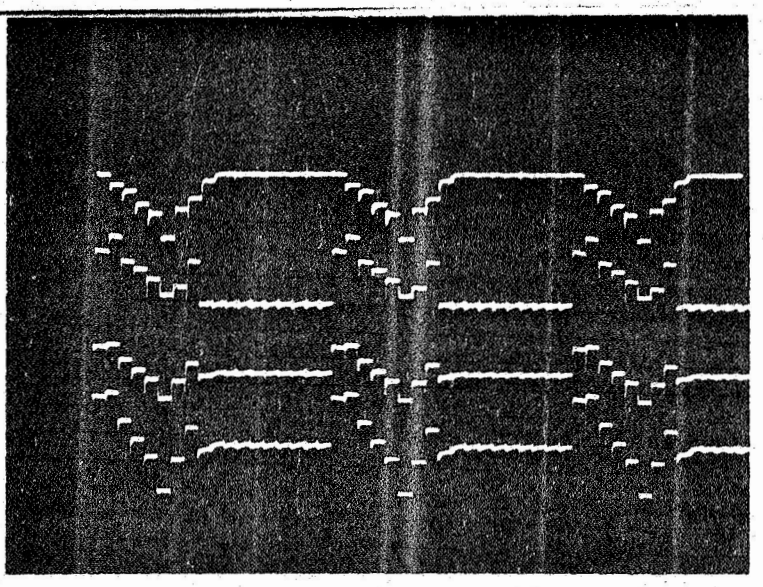


FIGURE 26: Oscillogram Showing the Process of Generating an Error Function between a Prototype and an Interrogating Function

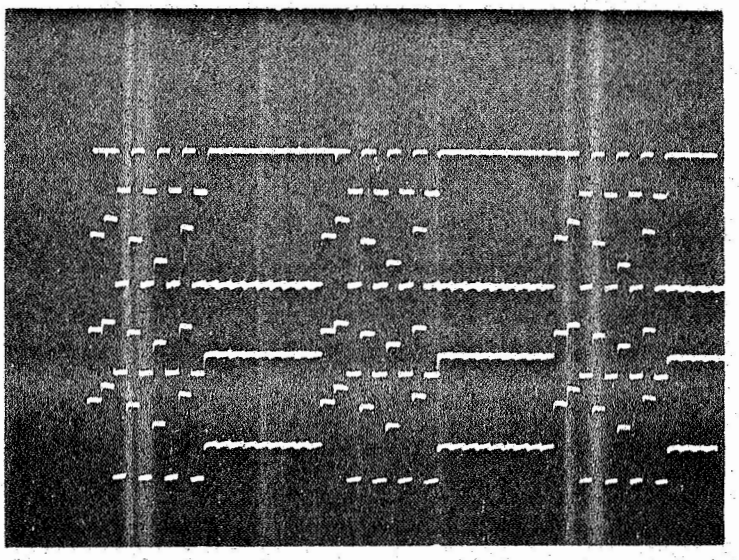


FIGURE 27: Oscillogram Showing the Process of Generating an Error Function between a Prototype and an Interrogating Function

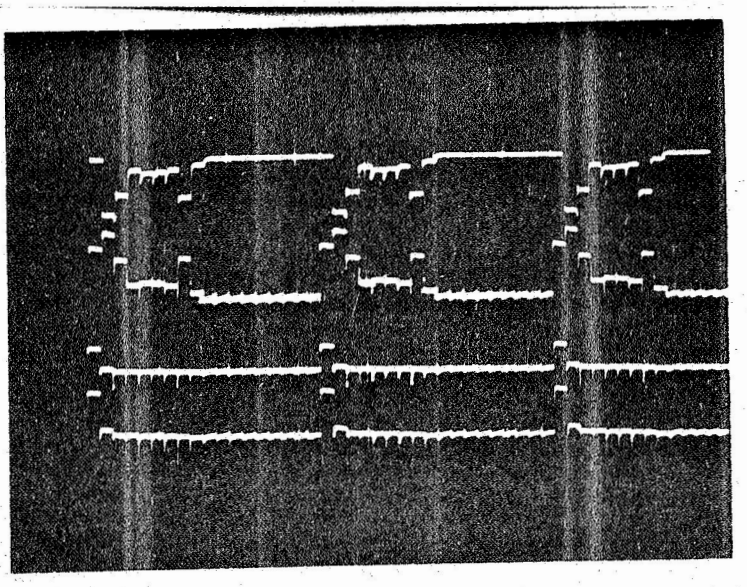


FIGURE 28: Oscillogram Showing the Process of Generating an Error Function between a Prototype and an Interrogating Function

on the prototype matrix. Trace #3 displays the comparator output, showing the correlation which has taken place between the two functions. Note that a "MATCH" condition does exist. The one remaining pulse is due to the "GATE" pulse used earlier to remove the "RESET" pulse. This remaining pulse will also be gated out in the future. Trace #4 displays the error function, which has been amplified for the training process. In this instance, the error function is "ZERO". The frequency of operation is 60 KHz. The scale is 5 v/cm, and the time is 0.1 ms/cm.

8. The Adaptive Training Circuitry

Having the capability of generating any type of an error signal, the next logical step was to apply this error signal in an adaptive training process. It should be noted here that the error signal is dependent upon the correlation between the prototype and interrogation matrices. Thus the limitations on the error signal are the same as those placed on the distribution function to be processed. It was theorized at the very beginning of the project, that the error signal could be fed back to the analog memory elements, and as a consequence, obtain a trainable analog memory element capable of adapting itself to a training pattern derived from the incoming signal. Thus, it was envisioned that through a repetitive process, the minimization of the error signal could be accomplished, and thereby achieve a learning process, i.e., one in which transfer of charges through the TRANS-POLARIZER* is facilitated by use. Experimentation was performed, and

it has been found that an analog associative memory with an adaptive learning characteristic is now feasible. A block diagram of the associated system of the electronic adaptive training process is shown in FIGURE 29. The error signal is obtained, as described in Section IV, B7, by comparing the interrogating signal with the output of the TRANSPOLARIZER* signal V_{out} (see Fig. 29). The error signal is prevented from controlling the TRANSPOLARIZER* because of the double zener diode D_3 which also insulates the control gate of the TRANSPOLARIZER*. In order to permit the error signal to correct the TRANSPOLARIZER* impedance, it is in a negative feedback mode fed back through the threshold bias elements T, D_3, and R, to the control gate of the TRANSPOLARIZER*. The biases required for offsetting the isolation offset of the diode D_3 are derived from the positive and negative error signal through diodes D_1, D_2, inverter I, level translators L_2 and L_1. The error signal will exist as long as a "MISMATCH" condition exists between the two matrices. At a time when the distribution functions are equal, due to the repetitive training of the prototype matrix, a "MATCH" condition set in. This denotes a lack in the error signal and signifies that the prototype matrix has been trained to the interrogating matrix. It is at this particular time that the associated adaptive training system may be removed either through a switch or a magnetic relay. It should be noted that the trainable analog memory element of Electrocristal just described should be a useful modular "buildingblock" in developing

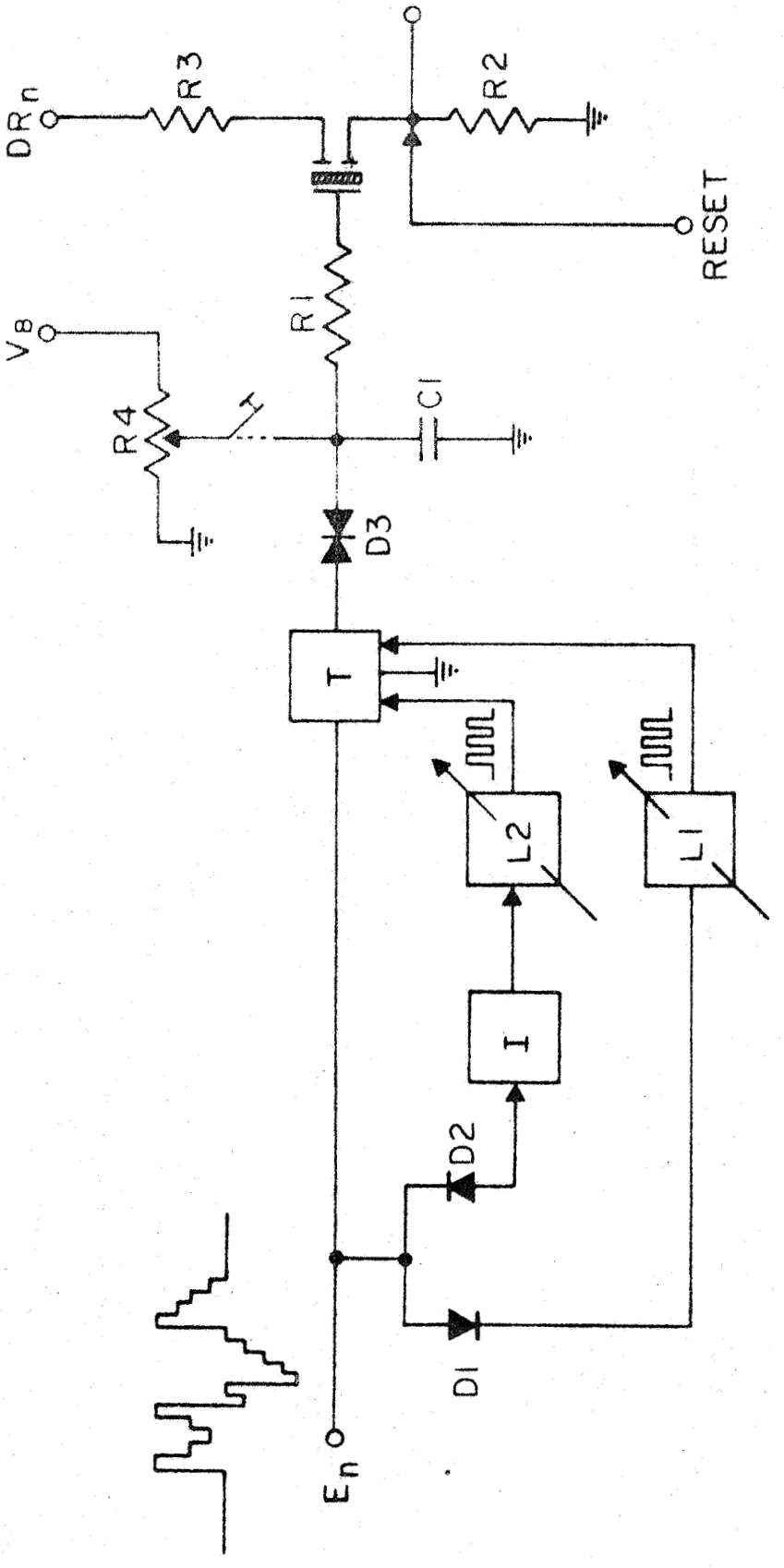


FIGURE 29: Schematic Diagram of a Trainable Analog Memory Element

simple learning machines of all kinds. Progress has come to a halt at this point, since our contractual period has come to an end.

V. TOPOLOGY OF THE EXPERIMENTAL MODEL

The experimental model accomodated in a rack is shown in FIGURE 30. It includes all units described in Section IV, B. FIGURE 31 is an enlarged upper part of the rack and comprises the following sections the content of which is given as follows:

Section A_1, A_2, A_3, --- A_{26}

Contains space for future development

Section B_1, B_2, B_3, --- B_{26}

Contains space for future development

Section C_1

Contains two inverters and two emitter-followers. One is used with the prototype generator and the other with the interrogating generator.

Section C_2, C_3, C_4, --- C_7

Contains the ripple-counter and the "AND" gates. The ripple-counter consists of nine flip-flops, from where eighteen sequential pulses are derived through eighteen "AND" gates.

Section C_8, C_9, C_{10}, --- C_{15}

Contains sixteen sequential drivers for the prototype matrix and sixteen sequential drivers for the interrogating matrix the outputs of which are shown in FIGURE 32.

Section C_{16}

Contains the "RESET" driver for the prototype matrix and one additional driver to be used for synchronization.

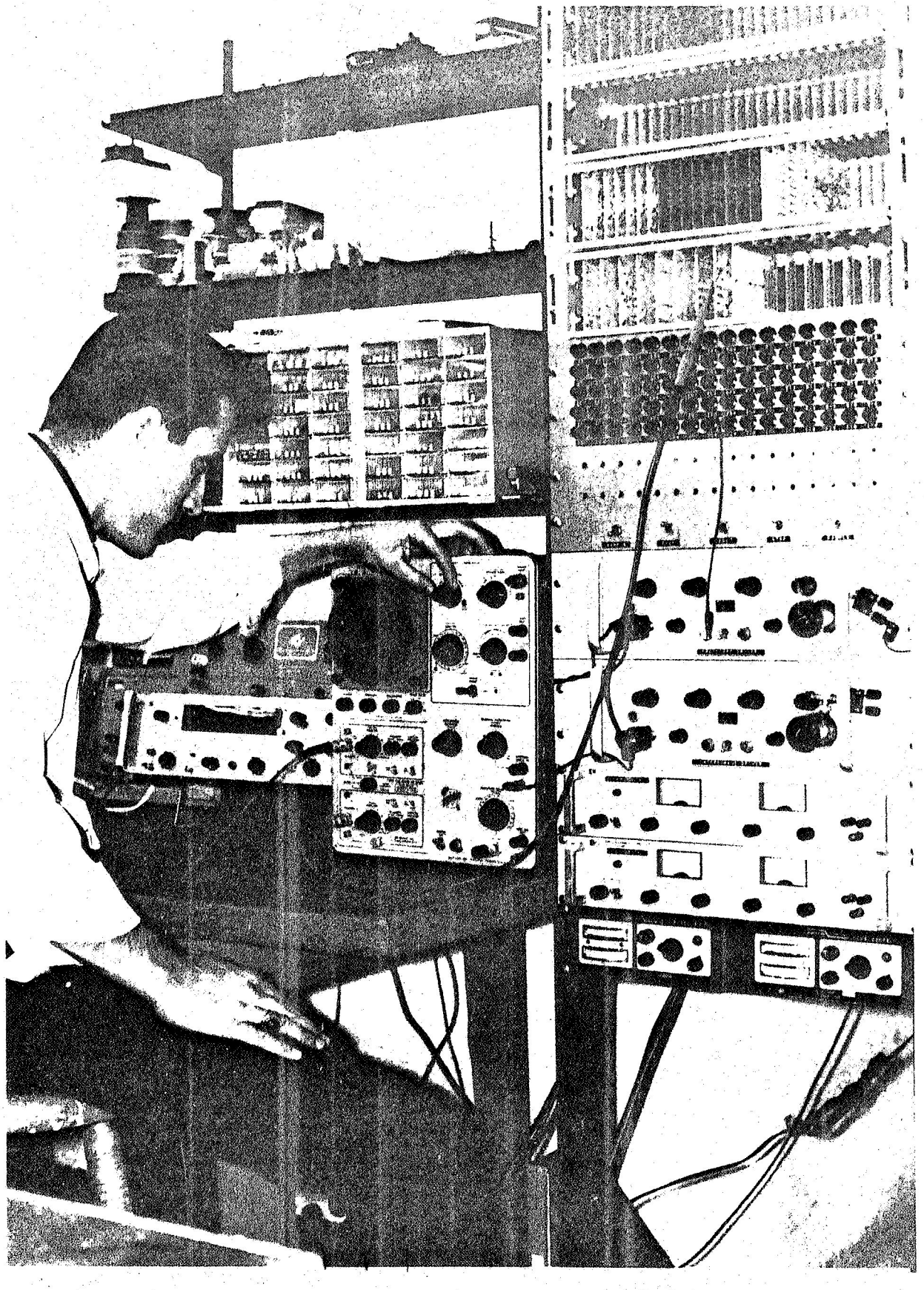


FIGURE 30: Topology of the Experimental Model

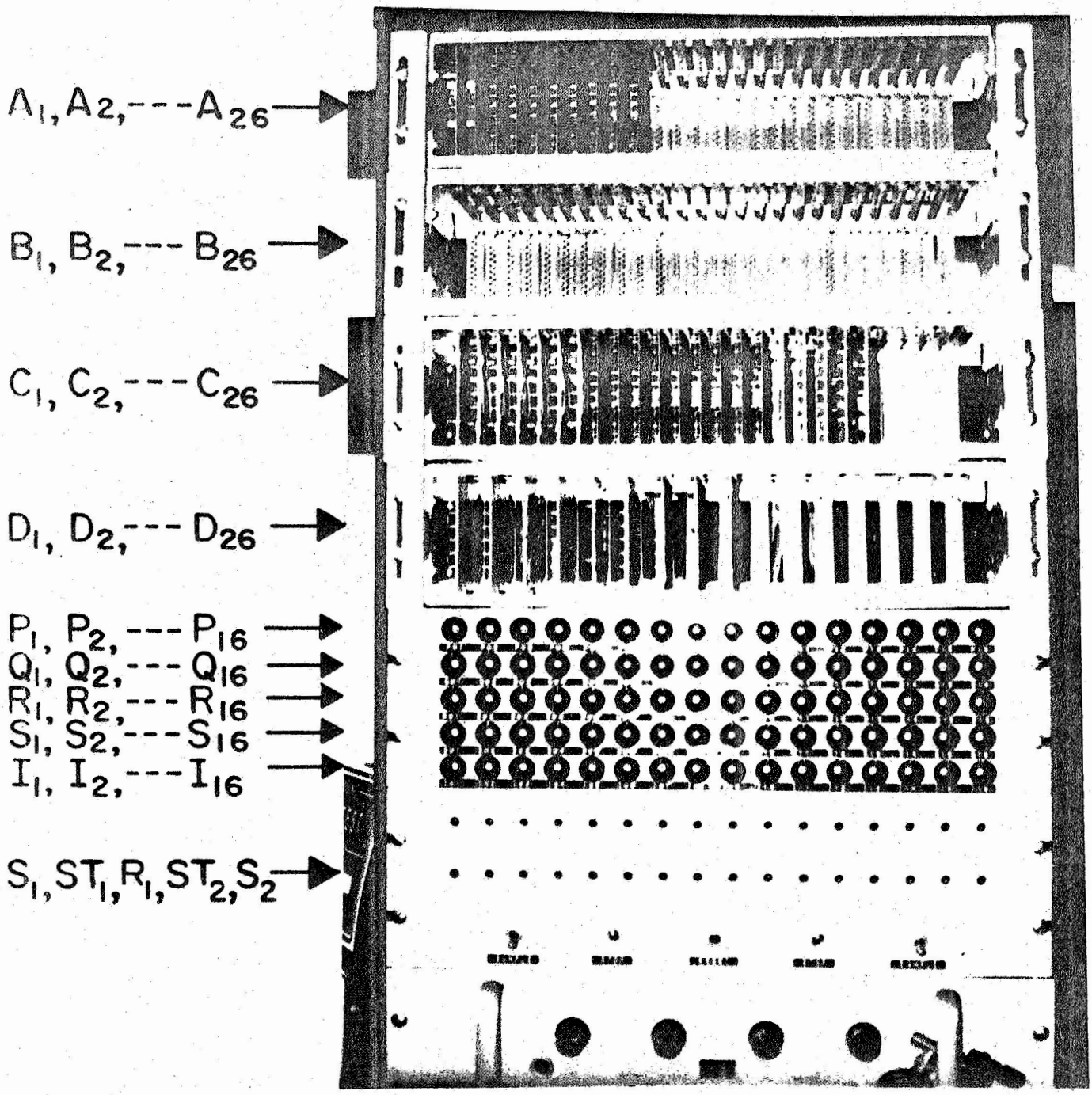


FIGURE 31: An Enlarged Upper Section of the Experimental Model

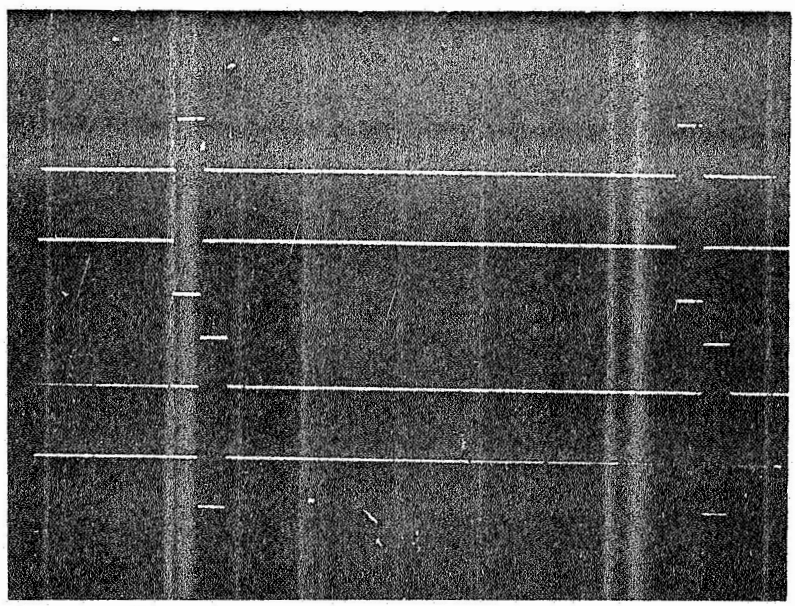


FIGURE 32

Traces # 1 and # 2, show the simultaneous drive from the driver cards to the prototype and interrogation functions. Both drivers are in synchronism.

Traces # 3 and # 4, show the next sequential simultaneous drive from the driver cards to the prototype and interrogation functions. Both drivers are again in synchronism.

Section C_{17}

Contains an interfacing circuit used in conjunction with the prototype matrix control points.

Section C_{18}, C_{19}

Contains the isolation diodes and the load for the interrogating matrix.

Section C_{20}, C_{21}

Contains the "FLAG". The "FLAG" consists of zener limiter, a flip-flop gate, a dual-transistor gate, an amplifier, a sample-hold circuit, two isolation amplifier, an analog comparator, and a pulse amplifier.

Section C_{22}

Contains the adaptive training system.

Section C_{23}, C_{24}, --- C_{26}

Contains space for future development

Section D_1, D_2

Contains the fourth row of the prototype matrix designated by S_1 through S_{16}

Section D_3, D_4

Contains the third row of the prototype matrix designated by R_1 through R_{16}

Section D_5, D_6

Contains the second row of the prototype matrix designated by Q_1 through Q_{16}

Section D_7, D_8

Contains the first row of the prototype matrix designated by P_1 through P_{16}

Section D_9

Contains the resistive interrogating matrix designated by I_1 through I_{16}.

Section P_1, P_2, P_3, --- P_{16}

Potentiometers used for the control settings on the first row of the prototype matrix.

Section Q_1, Q_2, Q_3, --- Q_{16}

Potentiometers used for the control settings on the second row of the prototype matrix.

Section R_1, R_2, R_3, --- R_{16}

Potentiometers used for the control settings on the third row of the prototype matrix.

Section S_1, S_2, S_3, --- S_{16}

Potentiometers used for the control settings on the fourth row of the prototype matrix.

Section I_1, I_2, I_3, --- I_{16}

Potentiometers used to drive the resistive interrogation matrix.

Switch S_1

Switch which is to be used in the sampling of the second row of the prototype matrix designated by Q_1 through Q_{16}.

Switch ST_1

Switch which s used for stopping the prototype matrix.

Push Button R

Push button used to reset all flip-flops in the ripple-counter to their original states.

Switch ST_2

Switch which is used for stopping the interrogating matrix.

Switch S_2

Switch which is used in the sampling of the first row of the prototype matrix designated by P_1 through P_{16}.

FIGURE 33 is an enlarged lower part of the rack and comprises the following sections the content of which is given as follows:

Section PG

Rutherford CMC, Model B15, pulse generator used to drive the prototype logic section.

Section IG

Rutherford CMC, Model B15, pulse generator used to drive interrogating logic section.

Section PS_1

HP-Harrison, Model 6438B, DC power supply used to provide 40 volts to the prototype drive section.

Section PS_2

HP-Harrison, Model 6438B, DC power supply used to provide -40 volts to the interrogating drive section.

Section PS_3

Electronic Research Associates-Magitran, Model SL36-2M, Silicon power supply used to provide -6 volts to both the prototype and interrogating logic sections.

Section PS_4

Electronic Research Associates - Magitran, Model SL36-2M, Silicon power supply used to provide - 6 volts to both the prototype and interrogating logic sections.

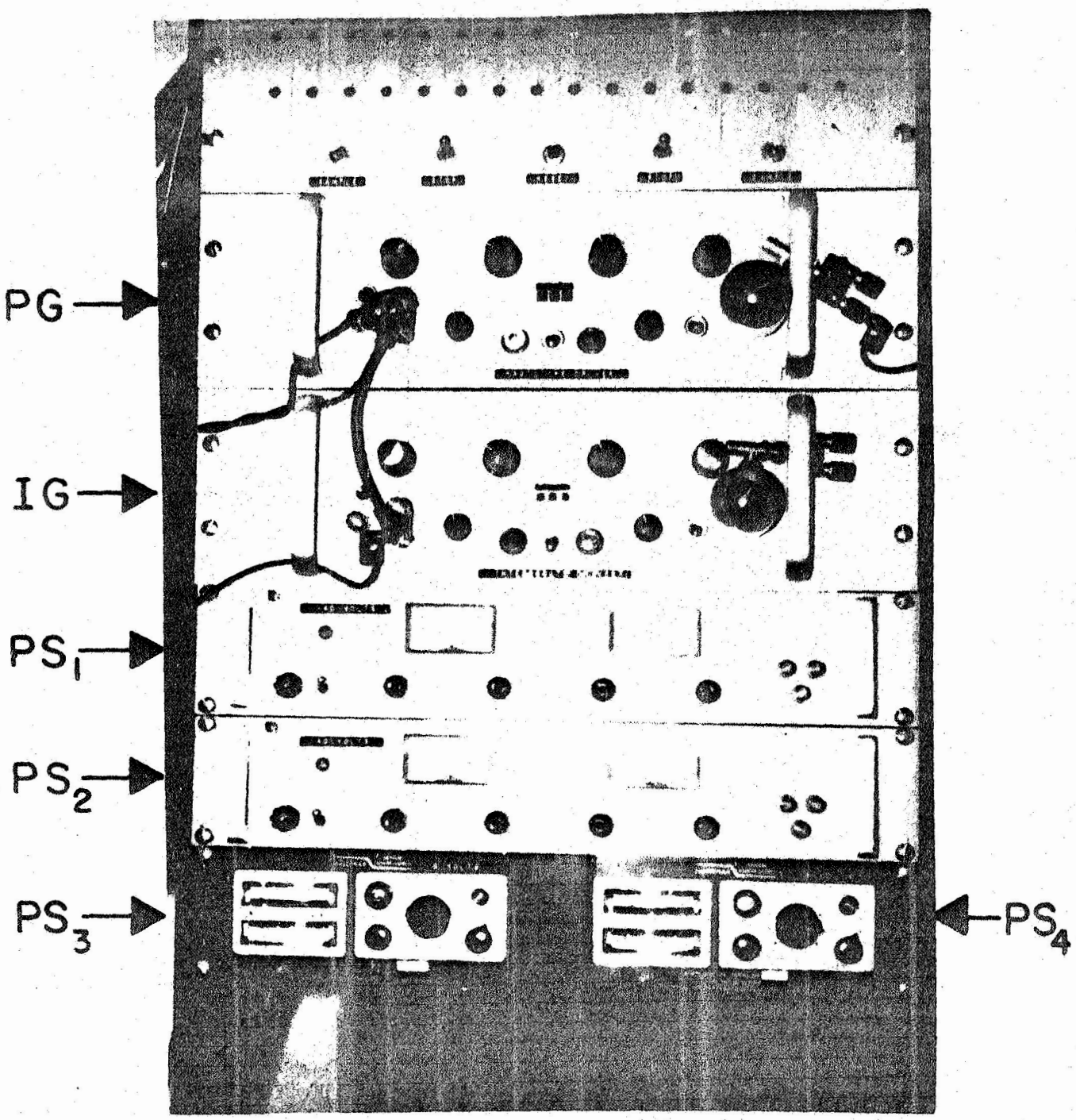


FIGURE 33: An Enlarged Lower Section of the Experimental Model

VI. SUMMARY

A concept of information processing was studied which utilizes multilevel samples for storing information. As a result, the concept of an Analog Associative Memory was developed. This required the development of the following main electronic blocks:

(1) A memory matrix capable of storing in its matrix a whole distribution function represented by multilevel samples. Each one of the distribution functions represents a prototype function.

(2) An interrogating matrix capable of simultaneously producing (in all of its matrix crosspoints) a particular distribution function represented by the same number of multilevel samples employed for representing the prototype function. Furthermore, this matrix must be capable of presenting any type of distribution function to all of the prototype functions for comparison.

(3) A flag capable of comparing and processing the information of both matrices so as to obtain meaningful classification.

In conformity with the statement of work, the experimental device which has been built was so designed that it has a capability of operating

between 0 and 2 MHZ. As a consequence, the pulse drivers cover nearly the frequency upt to video band spread. Since at present we have a 16-bit distribution function with 2 additional bits which are required for providing the re-cycling operation and the gating operation for the reset pulse, the maximum re-cycling frequency of a distribution function would be in the order of 100 KHZ. This high frequency was built in the first experimental model in order to have a sufficiently universal system for further expansion. The flag, which is the read-out section of the associated memory, will require more effort to match this spread.

In this first phase of work, we considered and used a 16-bit multilevel storage, in which case, if one considers only 10 distinct levels which can be set, the storage capacity of the present device when compared with a digital storage device would be in the ratio of $10^n/2^n$. However, if we consider that in this experimental model we use a potentiometer setting for the TRANSPOLARIZERS* we practically have "n" levels and as a consequence the storage capacity is incomparably larger than a binary storage. Since the volume of storage depends on the problem to which the associated memory will be applied, it was thought, that in developing the whole concept of an Analog Associative Memory, a distribution function represented by 16 multilevel bits would be adequate.

Instead of developing a mock-up system, an experimental model constructed which utilizes printed and integrated circuitries throughout.

Although this work took much more effort and time then originally contemplated, it permits the utilization of the present device in future developments, and in a next contractual phase it will not be necessary to lose time in converting a mock-up or bread-boarded model into a prototype system.

The 16-bit multilevel storage has been developed using TRANSPOLARIZERS* which permit the setting of any distribution function represented by 16 samples. This section of the TRANSPOLARIZER* storage has been built and operated for months and was used in the development of the read-out flag.

As stated before, we utilize 16 bits instead of 4 which far exceeds the requirements set by the Statement of Work. Preliminary work on controlling the conductivity of semi-conductors utilizing ferroelectric control elements was pursued. The technology of depositing semiconductors on the ferroelectric crystals has been successfully developed. At present Electrocristal has the capability to deposit excellent semiconductor layers of thin films on ferroelectric crystals. We would like to note also that five different vapor transport furnaces have been designed, constructed, and tested until satisfactory results were obtained. Furthermore, it is submitted that in developing improved TRANSPOLARIZER* elements, the following points are considered:

1. Improved doping crystals.
2. The development of quality lapping and polishing of crystals.

3. Optimization of the electroding process.

It should be noted that as a result of this work the preparation of two-section TRANSPOLARIZERS* with fairly uniform quality and low switching voltage (such as 12 volts) was accomplished. In addition, about 10 samples were prepared with a switching voltage as low as 4.5 volts. This has brought the TRANSPOLARIZER* well within the voltage range of transistors and as a result they are indeed compatible.

In the last period of this work, the concept of simple trainable multilevel storage elements was successfully tested and onperated. It is believed that this work opened new avenues in the field of pattern recognition, learning and automatic control.

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