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STUDY OF A NAVIGATION AND TRAFFIC CONTROL TECHNIQUE EMPLOYING SATELLITES

(Interim Report)

VOLUME III

USER HARDWARE

By Nathan Estersohn and Art Garabedian

DECEMBER 1967

Prepared under Contract No. NAS 12-539 by

TRW SYSTEMS GROUP
One Space Park • Redondo Beach, California 90278

Electronics Research Center
NATIONAL AERONAUTICS AND SPACE ADMINISTRATION

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STUDY OF A NAVIGATION AND TRAFFIC CONTROL TECHNIQUE EMPLOYING SATELLITES

Volume III. User Hardware

By Nathan Estersohn and Art Garabedian

1. INTRODUCTION

1.1 SCOPE OF EFFORT

The primary effort required in the NAVSTAR user equipment studies was to develop an interface with the other system elements (satellites, ground stations, etc.) leading to a systems concept which would assure the production of user equipments and a variety of user configurations at acceptable cost levels. In this instance, the design parameter to be optimized was clearly cost so that NAVSTAR could gain the broadest possible application.

Once an overall systems concept was established, the study effort in the user area was channelled along the major user subsystems. A flow chart illustrating the scope of effort in each area is presented in Figure 1. As detailed in the subsequent sections, the number of loops and iterations traversed varied with each subsystem design effort. For example, breadboarding was performed only for the antenna subsystem, and several design iterations were possible in the course of generating suitable antenna configurations. Industry pricing was available only on two of the subsystems, all others were internally generated. Because of the equipment complexity in receiver design, it was not possible in this study to perform extensive iterations.

1.2 USER CONFIGURATIONS

It is generally recognized that the basic design of the navigation satellite system must meet the needs of a wide variety of system users. Some users will want the maximum performance capability (self-contained, maximum accuracy and fix rates) and will be willing to invest considerable money in user equipment. Others will prefer to invest only a small amount in capital equipment in return for relaxation of certain capabilities, i.e., ground-aided computations, lower fix rates and decreased accuracies.

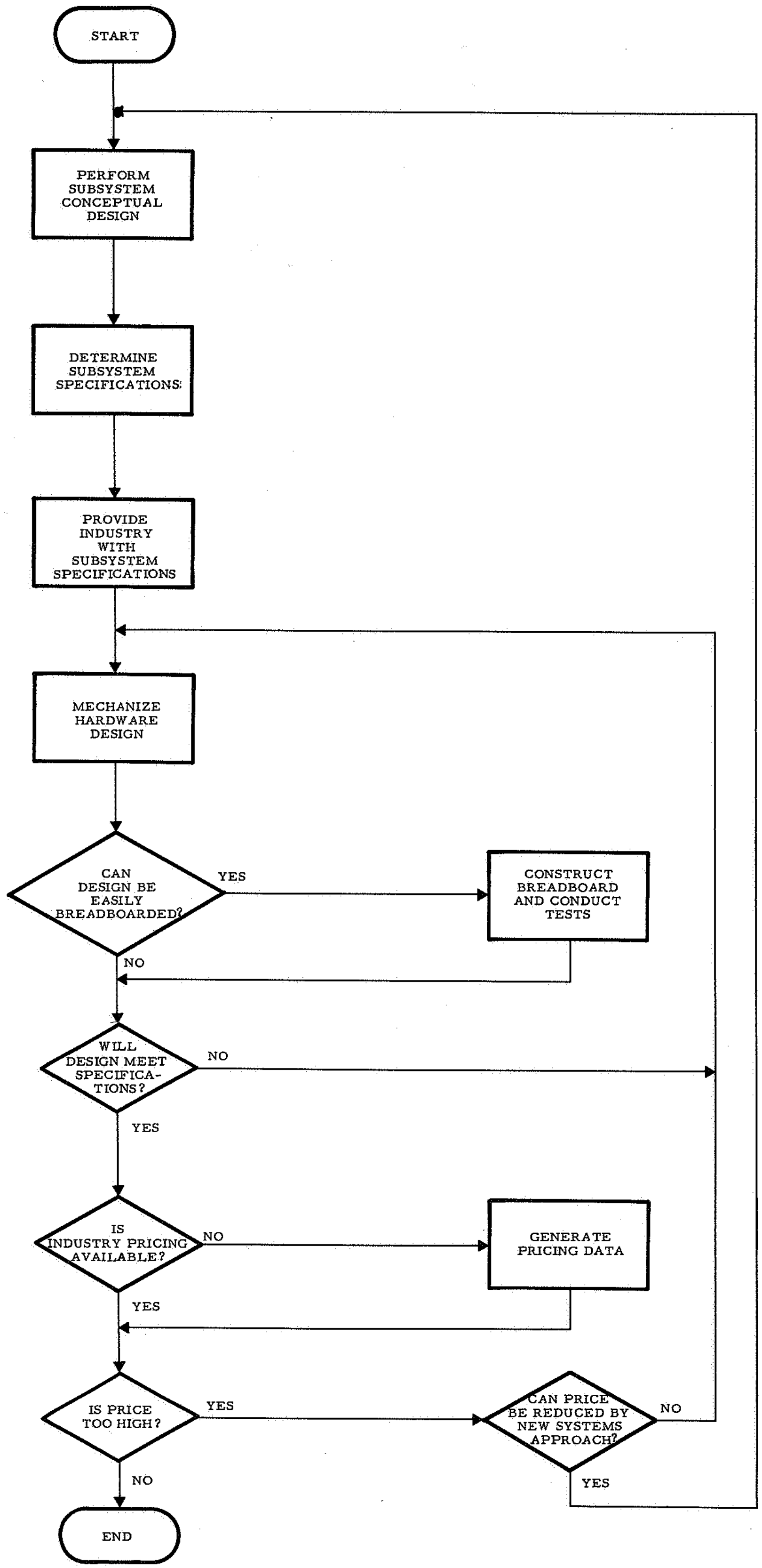


Figure 1. Flow Chart of Study Effort on User Equipment Studies

Thus, in the present NAVSTAR user equipment studies, TRW has simultaneously reviewed four basic user equipment configurations designed to appeal to distinct classes of system users. These basic configurations are described in this section and are referred to by letter designation as follows:

1) Configuration A — Automatic, self-contained (for supersonic aircraft)

2) Configuration A_1 — Automatic, self-contained (for general aviation)

3) Configuration B — Automatic, ground-aided computations (for all users)

4) Configuration C — Manual computations (for marine craft)

All of the above mentioned user configurations did not receive equal effort and consideration in the design of major user hardware subsystems. This is a logical and desirable consequence of orienting the studies on a subsystem hardware design basis rather than predicating them on the selected configurations. For example, with all but the computer subsystem the initial approach was to minimize design proliferation unless a significant improvement in cost was thereby achieved. Only in the design of the computing subsystem may one expect to see major design differences as a function of user configuration. Even so, the amount of engineering effort required for the design of a computing subsystem for Configuration A and A_1 is very substantial; for Configuration B, nonexistent (from the user's point-of-view); and for Configuration C, extremely modest.

A further observation relative to user configurations refers to general aviation and the user demanding inexpensive equipment. Because many users are involved in the general aviation class, it would be desirable if their NAVSTAR equipment costs coincided with those of the inexpensive user. However, even a cursory examination of the four specified configurations and their requirements would show that either Configuration B or C is the most inexpensive system. Configuration C would require further study to adapt it to the environmental limitations of the general aviation user.

Except for Configuration B, all user hardware configurations consist of five basic elements: the antenna, receiver, preprocessor, computing subsystem, and display subsystem. In Configuration B, the computing requirement is handled by the cooperating ground station.

1.2.1 Automatic Self-Contained User Hardware for SST Applications

A block diagram of Configuration A is shown in Figure 2. Transmissions from up to eight satellites are received by the user's L-band curved dipole turnstile antenna. The received signals are demodulated in the BINOR receiver. The preprocessor processes and decodes the two kinds of data appearing during satellite transmission — ranging data and satellite data. The output of the preprocessor is properly formatted for direct entry into the general-purpose computer. Using the range (phase) measurements, ephemeris, and other data received from the satellite, the general-purpose computer calculates the user's absolute position and presents it to the user via his display and control unit.

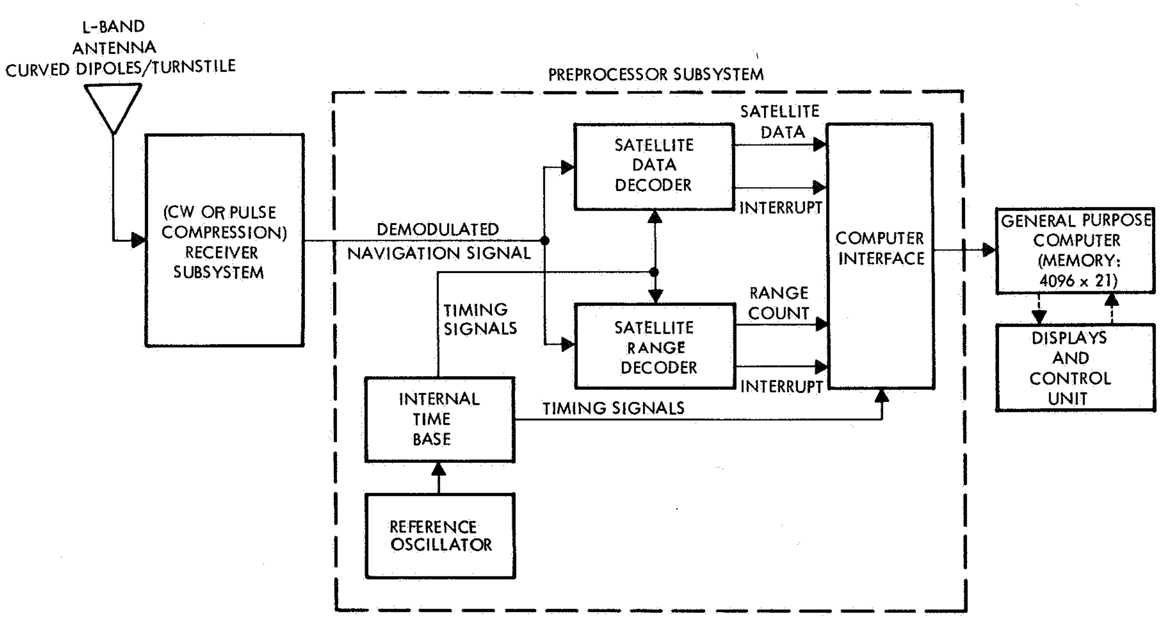


Figure 2. Block Diagram of NAVSTAR User Equipment Configuration A (Automatic, Self-Contained Computation for Supersonic Aircraft)

1.2.2 Automatic, Self-Contained User Hardware For General Aviation

Configuration A_1 is very similar to Configuration A except that a computer having lower performance and capacity can be used. The simplified set of equations which this user's equipment would be required to solve is discussed in sec. 3 of vol. II. Although less complex pre-processor and display units are probably in order, modifications to these units are relatively minor compared to the design changes permissible in the computing element.

1.2.3 Automatic, Ground-Aided User Hardware

The third basic user equipment configuration (Configuration B) is the fully automatic/ground station-dependent user system shown in Figure 3. It is recognized that certain classes of system users will want a substantial savings in user equipment capital investment. This type of user equipment configuration will accomplish this end through the elimination of the on-board computer.

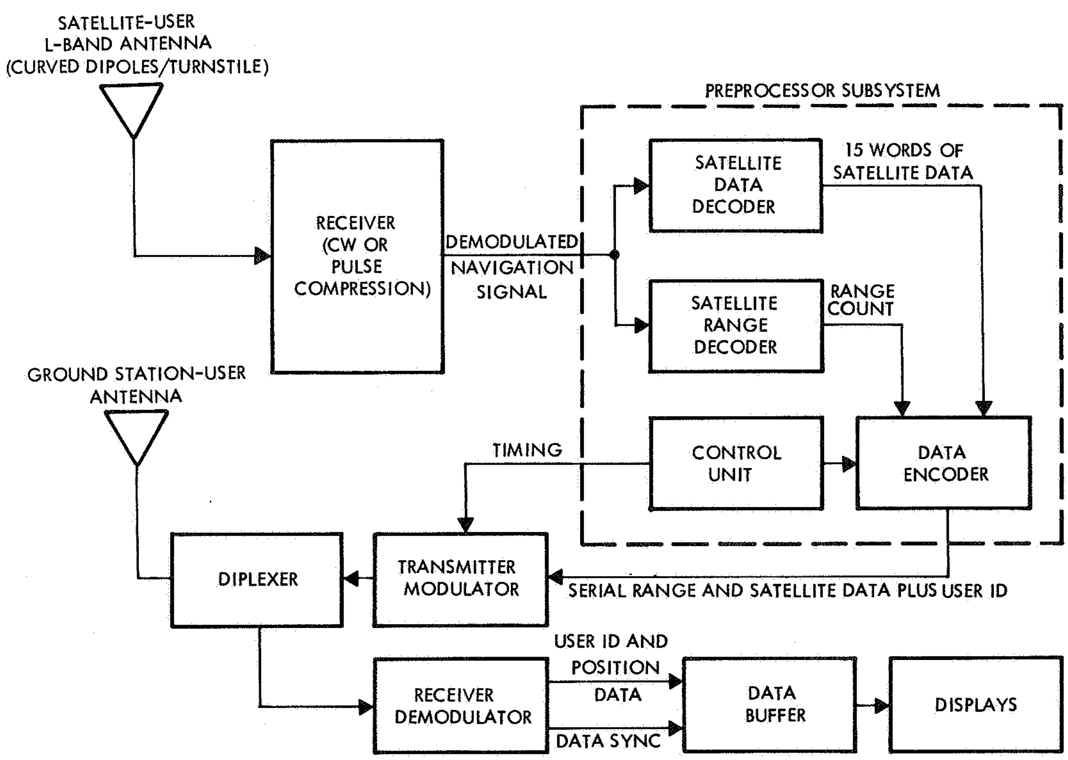


Figure 3. Block Diagram of NAVSTAR User Equipment Configuration B (Automatic, Ground-Aided Computations)

To achieve a navigational fix, the user will make the ranging tone phase measurements as before, but will relay this information along with his identification to a ground station where the actual computation will be performed. Once the fix is computed, the ground station will relay the computed information back to the system user for display. Unlike the fully automatic system, this class of system operation dictates a requirement for a two-way communication link with a ground computing facility.

A user having this basic equipment complex will have sufficient display capability to perform hand calculations on the raw satellite data in event of emergencies when two-way communication with the ground is lost.

It is anticipated that the communication link between the user and ground station will be shared by all users on a time-multiplexed basis.

1.2.4 Manually Operated User Configuration

The fourth class of user equipment configuration (Configuration C) is designed for the user who is satisfied with obtaining fixes having reduced accuracies, and at less frequent intervals, in exchange for greatly simplified and relatively inexpensive user hardware.

The basic equipment required is depicted in Figure 4 and utilizes the TRW-designed MINSCO technique for position determination (see sec. 3, vol. II). Again, the user equipment contains the basic equipment to determine the ranging-tone phase measurements from the navigation satellites within the user's field-of-view. These phase measurements, along with reference data received on a separate channel, are displayed on appropriate equipment. The user then solves a set of simple equations to compute his position relative to the nearest reference point, based upon this displayed information. This could be done with the aid of a desk calculator and would take a few minutes. An electronic calculator with temporary storage locations would reduce this time. Computing devices of low weight and cost could be developed for this application, but the investigation of such hardware was not considered.

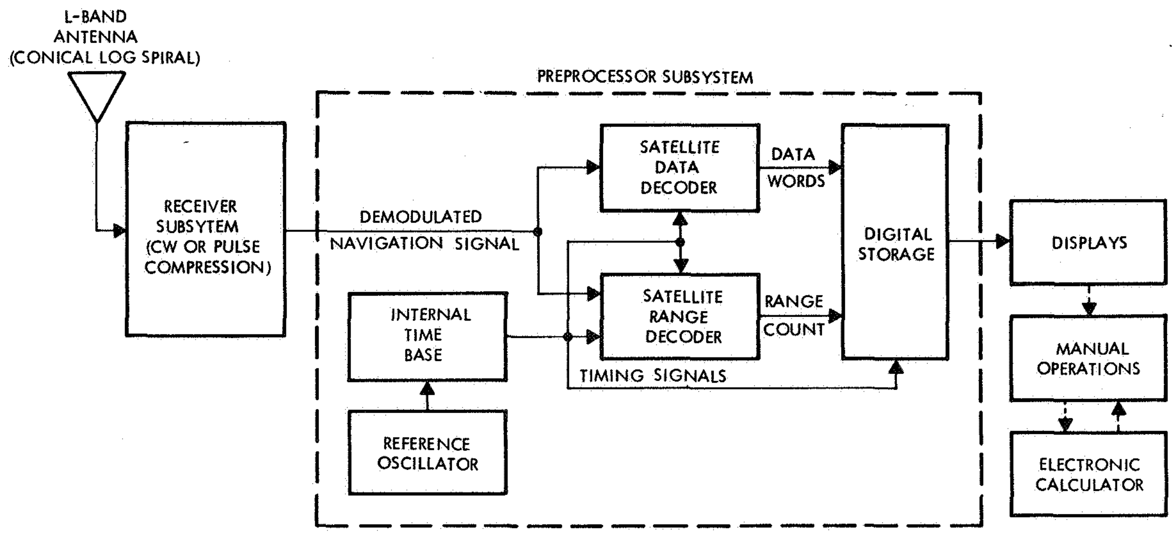


Figure 4. Block Diagram of NAVSTAR User Equipment Configuration C (Manual Computations)

1.3 OUTLINE OF OTHER SECTIONS

Sec. 3 on System Description is presented for reference purposes and describes the basic NAVSTAR system, including its key elements and major functions. Of primary interest is the relationship of the user equipment to other segments of the NAVSTAR system.

Sec. 4 represents the heart of the current user equipment studies and the separate subsecs. 4.1 through 4.5 describe each of the major user subsystems: antenna, receiver, preprocessor, computer, and display and control, respectively.

App. B on ranging modulation studies presents the theoretical design considerations inherent in the selection of a suitable ranging technique for the NAVSTAR system.

1.4 ACKNOWLEDGMENTS

The findings that are being submitted to NASA-ERC were the result of a strong team effort. While numerous technical personnel made contributions to the study results contained in the various volumes comprising

this interim report, the following TRW Systems people made significant contributions to the analyses presented in this volume:

Antenna:	G. Wong
Receiver:	A. Garabedian, A. Martin
Preprocessor:	B. Cappa, N. Estersohn, A. Garabedian, M. Kushner, B. Meyers, J. Molis
Computer:	N. Estersohn, J. Freedman, B. Handy
Displays:	G. Blechman, R. Selden, G. Triestman
Appendix:	A. Garabedian, P. Nilsen
Preparation of Volume III:	A. Garabedian, N. Estersohn
User Hardware Study Direction:	N. Estersohn, D. Otten
Modulation Techniques Studies:	A. J. Mallenckrodt

2. SUMMARY

2.1 GENERAL

The TRW NAVSTAR user equipment studies have resulted in the successful design of equipments utilizable in any one of four different options or configurations. The major elements in each configuration are shown in their corresponding block diagrams in sec. 1, Figures 2 through 4.

A very extensive initial effort to derive analytically an optimum ranging modulation technique preceded the hardware design phase. The results of the modulation studies are summarized both in vol. I and app. B of this volume. In potential NAVSTAR applications, the BINOR code appeared superior to the two other ranging schemes (CW fixed tones and pulse compression); however, it was decided to design receiver and preprocessor hardware for each system. Until a reasonable hardware mechanization is accomplished, it is not always obvious which design concept will be most economical to fabricate, particularly where large production volumes are possible.

Design specifications on all the NAVSTAR user subsystems were prepared (see subsecs. 4.1 through 4.5) and issued to the major manufacturers in each area of technology. The purpose of this was to determine the availability of off-the-shelf hardware and to secure cost projections for large production orders. This effort was particularly successful for the computing and display systems.

In the area of antenna design, TRW breadboarded and tested several designs after it was determined that stock items were not available from industry. This effort, aimed particularly at the SST user, revealed gain-pattern deficiencies in the previously proposed Archimedian spiral antenna design and validated several other techniques, such as the curved dipole turnstile antenna system.

The cost objectives underlying the user hardware design are met by today's technology for the supersonic aircraft user. For the other configurations, the cost projections into the 1970 - 1975 period are either within reasonable bounds or can be made as explained in subsec. 2.3.

2.2 AVAILABILITY OF OFF-THE-SHELF COMPONENTRY

One of the objectives of this study was to determine the developmental status of all equipments required by the NAVSTAR user. This has been successfully accomplished, and the results can best be explained in the following manner.

If a contract were to be let tomorrow for the mechanization of the TRW NAVSTAR system, off-the-shelf hardware could be immediately secured for the computing and display subsystems. The preprocessor presents no special design problems, but since its functions cannot be universally applied, it is not available as a regular stock item and must be ordered to specifications. An antenna configuration applicable for all users, except the supersonic aircraft user, is readily available in the form of a conical-log spiral antenna system. This, too, can be ordered as a supply item. Several suitable antenna designs have been developed in the course of the study for the SST user (the curved dipole turnstile antenna and the slotted dipole beam switching antenna), but these configurations require some additional research and development to select design parameters for optimum performance.

Three different designs have been postulated and carefully analyzed: the BINOR code, fixed tones, and the pulse compression systems. All three systems easily meet the basic NAVSTAR requirements. (Comparative data on the three modulation techniques are given in detail in app. B.) However, when cost and equipment complexity are considered, only the BINOR code and pulse compression systems are serious candidates for implementation in the NAVSTAR system. Either system is easily mechanized within today's state-of-the-art.

2.3 SUMMARY OF USER COSTS

The design of a NAVSTAR system to meet acceptable navigation requirements of accuracy, fix rate, worldwide coverage, etc., was never really regarded as an extremely formidable engineering undertaking. A very difficult problem, however, did exist in the engineering selection of techniques and equipments reducing user costs below a reasonable threshold value.

Based on the TRW NAVSTAR design, cost information was obtained from various sources for the four user configurations under study (see Table I). The cost data presented throughout this volume are current through 1967. Although the period of greatest interest is 1970-1975 (when the NAVSTAR system is expected to become operational), very little confidence can be attributed to "way-out" projected figures unless they are firmly based on today's technology and pricing structure. With reasonably accurate 1967 figures, further projections can be made on the basis of historical trends, emerging new technologies, etc.

Table I summarizes the average costs for the four NAVSTAR user hardware configurations. Tables II, III, IV, and V give the supporting cost breakdowns on a subsystem basis for each of the four configurations. Cost data for both BINOR code and pulse compression modulation concepts are included. However, only the receiver and preprocessor subsystems are affected by the modulation technique employed.

The cost data associated with the computing and display units were obtained from major manufacturers; all other pricing information was generated internally.

A review of the data presented in the summary cost tables reveals the following:

1) Configuration A (Table II) — The major cost item ($\geq$65% of total) is the computer, priced over \$20K even in large quantities. Although the total price of \$33K - \$35K is quite reasonable for the SST user, this figure would be reduced by as much as 50 percent in an integrated inertial/NAVSTAR system. The reduction would result from using single computer and display and control units for both functions.

2) Configuration A_1 (Table III) — Again the major cost item is the computing element which makes up approximately 60 percent of the total cost. A total of \$28K - \$30K is excessive for the general aviation class of user. The following alternatives are available: the general aviation user could utilize configuration B (ground-aided computations) as his primary mode of operation; or the MINSCO system (configuration C) could be made available to the general aviation user by further refinements of the hardware mechanizations in terms of size and weight.

TABLE I

SUMMARY OF AVERAGE COSTS FOR SEVERAL NAVSTAR USER HARDWARE CONFIGURATIONS

	Configuration	Unit Price in Dollars (For Ouantities Shown) 100 BINOR Code	100 Pulse Compression	1,000 BINOR Code	1,000 Pulse Compression	10,000 BINOR Code	10,000 Pulse Compression
A	Automatic, self-contained (for supersonic aircraft)	69,785	62,655	45,925	41,805	35,400	32,780
A_1	Automatic, self-contained (for general aviation)	52,710	45,580	39,960	35,840	30,350	27,730
B	Automatic, ground-aided computations	19,445	12,315	12,425	8,305	8,375	5,755
C	Manual computations	20,870	13,740	13,620	9,500	9,580	6,960

TABLE II

SUMMARY OF AVERAGE COSTS FOR NAVSTAR USER HARDWARE CONFIGURATION A

Subsystem	Unit Price in Dollars (For Ouantities Shown) 100 BINOR Code	100 Pulse Compression	1,000 BINOR Code	1,000 Pulse Compression	10,000 BINOR Code	10,000 Pulse Compression
Antenna	325		275		250	
Receiver	7,130	6,370	4,410	4,250	2,960	2,840
Preprocessor	11,630	5,260	7,440	3,480	4,890	2,390
Computing	35,700		28,800		23,300	
Display	15,000		5,000		4,000	
Totals	69,785	62,655	45,925	41,805	35,400	32,780

TABLE III

SUMMARY OF AVERAGE COSTS FOR NAVSTAR USER HARDWARE CONFIGURATION A_1

Subsystem	Unit Price in Dollars (For Quantities Shown)					
	100		1,000		10,000	
	BINOR Code	Pulse Compression	BINOR Code	Pulse Compression	BINOR Code	Pulse Compression
Antenna	250		210		200	
Receiver	7,130	6,370	4,410	4,250	2,960	2,840
Preprocessor	11,630	5,260	7,440	3,480	4,890	2,390
Computing	27,700		22,900		18,300	
Display	6,000		5,000		4,000	
Totals	52,710	45,580	39,960	35,840	30,350	27,730

TABLE IV

SUMMARY OF AVERAGE COSTS FOR NAVSTAR USER HARDWARE CONFIGURATION B

Subsystem	Unit Price in Dollars (For Quantities Shown)					
	100		1,000		10,000	
	BINOR Code	Pulse Compression	BINOR Code	Pulse Compression	BINOR Code	Pulse Compression
Antenna	325		275		250	
Receiver	7,130	6,370	4,410	4,250	2,960	2,840
Preprocessor	11,630	5,260	7,440	3,480	4,890	2,390
Display	360		300		275	
Totals	19,445	12,315	12,425	8,305	8,375	5,755

TABLE V

SUMMARY OF AVERAGE COSTS FOR NAVSTAR USER HARDWARE CONFIGURATION C

Subsystem	Unit Price in Dollars (For Quantities Shown)					
	100		1,000		10,000	
	BINOR Code	Pulse Compression	BINOR Code	Pulse Compression	BINOR Code	Pulse Compression
Antenna	250		210		200	
Receiver	7,130	6,370	4,410	4,250	2,960	2,840
Preprocessor	11,630	5,260	7,440	3,480	3,890	2,390
Computing	1,500		1,260		1,255	
Display	360		300		275	
Totals	20,870	13,740	13,620	9,500	9,580	6,960

3) Configuration B (Table IV) — The associated costs for ground-aided computations ($6K - $8K in large quantities) should be acceptable, particularly for commercial applications. A 50 percent cost reduction is projected into 1970 — 1975 making a $3K — $4K system available for users of this mode of operation.

4) Configuration C (Table V) — This configuration is most promising for the user desiring very inexpensive equipment and an independent capability of satellite navigation. The total price tag presented, $7K to $10K — with 50-percent cost reductions, $4K to $5K — can be projected for the 1970's. This configuration utilizes the TRW-designed MINSCO technique and was created as a clear low-cost alternative to the basic NAVSTAR concept. The MINSCO design was generated late in the effort, but additional cost savings in the receiver and preprocessor subsystem designs may result from further study.

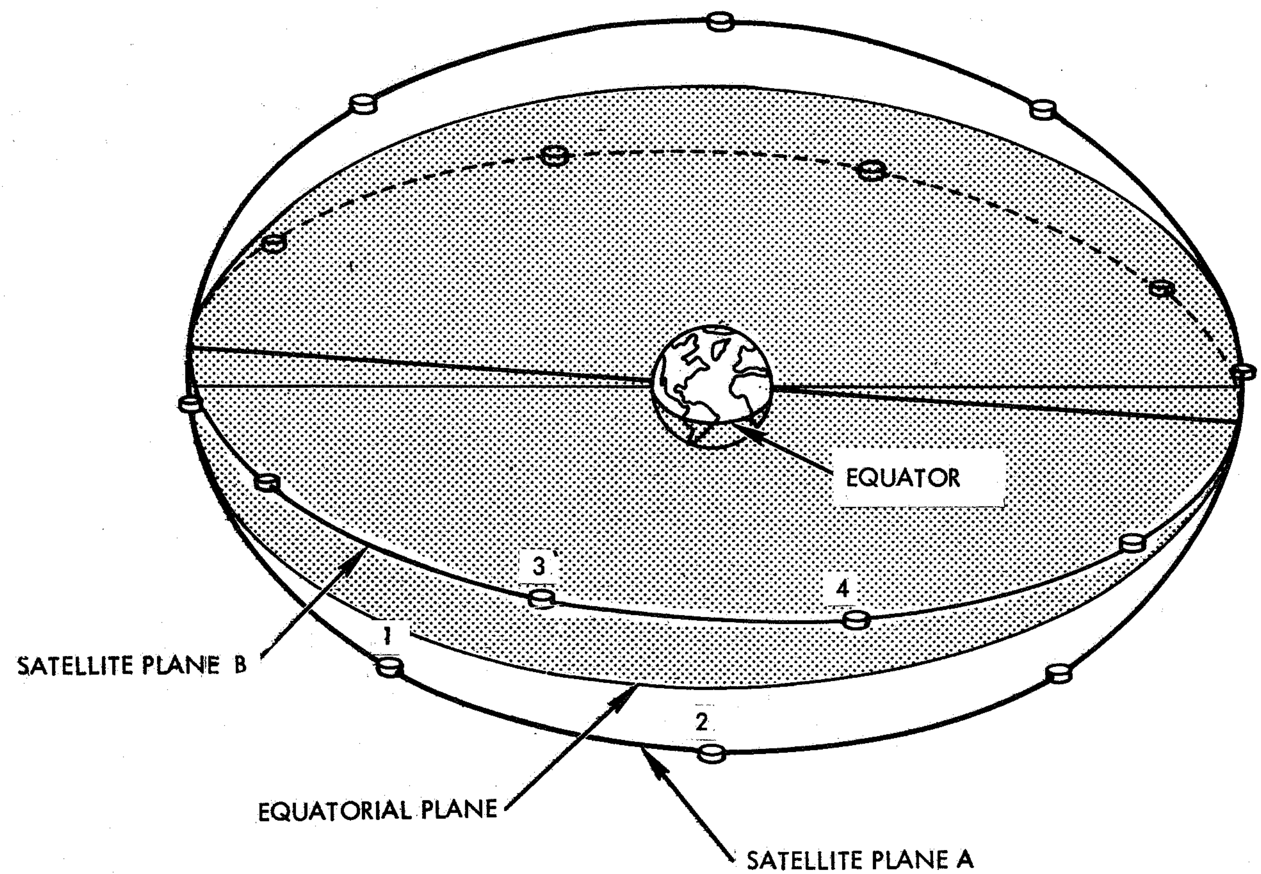
Cost savings are anticipated as refinements are implemented in the MINSCO design. For large quantities, Configuration C user hardware may be available in the $2K to $3K price range in the 1970's.

3. SYSTEM CONFIGURATION

The NAVSTAR network consists of satellites using synchronous inclined orbits. For worldwide coverage, 16 satellites would be placed in two orbit planes inclined 18.5° to the equator with their nodal lines 157.5° apart as depicted in Figure 5. For an interim system that would cover, for example, the Atlantic Ocean, a four-satellite network could be established. The satellite transmissions are time-multiplexed so that the satellites broadcast in time sequence. Each satellite radiates a precise navigation signal in its own assigned time slot. Since the satellite signals are accurately timed relative to each other by ultra-stable oscillators on board each satellite, a NAVSTAR user can measure range differences between the satellites by measuring the time difference between receipt of the ranging signals. Four satellites are sufficient to locate a user position both in earth coordinates and altitude. For the worldwide system, pairs of satellites on opposite sides of the globe would be assigned the same time slot. Consequently, eight satellites will be time-division multiplexed so that each satellite repeats its ranging signal every eight time slots.

Figure 6 portrays an interim system of four satellites covering the Atlantic Ocean and shows the operations and functions of the system elements. Each satellite repeatedly transmits range and certain data information in its assigned time slot on a single L-band carrier. In addition, the satellites contain a transponder to relay satellite tracking data from two remote tracking stations to a central ground station. This relay link uses L-band uplink and downlink carriers which are assigned L-band frequencies that will not interfere with reception of the satellite navigation signal by system users and ground stations.

The remote tracking stations track each satellite by receiving the satellite navigation transmissions and determining the range and satellite ID information. These data together with ground station ID and time of day are continually relayed via an L-band transmitter and the satellite transponders to the central ground station.



NOTES:

1. TWO ORBIT PLANES, INCLINED 18.5^{0} TO EQUATOR, LINES OF NODES 157.5^{0} APART

2. INTERIM SYSTEM CONSISTS OF SATELLITES 1, 2, 3, 4

Figure 5. NAVSTAR Satellite Geometry

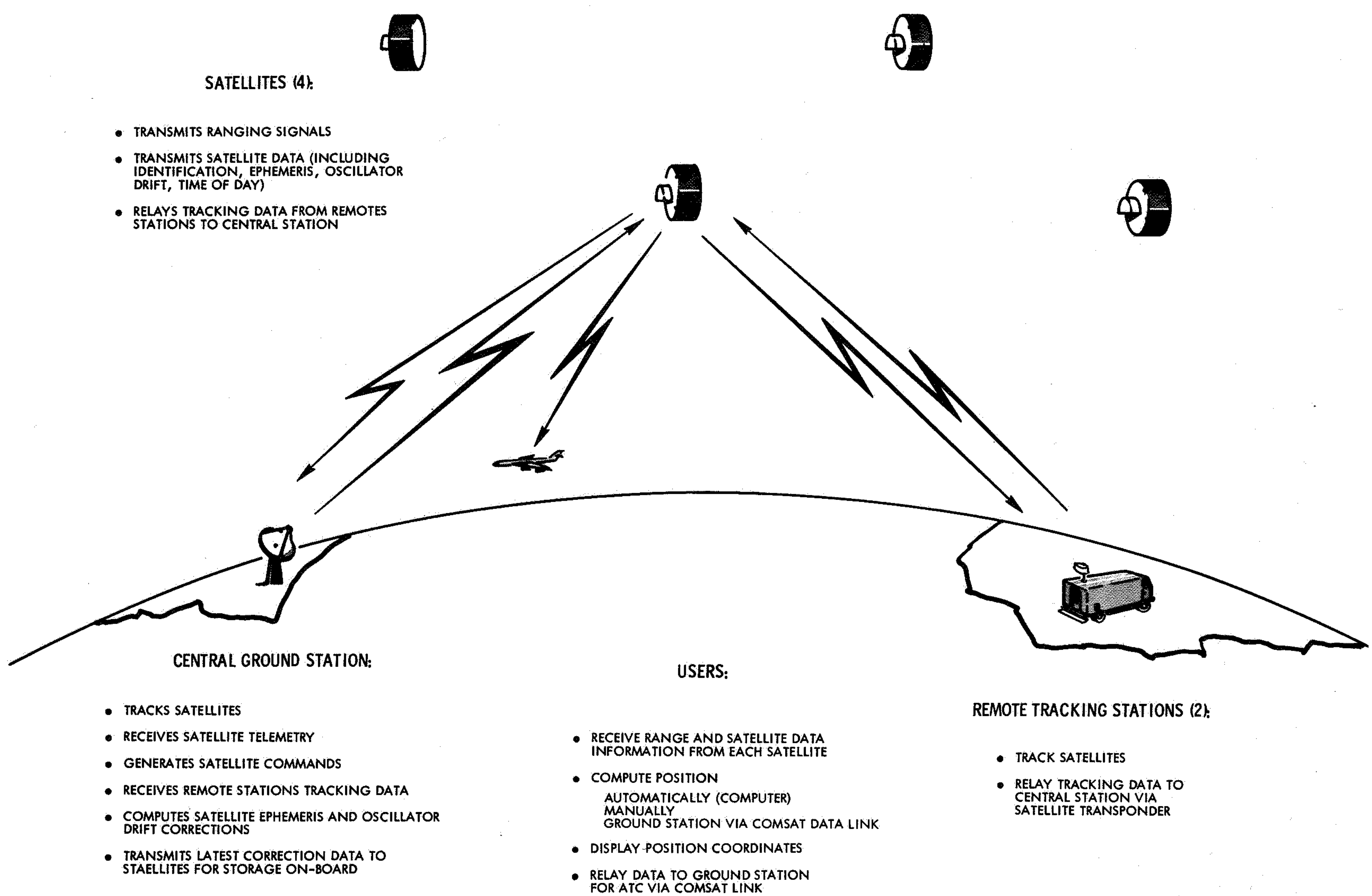


Figure 6. NAVSTAR Information Network

The central ground station contains the data processing computer which continually tracks the ephemeris and oscillator drift of each satellite. The computer generates and periodically updates satellite ephemeris and oscillator drift correction data to each satellite via an S-band command link. The data are stored on board and subsequently broadcast to system users as part of the navigation signal broadcasts. Other functions of the central station are generation of satellite commands and reception of satellite telemetry via an S-band telemetry carrier from each satellite. In addition, the central station performs the tracking function of a remote tracking station, thereby providing additional tracking data for the computer. The computer can also be used to display the telemetered status of each satellite.

The satellite navigation signal broadcasts are received by the NAVSTAR users, and position fixes are computed from the range and satellite data information. Any NAVSTAR user has the option of employing whichever method of position computation (i.e. Configuration A, A_1, B, C) he chooses and for which he is equipped. In Configurations A and A_1, the computation is done by a digital computer and the position coordinates are displayed for the user's information. In Configuration B, the range data are automatically relayed to a ground station via a COMSAT data link. The ground station computes the position fixes and sends these data back to the user over a COMSAT data link for display to the user. In Configuration C (the manual mode), the received range and satellite data are displayed visually for the user. From the displayed data, the user calculates the position fixes by hand with the aid of an electronic calculator. Finally, for certain users, position fixes or raw-range data are relayed to an air traffic control center (ATC) again via a COMSAT data link.

Figure 7 shows NAVSTAR RF links and simplified block diagrams for each element in the system. The COMSAT data links discussed above are not shown in this figure.

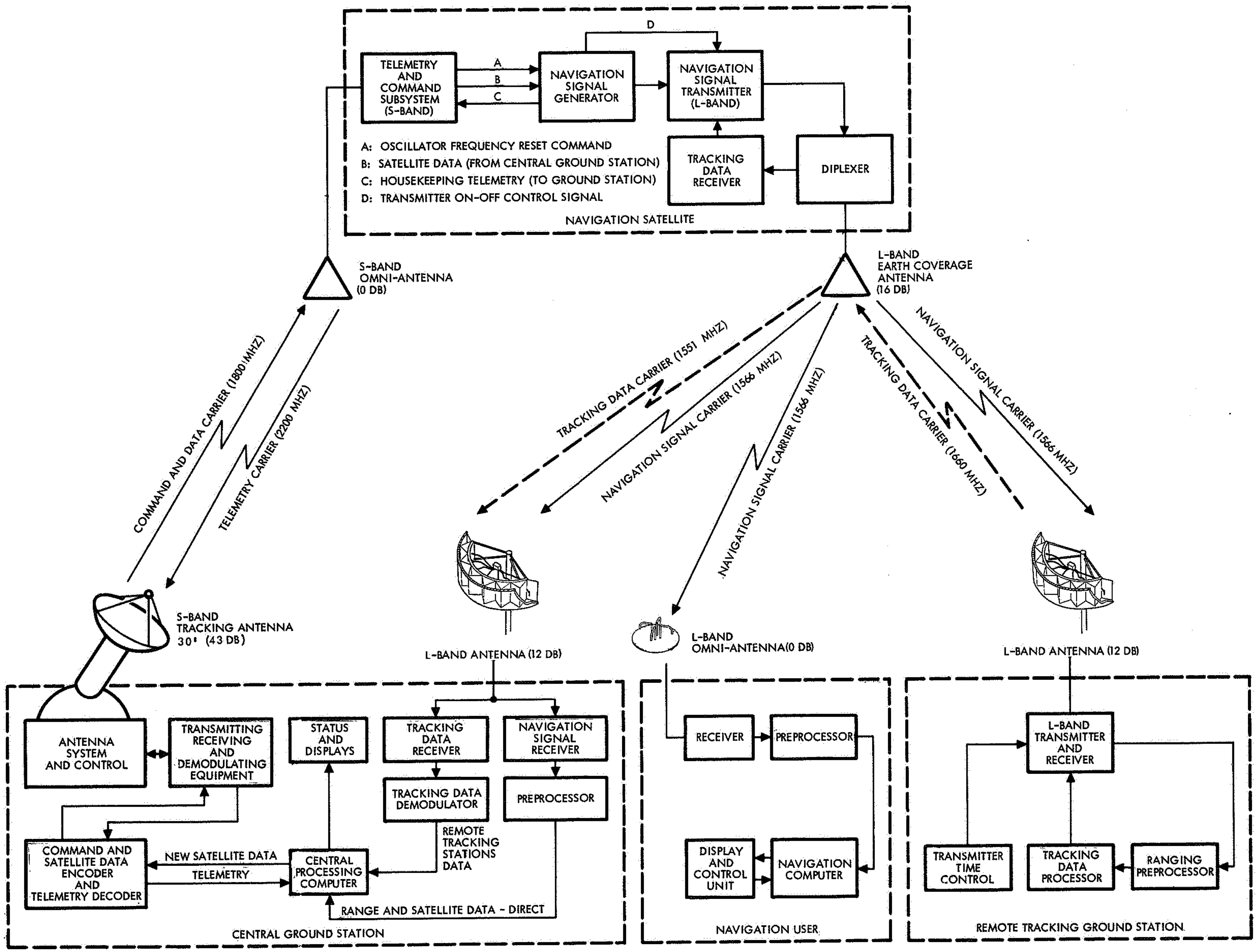


Figure 7. NAVSTAR Signal Flow

4. USER HARDWARE DESCRIPTION

4.1 ANTENNA SUBSYSTEM

4.1.1 INTRODUCTION

4.1.1.1 Scope of Effort

The TRW study effort for a NAVSTAR user antenna design was performed primarily in-house using both analytical and empirical measurement techniques.

Based on the technical skills of TRW's senior antenna designers, previous TRW experience, and an extensive literature review, certain antenna configurations were postulated as candidate systems for the typical NAVSTAR user (see Table VI). The most promising designs were breadboarded and subjected to extensive testing at one of TRW's antenna ranges. These test results were used iteratively to synthesize several desired antenna configurations.

In addition, a survey was conducted throughout the segment of industry which specializes in the manufacture of airborne antenna systems. The purpose of the survey was twofold: (1) to determine the availability of off-the-shelf hardware meeting the specified requirements; and (2) to obtain an estimate of recurring costs for large quantity production of current and projected 1970-1975 designs.

4.1.1.2 Preliminary Specifications

The initial step in this effort was to establish a list of realistic design objectives or preliminary specifications for all subsequent activity. Table VII represents the preliminary specifications derived from round-table discussions between the key participating designers on the TRW NAVSTAR program. Like all subsystem design goals, the NAVSTAR user antenna specifications are the result of extensive tradeoff analyses between a number of interacting parameters. Some of the more important tradeoffs include: satellite transmitter power output and satellite antenna gain as a function of user antenna gain; satellite ground coverage as a function of user antenna radiation pattern; and acquisition time and system complexity as a function of multimode user antenna configurations.

TABLE VI

SUMMARY OF ANTENNA CONFIGURATIONS

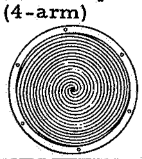
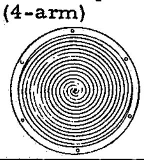
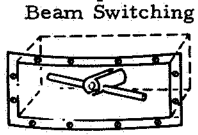
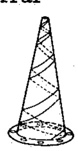
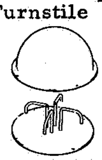
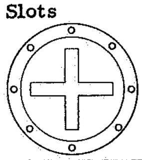
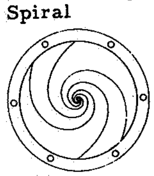
Type	Radiation Pattern	Gain	Axial Ratio (db)	Mounting	Dimension	NAVSTAR User Application	Relative Cost
Planar Spiral (4-arm) 	Directional	6.0 db Peak	<2	Flush	Circular- 8-in. dia	Inadequate	$500.00
Planar Spiral (4-arm) 	Directional	5.3 db Peak	<2	Flush	Circular- 5-in. dia	Inadequate	500.00
Slot Dipoles Beam Switching 	Hemispherical	3-6 db over 160^{o} cone	<5	Flush	7 x 2.5 x 1.9 in.	Supersonic aircraft	975.00
Conical-Log Spiral 	Hemispherical	0 to 5 db over 160^{o} cone	<5	Medium Profile	Cone shape 7-in. height	Subsonic aircraft and marine vessel	200.00
Curved Dipole Turnstile 	Hemispherical	0-4 db over 160^{o} cone	<5	Low Profile	Hemispherical 2-1/2 in. ht. 3-in. rad	Supersonic aircraft	250.00
Curved Cross-Slots 	Hemispherical	0-4 db over 160^{o} cone	<5	Low Profile	Hemispherical 2-in. rad	Supersonic aircraft	250.00
Dome Surface Log Spiral 	Hemispherical	-2 to 4 db over 160^{o} cone	<5	Low Profile	2 in height 2-1/2-in. rad	Supersonic aircraft	300.00

TABLE VII

NAVSTAR USER ANTENNA CHARACTERISTICS

Frequency:	L-band, 1540 to 1600 MHz
Polarization:	Circularly polarized
Axial ratio:	≤5 db
Antenna pattern:	Upper hemispherical, conical beamwidth greater than ±80° about axis
Gain:	≥0 db relative to isotropic
Multipath rejection ratio:	≥10 db
Input VSWR:	<1.5:1 referenced to a 50-ohm impedance
Configuration:	For supersonic aircraft, minimize aerodynamic effects

As with all other user equipment subsystems, the optimizing criterion for selecting one antenna configuration over another is cost. All references to cost in this study refer to the per-unit production cost which the ultimate user will have to pay in order to benefit from the NAVSTAR network.

Table VII lists the basic requirements for the user's antenna system(s) including: near-upper hemispherical coverage having high rejection to lower hemisphere signals; operating frequencies within the L-band and a bandwidth of approximately 5 MHz; antenna gain of at least 0 dbi with respect to a circularly polarized standard over a cone area of 160°; and an axial ratio within 5 db. A further explanation and justification for the specified NAVSTAR User Antenna specification are given below.

4.1.1.2.1 Antenna Gain and Pattern Coverage

The upper hemispherical pattern requirement represents optimum coverage for the user antenna since it will enable the user to receive signals from a greater number of satellites (as many as eight can be seen in certain geographical locations). The additional satellites visible by the user (beyond the minimum of three or four) will, in many instances, improve the system accuracy.

A cone of 160° coverage at 0-dbi gain was considered to be both adequate and practical for the NAVSTAR system described in sec. 3. Subsequent tradeoff analyses between satellite transmitter power, satellite antenna gain, user antenna gain, and user receiver sensitivity confirmed the desirability and reasonableness of the 0-dbi gain figure for the user antenna systems.

In addition, it was felt that the user antenna should have a minimum backlobe so that very little of the noisy earth environment (including multipath) will be illuminated when the antenna is operating in its normal position pointing skyward.

4.1.1.2.2 Polarization

Circular polarization was selected because it possesses desirable characteristics for rejecting multipath signals and provides the best overall system performance in areas of atmospheric and rainfall effects. Multipath rejection is accomplished when reflection from ground or water reverses the sense of circular polarization. The reflected waves with their reversed polarization sense are then partially rejected by the circularly polarized user antenna.

4.1.1.2.3 VSWR

The antenna bandwidth is usually defined as the frequency band for a given VSWR which is the ratio of the antenna impedance to the transmission line impedance. The antenna impedance, which is frequency-dependent, depends on many factors, such as geometry and proximity to surrounding objects. The specified antenna impedance for a NAVSTAR user antenna is established for a VSWR of less than 1.5:1 over a 10-MHz band. This VSWR limit could be improved to perhaps 1.3:1; however, the 1.5:1 value was considered to be consistent with the receiver design and certainly can be realized easily with current antenna design techniques.

4.1.1.2.4 Axial Ratio

The axial ratio of an antenna radiation pattern is an indication of the antenna's circular quality and should be maintained at a small value. As the axial ratio becomes lower, smaller polarization losses result.

For example, based on a 2-db axial ratio for the satellite antenna and a 5-db axial ratio user antenna, the polarization loss will be between 0.1 to 0.68 db. The range of losses will depend on the orientation of the two major axes of the satellite transmit antenna and the user receive antenna. When the two axes coincide, the polarization loss is at a minimum; when the major axes are orthogonal to each other, a maximum polarization loss occurs.

4.1.1.3 Outline of Other Subsections

The subsequent paragraphs of the user antenna study report contain the following subsections:

1) Summary — This subsection presents a brief synopsis of the significant study results and conclusions.

2) Design Approaches — This subsection discusses in some detail the major antenna configurations which were considered during the study.

3) Breadboard Modeling — This subsection presents technical descriptions and test data on several antenna configurations which were breadboarded and tested.

4) Cost — This subsection contains comparative cost data on several candidate antenna systems.

4.1.2 SUMMARY

As a result of this study effort, which included a critical examination of the candidate antenna systems shown in Table VI, several important concepts evolved in the area of NAVSTAR user antenna design. The significant findings discussed further in the subsequent sections are summarized below.

4.1.2.1 Number of User Antenna Configurations

Because a single antenna configuration cannot be optimized for all classes of users and supersonic aircraft cannot tolerate appreciable protrusions due to drag effects above the surface, most candidate systems which are not flush-mounted are eliminated.

4.1.2.2 Coverage Requirement

The 160°-antenna coverage at even 0 dbi represents a very difficult design problem, particularly for the supersonic aircraft application. Most known single-element antenna designs which are flush-mounted will not meet this requirement because of restrictions in the antenna geometry. To obtain reasonably good upper hemispherical coverage, either some form of surface protrusion should be provided, or multi-element antennas should be used.

4.1.2.3 Archimedean Spiral Antenna

The flush-mounted Archimedean spiral design originally proposed was found experimentally to be inadequate for NAVSTAR user applications because of narrow ($\pm 50^{\circ}$ cone) beamwidth limitations. Breadboard modeling has demonstrated that no appreciable improvement in coverage is realized by operation in a dual-mode (normal and axial) configuration.

4.1.2.4 Availability of Off-the-Shelf Hardware

No off-the-shelf antenna systems are available which meet the specified requirements for the supersonic aircraft user. Most companies responding to our industry survey indicated research and development effort (in the area of \$50,000 to \$100,000) would be required before a satisfactory design could be developed.

4.1.2.5 Recommended Design for SST Applications

The antenna design which TRW recommends for the SST is a low profile design of a modified turnstile antenna. This design, which TRW has breadboarded and tested, consists of a pair of curved dipoles mounted approximately 2-1/2 in. above a metal surface. The turnstile antenna configuration utilizes the height and curvature of the arms to produce an antenna pattern of near upper hemispheric coverage. Pattern measurements conducted on a breadboard model have produced encouraging results. However, additional measurements and refinements are required before the present design can be finalized.

4.1.2.6 Recommended Design for Other NAVSTAR Users

For applications where drag is no problem, the antenna design which TRW recommends is the conical log spiral. This antenna configuration is well understood, has wide applicability, and is relatively easy to design and comparatively inexpensive to fabricate.

4.1.2.7 Other Antenna Designs

A beam-switching antenna system was also investigated as a brute-force approach towards solving the SST user requirements with a flush-mounted system. This configuration consists of three slot-dipoles and offers considerably better gain and coverage performance over either the turnstile or conical spiral designs (See Figure 8). The major disadvantages of this design relative to the conical log spiral are cost and system complexity.

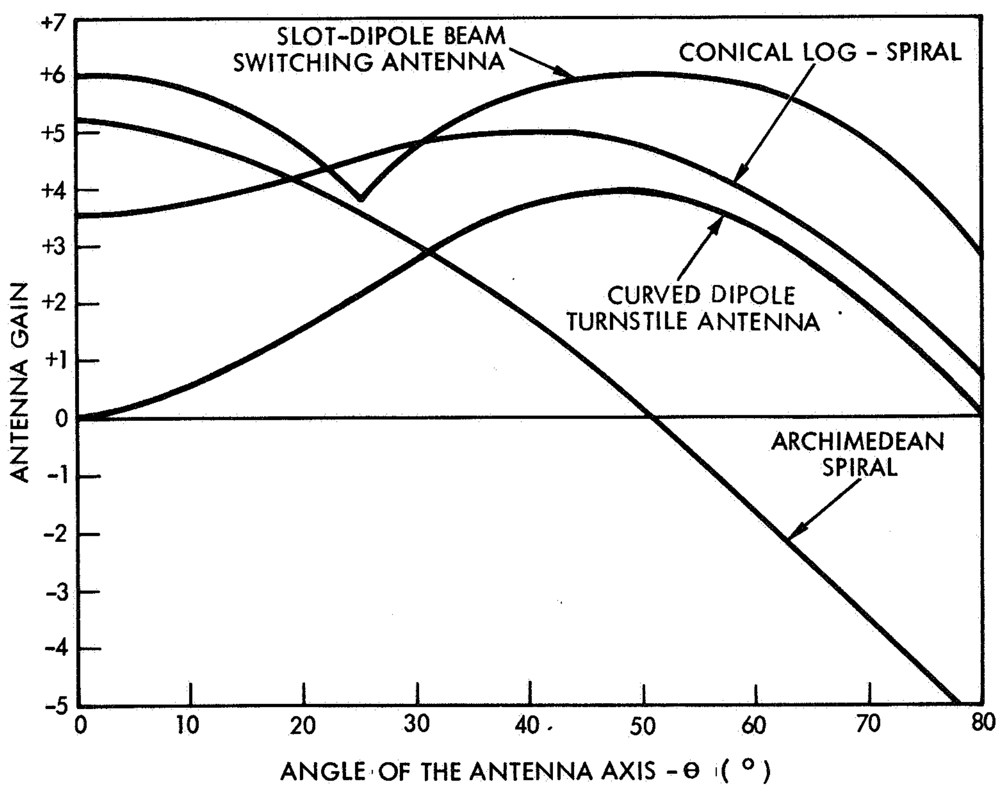


Figure 8. Comparison of User Antenna Design Gain

4.1.2.8 Comparative Costs

Table VIII presents the recurring cost data for candidate NAVSTAR user antenna configurations. The estimates were internally generated and do not include prices for nonrecurring engineering and development.

TABLE VIII

COMPARATIVE COSTS OF CANDIDATE NAVSTAR USER ANTENNAS

Antenna Configuration	Unit Price in Quantities of:		
	100	1000	10,000
Conical log spiral	$250	$210	$200
Curved dipole turnstile	$325	$275	$250
Beam switching (Slot-dipoles)	$975	$825	$785

4.1.3 DESIGN APPROACHES

Early in the study it was determined that no one antenna system could be designed which would optimize performance for all classes of NAVSTAR users. This is immediately obvious when one considers that a circularly polarized antenna system having broad coverage characteristics can be provided most easily by a surface-mounted configuration. Because of aerodynamic drag effects, a different approach had to be taken for the SST user who preferred a system which was either flush-mounted or had minimum surface protrusions.

Consequently, this subsection is correlated with the study effort and presents the TRW activities in the two categories: (1) subsonic aircraft and marine vessel antenna systems, and (2) high-performance supersonic aircraft antenna systems.

4.1.3.1 Subsonic Aircraft and Marine Vessels — Conical Log-Spiral Antenna

Much design information is reported in the literature pertaining to conical log-spiral antennas (see Refs. 2, 8, 9 and 10). This configuration has been demonstrated to possess radiation and impedance characteristics which can be varied at the designer's option. Additionally, this antenna is relatively easy to design and comparatively inexpensive to fabricate.

4.1.3.1.1 <u>Design Parameters</u>

The antenna performance of a conical log-spiral antenna can be properly specified in terms of the following five parameters:

1) Included cone angle, $2\theta_o$

2) Armwidth angle, δ

3) Spiral rate, α

4) Base diameter, D

5) Apex diameter, d

A conical log-spiral antenna with these parameters is shown in Figure 9.

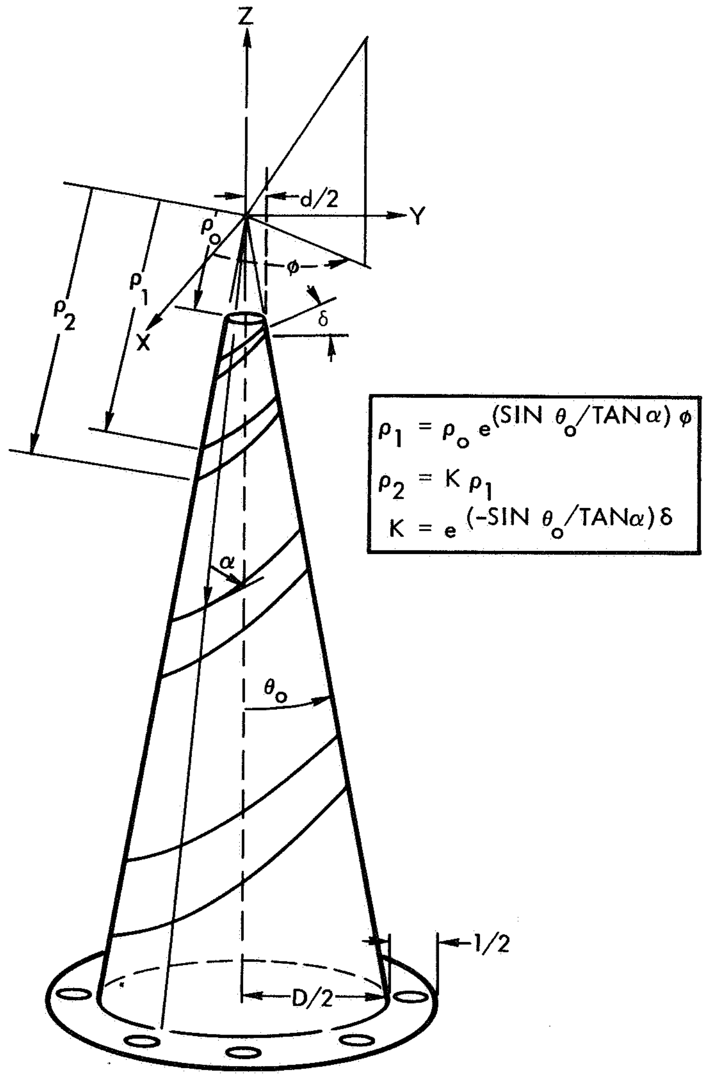


Figure 9. Conical Log-Spiral Antenna

Table IX summarizes performance characteristics for a two-arm configuration, as reported in Ref. 2.

TABLE IX

PERFORMANCE CHARACTERISTICS FOR A TWO-ARM CONFIGURATION

Cone Angle $2\theta_o$ (°)	Spiral Rate α (°)	Beamwidth Half-Power Points (°)
20	82	60 - 70
20	73	70 - 80
20	60	160 - 180
20	45	180 - 200

The apex diameter, d, and the base diameter, D, are normally selected for the highest and lowest frequency of operation.

4.1.3.1.2 Recommended Design Characteristics

For the NAVSTAR user application,the dimensions of the conical log-spiral design should be selected to produce a good axial ratio. This can be accomplished by using the design parameters as presented in Table X.

TABLE X

RECOMMENDED DESIGN PARAMETERS FOR A CONICAL LOG-SPIRAL ANTENNA

$2\theta_o$	$= 20^\circ$
α	$= 60^\circ$
d	= 0.7 in.
D	= 2.7 in.
δ	$= 90^\circ$

4.1.3.1.3 Mounting Considerations

The conical log-spiral design is suitable for mast mounting as well as for normal installation above the aircraft surface. This design is recommended primarily for subsonic aircraft and marine vessel users. However, if space can be made available in the tail region of the aircraft's vertical stabilizer, it should be possible to install the conical antenna system on a supersonic aircraft as well. (This approach may not be practical since all available space in the tail region is generally preempted by higher priority antenna requirements.)

4.1.3.1.4 Related TRW Experience

TRW has achieved excellent results on current military programs for a design of a conical log-spiral antenna operating in S-band (a typical antenna pattern is shown in Pattern No. 1, Figure 16). Its significant characteristics include the following:

1) Maximum gain of +5 dbi at 0°

2) 2 dbi gain over 140° and -0.5 dbi gain over 160°

3) Axial ratio within 4 db.

The gain measurements have included losses through the fiberglass radome.

4.1.3.1.5 Summary

Based on the empirical data indicated above and the parameters specified in par. 4.1.3.1.2, it can be shown that for an L-band design the conical log-spiral antenna will meet more than adequately all specified design objectives. In particular, the expected gain will be 0 db over the entire 160° cone of coverage with the axial ratio within 5 db.

4.1.3.2 Supersonic Aircraft

4.1.3.2.1 Archimedean Spiral Antenna

Four-Arm Spiral. Major emphasis was given initially to a cavity-backed, four-arm spiral antenna as a design approach for supersonic aircraft. By dual feeding the four-arm spiral antenna, a sum-and-difference pattern of circular polarization could be obtained for the same radiating element. By arranging the applied excitation for in-phase or out-of-phase currents, two modes of pattern generation could be achieved:

1) Axial Mode — This radiation pattern is represented by a single lobe with maximum field along the axis of the antenna. The pattern is obtained by exciting the spiral arms to produce in-phase currents.

2) Normal Mode — Another radiation pattern with a minimum field on-axis and maximum field off the antenna axis is obtained by exciting the spiral arms out of phase.

The antenna configuration, its associated excitation network, and the dual mode pattern characteristics are illustrated in Figures 10 and 11. By switching between the two modes, it was initially predicted that the gain coverage would be adequate for the NAVSTAR user application.

Subsequently, a two-arm spiral was laboratory-tested to demonstrate the anticipated characteristics. The results are described more fully in par. 4.1.4.1.

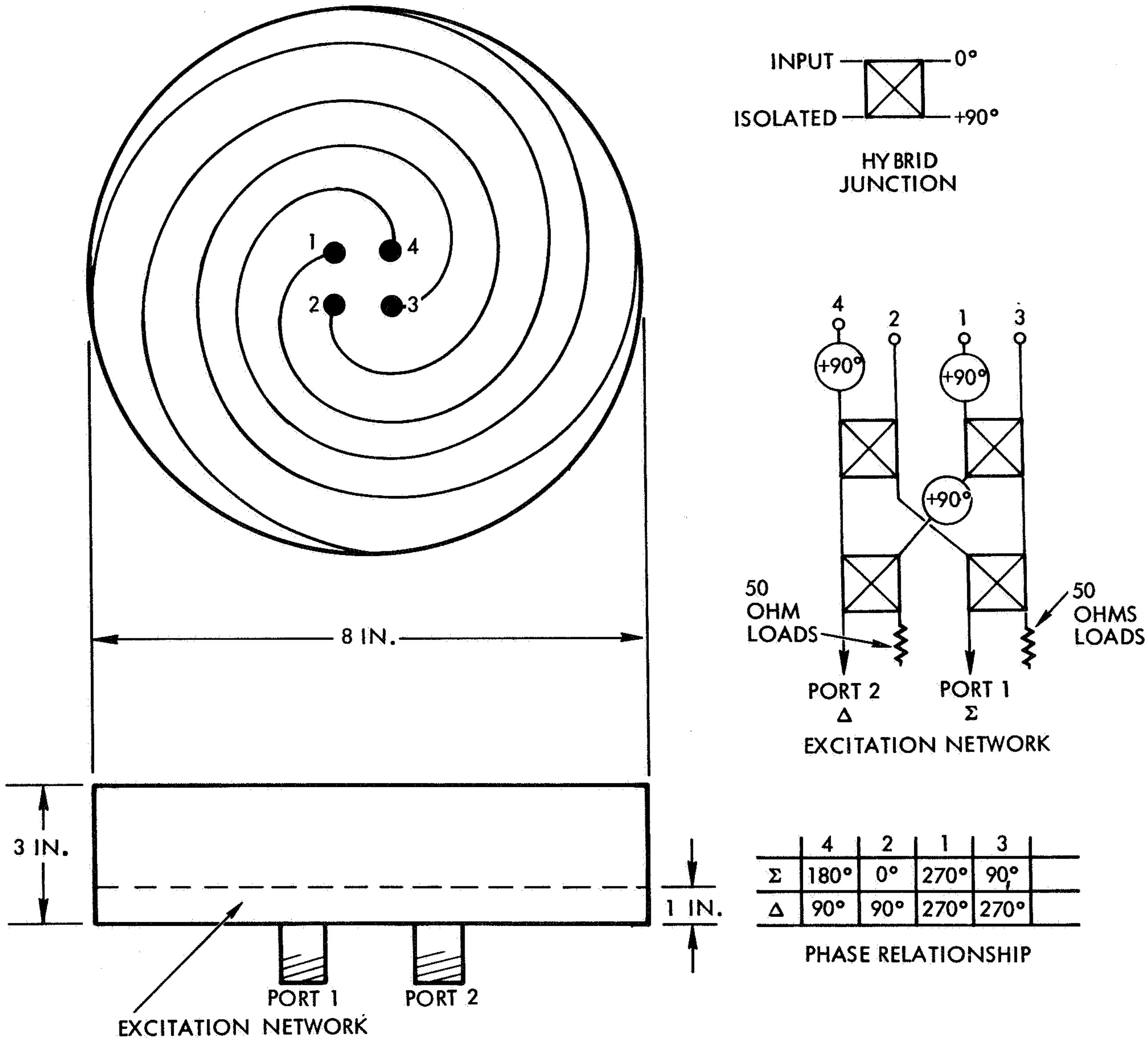
Two-Arm Spiral. Since the two-arm spiral antenna was readily available in-house it was used for the laboratory testing. However, the pattern characteristics of the two-arm design resemble, in many respects, those of the four-arm configuration. The basic difference between the two is in the manner of excitation required to generate the sum and difference patterns. The excitation circuit along with the antenna dimensions and detailed test results are presented in par. 4.1.4.2.

The test results on the Archimedean spiral antenna design show only a slight improvement in coverage achieved by dual-mode operation. Gain/pattern measurements show a -4 dbi gain over a 160° cone of coverage. Consequently, it was concluded that the dual-mode spiral design (whether two-arm or four-arm) is inadequate for the NAVSTAR user applications.

4.1.3.2.2 Curved Dipoles Turnstile Antenna

This antenna configuration consists of a pair of curved dipoles mounted approximately 2-1/2 in. above a ground plane. The overall dimensions of the antenna are shown in Figure 12.

The operating principle of this antenna is similar to the conventional flat turnstile antenna where equal magnitude quadrature currents are required from the orthogonal dipoles to produce circular polarized radiation. The subject antenna uses a 90° hybrid coupler to provide the



	4	2	1	3
Σ	180°	0°	270°	90°
Δ	90°	90°	270°	270°

PHASE RELATIONSHIP

PORT 1 - RECEIVE AXIAL MODE ANTENNA PATTERN
PORT 2 - RECEIVE NORMAL TOROIDAL BEAM PATTERN

Figure 10. Four-Arm Spiral Antenna and Associated Excitation Network

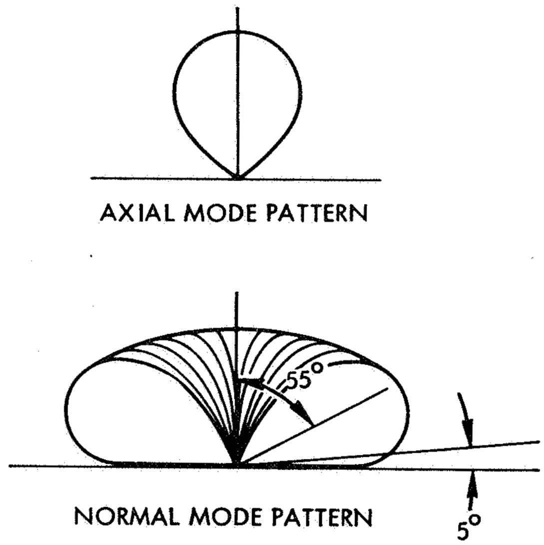


Figure 11. Archimedean-Spiral Antenna Pattern Modes

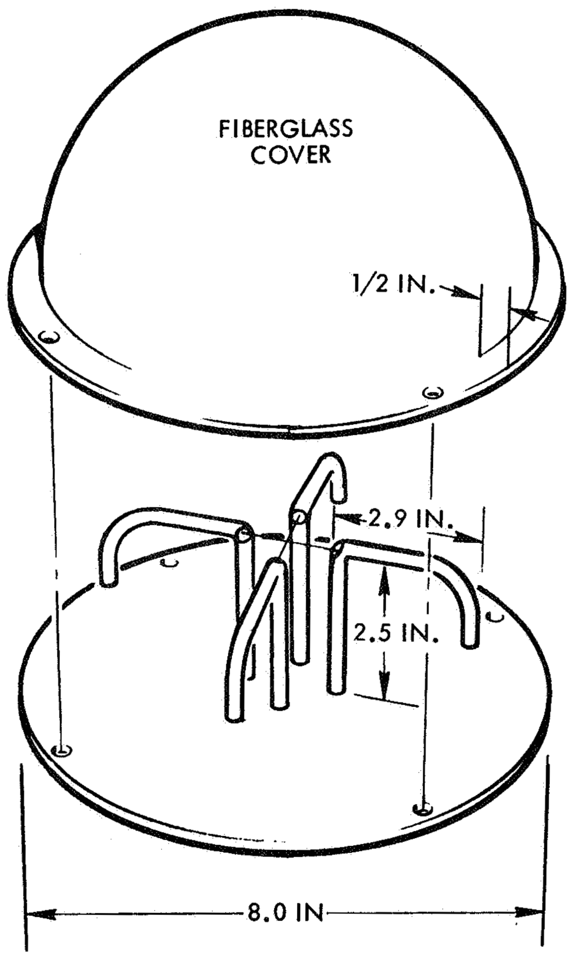


Figure 12. Curved Dipole Turnstile Antenna

necessary quadrature current relationship. The 2-1/2 in. height and the curved arms were carefully selected to give a broad pattern uniformly distributed in the front of the antenna. The conventional turnstile design using flat dipoles provides very poor radiation patterns (high axial ratio) for large angle off-the-antenna axis. This condition prevails since the flat dipoles design is insensitive to vertical fields from high angles off the antenna axis. By curving the dipoles, however, the vertical field is properly received.

Preliminary pattern measurements on a curved arm turnstile design using a very crude model have yielded encouraging results. The breadboard model exhibited a very high VSWR of 9:1 at a test frequency of 1.5 kMHz and the principal plane patterns were not symmetrical. Consequently, the antenna model did not perform optimally. However, the pattern results demonstrated that the antenna can receive vertical fields as well as horizontal fields over the cone angle of 160°.

By careful construction and determination that the two crossed elements are identical and in proper phase relationship, the design is expected to produce a near hemispheric coverage. The antenna should have a minimum gain of +0 dbi over the 160° cone and an axial ratio within 5 db. These performance predictions are based on the E- and H-plane patterns measured on the individual dipole. For further details see sec. 4.1.4.

4.1.3.2.3 <u>Slot-Dipole Beam Switching Antenna</u>

Another candidate antenna design for the supersonic aircraft user which is flush mountable is a beam switching system with three slot-dipole antennas. A typical configuration is shown in Figure 13. (See Ref. 4.)

The slot-dipole element produces circular polarization in a rectangular slot by placing a parasitic dipole in the aperture plane. The slot-dipole element has the normal slot pattern of a very broad fan beam, which is particularly useful in designing beam switching systems for broad coverage applications. For the configuration shown in Figure 13, the gain should be at least 3 dbi over a circular isotropic source and over a 160° cone.

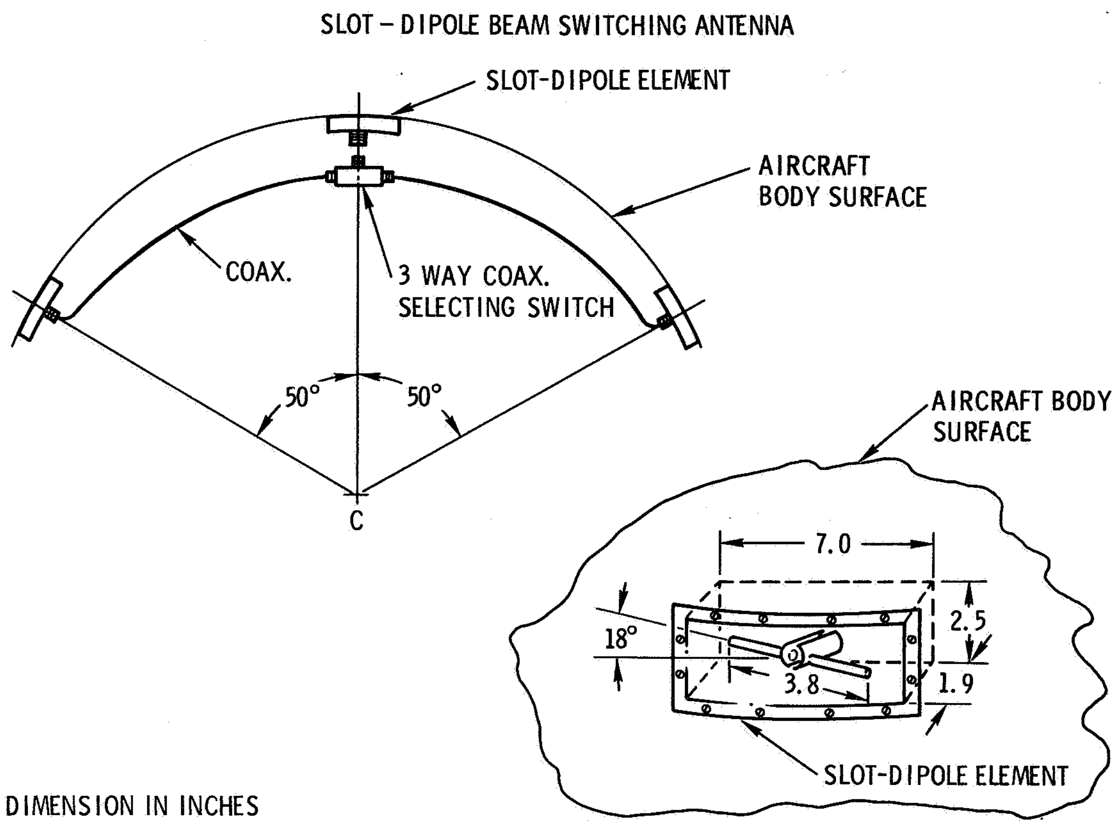


Figure 13. Slot-Dipole Beam Switching Antenna

Only the highest performance aircraft will require this antenna. It can be expected that the SST class of user will also carry an inertial system for attitude reference redundancy, and interpolation. The initial data can readily be used to switch between antennas. Alternatively, an RF sensor could be used. In any event, this configuration yields better gain and coverage than any other antenna considered.

4.1.4 BREADBOARD MODELING

Early in the study it became apparent that the NAVSTAR user antenna design for the supersonic aircraft application was not trivial. Gathering empirical data through breadboard modeling became necessary in order to verify the predicted performance capabilities of the more promising candidate antenna systems.

Of the two antenna configurations tested (i.e., the two-arm Archimedean spiral and the curved dipoles turnstile) most of the effort was devoted to the former design since it was originally proposed and had sound theoretical bases. However, sufficient data was collected on the second configuration to justify the stated conclusions.

The breadboard construction, test methods, and results are presented in the succeeding sections. (See Figures 14 through 55.)

4.1.4.1 Cavity-Backed, Archimedean Spiral

A picture of the spiral test model is shown in Figure 14. A spiral element is mounted at the mouth of a closed-back cavity. The spiral diameter as measured across the mouth of the cavity is 6 in. The cavity depth is 2 in. Pattern measurements were first made with the spiral excited by a colinear balun to obtain axial mode (Mode 1) patterns. (See Figures 17 through 25, patterns 2 to 11.) The excitation circuit for axial mode pattern is shown in Figure 14. The balun was mounted externally to the cavity. A rotating, linearly polarized transmitting source was used while the patterns were being recorded. Therefore, the axial ratio information may be obtained from the individual pattern directly. With the spiral excited by a colinear balun, principal

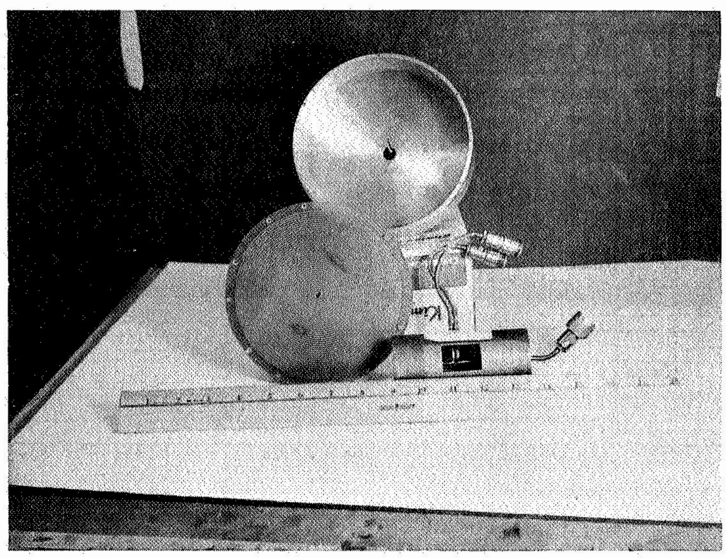


Figure 14. Cavity-Backed Archimedean Spiral (Mode 1, Test Model)

patterns were recorded over the frequency range of 1560 to 1640 MHz in 40 MHz increments (patterns 2 through 5). Patterns were also recorded on a rectangular chart for two frequencies: 1560 MHz and 1600 MHz (patterns 5 and 6). In addition, conical patterns were recorded in 20^{o} increments for a frequency of 1560 MHz (patterns 7 to 11). These patterns exhibit a $\cos^3\theta$ type of beam with a half-power beamwidth of approximately 75^{o}. The axial ratio is within 1 db over the 160^{o} cone. A $\cos^3\theta$ pattern theoretically should have 9 db in directivity. Because of unavoidable losses associated with a balun, stripline dielectric backing, and cavity arrangement, the on-axis antenna gain was measured to be +5.3 dbi.

Patterns were again measured with the test antenna excited in an unbalanced manner to obtain patterns with a maximum field off the antenna axes, a Mode 2 pattern for the spiral. The excitation configuration is shown in Figure 15. The recorded patterns are shown in patterns 12 to 21. Patterns 12 to 14 are principal plane patterns for frequency range of 1560 to 1640 MHz in 40 steps. Patterns 15 to 18 are 20^{o} steps in conical cut patterns. In addition, rectangular recording was made for frequencies 1560 and 1600 MHz (patterns 19 to 21). Pattern 20 is recorded

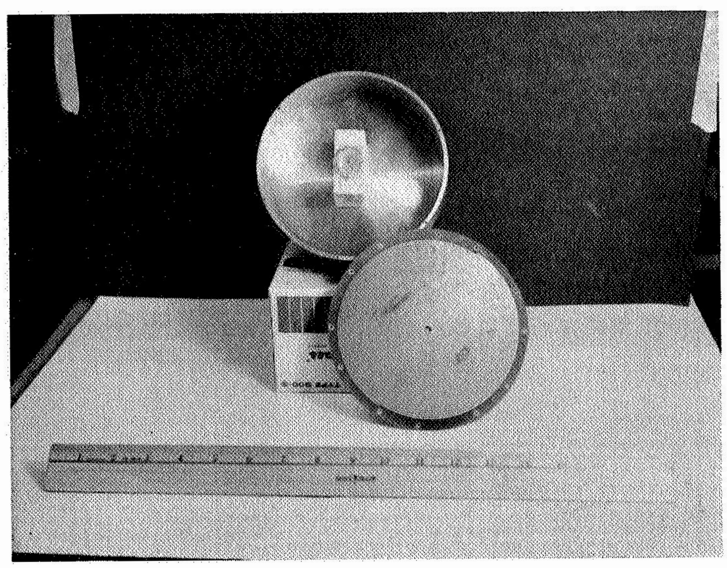


Figure 15. Cavity-Backed Archimedean Spiral (Mode 2, Test Model)

in an identical condition to pattern 19 except the antenna was mounted on a 3-ft square ground plane. The result shows that the ground plane tends to make the pattern more directional and also increases the axial ratio from 2 db to 10 db. The antenna model had a VSWR of 1.3:1 at 1560 MHz. Gain measurement was conducted at 1560 MHz using a linear standard horn for comparison and then converted to a gain with respect to a circular polarized source. The peak gain was determined to be 0 dbi. It occurs approximately 40° off the antenna axis.

By comparing pattern 5 with pattern 19 and noting the respective peak gain level, it is seen that there is little advantage in operating the spiral in a dual-mode. The Mode 1 pattern has almost as wide a pattern as the Mode 2. (The pattern study results are plotted in Figure 8 for comparison with other designs.)

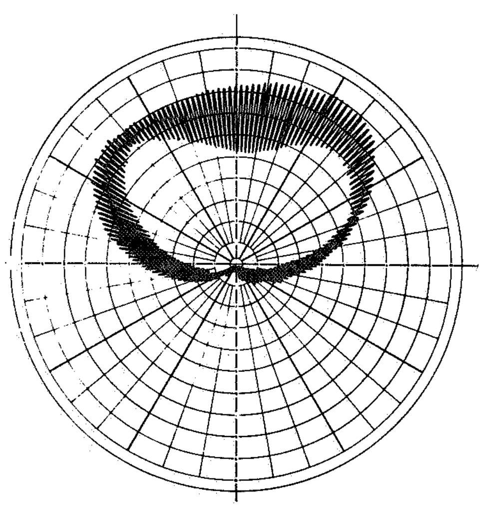


Figure 16. Pattern No. 1, TRW S-Band Conical Log-Spiral $\phi = 0^{\circ}$, Var. θ

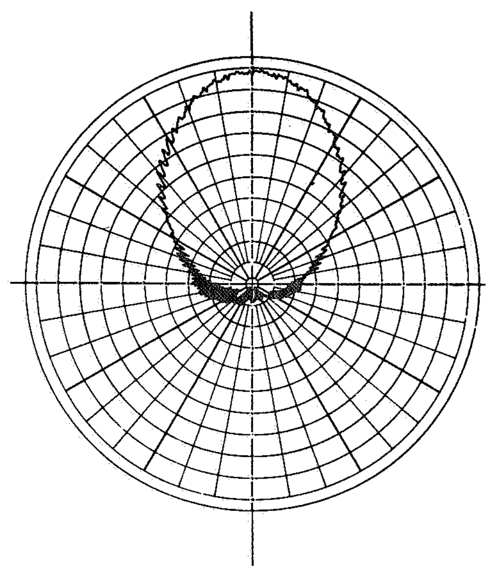


Figure 17. Pattern No. 2, Archimedean Spiral, (Mode 1 excitation), 1560 MHz, Var. θ, $\phi = 0^{\circ}$

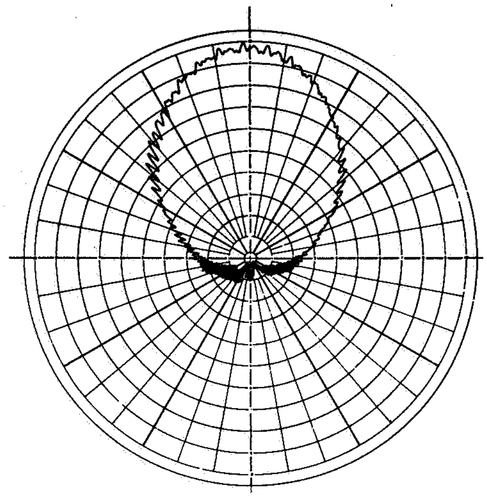


Figure 18. Pattern No. 3, Archimedean Spiral, (Mode 1 excitation), 1600 MHz, Var. θ, $\phi = 0^o$

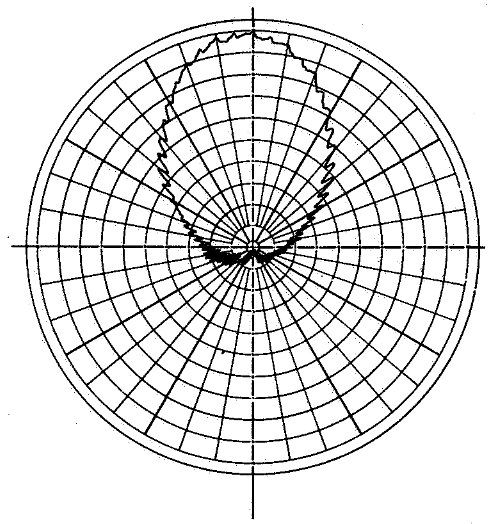


Figure 19. Pattern No. 4, (Mode 1 excitation), 1640 MHz, Var. θ, $\phi = 0^o$

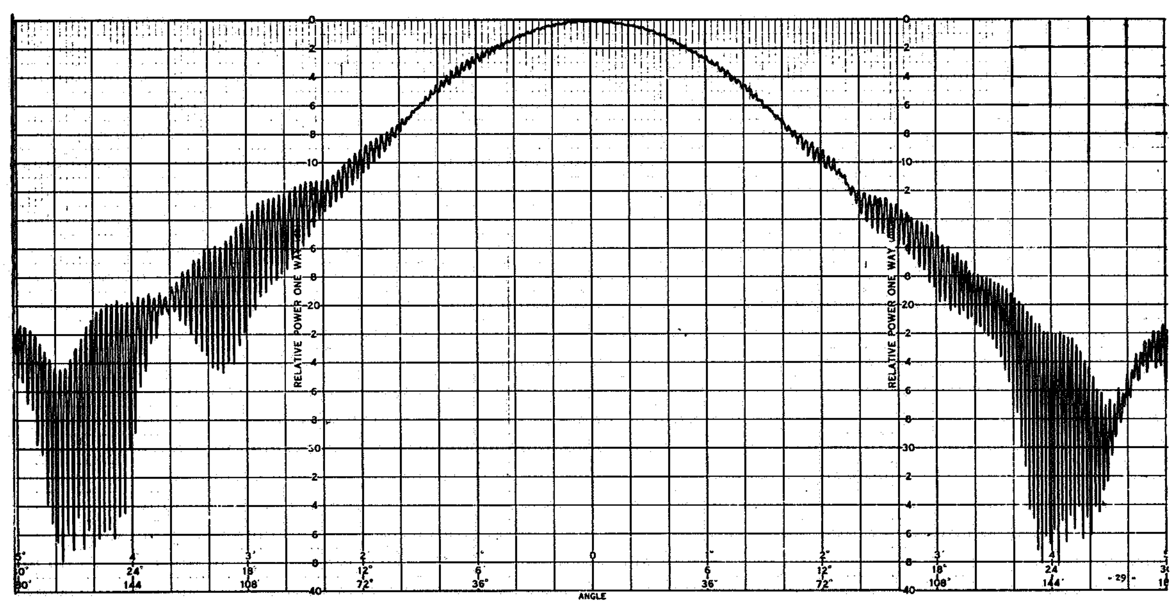


Figure 20. Pattern No. 5, Archimedean Spiral (Mode 1), 1560 MHz, Var. θ, $\phi = 0^o$

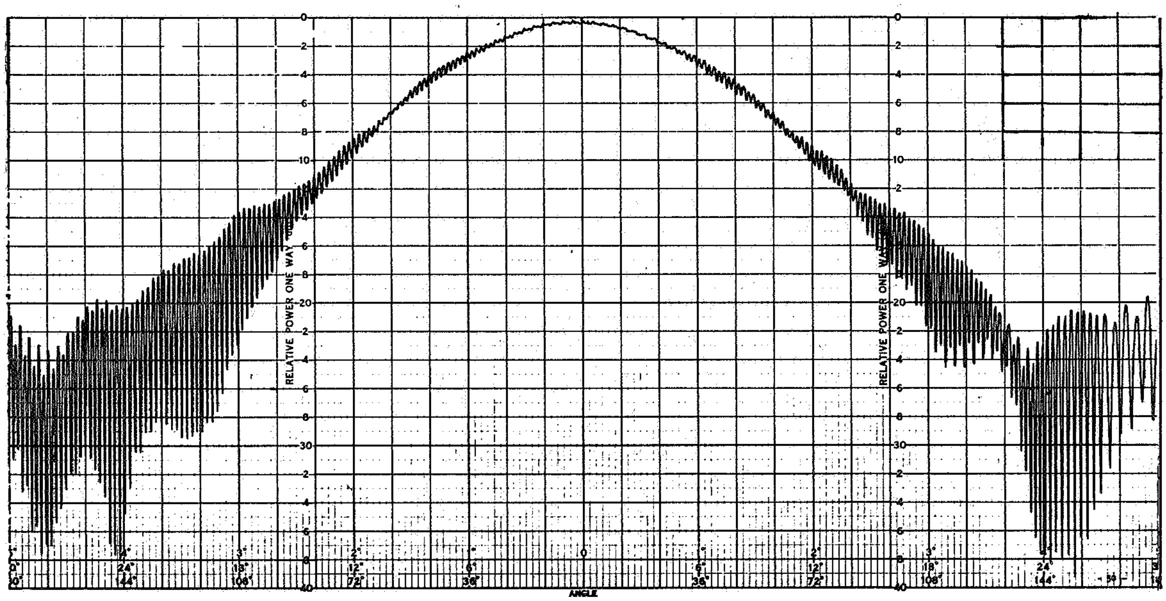


Figure 21. Pattern No. 6, Archimedean Spiral (Mode 1) 1600 MHz, Var. θ, $\phi = 0^{o}$

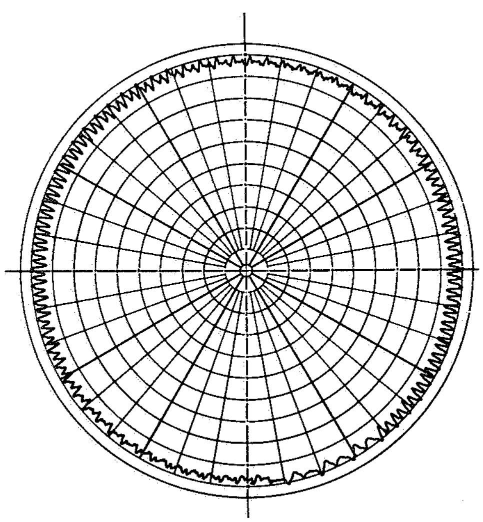


Figure 22. Pattern No. 7, Archimedean Spiral, (Mode 1), Conical Cut, 1560 MHz, Var. θ, $\phi = 0^{o}$

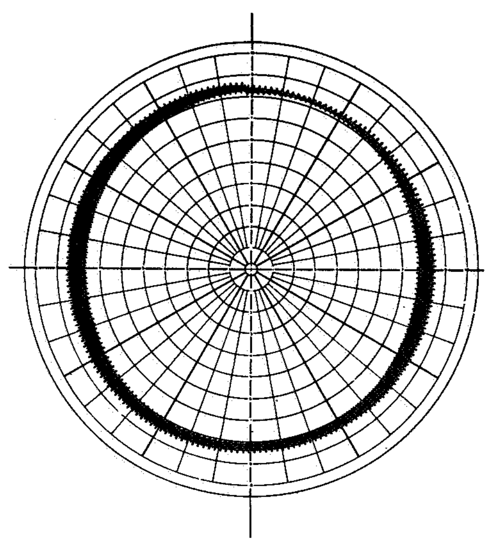


Figure 23. Pattern No. 8, Archimedean Spiral, (Mode 1), Conical Cut, 1560 MHz, Var. θ, $\phi = 20^{o}$

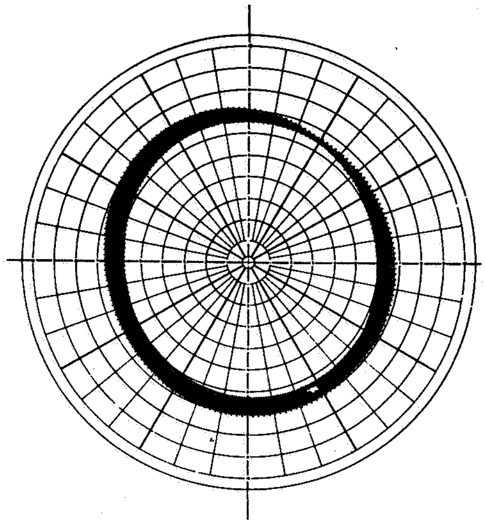


Figure 24. Pattern No. 9, Archimedean Spiral, (Mode 1), Conical Cut, 1560 MHz, Var. θ, $\phi = 40^{o}$

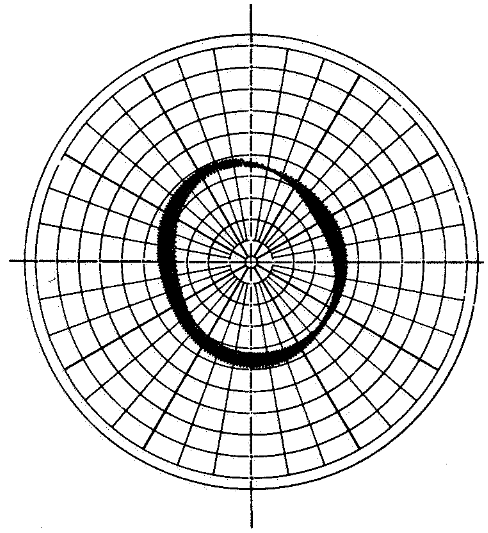


Figure 25. Pattern No. 10, Archimedean Spiral, (Mode 1), Conical Cut, 1560 MHz, Var. θ, $\phi = 60^{o}$

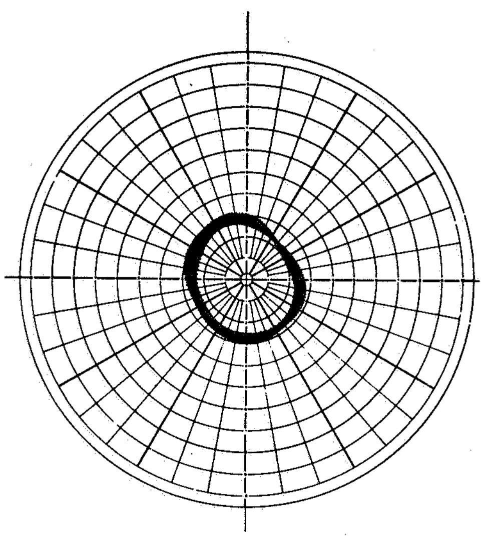


Figure 26. Pattern No. 11, Archimedean Spiral, (Mode 1), Conical Cut, 1560 MHz, Var. θ, $\phi = 80^{o}$

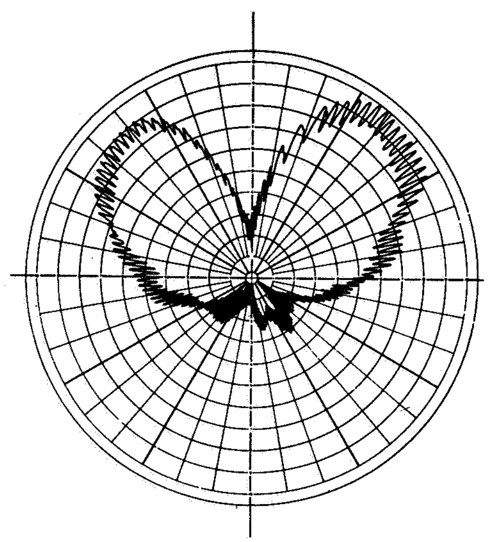


Figure 27. Pattern No. 12, Archimedean Spiral, (Mode 2), 1560 MHz, Var. θ, $\phi = 0^{o}$

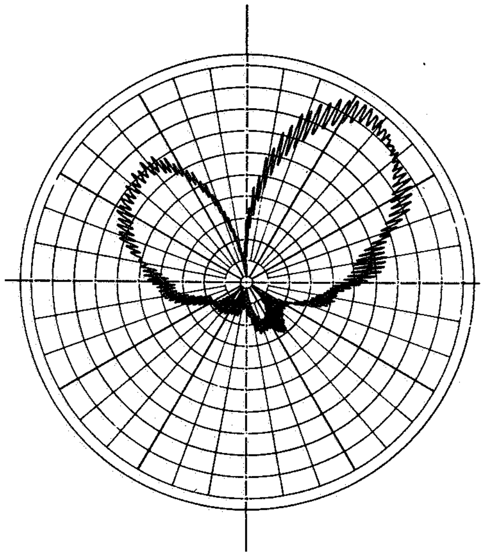


Figure 28. Pattern No. 13, Archimedean Spiral, (Mode 2), 1600 MHz, Var. θ, $\phi = 0^{o}$

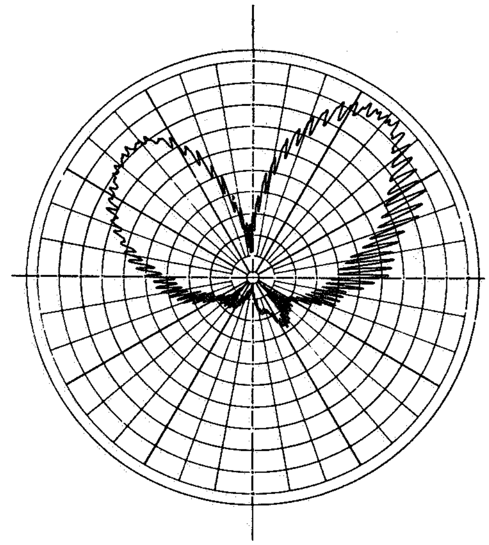


Figure 29. Pattern No. 14, Archimedean Spiral, (Mode 2), 1640 MHz, Var. θ, $\phi = 0^{o}$

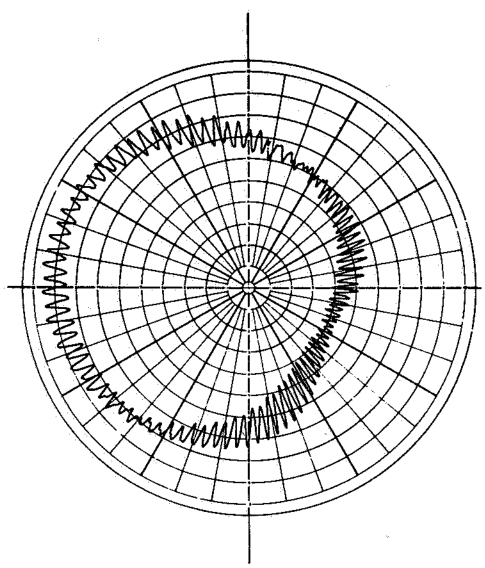


Figure 30. Pattern No. 15, Archimedean Spiral, (Mode 2), 1560 MHz, Var. θ, $\phi = 20^{o}$

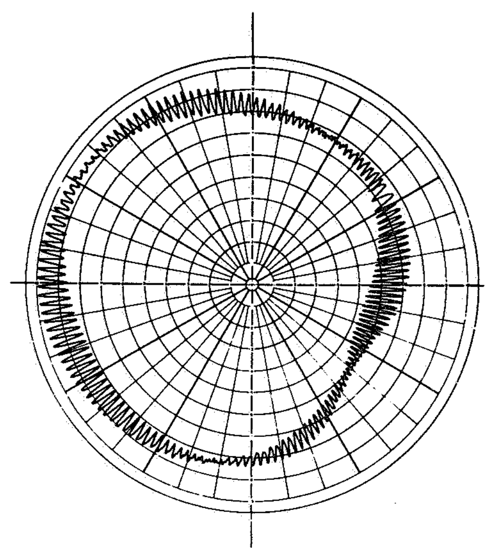


Figure 31. Pattern No. 16, Archimedean Spiral, (Mode 2), 1560 MHz, Var. θ, $\phi = 40^{o}$

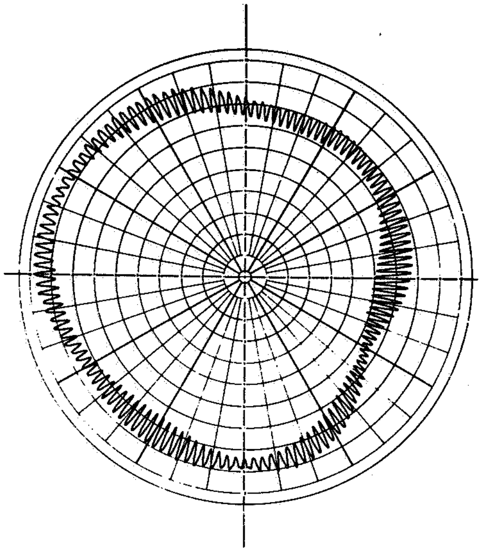


Figure 32. Pattern No. 17, Archimedean Spiral, (Mode 2), 1560 MHz, Var. θ, ϕ = 60°

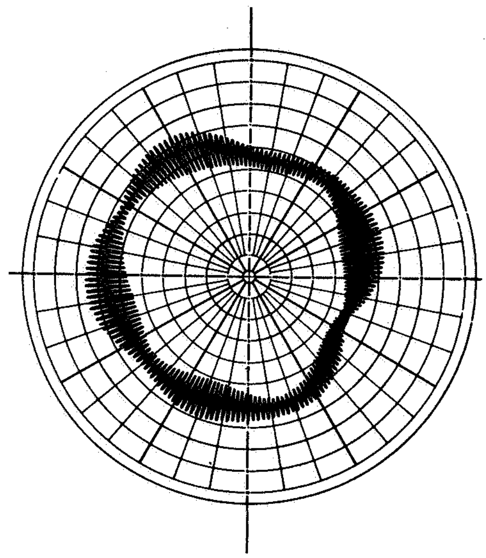


Figure 33. Pattern No. 18, Archimedean Spiral, (Mode 2), 1560 MHz, Var. θ, ϕ = 80°

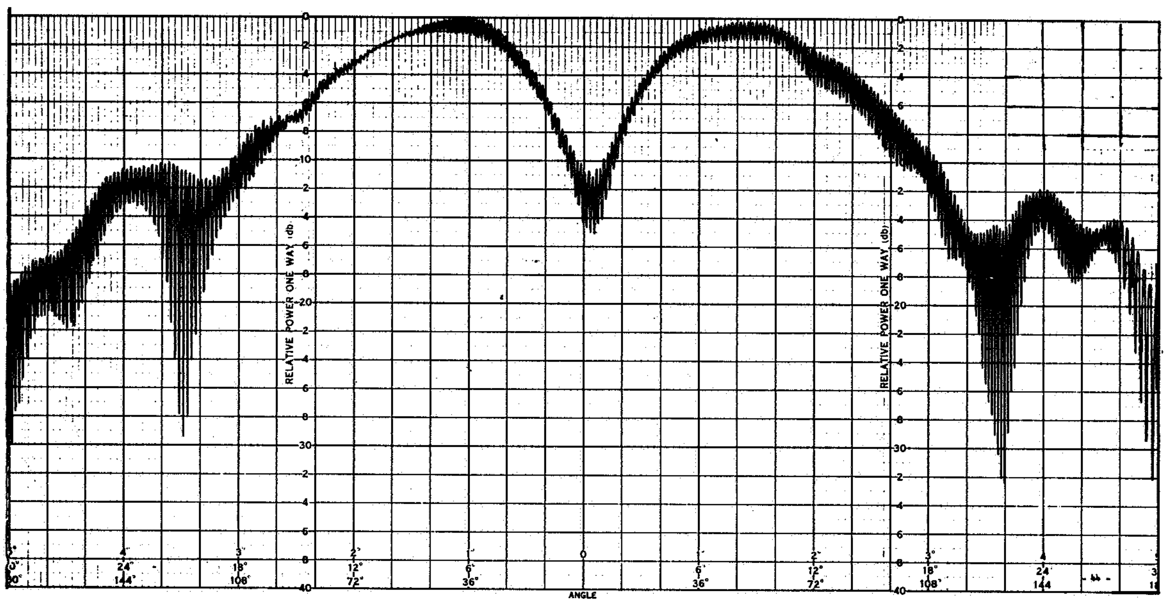


Figure 34. Pattern No. 19, Archimedean Spiral, (Mode 2), 1560 MHz, Var. θ, ϕ = 0°

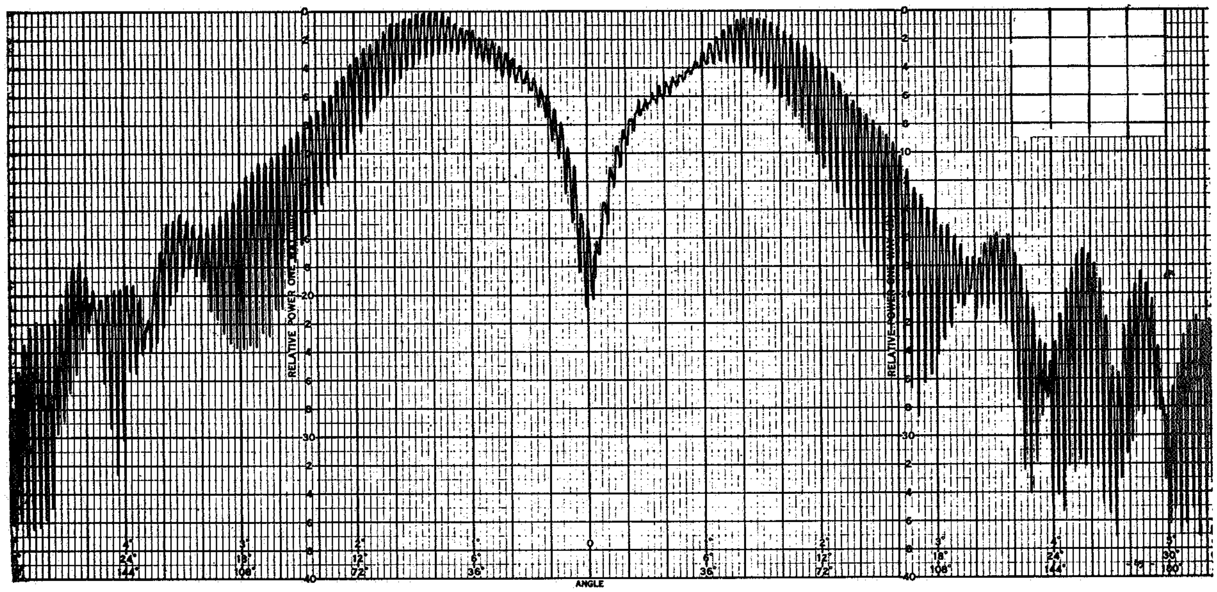


Figure 35. Pattern No. 20, Archimedean Spiral, (Mode 2), On 3' square ground plane, 1560 MHz, Var. θ, $\phi = 0^o$

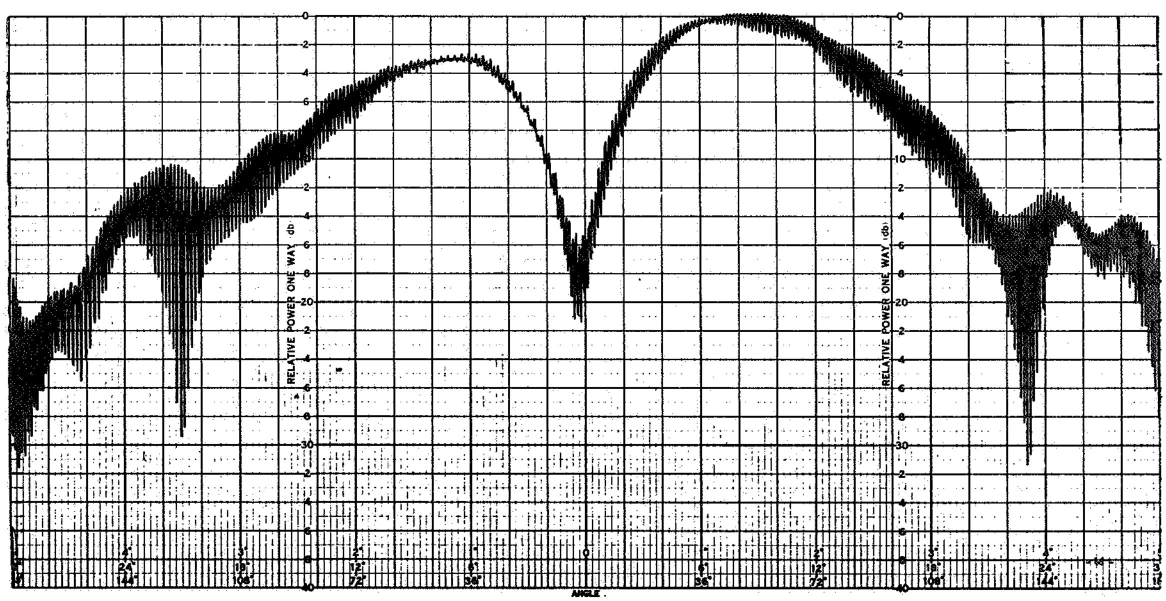


Figure 36. Pattern No. 21, Archimedean Spiral (Mode 2), 1600 MHz, Var. θ, $\phi = 0^o$

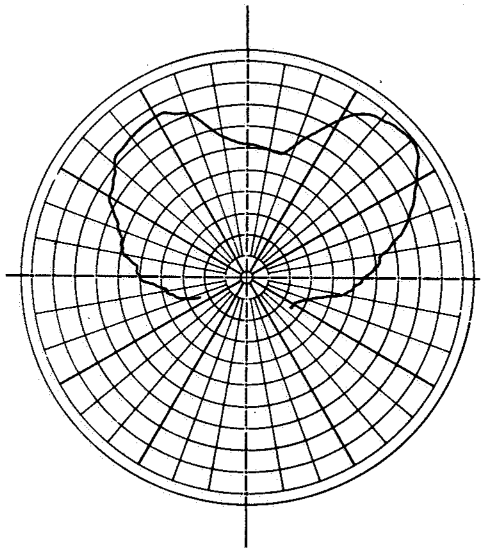


Figure 37. Pattern No. 22, Curved Dipole Turnstile Antenna E - Plane Pattern with Orthogonal dipole terminated, 1500 MHz,

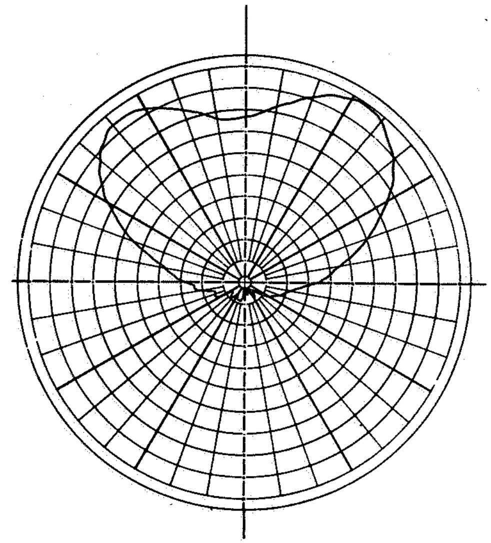


Figure 38. Pattern No. 23, Curved Dipole Turnstile Antenna H - Plane Pattern with Orthogonal dipole terminated, 1500 MHz,

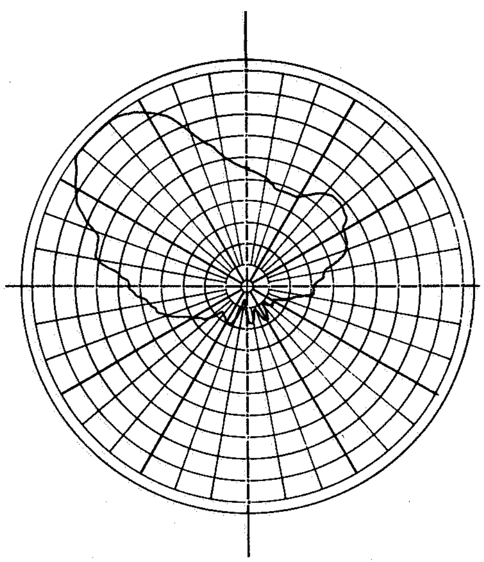


Figure 39. Pattern No. 24, Curved Dipole Turnstile Antenna, 1500 MHz, Vertical Polarization, Var. θ, $\phi = 0^{\circ}$

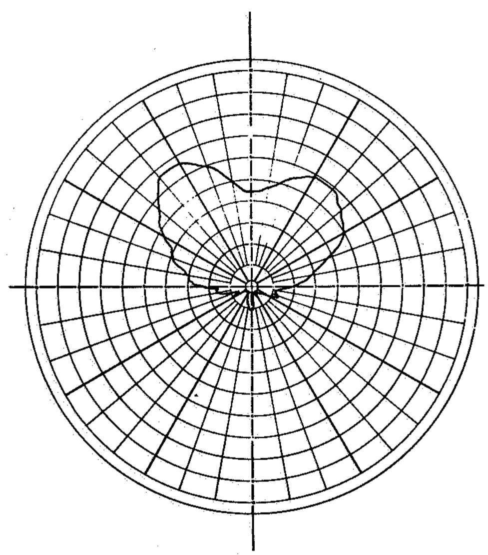


Figure 40. Pattern No. 25, Curved Dipole Turnstile Antenna, 1500 MHz, Horizontal Polarization, Var. θ, $\phi = 0^{\circ}$

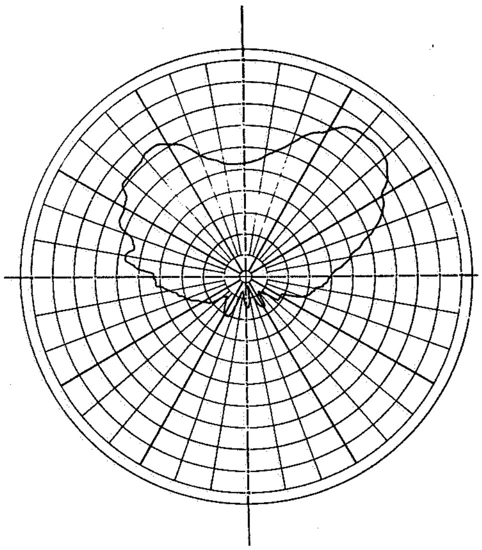


Figure 41. Pattern No. 26, Curved Dipole Turnstile Antenna, 1500 MHz, Vertical Polarization, Var. θ, $\phi = 45^{\circ}$

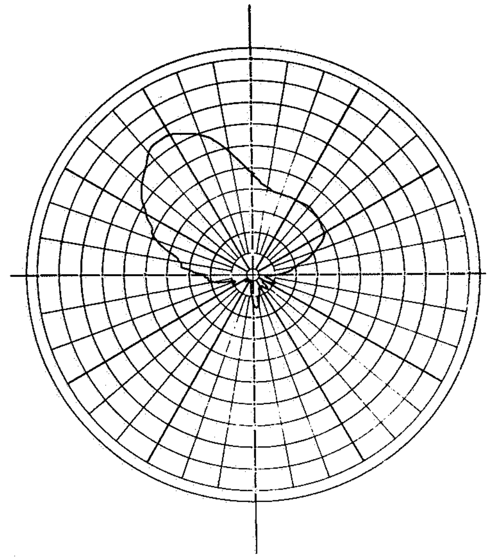


Figure 42. Pattern No. 27, Curved Dipole Turnstile Antenna, 1500 MHz, Horizontal Polarization, Var. θ, $\phi = 45^{\circ}$

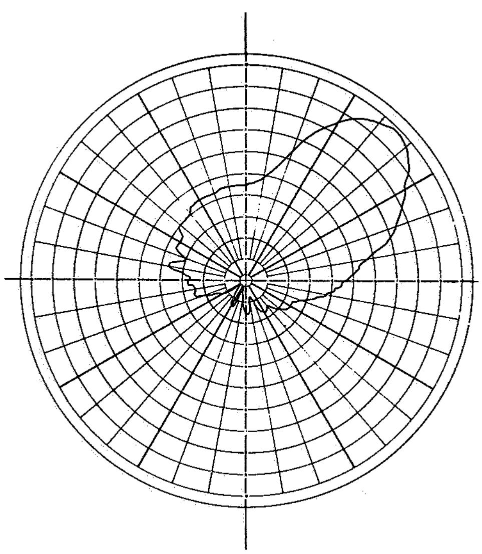


Figure 43. Pattern No. 28, Curved Dipole Turnstile Antenna, 1500 MHz, Vertical Polarization, Var. θ, $\phi = 90^{\circ}$

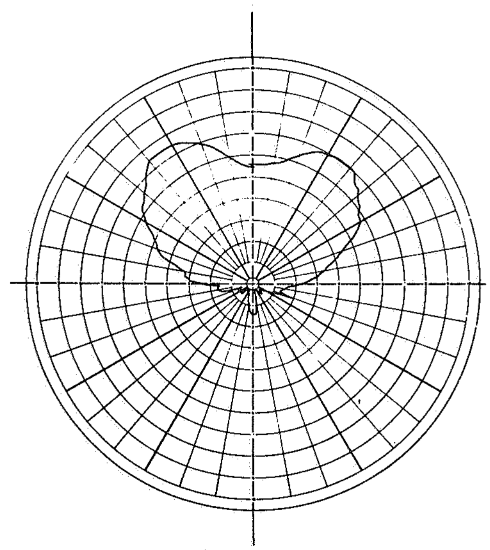


Figure 44. Pattern No. 29, Curved Dipole Turnstile Antenna, 1500 MHz, Horizontal Polarization, Var. θ, $\phi = 90^{\circ}$

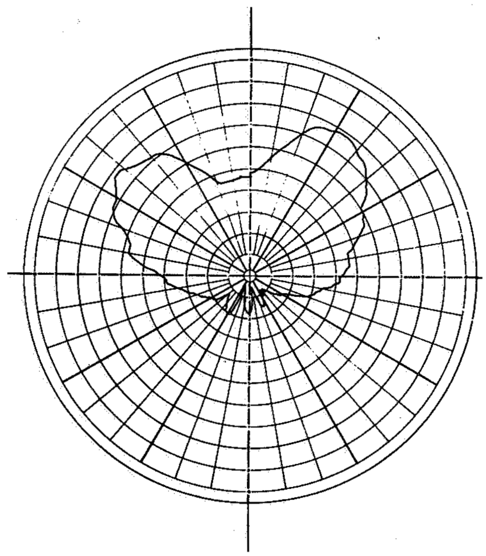


Figure 45. Pattern No. 30, Curved Dipole Turnstile Antenna, 1500 MHz, Vertical Polarization, Var. θ, ϕ = 135°

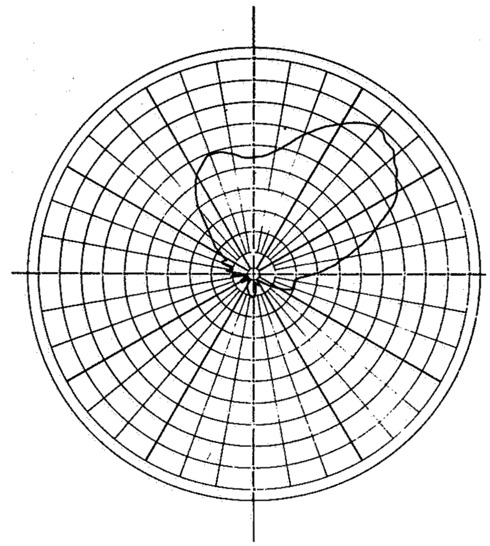


Figure 46. Pattern No. 31, Curved Dipole Turnstile Antenna, 1500 MHz, Horizontal Polarization, Var. θ, ϕ = 135°

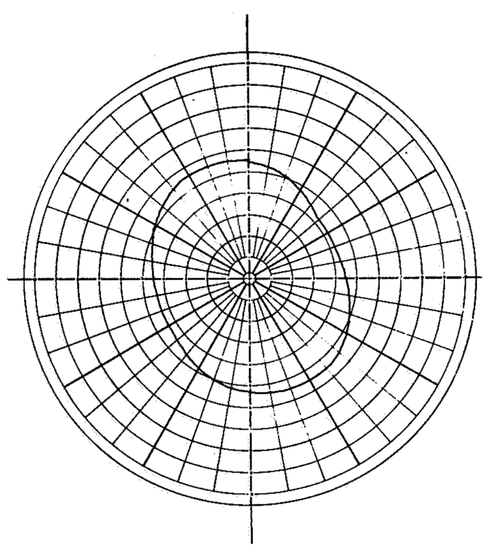


Figure 47. Pattern No. 32, Curved Dipole Turnstile Antenna Conical Cut, 1500 MHz, Vertical Polarization, Var. θ, ϕ = 0°

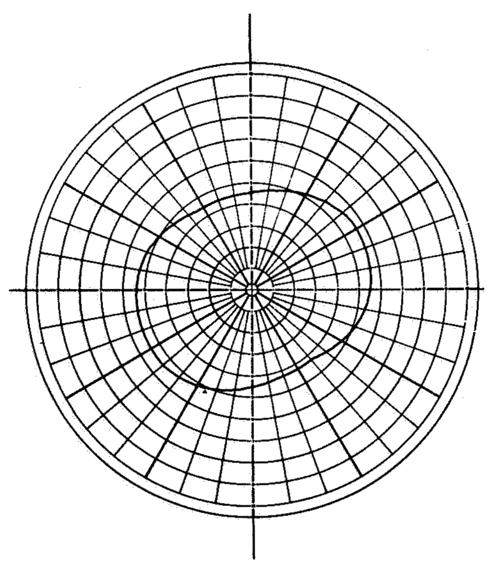


Figure 48. Pattern No. 33, Curved Dipole Turnstile Antenna Conical Cut, 1500 MHz, Horizontal Polarization, Var. θ, ϕ = 0°

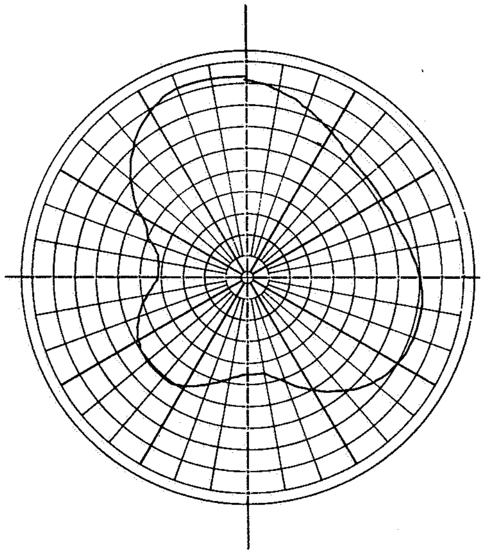


Figure 49. Pattern No. 34, Curved Dipole Turnstile Antenna Conical Cut, 1500 MHz, Vertical Polarization, Var. θ, $\phi = 30^{o}$

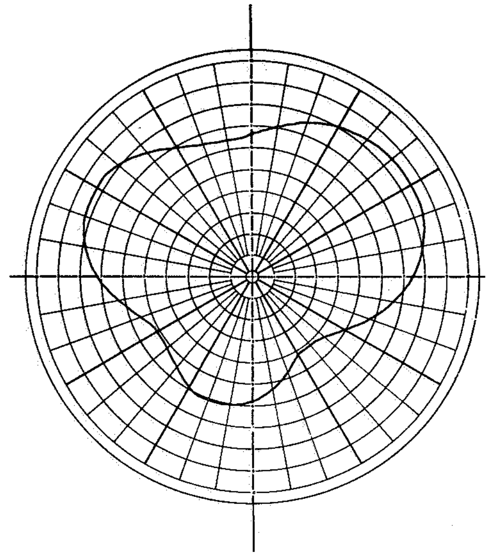


Figure 50. Pattern No. 35, Curved Dipole Turnstile Antenna Conical Cut, 1500 MHz, Horizontal Polarization, Var. θ, $\phi = 30^{o}$

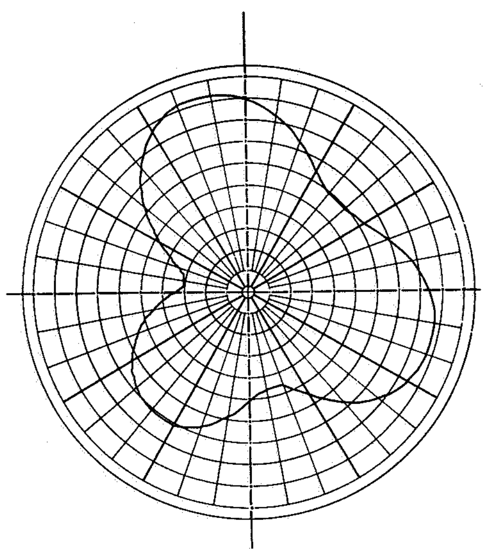


Figure 51. Pattern No. 36, Curved Dipole Turnstile Antenna Conical Cut, 1500 MHz, Vertical Polarization, Var. θ, $\phi = 60^{o}$

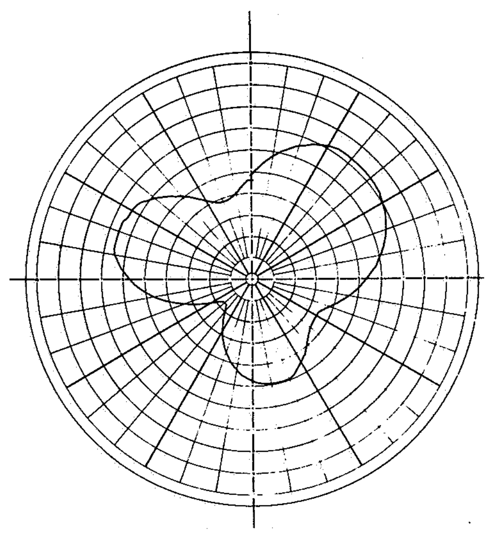


Figure 52. Pattern No. 37, Curved Dipole Turnstile Antenna Conical Cut, 1500 MHz, Horizontal Polarization, Var. θ, $\phi = 60^{o}$

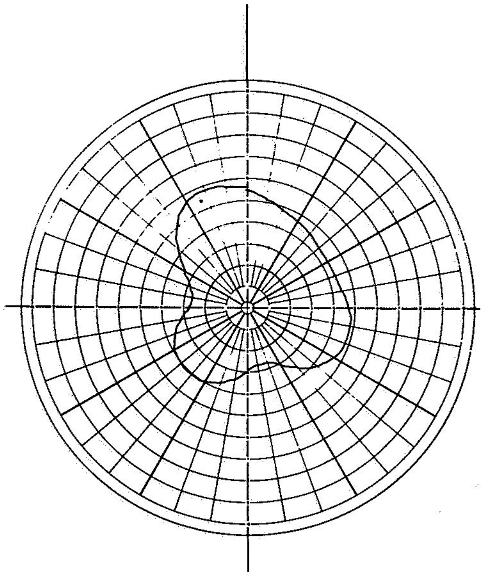


Figure 53. Pattern No. 38
Curved Dipole Turnstile
Antenna Conical Cut,
1500 MHz, Vertical
Polarization, Var. ϕ,
$\theta = 90^o$

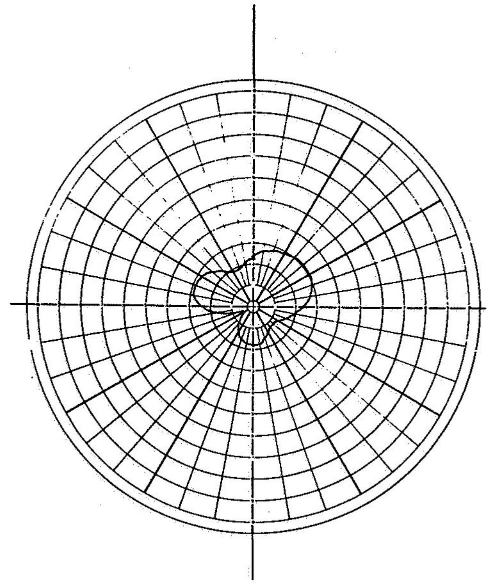


Figure 54. Pattern No. 39
Curved Dipole Turnstile
Antenna Conical Cut,
1500 MHz, Horizontal
Polarization, Var. ϕ,
$\theta = 90^o$

4.1.4.2 Curved Dipole Turnstile Antenna

A brief study was conducted on a turnstile design with a pair of curved dipoles. A picture of the test model is shown in Figure 55.

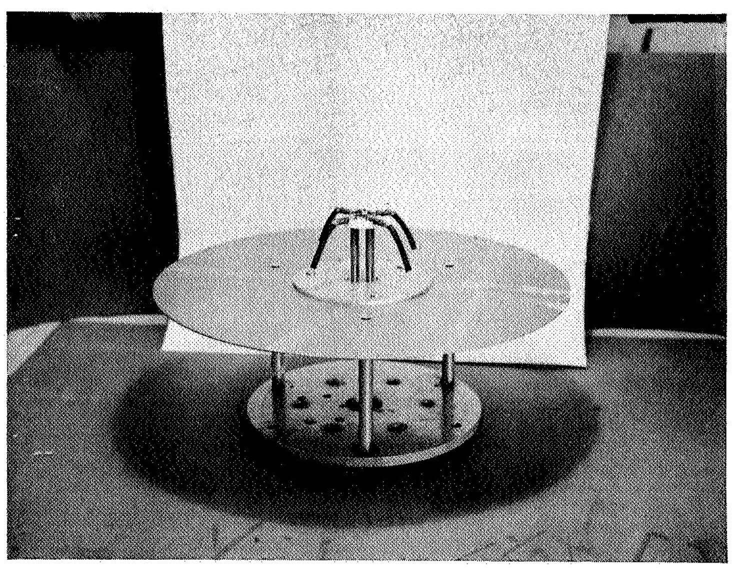


Figure 55. Curved Dipole Turnstile Antenna Test Model

This antenna, as described before, will produce a near-hemispherical coverage in a careful design. Because of time limitations, a detailed pattern performance was not fully explored. Patterns were taken on one curved dipole with the orthogonal dipole input terminated. The E- and H-planes recorded under this condition are shown in patterns 22 and 23, respectively. These two patterns exhibit a very broad coverage as was expected. For this model design study, only a stationary, non-rotating, linear transmitting source was available from the pattern range in use. Therefore, it was necessary to test the antenna by using both the vertical and horizontal sources in order to determine if the antenna is indeed circularly polarized.

With the dipole connected through a 3 db, 90° hybrid, coaxial device, patterns were recorded while the antenna was facing directly toward the source and rotated every 45°. These patterns are shown in patterns 24 through 31. It is noted that these patterns are not perfectly symmetrical, indicating that the model was not operating quite as hoped for. This condition could be caused by an incorrect phasing. Because the model had a high VSWR and the problem was not easily corrected within the time available for experimentation, further effort was not pursued.

A set of conical-cut patterns was taken; these are shown in patterns 32 through 39. Although the recorded conical patterns are not of the best quality, it does demonstrate that the design can provide good reception to vertical and horizontal fields. An estimated gain and beamwidth is given in Figure 8 for comparison with other design approaches.

4.2 RECEIVER SUBSYSTEM

4.2.1 INTRODUCTION

The NAVSTAR receiver subsystem demodulates the L-band carrier transmissions containing the range and satellite data information from the satellites. The demodulated receiver output is sent to the preprocessor which measures the range and decodes the satellite data information.

Two basic types of receivers were investigated for this study, as follows:

1) CW receiver — This is a phase-lock receiver, which may be used for either of the CW ranging schemes (the BINOR code or fixed-tones systems);

2) Pulse compression receiver — This equipment has characteristics very similar to a radar receiver which detects the presence or absence of pulses.

One phase-lock receiver design is contemplated for either the BINOR code or fixed-tones systems. The difference in total user equipment between the two techniques is reflected primarily in the preprocessor design. However, if the fixed-tones system requires large carrier-phase deviations by the five tones (for multipath error reduction), modifications will be needed on the basic CW receiver. This subject is discussed further in par. 4.2.3.

4.2.2 SUMMARY

The NAVSTAR receiver subsystem design study has considered three modulation techniques (BINOR code, fixed-tones, and pulse compression) that can be implemented through two receiver design configurations (CW and pulse compression). The decision as to which of the three modulation schemes should be selected for NAVSTAR depends primarily on cost. In this instance, both the receiver and preprocessor costs must be considered since each is affected by a change in the modulation configuration.

Simplified block diagrams for the CW and pulse compression receivers are presented in Figures 56 and 57.

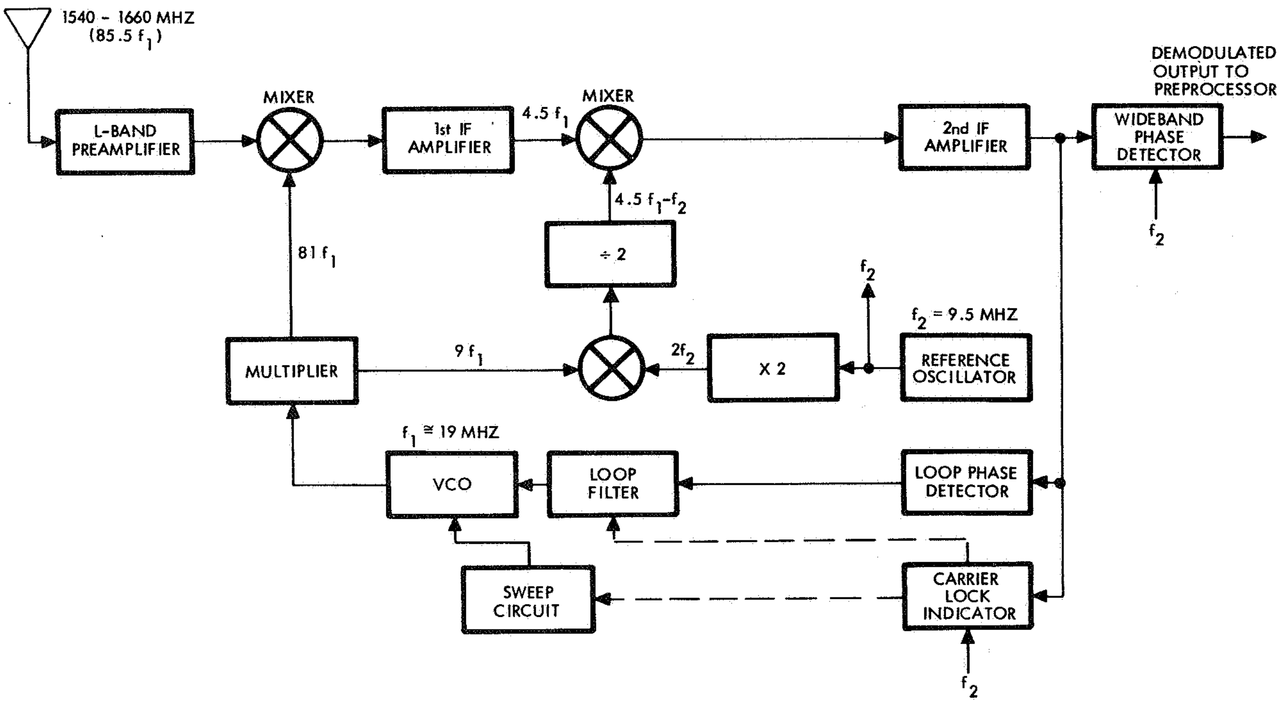


Figure 56. Simplified Block Diagram of NAVSTAR CW Receiver

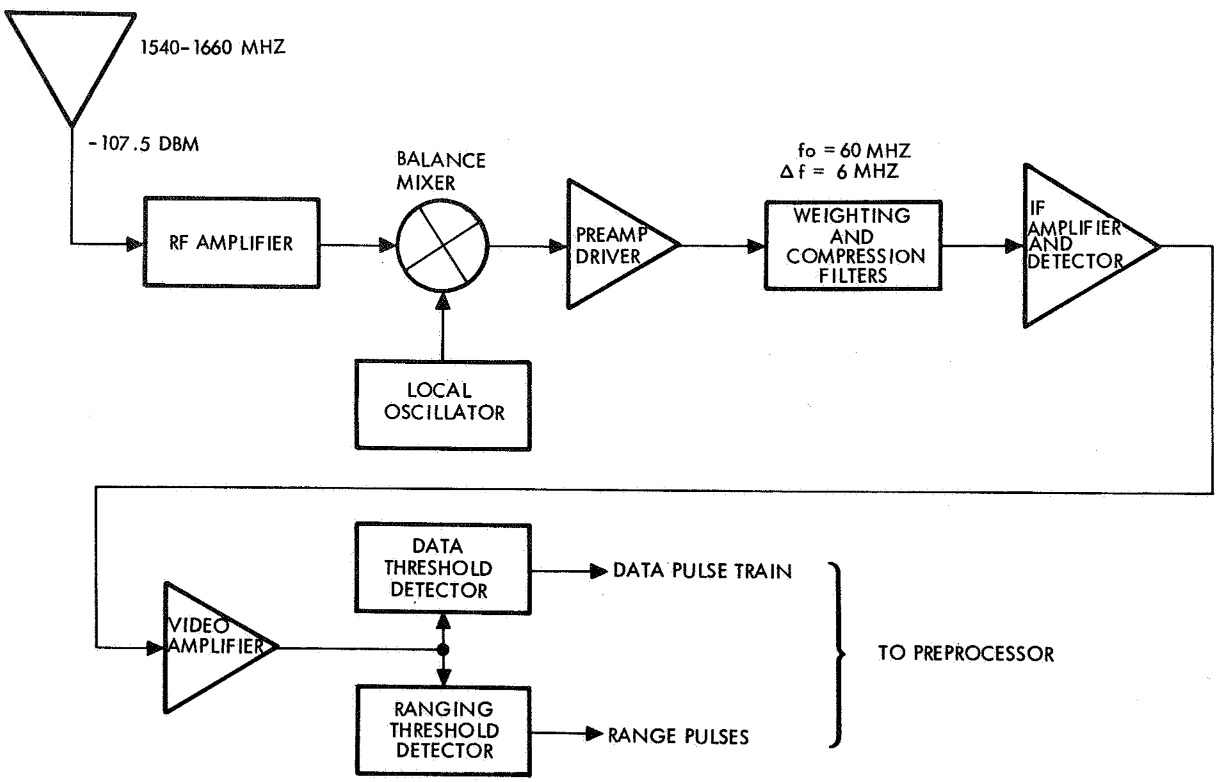


Figure 57. Simplified Block Diagram of the Pulse Compression Receiver

4.2.2.1 Receiver Specifications

CW Receiver. A preliminary specification for the CW receiver is shown in Table XI. The 5-MHz bandwidth is more than adequate to handle both the BINOR code and fixed tones modulations. The receiver noise figure, loop bandwidth, and carrier-acquisition signal threshold specified were assumed in the power budget for the BINOR code (see vol. I). The sweep range of ±26 kHz about the L-band carrier is derived as follows:

Maximum carrier doppler:	±4.8 kHz (3000 ft/sec)
TCVCXO stability:	±19.6 kHz (10 PPM long term plus 3 PPM temp. stability through -10°C to +60°C)
TCXO stability:	±1.6 kHz (1 PPM)
TOTAL	±26.1 kHz

Pulse Compression Receiver. A preliminary specification for the pulse compression receiver is shown in Table XII. Two pulse-detection thresholds are specified for the receiver: one to be used in connection with the ranging pulses and the other for the PPM data pulses. For the ranging pulses, the probabilities of detection and false alarm specified are given in reference to the detection of one pulse; however, the use of a two-pulse coincidence detector (which is part of the preprocessor) reduces these probabilities to 0.985 and 10^{-12}, respectively. Another detection threshold is established for the PPM data pulses, which results in equal false alarm and miss probabilities. The probability of a miss is equal to one, minus the probability of detection.

4.2.2.2 Availability of Off-the-Shelf Equipment

The major manufacturers of UHF receiver equipment were solicited to match their existing product lines against the NAVSTAR receiver requirements. It was later determined that their off-the-shelf equipment did not meet the desired NAVSTAR receiver characteristics. Although all companies solicited indicated their strong desire to support the NAVSTAR effort, they needed time for research and development before

TABLE XI

CW RECEIVER PRELIMINARY SPECIFICATIONS

Functions:	1) Continuous sweep in frequency over a search range when not locked to an incoming carrier 2) Phase locked to a carrier in the sweep range 3) Coherent demodulation of ranging signal and split-phase data modulating the carrier
Signal input:	Unmodulated carrier for 0.38 sec period followed by phase modulation of carrier by ranging and split-phase data
Carrier frequency:	In band 1540 to 1660 MHz
Dynamic range of signal:	-120 dbm to -135 dbm
Bandwidth:	5 MHz
Sensitivity:	Carrier acquisition threshold power at input of -132 dbm
Sweep range:	±26 kHz about nominal L-band carrier frequency
Sweep period:	0.38 sec
Probability of lock:	0.99 or better on one sweep
Carrier loop bandwidth (two-sided):	1650 Hz during sweep, automatically reduced to 50 Hz upon carrier acquisition
VCO stability:	±0.001% long term
Receiver differential time envelope delay:	±5 nsec variation over dynamic range of signal input at fixed frequency, and over input carrier frequency range of ±26 kHz at fixed input signal level
Receiver output:	Demodulated range signal followed by split-phase satellite data to preprocessor

TABLE XII

PULSE COMPRESSION RECEIVER
PRELIMINARY SPECIFICATIONS

Functions:	1) Detect ranging pulses 2) Detect PPM data pulse train
Signal input:	20 μsec chirped pulses at PRF of 78.125 pulses/sec
Pulse-carrier frequency:	In-band 1540 to 1660 MHz
Chirp range:	5-MHz linear sweep above nominal carrier frequency
Dynamic range of pulses:	-96 dbm to -110 dbm
Bandwidth:	6 MHz
Sensitivity:	Minimum detectable pulse input power of -107.5 dbm
Pulse compression ratio:	100:1
Compressed pulse length:	200 nsec
Compressed pulse SNR:	14.7
Range pulses detection threshold:	Detection probability = 0.993 False alarm probability = 10^{-6}
PPM data pulses detection threshold:	Miss probability and false alarm probability equals 10^{-4}
Output:	Detected range pulses and data pulses to preprocessor

submitting their design and production cost data. None of them were prepared to make this effort without further consideration, which was clearly beyond the scope of the present study.

4.2.2.3 Summary of Receiver Costs

Cost data was internally generated on each of the two candidate receiver designs. This information is summarized in Table XIII along with estimates on the required power, weight, and volume. (Note: No allowance has been made for modifications which may be required to minimize the effects of multipath.)

TABLE XIII

SUMMARY OF RECEIVER COSTS AND OTHER CHARACTERISTICS

Receiver Type	Unit Cost (For Quantities Shown)			Power	Weight	Volume
	100	1000	10,000	(w)	(lb)	(in.^{3})
CW (BINOR code and fixed tones)	$7,130	$4,410	$2,960	2.4	4.5	330*
Pulse compression	$6,370	$4,250	$2,840	16	17	680**

*Equivalent to 1/4 ATR box
**Equivalent to 1/2 ATR box

4.2.2.4 Alternate Techniques

Additional study is required to determine the nature and effect of multipath that will prevail in the NAVSTAR environment. Pending further study, it may prove necessary to modify the basic CW receiver for fixed tones use to reduce multipath errors. The proposed modification would consist of adding five tone-tracking loops, which track the high deviation tones. Further details on the tone-tracking loops are given in par. 4.2.3.

In the case of the BINOR code, however, multipath sensitivity can be appreciably reduced by increasing the code-clock frequency and associated code-bit rate. In this instance the CW receiver would be essentially unaltered, except for an increase in the RF and IF bandwidths necessary to accommodate the increased bit rate.

4.2.3 TECHNICAL DESCRIPTION

4.2.3.1 CW Receiver Design

The CW receiver shown in Figure 58 is a compact, relatively low-cost, high-performance, phase-locked loop receiver. Some of the salient features of the design are the following:

1) Low noise figure (approximately 5 db).

2) High-stability (±1PPM long term), temperature-compensated, crystal oscillator (TCXO) with reset capabilities.

3) High-stability (±10 PPL long term), temperatures-compensated, voltage-controlled, crystal oscillator (TXVCXO).

4) Transistor multipliers achieving low-cost multiplication with power gain where needed. Use of X3 and X2 multipliers produce simplicity and reliability in design.

5) Bandpass filters used before and after mixing produce clean signals and attenuate spurious responses down 60 db or more.

6) Double heterodyning, which achieves an elimination of high-level subharmonics of the received frequency at the first IF frequency.

When the receiver is not locked to an RF carrier, it is put in a search mode to look for a carrier signal in the frequency range of the search. The frequency range of the search is ±26 kHz about the nominal L-band carrier frequency, and is obtained by sweeping the VCO about its center frequency. After acquisition of a carrier, the VCO sweep is disabled, and the loop filter is switched from a wideband search mode to a narrowband tracking mode. In the tracking mode, the demodulated ranging signal, followed by split-phase data, will appear at the output of the receiver.

With the TCVCXO equal to f_1 and the input signal equal to $85.5\ f_1$, the first mixer output is $85.5\ f_1 - 81\ f_1$, or $4.5\ f_1$. The frequency f_1 will be 18 to 19.4 MHz, depending on the L-band frequency (1540 to 1660 MHz) to which the receiver is tuned. The first mixer ratio turn

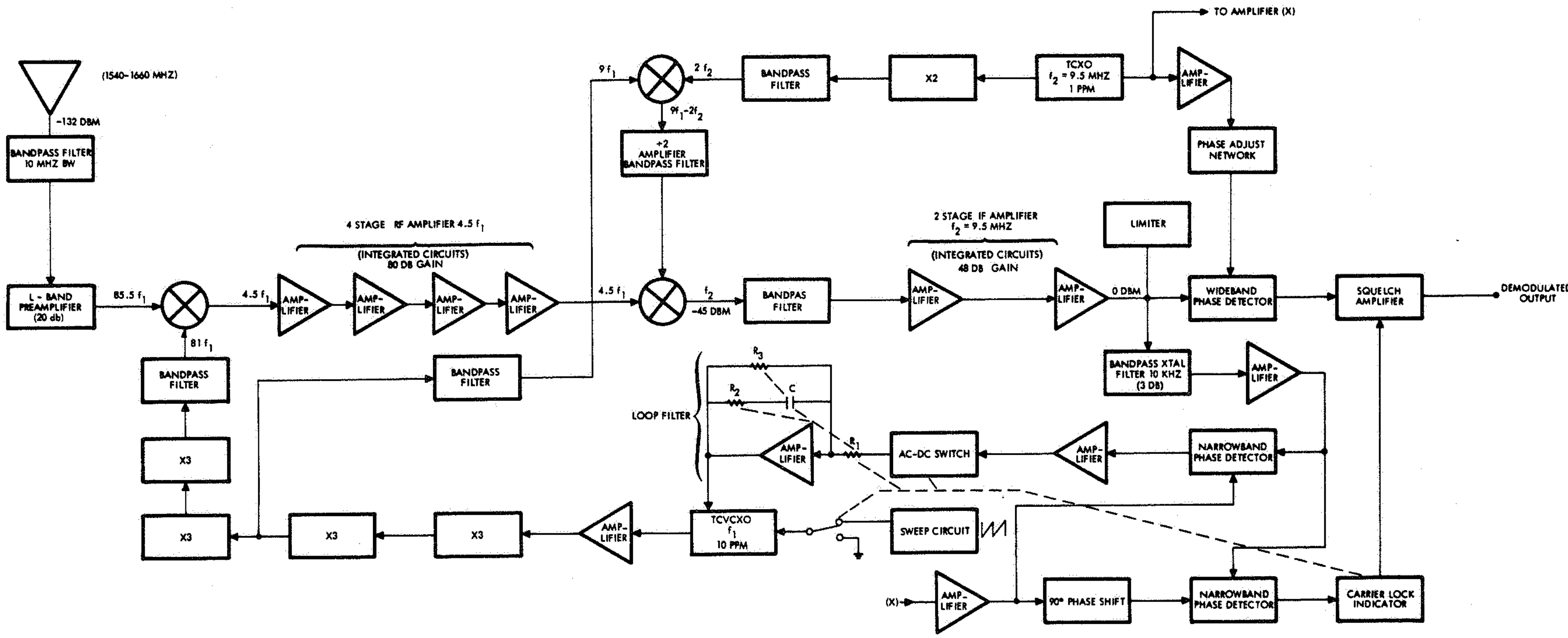


Figure 58. CW Receiver

$81/85.5 \approx 0.95$ produces no spurious responses below the seventh order with ±50 percent separation. Separation in percent is defined as

$$S = \frac{f_o - M}{f_o} \times 100$$

and

$$M = mf_i + nf'_i$$

where

f_i, f'_i = input frequencies to mixer

f_o = output frequency of mixer

m, n = positive and negative integers

The second mixer has a ratio of $1.125 - 0.25\, f_2/f_1$. With f_2 (the TCXO) equal to 9.5 MHz, this ratio will be about 0.89 which will have no spurious responses showing up within ±50 percent separation. The bandpass filter shown in the block diagram is used to remove spurious responses outside the ±50 percent separation, which may be necessary since the bandwidth of the signal will be on the order of 5.0 MHz. This filter, however, may be removed by breadboard testing.

The input bandpass filter is of the interdigital type. Stripline techniques could be used to reduce costs in production. Insertion loss would be less than 0.5 db with ripple through the passband less than ±0.1 db. With a passband of 10 MHz, attenuation at 4XBW would be down 60 db. Size and weight of this filter would be approximately 20 cu.in. and 13 oz.

The L-band preamplifier has a 4.6-db noise figure and 20-db gain. Size would be 12 cu.in. and weight would be approximately 12 oz. The above amplifier is based on using transistors. A lower noise figure can be had with tunnel diodes, but a slight penalty would be paid in gain.

The first mixer is of a stripline hybrid T design. This design is applicable to large production quantities. The radio frequency amplifiers are integrated circuits operating around 80 to 88 MHz, which is well below the 100-MHz maximum for the units in mind. The bandpass filter coming off the X3 multiplier to the first mixer will be similar to the input band pass filter at the front end of the receiver.

The multiplier chain, used to multiply the TCVCXO for use in the first and second mixers, is a reliable straightforward way of achieving the desired results. Inexpensive transistors (one each per X3 multiplier) are used, except in the last multiplier, which would use a more expensive transistor. The low power required from this last multiplier (approximately 4 mw) again reduces the cost of this stage. Breadboarding and final design of this circuit will probably remove the amplifier shown between the TXVCXO and the first X3 multiplier. The inclusion of the amplifier would be worst-case at this time.

The TXVCXO and the TCXO represent high-quality, lightweight, and small-size crystal reference sources. Because of the significant advances made within the past few years, the manufacturer can easily meet the specifications for these units. Output power is 0 dbm. Both have the reset capbilities permitting adjustments to be made in the initial 3 or 6 months of operation for further improvement of system performance. These are not mandatory adjustments but they may be found desirable.

The mixer producing $9f_1 - 2f_2$ and the second mixer can be balanced quad diodes or transistor pairs. Recently, an investigation was made of a transistor pair mixer in which spurious products were found to be down 40 to 45 db. This feature is as good as any available with commercial diode mixers. Further work is scheduled here and the final results will be available to this design.

The divide-by-two circuit can be solved by using a tunnel diode. Here, also, transistor circuit can serve, taking about two to three times the number of parts. An amplifier and filter are then required to drive the second mixer. The power level out of this mixer is nominally -45 dbm.

The two-stage IF amplifier following the second mixer provides 48 db gain, using integrated circuit amplifiers operating at 9.5 MHz. The limiter at the end of the IF amplifiers consists of a pair of biased diodes to maintain the power level at 0 dbm ±1 db.

In the initial acquisition of the CW signal, the TCVCXO is continuously swept by the sweep circuit over a range of ±26 kHz divided by 81 (TCVCXO multiplication) about its center frequency. The sweep waveform is a sawtooth with a period of 0.38 sec. While the sweep is operating, the ac-dc switch is in the ac position to prevent dc drift from being amplified by the loop-filter amplifier. When acquisition takes place as determined by the carrier lock indicator circuit, the sweep circuit is inhibited and the ac-dc switch circuit takes the dc position. In addition, a relay switches the component values in the loop filter to change the loop bandwidth from 1650 Hz in the wideband acquisition mode to 50 Hz in the narrowband tracking mode. These bandwidth values correspond to loop SNR's of 6.0 db for acquisition and 10 db for tracking. The carrier lock indicator circuit, which is a dc-level detector, also opens the squelch amplifier at the output of the wideband phase detector when acquisition takes place.

The phase-adjustment network between the TCXO and the wideband phase detector is used to compensate for the loop static phase error and the phase shift from the TCXO due to the amplifier.

Alternate Design. In the event that further analysis dictates large carrier phase deviation for the fixed-tones system, the following modification is recommended in the basic CW receiver design. To modify the receiver for operation with the high-deviation fixed tones system, five tone-tracking loops must be added. The five ranging tones at the receiver output are filtered by five narrow bandpass filters. The filter outputs are amplified and fed back to the carrier loop TCVCXO where they phase modulate the TCVCXO output. The phase deviations at the output of the first mixer are compressed or reduced by this operation to low deviation values and, consequently, the majority of the received power is tracked back into the carrier and tone first order sidebands. The tone loop gains will be about 30 db for this application.

4.2.3.2 Pulse Compression Receiver Design

A simplified block diagram of the pulse compression receiver is shown in Figure 57. Carrier pulses at the receiver input are chirped with a delay dispersion of 20 μsec and with a dispersive bandwidth of 6 MHz (rise time = 0.2 μsec). The receiver then provides a compression ratio of 100:1. The resulting peak power of the compressed pulse is 20 db higher than the peak power of the dispersion pulse and the pulse width is reduced to 0.2 μsec. The major receiver circuit building blocks are described as follows:

1) RF Amp. — The dispersed signal received at the antenna is amplified in a commercially available L-band RF amplifier with a noise figure of 4.6 db. Power gain of this transistor amplifier is 20 db to reduce "second stage" noise contribution of the mixer.

2) Local Oscillator (LO) and Mixer.—A balanced mixer is used to minimize LO noise. The dispersed signal is mixed down to a 60-mc IF to match the design center frequency of the compressive filter. This is because the block contains driver and post amplification as well as a weighting filter to minimize time sidelobe levels. A sidelobe level of -30 db is anticipated and, consequently, the time sidelobes should be "in the noise." These requirements are nearly identical with an off-the-shelf filter manufactured by Anderson Laboratory (Model No. 4357-D).

3) Detector and Video Amplifier/Threshold. — The compressed pulse (0.2 μsec duration) is further amplified in a solid-state 60-mc IF amplifier and then amplitude detected in straightforward fashion.

Further level enhancement is provided by the video amplifier and the signal is split into two paths for quantization above two different thresholds. The higher threshold is used for the ranging pulses (also data sync) and the lower threshold is used for data pulses. The two different thresholds are used to optimize the relationship between false alarm and detection probabilities for each case.

The threshold for the ranging pulses with a 14.7-db SNR is set to yield a false alarm probability (P_{FA}) of approximately 10^{-6} and a probability of detection (P_D) of approximately 0.993. A lower threshold is desirable for the data pulses and this is set to equalize the P_{FA} and P_{MISS} performance for maximum detection efficiency. These probabilities will be 10^{-4} each.

4.3 PREPROCESSOR SUBSYSTEM

4.3.1 INTRODUCTION

4.3.1.1 Scope of Effort

The preprocessor serves as the link between the NAVSTAR user receiver and the computing and/or display subsystems. The primary functions of the preprocessor are:

1) To perform the range measurement. (The preprocessor receives a demodulated video range signal from the receiver and uses it to measure the range from satellite to user.)

2) To decode PCM satellite data. (The demodulated satellite data from the receiver is decoded by the preprocessor and then grouped into the appropriate word structure.)

3) To provide computer/display interface. (The preprocessor reformats range and satellite data for the direct entry to the computing or display subsystem.)

4.3.1.2 Preprocessor Configurations

Five preprocessor configurations were considered in this study; three are a function of the desired range modulation technique and two are a function of the proposed system operation. The first three types (BINOR code, pulse compression,and fixed-tones preprocessors) assume that each NAVSTAR user possesses all the necessary equipment for complete and independent position determination. The fourth configuration, which is the inexpensive user mode of operation, utiilizes the BINOR code for ranging and assumes that all the computation is done by hand. The fifth configuration also utilizes the BINOR code for ranging, but assumes that the computation is performed by a cooperating ground station and then relayed to the user for display.

As previously indicated in sec. 3, three modulation schemes are available for possible use in the NAVSTAR system. The final determination as to which is to be recommended rests primarily on the reflected costs to the NAVSTAR user. Only the receiver and preprocessor are affected by the choice of modulation technique. These units, therefore, have been carried through to the design stage in order to permit a reasonable cost determination.

The succeeding subsections describe the design aspects of the preprocessing equipment required to handle each of the above modulation schemes. Also covered are the required preprocessor implementations for the other two NAVSTAR system utilization concepts, namely, the manual and ground station aided configurations.

4.3.2 SUMMARY

The preprocessor subsystem consists of the following basic elements: a stable reference crystal oscillator, a range measurement section, a satellite data decoder, a data buffer, and a computer interface. The functional interrelationships of these sections are shown in block diagram form.

Three candidate range measurement modulation techniques were reviewed in the course of the present study: the BINOR code, pulse compression, and fixed tones. Preprocessor designs have been prepared to operate with each of these modulation techniques. The corresponding specifications which were used as system design goals are presented in Tables XIV, XV, and XVI. A summary of each preprocessor design is given below.

4.3.2.1 BINOR Code Preprocessor

The BINOR range measurement technique uses a binary code 2^{13}-bits long. The acquisition procedure for the code consists of acquiring a clock component with a phase-lock loop followed by 12 correlations in sequence with 12 squarewaves, each at half the frequency of the preceding wave. The code is derived from the highest frequency squarewave of 320 kHz (to give 30-ft rms range error) and the lowest frequency squarewave of 78.125 Hz (to give 2100-nmi range ambiguity). After all of the correlations have been performed, the lowest frequency squarewave will be in-phase with the transmitted code sequence. The desired range can then be secured by measuring the phase delay between the derived in-phase lowest frequency squarewave from the received signal and a reference

TABLE XIV

BINOR CODE PREPROCESSOR PRELIMINARY SPECIFICATIONS

Functions:	1) Perform range measurement 2) Decode PCM satellite data 3) Provide computer interface
Basic Elements:	1) Code acquisition network 2) Reference oscillator 3) Range measurement unit 4) PCM data signal conditioner and bit synchronizer 5) Data buffer 6) Computer interface
Code acquisition network:	
Input:	BINOR code at 640 kb/sec
Output:	78.125-Hz squarewave in-phase with BINOR Code sequence
Reference oscillator:	
Frequency:	20.48 MHz
Stability:	1 part in 10^9 (per 12 sec)
Range measurement unit:	
Inputs:	1) 78.125 Hz-squarewave from code acquisition network 2) Reference 78.125-Hz squarewave (internally generated from reference oscillator)
Number of measurements:	8 independent range measurements per satellite transmission
Outputs:	1) Timing signals for code acquisition network 2) 20-bits parallel data (representing weight accumulated range counts),
PCM data signal conditioner and bit synchronizer:	
Input:	625 b/sec, split-phase coded
Acquisition time (bit sync):	≤ 35 bits
Bit error rate:	10^{-4} (SNR = 9.5 db in a 625-Hz BW)
Outputs:	1) Decoded satellite data (15 10-bit words) 2) Word count (4 bits) 3) Parity test indicator 4) Interrupt signal
Data buffer:	See Table XVI
Computer interface:	
Inputs:	Binary data from range measurement and data buffer units
Outputs:	Formatted data are 20-bit computer words and data ready signal

TABLE XV

PULSE COMPRESSION PREPROCESSOR PRELIMINARY SPECIFICATIONS

Functions:	1) Perform range measurement 2) Decode PPM satellite data 3) Provide computer interface
Basic Elements:	1) Coincidence detector 2) Range decoder 3) Reference oscillator 4) PPM data demodulator 5) Data buffer 6) Computer interface
Range Decoder:	
Input:	200-nsec ranging pulses
Measurement accuracy:	30-nsec rms noise error pulse leading edge
Coincidence detector:	
Probability of detection:	0.984
Probability of false alarm:	10^{-12}
Reference oscillator:	
Frequency:	50 MHz
Stability:	1 part in 10^9 (per 10 sec)
PPM data demodulator:	
Input:	200-nsec PPM pulses at 78.125 p/sec
Bit error rate:	10^{-4} (pulse SNR = 14.7 db)
Outputs:	Sync plus NRZ-L data at 156.25 b/sec
Data buffer:	
Inputs:	NRZ-L data and clock from PPM data signal demodulator
Outputs:	1) Decoded satellite data (15 10-bit words) 2) Word count (4 bits) 3) Parity test indicator 4) Interrupt signal
Computer interface:	
Inputs:	Binary data from range measurement and data buffer units
Outputs:	Formatted data are 20-bit computer words and data ready signal

TABLE XVI

FIXED-TONES PREPROCESSOR PRELIMINARY SPECIFICATIONS

Functions:	1) Perform range measurement 2) Decode PCM satellite data 3) Provide computer interface
Basic elements:	1) Range tone filters 2) Reference oscillator 3) Range measurement unit 4) PCM data signal conditioner and bit synchronizer 5) Data buffer 6) Computer interface
Range tone filters:	
Input:	Composite of 5 ranging tones — 320 kHz, 40 kHz, 5 kHz, 625 Hz, 78.125 Hz
Filter bandwidths:	5 Hz (320 kHz tone); 4 Hz (others)
Output:	5 tones, each at SNR of 21 db
Reference oscillator:	
Frequency:	20.48 MHz
Stability:	1 part in 10^9 (per 18 sec)
Range measurement unit:	
Inputs:	1) 5 range tones (from range tone filters) 2) Reference pulse (internally generated from reference oscillator)
Number of measurements:	8 independent range measurements per satellite transmission
Outputs:	20 bits parallel data (representing eight accumulated range counts)
PCM data signal conditioner and bit synchronizer:	See Table XIV
Data buffer:	
Inputs:	NRZ-L data and clock from PCM signal conditioner and bit synchronizer
Outputs:	1) Decoded satellite data (15 10-bit words) 2) Word count (5 bits) 3) Parity test indicator 4) Interrupt signal
Computer interface:	
Inputs:	Binary data from range measurement and data buffer units
Outputs:	Formatted data are 20-bit computer words and data ready signal

squarewave of the same frequency generated internally. The preprocessor contains a 20-MHz reference oscillator used in measuring the phase delay. The range count is averaged over eight periods during each satellite transmission interval in order to minimize quantization errors.

The satellite data is extracted by the PCM signal conditioner and bit synchronizer providing NRZ-L data and a sync signal to the data buffer. The data demodulator receives a split-phase code at a frequency equal to the data bit rate of 625 b/sec. The data is received following the end of the BINOR code ranging signal.

4.3.2.2 Pulse Compression Preprocessor

Range measurements using the pulse modulation technique are performed by measuring the average time difference between locally generated clock pulses at the PRF rate of 78.125 p/sec and four coincidence ranging pulses. The coincidence pulses are generated by accurately duplicating the time interval (1/78.125) between each of the five ranging pulses transmitted by the satellite pulse of each interval, arriving precisely at the completion of this locally generated time interval. The range measurement is performed with a granularity of 20 nsec.

The satellite data is pulse-position modulated (PPM) with an average PRF of 78.125 p/sec and is transmitted following the five range pulses. The PPM data demodulator operates by detecting the existence of data pulses in the four positions available during each 12.8-msec interval. The data is converted to an NRZ-L format and then fed to the data buffer for processing.

4.3.2.3 Fixed-Tones Preprocessor

The preprocessor for fixed-tones modulation performs range measurements by determining the precise phase relationships of five ranging tones transmitted from the satellites with respect to the local reference oscillator. The range measurement is accomplished by measuring the time interval between a locally generated markpulse and the point where all ranging tones experience a zero crossing. The reference oscillator must be accurate to 1 part in 10^9 over an interval of 16 sec, since it is used to obtain the precise time mark from which the range tone phase differences are measured. The phase-time interval is measured to an accuracy of 50 nsec.

The satellite data are extracted in an identical manner to the BINOR code system. As in the latter system, the satellite data are received following the end of the range tones signal.

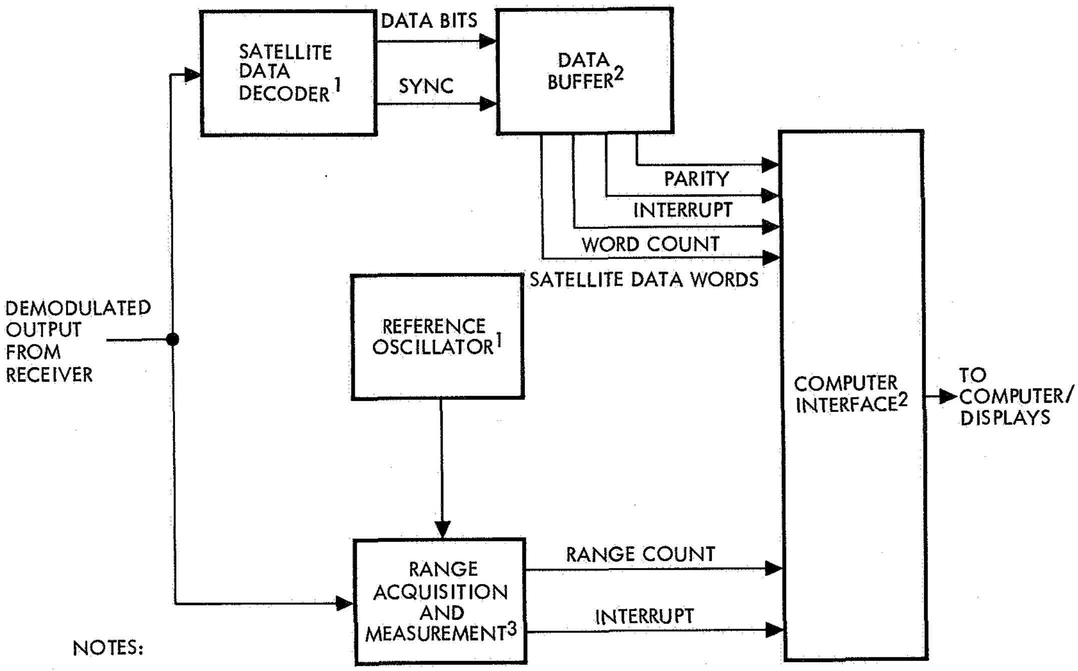
4.3.2.4 Common Preprocessor Elements

The operation of the data buffer section of the preprocessor is independent of the range measurement technique or data decoder employed. The data buffer receives the NRZ-L data stream and data (bit) sync signals from the data decoder and performs a cross correlation test for data frame sync. The data format transmitted from the satellite contains a frame sync code and 15 11-bit words. Each word contains a parity bit that maintains even parity over the word.

When frame sync is detected, the data following is collected, a word at a time, and checked for correct parity. A data interrupt is then generated and the word is outputted in parallel. The word count is provided to aid interpretation or placement of the data by the computer.

The preprocessor is designed to accommodate a wide range of user hardware options. By adding circuit elements to the basic unit the preprocessor is mechanized to meet the user equipment requirements.

The basic preprocessor unit, as shown in Figure 59, supplies outputs compatible with an on-board computer. This comprises the fully automatic user configuration. The outputs of the basic preprocessor unit are: 20 bits of range count data and a range count interrupt; 15 10-bit satellite data words issued consecutively comprising the satellite data frame, data word interrupt issued for each word, 4 bits of word count, and a data word parity signal.



NOTES:

1. COMMON TO BINOR AND FIXED TONES.
2. COMMON TO ALL.
3. DIFFERENT FOR EACH.

Figure 59. Generalized Preprocessor Block Diagram

4.3.2.5 Other Preprocessor Configurations

For the automatic ground-dependent user configuration, the basic preprocessor unit requires the addition of a data encoder. The data encoder circuits temporarily store the range count and the satellite data as they are received and serially outputs these data to a transmitter/modulator for transmission to the ground station. Outputs from the preprocessor are also provided for a display unit if manual calculations are required because of interruption of the user/ground station link.

The outputs of the basic preprocessor unit are equally applicable to a display unit incorporating an internal data register. However, a small number of additional circuits in the data buffer of the preprocessor are required for individual satellite data selection. This feature enables continuous display of data from selected satellites, facilitating data presentation for manual position-fix calculations.

4.3.2.6 Summary of Preprocessor Costs

Cost data were internally generated on each of the three major preprocessor designs analyzed for the completely automatic NAVSTAR user. This information is summarized in Table XVII along with estimates on the required power, weight and volume.

TABLE XVII

SUMMARY OF PREPROCESSOR COSTS AND OTHER CHARACTERISTICS

Preprocessor Type	Unit Cost (for Quantities Shown)			Power	Weight	Volume
	100	1000	10,000	(w)	(lb)	(in.^{3})
Binor code	$11,627	$7,444	$4,891	17	16	680*
Pulse compression	$5,260	$3,475	$2,391	14	10	330**
Fixed tones	$13,204	$8,265	$5,268	20	17	680*

*Equivalent to 1/2 ATR box
**Equivalent to 1/4 ATR box

4.3.3 BINOR CODE PREPROCESSOR DESIGN

4.3.3.1 Introduction

A simplified block diagram of the preprocessor for the BINOR code system is shown in Figure 60. The range measurement portion of pre-preprocessor consists of the code acquisition, range measurement, and timing circuitry. The code acquisition circuitry acquires the phase of the received noise BINOR code as represented by the phase of the 78.125-Hz squarewave. The SNR of the code at the receiver output is very low,

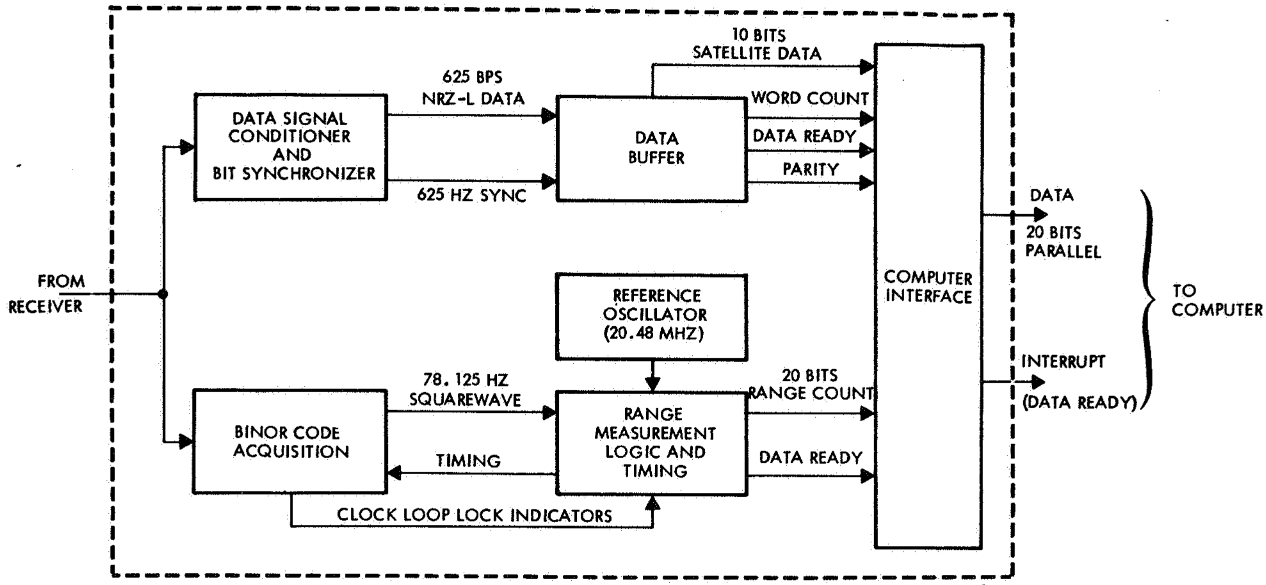


Figure 60. BINOR Code - Preprocessor Block Diagram

about -22 to -28 db. The range measurement logic and timing circuitry provides timing for the correlation circuits of the code acquisition and converts the phase of the 78. 125-Hz squarewave to a range count. The reference phase for the 78. 125-Hz squarewave and the timing signals are obtained from a stable reference oscillator operating at 20. 4 MHz.

The satellite data-decoding portion of the preprocessor consists of a data signal conditioner and bit synchronizer and a data buffer. The noisy split-phase satellite data at the receiver output are reconditioned and converted into a noise-free NRZ-L data stream by the signal conditioner and bit synchronizer. The data stream and the bit sync are sent to the data buffer, which converts the data to 10-bit words.

The computer interface formats the range count and satellite data for input to the computer. A more detailed description of each major unit in the preprocessor follows.

4. 3. 3. 2 Code Acquisition Network

A block diagram of the acquisition circuitry for the BINOR code is shown in Figure 61. The circuitry consists of a phase-lock loop for acquiring the code clock phase, a two-level loop lock indicator, and

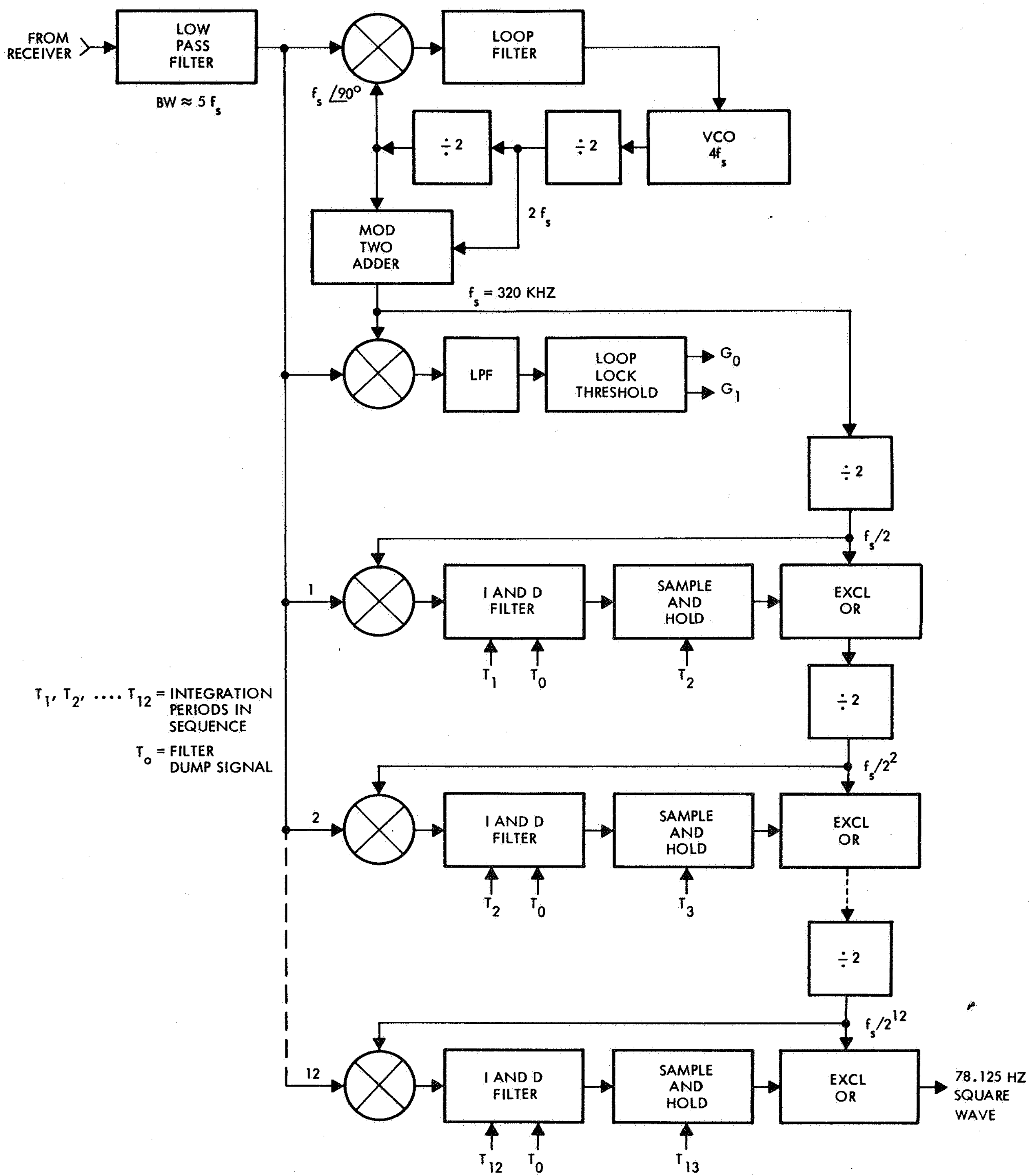


Figure 61. BINOR Code Acquisition— Conceptual Block Diagram

12 correlators. Each correlator, in turn, consists of a multiplier, integrate and dump filter, and sample-and-hold circuit. The block diagram, however, portrays only a conceptual design. In the actual design, the 12 correlators will be replaced by one time-shared correlator, since only one correlation occurs at a time. The total circuitry is simplified by this approach as the added gates and control signals contain much less circuitry than the eleven correlators they replace. To simplify the explanation on the code acquisition, however, the conceptual design configuration as shown is presented here for discussion.

The phase-lock loop (Figure 61) establishes lock with the phase of the BINOR code clock (or highest squarewave frequency). The phase-lock loop threshold circuit indicates phase lock to the clock frequency and its threshold is set for 22.5 percent clock correlation. The lock-indicator signal G_o initiates the timing sequence for the code squarewave correlations. The first correlation is with the $^{f}s/2$ (160 kHz) squarewave. The squarewave and the code are multiplied together and the multiplier output is integrated for two periods of the code (2/78.125 sec) and sampled. The polarity of the sampled voltage sets a flip-flop to one of its two states. The state of the flip-flop then determines whether the squarewave is or is not inverted, corresponding to whether the squarewave is in or out of phase with the code. The exclusive "or" gate logic serves as the squarewave inverter. The "T" timing pulses, T_1 through T_{12}, are the integration times in sequence for the integrate and dump filter and are two code periods long. The leading edge of a "T" pulse serves as the sample signal for the preceding correlation. For example, the leading edge of T_2 samples the integration during T_1.

After the first correlation, the correlations continue until the start of T_{13}, at which time the 78.125-Hz squarewave will be in phase with the code. The code phase, as represented by the 78.125-Hz squarewave phase, is now acquired. After reception of the code, which is on for a sufficient time to acquire the code phase, the 320-kHz clock is received alone without any signal modulation. The clock loop correlation now increases to 100 percent. This event is indicated by loop-lock threshold G_1 and is used to initiate the range measurement. The "T" pulse T_o

occurs eight "T" times after the T_{13} event and is the dump signal for the filters and the reset signal for the range measurement logic. The event T_o readies the preprocessor for the next range measurement from another satellite.

4.3.3.3 Range Measurement Unit

The range measurement unit shown in Figure 62 contains the fol-owing circuits:

1) 20.48-MHz crystal oscillator – reference
2) Divider - 18 stages
3) Time interval counter – 20 stages
4) Range sample counter – 3 stages
5) Code period or "T" pulses counter – 6 stages

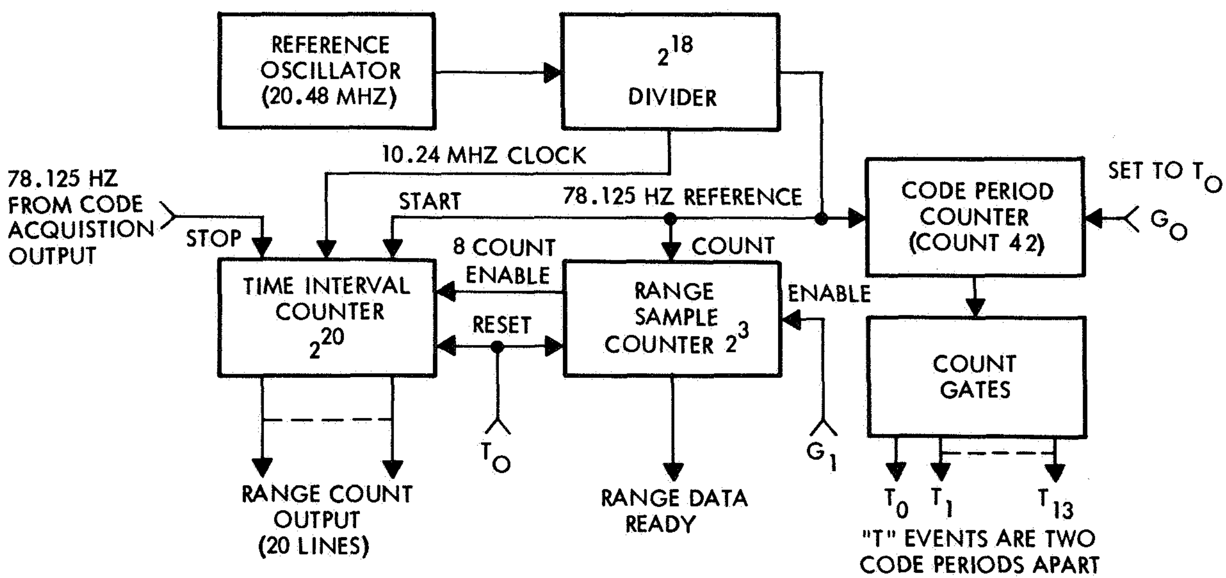


Figure 62. BINOR Code Range Measurement Unit

The lock indicator signal G_o from the code acquisition clock loop sets the code period counter to T_o, initiating the sequence of "T" pulses representing the correlation time sequence of the code-acquisition circuitry. Some time after T_{13}, the lock-indicator signal G_1 occurs and enables the range-sample counter. The range-sample counter counts eight samples of the range measurement by the time-interval counter, disables this counter, and then generates a range-count ready pulse for the computer interface circuitry.

The time-interval counter is driven by a 10.24-MHz symmetrical clock derived from the 20.48-MHz crystal reference oscillator. The interval counter is started and stopped by the leading edges of the reference and code acquired 78.125-Hz signals. The reference squarewave, which is derived from the 20.48-MHz oscillator by a 2^{18} divider, is used also as the clock for generating the "T" pulses.

One range measurement is represented by the time interval between the start and stop signals of the time-interval counter. Since a 10.24-MHz clock is used to count the time interval, a maximum timing error of 50 nsec and an rms error of $50/\sqrt{3}$ or 29 nsec results. This would be undesirable for the high-accuracy user, consequently, eight range measurements are made to reduce the rms error by $\sqrt{8}$. The time-interval counter is allowed to accumulate the count over the eight time intervals so that the range-count output must be divided by eight to obtain the correct range count. For one measurement, the capacity of the time-interval counter must be 2^{17} counts of the 10.24-MHz clock. For accumulating eight measurements, the capacity must be increased by eight or to 2^{20} counts. The computer can perform the divide-by-eight function so that the range-count word consists of 20 bits out of the time-interval counter.

Some time after the range count is completed (eight "T" events after T_{13}), the T_o event occurs and resets the time interval and the range-sample counters to zero so that a new range count can be made on initiation of another G_o signal.

For the low-cost, low-accuracy user the eight range counts are not necessary. Therefore, the range-sample counter and some logic can be eliminated from the circuitry and the total range-count word would remain at 17 bits.

4.3.3.4 Data Signal Conditioner and Bit Synchronizer

The data signal conditioner and bit synchronizer (see block diagram Figure 63) extract NRZ-L data and a clock signal from a split-phase code input signal under conditions of poor signal-to-noise ratio. A code (shown in Figure 64 can be considered as the modulo 2 sum of the NRZ-L data and the clock squarewave. The design of the data signal conditioner and bit synchronizer will employ the same principles as those employed by TRW on the Pioneer Telemetry Demodulator and is composed of the I (in-phase) channel; the Q (quadrature) channel; and the bit sync channel.

I (In-Phase) Channel. The I (in-phase) channel determines the sense of each received bit and produces a noise-free NRZ-L data bit stream. It consists of a switching multiplier that multiplies the noisy input data stream by a locally generated reference clock signal "I" that is in phase with the input split-phase code. The output of the multiplier (see Figure 64) is integrated over each bit period by an integrate-and-dump circuit containing the best estimate (in the presence of noise) of the polarity of the bit information as integrated over the bit period. The integrator output is sampled and held for the succeeding bit period, and a comparator is used to determine the polarity of the received bit. The comparator drives a data flip-flop, which is gated at the end of each bit period by the dump pulse. The data flip-flop output and a bit-sync reference signal "g", derived from the bit-sync loop, are gated with "exclusive or" logic. The resulting signal forms the NRZ-L data output (see Figure 64).

Q (Quadrature) Channel. The Q (quadrature) channel provides loop sense information to the VCO. A digital-switching multiplier in the Q channel multiplies the noisy input data stream by a locally generated reference signal (Q) that is shifted 90° with respect to the I channel multiplier reference signal "I." The multiplier output is integrated over each bit period by an integrate-and-dump circuit, sampled, and held for the duration of the succeeding bit period. This sample, which is the VCO correction, is multiplied by the output of the data flip-flop, M, in a data multiplier to remove 180° ambiguities and is passed through the loop filter to the VCO, which drives a bit-rate counter.

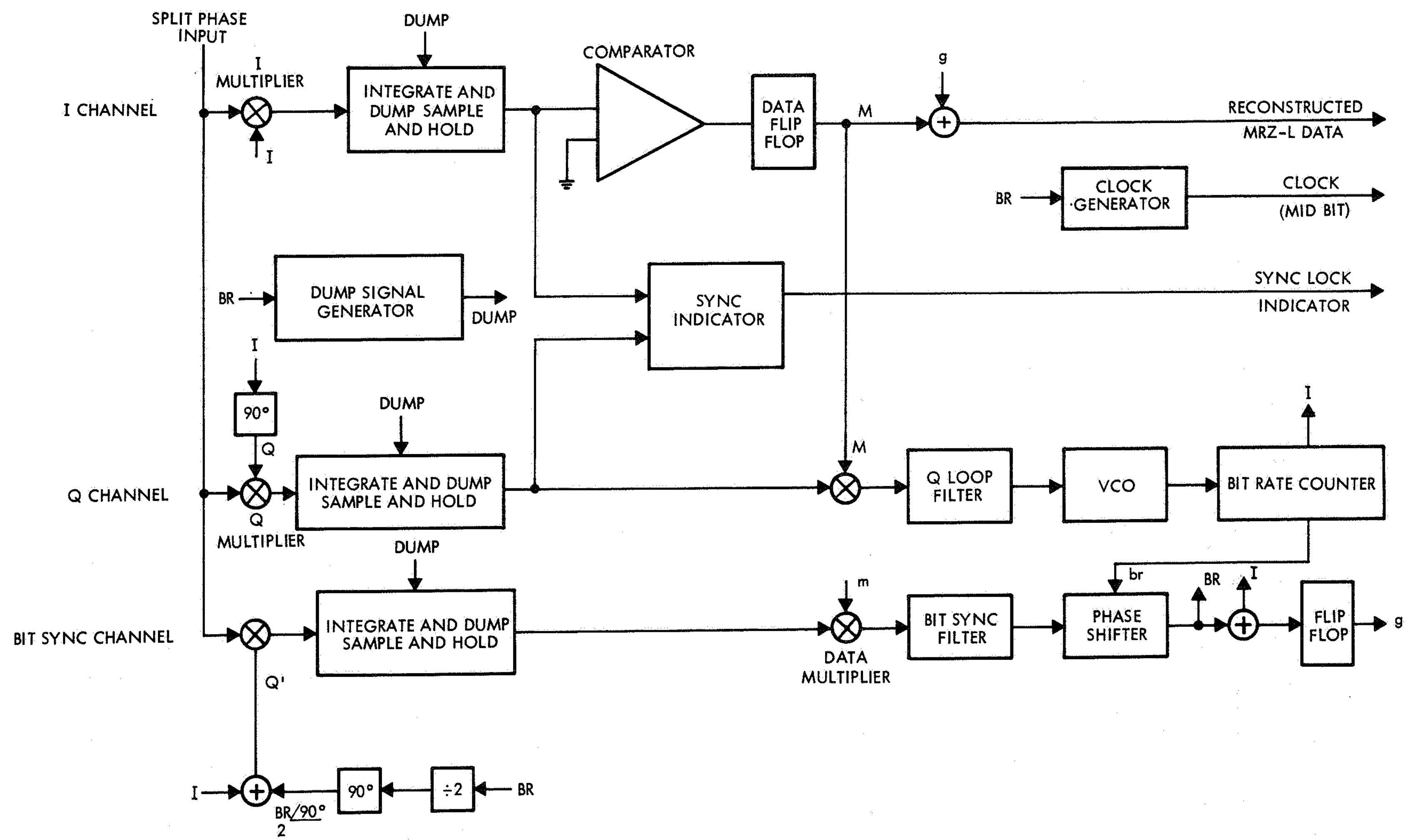


Figure 63. Data Signal Conditioner and Bit Synchronizer Block Diagram

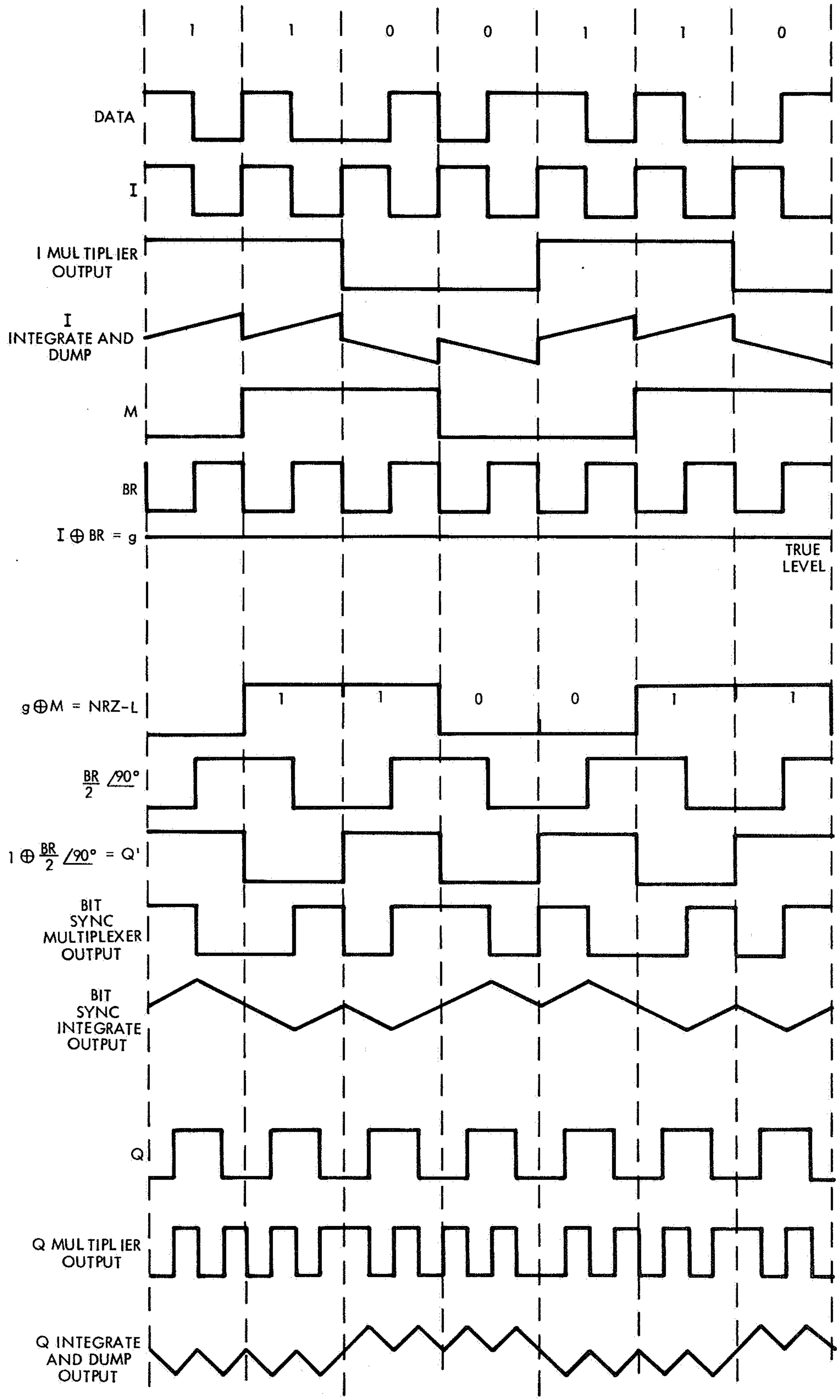


Figure 64. Data Signal Conditioner and Bit Synchronizer Waveforms

Bit-Sync Channel. Since the loop formed by the I and Q channels can lock onto the input signal with a 90° phase error, the bit-sync channel provides correct bit-phase information for the unit. The bit-sync loop operation is described as follows:

The input signal is multiplied by a reference signal (Q') that is generated by forming the "exclusive OR" of the "I" reference signal and one-half the bit rate signal shifted by 90°. The multiplier output is passed through an integrate-and-dump circuit and is sampled and held for the succeeding bit period. This sample, which is the phase shifter correction signal, is multiplied by a signal "m," that changes phase with each data phase transition, to remove the 180° ambiguities. The multiplier output correction signal is passed through the bit-sync filter and to the phase-shifter circuit. The phase-shift circuit uses the correction signal to change the phase of the bit-rate signal (br) from the bit-rate counter in the Q channel. The phase shifter output (BR) is used to generate the dump-pulse signal for the three channels and the "g" reference signal used by the I channel.

The data signal conditioner and bit synchronizer generate a signal that continuously indicates that the unit has or has not attained lock on to the input signal. This is accomplished by the sync indication circuitry which subtracts the averaged output of the Q channel I & D, S & H from the averaged output of the I channel I & D, S & H. The sync-lock indication is obtained when the I to Q function exceeds a predetermined reference level generated by the sync-indication circuit.

The data signal conditioner and bit synchronizer will have a very wide-loop bandwidth to allow fast acquisition of the input signal. This tradeoff will result in some degradation of error rate performance. The unit will have the following performance characteristics:

- Bit error probability: Equal to or less than 10^{-4} for a signal-to-noise ratio of 9.5 db in the data bandwidth
- Acquisition time: Less than or equal to 56 msec (35-bit periods)
- Input frequency stability: The input signal frequency stability greater than or equal to 0.01 percent

4.3.3.5 Data Buffer

A block diagram of the preprocessor data buffer is shown in Figure 65. The data buffer receives inputs from the data demodulator on two lines. One line carries the NRZ data, and the other carries the bit-synchronization signal. At the beginning of each frame, data is continually fed to the frame-sync detector, which contains an 11-bit register and cross-correlation detection logic. Each bit-sync pulse shifts the contents of the register while the incoming data bit is entered. During each bit time, the contents of the register are added, modulo 2, with a hardwired Barker synchronization code. The output is fed to a summing network, and a threshold level test is performed. When correlation is sensed, a frame-sync pulse is generated to reset the bit counter, word counter, and parity check logic in preparation for processing the succeeding data.

Following the establishment of frame synchronization, the data is shifted into the data register while each bit-sync pulse increments the bit counter. Parity is computed by toggling a flip-flop each time a "one" bit is sensed. When the bit counter reaches the eleventh state, the computed parity is compared with the received parity bit. If a positive check occurs, an interrupt signal is fed to the computer interface to provide a data-ready signal for sampling of the word. The contents of the word counter are provided to aid interpretation of the data. Following the interrupt signal, the bit counter is reset, and the word counter is incremented by one. This procedure is repeated for each word of the data frame. If the parity check on any word indicates an error, the data buffer is reset and a parity error signal is fed to the user equipment. Completion of the data frame preprocessing is indicated when the interrupt signal occurs with the word counter in the fifteenth state. The data buffer is cleared and is prepared for sync detection of the data frame from the next satellite in sequence.

For users who intend to find position fix by manual calculations, the preprocessor provides outputs on a selected satellite basis. This is performed by satellite identification logic in the data buffer. The selection logic contains a register that receives four bits of the first data word following frame sync. These bits contain the satellite-identification code and are compared with the code received from the selector on the user display

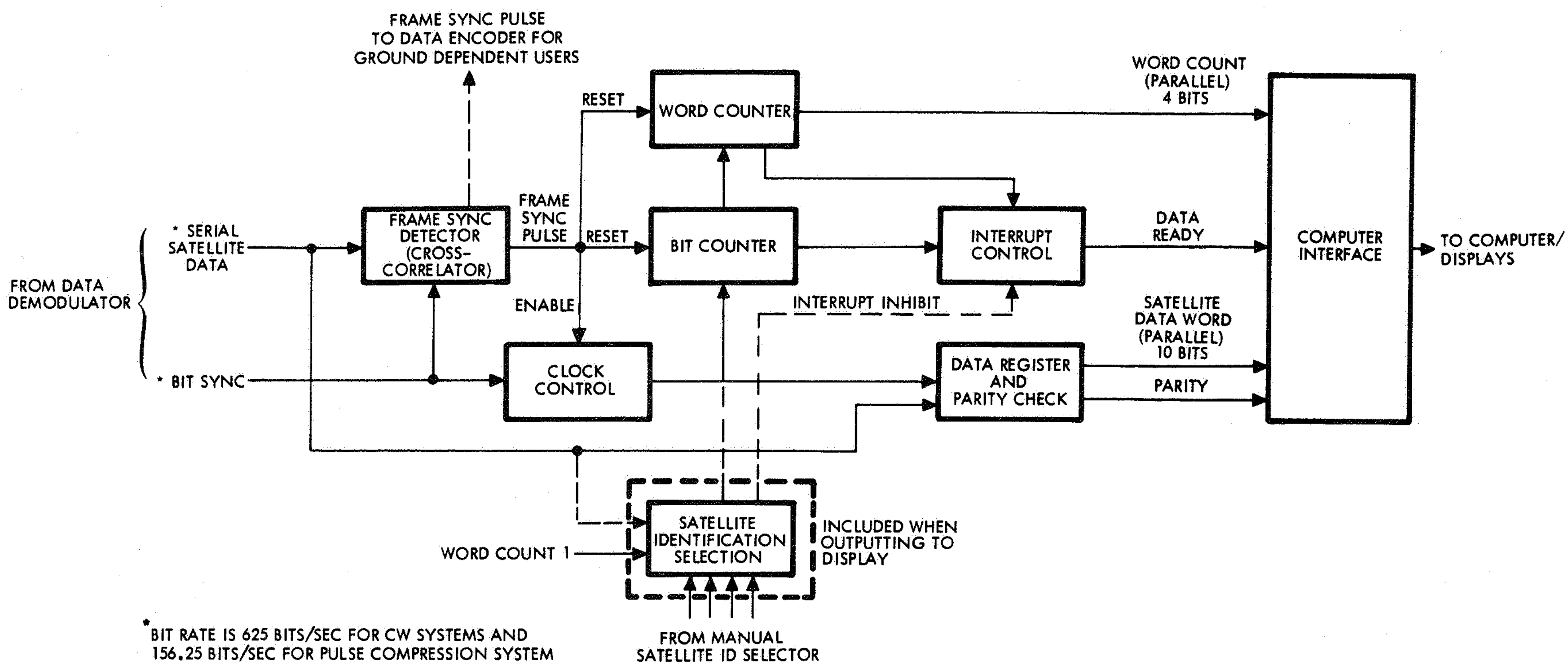


Figure 65. Block Diagram of the Preprocessor Data Buffer

panel. All interrupt signals to the display panel are inhibited, except those that occur during the data frame containing the matching satellite identification code. Hence, only data from the selected satellite are displayed for the user. The selection logic may be omitted for those users equipped with an onboard digital computer.

For users employing the automatic/ground-dependent configuration, a data encoder is required. This element stores the range measurement and satellite data at the incoming bit rate and then feeds this information to the transmitter/modulator for transmission to the ground-based computer for position-fix calculations.

The range measurement is transferred in parallel to a holding register upon receipt of the range data interrupt signal. The satellite identification and ephemeris data are gated to the encoder storage directly from the data demodulator when the data buffer indicates that frame sync has occurred.

Upon indication of frame complete, the user control may initiate transmission. A new frame sync word is generated and the data is shifted out of the encoder at the transmission bit rate.

4.3.4 PULSE COMPRESSION PREPROCESSOR DESIGN

4.3.4.1 Introduction

The primary functions of the Pulse Compression Preprocessor are to perform the range measurement on the pulse compressed data, to decode the PPM data, and to provide the required computer interface through proper timing and formatting.

The inputs to the preprocessor are the pulse trains shown in Figure 66. As explained in (subsec. 4.2) two lines at different threshold values are available from the receiver. In a good signal-to-noise environment, the waveforms are identical; in more typical situations however, the signals will differ in the false pulse detection and bit-error rates.

The demodulated signal consists of two subgroups corresponding to the two types of information required by the NAVSTAR user, ranging data and satellite position data. The first subgroup consists of five 200-nsec ranging pulses spaced at 1/PRF intervals or 12.8 nsec (PRF = 78.125 Hz).

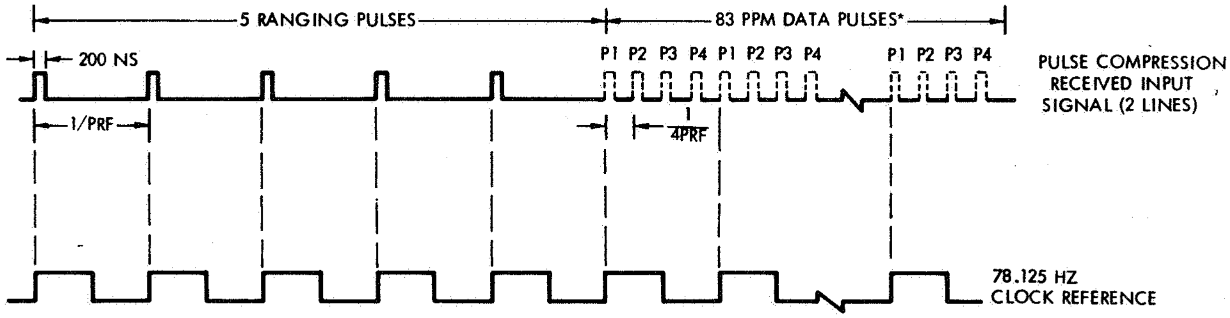


Figure 66. Input Waveform to Pulse Compression Preprocessor

Each individual pulse in this second subgroup can occupy any one of four equally spaced positions (P_1-P_4) in the 12.8-nsec time interval.

The block diagram of the pulse compression preprocessor (Figure 67) shows the major elements of the preprocessor which are discussed in greater detail below. (The data buffer and computer interface units are identical with those described in the BINOR preprocessor system. See pars. 4.3.3.5-6 for further details.) The range measurement is performed through circuitry in the Coincidence Detector and Range Decoder units. PPM decoding of satellite position data is accomplished by the data demodulator/sync detector and data buffer units. The reference oscillator whose frequency is 50 MHz provides the master clock timing throughout the preprocessor.

4.3.4.2 Coincidence Detector

An expanded block diagram of the coincidence detector is shown in Figure 68. Two coincidence channels are employed to minimize the possibility of lockup of the ranging determination circuitry from a false trigger. If one counter has been triggered by a noise spike, the second counter can take over the coincidence task.

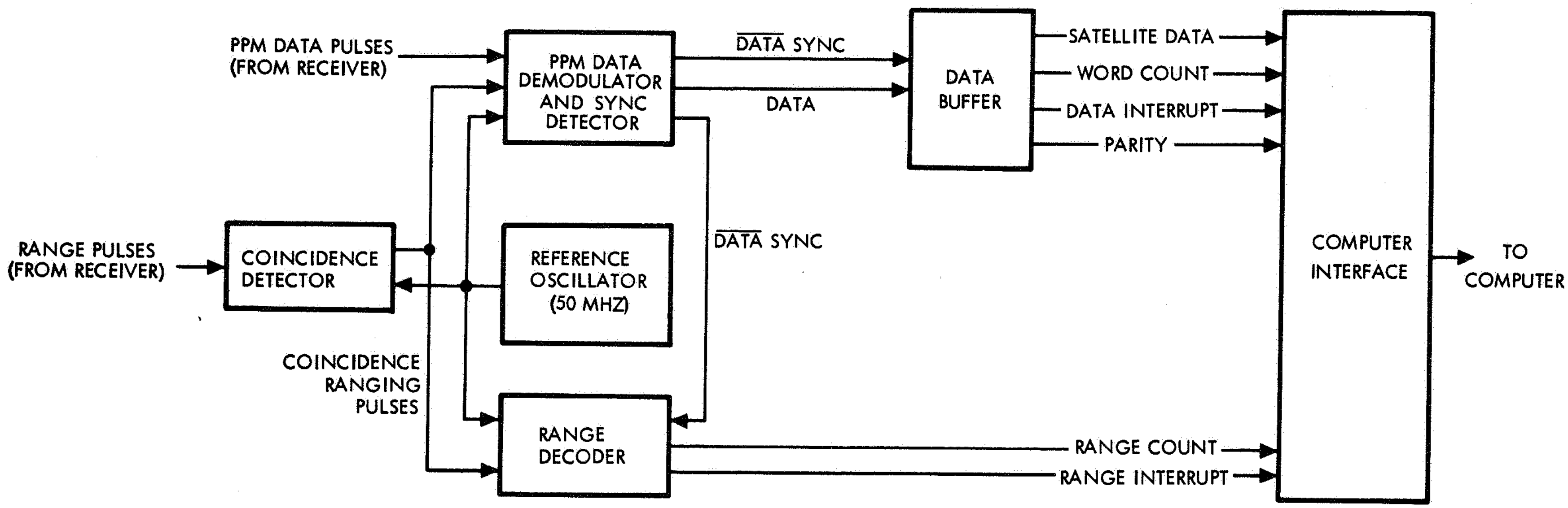


Figure 67. Block Diagram of Pulse Compression Preprocessor

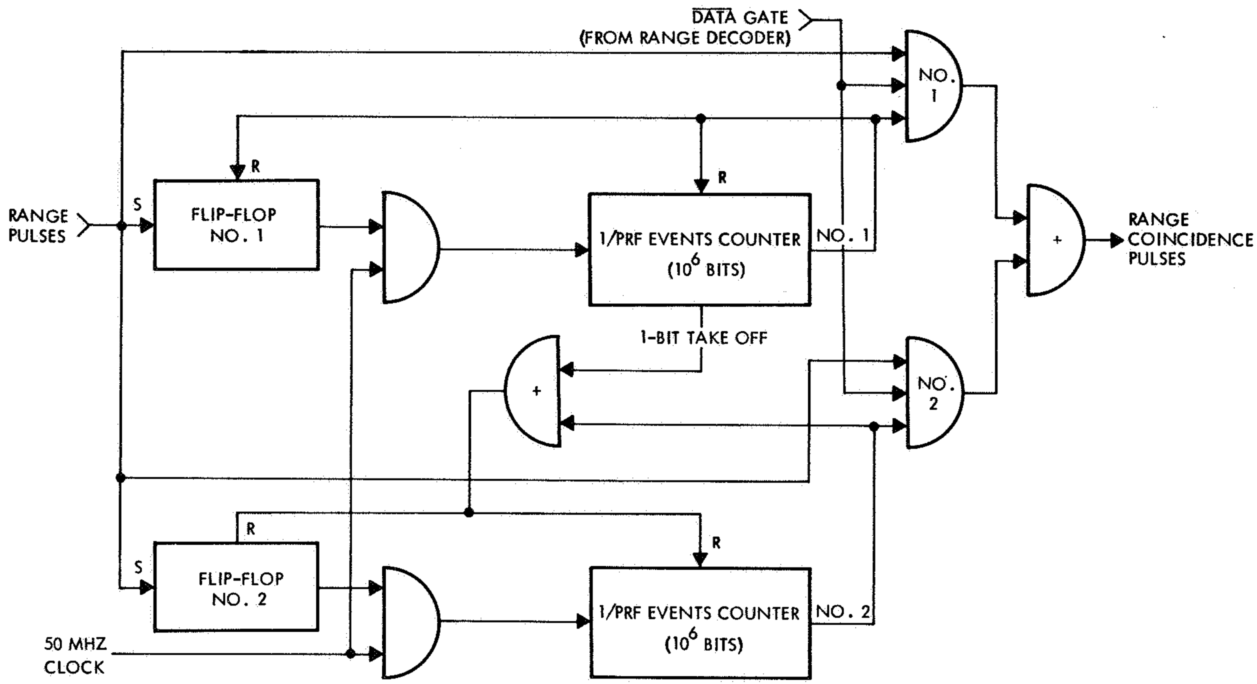


Figure 68. Coincidence Detector

The first range pulse received triggers flip-flop No. 1 which enables the 50-MHz clock pulses to be counted by events counter No. 1. Pulse spacing of the clock corresponds to 20-ft range increments of which there are approximately 6 x 10^5 for a 2000-mi differential range. Therefore, the storage capability of the counter is approximately 10^6 events and its clocking speed is 50 MHz.

At exactly one PRT following the initiation of the count, the counter automatically resets itself at flip-flop No. 1 and delivers an output to AND Gate No. 1. If the first received pulse is a true ranging pulse, the second ranging pulse will be present in time coincidence with the first pulse delayed by one PRT by the counter.

Twenty nsec after the events counter No. 1 has begun counting, FF No. 2 and events counter No. 2 are reset and this second coincidence channel is ready to accept the next ranging pulse. The sequence of operations is the same as for coincidence channel No. 1 and an OR Gate delivers the resulting coincidence ranging pulses from either channel.

To prevent possible coincidences during the data pulse train, the coincidence detector is disabled when the data sync pulse is generated. Thus, the only outputs from the coincidence detector are the four coincidences derived from the five ranging pulses.

4.3.4.3 Range Decoder

The range decoder block diagram is shown in Figure 69. The 50-MHz master clock signal is divided (in two separate steps) to provide a PRF clocking rate of 78.125 sec. Coincidence ranging pulses and the PRF clock signal are first checked for exact coincidence, since this condition is possible though not very probable. Remaining processing measures the average time difference between the PRF clock pulses and the four coincidence pulses.

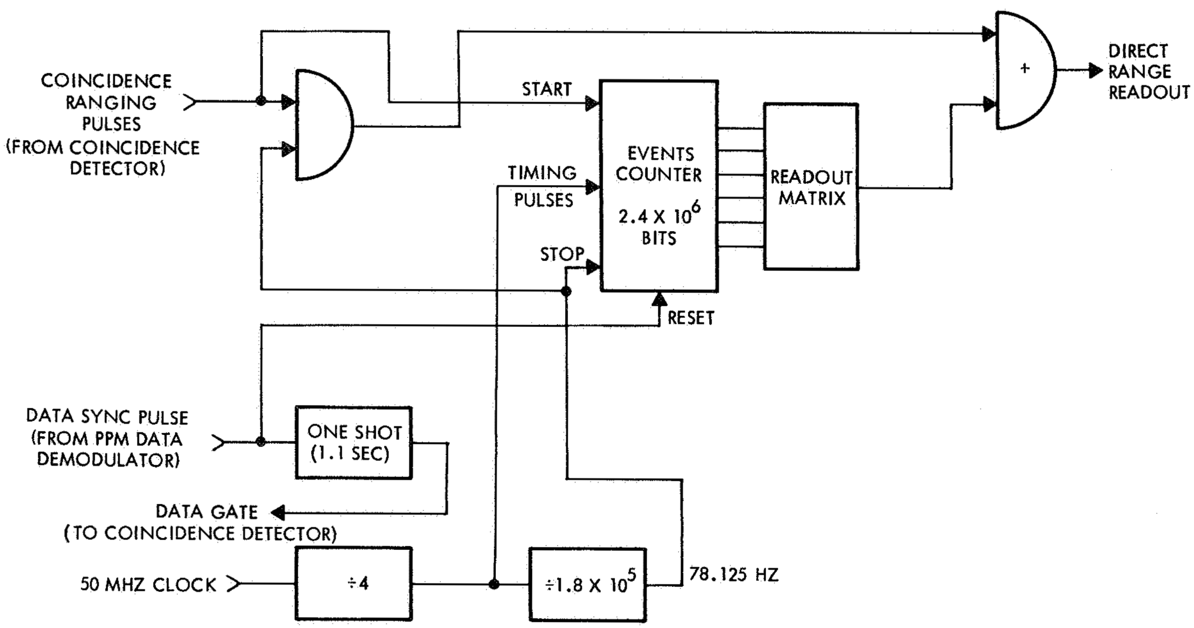


Figure 69. Range Decoder

To provide direct range readout, the master 50-MHz clock is divided by four to act as the time base for the events counter. The counter is started upon receipt of each coincidence ranging pulse and stopped upon receipt of each PRF clock pulse. The readout matrix then delivers an output which is the accumulated range difference divided by four.

The counter is reset upon the arrival of the next data sync pulse to allow a new count to begin.

After a sufficient time has elapsed for all the data pulses (plus a guard period) to have been processed, a gate is formed by the 1.1-sec one-shot to inform the ranging circuits that new ranging determinations are to begin.

4.3.4.4 PPM Data Demodulator

The PPM data demodulator (Figure 70) is enabled only upon recognition of the receipt of the sync word comprising the detection of the four coincident ranging pulses. When all four are counted by the divide-by-four circuit, a flip-flop removes a low-impedance shunt from an astable multivibrator clock which then begins its timing cycle at a period $\frac{T}{2}$ (T is the desired width of the gate to surround the data pulses). T is preferably no wider than absolutely necessary to minimize false alarms, i.e. no wider than about two signal pulsewidths (about 0.5 msec).

The data clock (the output of the astable multivibrator) drives another -4 circuit to generate four gating signals equally spaced over the 1/PRF time interval. The appropriate timing and logic signals can best be understood by reference to the waveforms in Figure 71. The gating signals, G, -G4, trigger corresponding one-shot circuits, used to detect the presence of a PPM pulse at any of the 4 phase intervals. Whenever a pulse is recognized it sets its designated flip-flop as shown by the typical coding scheme in Figure 71.

A decimal to binary converter is used to convert the information on pulse position from decimal (4 lines) to binary (2 lines) notation. Appropriate gating circuitry is applied to the converter output so the position data are read out serially at a bit rate of 156.25 b/sec.

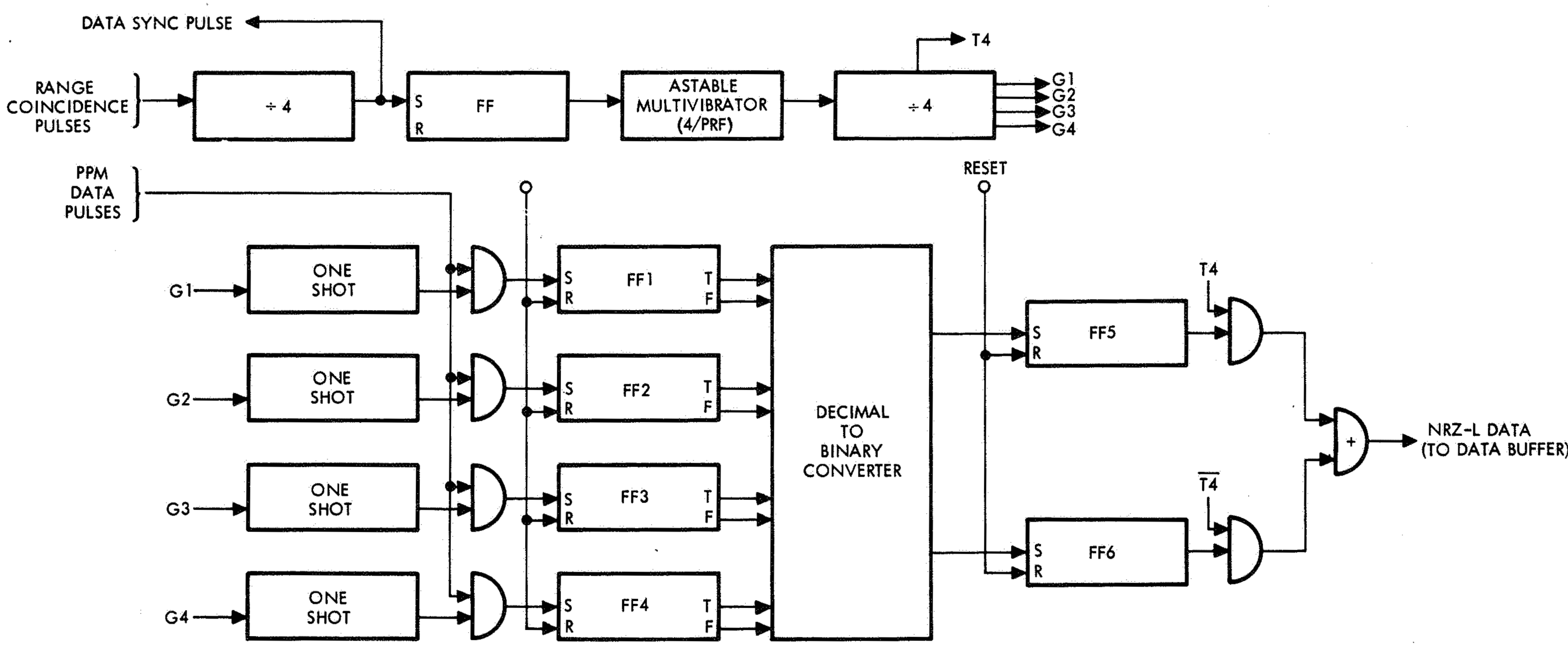


Figure 70. PPM Data Demodulator

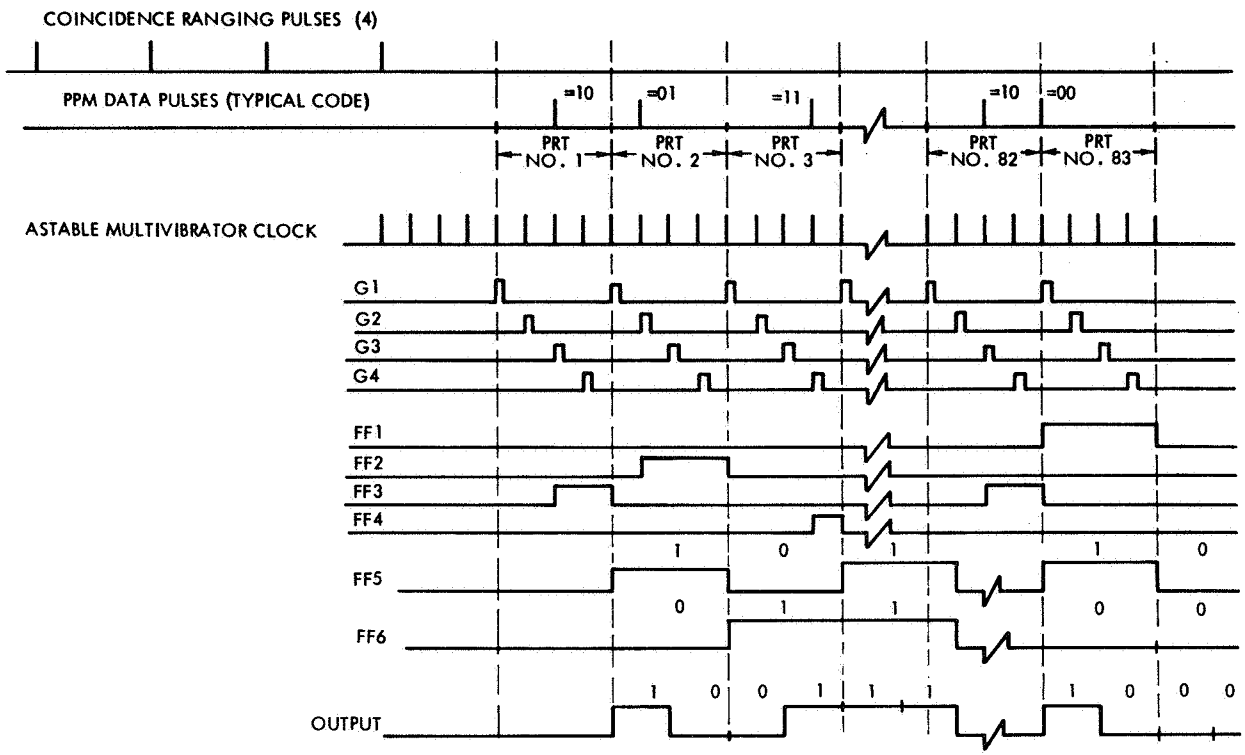


Figure 71. PPM Data Demodulator Waveforms

4.3.5 FIXED-TONES PREPROCESSOR DESIGN

4.3.5.1 Introduction

A simplified block diagram of the preprocessor for the fixed tones system is shown in Figure 72. The preprocessor will be identical to the BINOR code preprocessor except in the range acquisition and measurement functions provided by the range-tone filters and range-measurement logic. The range-tone filter unit takes the composite signal of five tones from the receiver and filters each of the tones individually to obtain a clean (high signal-to-noise ratio) replica of the tones for fine and coarse range measurement. The range-measurement logic converts the tone phases to a measurement of the unambiguous range.

The data signal conditioner and bit synchronizer, data buffer, and computer interface units are identical to those included in the BINOR code preprocessor (see par. 4.3.3.3-6 for a description of their design and operation).

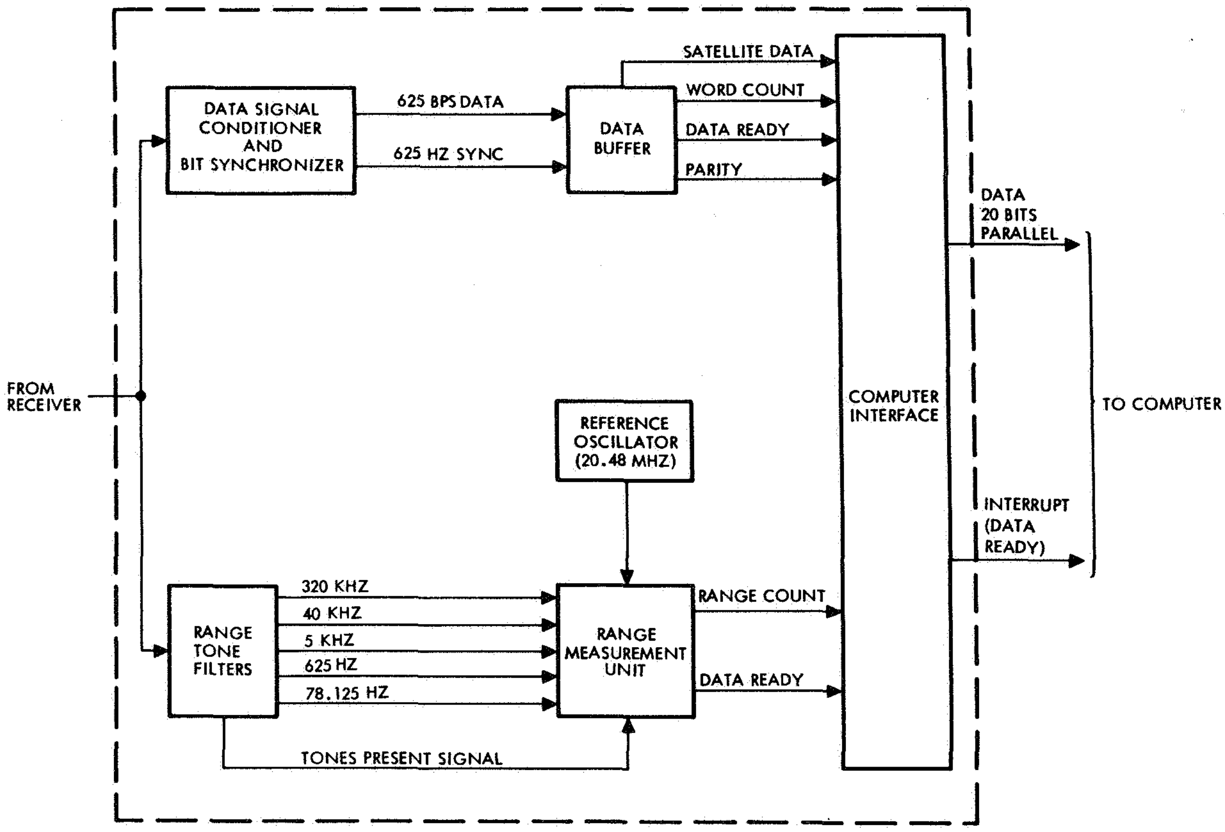


Figure 72. Preprocessor Block Diagram Fixed Tones

4.3.5.2 <u>Range Tone Filters</u>

This unit consists of five phase-lock tracking filters and phase-lock indicators as shown in Figure 73. The lock indicators consist of a quadrature phase detector and voltage threshold detector which are necessary to tell the range-measurement logic when the tone phases are correct for a range measurement. The need for five tracking filters instead of passive filters has been assumed, since careful control is required of the phase shifts from filter input to output. Further design studies are necessary to determine whether or not some or all of the filters can be replaced with simpler narrowband passive filters. The phase stability of the passive filter will have to be excellent despite aging, frequency, and environmental changes. If a passive filter replaces a tracking filter, the lock indicator can be replaced by a voltage threshold detector at the output of the filter.

The lower frequency tones can be translated up if filtering requirements dictate that this is desirable. For example, the 78.125-Hz tone

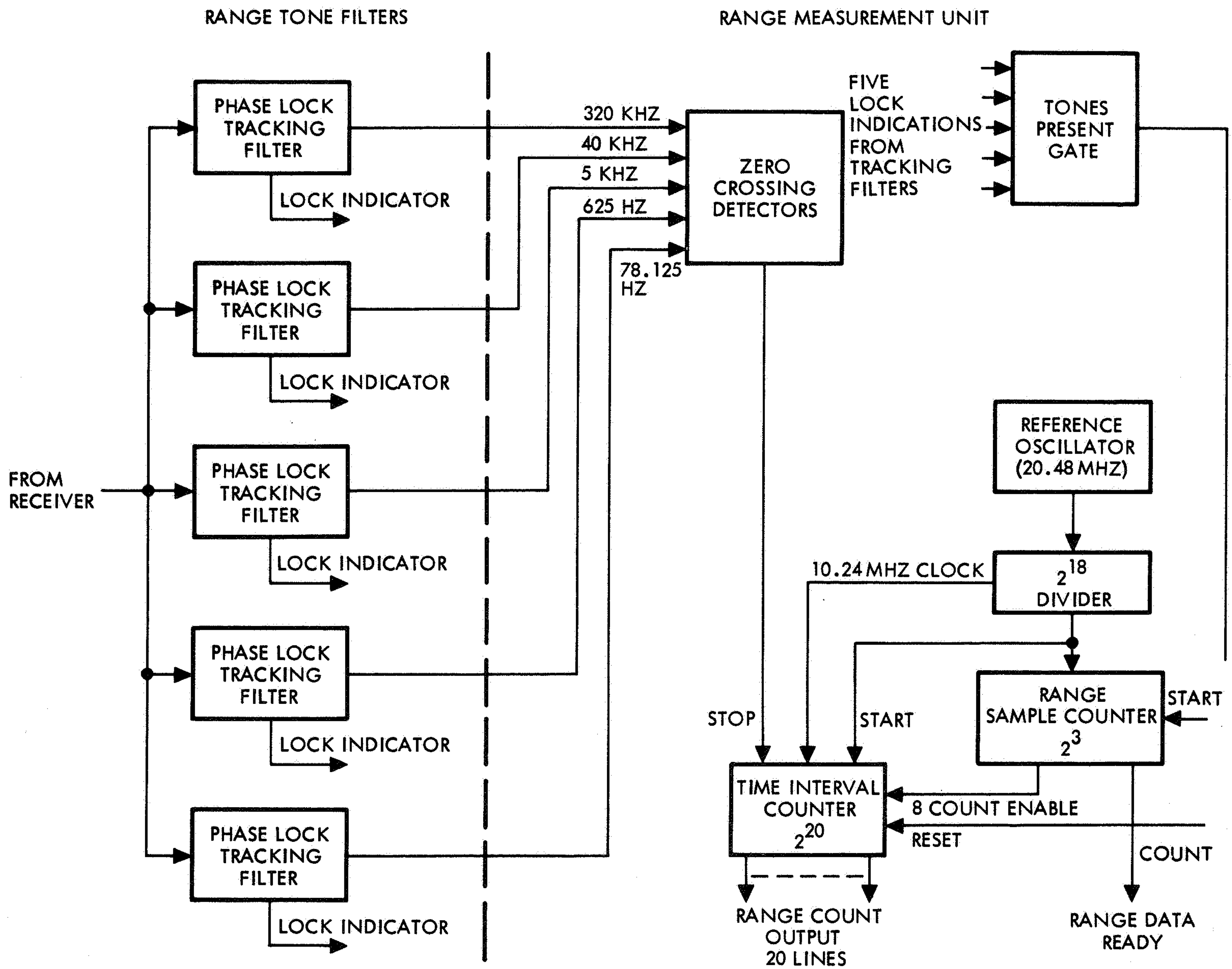


Figure 73. Block Diagram Fixed Tone Filters and Range Measurement Unit

can be replaced by a 45.078125 kHz tone (derived from 40 + 5.0 + 0.078125-kHz translation). The translations can be done at the transmitter so that the preprocessor will be the same except for the center frequency of the filters.

4.3.5.3 Range Measurement Unit

A block diagram of this unit is also shown in Figure 73, to the right of the dotted line. The logic is nearly identical to the range-measurement unit of the BINOR code (Figure 62) except for the zero-crossing detectors. The latter detect the common zero-crossing point of all five tones and put out a pulse for the time-interval counter at the occurence of this event. Common zero crossings will occur at the same frequency as the lowest tone frequency (78.125 Hz). The tones present gate puts out a pulse when all five lock indicators from the tone-tracking filters are positive. This pulse resets the time-interval counter to zero and starts the range-sample counter. Eight range samples are measured by the time-interval counter in the same way as for the BINOR code. At the end of eight samples, a range-data-ready pulse is generated and the 20-bit range word is read out of the time-interval counter by the computer interface. The operation of the time-interval counter and range-sample counter are essentially identical to those in the BINOR code preprocessor (see par. 4.3.3.3 for additional details).

4.4 COMPUTING SUBSYSTEM

4.4.1 INTRODUCTION

4.4.1.1 User Configurations

There are many possible NAVSTAR user configurations capable of being grouped into different categories of cost, accuracy, fix rate, and military/commercial applications as discussed in sec. 1. In this study, however, primary attention has been directed towards generating design and cost data for two major configurations:

1) Supersonic aircraft (SST)

2) Small-to-medium size marine vessels.

For the former, it will be demonstrated that the computing subsystem requires a digital computer. For the latter, only manually aided electronic calculators are recommended.

Other configurations have also been explored but in considerably less detail. These include subsonic aircraft (general aviation), military aircraft, and ocean liners.

4.4.1.2 Method of Attack

The approach taken in mechanizing solutions to the computing subsystem requirements for the specified NAVSTAR user has been different from the ones taken for the other user hardware subsystems. The reason for this is the high degree of standardization and versatility which is characteristic of the stored-program digital computer. A general-purpose computer which has been designed and constructed for one set of avionic applications will probably be adaptable to an equally complex, albeit different, set of avionic requirements. With the possible exception of the display subsystem, off-the-shelf hardware for the other NAVSTAR subsystems does not exist. With this thought in mind, the study effort performed in the computing subsystem area has consisted logically of two parts:

1) Transformation of NAVSTAR user equations into generalized computer specifications

2) Survey of state-of-the-art candidate computing systems which could be used for the NAVSTAR program.

4.4.1.2.1 Transformation of NAVSTAR Equations

The specifications for the computing subsystem have been derived by evaluating the appropriate NAVSTAR user equations for determining position. In addition, certain allowances have been made for special-purpose processing requirements, such as displays, input/output, and self-test routines.

The NAVSTAR user equations which are analyzed in the next section are described in detail in vol. II. For convenience, Figures 74 and 75 reproduce the user equation flow charts for both the SST and the simplified version thereof. The actual equations which make up each box and their justification are given in sec. 3 of vol. II.

Late in the course of the study it was observed that the simplified set of equations (Figure 75), which operated along the same systems concept as the nonsimplified version, would not produce a significant cost reduction in hardware implementation. (See subsec. 4.4.3.) Consequently, it became necessary to think in terms of a radically new NAVSTAR system concept which would lend itself to low-cost hardware mechanization for slow-moving and low-accuracy users. The result was the MInimum Navigation Satellite COmputations (MINSCO) technique which is described briefly in sec. 3 of this volume.

4.4.1.2.2 State-of-the-Art Surveys

After preliminary computer specifications were generated, an industry-wide survey was conducted to determine the availability, suitability, and cost of possible candidate NAVSTAR computer systems. Not all computer manufacturers were solicited, only those who are active in the avionics field and who are under contract to either a military or commercial agency for delivery of their proposed NAVSTAR computer system.

In addition, each company participating in the survey was encouraged to extrapolate the 1970-1975 costs based on the projected fruition of "blue-sky" designs now on the drawing boards. Because of the proprietary nature of such data, only general price guidelines were expected along with the identification of the key technologies which would be responsible for improvement in 1970-1975 computer costs and performance capabilities.

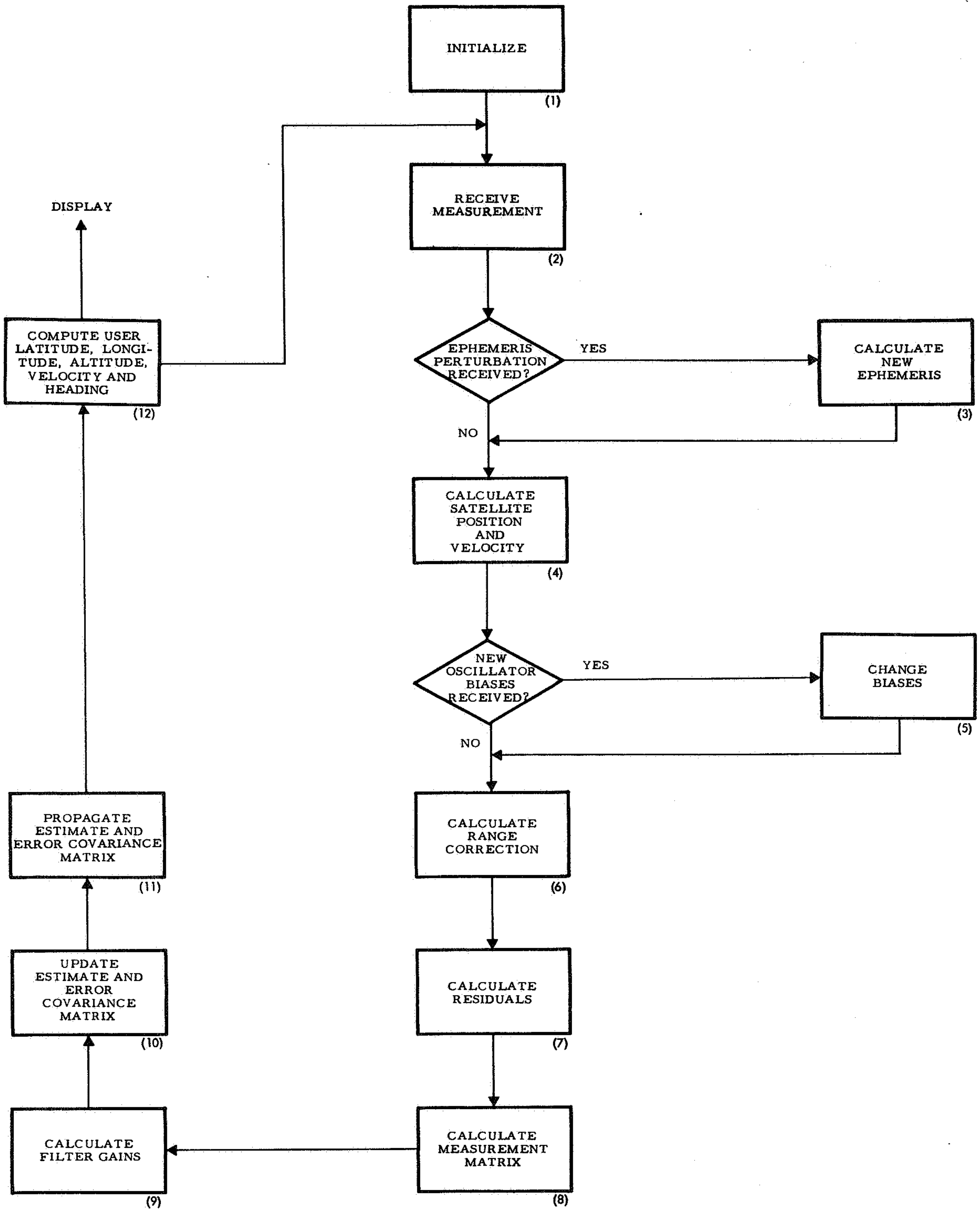


Figure 74. Flow Chart of SST NAVSTAR User Computations

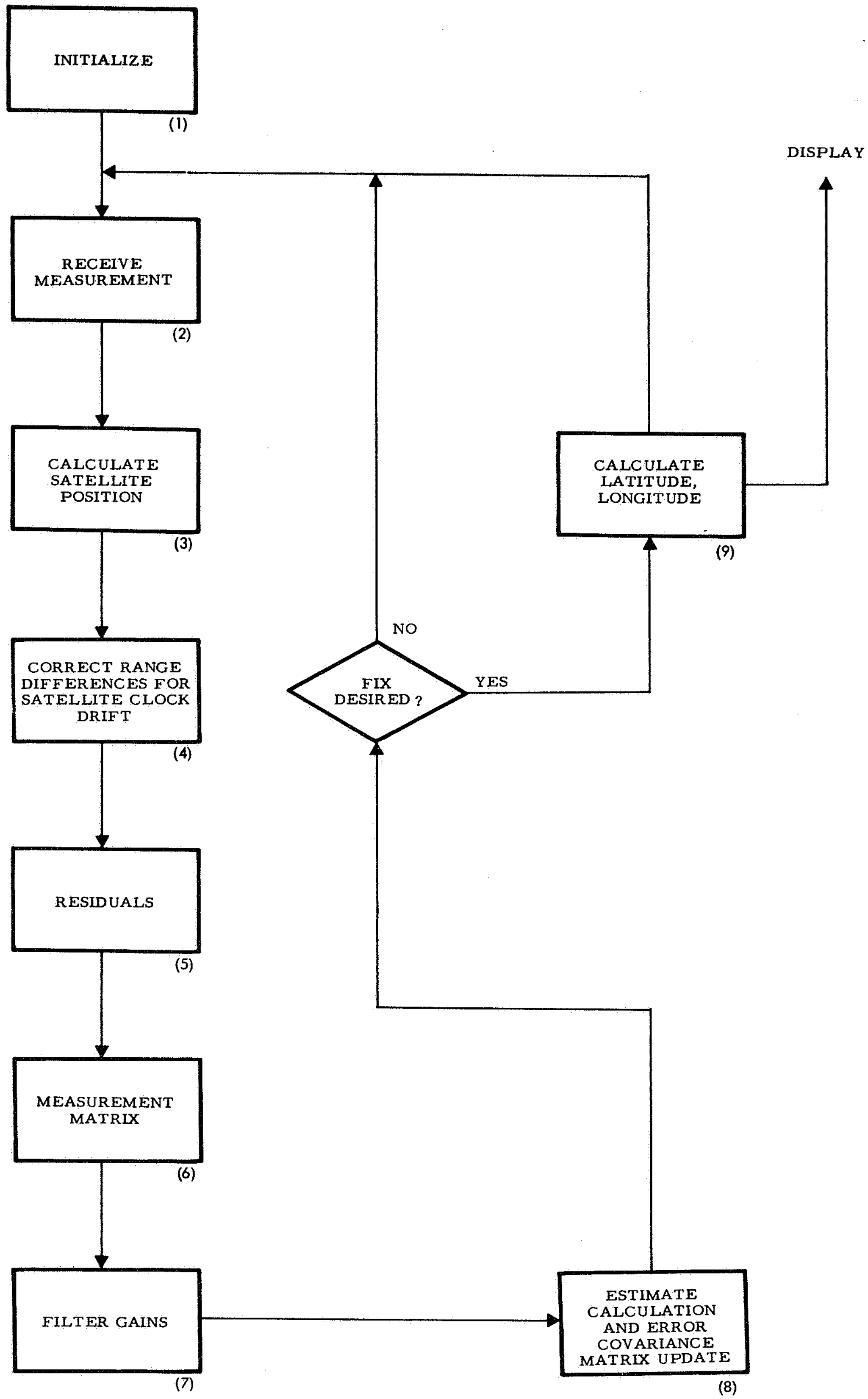


 Figure 75. Flow Chart of Simplified NAVSTAR User Computations

A second survey of computational equipment was required for the inexpensive user, i.e., the operator of small-to-medium size marine vessels, who would be the prime beneficiary of the MINSCO NAVSTAR technique. The types of hardware suggested by the simple arithmetical equations required in the MINSCO system are electronic calculators and/or desk-top computers.

4.4.1.3 Outline of Other Sections

Subsec. 4.4.3 on computer sizing describes the programming techniques used to determine the memory size, execution rate, and the word length of the computer subsystem. The results of this analysis are necessarily less refined than would be possible with more sophisticated and expensive techniques. Recommendations for continued refinement of the specifications by simulation techniques, are made in subsec. 4.4.7.

Subsec. 4.4.4 describes the survey that was made of computer equipment meeting the specifications determined in subsec. 4.4.3. To establish as broad a base as possible for survey purposes, the specifications were made very general. A large number of computer manufacturers were queried on their product lines, and replies were received from ten. Descriptions and costs of computers currently available off-the-shelf and meeting the general requirements are included.

Subsec. 4.4.5 describes desk-calculator equipment that could meet the needs of the small marine craft user. The prices listed are for single unit buys; therefore, it is highly probable that the potential costs for multiple units (should these be supplied as part of the user package) could decrease significantly.

4.4.2 SUMMARY

4.4.2.1 General

Analysis of the NAVSTAR user computational requirements resulted in three levels of computing complexity based primarily on the accuracy and rate of update demanded by the user. Established goals were:

1) For supersonic aircraft — better than 0.1 nmi in position error and an update rate of no less than once per minute.

2) For general aviation — less than 1.0 nmi in position error and update rate of once every 15 min.

3) For the small marine craft — 1.0 nmi in position error with present position updated once per hour.

To determine memory size, execution rate, and data word length for the computational subsystem, the sets of equations derived in sec. 3 of vol. II were analyzed. For the supersonic aircraft a medium-speed computer with 4,096 words of memory was capable of providing the required accuracy and update capability (see Table XVIII). For the general aviation user a computer with 2,048 words of memory was adequate. For the small marine craft user, the relatively simple set of calculations could be handled using only a small calculator, paper, and pencil.

4.4.2.2 Availability of Off-the-Shelf Hardware

Unlike the other NAVSTAR user hardware subsystems, off-the-shelf hardware which is capable of handling the user requirements is available for immediate delivery and in most instances has considerable excess handling capacity.

TABLE XVIII

SUMMARY OF NAVSTAR USER TOTAL COMPUTER MEMORY REQUIREMENTS

Computational Requirements	NAVSTAR User Configuration	
	SST (No. of Memory Locations)	General Aviation (No. of Memory Locations)
Positional determination	1750	840
Display processing Input/output processing Computer self-test	1000	500
Data (constants and variables)	500	250
Spare	846	458
Total	4096	2048

4.4.2.3 Generation of Preliminary Computer Specifications

Analysis of the TRW NAVSTAR user equations resulted in the establishment of the processing requirements for the NAVSTAR computer system as shown in Table XIX. The values given are required for position determination alone.

From data on the memory size, processing time, word length, addressing, interrupts and input/output requirements, a generalized set of preliminary specifications was devised (Table XX). It should be emphasized that the specifications exhibit no a priori equipment biases; they reflect only the minimum computational capability required to perform within the constraints of the TRW proposed NAVSTAR system.

4.4.2.4 Results of Computer Survey

Of 15 major manufacturers of airborne computers, 10 elected to match their available equipments against TRW performance specifications. As indicated in Table XXI, a large number of off-the-shelf computers are capable of handling the user requirements and have considerable excess computing and data handling capacity. Current estimates, however, show that over 1/2 the cost of computers is associated with the memory module, and future trends in integrated circuit development forecast that in 1970-75 as much as 90 percent of the computer cost will be in the memory subsystem. Thus reducing the computer capability will not necessarily provide any meaningful overall cost reduction. Furthermore, the existence of extra computing capacity may not be excessively high considering the potential growth requirements such as air traffic control, collision avoidance, etc.

TABLE XIX

PROCESSING REQUIREMENTS FOR NAVSTAR COMPUTER SYSTEM

Configuration	Memory Locations (No. of Words)	Arithmetic Operations	
		No. of Long Instructions	No. of Short Instructions
SST user equations	1750	1270	1700
Simplified user equations	840	558	515

TABLE XX

NAVSTAR COMPUTER TYPICAL CHARACTERISTICS

Organization:	General-purpose
Memory:	Random-access core, 4096 words expandable to 8192, nonvolatile DRO operation
Word length:	≥21 bits including sign
Arithmetic:	Binary, 2's complement, fixed point fractional
Add time:	$\leq 50\ \mu$sec
Multiply time:	$\leq 500\ \mu$sec
Indexing:	≥3 index registers
Interrupt capability:	One external interrupt
Input/output:	One serial direct input/output channel at 250 kHz; 6 each input/output discretes
Size, volume, weight, and power:	Minimum for stated requirements
Environment:	To be installed in supersonic aircraft

Present computer costs for quantity buys range from $13, 000 to $35, 000 with an average of about $23, 000. Projection into the 1970-75 era indicates that for the supersonic craft, quantity buys will range from $10, 000 to $15, 000; for general aviation, from $5, 000 to $10, 000; and for the small marine craft user, from $500 to $1, 000.

Should major breakthroughs occur in the development of low-cost memories for airborne environments, these costs would drop in proportion. Promising developments on batch-processed memories could result in significant decreases. Successful developments coupled with current trends in large-scale integration (LSI) could result in NAVSTAR computers being available for SST applications for less than $10, 000; general aviation computers for less than $5, 000; and small marine craft computers for several hundred dollars.

TABLE XXI

SUMMARY OF NAVSTAR SST COMPUTATION CAPABILITY FOR EXISTING HIGH PERFORMANCE AIRBORNE COMPUTERS

Computer	Model No.	Approximate Time Required to Make TRW NAVSTAR Computation*	Word Size	Memory** Capacity (No. of Words)	Approximate Unit Cost (In Large Quantities)
General Electric	M-355	17 msec	36 bits	4 K (16 K)***	$40 K
Teledyne	CCC	32 msec	20 bits	4 K (8 K)	$13 K
Univac	1818	35 msec	18 bits	4 K (12 K)	$14 K
Hughes	HCN-305	35 msec	18 bits	4 K (16 K)	$20 K
Nortronics	NDC-1060	43 msec	28 bits	4 K (16 K)	$33 K
Autonetics	D26J	74 msec	16 bits	1 K (16 K)	$35 K
Litton	LC-728	86 msec	28 bits	4 K (32 K)	$31 K
IBM	4π-TC	109 msec	8 bits	8 K (16 K)	$20 K
Control Data	5360	135 msec	24 bits	8 K (32 K)	$18 K
AC Electronics	MAGIC 311	263 msec	12 bits	6 K (8 K)	$27 K

*For position determination, instructions required: 1700 add, 1300 multiply.

**NAVSTAR requirement: 1750 word locations for position determination, and 4 K overall total.

***( ) = Expandable to.

4.4.3 COMPUTER SIZING ANALYSIS

The basic design considerations discussed below reflect the influences of the NAVSTAR computational requirements and the state-of-the-art in computer technology. The specification for the NAVSTAR computer (Table XX), which resulted from the computer sizing study, describes a device which is well within the capability of existing equipments yet provides a relatively large margin for error or expansion. The techniques for generating the specifications are not new or unique but represent established methods of estimating. It is felt that high confidence exists in the derived values since the specification seems to represent an upper-performance bound.

4.4.3.1 Memory Size Analysis

Two independent methods of estimating memory requirements were employed in the study: one technique utilizes a tally of estimated operations and the other extrapolates memory requirements based on coding projections. The total number of memory words estimated by each of the two methods correlated within 5 percent.

The estimating techniques which are described in the subsequent paragraphs have been employed on a number of TRW programs and have resulted in very reliable memory estimates. In fact, all errors estimated are on the high side to provide a margin of safety. It should be noted that the application of these techniques provides an estimate of memory requirements, not execution time. Subsec. 4.4.3.3 will describe the method for estimating this latter quantity.

Table XIX gives the total memory requirement as 1750 storage locations for processing the NAVSTAR user equations on position determination. Additional processing requirements include:

1) Display processing
2) Input/output processing
3) Computer self-test.

A conservative estimate, based on similar processing for other projects, indicates that about 1000 locations would be a reasonable maximum for these three items. The actual numbers will, of course, depend on the characteristics and operation of the devices that are addressed by the computer and on the input/output characteristics of the computer. If another 500 locations are set aside for data, both constants and variables, total actual memory requirement will be 3250 locations. Selection of a 4096-word memory should provide some margin for special requirements, such as double-precision computation (which depends on word length) or the implementation of inner and outer loops (which depends on execution rate).

The equations for the general aviation user were also analyzed to estimate probable memory size. Using the same techniques described above, an estimated 2048 words were considered adequate. The actual number of memory locations is about 1500, but since memories generally come in at least 1024-word increments, the requirement was set at 2048 words. As indicated above, the unused memory provides an adequate margin for special requirements.

4.4.3.1.1 Estimate by Operation Count

The most common expressions encountered in computation can be shown as:

$$y = (x.y.z + a) \tag{1}$$

$$y = (a.x + b.y) \tag{2}$$

An analysis of the elementary coding requirements of these two expressions would reveal that Eq. (1) requires five instructions (CLAX, MPYY, MPYZ, ADDA, STORESUIT), and Eq. (2) requires seven instructions (CLAX, MPYA, STOAX, CLAY, MPYB, ADDAX, STO RESULT). Both expressions contain only three arithmetic instructions; the remainder are load and store instructions.

If we double the number of arithmetic operations in the expressions and temporarily ignore the other coding requirements, the new figure of six will allow for one unnecessary instruction in estimating the coding requirements for Eq. (1) and will be short by one for Eq. (2). If we hypothesize that the expressions to be evaluated are an evenly divided mixture of these two, then the technique of counting the arithmetic operations and doubling them should provide a reasonable estimate. No provision for scaling and housekeeping has been made, but a factor of 15 percent added to the total provides adequate coverage.

The calculation of special functions, such as trigonometric functions, matrix operations, and square roots is usually handled by subroutines; they are coded once and special linkage instructions are invoked for each requirement to compute the function. The number of storage locations included for each linkage depends upon the frequency of subroutine use. The number of calls are counted for each subroutine and this number is multiplied by the number of linkage instructions for the particular subroutine. Then, the number of instructions required for the subroutine library is added and the total is the number of memory locations required.

Example of Estimate By Operation Count. Let us estimate the number of operations required to compute the values $\hat{x}$, $\hat{y}$ and $\hat{z}$ whose equations are:

$$\hat{x} = v\,(\sin\phi\ \cos\lambda\ \cos\psi\ \sin\lambda\ \sin\psi) \tag{3}$$

$$\hat{y} = v(\sin\phi\ \sin\lambda\ \cos\psi - \cos\lambda\ \sin\psi) \tag{4}$$

$$\hat{z} = v\,(\cos\phi\ \cos\psi) \tag{5}$$

Eq. (3) requires four multiplies and one add for a total of five arithmetic operations; Eq. (4) also requires five operations; while Eq. (5) requires two. The total number of arithmetic operations for the 3 equations is therefore 12 which when doubled is 24; adding 15 percent gives the 27 required locations. However, if instead of estimating, we were to perform direct coding of the 3 equations, this would result in 22 instructions, 2 temporaries, and storage for the values of $\hat{x}$, $\hat{y}$, and $\hat{z}$, for a total of 27 locations. Hence, in this illustration, which is quite typical, we observe that the estimate was very precise (assuming, of course, that the transcendental functions $\sin\psi$, $\cos\psi$, $\sin\phi$, etc., have previously computed and stored).

4.4.3.1.2 Estimate by Coding Projection

Another method employed to estimate memory size is to code various representative sections of the computation using a basic instruction set and then to extrapolate the results to an estimate of memory size for the total problem. Extremely good estimates can be achieved in this manner; however, the accuracy of the estimate generally depends upon the experience of the estimator. For example, in the calculation of filter gains (Item 9 appearing in the flow chart of Figure 73) it can be shown that coding the computation of the quantity K_{p1} can be used as a basis for estimating the memory requirements of the entire block of computation. To generate K_{p1} requires approximately 24 instructions plus matrix subroutines. The estimate is then 7 x 24 = 168 locations plus 21 for computation of B^{-1} which gives 189. Actual coding shows 190 locations are necessary.

4.4.3.2 Timing Analysis

To specify the computer execution rate, it was necessary to analyze the basic cycle of the user system operation. The following analysis was performed for the supersonic aircraft but it should be apparent that the underlying technique would apply for all other NAVSTAR user configurations.

4.4.3.2.1 Iteration Rate

A preliminary investigation of the requirements of a supersonic aircraft for accurate position fixing indicated that an update rate of once per minute could assure an instantaneous position error of less than 0.1 nmi. The satellite system broadcasts ranging information and ephemeris data over a time-division-multiplexed link in which each satellite is available every 2 sec; this is the maximum time available for processing data from a single satellite. To leave a margin for input/output functions, display processing, self-test, and possible new functions, an iteration time of 0.75 sec was selected as a measurable design goal.

4.4.3.2.2 Execution Rate

To provide a basis for analysis, a hypothetical computer instruction repertoire was divided into two classes of instructions, the short instructions (add, subtract, load, and store) and the long instructions (multiply and divide). The latter are assumed to have an execution rate of no more than 10 times the rate of the short instructions. Tables XXII and XXIII illustrate the actual number of instruction executions in terms of longs and shorts which were required for each section of the flow chart for the supersonic and general aviation user configurations. This number will generally agree with the number of storage locations except where subroutines and loop coding are employed; for example, determining the total number of instructions executed during a matrix operation depends on the matrix size, even though the program size is fixed. Formulas have been developed which permit calculation of the number of executions based on the parameters (m, n) and the particular operation (ADD, MULTIPLY, INVERSE, or TRANSPOSE).

A total of 14,400 instruction executions were required, of which 1700 were short instructions. The formula for the execution time, t, is given by the following expression:

$$s \times t + \ell \times 10\,t = 0.75$$

or

$$t = \frac{0.75}{s + 10\ell}$$

where

s = number of short instructions

ℓ = number of long instructions

t = execution time for short instructions

Using the values shown in Table XXIII, the time, t, for computing a short instruction is 52 sec. Since this number is well within the state-of-the-art of today's airborne computers, the NAVSTAR computer specification (Table XX) called out 50-μsec requirement for short instructions (the add time) and 500-μsec for long instructions (the multiply time). It is interesting to note that all the computers described in subsec. 4.4.4

TABLE XXII

COMMERCIAL AIRCRAFT (SST) COMPUTER
MEMORY ALLOCATION

*Flow Chart Block No.	Function	Memory Locations	No. of Arithmetic Operations		
			Multiply	Divide	Add
1	Initialize	50	15	--	40
2, 3, 4	New ephemeris and satellite position and velocity	90	20	--	75
5, 6, 7	Range residuals	100	15	5	75
8, 9	Measurement matrix and filter gains	275	--	5	275
10	Estimate matrix and update	240	15	--	230
11	Matrix propagation	180	50		130
12	User fix	100	10	10	75
All	Input/output	50			
All	Subroutines:				
	Sin/cos	50	200		
	Matrix function	435	775		800
	Tan^{-1}/cos^{-1}	130	60		
	Square root	50	90		
	Total	1750	1250	20	1700

*See Figure 74 in sec. 4 of this volume and sec. 3 of vol. II.

TABLE XXIII

SIMPLIFIED USER COMPUTER MEMORY ALLOCATION

*Flow Chart Block No.	Function	Memory Locations	No. of Arithmetic Operations		
			Multiply	Divide	Add
1	Initialize	20	5	--	15
2, 3	Satellite position	50	10	--	40
4, 5	Correct range difference and residuals	50	10	--	35
6, 7	Measurement matrix and filter gains	125	30	2	100
8	Estimate and covariance	85	5	--	80
9	User fix	85	10	10	65
All	Input/output	50			
All	Subroutines:				
	Sin/cos	50	230		
	Matrix function	200	90		180
	Tan^{-1}	75	30		
	Square root	50	125		
	Total	840	545	13	515

*See Figure 74 in sec. 4 of this volume and sec. 3 of vol. II.

satisfy this requirement which indicates that word length is not critical since double-precision operation subroutines could be used to minimize quantization error.

4.4.3.3 Word Length Analysis

To achieve a position accuracy to within 0.1 nmi of true position, the data or operand word length must be sufficient to permit storage and processing operations on the variables so that the quantization errors due to truncation do not significantly influence the end result. Table XXIV lists the satellite input data and their resolution requirements. (See sec. 3 of vol. II for further details.)

An analysis of the computation has shown that the resolutions suggested by Table XXIV are required if the error bound of 0.1 nmi is to be met. Further analyses by simulation of critical computations suggest that a word length of 20 bits, plus sign, would be adequate for most computations. More precise simulation, however, is still required to determine to what degree double-precision operations, or more accurately, a longer word length is required. The matrix operations for the filter calculations are most critical, and a word length of 28 to 32 bits is recommended.

4.4.3.4 Computational Requirements for MINSCO

Par. 4.4.1.2.1 points out that consideration of the needs of the user whose update rate and accuracy requirements were not critical led to the development of the computational technique referred to as the MINSCO technique. The basic assumptions underlying this technique are:

1) One hundred "reference regions" are chosen for the surface of the earth; each region consists of approximately 400 mi on a side. The center of each region is determined as a reference point and the user has the table of these points.

2) The user receives range measurements from satellites. In addition, he receives sufficient data on a voice channel to enable him to calculate his position relative to the nearest reference point by means of the following expansions:

TABLE XXIV

SUMMARY OF SATELLITE TRANSMITTAL DATA

Quantity	Definition	Maximum Value	Accurate to	Number of Required Bits
$\Delta\rho_i$	Radius perturabtion from nominal	±10,000 ft	10 ft	11*
Δi_i	Angle of ascending node of orbit from earth-fixed rectangular system	±0.524 rad	10^{-7} rad	20*
$\Delta\lambda_i$	Inclination of satellite orbit	±0.105 rad	10^{-7} rad	21*
t	Present time	86,400 sec	10^{-3} sec	27
t_i	Time of orbit nodal crossing	±1,440 sec	10^{-3} sec	22*
b_{io}	Position bias caused by satellite clock drift	12×10^6 ft	10 ft	21
b_{i1}	Drift rate of satellite clock	1 ft/min	10^{-2} ft/min	7

*Number of bits required includes sign.

$$\begin{Bmatrix}\text{User miles north} \\ \text{or south of nearest} \\ \text{reference point}\end{Bmatrix} = \begin{aligned} & K_1 (X_1 - X_{10}) + K_2 (X_1 - X_{10})^2 \\ & +K_3 (X_2 - X_{20}) + K_4 (X_2 - X_{20})^2 \\ & +K_5 (X_3 - X_{30}) + K_6 (X_3 - X_{30})^2 \end{aligned}$$

$$\begin{Bmatrix}\text{User miles east} \\ \text{or west of nearest} \\ \text{reference point}\end{Bmatrix} = \begin{aligned} & K_7 (X_1 - X_{10}) + K_8 (X_1 - X_{10})^2 \\ & +K_9 (X_2 - X_{20}) + K_{10} (X_2 - X_{20})^2 \\ & +K_{11} (X_3 - X_{30}) + K_{12} (X_3 - X_{30})^2 \end{aligned}$$

Let four visible satellites be numbered 1, 2, 3, 4; then the quantities above are defined:

X_1 = measured range difference between satellite 1 and 2. X_2 and X_3 are defined similarly.

X_{10} = range difference from satellite 1 and 2 to the reference point with correction terms such as clock drift, motion, etc. X_{20} and X_{30} are similarly defined.

$K_1 \ldots K_{12}$ are parameters determined by the geometry of the four satellites involved in the range difference measurement which are updated approximately every 15 sec by the ground track station.

As it can be seen, X_{10}, X_{20}, X_{30}, $K_1 \ldots K_{12}$ have to be received and manually or automatically stored along with the four range measurements needed to form X_1, X_2, and X_3. Once this has occurred, the two offset distances may be calculated using only 12 multiplies, 10 additions and 6 subtractions or less. Even with only a desk calculator, once the input parameters have been obtained, the fix determination time should be less than 5 min.

If the user then wishes to compute his position in terms of latitude and longitude, since the latitude and longitude of the reference point are known, the solution of a few general equations should be able to generate them.

This solution may be done directly or by calculating in incremental latitude and longitude which are added to those of the reference point to get the user's position.

4.4.4 AEROSPACE COMPUTER SURVEY

4.4.4.1 General

A number of potential suppliers were canvassed to provide data on existing off-the-shelf hardware according to the preliminary specifications for a computational subsystem (Table XX). While it was evident that the time frame for hardware for this program was five or more years away, two factors influenced the decision to solicit companies with an off-the-shelf capability and they were:

1) The trend in computer development has shown a factor of 10 or more improvements in performance every five years. If existing hardware meets the performance specification, better hardware will be available in the time frame of our study.

2) The unit cost of computer hardware has experienced a remarkable downward trend within the past five years. The continued technological breakthrough in componentry and materials processing permits us to project this trend even further into the foreseeable future.

These two factors, today's performance and cost, are therefore proposed as the upper bound with the probability of significant future improvement.

The computers described in this subsection are state-of-the-art, general-purpose digital computers. While a more cost-effective system might be developed by using a special-purpose computation subsystem, it was decided to select the general-purpose approach for several reasons:

1) The development of a special-purpose computer would entail considerable nonrecurring costs.

2) The software for such a computer would be limited.

3) Special-purpose computers have limited growth capability; this consideration is important since the possibility of adding other functions such as traffic control and collision avoidance is highly probable.

No recommendations of a particular computer have or should have been made for this report. The objective was to provide a broad survey of current technology to project the available equipments and suppliers of the 1970 to 1975 time frame.

While the computers described herein will solve the general aviation problem, it seems reasonable to assume that the reduced accuracy and less-frequent update requirements would make a less sophisticated computer more desirable. While a number of computers of this nature exist, all those surveyed were designed for commercial ground environment and would have to be ruggedized for airborne use.

Since the computing requirements for the small marine craft user did not call for a stored-program computer, a separate survey was made of desk-top calculating equipment. Subsec. 4.4.5 describes the results of this survey.

4.4.4.2 Survey Implementation

A basic assumption in the present study was that the NAVSTAR user system would be self-contained and be capable of providing the user with all the necessary data on present position, velocity, and altitude without referencing other NAVAIDS aboard the aircraft.

A large group of computer suppliers was requested to supply availability and budgetary cost data on any and all products that seemed to meet the proposed specification. Ten companies (a significant cross-section of the suppliers of airborne digital computers) replied; their proposed computers are briefly described in the following paragraphs and are summarized in Table XXV.

Each of these companies was briefed on the TRW NAVSTAR system and was asked to submit budgetary quotations for large quantity purchases of suitable computer systems. It was stipulated that no nonrecurring

TABLE XXV.

SUMMARY OF AIRBORNE COMPUTER CHARACTERISTICS

Feature	AC Electronics (Magic 311)	Autonetics (D26J)	Control Data (5360)	General Electric (M-355)	Hughes (HCM-205)	IBM (4π-TC)	Litton (LC-728)	Nortronics (NDC-1060)	Teledyne (CCC)	Univac (1818)
Word Size (bits)										
Instruction	12	12 or 16	24	18	18	18/16/24	14	14	26	18
Data	24	12 or 16	24	6, 9, 18, 36	18	16/32	28	28	20	18
Memory										
Std Size (words-bits)	6144-12	1024-16	8192-24	4096-36	4096-18	8192-8	4096-28	4096-28	4096-20	4096-18
Expandable	8192	16, 384	32, 768	16, 384	16, 384	16, 384	32, 768	16, 384	8192	12, 288
Cycle time (μsec)	26	6	6	2	2	2	2	2	2. 5	2
No. of Instructions	18	27	41	91	41	54	30	42	29	62
Execution Times (μsec)										
Add	19. 5	12	12	4	4	9-24	4-8	6	5. 7	4
Multiply	32. 5-178. 8	42 or 54	90	8	22	48-54	56. 5-58. 5	26	17. 7	22
Divide	332	42 or 54	90	10	25	48-54	108-110	28	31	22
Index Registers	0	0	28	3	3	0	0	7	3	3
Input/Output Words	32 in 32 out	1	1 in 1 out	16 exterior 32 interior	1 in 5 out	1 in 1 out	1 in 1 out	32 in 32 out	32 in 32 out	2 in 2 out
Interrupt Capability	yes	yes	yes	yes	yes	yes	yes	yes	yes	yes
Physical/Electrical										
Weight (lb)	29. 7	20	30		13. 3	17. 7	29. 4	38		43
Power (output)	169	62	105		100	65	230	180		130
Volume (cu ft)	0. 4	0. 21	0. 6		0. 2	0. 4	0. 6	0. 9		0. 39
Available Software	Assembler Simulator Diagnostics	Assembler Simulator	Assembler Simulator Diagnostics	Assembler Simulator Utility Package	Assembler Diagnostics	Assembler Service Routine Dynamic Check	Assembler Simulator	Assembler Simulator	Assembler Interpreter	Assembler Simulator
Procurements Awarded	Boeing 747	SRAM	ALR-35	In-House	In-House V-FAP	TIAS	Joint Task Force II	C5A	AAFSS	ILAAS
Operational Date	January 1968	August 1967	August 1967	Early 1968	November 1966	June 1967	January 1968	November 1967	August 1967	January 1967

development costs were to be involved and, if a company had a group of computers that satisfied the requirements, only the least costly was to be proposed. Table XXVI lists the quotations received from the 10 companies.

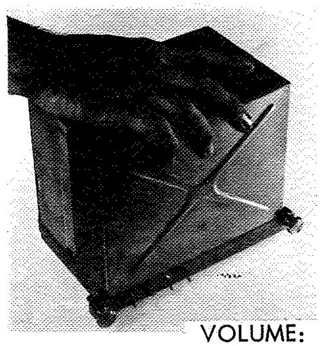
TABLE XXVI

COMPUTER PRICE QUOTATIONS

Company	Computer (Model No.)	Unit Price for Quantities Shown (Thousands of Dollars)				
		100	500	1000	1500	5000
AC Electronics	Magic 311	37	34.2	30	28	26.5
Autonetics	D26J	52	46.7	41	39	35
Control Data	5360	30	25	20	19	18
General Electric	M-355	--	45	43	42	--
Hughes	HCM-205	40	35	30	25	20
IBM (16K - 8-bit words)	4 -TC	27	24	21	20.5	19.5
Litton	LC-728	38.8	37	34.3	33	30.5
Nortronics	NDC-1060	38.8	36.2	34.5	33.9	33.3
Teledyne	CCC	33.1	23.2	19.5	17.6	13.3
Univac	1818	25	15	15	15	14
Average Price		35.7	32.1	28.8	27.3	23.3

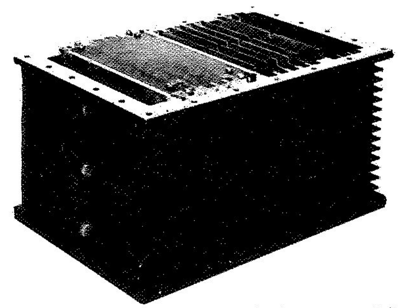
4.4.4.3 Proposed Companies

Table XXVI provides a quick overview of 10 computers that are capable of satisfying the computational subsystem requirements for the SST user. Pars. 4.4.4.2.1 through 4.4.4.2.10 provide a summary description of the characteristics of each of the 10 computers. Figure 76 compares the physical characteristics of nine of these computers.



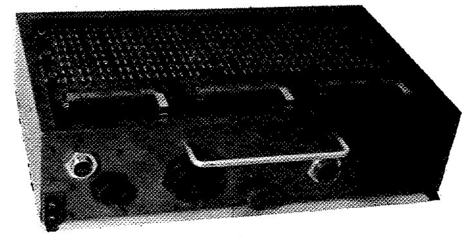
HUGHES
HCM-305

VOLUME: 0.2 CU FT
WEIGHT: 13.3 LB
POWER: 100 W



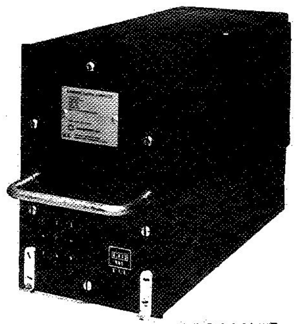
AUTONETICS
D26J

VOLUME: 0.21 CU FT
WEIGHT: 20 LB
POWER: 62 W



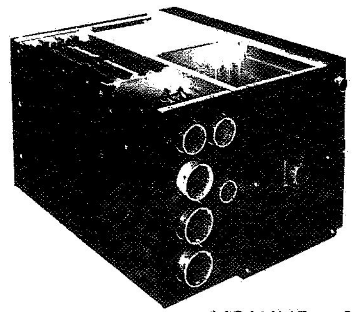
IBM
4π-TC

VOLUME: 0.4 CU FT
WEIGHT: 17.7 LB
POWER: 65 W



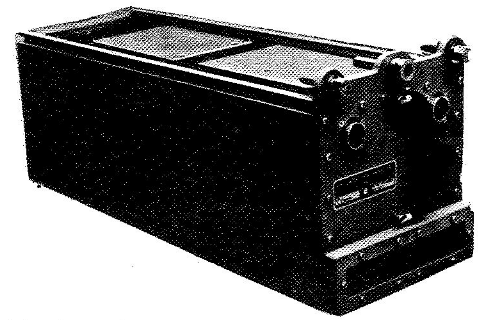
AC ELECTRONICS
MAGIC 311

VOLUME: 0.4 CU FT
WEIGHT: 29.7 LB
POWER: 169 W



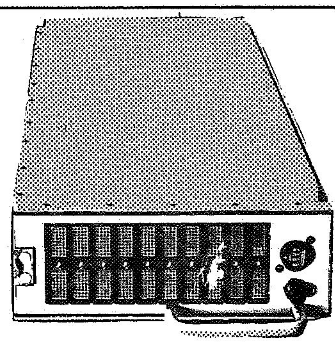
LITTON
LC-728

VOLUME: 0.55 CU FT
WEIGHT: 29.4 LB
POWER: 230 W



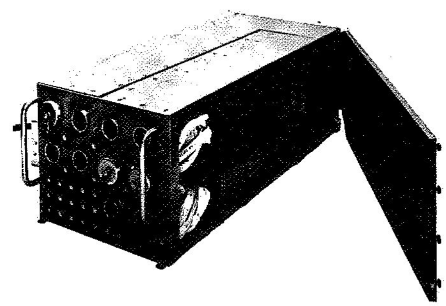
CONTROL DATA
CORPORATION
CDC-5360

VOLUME: 0.6 CU FT
WEIGHT: 30 LB
POWER: 105 W



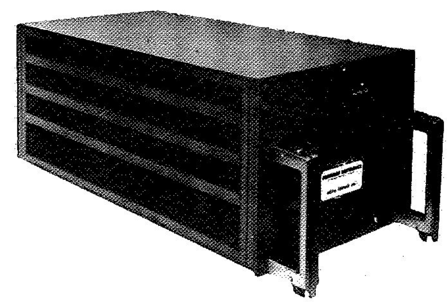
TELEDYNE
CCC

VOLUME: 0.8 CU FT
WEIGHT: 41.5 LB
POWER: 400 W



UNIVAC
1818

VOLUME: 0.89 CU FT
WEIGHT: 43 LB
POWER: 130 W



NORTRONICS
NDC-1060

VOLUME: 0.9 CU FT
WEIGHT: 38 LB
POWER: 180 W

Figure 76. Physical Characteristics of Candidate NAVSTAR Computers

4.4.4.3.1 AC Electronics Magic 311

General. The Magic 311 is a member of the AC Electronics Magic III series of general-purpose digital computers. It is a single address machine with 24-bit data words and 12-bit instruction words. Negative numbers are represented in 2's complement form. The Magic 311 is a serial computer with an instruction repertoire of 18 basic instructions. Add/subtract takes 19.5 μsec, multiply takes 32.5 μsec, and divide requires 33.2 μsec. The computer does not have index registers but there is a bias register which can be used for relative addressing.

Memory. The memory for the Magic 311 is a random-access, coincident-current, DRO, ferrite-core memory with 6144 12-bit words. The memory is designed to allow direct interchangeability of magnetic memory modules with a capability of electrically alterable or fixed (wired-in) program storage. The memory is designed to operate over the range -55 to 100°C.

Input/Output. The input/output unit provides the basic communications between the central processor and the associated subsystems. A direct channel to the memory has been provided for the processing of the input/output data. This input/output memory channel operates on a noninterfering basis with the normal operational program. The maximum cycle time is under program control and will be 600 msec for most applications. The input/output processes digital input data as required under the control of priority logic. Digital output rates are under program control but are synchronized through the input/output channel.

The digital input/output channel contains buffer registers and associated logic necessary to provide both serial binary and serial binary-coded decimal interface.

Three digital data channels transmit digital data to other subsystems. Channel 1 transmits binary-coded decimal data, channel 2 transmits binary data, and channel 3 transmits binary-coded decimal data and control data. A transmitted word consists of 24 data bits and 8 label bits. Separate line drivers are provided for clock, data, and synchronization for each channel. A common data and address register is time-shared for all three channels.

Three digital data input channels are provided to accept data from other sources. Two input registers are available to accept digital data concurrently. Access to the register data is under program control. A received word will consist of 24 data bits and 8 label bits.

Software. The following software and programming aids are available for the Magic 311 computer:

1) Assembler

2) Load program

3) Simulator

(These programs are executed on an IBM 7090 or IBM 704 in the FORTRAN IV and IBMAP languages.)

4) Diagnostics

5) Subroutine library.

Physical Characteristics. The computer is housed in a standard, short, one-half ATR case per ARINC 404 specifications and weighs 29.64 lb. It is composed of replaceable plug-in circuit card assemblies and modules. Heat is transferred by conduction from the electronic circuits to the module structure and then to the other cold wall of the heat exchanger. A blower forces air through the heat exchanger to remove the heat from the modules without passing over the electronic assemblies or connectors.

4.4.4.3.2 Autonetics D26J

The D26J is a microminiaturized, general-purpose, binary digital computer. It is a single-address machine with both data and instruction words 24 bits in length including sign. Negative numbers are represented in 2's complement form.

The D26J is a parallel processor with an instruction repertoire of 46 basic instructions including double-precision add/subtract. Short operations are 7.2 μsec, multiply is 15.3 μsec, and divide is 30.6 μsec. Double-precision add/subtract is 10.8 μsec. The computer has eight index registers, indirect addressing, and automatic power control to prevent memory loss during power transients.

Memory. The D26J memory consists of from 4,076 to 32,768 word memory modules of coincident-current DRO core. The word length is 24 bits and the cycle time is 3.6 μsec. A temperature-compensated current source is used to ensure proper memory readout signal over a wide operating temperature range.

Input/Output. The D26J input/output section is of modular design to provide the capability for high-speed data transmission simultaneously and independently of the central processor. The standard input/output section consists of a parallel 24-bit input channel and a parallel 24-bit output channel, each capable of data transfer rates up to 50,000 words/sec.

Interrupt Feature. The D26J has 20 program interrupts with both external and internal control under fixed priority. These interrupts are grouped into three types: real-time clock, external, and internal (in the order of descending priority). All interrupts can be enabled or disabled by the central processor program.

Software. The following software and programming aids are available for the D26J computer:

1) Symbolic assembly program
2) Computer functional simulator
3) Relocatable loader
4) Boot strap loader
5) Functional test program

The symbolic assembler, simulator, and relocatable loader are programmed to operate on the IBM 7094 computer system.

Power Supply. The D26J power supply consists of a transformer rectifier set, battery switching electronics, a regenerating dc-to-dc converter, and a series voltage regulator. It performs the following functions:

1) Isolation of dc power and ground signals
2) Regulation of secondary voltage outputs

3) Prevention of RFI from being conducted back to the primary power source

4) Operation with input power from a +28-vdc source during power transients of the primary ac supply.

Packaging. The D26J computer is designed to slide into a rack and to mate with system connectors at the rear of the chassis. The computer requires forced-air cooling and is designed to meet MIL-E-5400 Class 2X and MIL-I-6181 environment. It has 16,384 memory words, the volume is 0.85 cu ft, and the weight is 50 lb. Interconnection of the electronic modules and the core memory stack is accomplished with a single MIB. The MIB is made up of several independent layers which contain conductive parts similar to a printed circuit board. The logic circuitry is mounted on multilayer laminated boards.

4.4.4.3.3 Control Data 5360

General. The control data 5360 is a microminiaturized, general-purpose, binary digital computer. It is a single-address machine with both data and instruction words 24 bits in length including sign. Negative numbers are represented in 2's complement form.

The 5360 is a parallel processor with 31 basic instructions. The short operations require 12 μsec, and the long operations 90 μsec. The computer has 28 index registers and automatic power control to prevent memory loss during power transients.

Memory. The memory for the 5360 is a coincident-current core memory with 24-bit words and random-access capability. It has a cycle time less than 6 μ sec and an access time less than 1.5 μ sec. The logic design of the computer is such that the memory system is functionally expandable in modules of 4096 words to 32,768 24-bit words.

Input/Output. The input/output section of the computer provides the data communication with the outside world. Its capabilities consist of the following:

1) One 24-bit parallel input channel

2) One 24-bit parallel output channel

3) Two 8-bit parallel peripheral input/output channels

4) Two serial input channels

5) One serial output channel.

The 24-bit parallel input channel can accommodate up to 12 selectable devices and the 24-bit parallel output channel can accommodate up to five selectable devices. Two 8-bit parallel channels can accommodate one input and one output device each. The serial channels accommodate one device each.

Interrupts. The 5360 has internal electronics for accepting eight external interrupts through discretes received at 8-bit inverters. Bit No. 1 is permanently wired in the computer to have the highest priority. Bit Nos. 2 through 8 are under program control. Bit No. 3 is available for an operator maintenance console.

Software. The following software and programming aids are available for the 5360:

1) MICAP assembly program (executed on CDC 1604)

2) Maintenance test program

3) Simulator (executed on CDC 1604 or 3600)

4) Subroutine library.

Packaging. The computer is designed to slide into a rack and mate with system connectors at the rear of the cabinet. Forced air at a rate of 30 cu ft/min enters the rear of the cabinet and exhausts at the front. The computer is 7-1/8 in. wide, 7 in. high, and 19-3/4 in. long with a core memory up to 8192 words. This unit weighs 30 lb. The 5360 is designed to operate satisfactorily under the environmental conditions of MIL-E-5400 Class 2X and MIL-I-6181.

4.4.4.3.4 General Electric M-355

General. The General Electric M-355 is a small, lightweight, militarized, general-purpose digital computer. The M-355 is a parallel, binary, fixed-point computer that utilizes a random-access coincident-current memory. The computer accommodates data of variable word length: 6-, 9-, 18-, or 36-bit negative numbers are in 2's complement form.

The M-355 provides 91 instructions, 18 bits in length with one single-address instruction per word. The add instruction requires 2 μsec, the 36-bit multiply requires 21μsec, and divide requires 22 μ sec. Three index registers and multilevel indirect addressing with indexing at all levels give an addressable memory capability of up to 32,768 18-bit words.

Memory. The M-355 memory is a random-access, coincident-current DRO core storage with a capacity of 16,384 36-bit words in modules of 4096 words. The cycle time is 1 or 2 μ sec.

Input/Output. The input/output is designed to facilitate real-time concurrent servicing of multiple data processing peripherals and non-standard external devices. Up to 16 channels can be provided to accommodate a total transfer rate of 1,000,000 words/sec (with 6, 9, 18, or 36 bits per word) independently of process or operation through the use of an input/output controller (IOC). All data transfers go directly to and from the M-355 memory independently on a "cycle stealing" basis. Each channel of the IOC is tailored to the specific needs of the external equipment, which is facilitated by the bus structure off the IOC.

Interrupt System. The M-355 has up to 128 separate input/output interrupts which are arranged in 8 groups or levels of 16 interrupts. Each interrupt has a unique core location assigned to it, which should contain the address of the appropriate service routing. The interrupts may be masked in groups which postpone their recognition until the mask is limited. In addition, all interrupts may be inhibited independently of the mask setting.

Software. The following items of software are available for the M-355:

1) Assembler (executes on any General Electric compatible/600 computer)

2) Simulator (executes on any General Electric compatible/600 computer)

3) Utility package

4) Library subroutines.

4.4.4.3.5 Hughes Aircraft

General. The Hughes HCM-205 is a small, lightweight, militarized, general-purpose digital computer. It is a single-address machine with both data and instruction words 18 bits in length including sign. Negative numbers are represented in 2's complement form.

Memory. The HCM-205 memory is variable from 4096 words to 16,384 words in 2048-word modules. The word length is 18 bits and the cycle time is 2 μ sec. The memory is a coincident-current DRO core and operates over the temperature range of -55 to +100°C. The memory is fully integrated, using monolithic and hybrid circuits, and it is fully protected against power transients.

Input/Output. The HCM-205 input/output is under computer program control and provides one 18-bit parallel input/output channel to an input/output controller. The input/output controller provides centralized control over all input/output functions. It is program-controlled but can be externally controlled as needed. Up to 18 levels of external priority interrupts are available. Available through the input/output controller are discrete input/output, serial input/output, 18-bit parallel input/output, and incremental input/output.

Software. The following software and programming aids are available for the HCM-205:

1) Assembler
2) Simulator
3) Utility programs
4) Subroutine library
5) Diagnostic programs.

Physical Design. The HCM-205 computer is designed to reduce weight and volume by interconnection minimization and a unique packaging method which employs three-dimensional interconnection of components in a common module frame, unit structure, and heat exchanger. The HCM-205 weighs 13.3 lb and requires 0.2 cu ft of volume with an 8192-word memory and power supply. Thermal design is simple and efficient. Heat is transmitted from the integrated circuit flatpack to the module frame and then directly to the cooling air. The airflow requirement is 0.7 lb/min at 80°F maximum inlet temperature. The HCM-205 will meet or exceed the MIL-E-5400 Class 2 specification.

4.4.4.3.6 IBM 4π-TC

General. The IBM 4π-TC is a general-purpose, stored-program, binary digital computer with a single address and instruction words of 8, 16, or 24 bits and data words of 16 or 32 bits. Negative numbers are represented in 2's complement form.

The 4π-TC uses an 8-bit byte parallel data transfer operation and multifunction register. The computer uses an instruction set made up of 54 instructions. Execution times depend on the length of the instruction word (short, long, or immediate) but a long add or subtract (16-bit instruction, 16-bit operand) takes 18 μsec; a long multiply or divide, 54μsec. The 4π-TC has no index registers but does provide automatic power sequencial.

Memory. The 4π-TC has a basic 8,192 8-bit byte core storage which is expandable to 65,536 8-bit bytes. Main storage has a 2.5-μsec read/write cycle time. The memory uses a coincident-current (3-D) selection scheme. Operation is possible over the ambient temperature range of -55 to 100°C.

Input/Output. The input/output selection of the computer performs the following functions: data transfers, device address generation, data formatting, real-time clock generation, field-operating-unit hardware control, and interrupt control. This section contains the following:

1) One input/output channel, 16-bit parallel, program-controlled
2) One input/output channel, serial, program-controlled
3) Thirteen control lines (6 lines decoded, 5 lines (32 addresses) not decoded, 2 read/write lines
4) Three external interrupts (1 level)
5) Six discrete outputs, (latched, test, or operational)

6) Seven discrete inputs (levels sampled, tests, or operational)

7) Three timing signal outputs.

Interrupt System. The interrupt system used in the computer permits the operating state to change in response to conditions external to the system. There are three external interrupt levels designed into the computer. The interrupt operation is single priority and does not allow an interrupt of an interrupt, which can be handled under program control.

Software. The following software and programming aids are available for the 4π-TC computer:

1) Assembler program

2) Service programs

3) Dynamic program checkout system.

Packaging. The computer design was based on the requirements for a small, low-power, extremely rugged unit. The computer is 10 in. deep, 16.5 in. wide, and 4.0 in. high with a volume of 0.38 cu ft. The computer is mounted on an isolation rack to meet the shock and vibration requirements of MIL-E-5400H Class 2. It weighs 17.7 lb.

4.4.4.3.7 Litton LC-728

General. The Litton LC-728 is a low-cost, high-performance, binary, general-purpose digital computer. Its design is based on fitting the machine to the requirements. Three areas of the LC-728 design make use of the modularity concept: memory, input/output, and arithmetic unit.

The LC-728 is a two-instruction, two-address-per-word computer, with a 28-bit word length. Negative numbers are handled in 2's complement form. Arithmetic and logical operations are generally performed in parallel on 4-bit bytes. The bytes are sequenced serially at a 2-MHz rate.

Memory. The LC-728 memory system consists of from one to eight modules, each containing 4096 words of memory, and one set of memory interface logic, which consists of a 28-bit buffer register, a memory address register, and the timing and control systems.

Input/Output. The LC-728 input/output system provides a digital interface for use with external equipment. Data transfer paths include a basic 28-bit serial/parallel register and memory interleave. The serial/parallel input/output channel is set up by the digital computer under program control and then communicates with an external device under its control.

Interrupt System. Program interrupt is handled through a single interrupt request line, which is available to the interface and transfers program control to any place in memory specified by an address generated in the interface.

Software. The following items of software are available with the LC-728:

1) Assembler
2) Simulator
3) Program editor
4) Fortran IV complier
5) Diagnostics
6) Subroutine library.

Packaging. The LC-728 computer is a microelectronic unit, using a combination of monolithic integrated circuits and flatpack hybrid microelectronic circuits. Transistor-transistor logic (TTL) integrated circuits are used for all logic elements. The flatpack microelectronic circuits are used for high power and nonrepetitive circuits in memory.

4.4.4.3.8 Nortronics NDC-1060

General. The Nortronics NDC-1060 is a microminiaturized, general-purpose, binary digital computer. It is a single-address machine with both instructions and data words 24 bits in length including sign. Negative numbers are represented in 2's complement form.

The NDC-1060 is a parallel processor with an instruction repertoire of 42 basic instructions, which operate on whole words or half-words. Short operations are 8 μsec for 28 bits, multiply is 74 μsec. Instructions may be modified for indexing, indirect addressing, roll table relative addressing, or any combination of these. There is unlimited subroutine nesting capability with return address for each level automatically stored in the roll table. There are seven index registers available at each subroutine nesting level.

Memory. The NDC-1060 memory consists of random-access DCO core storage with a capacity of 16, 384 28-bit words in modules of 4096 words. The cycle time is 2 μsec with parallel readout of 14 bits at a time.

Input/Output. The input/output concept employed by the NDC-1060 provides flexibility for adaptation to a variety of applications. All input/output communication is routed through the input/output section. Both internally and externally controlled input/output operations are provided. Internally controlled operations are executed in accordance with the stored program and externally controlled operations are executed as the direct or indirect result of an interrupt signal.

Interrupt Feature. The basic control mechanism available to external devices is the interrupt. In the NDC-1060, 32 memory locations are reserved for interrupts. The input/output supplies an address associated with each interrupt. The computer can inhibit all interrupts by command.

Software. The following items of software are available for the NDC-1060:

1) Computer diagnostic program
2) Symbolic assembler (SASS) for IBM 360/65
3) Computer simulator for IBM 360/65
4) Utility arithmetic routines
5) Program loading routines.

Packaging. The NDC-1060 computer is housed within the envelope of one ATR case. There are four individual plug-in modules: logic assembly, memory assembly, input/output assembly, and power supply assembly. Low weight is achieved through maximum use of thick-film hybrid circuits and integrated circuits by combining computer and buffering functions in one case, and by using a minimum of structure consistent with connective cooling. The volume is 1510 cu in. and with an 8K memory the NDC-1060 weighs 38 lb. The computer was designed to meet the MIL-E-5400 (G), Class 1 specification.

4.4.4.3.9 Teledyne Computer Central Complex

General. The Teledyne computer central complex is a system of digital computing modules designed to perform the computations and decision-making functions required in advanced guidance and control applications.

The computer central complex consists of two types of computing devices in addition to the necessary input/output channels. One computing device, the STU, utilizes whole number computational techniques, while the second device, the central processing unit (CPU), uses incremental or digital differential analyzer (DDA) computing techniques. Prime requirements of the computer central complex are 1) ultra-high reliability and 2) functional modularity, wherein the failure of one unit does not affect the operation of the other units. The first requirement culminates in the triple redundancy of the computation units and the second requirement manifests itself in the modularity of the program memories and the CPU's.

The STU computational unit is a general-purpose, whole-number type computer composed of three major sections:

1) Read only program modules for storage of instructions and constants, and a modifiable memory module used for storage of variables

2) Arithmetic and control modules which perform the arithmetic and control functions

3) Input/output control logic which performs the gating and transmission of data.

The CPU computational units perform the arithmetic calculations using incremental techniques. Each CPU consists of up to 36 modules called general-purpose computing modules which have the capability to perform a computational function.

The STU. The STU is a binary, whole-number, general-purpose digital computer with a command list of 29 instructions. It is a single-address machine with both instructions and data words 20 bits in length including sign. Negative numbers are represented in 2's complement form.

The STU is a parallel processor with a basic clock rate of 750 kHz. Operation times are 10-2/3, 12, 49 (average), and 62-2/3 μsec for transfer, add/subtract, multiply, and divide, respectively. The STU has three index registers.

The STU Memory. The STU Memory consists of a group of modules, each module containing 512 20-bit words. Memory modules are either electrically alterable or permanently wired. Up to 8,192 words may be incorporated into the STU. Any combination of modifiable and permanent modules may be used. The modifiable memory is a random-access core memory operating in a parallel readout mode. The permanent memory is a core rope in which the cores are wired in accordance with the desired contents.

Interrupt System. The STU has the capability to be interrupted automatically under external control. There are five interrupts: power-on (initialization); power dropout; input of stationkeeping data; CPU derived interrupt; and STU malfunction.

The CPU. The computer central complex has three identical CPU's each containing a maximum of 36 general-purpose computing modules. The three CPU's perform identical calculations and the results are voted upon. Each general-purpose computing module is made up of a combination of DDA elements and majority logic elements which perform the computations and the voting. The number system is the 2's complement system. For the most part ternary logic is utilized; that is, incremental quantities can be either H, O, or -1. All elements are processed simultaneously during a single 24-bit time frame (32 μsec) and thus the CPU is called a parallel DDA.

General-Purpose Computing Module. The general-purpose computing module consists of a collection of building blocks which are used to construct DDA components (such as digital integrators using either trapezoidal or rectangular integration and servos) to vote, to isolate faults to a general-purpose computing module, and to accept inputs from external devices.

The Digital Interface Unit. The digital interface unit contains the elements of communication between the computer central complex and the outside world. The four components which take part in the communication are: transmitter module remote and receiver module local, transmitter module local, and receiver module remote. All information transferred between the transmitter modules and the receiver modules is transmitted serially. Either the STU or CPU may transmit data as needed to or from the digital interference unit.

4.4.4.3.10 Univac 1818

General. The Univac 1818 Avionics computer is a versatile, small, light weight and highly reliable general-purpose computer. Its versatility is based on its modular design. Various memory and input/output modules can be combined with the central processor to provide a wide range of configurations to meet specific requirements. The 1818 is a single-address machine with instruction and data words 18 bits in length. Negative numbers are represented in 2's complement form. The 1818 is a parallel processor with a basic repertoire of 62 instructions and it has three index registers. The add/subtract instructions take 4 μsec, multiply/divide 22 μsec.

Memory. The memory of the 1818 can consist entirely of DRO coincident-current core storage or it can be composed of various combinations of core memory and NDRO core-rope storage. The basic computer contains a DRO core memory comprising 4096 18-bit words. Modular expansion may be made to 32,768 words in 4096-word increments; parity is available as an option.

Nondestructive readout (NDRO) core-rope memory is available as an option and is implemented in 1024 18-bit word modules.

Input/Output. Transmission of data into or out of the 1818 is primarily via parallel, externally controlled channels or program-controlled channels. The input and output section provides for external store-read, timing, multiplexing, and control functions to interface the processor and memory sections with the peripheral equipment. Parallel data transfer may be controlled externally or internally by the externally and program-controlled channels. The 1818 can handle up to 16 program-controlled channels in addition to the externally controlled channels. Serial input and output is available as an option.

Interrupt System. The 1818 contains the necessary circuitry to honor nine interrupts. In case of simultaneous interrupts, the highest priority interrupt will be honored first. The nine interrupts are listed in order of descending priority:

1) Power interrupt
2) Fault interrupt
3) Real-time clock interrupt
4) Six external interrupts.

A request by any interrupt that is locked out due to the processing of a higher priority interrupt will be stored until such time that it can be honored.

Software. The available software for the 1818 consists of the following:

1) Assembler
2) Emulator
3) Utility programs
4) Subroutine library
5) Diagnostic maintenance programs.

Packaging. The 1818 weighs 43.0 lb and has a volume of 89 cu ft. It is designed in accordance with MIL-E-5400J to meet all the requirements of electrical (MIL-STD-704A), environmental, and mechanical (MIL-T-5422E) qualifying tests. The computer utilizes internal conduction cooling with the heat transferred to integral forced-air heat exchangers.

The primary circuit elements are monolithic integrated circuits packaged in 14-lead flatpacks. The memory circuit modules include both discrete components and integrated circuit flatpacks.

4.4.5 ELECTRONIC CALCULATOR/DESK-TOP COMPUTER SURVEY

The small marine-craft user needs either very precise or very frequent computations. Sec. 3 of vol. II describes the MINSCO technique which requires only a set of simple arithmetic computations to determine user position accurately when sufficient data were available from the satellite and other sources. Because this type of user would use the NAVSTAR system no more than once per hour, and because the necessary calculations require at the most a small calculator, the small marine craft user can do these calculations by hand.

4.4.5.1 Status of Available Equipment

Table XXVII presents data on a number of desk-top computers and electronic calculators available from industry. This guide was developed by William I. Hillenbrand for an article appearing in Electronic Products, entitled "Desk-Top Computers/Electronic Calculators for Engineers."

As can be noted, these equipments range in cost from less than $1000 to over $10,000. The user can select the machine best suited to his needs. The equipment described in the table operates on electronic principles, and is therefore generally more reliable, quieter, and more rapid than equipment based on mechanical techniques.

The automatic calculator includes some form of storage, enabling it to perform a predetermined series of operations on command. This enables the user to enter only the variables each time, reducing the probability of errors due to missing a step in the computation. Examples of the automatic calculator are given in Figure 77. For the more sophisticated user, the desk-top computer adds both register and program storage along with some decision-making ability.

TABLE XXVII.

SUMMARY OF DESK-TOP COMPUTERS

Manufacturer or Distributor	Model	Keyboard Type	Digits of Entry (listing columns)	Digits of Total (totaling columns)	Input (type)	Output (type)	Square Root	Log Keys (exponential operations)	Storage Registers	Program Memory	Decimal Points	Options	Price and Availability
Canon, U.S.A. Inc.	130	10 key	13	13	keyboard	special bulb-type display	–	–	–	1	floating	–	$1,195 1 wk
	161	10 key	16	16	keyboard	special bulb-type display	–	–	–	1	floating	–	$1,475 60 dyas
Data Acquisition Corp.	512	10 key	100	100	keyboard (supp. access.)	NIXIE-tube display	yes	via programming	120	512 steps	floating	tape unit, printer	$9,500 3 mo
Dero Research and Development Corp.	Sage 1	10 key	10	20	keyboard	special bulb-type display	by approx.	–	2	–	–	–	$995 June '66
Friden, Inc.	EC-132	11 key	13	13	keyboard	C-R tube display	yes	–	3	–	yes	entry counter	$1,950 45 days
	EC-130	11 key	13	13	keyboard	C-R tube display	–	–	3	–	yes	–	$1,695 30 days
IME/U.S.A., Inc.	84M	10 key	16	16	keyboard	NIXIE-tube display	–	–	3	–	floating	–	$995 30 days
	84	10 key	16	16	keyboard	NIXIE-tube display	–	–	4	optional (external)	floating	–	$1,295 30 days
	84K	10 key	16	16	keyboard	NIXIE-tube display	optional	–	4	optional (external)	floating	satellite keyboards (nonsimul.)	$1,695 60 days
Inter-Continental Trading Corp., Anita Div.	Anita Mark VIII	full keyboard	10	12	keyboard	NIXIE-tube display	yes	–	optional	–	auto-matic	extra register storage	$890 stock
	Anita Mark IX	full keyboard	10	12	keyboard	NIXIE-tube display	yes	–	–	–	auto-matic	–	$1,380 stock
Mathatronics, Inc.	424	10 key (plus algebraic control)	9 (plus exponent)	9 (plus exponent)	keyboard	serial strip printer	yes	optional	4	24 steps	floating	expandable to any model listed	$3,490 45 days
	848, 848-1, 848-2, -3, -4	10 key (plus algebraic control)	9 (plus exponent)	9 (plus exponent)	keyboard	serial strip printer	yes	optional	8	48 steps Models 848-1, -2, -3 and -4	floating	expandable to any model listed	$3,490 to $7,740 45 days
	848 PTP, 848 PTP APS, 848 APS	10 key typewriter	9 (plus exponent	9 (plus exponent)	2 keyboards or paper tape [Model 848 APS keyboard]	page printer, serial strip printers, punched tape [Model 848 APS serial strip printer]	yes	optional	48	48 steps intnl. (848 PTP); 480 steps intnl. (848 PTP APS); 480 steps (848 APS)	floating	expandable to any model listed	$7,740 to $11,400 90 to 120 days
Monroe International, Inc.	EPIC 2000	10 key	16	16	keyboard	printed paper tape	yes	via programming	5	14 steps	yes	–	$2,250
	EPIC 3000	10 key	16	16	keyboard	printed paper tape	yes	via programming	5	42 steps	yes	–	$2,750
Olivetti Underwood Corp.	Programma 101	10 key	22	23	keyboard and magnetic card	printed paper tape	yes	written programs available	10	120 steps	auto-matic	–	$3,200 4 to 6 mo
SCM Corp.– Calculator Div.	Cogita 240-SR	10 key	12	24	keyboard	C-R tube display	yes	–	3	–	floating	–	$2,195 30 to 90 days
Sharp Electronics Corp.	CS-20A	10 key	14	14	keyboard	NIXIE-tube display	–	–	–	–	auto-matic	–	$1,145 30 days
Victor Comptometer Corp. (Bus. Ma. Gp.)	3900	10 key	20	20	keyboard	C-R tube display	yes	–	–	5	floating	–	$1,825 6 mo
Wang Laboratories, Inc.	300 (business)	10 key	10	10	keyboard	NIXIE-tube display	–	–	3	–	floating	satellite keyboards non-simultaneous & simultaneous operation	$1,690 to $4,280 8 to 10 wk
	310 (statistical)	10 key	10	10	keyboard	NIXIE-tube display	yes	–	3	–	floating	"	$1,895 to $4,710 8 to 10 wk
	320 (scientific)	10 key	10	10	keyboard	NIXIE-tube display	yes	yes	3	–	floating	"	$2,095 to $5,130 8 to 10 wk
	LOCI 2	10 key	10	10	keyboard, card reader, Teletype 33 ASR, tape reader, on-line input	NIXIE-tube display, column printers punched tape, Teletype 33 ASR output writer, BCD on-line output	–	–	2,4 or 16 plus 3 working registers	prescored tab card and/or punched tape	floating	2 readers for 160 steps; on-line operation; tape input parallel-ing readers	$4,750 to $8,950 8 to 10 wk
Wyle Laboratories	WSS/1	10 key	24	24	keyboard and/or card program	C-R tube display	yes	via programming	3	program cards (unlimited)	auto-matic	–	$4,950 2 to 4 wk
	WSS/5	10 key	24	24	"	C-R tube display	yes	via programming	11	program cards (unlimited)	auto-matic	–	$7,900 3 to 4 wk
	WSS/10	10 key	24	24	"	C-R tube display	yes	single key or via programming	11 to 27	512 steps internal	auto-matic	–	$9,850 3 to 4 wk

FOLDOUT FRAME 1

FOLDOUT FRAME 2

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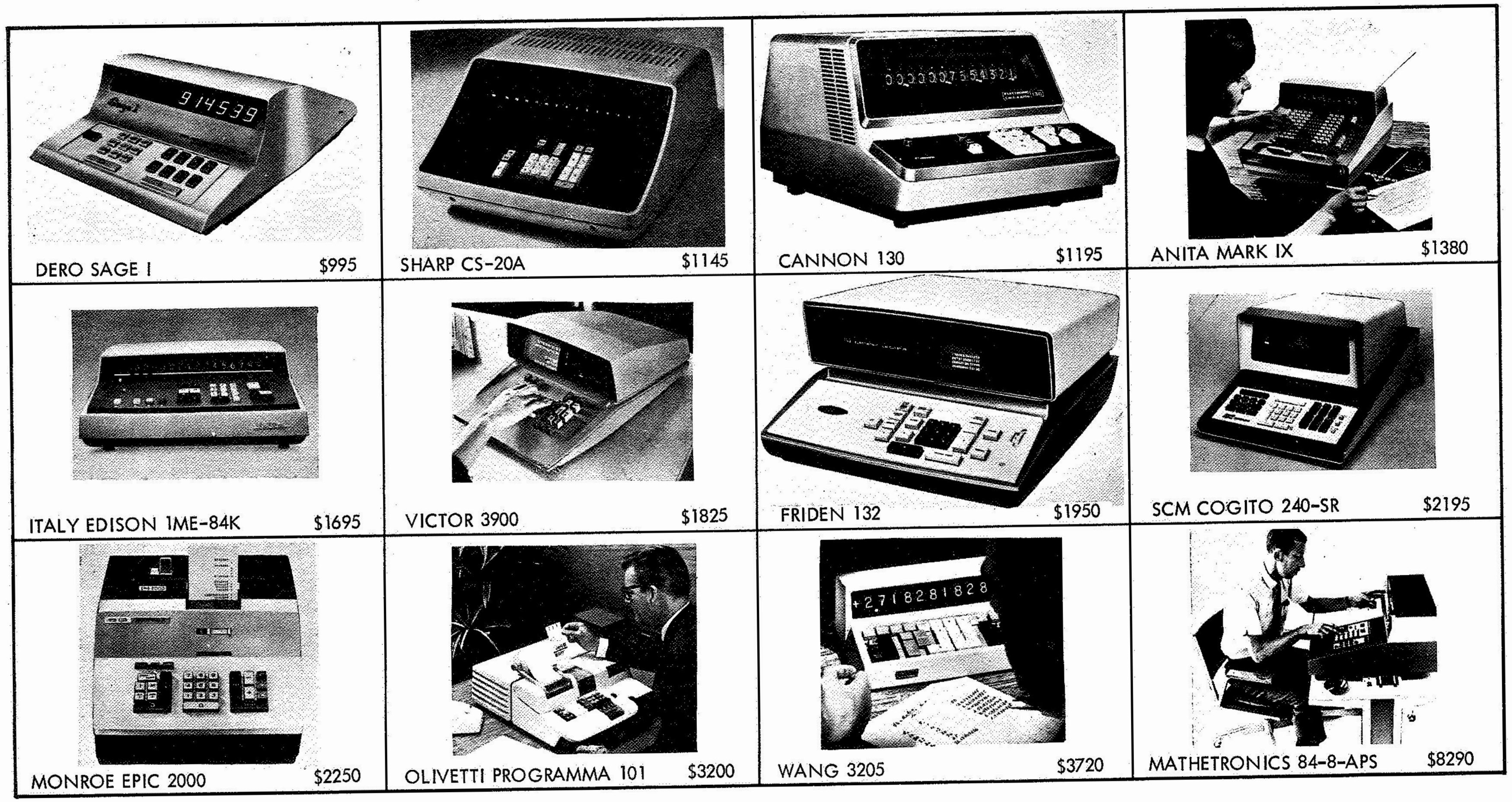

Figure 77. Comparison of Electric Calculators/Desk Top Computers

4.4.6 NEW COMPUTER TECHNOLOGY DESIGN CONSIDERATIONS

4.4.6.1 General

The new computer technology design considerations given above are primarily concerned with the organization or architecture of the computer. They represent ways of analyzing the technologies in memory and components which will be available in the time frame of interest and finding optimum ways of configuring the computer to minimize production costs.

The NAVSTAR computer can be generally characterized by a modest memory size (probably 4K to 8K memory capacity), low speed, moderate accuracy (21 bits), minimal digital input-output interface and relatively nonstringent environmental requirements. A typical aerospace computer satisfying this general description might have the following cost breakdown:

Memory	50 percent
Input-output	30 percent
Arithmetic and control	10 percent
Power supply, clock, and miscellaneous	10 percent

4.4.6.2 Methods of Reducing Memory Cost

It is, therefore, apparent that minimizing the cost of the NAVSTAR computer subsystem entails making the memory cost as low as possible even at the expense of other computer parts. At the present time, semiconductor logic is becoming less expensive at a rate faster than memories. This trend may be reversed in a few years with the advent of new memory types, such as plated-wire and semiconductor memories.

Two ways of reducing the memory cost are to 1) Reduce the size of the memory (this reduction is accomplished by making the arithmetic and control section more complex and more versatile and in giving more control to the input-output section) and 2) use several types of memories together to form the total memory, each type being the cheapest for a particular storage requirement. To apply these concepts, tradeoff studies will be made on the basis of more detailed analysis of projected computer requirements.

In reducing the number of bits in memory, consideration should be given to the percentage of memory for instructions versus the percentage of memory for data. If the percentage for instructions is high, as in most computers, then savings will be made by tailoring the bit length of the word to the instruction format rather than to the data accuracy. To achieve the correct data accuracy, double-precision instructions can be used. If the instruction word length is longer than the data accuracy, then these additional bits in the data word can be economically wasted. The cost of double precision is additional logic complexity and computational speed.

In single-address computers, a great deal of memory is inefficiently used if the full-address field is specified in the instruction. Using a restricted-address field and bank registers in the arithmetic and control section to augment the address may result in savings. For instance, in a 24-bit single-address instruction computer, 13 bits are required to address an 8K memory. Thirteen bits out of the 24-bit instruction represents over half the bits in the instruction; and if the memory contains 80-percent instructions, nearly half the memory is used for addressing. An 8-bit address with a bank register would save a considerable number of bits in memory. The cost of banking is additional logic complexity and also an increased number of instructions, since some instructions are required to load or modify the bank register. It also costs computational speed since adding the bank register to the restricted address field to obtain the actual address requires time. Index registers might cut down the number of instructions. However, indexing makes the instruction word longer and increases the memory size. The compromise must be based on the nature of the program to be run in the computer. A multiplicity of arithmetic registers, such as dual accumulators, might reduce the number of instructions required in the program. Again this versatility increases the number of bits required in the instructions so that a tradeoff is necessitated.

There are various types of information stored in memory, each with unique memory requirements. The program can be stored in a fixed memory if sufficient versatility is incorporated in the arithmetic and control section. Temporary working storage can be provided in volatile storage. In some systems, there are data words, such as calibration constants or position information, which must be retained when the computer is turned off and must therefore have a nonvolatile, alterable store. A magnetic, alterable memory with appropriate control for power-supply shutdown satisfies all of these requirements; however, the magnetic memory may not be the cheapest memory. Consideration should be given to fixed memories, such as diode arrays, for the program storage. Semiconductor scratch pad memories might be useful for temporary working storage. If required, small magnetic alterable memories might be used for data which must be nonvolatile. In the latter case, the data rate can be quite low and unique small memories, such as magnetic shift registers, can be considered. A multiplicity of memory types in a computer generally leads to an increase in the amount of memory electronics. Therefore, even though each memory type might be quite economical, a single type might lead to a minimal memory cost.

When a computer is used as an integral part of a system, part of the computer's ancillary hardware might be shared with the rest of the system to achieve a cost savings. For instance, power supplies, cooling, intraconnect, mechanical assembly, and chassis might be common in the system. The computer could very well be reduced to a few circuit boards or modules which plug into the rest of the system.

4.5 DISPLAY SUBSYSTEM

4.5.1 INTRODUCTION

The display subsystem, which provides the man-machine interface between the user and his NAVSTAR equipment, fulfills the system's primary mission of enabling the user to navigate his craft. The display subsystem is designed to display the information required for enhancing the user's decision-making processes, for understanding his craft's status, and for effective control. A number of display subsystems, designed for use with other navigation aids, provide the type of information needed to implement the system objectives. The extent to which these subsystems could be integrated into the NAVSTAR user system has been evaluated and suggestions made for either the new or improved display subsystems required to meet the user's needs.

4.5.1.1 User Configurations

The display subsystem mechanizations to be recommended for NAVSTAR will be based on the individual user's specific requirements. The scope of this study was limited to examining the needs of two classes of users: 1) The supersonic aircraft, and 2) the small marine craft. The selection of these configurations was based on the different computational subsystems proposed with the concomitant need for a different type of data input. Where a stored program digital computer is the recommended computational system, the type of display subsystem recommended for the supersonic aircraft will satisfy the user's requirements. Where a desk-top calculator is to be used, other forms of display subsystems are required.

4.5.1.2 Method of Attack

The design of the display subsystem was constrained by two factors: the specific objectives to be served by the NAVSTAR system, and the data processing capability the user possesses. The primary objective of NAVSTAR is to provide accurate navigation data to the user. The ultimate goal is to provide such information as present position, course, altitude, and velocity. The method to be implemented to achieve this goal would differ somewhat from user to user. In this study, the requirements of the supersonic transport aircraft and the small marine user were selected to demonstrate two extremely different approaches.

For the SST user, a survey was made of existing navigation displays to evaluate their suitability for use with NAVSTAR. A limited pilot survey was made from the viewpoint of the user relative to the priorities of data to be displayed under various circumstances.

The requirements of the small marine user needing a low-cost system and having a low computational capability were analyzed, and an attempt was made to provide rough guidelines.

4.5.2 SUMMARY

Consideration of current display practices on high-speed aircraft indicates that the most useful data for navigation purposes, in order of priority, are as follows:

1) User's position
2) Range and bearing of destination (course)
3) Time to go to destination
4) Estimated time of arrival.

Most pilots indicated a need for more accurate traffic control and sea-rescue data. In particular, they cited the need for an alarm method which would warn them of impending collisions or hazardous weather along their flight path.

The design requirements for navigation displays were analyzed. Included in this analysis were controls, display items, data-entry keyboards, and human factors. In general, several constraints on the display design were encountered:

1) Legibility and comprehensibility
2) Limitations on the amount of data to be displayed at any one time
3) The need for small size, low weight, and low-power requirements
4) Cost-effectiveness.

The survey of existing displays pointed up the accepted practice of displaying only two quantities at a time, such as latitude/longitude; velocity/heading; or time to go/estimated time of arrival. Other data which may be displayed include altitude, distance from nearest fix points, alarm warnings, traffic control information, position update data, weather alerts, and pertinent data from ground stations.

The proliferation of displays in today's aircraft poses a major problem to flight safety. Further study is recommended in integrated displays, more positive traffic control, sea-rescue displays, and the development of lower-cost displays through the new technology.

Two radically different display subsystems are required for the NAVSTAR users at both ends of the user spectrum. The SST user will have a navigation computer which may handle navigation with one or more systems (NAVSTAR, LORAN, etc.) Generally available with the computer is a control and display unit that can serve quite adequately for any or all systems. Therefore, no special display unit need be purchased if navigation by satellite is added to the older systems as an alternate method.

At the other extreme is the marine craft with severe equipment and cost limitations. A low-cost system will have to be designed for this type of user; a slide rule or desk-top calculator for NAVSTAR computations may be all that is available to this user. The display unit will, therefore, be tied into the receiver/preprocessor and will show basic quantities received (constants and variables associated with simplified calculations).

As technology progresses, it is envisioned that cathode-ray tube (CRT) displays or their solid-state equivalent will displace the separate indicators presently in use. Much more versatility will result, allowing a full set of alphanumeric characters and symbols to be displayed quickly and legibly. More quantities can be shown simultaneously upon request. In addition, analog-type displays are possible which will be very helpful in traffic control situations and rescue operations. Bright-tube displays with memory capabilities are now available to eliminate the old CRT problem of low brightness and flicker.

4.5.3 DESIGN CONSIDERATIONS

The most general objective of a display subsystem is to improve the decision-making faculty of the man in the system. For this reason, the data to be displayed must be presented in a legible and easily comprehensible form. Because of the constraints imposed by size, weight, and money, as well as the psychological limitations of the user's perception, tradeoffs must be made on the basis of the amount of information which should or could be displayed simultaneously and the method selected for controlling the quantities to be displayed.

In addition to the purely output function of displaying the results of system data processing, the total display subsystem must also provide the facility for data entry. Items such as course changes, wind velocities, etc., should be provided by the pilot to the system. Therefore, the design process must be concerned with output, input, and system control. System control includes display selection and computer control.

A number of factors, generally referred to as human factors considerations, must be specified for a display subsystem. The output, alphanumeric or symbolic, must be easily readable within the ambient light conditions of a craft cockpit or control area. All knobs and pushbuttons should be easy to operate, conveniently located, and clearly marked. Warning indicators should be clearly distinguishable and of the attention-getting type.

From a hardware point of view, the display subsystem should be reliable and should utilize the most efficient components available. Cost is an important criterion in the development of design specifications, particularly in the case of the small marine-craft user.

4.5.3.1 User Survey

The first step in the design of the NAVSTAR display subsystem was to perform a survey of operator needs and preferences. Several experienced navigators and pilots were interviewed, including representatives from the following organizations: United Airlines, Flying Tiger Lines, TAC, SAC, U.S. Coast Guard, and TRW Systems.

Table XXVIII gives the ranking of information for the various types of craft. While data are provided on the need for traffic control and sea-rescue operation information, the primary emphasis of the study was on navigation information. For navigation, the most important information was present position, followed by range and bearing to destination, time to go, and estimated time of arrival. For traffic control, the need for an alarm condition to warn of impending collision or hazardous weather conditions was most important; and for sea-rescue operations, a distress condition alert was most important.

TABLE XXVIII

SUMMARY OF SURVEY ON USER'S DATA DISPLAY REQUIREMENTS

Data to be Displayed	Rank	Commercial Aircraft (SST, 707, 747, etc.)	General Aviation (Private and Business)	Military		Ocean Vessels (Coast Guard Viewpoint)
				TAC Fighter-Bomber	SAC	
1. Navigation Data						
User's position — latitude and longitude	1*	1	1	1	1	1
User's destination — latitude and longitude	7		7		6	
Estimated time of arrival	4	4	3	4	5	
Time of day	6		6			3
Estimated time to reach destination	3	3	4	2	4	
Range and bearing of destination from user	2	2	2	3	3	
Time at which current fix was obtained	5	5	5	5	2	2
2. Traffic Control Data						
ALARM condition (approaching collision, hazardous weather pattern, etc.)	1	1	1	1		1
Steady or flashing warning signal	5	5			1	5
Description of alarm condition	3	3	3	2		2
Recommended corrective action (new course data, heading altitude)	2	4	2	3	2	3
Range, bearing, and altitude of nearest neighbor (s)	4	2		4	3	4
3. Sea-Rescue Operations						
Distress condition alert	1	1	1	1	1	1
Description of distress condition	3	3	2	3	4	3
New navigation data		5				4
Range bearing to rescue area	2	4		2	2	2
Estimated time to make contact and ETA	5	6		5	3	5
Alternate destinations (with modified flight plan data, ETA's, etc.)	4	2		4		

*Ranking in order of importance

4.5.3.1.1 Aircraft User Requirements (Configuration A — Automatic, Self-Contained)

While developing the display subsystem design for the aircraft user, it became apparent that the displays currently used with other navigation aids (such as inertial navigation systems) could be used with little or no modification for the NAVSTAR display subsystem. This study was not concerned with an in-depth investigation of programs leading to the development of integrated display systems, but considered the problem from the "Separate Subsystem" concept. Par. 4.5.3.2 describes the survey of off-the-shelf navigation display subsystems available in industry.

4.5.3.1.2 General Aviation Requirements (Configuration B — Automatic Ground-Aided Computation)

The cost of available navigation display systems is prohibitive for the general aviation user; hence, a separate study was made of his requirements for display. Figure 78 is a block diagram of a potentially low-cost display, which could be developed for the low-cost user who does not possess a stored-program digital computer as part of his NAVSTAR system but instead uses a cooperative ground station for required computations.

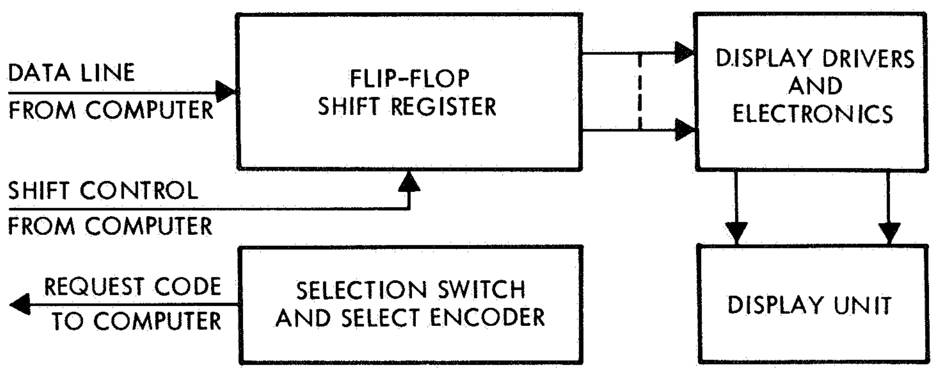

Figure 78. Low-Cost Display, Block Diagram

Figure 79 shows the simplified panel and control unit. Only one quantity would be stored in the display system in a low-cost flip-flop register. A request code would be sent to the computer denoting the quantity to be displayed. At this time, the computer would serially shift the new data into the register for display. This system could be implemented for the target cost of $250.00 in quantity production in the 1975 era.

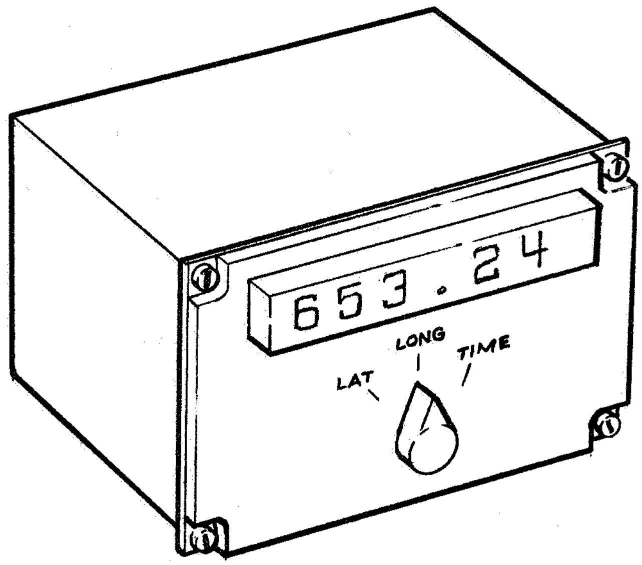

Figure 79. Panel — Low-Cost Display

4.5.3.1.3 Small Marine Craft Requirements (Configuration C — Manual Computation)

At the other end of the spectrum, the small marine-craft user does not need an elaborate display. The MINSCO equations (see sec. 3, vol. II) provide a set of simple calculations that can be performed on a desk calculator. In this case, however, certain data must be received and stored in the display unit to be used in the calculations. The data could be selected by the simple push of a button.

The system shown in Figure 80 is somewhat more complex than that proposed for the general aviation user, since about 20 values must be received and stored for pushbutton retrieval. The storage could be a low-cost sonic delay line. The operation of the display is based on a panel selection of a quantity (see Figure 81). The selection switch sets up the address code which in turn gates the desired information to the display. Entry of new data would be under control of the receiver/preprocessor equipment.

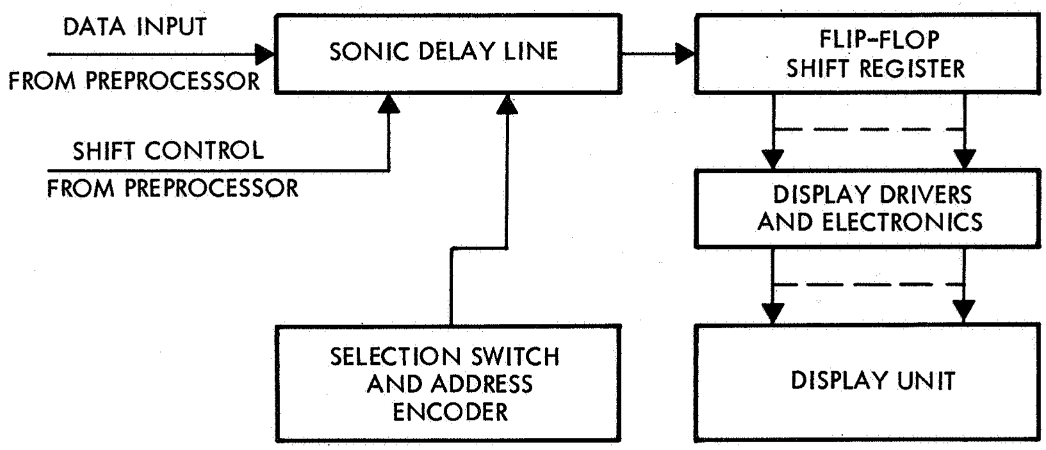

Figure 80. Small Marine-Craft Display, Block Diagram

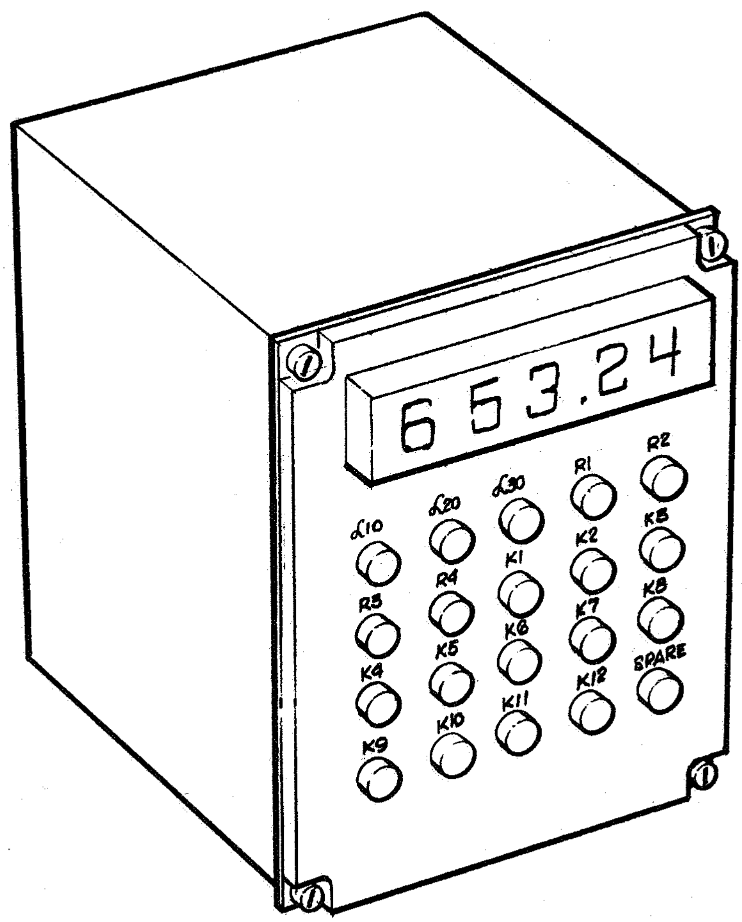

Figure 81. Small Marine-Craft Display, Panel

4.5.3.2 Survey of Navigation Displays

A number of manufacturers of navigation equipment were surveyed for this study. The following paragraphs describe the display subsystems submitted in answer to the request for information. The companies replying were Litton, AC Electronics, General Precision, and Nortronics.

4.5.3.2.1 Litton LTN-51 Control and Display Unit (CDU)

Figure 82 shows a block diagram of this system. Switches on the front panel control the selection of data to be displayed. These data may come from either the associated computer or the panel-mounted keyboard. The displays are formed of segmented illuminated bars (7 bars per number) with illumination provided by 5-v long-life incandescent lamps. The high-brightness characters are 0.32 in. high and 0.19 in. wide. Brightness may be varied with a 12-position switch, and each unit may be replaced from the front for easy maintenance.

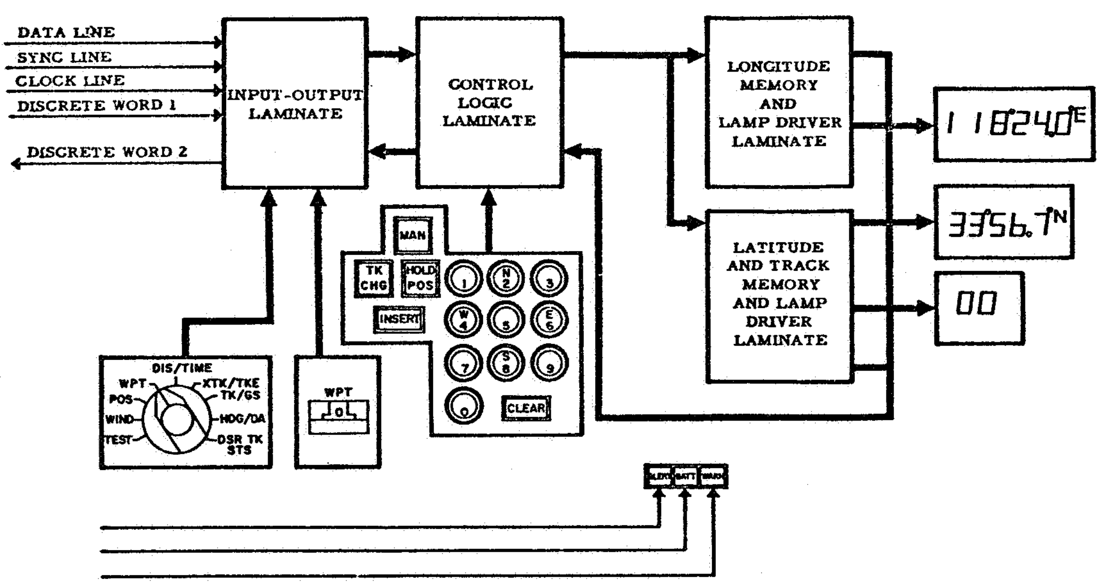

Figure 82. Litton LTN-51 Control/Display Block Diagram

The LTN-51 has its own power supply, requiring 28 vdc. The digital electronics are contained on several boards, which are generally plug-in. There are 15 pushbuttons: four for mode selection and the rest for the data-entry keyboard. The panel layout is shown in Figure 83. A description of the panel is given in Tables XXIX and XXX, and a photograph of the LTN-51 is shown as Figure 84.

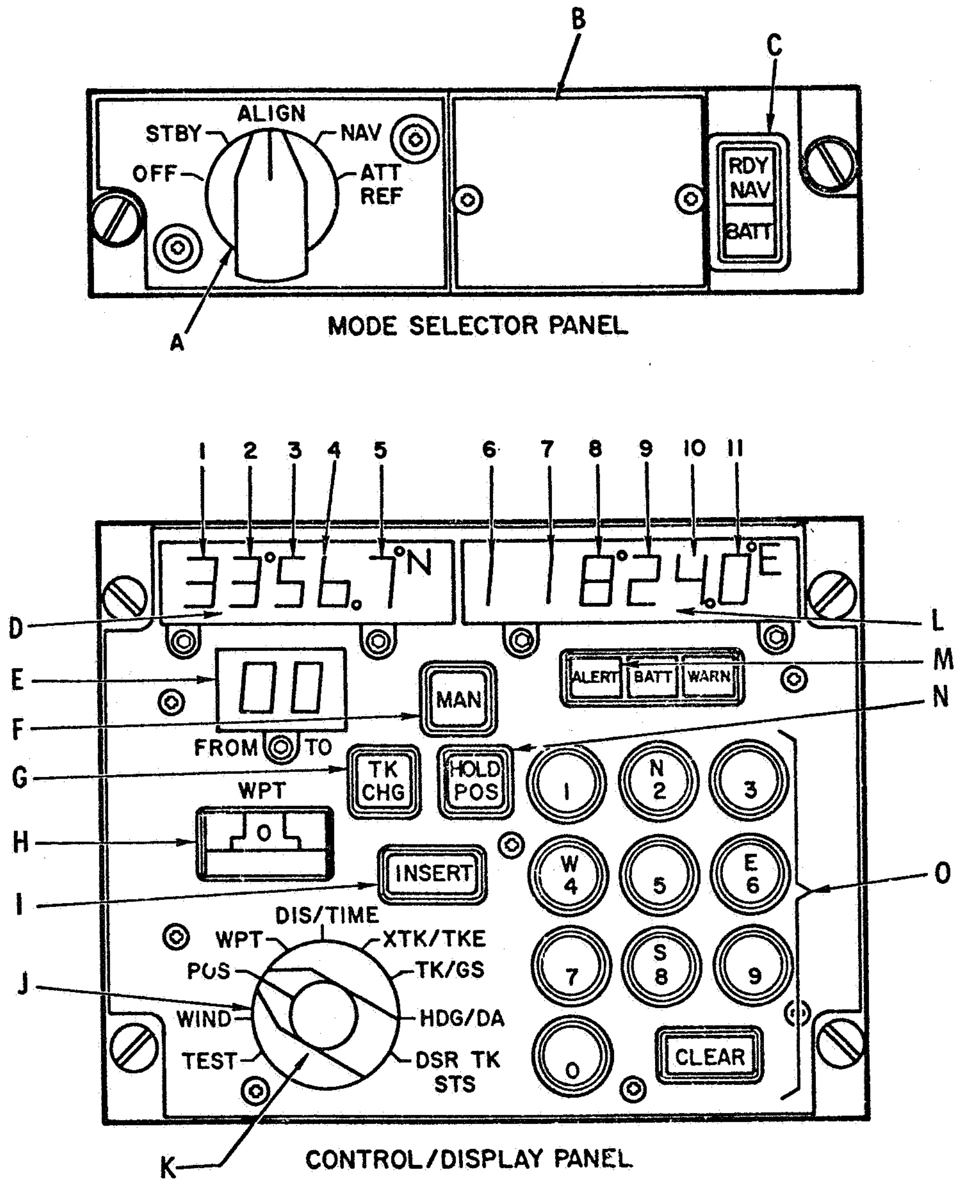

Figure 83. Litton LTN-51, Panel Layout

TABLE XXIX

LITTON LTN-51 NUMERICAL DISPLAY FUNCTIONS

Display Switch Position	System Mode	Function on Left Display	Function on Right Display
Test	STBY ALIGN NAV	Characters 1 through 5 read the number selected on the Waypoint Thumbwheel.	Characters 6 through 11 read the number selected on the Waypoint Thumbwheel.
WIND	NAV	Reads Wind Speed. Characters 1 and 2 are blank. Characters 3 through 5 read 0 to 399 knots in 1 knot increments.	Reads Wind Direction with respect to true north. Characters 6, 7, and 8 are blank. Characters 9, 10, and 11 read 0 to 359° in 1° increments.
POS	STD-BY ALIGN NAV	Reads aircraft present position Latitude. Characters 1 through 5 read 0° to 90°0' in 0.1' increments. In NAV, character 5 is blank unless "HOLD POS" pushbutton is depressed. Degree, decimal, minute and N or S legends are lit.	Reads aircraft present position Longitude. Characters 6 through 11 read 0° to 180°0' in 0.1' increments. In NAV, character 11 is blank unless the HOLD POS pushbutton is depressed. Degree, decimal, minute and E or W legends are lit.
WPT	STD-BY ALIGN NAV	Reads Latitude of stored waypoint corresponding to digit on "WPT" thumbwheel. Characters are as for "POS" above.	Reads Longitude of stored waypoint corresponding to digit on "WPT" thumbwheel. Characters are as for "POS" above.
DIS/TIME	NAV	Reads Distance-to-Go to the TO waypoint. Character 1 is blank. Characters 2 through 5 read 0 to 9999 nautical miles in 1.0 nautical mile increments.	Reads Time-to-Go to the TO waypoint at the present ground speed. Characters 6 and 7 are blank. Characters 8 through 11 read 0 to 999.9 minutes in 0.1 minute increments. The decimal character is lit.
XTK/TKE	NAV	Reads aircraft Cross Track Distance from great circle track established by the waypoints shown on the FROM-TO display. Character 1 reads L or R. Characters 2, 3, 4 and 5 read 0 to 999.9 nautical miles in 0.1 nautical mile increments. The decimal point is lit.	Reads difference between aircraft's actual Track Angle and Desired Track Angle. Character 6 reads R or L. Character 7 is blank. Characters 8 through 11 reads 0° to 180.0° in 0.1° increments. The decimal point is lit.
TK/GS	NAV	Reads Track Angle being made good with respect to true north. Character 1 is blank. Characters 2 through 5 read to 0 to 359.9° in 0.1° increments. The decimal digit is lit.	Reads aircraft Groundspeed. Characters 6 and 7 are blank. Characters 8 through 11 read 0 to 1999 NM/Hour in 1.0 NM/Hour increments.
HDG/DA	NAV	Reads aircraft Heading with respect to true north. Character 1 is blank. Characters 2 through 5 read 0 to 359.9° in 0.1° increments. The decimal digit is lit.	Reads the difference between Track Angle being made good and aircraft Heading. Characters 6 through 8 are blank. Characters 9 through 11 read 0 to 45.0° in 0.1° increments. The decimal digit is lit.
DSR/TK/STS	NAV ALIGN	In NAV, reads the Desired Track Angle with respect to true north for great circle navigation between the waypoints on the FROM-TO display. Character 1 is blank. Characters 2 through 5 read 0 to 359.9° in 0.1° increments. The decimal digit is lit.	In ALIGN, reads Alignment Status. Characters 6 through 10 are blank. Character 11 reads 0 to 9 in 1 increments.

TABLE XXX

LITTON LTN-51 PANEL ITEMS

Callout (Figure 81)	Item
A	Mode selector switch
B	Self test access panel
C	Mode selector annunciator lamps
D	Right numerical display
E	FROM-TO waypoint display
F	Manual track selection pushbutton
G	Manual track change pushbutton
H	Waypoint display thumbwheel
I	Data insert pushbutton
J	Display selector switch
K	Display dim switch
L	Left numerical display
M	Control display annunciator lamps
N	Position display hold pushbutton
O	Data entry keyboard

Figure 84. Litton LTN-51 Control and Display Unit

The LTN-51 system is currently in production for use on aircraft such as the 707 and DC8. Budgetary prices on the control and display units have been supplied as follows:

Quantity	Price Per Unit ($)
100	12,800
500	8,600
1000	7,700
1500	6,600
5000	5,000

4.5.3.2.2 AC Electronics Control and Display Unit for Magic 311 Computer

This unit is similar to the Litton unit and would serve the same purpose in a navigation system (see Figure 85). It was made to fit into a Boeing 747. Weight is 5-1/2 lb and volume is 140 cu in. The segmented numerical displays the data-entry keyboard, and other buttons and controls are basically the same as in the Litton LTN-51.

Prices (budgetary estimate) for the AC Electronics CDU are as follows:

Quantity	Price Per Unit ($)
100	6,000
1,000	5,000
11,000	4,000

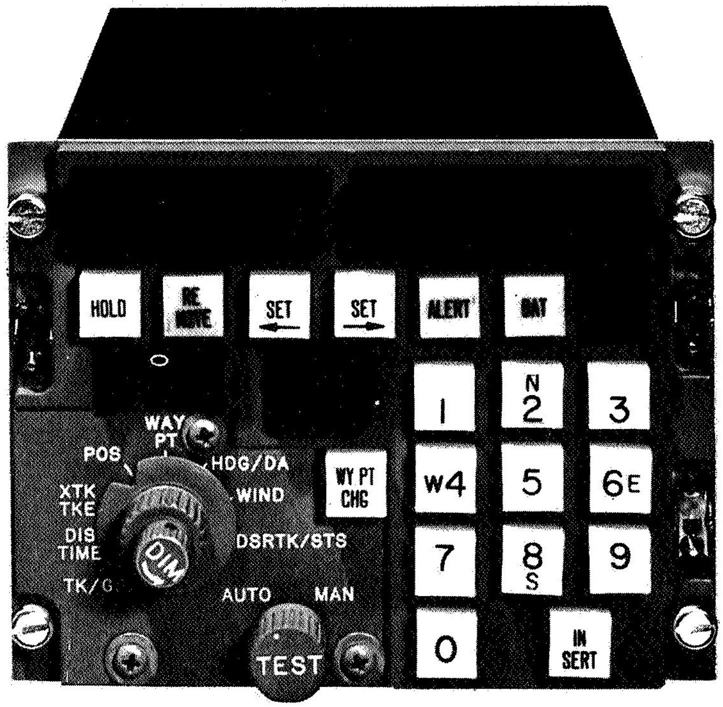

Figure 85. AC Electronics Control and Display Unit for Magic 311

4.5.3.2.3 <u>General Precision and Nortronics</u>

More elaborate avionic displays are available from the Kearfott Products Division of General Precision and from Nortronics. Photographs of these units are shown in Figures 86, 87, and 88. Since they are somewhat more elaborate than is necessary for the present application, no further description will be given. One of the Kearfott units is close enough to the Litton and AC units to be considered an alternate to them. The cost of the Nortronics unit is from $7,000 in lots of 1500 to $11,600 in lots of 10 (budgetary estimate). Prices were not obtained for the Kearfott units.

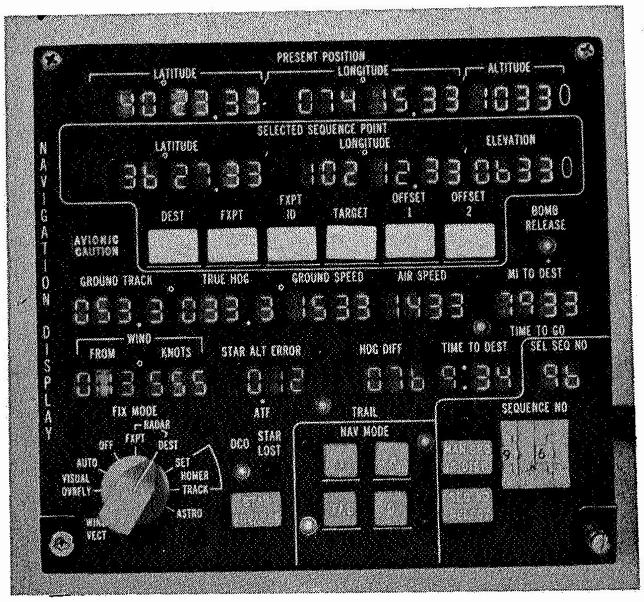

Figure 86. Kearfott Display Unit

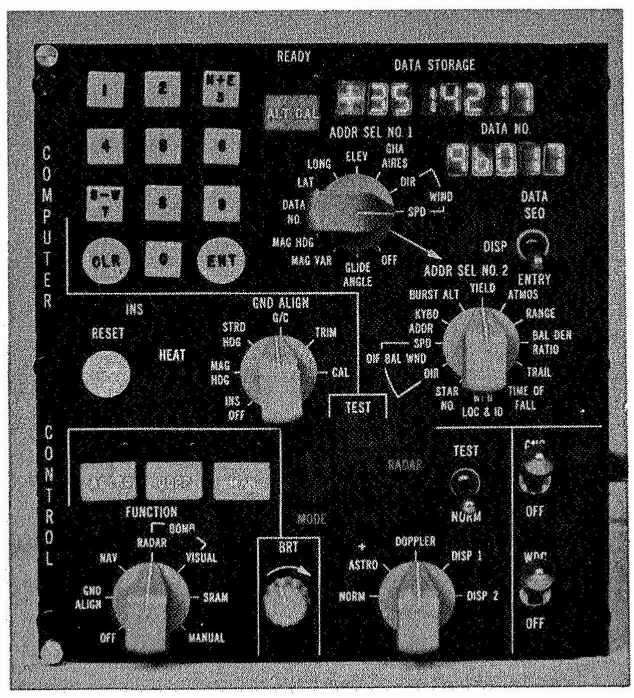

Figure 87. Kearfott Control Unit

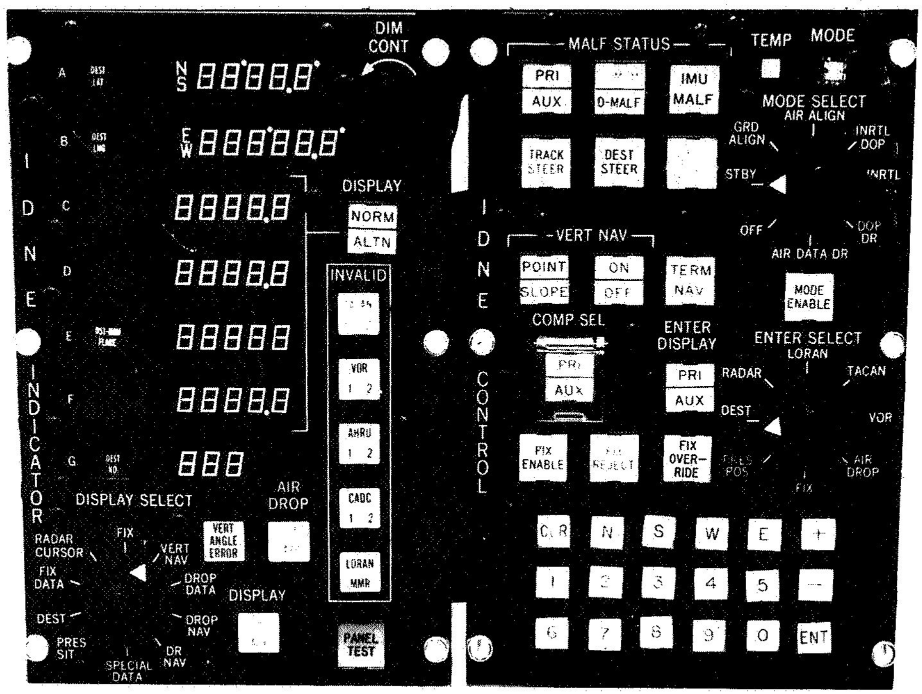

Figure 88. Nortronics Control and Display Unit

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4. Wilkinson, E.J., "A Circularly Polarized Slot Antenna," The Microwave Journal, March 1961, pp 97-100.

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APPENDIX A

NEW TECHNOLOGY

New technology and innovations developed under this contract are discussed in the appendix to vol. I.

APPENDIX B

RANGING MODULATION STUDIES FOR USER POSITION LOCATION USING A NAVIGATION SATELLITE SYSTEM

1. INTRODUCTION

The choice of a ranging subsystem design for the navigation satellite system will depend on several factors and design parameters of particular importance to the navigation satellite program. The important factors that are to be considered in this choice are:

- User Receiver Complexity and Cost
- Ranging Power Efficiency
- Satellite Equipment Complexity
- Multipath Error Sensitivity
- Efficiency for Data Transmission

The first factor is perhaps the most important since a low cost receiver will expand the user spectrum and results in a more useful and economical navigation system. The signal power required at the receiver to perform the ranging function should be a minimum in order to keep the satellite transmitted power to a minimum and to permit signal reception with an omni-directional antenna. Satellite equipment complexity should also be minimized to increase overall reliability of the satellite network but simplification of the satellite equipment should not be made at the expense of complicating the user receiver. At low elevation angles multipath signal reception from reflected rays can cause excessive errors in range measurement. Design of the ranging signal to minimize the error sensitivity to multipath reception should be considered. Data on satellite ephemeris, oscillator drift, etc., is transmitted by the satellite to the user. Combining the data transmission with the ranging signal on one RF carrier is preferred over separate carriers in order to minimize satellite and user equipment. Therefore, the ranging signal design should be compatible with the efficient transmission of data on the same carrier.

The important design parameters for the ranging subsystem are listed below:*

Range Difference Accuracy	50 ft rms random 50 ft rms bias
Range Difference Ambiguity	2000 nmi (±1000 nmi)
Receiver Acquisition Time	≤ 2 sec
RF Carrier Frequency	L-band (1540 to 1660 MHz)

The actual maximum range difference possible between pairs of satellites for the selected satellite orbits is ±0. 92 times an earth radius or a total of 6300 nmi. However, an ambiguity of 2000 nmi (±1000 nmi) is felt to be adequate for resolving user position and the reduced ambiguity helps to simplify the range signal design enough to warrant its use. The receiver acquisition time should be as small as possible in order to maximize the number of user position fixes per minute. A two second value is felt to be the maximum desirable. With eight time division multiplexed satellites a fix every 16 seconds is possible. The fix time can be reduced to a minimum of two seconds by using frequency multiplexed satellites or to some intermediate value by a combination of time and frequency division multiplexing. The use of the 1540 to 1660 MHz frequency band has been discussed elsewhere[1] and will not be covered here except to mention that this band has already been designated for radionavigation use.

Using the preceding design parameters as ground rules, several ranging systems were designed and compared against the factors listed at the beginning of this report. The ranging techniques that were investigated can be broken down into two main categories and are listed below. Data transmission on the same carrier as the ranging signal was also investigated and is discussed in a separate section.

CW systems:
1) Fixed Tones
2) Swept Tone
3) Digital Code

Pulse systems:
1) Pulse
2) Pulse Compression

---

*In the NAVSTAR system a user makes range measurements which in reality are pseudo ranges since the user clock is not synchronized with the satellite clocks. However, true range differences between pairs of satellites are obtained by differencing the pseudo range measurements from the two satellites.

2. SUMMARY

A summary of the key parameters for the ranging system studied in this report are shown in Table 1. The required received signal powers were computed for total acquisition times of two seconds or less. The two seconds represents a desirable upper limit for the Navsat system. Faster acquisition times are obtainable with increased values of received signal power as shown by the plots* in Figures 3 through 6. The total acquisition times shown in the table are the sum of the carrier acquisition (CW systems only), range acquisition, and data acquisition times. Data is time division multiplexed with the ranging as this is shown to result in faster total acquisition than frequency multiplexing of the range and data.

Of all the CW systems, the BINOR code is seen to be superior to the others. In particular, when the segmented method of transmitting the BINOR code is used, the acquisition times are a minimum. In addition to the superiority of the BINOR code in regards to required signal power and acquisition time, the receiver and range acquisition circuitry for the code is felt to be the simplest to implement of all the CW systems. This feeling is based on the assumption that the code digital techniques are easier to design and more reliable than the analog filtering techniques necessary with the tone systems. In addition, the amount of digital hardware necessary for acquisition of the BINOR code is much less than is necessary with the much more complex acquisition of the PRN code. The segmented transmission of the BINOR code though resulting in more rapid acquisition has the disadvantage of creating difficult synchronization problems in the receiver and is not recommended at present. Further work on the segmented transmission technique is necessary to find possible solutions to this problem. The satellite equipment design and complexity should also be a minimum with the BINOR code, again since digital techniques are used to generate the code compared to analog techniques for the tone systems and also since the transmitter power is a minimum.

*Plots are shown as a function of the ratio of received signal power-to-noise spectral density rather than the received signal power only as portrayed in Table 1.

TABLE 1.

SUMMARY OF SYSTEM PARAMETERS

System*	Modulation**	RF BW	Total Acquisition Time (sec)	Required Received Signal Power† (dbm)
Fixed Tones	PM (5 Tones)	700 kHz		
Low Deviation	<1.0 rad each	700 kHz	2.0	-133.0
High Deviation††	8.0 rad each	5.5 MHz	2.0	-133.0
Swept Tone	PM (1 Tone Swept 48 kHz)			
Low Deviation	1.84 rad	700 kHz	2.0	-132.3
PRN Code	PSK (±1.2 rad)			
320 kHz clock	640 kb/sec	3.2 MHz	2.0	-130.6
BINOR Code	PSK (±1.15 rad)			
320 kHz clock	640 kb/sec	3.2 MHz	1.5 (1.1)***	-134.3
1.28 MHz clock††	2.56 Mb/sec	12.8 MHz	2.0 (1.2)	-134.3
Pulse Compression				
100:1 ratio	20 μs chirp pulse 5.0 MHz sweep	5.0 MHz	0.9	-108.3 PK -136.2 AV

*Includes 130 bits of data transmission.

**Modulation also includes bi-phased data subcarrier for CW system and 4-position PPM data for pulse compression system with data modulation time division multiplexed with range modulation.

***Values in parentheses are for the segmented method of transmitting BINOR code.

†For receiver noise Figure of 4.0 db.

††For added protection against range errors due to multipath reception

In particular with the swept tone system, each satellite must provide the same number of cycles during a sweep and hence control circuits must be designed to provide this function.

The pulse compression system is seen to result in the fastest acquisition time of all. This is the primary attraction of the pulse compression system. The unknowns in the system are the practicality and reliability of large peak powers for the satellite transmitter (20 kw) and the cost and size of the 100 to 1 pulse compression filter required in the receiver. The above factors plus cost studies on the pulse and CW receivers remain to be completed before the final choice of a ranging system can be made with confidence. In addition, further studies need to be done on multipath reception at L-band and the magnitude of range measurement errors caused by multipath for each of the systems studied in this report.

3. RANGING SIGNAL DESIGN

3.1 CW TECHNIQUES

There are primarily in use today three types of CW ranging systems—fixed tones, swept tone, and digital code. Examples of these three systems have been designed to meet the NAVSTAR requirements given in Section 1. All three of these systems have one common feature. The fine range measurement (or the measurement accuracy) is obtained from measuring the phase of a sinusoidal or square-wave signal. The accuracy increases as the frequency or bandwidth of the signal increases. The difference in these systems is the way in which the range ambiguity in the period is resolved. In the following sections the three system designs are discussed in detail and compared with each other. A power budget for the L-band RF link from the satellite to the user is shown in Table 2 and establishes the available signal power at the receiver for the ranging function. The power budget assumes a 50 watt satellite transmitter, an earth coverage satellite antenna, and an upper hemispherical coverage antenna for the user. In order to keep the satellite transmitter power to a minimum, the ranging system should perform to requirements with a minimum level signal at the receiver. It would be desirable if both the ranging and data transmission requirements could be met with the 50 watt transmitter.

TABLE 2.

NAVSAT RF LINK POWER BUDGET
F_C = 1600 MHZ

Parameter	Value
Satellite Transmitter Power (50 watts)	+47.0 dbm
Circuit Losses	1.0 db
Satellite Antenna Gain (earth coverage)	16.0 db
Space Loss (22,000 n mi)	188.1 db
User Antenna Gain	0.0 db
Polarization Losses	0.3 db
Circuit Loss	1.4 db
Net Transmission Loss	175.3 db
Received Carrier Power (C)	-128.3 db
Receiver Noise Spectral Density (Φ)(N.F. =5.0 db)	-170.0 dbm/Hz
Received C/Φ	41.7 db-Hz

Phase modulation of the RF carrier by the ranging signal is the best modulation technique to use. A phase lock receiver can then be used for coherent demodulation of the ranging to obtain maximum power efficiency for the RF link. Noncoherent techniques which do not require acquisition of a carrier are prohibitive in their power requirements and have therefore been ruled out for the Navsat application. The drawback to coherent detection is the necessity for acquisition of the RF carrier. Since the overall receiver acquisition time must be as small as possible, rapid acquisition of the carrier is important. Therefore, with any of the three CW techniques, the satellite will initially transmit an unmodulated carrier. This places all available transmitter power in the carrier and consequently acquisition can be accomplished more rapidly. In addition the possibility of false lock on a modulation sideband component is eliminated.

3.1.1 Carrier Acquisition and Tracking

When the receiver is unlocked, a carrier search is conducted wherein the loop VCO is swept over a frequency uncertainty range. The sweep rate for a high probability of acquisition (better than 90 percent in one sweep) and a reasonably high loop SNR (6.0 db) is given by the following relationship

$$\dot{f} = KB_L^2 \qquad \text{(B-1)}$$

where

$\dot{f}$ = sweep rate (Hz/sec)

B_L = one-sided loop noise bandwidth (Hz)

K = constant

The value of K found in the literature varies between 0.2 and 0.4. Analysis by Viterbi[2] of noise free acquisition indicates a value for K of 0.28. For the purposes here, the conservative value of 0.2 will be used. Since the maximum acquisition time is the time to complete one sweep of the VCO, it is given by

$$\tau = \frac{\Delta f}{\dot{f}} = \frac{5\Delta f}{B_L^2} \qquad \text{(B-2)}$$

where Δf = sweep range or total frequency uncertainty.

The total frequency uncertainty is the sum of the maximum carrier doppler shift and the VCO and transmitter center frequency uncertainties. Since the satellite requires an ultra stable clock source, the transmitter frequency can be derived from this source so that the transmitter frequency uncertainty is negligible (less than ±1 Hz) and does not contribute to the total frequency uncertainty. The receiver loop VCO can be designed for a stability of ±0.0001 percent.* For a doppler velocity of 3000 ft/sec between the satellite and the receiver the total frequency uncertainty will be 12.8 kHz (±6.4 kHz about 1600 MHz RF carrier). This allows for a high performance supersonic aircraft since the maximum doppler velocity due to the satellite motion is only about 400 ft per second.[3]

The loop bandwith should be as wide as possible in order to decrease the acquisition time. However, the bandwidth is limited by the power in the carrier component as a 6.0 db or better SNR must be maintained in the loop. Therefore the loop noise bandwidth is given by

$$\frac{C}{\Phi(2B_L)} = 6.0 \text{ db}$$

or

$$B_L = \frac{1}{8}\left(\frac{C}{\Phi}\right) \qquad \text{(B-3)}$$

where

$\frac{C}{\Phi}$ = received carrier power-to-noise spectral density ratio

As the initial transmission from a satellite is the unmodulated carrier, all of the received power is in the carrier component and C/Φ is given by the power budget of Table 2. Substituting into Equation (B-2) the value for the frequency uncertainty and the value for the loop bandwidth given

*Investigation of the receiver design after the work in this report was completed indicates a more realistic loop stability is ±0.001 percent which results in a total frequency uncertainty of 40 kHz. Hence, the carrier acquisition time will increase for a given power but the basic conclusions of this report are still valid.

by Equation (B-3), an expression for the maximum acquisition time as a function of C/Φ is obtained.

$$\tau = 4.096 \cdot 10^6 \left(\frac{\Phi}{C}\right)^2 \tag{B-4}$$

where

τ = maximum acquisition time in seconds for one full sweep of the receiver VCO

Plots of Equations (B-3) and (B-4) are shown in Figure 1.

The satellite will transmit the unmodulated carrier for τ seconds to allow time for carrier acquisition on one sweep. If the receiver fails to lock during the τ seconds the satellite transmission is missed and the receiver must wait for the next broadcast. The probability of acquisition during the τ second interval will be better than 90 percent. To increase the acquisition probability the sweep rate can be decreased with a comsequent proportional increase in the acquisition time. After τ seconds the ranging signal modulation appears on the carrier. Since the power in the carrier component will drop after modulation the loop bandwidth must be made smaller to maintain a good SNR in the loop. In addition, the loop bandwidth must be small enough so as not to track out any ranging modulation sideband components near the carrier component. The range ambiguity desired is 2000 n mi. Therefore, the periodicity of the ranging signal or the lowest frequency component in the signal may be 81 Hz and if this is true the phase lock loop bandwidth after acquisition should be less than this value. After carrier acquisition the receiver will be designed to automatically switch the loop bandwidth from the wideband acquisition mode to a narrowband tracking mode. A narrowband loop noise bandwidth of 50 Hz (two-sided) will be adequate. This value is sufficiently below any possible 81 Hz sideband component to prevent its tracking and still large enough to allow an aircraft to undergo a high acceleration maneuver without losing carrier lock.

The maximum acceleration possible without losing lock using the 50 Hz bandwidth is six g's and is derived as follows. The loop tracking

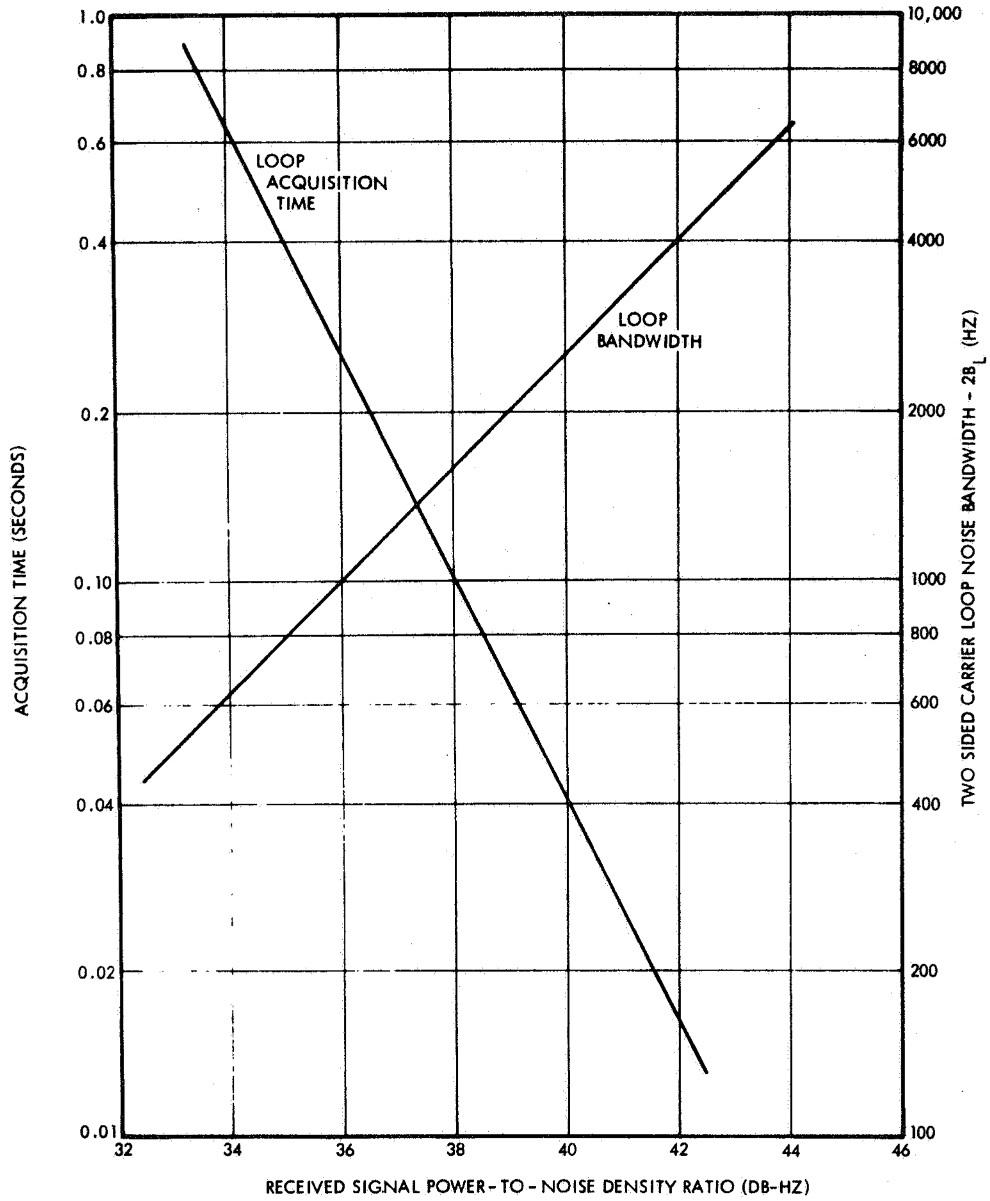

Figure 1. Carrier Loop Acquisition Time and Noise Bandwidth as a Function of Received Signal Power-to-Noise Spectral Density Ratio

error with a frequency ramp input (due to a doppler rate or constant acceleration) is given by the well-known relationship.

$$\epsilon_a = \frac{\dot{\omega}}{\omega_n^2} = 7.03 \frac{\dot{f}}{(2B_L)^2} \qquad \text{(B-5)}$$

where

ϵ_a = loop phase error (radians)

$\dot{\omega}$ = frequency rate due to acceleration (rad/sec^2)

ω_n = loop natural frequency (rad/sec)

$2B_L$ = 1.06 ω_n (for 2nd order loop with $1/\sqrt{2}$ damping)

The frequency rate is related to the acceleration by the doppler expression

$$\dot{f} = \frac{\ddot{r}}{c} f_c = 51.5 \frac{\ddot{r}}{g} \qquad \text{(B-6)}$$

where

$\ddot{r}$ = acceleration (ft/sec^2)

f_c = carrier frequency (1600 MHz)

c = velocity of light (10^9 ft/sec)

g = 32.2 ft/sec^2

With $2B_L$ equal to 50 Hz, Equation (B-5) becomes

$$\epsilon_a = 0.145 \frac{\ddot{r}}{g} \qquad \text{(B-7)}$$

To insure loop lock, the following relationship for the loop phase errors must hold

$$\epsilon_T = \epsilon_a + \rho\sigma_n \leq \frac{\pi}{2} \qquad \text{(B-8)}$$

where

ϵ_T = total loop phase error

ϵ_a = phase error due to acceleration

σ_n = rms phase jitter due to thermal noise in loop

ρ = peak factor for the thermal noise jitter

The rms jitter σ_n is given by the loop SNR. In the narrowband tracking mode the loop SNR should be increased from the 6.0 db value during acquisition so that the noise jitter on the carrier reference will not cause significant degradation of the demodulated ranging signal. A loop SNR of 10 db is felt to be adequate for this purpose and therefore the modulation index of the ranging signal will be so specified as to leave adequate power in the carrier component for a 10 db or better loop SNR. The jitter σ_n will then be equal to

$$\sigma_n = \frac{1}{\sqrt{2\,(\mathrm{SNR})_{\mathrm{loop}}}} = \frac{1}{\sqrt{20}} \qquad \text{(B-9)}$$

Using a value of three for ρ which for a gaussian distribution on the phase jitter results in a 0.997 probability of the loop remaining in lock, Equation (B-8) can now be expressed as

$$\frac{\ddot{r}}{g} \leq 6.9\left(\frac{\pi}{2} - \frac{3}{\sqrt{20}}\right) = 6.2 \qquad \text{(B-10)}$$

Therefore, the acceleration $\ddot{r}$ can be more than 6 g's before the loop will break lock.

With the RF carrier acquired and being tracked by the phase lock loop, the demodulated ranging signal will appear at the output of the receiver wideband phase detector. Acquisition of the range must now occur in the range acquisition and readout equipment following the receiver. This is discussed in the following sections for the three different CW ranging techniques being considered in this report.

3.1.2 Fixed Tones

In a fixed tones system, the ranging signal consists of a group of coherent tones each of which modulates the RF carrier. By a series of phase measurements starting with the lowest frequency tone and ending with the highest frequency tone, the accuracy of the range measurement is stepwise increased to that of the highest tone while the ambiguity resolution is equal to the period of the lowest tone.

The accuracy of the range measurement is determined by the magnitude of the top tone frequency and the SNR of that tone. The rms phase noise (in radians) on the tone is equal to

$$\sigma_n = \frac{1}{\sqrt{2(S/N)_t}} \tag{B-11}$$

where

$(S/N)_t$ = SNR of tone at tone filter output

and the corresponding rms range measurement error is

$$\sigma_R = c\left(\frac{\sigma_n}{2\pi f_t}\right) \tag{B-12}$$

where

σ_R = rms range error in feet

f_t = tone frequency

c = velocity of light

These two equations can be used to establish the top tone frequency and the tone SNR. The top tone should be as low in frequency as possible to keep the bandwidth and the total number of tones to a minimum but must be large enough to meet the range accuracy requirement. A practical limit on measuring the phase of a tone in a simple receiver is about 1/100 of a cycle. The range accuracy requirement previously specified is 50 feet rms random error in range difference. Since a range difference is made up of two independent range measurements the error in each range measurement must be $50/\sqrt{2}$ or 35 feet rms. Therefore, from Equation (B-12) the top tone frequency must be at least 290 kHz. Actually a frequency of 320 kHz has been picked which should provide a slightly better accuracy than 50 feet. From Equation (B-11), the required top tone SNR is 21 db.

The next question is the choice of the frequency ratio to be used for the lower ambiguity resolving tones. Each tone must resolve the ambiguity of the next highest tone which is equal to one cycle of that tone. Assuming that the total rms phase errors are equal and independent for each tone, the tone ratio must have the following relationship.

$$\sqrt{r^2 + 1}\,\sigma_T \leq \frac{\pi}{F} \tag{B-13}$$

where

r = ratio of a tone to the next lower tone

F = confidence factor for resolving ambiguity, expressed as a multiple of the rms value σ_T

The rms error σ_T is equal to

$$\sigma_T = \sqrt{\sigma_n^{\ 2} + \sigma_b^{\ 2}} \tag{B-14}$$

where

σ_b = rms phase bias error due to bias error sources in the receiver and tone filters

Assuming for present purposes that the bias error is zero and substituting Equation (B-11) into (B-13), the tone SNR's for ambiguity resolution must be

$$(S/N)_t \geq \frac{(r^2 + 1)\,F^2}{2\pi^2} \tag{B-15}$$

The number of tones is given by

$$f_h/f_l = r^{n-1} \tag{B-16}$$

where

f_h = highest tone for range accuracy

f_l = lowest tone for range ambiguity

n = number of tones

The lowest tone must be 81 Hz or less to achieve the 2000 n mi ambiguity resolution. Having previously established the top tone at 320 kHz the magnitude of r^{n-1} is equal to 3960. Using Equations (B-15) and (B-16) an optimum choice for r and n can be calculated based on the minimum total signal power necessary to achieve the ambiguity resolution. The optimum choice for the ratio r turns out to be approximately two.[4] However, a tone ratio of two requires 13 tones which results in more complex receiver and range extraction equipment.*

The simplest receiver would require the smallest number of tones and consequently the largest possible ratio r. The magnitude of r is limited by bias error sources which limit the accuracy of the phase measurement. Experience indicates that the ratio r should not exceed eight for reliable ambiguity resolution. This value results in four ambiguity tones plus the top tone of 320 kHz and a value for r^{n-1} of 4096. To reduce the number of ambiguity tones to three, the tone ratio would have to be 16. With a ratio this high the receiver may have difficulty resolving ambiguity with high probability unless the receiver and tone filters are carefully aligned to reduce bias error sources. Therefore, the fixed tones ranging system will be designed with the five tone frequencies shown in Table 3.

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*A ranging system has been devised which is equivalent to a fixed tones ranging system with tone ratios equal to two and is covered later on in this report under the digital code discussion.

TABLE 3

FIXED TONES PARAMETERS

	Ambiguity Tones(*)	Accuracy Tone(**)
Tone SNR	21 db	21 db
Random Error (σ_n)	0.0628 rad	0.0628 rad (0.01 cycles)
Bias Error (σ_b)	0.084 rad	0.0628 rad
Total Errors (σ_T)	0.105 rad	0.089 rad
Accuracy	-	31 ft random (***)
		31 ft bias(***)

---

*Tone Frequencies: 40 kHz, 5 kHz, 625 Hz, 78.125 Hz.
**320 kHz.
***For a range difference measurement the random error is $\sqrt{2}$ larger or 44 feet and the bias error is also $\sqrt{2}$ larger provided the bias errors are independent for each range measurement.

Also shown are the required tone SNR's and the acceptable total rms bias errors to resolve each range ambiguity with 99.9 percent confidence. This requires F to be 3.7 assuming that the random and bias errors have gaussian distribution.

An alternative to transmitting the five tones as shown is to translate the four lower tones about the top tone and transmit a group of tones in the vicinity of the top tone. For example, the following group of tones may be transmitted:

Translation	Frequency (kHz)
None	320.0
320-5	315.0
320-40	280.0
320-40 +5 +0.625	285.625
320-40 -5 -0.078125	274.921875

The advantage of transmitting the tones in this manner is that the range signal occupies only a small region of the receiver bandwidth easing the phase and amplitude design requirements in the receiver and the tone filters. The best method for transmitting the tones will be the one resulting in the lowest cost receiver.

The acquisition time for the range measurement and the signal power at the receiver necessary to provide the accuracy and ambiguity resolution is computed as follows. The acquisition time is dependent on the bandwidth used in the tone filters to obtain the required 21 db tone SNR's. For passive bandpass filters of low order the settling time of the tone phase at the filter output is approximately

$$\tau \approx \frac{1}{B} \qquad \text{(B-17)}$$

where

B = 3 db filter bandwidth

For phase lock loop tracking filters, the loop acquisition time can be longer than for an equivalent passive filter. However, passive filters have phase stability problems that are eliminated by tracking filters. For this reason in a high accuracy, high tone ratio system tracking filters are used and are especially used with the high accuracy top tone. From phase plane trajectories for second-order phase lock loops given by Sanneman and Rowbotham,[5] the time to phase lock can be computed for the case where the initial frequency error between the incoming tone and the loop VCO is less than the noise bandwidth of the loop. Assuming as previously for the carrier loop a VCO stability of ±0.0001 percent* and a maximum doppler velocity of 3000 feet per second, the maximum frequency error occurs for the 320 kHz top tone and is 1.3 Hz. For a worst case initial phase error of 180 degrees, the loop acquisition time or the time to reduce the frequency error to zero and the phase error to less than 1/100 of a cycle has been plotted as a function of the loop noise bandwidth in Figure 2 for several different values of the initial frequency error normalized to the loop noise bandwidth. One of the dashed curves is a plot of the acquisition time for an initial frequency error of 1.3 Hz and thus represents the acquisition time for the top tone. The acquisition times for the ambiguity tones will be about the same or less since the doppler shift and consequently

*See footnote page 8.

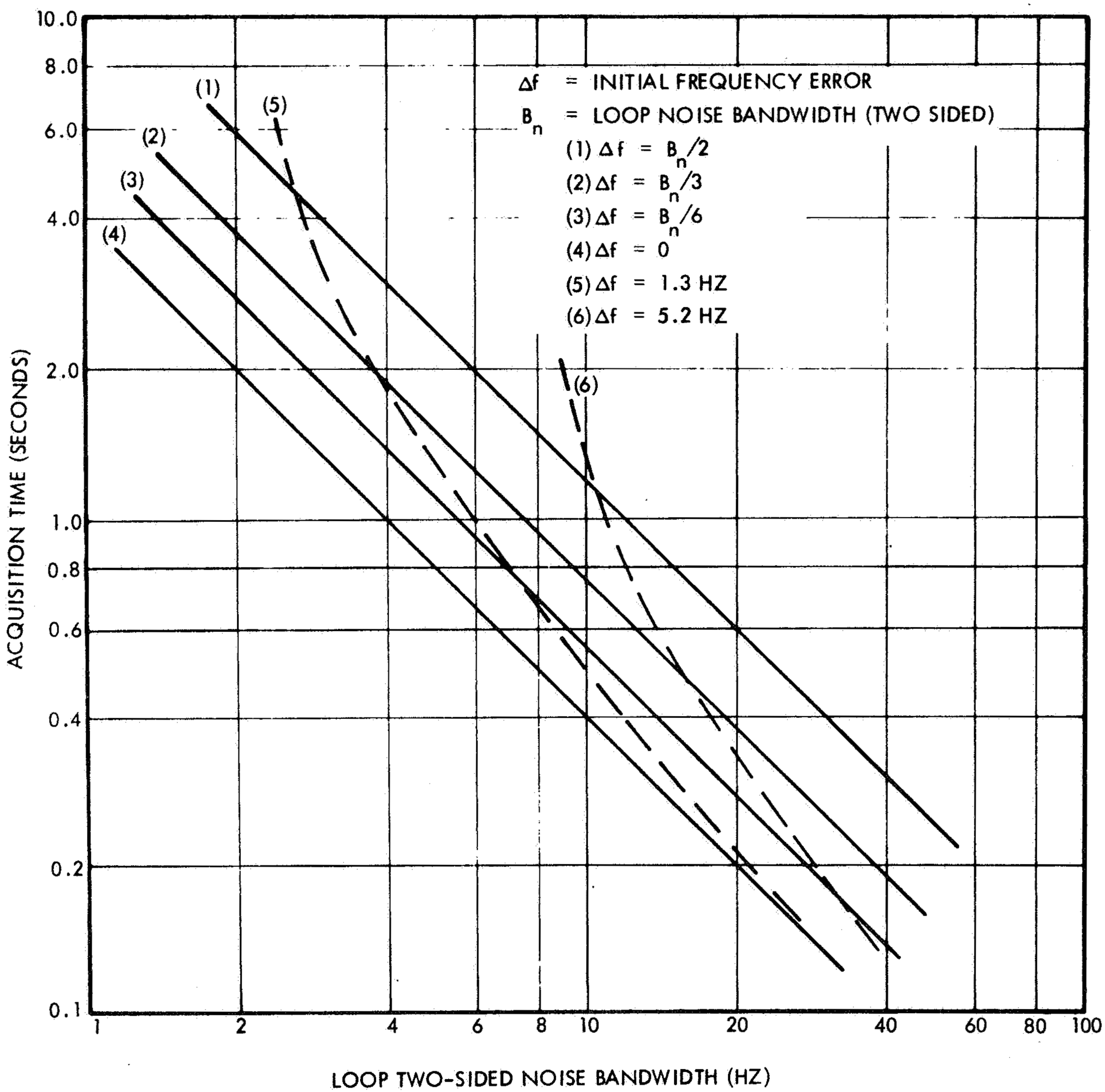

Figure 2. Acquisition Time for a Second Order Phase Lock Tracking Filter

initial frequency error will be less particularly if the lower tones are transmitted without frequency translation. Therefore assuming that the range acquisition circuitry is mechanized so that all of the tones are acquired in parallel the total range acquisition time will be equal to the top tone acquisition time. Some mechanizations may use sequential acquisition of the tones which of course increases the total range acquisition time. For purposes here, parallel acquisition will be assumed.

Figure 2 establishes the range acquisition time for a given set of tone filter bandwidths. The next task is the establishment of the necessary signal power at the receiver to maintain the carrier loop in lock and to obtain 21 db tone SNR's at the tone filter outputs. The five tones each phase modulate the carrier with small deviations. Under multipath signal reception conditions high deviations prove to be desirable and this situation is discussed in the section on multipath reception. For present purposes low deviations will be used in which the majority of the tone powers are in the first order sidebands. Since with a carrier only tracking loop in the receiver the recoverable tone powers after demodulation are in the first-order sidebands only, the tone modulation indices should be picked which maximize the first-order sideband powers. This is subject to the constraint of sufficient power in the carrier component to maintain the receiver loop in phase lock and provide a clean coherent reference for demodulation. A loop SNR of 10 db is specified for this purpose. Consequently, the following equations must hold.

$$\frac{CM_t^{(i)}}{\Phi B_t^{(i)}} = 21 \text{ db} \tag{B-18a}$$

$$\frac{CM_c}{\Phi(2B_L)} \geq 10 \text{ db} \tag{B-18b}$$

where

$\frac{C}{\Phi}$ = received signal power-to-noise spectral density ratio

$M_t^{(i)}$ = modulation loss for ith range tone

M_c = modulation loss for carrier component

$B_t^{(i)}$ = noise bandwidth of ith tone filter

$2B_L$ = carrier loop noise bandwidth (50 Hz)

i = 1, 2, 3, 4, 5

The modulation losses are equal to

$$M_t^{(i)} = 2J_1^{\,2}(\beta_i) \prod_{\substack{m=1 \\ m \neq 1}}^{5} J_o^{\,2}(\beta_m)$$

$$M_c = \prod_{m=1}^{5} J_o^{\,2}(\beta_m) \qquad \text{(B-19)}$$

where

β_m = modulation index of mth tone

Using a set of bandwidths derived for a specific acquisition time, Equations (B-18) and (B-19) can be used to derive the required C/Φ. A set of indices β_m is chosen which minimize the set of modulation losses $M_t^{(i)}$. A sample calculation goes as follows.

Assume a top tone filter bandwidth of 10 Hz which from Figure 2 results in an acquisition time of 0.5 seconds. Using curve (4) in Figure 2 for the other four tones, the filter bandwidths cannot be less than 8 Hz in order not to exceed the 0.5 second acquisition time of the top tone. Using this set of bandwidths Equation (B-18) reduces to

$$\frac{CM_t^{(1)}}{\Phi} = 31 \text{ db-Hz} \qquad \text{(B-20a)}$$

$$\frac{CM_t^{(i)}}{\Phi} = 30 \text{ db-Hz} \qquad i = 2, 3, 4, 5 \tag{B-20b}$$

$$\frac{CM_c}{\Phi} \geq 27 \text{ db-Hz} \tag{B-20c}$$

From an optimization procedure[6] the optimum set of modulation indices for the above requirements and the corresponding modulation losses are

$$\beta_1 = 0.70 \qquad M_t^{(1)} = -10.2 \text{ db}$$

$$\beta_2 = \beta_3 = \beta_4 = \beta_5 = 0.63 \quad M_t^{(2)} = M_t^{(3)} = M_t^{(4)} = M_t^{(5)} = 11.2 \text{ db}$$

$$M_c = -4.7 \text{ db}$$

From these results the required C/Φ is 41.2 db-Hz. It will be noted that the carrier loop SNR will exceed 10 db by a large margin so that more power than necessary is in the carrier. This condition cannot be avoided as it is characteristic of coherent carrier demodulation of low deviation PM systems. Removing additional power from the carrier by use of larger indices also removes power from the first-order sidebands. The removed power goes into higher order sidebands which are not recoverable.

Figure 3 is a plot of the fixed tones ranging acquisition time versus the signal power-to-noise spectral density ratio at the receiver (C/Φ). In addition, the total acquisition time is plotted which equals the carrier loop acquisition time given in Figure 1 added to the tones range acquisition time. For the above sample calculation, the carrier acquisition time is 0.024 second and the corresponding loop acquisition bandwidth ($2B_L$) is 3200 Hz. The total acquisition time is then 0.524 second. Other points on the curve have been similarly derived. If a 6 db power margin is desired from the power budget given in Table 2, a total acquisition time of about 2.9 seconds would be required.

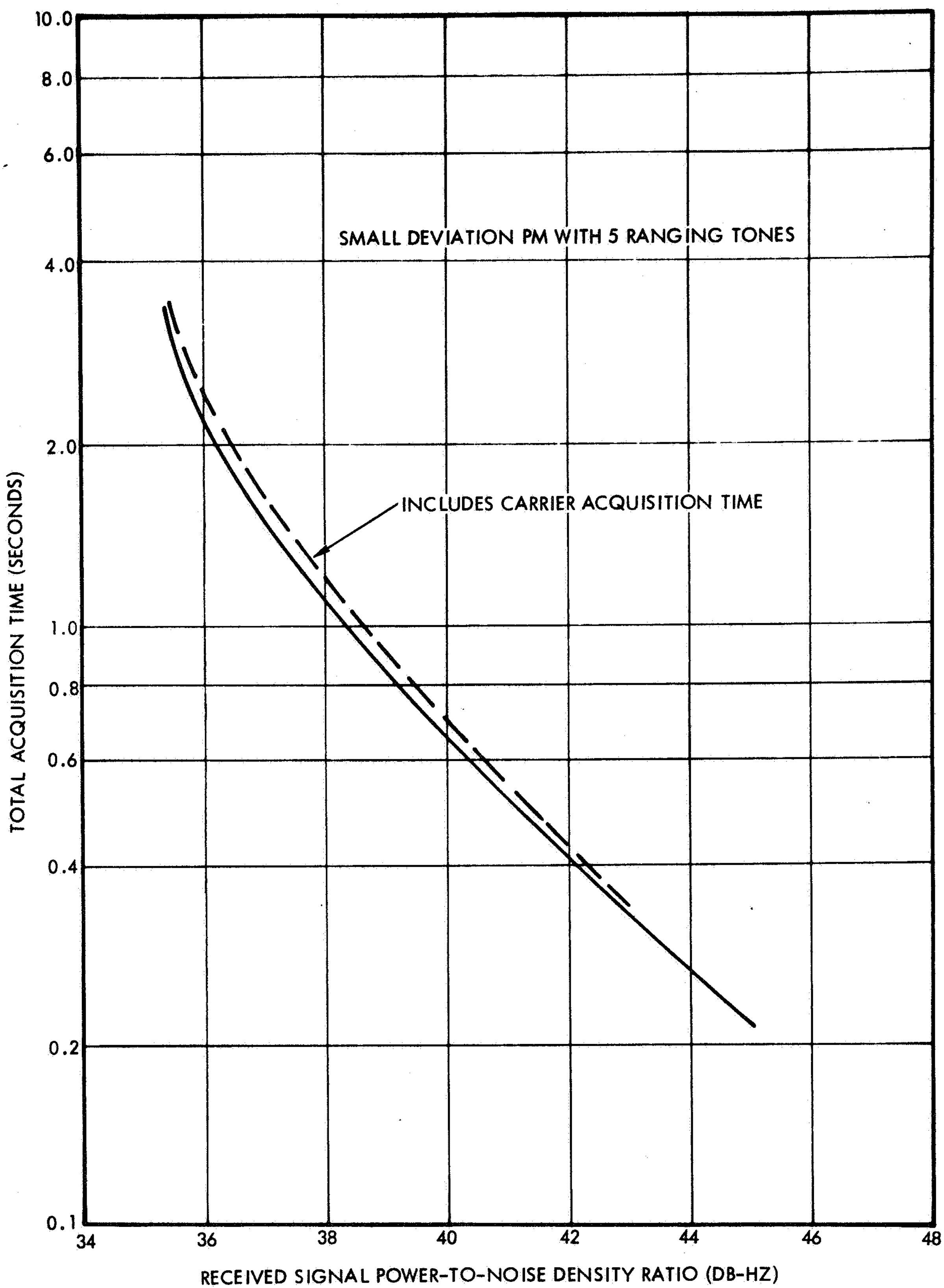

Figure 3. Acquisition Time versus Received Signal Power-to-Noise Spectral Density Ratio for Fixed Tones Ranging System

3.1.3 Swept Tone

In a swept tone system the ambiguity tones of the fixed tones system are replaced by a single tone which is swept in frequency over a large enough range to resolve the ambiguity. Typically a tone is swept from a lower frequency to a higher frequency. The fine range measurement or range accuracy is obtained by measuring the phase of the tone at the end of the sweep and in this regard is identical with the fixed tones system. Therefore for the same reasons developed for the fixed tones system, the highest frequency in the sweep will be 320 kHz. The range ambiguity is resolved by counting the number of cycles of phase shift of the sweep tone and the carrier doppler during the tone sweep.*

The number of cycles of phase shift is given by the difference between the phase shift at the end of the sweep and at the beginning of the sweep.

$$N_s = \frac{R_2 f_2}{c} - \frac{R_1 f_1}{c} \quad \text{with } f_2 > f_1 \qquad \text{(B-21)}$$

where

N_s = cycles of phase shift

f_2 = frequency at end of sweep

f_1 = frequency at start of sweep

c = velocity of light

R_2 = range at end of sweep

R_1 = range at start of sweep

*Further details on the theory of swept tone ranging can be found in Reference 7.

The range R_2 is the desired measurement. The range R_1 can be related to R_2 by counting the doppler cycles of the carrier frequency. The doppler velocity during the tone sweep is

$$\dot{R} = \frac{R_2 - R_1}{T_s} = c\,\frac{f_d}{f_c} \tag{B-22}$$

where

T_s = tone sweep time

f_c = RF carrier frequency

f_d = doppler shift on carrier

Rearranging Equation (B-22)

$$R_2 - R_1 = c\,\frac{f_d T_s}{f_c} = \frac{cN_c}{f_c} \tag{B-23}$$

where

N_c = cycles of doppler shift during time T_s

and substituting into Equation (B-21), the range R_2 is equal to

$$R_2 = \frac{c}{f_2 - f_1}\left(N_s - \frac{f_1 N_c}{f_c}\right) \tag{B-24}$$

This is the coarse unambiguous range measurement. The accuracy with which this measurement is determined depends on the accuracy with which the cycle counts N_s and N_c are measured. The errors in these counts are given as follows

$$\Delta N_s = \Delta q_2 - \Delta q_1 \tag{B-25a}$$

$$\Delta N_c = \Delta p_2 - \Delta p_1 \tag{B-25b}$$

where

$$q_2 = \frac{R_2 f_2}{c} \qquad q_1 = \frac{R_1 f_1}{c}$$

$$p_2 = \frac{R_2 f_c}{c} \qquad p_1 = \frac{R_1 f_c}{c}$$

Therefore, the error in R_2 from Equation (B-24) is

$$\Delta R_2 = \frac{c}{f_2 - f_1}\left[\Delta q_2 - \Delta q_1 - \frac{f_1}{f_c}\left(\Delta p_2 - \Delta p_1\right)\right] \qquad \text{(B-26)}$$

However, since $f_1 << f_c$ the doppler count error is small compared to the tone sweep count error and can therefore be ignored. Thus ΔR_2 becomes

$$\Delta R_2 = \frac{c}{f_2 - f_1}\left(\Delta q_2 - \Delta q_1\right) \qquad \text{(B-27)}$$

The fine range measurement is made at the end of the sweep so that the error $\Delta R_2'$ in this measurement is given by

$$\Delta R_2' = \frac{c}{f_2} \Delta q_2 \qquad \text{(B-28)}$$

To resolve the ambiguity in the fine range measurement, the error in the coarse range measurement minus the error in the fine range measurement must not exceed one half of a cycle of the fine range tone ambiguity.

$$\Delta R_2 - \Delta R_2' \leq \frac{c}{2f_2} \qquad \text{(B-29)}$$

Consequently from Equations (B-27) and (B-28), the following result is obtained.

$$f_1 \Delta q_2 - f_2 \Delta q_1 \leq \frac{f_2 - f_1}{2} \qquad \text{(B-30)}$$

Since the errors Δq_2 and Δq_1 are independent

$$f_1^2 \sigma_{q_2}^2 + f_2^2 \sigma_{q_1}^2 \leq \left(\frac{f_2 - f_1}{2F}\right)^2 \tag{B-31}$$

where

$$\sigma_q = \text{rms error}$$

The confidence factor F is introduced and assuming 99.9 percent probability of correct range ambiguity resolution is desired as in the fixed tones system, F is equal to 3.7 for the assumed gaussian distribution on the errors. The two rms errors will be equal if the tone SNR is the same before and after the sweep. Assuming the total bias error is equal to the random or noise error and taking the rms sum of the two error sources,

$$\sigma_{q_2} = \sigma_{q_1} = \frac{1}{2\pi\sqrt{(S/N)_{f_s}}} \tag{B-32}$$

where

$$(S/N)_{f_s} = \text{tone SNR before and after tone sweep}$$

The sweep range $f_2 - f_1$ is given from Equations (B-31) and (B-32) and is equal to

$$f_2 - f_1 \geq \frac{F\sqrt{f_2^2 + f_1^2}}{\pi\sqrt{(S/N)_{f_s}}} \tag{B-33}$$

The value for $(S/N)_{f_s}$ must be 21 db in order to obtain the same fine range accuracy as for the fixed tones system and with F equal to 3.7 Equation (B-33) reduces to

$$f_2 - f_1 \geq 0.105\sqrt{f_2^2 + f_1^2} \tag{B-34}$$

For a small sweep range $f_2 \approx f_1$

$$f_2 - f_1 \gtrsim 0.149\, f_2$$

Since f_2 must equal 320 kHz for the fine range measurement, the sweep range is approximately 48 kHz.

The length of the sweep in time will be dependent on the bandwidth of the phase lock loop filter that is used to track the swept tone. Assuming a linear tone sweep, the peak phase error in the loop (second order) during the sweep is equal to

$$\epsilon_p = \frac{1.12\, D}{B_N^2} = \frac{2.24\pi\,(f_2 - f_1)}{B_N^2 T_S} \qquad \text{(B-36)}$$

where

B_N = two-sided loop noise bandwidth (Hz)

D = sweep rate (rad/sec^2)

T_S = sweep time

Rearranging Equation (B-36) the loop noise bandwidth is equal to

$$B_N = 2.66 \left(\frac{f_2 - f_1}{\epsilon_p T_S} \right)^{1/2} \qquad \text{(B-37)}$$

Since it is necessary for the loop to maintain lock during the sweep Equation (B-8) must also hold here with ϵ_p replacing ϵ_a. Therefore ϵ_p must not exceed

$$\epsilon_p \le \frac{\pi}{2} - \frac{3.7}{\sqrt{2(\mathrm{SNR})_{loop}}} \qquad \text{(B-38)}$$

where

ρ = 3.7 which gives 99.9 percent confidence loop will not break lock during sweep

$(SNR)_{loop}$ = signal-to-noise ratio in the loop during sweep

The SNR in the loop during the sweep should be as small as possible in order to minimize the power requirements. A minimum value which should be adequate for tracking is 6.0 db.* This means that the tone tracking loop must be widened after measurement of q_1 and then narrowed again prior to measurement of q_2 so as to change the tone SNR from 21 to 6 db back to 21 db again.

The phase error ϵ_p from Equation (B-38) cannot exceed 1/4 for a 6.0 db loop SNR. Substituting this value and the 48 kHz tone sweep in Equation (B-37) the loop bandwidth during sweep must equal

$$B_N = \frac{1166}{\sqrt{T_S}} \qquad \text{(B-39)}$$

The received signal power requirement is given by

$$\frac{CM_t}{\Phi B_N} = 6.0 \text{ db} \qquad \text{(B-40)}$$

where

$M_t = 2J_1^2(\beta_t)$ (tone modulation loss)

β_t = modulation index of tone

*Though not shown here, higher loop SNR's during sweep will increase the required signal power at the receiver.

The acquisition time is equal to the sweep time plus the time to acquire the tone phase prior to the sweep and after the sweep when the loop is narrowed to obtain the 21 db SNR. The loop bandwidth at these times must be 15 db or 31.5 times smaller than during the sweep so that calling this bandwidth B_N'

$$B_N' = \frac{B_N}{31.5} = \frac{37}{\sqrt{T_S}} \tag{B-41}$$

Assuming the loop acquisition time is the same before and after the sweep the total acquisition time for the swept tone system is T_S plus twice the time corresponding to the value of B_N' in Figure 2. These relationships have been used to plot the swept tone acquisition time as a function of C/Φ in Figure 4. The total acquisition time which includes the time to acquire the RF carrier is also plotted in Figure 4 as the dotted line. The modulation loss M_t is a minimum when β_t equals 1.84 radians. However, the corresponding carrier modulation loss is 10 db so that because of the carrier power requirement as given by Equation (B-20c), C/Φ must equal 37 db-Hz or more when β_t is 1.84 radians. For lower values of C/Φ a correspondingly lower value for β_t was used. With a 6.0 db power margin (C/Φ = 35.7 db-Hz) from the power budget in Table 2, a total acquisition time of about 4.5 seconds would be required. This compares to 2.9 seconds for the fixed tones system.

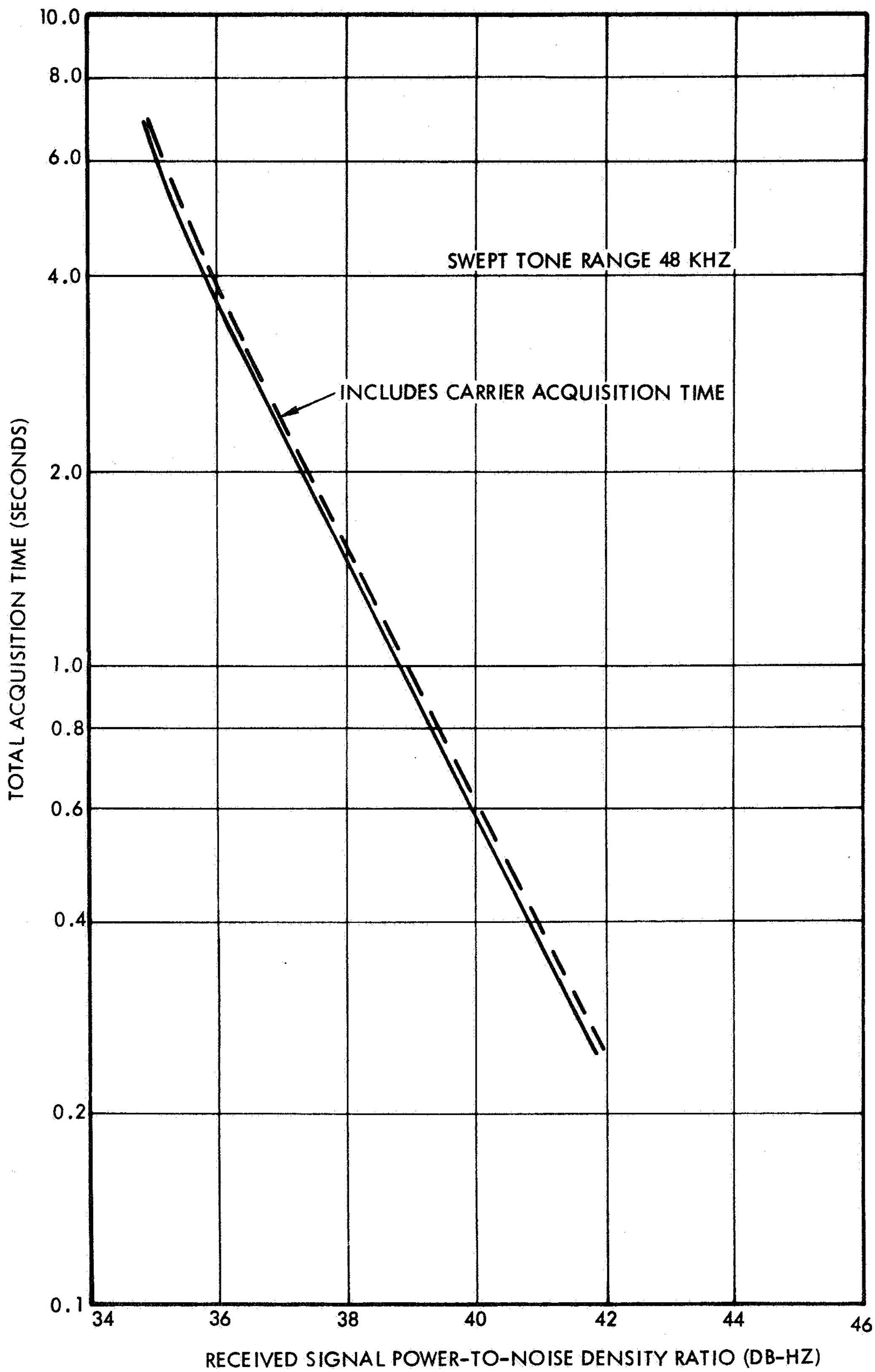

Figure 4. Acquisition Time versus Received Signal Power-to-Noise Spectral Density Ratio for Swept Tone Ranging System

3.1.4 Digital Code

A digital code ranging system repeatedly transmits a binary sequence and then determines the phase of the sequence at the receiver. In actuality the fine range or accuracy measurement is obtained from a phase measurement of the binary sequence's clock frequency and the range ambiguity is resolved by measuring to the nearest bit the phase of the sequence. Therefore, the clock rate for the sequence should be 320 kHz for the reasons developed previously. For 2000 n mi ambiguity the length of the sequence should be at least 8000 bits. The sequence phase can be determined by a correlation of the received sequence with the reference sequence. Since there are 8000 possible phase positions, up to 8000 correlations may be required. Equipment limitations prevent the use of simultaneous determinations of the correlations and excessive acquisition time results from sequential determination of the correlations. Consequently special binary sequences have been developed which reduce the number of required correlations. Two such binary sequences are investigated here. The first is the component structured PRN codes developed at JPL and the second is a code developed by Stiffler[8] which will be called the BINOR code for BINary Optimum Ranging.

The binary sequences will biphase modulate the carrier. Therefore, the RF portion of the receiver will be essentially the same as that used for the fixed and swept tone systems. The difference in the receiver will of course be in the range acquisition circuitry. Since digital techniques are generally easier to implement than analog techniques, mechanization of the range acquisition circuitry should be easier. However, this does not necessarily imply that a digital code system will result in a less costly receiver than an analog technique.

3.1.4.1 PRN Ranging Codes

The theory of operation of the JPL PRN ranging system will not be discussed here as it is well-documented elsewhere.[9] Therefore, the reader will be assumed to be familiar with the operation of the code. The particular PRN code to be evaluated here is a three component plus clock component code which is 8246 bits in length. The boolean logic which forms the code is

$$\text{Code} = \text{cl} \oplus (AB + BC + CA) \cdot \text{cl} \qquad \text{(B-42)}$$

where

$$cl = 320 \text{ kHz clock}$$
$$A = 7\text{-bit PRN code}$$
$$B = 19\text{-bit PRN code}$$
$$C = 31\text{-bit PRN code}$$

The correlation properties of this particular code are shown in Table 4.

TABLE 4

CODE CORRELATION PROPERTIES

	Operation	Reference Code*	Correlation Value (%) Not Acquired	Acquired
1	Acquire cl	0	0	50
2	Acquire A	a · cl	50	75
3	Acquire B	b · cl	50	75
4	Acquire C	c · cl	50	75
5	Tracking	(AB+BC+CA) · cl	-	100

*The lower case letters for the code indicates the reference code is not in phase with the received code.

The acquisition time for the code includes the time for the clock loop to acquire the clock component (step 1 in Table 4) plus the time to acquire the three code components in sequence. These three components could be acquired in parallel, thus decreasing the total acquisition, but at the expense of an impractical increase in acquisition circuitry. Consequently, serial acquisition of the components will be assumed. The clock acquisition time depends on the clock loop noise bandwidth and is again given by Figure 2 for an initial frequency offset of 1.3 Hz. Again also the range accuracy is determined by the clock loop SNR and must equal 21 db prior to the range measurement. After clock acquisition the correlation level is only 50 percent so that after complete code acquisition the loop SNR will increase by 6 db. Therefore, the clock loop ratio can be 15 db initially so that the loop bandwidth must satisfy the following relationship

$$\frac{S\rho^2}{\Phi B_n} = 15 \text{ db} \qquad \text{(B-43)}$$

where

S/Φ = ratio of power in code-to-receiver noise spectral density

ρ = clock correlation (50%)

The acquisition times for the code components are derived from Viterbi's[10] word error probabilities for orthogonal codes. Again assuming a 99.9 percent acquisition probability the required ratio of signal energy to noise spectral density for the seven bit A component is from Viterbi

$$\left(\frac{E}{\Phi}\right)_A = \left(\frac{ST}{\Phi}\right)_A = 4.5 \log_2 7 = 12.6 \tag{B-44}$$

The integration or correlation time for each correlation is then

$$T = 12.6 \left(\frac{\Phi}{S}\right) \tag{B-45}$$

Since seven correlations are required to resolve the phase of the A component and the change in correlation level from Table 4 is 25 percent, the acquisition time for the A component equals

$$T_A = 7 \cdot 16T = 1410 \left(\frac{\Phi}{S}\right) \tag{B-46}$$

Similarly, the acquisition times for the B and C components are

$$T_B = 19 \cdot 16T = 4530 \left(\frac{\Phi}{S}\right) \tag{B-47a}$$

$$T_C = 31 \cdot 16T = 7410 \left(\frac{\Phi}{S}\right) \tag{B-47b}$$

and the total acquisition time for the three components is

$$\tau = T_A + T_B + T_C = 13350 \left(\frac{\Phi}{S}\right) \tag{B-48}$$

The code power-to-noise spectral density ratio (S/Φ) is related to the received power-to-noise spectral density ratio by the modulation index of the code on the carrier. For biphase modulation

$$\frac{S}{\Phi} = \frac{C \sin^2\beta}{\Phi} \tag{B-49}$$

where

β = code modulation index

The power requirements for the carrier loop are the same as before; so by Equation (B-20c)

$$\frac{CM_c}{\Phi} = \frac{C \cos^2 \beta}{\Phi} \quad 27 \text{ db} \tag{B-50}$$

The modulation index β is chosen so as to satisfy both the carrier and PRN code power requirements represented by Equations (B-49) and (B-50). However, the maximum index that should be used is 1.25 radians as the carrier component becomes unstable or uncontrollable for indices above 1.25 radians. This instability results since small changes in β in this region cause large changes in the carrier component level. At 1.57 radians the carrier component is completely suppressed. Using the above results the PRN code acquisition time which includes the clock loop acquisition time, is plotted in Figure 5 as a function of the received signal-power-to-noise spectral density ratio C/Φ. The dotted curve represents the total acquisition time which includes the RF carrier acquisition given in Figure 1.

3.1.4.2 <u>BINOR Code</u>

A binary code sequence has been developed which both reduces the acquisition time of the PRN sequence and results in much simpler range acquisition circuitry in the receiver. The code is equivalent to a fixed tones system with a near optimum tone ratio of two.* The range acquisition circuitry is moreover simplified by the use of digital techniques in place of the analog filtering requirements of the tone system.

The code sequence is generated from a series of n coherent square waves which are harmonically related by multiples of two. That is, the frequency of each square wave is given by the following relationship:

$$\text{square wave frequency} = \frac{2^{i-1}}{T} \tag{B-51}$$

where

$$i = 1, 2, 3, \ldots, n$$
$$T = \text{code period}$$

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*See section on fixed tones for discussion of optimum tone ratio.

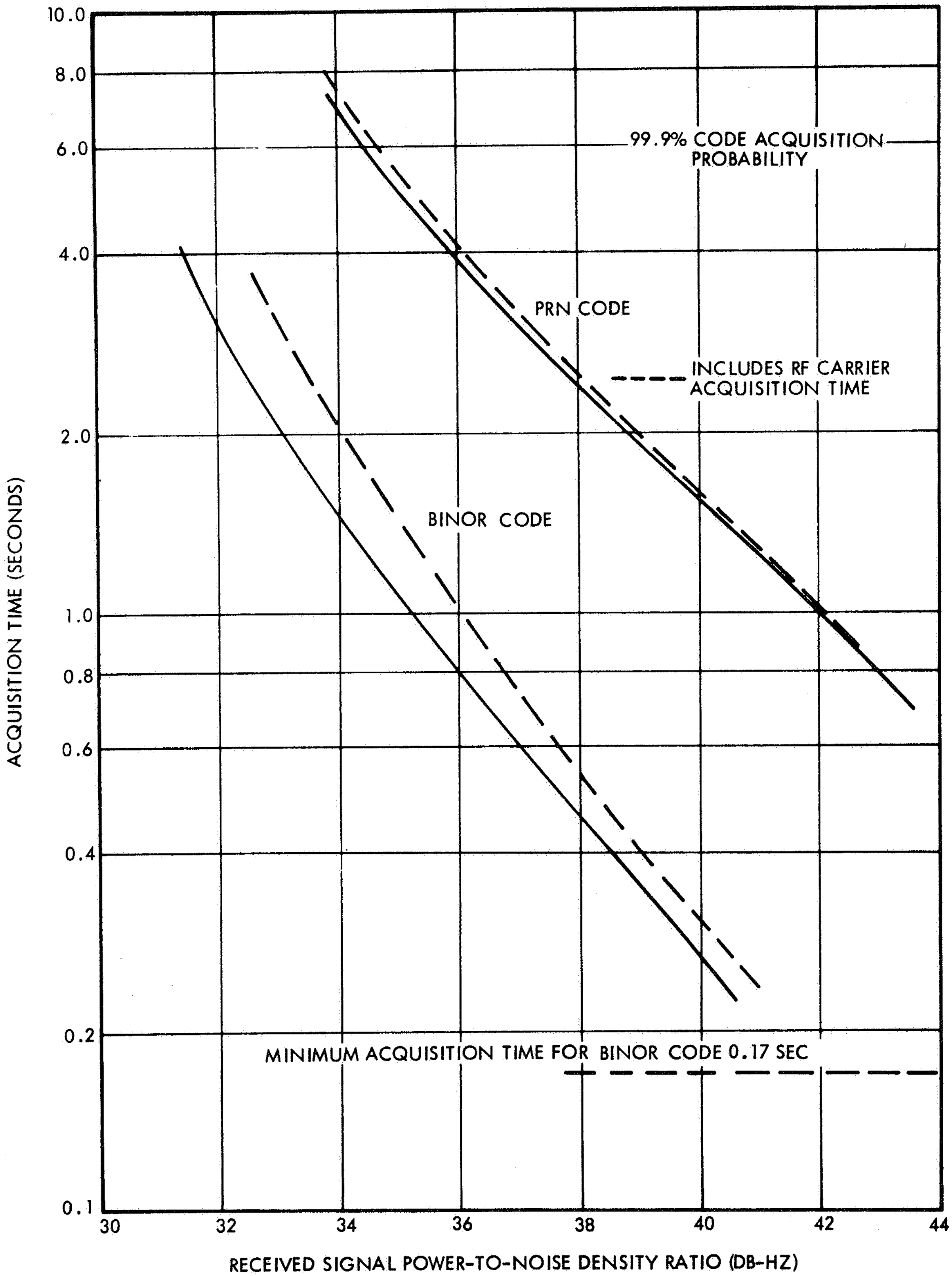

Figure 5. Acquisition Time versus Received Signal Power-to-Noise Spectral Density Ratio for Two Digital Code Systems

The binary code is generated from the square waves by the following rule. During each bit time of the highest frequency square wave or clock the number of square waves in binary state zero are subtracted from the number of square waves in binary state one. If the result of this subtraction is negative the code is put in binary state zero and if the result is zero (possible only when n is even) or positive the code is put in binary state one. Therefore, the code bit rate is equal to twice the highest square wave frequency (the clock) and the code period is equal to the period of the lowest frequency square wave.

The acquisition procedure for the code consists of first acquiring the clock component with a phase lock loop as for the PRN code followed by n-1 correlations in sequence of the code with n-1 square waves from a divide down chain of flip-flops driven from the acquired clock. Each correlation will be positive or negative depending on whether the square wave is in-phase or out of phase with the code. Therefore, a total of n binary decisions (including the clock acquisition as one binary decision) are required to resolve the phase of a 2^n bit long code. From information theory this equals the minimum number of binary decisions possible since a 2^n-bit code contains n bits of information. Consequently the code lends itself to rapid acquisition and with each acquisition step involving only a binary decision, the mechanization of the code acquisition is considerably simplified. The clock or highest frequency square wave will be 320 kHz as before and the lowest frequency square wave will be 78.125 Hz. Therefore n is equal to thirteen and the code length is 2^{13} or 8192 bits compared to 8246 bits for the PRN code. After n binary decisions or correlations the 78.125 Hz square wave will be in-phase with the received code. The range is obtained by measuring the phase of this square wave and the ambiguity resolution is equal to the period of the square wave or about 2100 n mi. The range accuracy is determined by the phase jitter in the clock loop since this jitter appears on the 78.125 Hz square wave through the divide down flip-flop chain. The clock loop SNR must therefore be 21 db prior to the phase measurement.

The correlation of each of the square waves with the code has been derived by Stiffler and the results are repeated here

$$\rho = \frac{1}{2^{n-1}} \binom{n-1}{\frac{n-1}{2}} \quad n \text{ odd} \tag{B-52}$$

$$= \frac{1}{2^{n}} \binom{n}{\frac{n}{2}} \quad n \text{ even} \tag{B-53}$$

For large n, by Stirling's formula

$$\rho \simeq \sqrt{\frac{2}{\pi n}} \tag{B-54}$$

With each of the n square waves containing $1/n$ of the total power it can be seen that the correlation is reduced by $\sqrt{2/\pi}$ from the case where the received signal is the sum of the square waves. This signal is an n-ary wave with n amplitude levels. Hence, the penalty for replacing the n-ary wave with the binary code is 2.0 db when n is large. For n equal to 13 the correlation is 0.225 (22.5 percent) and the penalty is 1.8 db.

The code acquisition time is derived as follows. The acquisition time equals the clock loop acquisition time plus 12 correlation times in sequence for the remaining 12 square waves. The clock loop acquisition time is derived the same way as for the PRN code. For acquisition purposes the clock loop SNR can be 10 db. The 21 db necessary for the range accuracy is obtained by transmitting pure clock following acquisition of the code. This increases the clock correlation factor from 22.5 to 100 percent or 13 db and actually increases the loop SNR from 10 to 23 db (ignoring loop bandwidth expansion effects). Therefore the code transmission will consist of the code sequence for a length of time to allow for acquisition followed by pure clock or the 320 kHz square wave for a short period. This increases the overall acquisition time slightly and to account for this 13 correlation times will be assumed in place of the necessary 12. The clock loop acquisition bandwidth is then given by

$$\frac{S\rho^2}{\Phi B_N} = 10 \text{ db} \tag{B-55}$$

where

S/Φ = ratio of power in code-to-receiver noise spectral density

ρ = clock correlation (22.5%)

Deriving B_N from Equation (B-55), the loop acquisition time is given in Figure 2.

The correlation time for each square wave is derived as follows. The probability of a correct binary decision for matched filter correlation is equal to

$$P_c = \frac{1}{\sqrt{2\pi\sigma}} \int_o^\infty e^{-\frac{(x-\mu)^2}{2\sigma^2}} dx = \frac{1}{2}\left(1 + \operatorname{erf} \frac{u}{\sqrt{2\sigma}}\right) \tag{B-56}$$

where

μ = correlator output level = $\rho\tau\sqrt{S}$

σ^2 = correlator output noise power = $\frac{\Phi\tau}{2}$

τ = correlation time

The probability of correct code acquisition is simply

$$\left(P_c\right)_T = \left(P_c\right)^{12} = \left(1 - P_e\right)^{12} \approx 1 - 12\, P_e \tag{B-57}$$

where

$$P_e = 1 - P_c = \frac{1}{2}\left(1 - \operatorname{erf} \frac{u}{\sqrt{2\sigma}}\right)$$

For $\left(P_c\right)_T$ equal to 99.9 percent, the corresponding value for $\frac{u}{\sqrt{2\sigma}}$ is 2.66 and therefore the correlation time* is equal to

$$\tau = 140.5\left(\frac{\Phi}{S}\right) \tag{B-58}$$

For 13 correlations

$$\tau_T = 13(140.5)\left(\frac{\Phi}{S}\right) = 1830\left(\frac{\Phi}{S}\right) \tag{B-59}$$

*The correlation time actually must be an integer multiple of the code period of 1/78.125 seconds in order to obtain the correct correlation value.

Using Equation (B-59) and the clock loop acquisition time, the overall acquisition time for the BINOR code is plotted in Figure 5 as a function of the received signal power-to-noise spectral density ratio.* The division of power between the carrier and the code, given by the carrier modulation index β , is also represented by Equations (B-49) and (B-50) and the same considerations on β also apply here.

A comparison between the two digital code schemes, represented by plots in Figure 5, shows the superiority of the BINOR code. For a 35.7 db-Hz value for C/Φ (6 db margin over the Table 1 power budget) the PRN code acquisition time is 4.5 seconds and the BINOR code acquisition time is 1.15 seconds. Therefore not only does the BINOR code result in a simpler acquisition procedure than the PRN code but in a faster acquisition time. Further details on the BINOR code ranging system including block diagrams of the code transmitter and code acquisition and range measurement circuitry are given in the reference.[11]

A different method of transmitting the BINOR code results in even faster acquisition of the code. Instead of transmitting the complete code consisting of the 13 squarewave frequencies, the code is transmitted in segments consisting of the clock and two of the square waves during each segment.** The code transmission sequence in time will have the following format.

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*Since the correlation times are restricted to integer multiples of the code period; the acquisition time plot is actually not a smooth curve as shown in Figure 6, but is stair step in shape. The minimum acquisition time is 13 times the code period or 0.17 seconds.

**Transmitting the clock plus one-square wave during each segment results in an unsymmetrical code sequence, i.e., more ones than zeros, resulting in DC level problems in the receiver. This unsymmetry results for any sequence with an even number of square wave components. Therefore the code segments are transmitted with the clock plus two square waves to get around this problem.

1. Clock square wave

2. Clock + $\frac{\text{clock}}{2}$ + $\frac{\text{clock}}{2^2}$ code sequence

3. Clock + $\frac{\text{clock}}{2^3}$ + $\frac{\text{clock}}{2^4}$ code sequence

. . .

. . .

. . .

7. Clock + $\frac{\text{clock}}{2^{11}}$ + $\frac{\text{clock}}{2^{12}}$ code sequence

8. Clock square wave

The correlation ρ for the BINOR code with three squarewave components is 0.5 [from Equation (B-52)] compared to 0.225 for the complete 13 square-wave code. Hence each correlation time can be shorter using the above transmission sequence. The code sequence during each of the transmission periods two through seven above is derived by the majority logic shown below

$$(\text{code})_n = AB_n + AC_{n+1} + B_nC_{n+1} \tag{B-60}$$

where

$$A = \text{clock square wave}$$

$$B_n = \frac{\text{clock}}{2^{2n-3}} \text{ square wave}$$

$$C_{n+1} = \frac{\text{clock}}{2^{2n-2}} \text{ square wave}$$

n = 2, 3, 4, ..., 7 (represents period in transmission sequence)

Clock only is transmitted during period one to allow the clock loop to acquire. Clock only is also transmitted at the end of the sequence (period 8) for the same reasons as previously discussed.

With ρ equal to 0.5, the correlation time is reduced from that of Equation (B-58) to

$$\tau = 28.2 \left(\frac{\Phi}{S}\right) \tag{B-61}$$

The minimum possible correlation time is equal to one period of the code sequence which for the code segment generated during period 7 is 1/78.125 seconds. To simplify timing requirements in the receiver, this value will be the correlation time used in the receiver for all the code segments two through seven. From Equation (B-61) the required value of S/Φ is 33.4 db-Hz. The corresponding code acquisition time which includes clock only during period 8 will be (assuming one code period at the end for the clock only transmission).

$$\tau_T = \frac{13}{78.125} \approx 0.17 \text{ seconds} \qquad \text{(B-62)}$$

and is equal to the minimum acquisition time as shown in Figure 5 for the 13 square wave BINOR code. This minimum acquisition time is however obtained with a much smaller S/Φ requirement.

Since full power is placed in the clock both at the beginning and at the end of the transmission sequence the clock loop SNR must be 21 db. With S/Φ equal to 33.4 db-Hz, the clock loop noise bandwidth must be 17.5 Hz which from Figure 2 results in a loop acquisition time of 0.25 second. The carrier modulation index of the code must be 1.12 radians or less to insure proper power in the carrier [see Equation (B-20c)] and therefore C/Φ (for S/Φ equal to 33.4 db-Hz) equals 34.3 db-Hz. From Figure 1, the resultant carrier acquisition time is 0.55 second. Therefore, the total acquisition time for C/Φ equal to 34.3 db-Hz is equal to

carrier acquisition	0.55 second
clock acquisition	0.25 second
code acquisition	0.17 second
Total	0.97 second

This value compares to 1.9 seconds for the full BINOR code as given in Figure 5. For C/Φ equal to 35.7 db-Hz the code acquisition time will still be 0.17 seconds but the clock loop bandwidth can be increased to 25 Hz reducing clock acquisition time to 0.17 second and the carrier loop acquisition time decreases to 0.3 second. Therefore, the total acquisition time is 0.64 second compared to 0.9 second for the full code. The disadvantage of the segmented method of transmitting the code is the resultant synchronization problems in the receiver. Since a given squarewave component is present in only a small portion of the transmitted sequence, correlation in the receiver must be accomplished at the proper time in the sequence. Hence the resultant synchronization problem for which at this writing no easy solution has been found.

3.2 Pulse Techniques

Pulse techniques have a distinct advantage over the CW techniques in that acquisition of a carrier is not required. The pulse receiver is non-coherent and simply detects the presence of a pulse. The time of occurrence of the pulse is the measure of the range. A disadvantage of pulse systems is the high peak powers required for the transmitter since the total signal energy occurs in a short duration pulse rather than being uniformly distributed over the entire transmission time as in CW systems. Of course, this concentration of energy in a short time significantly shortens the range acquisition time. The fix rate for a pulse system is limited by the PRF (pulse repetition frequency) which is a function of the range ambiguity resolution; while for CW techniques the fix rate is limited by the carrier and range signal acquisition time which is considerably longer. The PRF to obtain the same range ambiguity as was used for the CW systems is 78.125 pulses per second. Two pulses are needed for a range measurement since pulse coincidence detection will be used in the receiver to decrease the false alarm probability. Therefore, the range acquisition time is the time between adjacent pulses or less than 0.1 second.

Pure rectangular pulse systems are not practical for the Navsat as the peak powers in the satellite become excessive at L-band hundreds of kilowatts). Consequently a pulse compression system is needed to reduce the peak power requirements to reasonable levels. Details of the design of the pulse compression system have been covered in two separate documents [12] so will not be repeated here. A summary of the system parameters is given as follows:

Peak transmitter power = 20 kw

Average transmitter power = 31 W (during satellite transmission)

Signal = 20 μs chirp pulse (5.0 MHz frequency sweep)

PRF = 78.125 pulses per second

Compression ratio = 100

 Probability of pulse detection = 0.985

False alarm time = 55 hours

Acquisition time = 0.1 second

RF bandwidth = 5.0 MHz

The specified transmitter powers allow for a 6 db margin and assume the same RF link parameters as for the CW systems (Table 2). The probability of pulse detection (using two pulse coincidence detection) is 0.985. This compares to the probability of acquisition for the CW systems of better than 0.9 for the carrier and 0.999 for the range signal. The false alarm time is unique to the pulse system as the receiver is continuously open and occasionally will mistake noise for a pulse. With two pulse coincidence detection this type mistake will occur on the average of only once every 55 hours. Without coincidence detection the probability of detection increases to 0.993 but the false alarm time is a very undesirable 0.2 second.

4. MULTIPATH ERROR REDUCTION TECHNIQUES

The reception of multipath signals at the user antenna tend to degrade the range measurement accuracy of the ranging system. Studies[13] of the problem have indicated that the accuracy with multipath reception is related to the RF bandwidth of the ranging signal. Consequently modulation techniques or signal designs which increase the RF bandwidth should be less susceptible to range measurement errors in the presence of multipath signal reception.

The digital code systems should be less susceptible to multipath errors if the clock frequency is increased. This increases the bandwidth of the signal and increases the fine range measurement accuracy of the clock phase. However, the increased clock frequency also increases the length of the code if the same range ambiguity resolution is desired. As a result the code acquisition time is also increased. For example with the BINOR code if the clock frequency is increased from 320 kHz to 1.28 MHz, a factor of four, the square wave correlations required to acquire the code increase from 13 to 15. In addition the square wave and clock correlations decrease from 22.5 to 21 percent and the maximum initial frequency offset for the clock loop increases by a factor of four from 1.3 Hz to 5.2 Hz. Computation of the code acquisition time for a received signal power-to-noise spectral density ratio of 35.7 db-Hz shows that it increases from 0.88 second (Figure 5) to 1.37 seconds. The carrier acquisition time of 0.3 seconds does not change. Using the segmented BINOR code transmission technique, the code acquisition time simply increases by two code periods or 2/78.125 seconds. The clock acquisition (with 25Hz loop bandwidth) increases from 0.17 to 0.24 seconds with the increased frequency offset of 5.2 Hz. Therefore, with C/Φ equal to 35.7 db-Hz, the total acquisition time goes from 0.64 second to about 0.74 second. Therefore with the segmented code transmission, acquisition time does not increase significantly.

The fixed and swept tone systems should also be made less susceptible to multipath errors by increasing the frequency of the fine range or accuracy tone. For the fixed tones system this would require one additional tone and the acquisition time would increase due to an increase in the top tone initial frequency error for the higher frequency.

An additional technique for reducing the susceptibility of the fixed tones system to multipath errors is to increase the individual tone modulation indices to large values. Indices as high as 6 to 10 radians may be necessary.[14] The large indices also increase the RF bandwidth. For example using modulation indices of 8 radians for each tone the fixed tones system RF bandwidth increases from about 700 kHz to about 5.5 MHz. With large indices the tone powers are spread out over many sideband components and the carrier component is reduced to a low level. Therefore, modulation feedback is required in the receiver to reduce the indices and restore power in the carrier. The feedback is implemented by the use of five tone tracking loops which feed the five demodulated range tones back to the receiver where they phase modulate the carrier loop VCO and reduce the incoming signal modulation indices to a small value. For tone modulation indices of 8.0 radians each and a tone feedback loop gain of 30 db the modulation indices are reduced to 0.25 radian. The acquisition time for the feedback receiver and corresponding required received signal-to-noise density ratio is estimated as follows. The feedback loops as well as providing modulation index reduction, also provide phase stability around the receiver and should thus be operated in a linear region. Assuming that a SNR of 10 db is adequate for linear loop operation, the received power requirements should be

$$\frac{C}{\Phi\left(2B_L + B_t\right)} = 10 \text{ db} \qquad \text{(B-63)}$$

where

$2B_L$ = carrier loop noise bandwidth (50 Hz)

B_t = sum of the five tone loop bandwidths

The sum of the tone loop bandwidths assuming they are equal is[15]

$$B_t = 5\left[2\left(\frac{\beta_i}{\beta_o}\right) B'_t\right] \qquad \text{(B-64)}$$

where

$$\frac{\beta_i}{\beta_o} = \text{ratio of input tone modulation index to IF modulation index or equivalently the loop voltage gain}$$

B'_t = open loop filter bandwidth of each tone loop

Assuming 30 db for β_i/β_o or 31.8 and 2 Hz for the open loop bandwidth, the value for B_t is 636 Hz. The value for C/Φ from Equation (B-63) becomes 38.4 db-Hz. The corresponding acquisition time is derived as follows. The carrier acquisition will be the same and from Figure 1 is about 0.1 second. The tone loop acquisition procedure is as follows. After carrier acquisition, the five range tones are modulated onto the carrier at deviations of 0.8 radian each. This permits sufficient power to remain in the carrier to keep the carrier loop in lock. Since the open loop tone filter bandwidths are 2 Hz each the filter acquisition time is 0.5 second [see Equation (B-17)] and the tone loops should acquire in about 0.5 second. Therefore the tone modulation indices will be left at 0.8 radian for 0.5 second and then will be linearly increased to the final value of 8.0 radian in 0.1 second.

From previous results it was noted that the required tone SNR's are 21 db. Hence additional filtering of the tones is required after the tone loops. The individual tone loop bandwidths are twice 31.8 times the 2 Hz open loop bandwidth or 127.2 Hz. Since the specified tone loop SNR's were 10 db, to obtain a final SNR of 21 db the filter noise bandwidth after the tone loop must be about 10 Hz. Assuming a phase tracking filter for the top tone, from Figure 2 the acquisition time for this filter should be 0.5 second. Consequently the total acquisition time for the tones feedback receiver at a received signal power-to-noise spectral density ratio of 38.4 db-Hz is equal to

RF Carrier Acquisition	0.1 second
Tone Loops Acquisition	0.5 second
Final Filter Acquisition	0.5 second
Total	1.1 seconds

The acquisition time for the low deviation PM fixed tones system at the same power level is also about 1.1 seconds (see Figure 3). Therefore the high deviation PM feedback receiver does not compromise performance.

The penalty for the reduced multipath error sensitivity is a more complicated receiver design and transmitted signal structure.

The pulse compression system is perhaps the least vulnerable to multipath. By using gating logic in the receiver, reflected path pulses which arrive at the receiver after the direct path pulse can usually be blocked from the range measurement circuitry. Multipath becomes a problem only when the propagation time difference between the direct path and the reflected path is equal to or less than the compressed pulse length. For the pulse compression system this time is 1/100 of the 20 μsec chirp pulse or 200 nanoseconds.

5. DATA TRANSMISSION

In addition to range difference measurements the user requires information on satellite identification and on corrections to satellite ephemeris and clock phase. This information plus time of day is broadcast to the user by the satellites in the form of PCM data and is transmitted on the same RF carrier as the ranging signal. Therefore, some form of multiplexing the two signals is required. The number of bits required to transmit the above information has been estimated to be about 130. This total includes simple error coding plus some initial non-information bits at the start to provide for bit synchronization. A bit error probability of 10^{-3} should be sufficient for the data transmission. The bit transmission rate will depend on the form of multiplexing and the number of bits transmitted during a satellite broadcast. It will be assumed that all 130 bits are transmitted during one satellite broadcast.

Two forms of multiplexing will be investigated. These are frequency division multiplexing (FDM) where both signals appear on the carrier simultaneously and time division multiplexing (TDM) where the two signals occur in time sequence.

5.1 DATA TRANSMISSION WITH CW RANGING

The PCM data is transmitted on a subcarrier with either multiplexing technique. With frequency multiplexing the subcarrier is located in a non-interferring portion of the range signal frequency spectrum and with time multiplexing the subcarrier is placed at a frequency which is sufficient to remove the data sidebands from the 50 Hz carrier loop.* The PCM data biphase modulates the subcarrier and the subcarrier demodulator uses coherent detection with matched filtering of the PCM data. This technique is the most optimum from a power efficiency standpoint. Other non-coherent schemes can allow for simpler subcarrier demodulator designs

*With large data rates and TDM (500 bits per second or greater) split-phase coding may be used to modulate the data directly on the carrier. This results in slightly better power utilization than the use of a subcarrier. The following discussion however will assume use of a subcarrier for the data.

but result in excessive power demands on the transmission link and for this reason are not considered here. Since the subcarrier demodulator will be a small portion of the overall user equipment costs the necessity for minimizing the demodulator design is not of paramount importance.

A major problem in the data transmission design is the provision for data bit sync in the demodulator. Bit sync can either be derived in the demodulator from the data stream or can be transmitted along with the data. For the present bit sync will be assumed to be derived in the demodulator by a bit synchronizer operating on the data stream. Transmission of bit sync with the data will be discussed briefly later.

Coherent detection of the data requires knowledge of the unmodulated subcarrier phase for the reference signal. This reference can be obtained either by leaving some power in the subcarrier frequency after data modulation or by deriving the subcarrier phase from the data modulation sidebands. This latter technique is preferable since no power is wasted in the subcarrier itself but is completely in the data sidebands. In addition leaving power in the subcarrier necessitates the use of split-phase PCM modulation in order to place the data sidebands sufficiently far from the subcarrier to allow acquisition and tracking of the subcarrier phase by a phase-lock loop.

The subcarrier phase is obtained from the data sidebands by a squaring loop. The biphase modulated (±90 deg) subcarrier is filtered by a bandpass filter W Hz wide and then squared. The resulting double frequency term is then filtered by means of a phase-lock filter whose VCO output is divided by two and used as the subcarrier phase reference.* The output of the phase detector is the noisy PCM data stream. Matched filtering of the data and bit synchronization are accomplished by a bit synchronizer loop following the phase detector.

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*The divide by two creates an ambiguity of 180 degree in the reference phase and hence in the PCM data. This ambiguity can be resolved by differential encoding of the data or by initially transmitting a few bits of known polarity.

The performance of the square loop demodulator has been analyzed by Lindsey.[16] The results indicate that for the parameter $\delta > 5$ the demodulator performance is near that of perfect coherent PCM/PSK detection. The parameter δ is given by

$$\delta = \frac{2H}{B_N}\left(1 + \frac{\Phi W}{2S}\right)^{-1} \tag{B-65}$$

where

H = data bit rate

B_N = double frequency phase-lock loop noise bandwidth

W = input subcarrier bandpass filter noise bandwidth

S/Φ = subcarrier signal-power-to-noise spectral density ratio

The bandwidth W must be wide enough to pass the modulated subcarrier without serious distortion. A bandwidth sufficiently wide to accomplish this objective is equal to three times the bit rate. Equation (B-65) then is equal to

$$\delta = \frac{2H}{B_N}\left[1 + \left(\frac{3}{2}\ \frac{\Phi H}{S}\right)\right]^{-1} \tag{B-66}$$

For a 10^{-3} bit error rate, $S/\Phi H$ ideally is equal to 6.8 db. However, due to non-ideal hardware implications a value of 8.0 db is more realistic in any actual demodulator implementation. Consequently for $\delta > 5$ the phase-lock loop bandwidth must be related to the bit rate by

$$B_N < \frac{H}{3.1} \tag{B-67}$$

Knowing the bandwidth B_N, the loop acquisition time can again be found from Figure 2 and is the acquisition time for the subcarrier demodulator.

With frequency division multiplexing, the time available for data reception is the range signal acquisition time less the subcarrier demodulator acquisition time. For example, given a range signal acquisition time of one second the data rate must be greater than 130 bits per second to receive all 130 bits of information. Assuming a data rate of 150 bits per sec the loop bandwidth B_N will be 48 Hz and the acquisition time will be approximately 0.1 second.* The time available for data transmission is then 0.9 second during which time bits can be received. The corresponding data subcarrier power requirement is

$$\frac{S}{\Phi} = 8.0 + 10 \log 150 = 29.8 \text{ db-Hz} \tag{B-68}$$

Since the data subcarrier is present simultaneously with the range signal additional signal power at the receiver is necessary. With a subcarrier modulation index of β radians on the carrier the modulation losses for the carrier and range signal increase by the factor $J_o^2(\beta)$. An optimum set of modulation indices for the range and the data subcarrier can be found in the same manner as was previously found for the range signal by itself. Table 5 gives a summary of the effect of the data transmission on the three CW ranging systems. Adding the data transmission function increases the received power requirements by 1.3 db for the fixed tone system and 3.5 db for the BINOR code system over that for ranging only when the received signal power-to-noise spectral density (C/Φ) is 3.5 db-Hz. The higher extra power required with the BINOR code is primarily due to the higher data rate necessary which itself is due to the shorter range acquisition time for the code compared to the tone ranging. For both tone systems the subcarrier frequency can be placed at 3 kHz but for the BINOR code the subcarrier is placed at 1.7 MHz which is outside the code bandwidth extending from 78 Hz to 1.6 MHz (5th harmonic of clock).

With time division multiplexing additional received power is not necessary but the total acquisition time which now includes data acquisition will increase. The total power for ranging is also available for data

*Assuming initial frequency error of zero for 3 kHz subcarrier frequency.

reception since the two transmissions occur in time sequence. For a given C/Φ, the data rate H can be calculated as follows. The power required in the subcarrier is

$$\left(\frac{CM_d}{\Phi}\right)_{db\text{-}Hz} = 8 + 10 \log H \qquad \text{(B-69)}$$

where

$M_d = 2J_1^{\,2}(\beta)$ = modulation loss for the subcarrier

β = subcarrier modulation index on carrier

TABLE 5

EFFECT OF MULTIPLEXING RANGE AND DATA SIGNALS FOR THREE CW RANGING SYSTEMS

System	Required C/Φ (db-Hz)	Data Rate (bits/sec)	Subcarrier Frequency	Total Acq. Time (sec)
Fixed Tones	35.7	0	---	2.9
Plus FDM-Data	37.0	60	3 kHz	2.9
Plus TDM-Data	35.7	400	3 kHz	3.3
Swept Tone	35.7	0	---	4.5
Plus FDM-Data	36.8	40	3 kHz	4.5
Plus TDM-Data	35.7	400	3 kHz	4.9
BINOR Code	35.7	0	---	1.2
Plus FDM-Data	39.2	160	1.7 MHz	1.2
Plus TDM-Data	35.7	400	3 kHz	1.6

The power required in the carrier is still given by Equation (B-20c) where M_c is equal to $J_o^{\,2}(\beta)$. For example, given a C/Φ of 35.7 db-Hz the optimum modulation index* is 1.75 radians and M_d is -1.7 db. Using Equation (B-69) the data rate H is 400 bits per second. At this rate 130 bits requires

*The optimum index places maximum power in the data subcarrier while till insuring sufficient power in the carrier.

0.325 seconds of data transmission. The squaring loop bandwidth will be 130 Hz and the corresponding acquisition time will be less than 0.1 second. Consequently the overall acquisition time is increased about 0.4 seconds from that for ranging only at a C/Φ of 35.7 db-Hz. For other values of C/Φ the data rate will be different and therefore the data acquisition time will be different. Table 5 also summarizes the effect of time division multiplexing for the three CW systems.

In order to compare the two multiplexing schemes, plots of the total acquisition time for the range and data were made using the BINOR code ranging technique as a function of C/Φ. The plots for both multiplexing methods are shown in Figure 6 and clearly demonstrate the superiority of time division multiplexing. For instance at C/Φ equal to 35.7 db-Hz the acquisition time for FDM is 3.1 seconds while for TDM it is only 1.5 seconds. A similar advantage for TDM also applies with the tone systems.

In the above discussion bit sync was derived by a bit synchronizer loop following the demodulator phase detector. An alternative is to transmit the bit sync timing simultaneously with the data. This eliminates the necessity for the bit synchronizer loop but additional power is required for the bit sync waveform and some form of bit sync detection circuitry is required in place of the bit synchronizer loop. Two ways to transmit bit sync suggest themselves. A tone equal to the bit rate frequency can either directly modulate the carrier or can AM the subcarrier. In the TDM system the bit rate is large enough so that the sync tone will not interfere with the RF carrier loop and since ranging is not present during data transmission the sync tone also cannot interfere with the ranging signal. In FDM if interference with the carrier loop or ranging is a problem the sync tone can AM the subcarrier or a tone spaced the bit rate frequency from the subcarrier frequency can be used and the bit sync derived from the beat frequency between the two. This tone will not interfere with the subcarrier data as it will be located in a null of the subcarrier frequency spectrum.

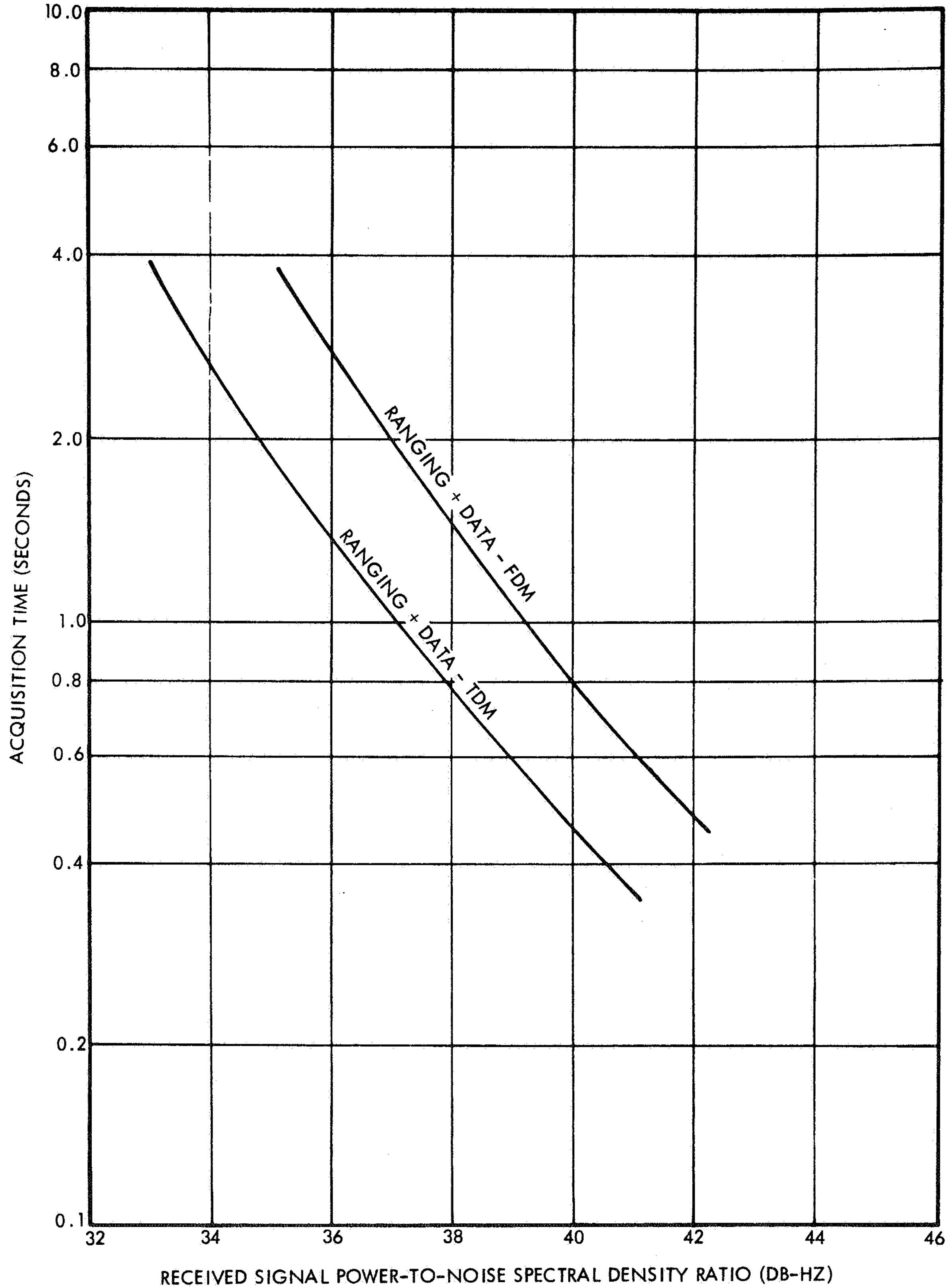

Figure 6. Acquisition Time for BINOR Code Ranging and PCM Data versus Received Signal Power-to-Noise Spectral Density Ratio

As the TDM system is the one of interest, the effect of bit sync transmission on the power requirements will be investigated further for this system. For a bit rate of 400 bits per second the sync tone used will be a 400 Hz tone directly phase modulating the RF carrier. The sync tone is detected in the subcarrier demodulator by a bandpass filter centered at 400 Hz and a zero crossing detector. The power required in the sync tone is determined by the SNR necessary at the tone filter output. For a SNR of 10 db and a filter bandwidth of 10 Hz* the sync tone power requirement is

$$\frac{CM_t}{\Phi} = 10 \text{ db} + 10 \log 10 = 20 \text{ db} \tag{B-70}$$

where

$$M_t = 2J_1^{\ 2}(\beta_t)\, J_o^{\ 2}(\beta_d) = \text{sync tone modulation loss}$$

$$\beta_t = \text{sync tone modulation index}$$

$$\beta_d = \text{data subcarrier modulation index}$$

The subcarrier power requirement for 400 bits per second of data is from Equation (B-69)

$$\frac{CM_s}{\Phi} = 34.0 \text{ db}$$

where

$$M_s = 2J_1^{\ 2}(\beta_d)\, J_o^{\ 2}(\beta_t)$$

Again picking an optimum set of indices the required value for C/Φ is 36.4 db-Hz. This compares with 35.7 db-Hz when sync is not transmitted and hence for this particular case the sync transmission requires 0.7 db more power.

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*The sync tone acquisition time will be about 0.1 second or on the order of the subcarrier squaring loop acquisition time.

5.2 DATA TRANSMISSION WITH PULSE RANGING

Data transmission can be incorporated with the pulse compression ranging system by using the pulses themselves. Data can be transmitted by sweeping the pulse chirp frequency either up or down to differentiate between a 0 or 1 or alternatively by pulse position modulation, PPM. The data rate for the chirp frequency pulses will be equal to the PRF or 78.125 bits per second. With PPM the data rate is dependent on the number of possible pulse position positions per received pulse. For four positions per pulse the data rate is twice the PRF or 156.25 bits per second. This latter technique appears from a brief investigation to be the best method for the data transmission requirements. From the discussion of pulse compression ranging it was noted that at least two pulses are required to make a range measurement. Therefore the satellite can initially transmit two or more pulses periodic at the PRF to establish the range measurement followed by 65 PPM pulses for the 130 bits of data required.* The total number of pulses per transmission then will be 67 more and the corresponding total range and data acquisition time is about 0.86 second.

Bit sync for the data can be easily derived from the pulses. The first five or more pulses can be used to synchronize a free running multivibrator operating at the proper frequency. After sync of the multivibrator, it's phase must remain stable only over the duration of the remaining 60 or so pulses.

The SNR required for each pulse to obtain the detection and false alarm probabilities specified for the ranging function (see Section 3.2) is 14.7 db. This pulse SNR is adequate for reception of the PPM data and should provide a bit error probability of less than 10^{-5}.[17] Therefore no additional transmitter power is required to transmit the PPM data pulses following transmission of the ranging pulses. As for the CW TDM data case, the data transmission simply increases the total satellite broadcast time over that necessary for range only transmission.

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*This is analogous to TDM of the range and data with the CW systems.

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