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Quarterly Report No. 1

REDUCED GRAVITY BATTERY TEST PROGRAM

Research and Development Center
General Electric Company
Schenectady, New York

Contract Number: 952121

July 1968

Prepared for:

Jet Propulsion Laboratory
California Institute of Technology
Pasadena, California 91109

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This work was performed for the Jet Propulsion Laboratory, California Institute of Technology, as sponsored by the National Aeronautics and Space Administration under Contract NAS 7-100

FOREWORD

This report was prepared by the General Electric Company, Schenectady, New York, on J.P.L. Contract Number 952121. This contract is a subcontract under NASA Contract NAS 7-100 , Task Order No. RD-26. This contract is administered by the Jet Propulsion Laboratory, California Institute of Technology, Pasadena, California. Mr. G. L. Juvinall is the designated JPL Technical Representative for the Laboratory.

The work presented in this Quarterly Report was accomplished between February 21, 1968 and May 20, 1968. The work was performed by the Research and Development Center of the General Electric Company.

Principal contributors were: A. J. Yerman, Technical Director; Dr. W. J. van der Grinten, Senior Chemical Physicist; J. M. Holeman, Engineer--Optic Systems; S. C. Richardson, Engineer--Measurements and Instrumentation; M. D. Ketchum, Engineer--Electronic Systems; and E. Siwek, Specialist--Battery Technology.

ABSTRACT

This is the first quarterly report of JPL Contract No. 952121 with the General Electric Company Research and Development Center covering the design, construction and testing of a breadboard model of test equipment capable of investigating the behavior of secondary Ag-Zn batteries in the zero-g environment of an earth orbit. Three types of test are to be performed automatically in sequence by the equipment.

This report covers the basic experimental work carried out to define the test procedures and equipment requirements for two of these, together with a description of the control circuits to be used for programming the test sequence and recommendations covering an instrumentation tape recorder which is to be a part of the breadboard unit.

The experimental work reported on includes the results obtained with a current ramp generator which is proposed as a convenient way of obtaining polarization data on cell electrodes, and data obtained from tests of a commercial Ag-Zn battery which has been selected as a representative test specimen for one of the space experiments.

A basic approach to the control and programming of the experiments based on the use of available digital integrated circuits is described. Also, results are presented covering a survey of instrumentation tape recorders for the application, and recommendations of specific instruments are made.

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SECTION I - INTRODUCTION

As more protracted and complex space missions are planned and executed, the design of efficient and reliable energy storage systems becomes increasingly important. While much knowledge has been acquired recently as a result of intensified research and development in the area of rechargeable batteries, space use imposes special environmental factors which are not readily realizable in normal laboratory investigations. A particularly difficult one to cope with in terrestrial laboratories is the effect of low or zero gravity.

However, recent Jet Propulsion Laboratory work on smooth zinc electrodes in alkaline electrolytes has shown that gravity can have significant effects on electrode performance with wide variations in the effect resulting when the internal geometry of the cell is changed. Extrapolation of these results at one gravity and higher to sub or zero gravity conditions is revealing, but uncertainties in this procedure detract from the usefulness of such results. In view of the significance of the effects noted, it is essential that more reliable and useful information be acquired on low g effects by direct measurement. Recognition of this need has resulted in the Jet Propulsion Laboratory's interest in conducting a reduced gravity test program which is the subject of Contract Number 952121 issued by California Institute of Technology, Jet Propulsion Laboratory to the General Electric Company Research and Development Center.

Under this contract starting February 21, 1968, the Research and Development Center has taken on the responsibility of designing, fabricating, and testing a breadboard unit of a test system which is to be capable of investigating the behavior of battery cells during flight in a low or zero-g environment. The breadboard unit is to be capable of conducting three separate tests which

have been assigned task numbers which are defined as follows:

Task 1 - To measure the limiting current density of a smooth, pure zinc anode in the region of 0 to 1g, in an experiment designed to provide maximum correlation with data previously obtained by JPL over a 1-20g range.

Task 2 - To investigate the performance of battery electrodes in a special silver-zinc research cell as a function of bubble formation on the electrode surfaces.

Task 3 - To measure the electrical capacity of a secondary silver-zinc cell as a function of charge-discharge cycling in a 0 to 1 g environment as well as the limiting current capability (polarization curve).

During the first quarter of this contract, effort has been concentrated mostly on Task 1 and Task 3. Considerable experimental work has been carried out in an effort to better define these individual experiments and provide necessary information for the design of adequate test control and instrumentation systems. Concerning Task 1, the possibility has been investigated of employing a current ramp loading circuit which would increase the discharge current from the cell linearly with time up to some level at which a preset value of polarization voltage is observed. Section 1.0 of the Technical Discussion Section of this report details the initial results obtained, and the circuits used. Also covered are the initial results obtained in attempts to simulate zero gravity conditions by orienting the test cell so that convection is suppressed.

Effort on Task 3 has been directed at the definition of a testing sequence, selection of a suitable commercial cell for testing, and design and development of the control circuitry for programming the test. Results obtained to date are reported in Section 2.0. Experimental Measurements covering a Yardney

HR5-DC-7A cell which was cyclically charged and discharged 35% of its rated 5 ampere-hour capacity.

Section 3.0 of this report covers the results of an initial study of switching methods made in order to permit selection of the best approach to controlling the various tests. Based on this study the selected approach for programming Tasks 1 and 3 tests is presented in considerable detail.

Section 4.0 covers a survey of instrumentation tape recorders suitable for application to the experiments in space, and commercial instrumentation recorders which have the requisite characteristics to provide a useful substitute for tests of the breadboard. Based on the survey, recommendations are made regarding the best choice of recorder for the breadboard model.

This report does not include coverage of the Task 2 experiments. Work done to date is regarded as too preliminary in nature in contrast to the Task 1 and 3 effort where significant milestones have been reached. It is our intent to give detailed coverage of the Task 2 results in the next scheduled quarterly report.

SECTION II - TECHNICAL DISCUSSION

1.0 Task 1 - Polarization of a Smooth Zinc Anode

1.1 Technical Discussion

The objective of Task 1 can be interpreted as follows:

> The limiting current density of the smooth pure zinc anode of a silver-zinc cell is to be measured with the zinc electrode positioned in the vertical and horizontal directions. The experiment shall be designed in such a way as to provide maximum correlation data with data previously obtained by JPL and furnished as part of this contract.

The chief investigator of this JPL program was Dr. G. Myron Arcand, now at the Idaho State University, Chemistry Department. At various times during the earlier part of this contract Dr. Arcand has kindly supplied us with additional information on the JPL test setup, testing procedures and test results for the vertically positioned zinc electrode and his valuable contributions to the program is hereby gratefully acknowledged. Without this it would have been difficult to provide the "maximum correlation" specified in the Statement of Work.

Figure 1-1 gives a cross-sectional view of the JPL-Arcand cell in the vertical position. It was used to measure the effect of gravity (1 to 20-g) on the performance of the smooth zinc-electrode. Only a small part of the negative zinc-electrode (1 cm^2) is exposed to the KOH-electrolyte and the positive AgO-counter-electrode through a square opening in the mask. The zinc reference electrode shown in Figure 1-1 makes it possible to study the polarization of the zinc electrode separately.

This arrangement is very different from the one normally prevailing inside a conventional silver-zinc cell (e.g. the HR5-cell to be used for

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* JPL Space Program Summaries Vol. 5, 73-23, 73-26, and 73-30 (1966).

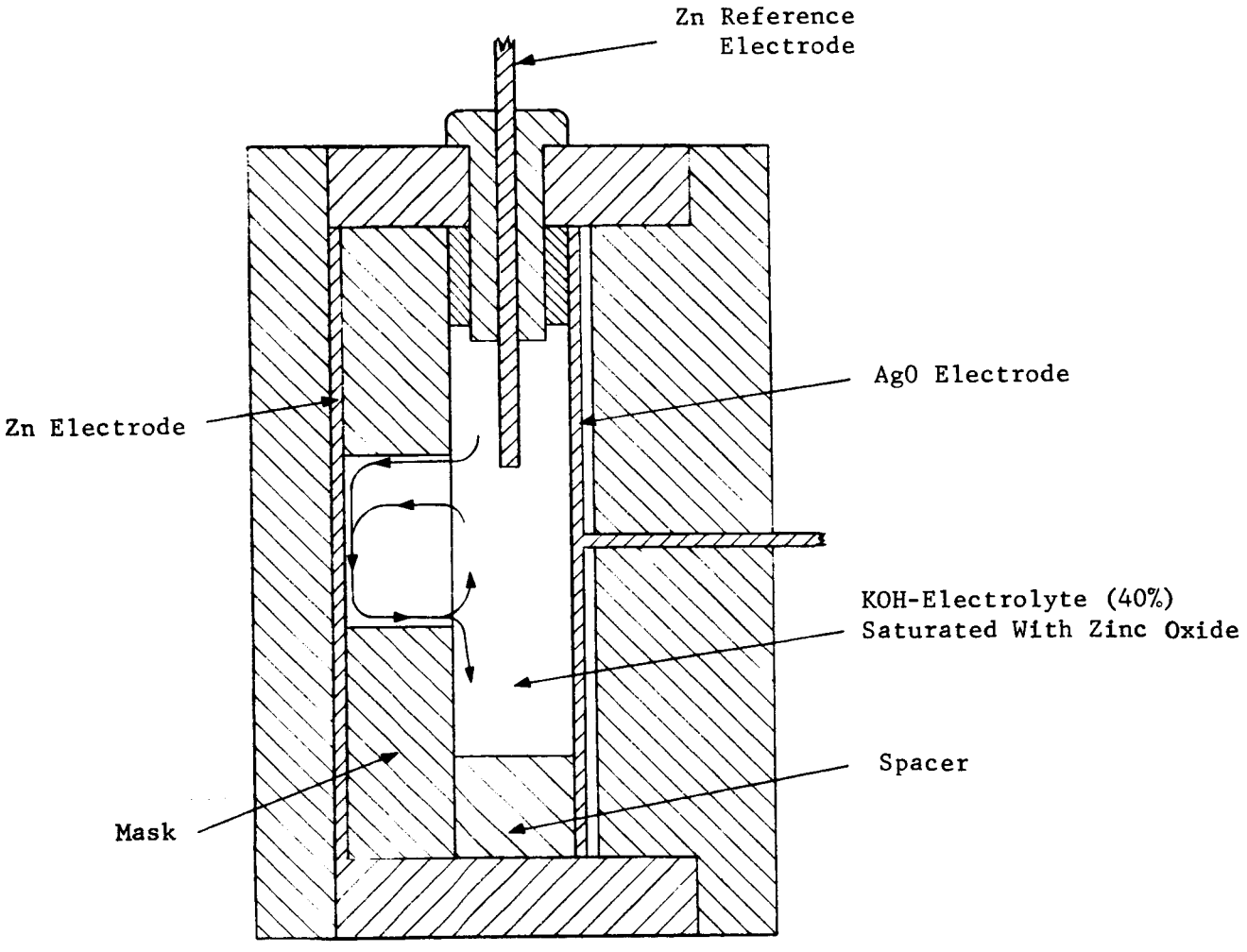

Figure 1-1 Cross-Sectional View of the JPL-Arcand Silver-Zinc Cell in the Vertical Position

Task 3). Commercial zinc-electrodes are usually of the high porosity and high surface area type whereas the one used for this task has no porosity and its true surface area at the time of passivation is not much larger than 1 cm^2. Secondly, the compact structure of a commercial silver-zinc cell leaves very little room for natural convection to occur, whereas the JPL-Arcand cell is very sensitive to convection. Such differences greatly influence the functioning of alkaline zinc electrodes because under these conditions the rate of the discharge process at the surface of the zinc electrode:

$$Zn + 2OH^- + 2KOH \longrightarrow K_2Zn(OH)_4 + 2e^- \qquad (1)$$

is controlled by the movement of the zincate $K_2Zn(OH)_4$ dissolved in the electrolyte from the zinc-electrolyte interface by liquid diffusion or convection. Likewise the g-effects measured on the JPL-Arcand cell may not be applicable to commercial cells.

Earlier, Eisenberg and coauthors* did measure simulated gravity effects on a similar silver-zinc electrode arrangement as a function of free convection. In this case, however, convection was not impaired by a mask in front of the zinc electrode. These authors also measured densities of various zincate solutions in 30% KOH, a selection of which is given in Table 1-1. From this table one can find the increase in density from 1.294 to 1.336, if the zincate is derived from solid zinc oxide (ZnO). If, on the other hand, the zincate in solution is derived from the discharge of a zinc electrode (line 3) the density of the electrolyte may increase up to 1.411. Returning now to Figure 1-1, one can easily see how the discharging zinc electrode will soon be covered by a high density liquid film, which, if

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* M. Eisenberg, H. F. Bauman, D. M. Brettner: "Gravity Field Effects on Zinc Anode Discharge in Alkaline Media", J. Electrochem. Soc., 108, 909 (1961).

Table 1-1

Densities of 30% KOH Solutions at 25°C

(M. Eisenberg, l.c.)

		gms/cm^3
(1)	No dissolved zincate	1.294
(2)	Saturated with ZnO	1.336
(3)	Anodic dissolution	up to 1.411

vertically oriented in a gravitational field, will soon slide downward as indicated, setting up free convection and returning thereby fresh unloaded electrolyte to the upper regions of the zinc electrode. This in turn retards the onset of passivation of the zinc electrode. In spite of several minor differences in experimental parameters between the Eisenberg and the JPL-Arcand test cells, the same basic reasoning can be applied also to the latter. In the horizontal zinc position with the heavy zincate layer at its lowest possible level, free convection of the electrolyte does not normally occur, leading to earlier passivation. The absence of natural convection despite density gradients is typical also of a 0-g environment in any orientation. Therefore, the horizontally oriented zinc electrode at the bottom and at 1-g can be looked upon, at least qualitatively, as a "simulation" of the 0-g environment.

Since the onset of passivation occurs rather suddenly it is necessary to approach the limiting current density (LCD) condition in small incremental steps, if reasonable accuracy is desired. Customarily these small current steps have been kept constant for a duration of one minute. Figure 1-2 illustrates such current step sequences used by Eisenberg and Arcand for measuring LCD's, while Table 1-2 summarizes some of their results. In this

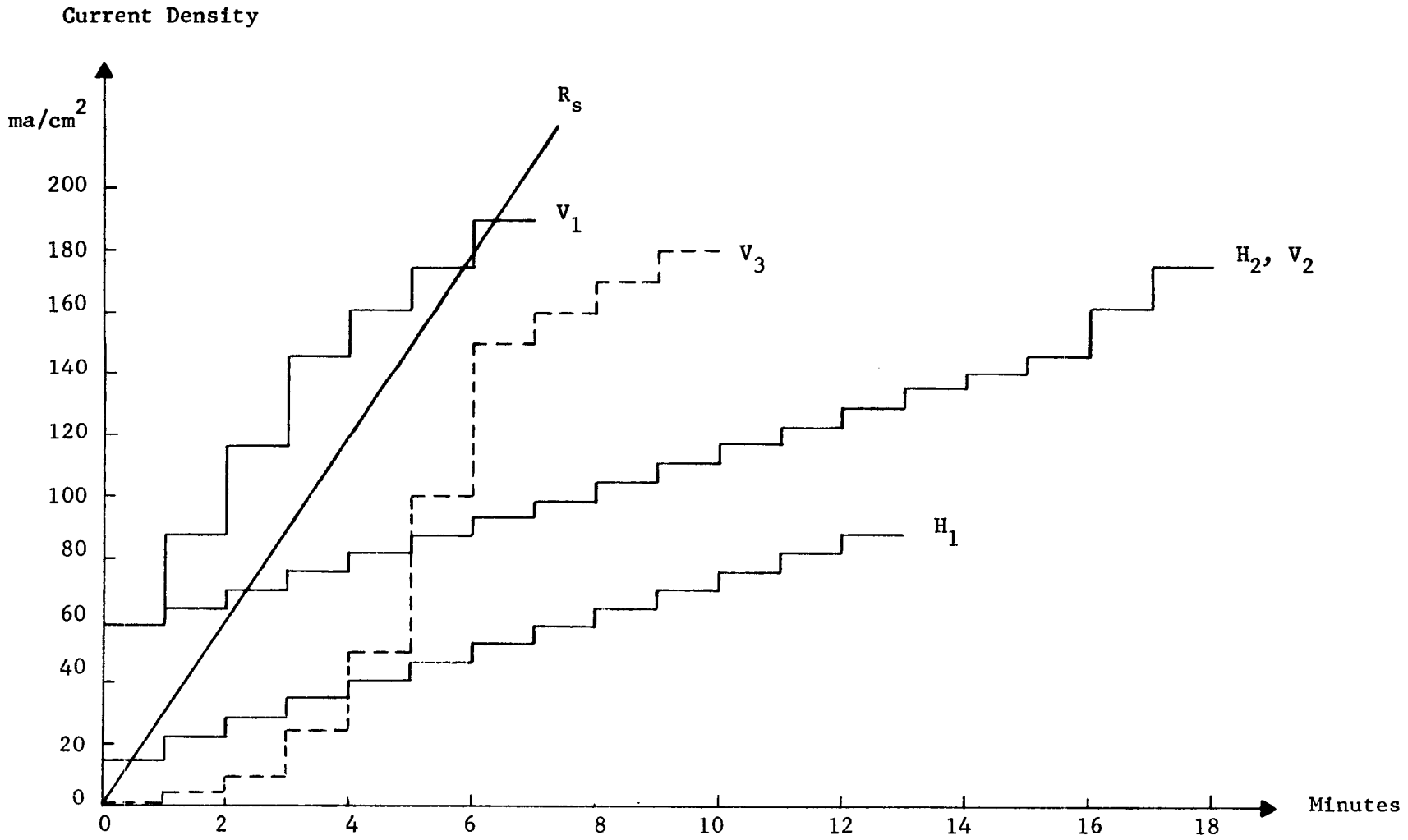

Figure 1-2 Current Step Sequence for Measuring LCD

Table 1-2

Limiting Current Densities (LCD)

Test No.	Source	Sequence (Figure 1-2)	Ramp Slope Equiv. $I_o + \Delta I/\Delta t$	LCD_{hor} $\frac{mA}{cm^2}$	C_d $\frac{mA\ min}{cm^2}$	LCD_{vert} $\frac{mA}{cm^2}$
1	Eisenberg*	H_1	$\frac{15mA}{cm^2} + \frac{5.6mA}{min\ cm^2}$	83	494	--
2	"	"	" "	90	524	--
3	"	V_1	59 + 18.5	--	495	190
4	"	"	" "	--	530	190
5	"	H_2	59 + 6.5	99	570	--
6	"	"	" "	105	736	--
7	"	V_2	" "	--	2,200	170
8	"	"	" "	--	2,235	170
9	JPL-Arcand	V_3	0 + 30	--	420	160

* All Eisenberg ramp slope equivalents were calculated, assuming the cell surface area to be 34.2 cm^2.

table the column marked "Sequence" refers back to the different current profiles given in Figure 1-2. An analysis of these profiles is given in the next column, marked "Ramp Slope Equivalent", in terms of an initial current density level I_o and an average rate of change level $\Delta I/\Delta t$. Columns marked LCD_{hor} and LCD_{vert} list the limiting current density values obtained for the horizontal and vertical zinc electrode positions. The column marked C_d gives the integral of the current-time curve; since it measures the discharge capacity or discharge depth of the particular test, equal C_d-values for horizontal and vertical tests would standardize the degree of etching of the zinc electrodes and the amounts of zincate injected into the electrolyte.

Unquestionably the limiting current density levels obtained with the zinc electrodes in the vertical position LCD_{vert} (Tests Nos. 3, 4, 7, 8 and 9) are substantially higher than those obtained in the horizontal positions LCD_{hor} (Tests Nos. 1, 2, 5 and 6), as expected. For the purposes of our breadboard programming it is important to note that this ratio LCD_{vert}/LCD_{hor} is approximately 2. However, this ratio may vary somewhat, depending on test conditions. With the exception of Tests 7 and 8 all other vertical and horizontal tests have been performed at approximately the same depth of discharge level C_d. This has been achieved by increasing the current slope ($\Delta I/\Delta t$)--initial value (I_o) combination for the vertical measurements. Without this adjustment the C_d-values run much higher (Tests 7 and 8). Such high discharge depths seem to have a small depressing effect on the LCD_{vert} values as expected. Reproducible results seem to be easier to achieve in the vertical position. It must be remembered that test No. 9 was <u>not</u> performed under the same experimental conditions of Tests 1-8. JPL-Arcand used a different geometry, the KOH-concentration was high (40% instead of 30%) and the electrolyte was saturated with zincate prior to testing.

Electronic circuitry for the automated LCD-determinations just described can be simplified substantially, if a linear current-time relationship with $I_o = 0$ (see R_s, Figure 1-2) is substituted for the complicated step functions used by Eisenberg and JPL-Arcand. Such a current ramp can be defined by a single parameter, the ramp slope R_s, expressed in mA/min. The relationship between the discharge capacity C_d and R_s is also simplified:

$$C_d = \frac{LCD^2}{2R_s} \qquad (2)$$

It is interesting to speculate how the various parameters:

Vertical (1-g)	Horizontal (0-g simulation)
LCD_1	LCD_0
C_{d1}	C_{d0}

vary as a function of R_s. At high R_s-values the LCD-level is reached so fast that natural convection has no time to develop. Therefore:

$$LCD_1 \approx LCD_0 \quad (R_s = \text{high}) \qquad (3)$$

Also all LCD-values should be relatively high because removal of zincate from the interface by diffusion is efficient. At low R_s-values on the other hand:

$$LCD_1 > LCD_0 \quad (R_s = \text{low}) \qquad (4)$$

and a lower limit should be reached for both orientations below which passivation can no longer occur, regardless of the smallness of the ramp slope. Figure 1-3 illustrates these correlations qualitatively. In this log-log plot LCD's and C_d's are plotted as a function of R_s. Consider a low ramp slope first (arrow No. 1). The differentiation between the two

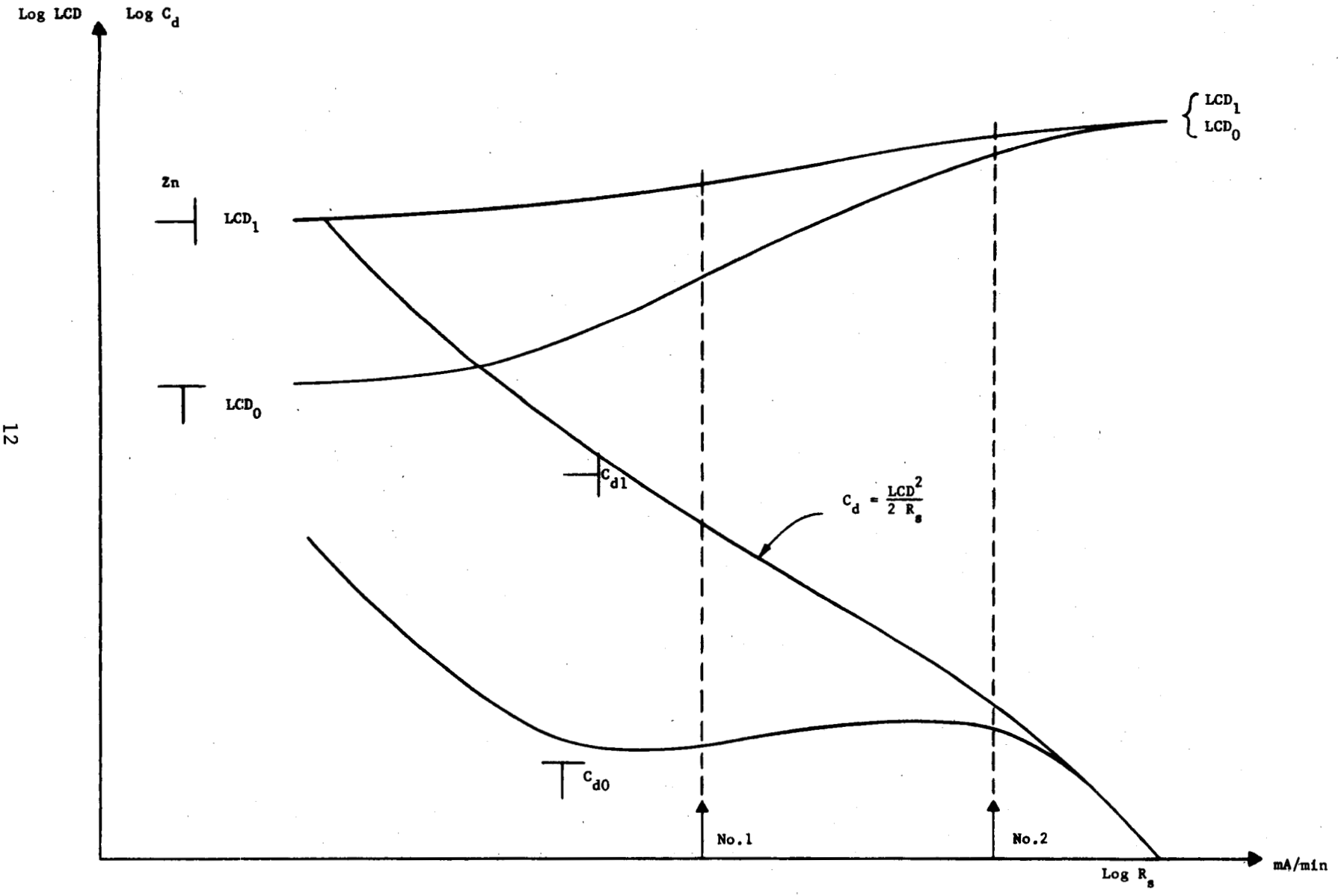

Figure 1-3 Qualitative Relations for LCD and C_d as a Function of R_s ($I_o = 0$)

LCD's is OK but the two C_d's are very unbalanced. At the high ramp slope No. 2 the reverse is true. There is hardly any differentiation between LCD's and therefore an excellent C_d-balance is of no avail. However, combining the results of ramp slope measurements Nos. 1 and 2 gives satisfactory differention and balanced discharge depths.

The same type of balance can be achieved by varying I_o. As can be seen from Table 1-2, this is how Eisenberg matched his C_d-values.

During our private conversations with Dr. G. M. Arcand at the Idaho State University a substantial number of experimental details concerning the JPL test cell were revealed. The zinc used for the zinc electrodes was 99.999% pure zinc, purchased from the Electronic Space Products Corporation in Los Angeles. The thickness of the polycrystalline zinc sheets was given as approximately one-half of a millimeter. The 3.7 centimeter diameter zinc discs are given a short hydrochloric acid etch after which they are rinsed in distilled water and polished on one side with either emery cloth or jewelers rouge. According to Dr. Arcand this polishing step is not very critical because, at the time passivation occurs, discharge etching of the zinc surface is already quite pronounced. Each surface is used only once because after a run the pitting of the zinc is too deep for polishing.

Delayed testing after activation may impair the reproducibility of the LCD values measured. Dr. Arcand prefers to test his electrodes within the first 10 hours after activation.

Dr. Arcand used unformed sintered silver plaques, approximately 1 to 1.5 millimeter thick, which were obtained from Delco-Remy. These plates were charged at approximately 10 milliamps per square centimeter for approximately 24 hours until oxygen evolution could be observed.

1.2 Cell Design and Construction

Since one part of Task 1 includes the repeating of Dr. Arcand's limiting current density tests at 1 G., an exact duplicate of his test cell was desired, however no drawings of the test cell were available. Details of cell construction and a figure were available in JPL Space Programs Summary 37-23, Vol. IV, pp. 23, 24. From the figure and text, a design was developed which included the following critical dimensions and electrode characteristics:

1.	Area of anode:	1 cm x 1 cm (active)
2.	Distance from anode to reference electrode:	1 cm
3.	Distance from anode to cathode:	1.3 cm
4.	Purity of anode:	99.999%
5.	Purity of reference electrode:	99.9%

The cell configuration is that previously shown in Figure 1-1.

It was constructed of plexiglas, held together by machine screws, and sealed with neoprene gaskets. The reference electrode is held and positioned with a nylon screw which also serves as an electrolyte filling port.

The internal cell volume is 6 ml. Electrolyte is 45% KOH saturated with zinc oxide.

The anode material, 0.020" thick Zn, 99.999% was obtained from Electronics Space Products, Inc., Los Angeles.

Anode preparation consists of an etch in 0.01 N HCl followed by a distilled water rinse and polishing with #600 emery paper. The anode is then cemented to the anode mask so that a 1 cm x 1 cm surface is active.

The cathode is cut from a cathode plate from a HR5-DC-7A Yardney Silvercell.

The reference electrode, 0.20" diameter Zn wire, 99.9% is cemented in the nylon screw so that its entire length suspended in the cell is active.

The test cell has been used approximately 35 times. It is leak tight, easily assembled and disassembled. The reference electrode has been replaced twice due to accidental breakage during assembly. The cathode has been recharged four times, recharging being done whenever the surface of the cathode becomes brown in color.

1.3 Test Results

The cell has been tested in two orientations:

a. Gravity vector parallel to anode face, (vertical position):

   1 G. test

b. Gravity vector perpendicular to anode face (horizontal position):

   0 G. simulation test

Preliminary tests were made in orientation (a), (vertical position) under two conditions:

1. Constant current power supply for cell discharge current regulation.
2. Variable resistor across the cell for cell discharge current regulation.

Results of the first test are shown in Table 1-3.

Table 1-3

Task 1 Test Cell Discharged With a Constant Current Power Supply

Test No.	Cell Current ma	Anode to Ref. Volts	Cell Volts
1	24	-0.068	+1.8
	34	-0.107	+1.75
	42	-0.135	+1.72
	50	-0.163	+1.69
	100	+3.40	-1.50

Note: Each test point held 1 minute, approximately

The anode and cell voltage inverted between 50 and 100 milliamps. It was difficult to reset the power supply from test point to test point rapidly enough to assure a given current density being held for 1 minute.

The test was repeated using smaller current increments above 50 ma. These results are shown in Table 1-4.

Table 1-4

Task 1 Test Cell Discharged With a Constant Current Power Supply

Test No.	Cell Current ma	Anode to Ref. Volts	Cell Volts
2	21	-0.030	1.80
	34	-0.071	1.75
	42	-0.106	1.73
	50	-0.130	1.56
	60	-0.144	1.56
	70	-0.220	1.54
	80	-0.255	1.59
	90	-0.320	1.53
	100	+2.30	-1.58

Note: Each test point was taken as quickly as possible. Again the anode and the cell inverted at ~100 ma.

In order to avoid anode and cell inversion, this approach was abandoned, and instead the cell was discharged through a variable resistance. Results of this test are shown in Table 1-5.

Table 1-5

Task 1 Test Cell Discharged Through a Variable Resistance

Test No.	Cell Current ma	Zn to Ref. Volts	Cell Volts
3	0	-0.002	+1.85
	1	-0.013	+1.85
	5	-0.034	+1.85
	10	-0.057	+1.85
	25	-0.122	+1.80
	50	-0.254	+1.57
	60	-0.310	+1.50
	70	-0.360	+1.44
	80	Passivated	

Note: Considerable difficulty was experienced in attempting to hold each point for 1 minute.

In an attempt to more accurately set the load resistance, a decade resistance box was used as a load resistor for the next test refinement. Results of this are shown in Table 1-6.

Table 1-6

Task 1 Test Cell Discharged Through a Variable Resistance (Decade Box)

Test No.	Cell Current ma	Zn to Ref. Volts	Cell Volts	Load Resistance
4	0	0	1.85	8
	1.64	0.014	1.84	1110
	5	0.026	1.81	356
	10	0.043	1.79	174
	25	0.093	1.71	68
	50	0.178	1.61	30
	60	0.218	1.54	23
	100	0.400	1.35	1.5
	150	*		

* Before the current could be adjusted to 150 ma, the anode reached its limiting current density.

The high degree of uncertainty in determining limiting current density by these manual methods indicated that tests would have to be replicated many times to get a reasonably reliable number for LCD. In order to circumvent this difficulty, consideration was given to the use of a current ramp increasing linearly with time. It was felt that such a method should offer better repeatability. However a question arose concerning the best choice of current ramp slope.

Dr. G. Arcand had previously been contacted by phone on March 20, 1968 in an effort to get more detail regarding the testing procedure he had used in his work at JPL. He had indicated that a step-wise current increase had been used as shown in Table 1-7 which we had attempted to follow, e.g. Table 1-6.

Table 1-7

Current Steps Used In Vertical Cell Position

In Dr. Arcand's Tests at JPL

Elapsed Time Minutes	Current ma
0 - 1	1
1 - 2	5
2 - 3	10
3 - 4	25
4 - 5	50
5 - 6	100
6 - 7	150
7 - 8	160
8 - 9	170
9 - 10	180

Based on Dr. Arcand's limiting current density value of 160 ma, and a 1 minute uncertainty in reaching the cutoff voltage, the anode could have been discharged as much as 501 milliamp-minutes if it was held at 160 ma for 1 minute, or as little as 341 milliamp minutes, if the anode reached its limiting current density as soon as it was set at 160 milliamps.

The Task 1 test cell was then discharged using a ramp current increase with the results shown for test 5 in Table 1-8. We selected at first a current ramp slope which would approximate the rate of rise of current shown in Table 1-7 at the upper current levels. Accordingly, a ramp rate of 35 ma/min. was used.

Table 1-8

Current Ramp Tests on Task 1 Cell - Vertical Position

Test No.	Limiting Current Density ma/cm^2	Time To Passivation min.	Ramp Slope ma/min.	Anode Discharge ma-min.
5	180	5.1	35.3	459
6	173	6.5	26.7	564

Since the desired result was 160 ma/cm^2 at 341 - 501 ma minutes, the above data were accepted as encouraging. However, more information was needed on the effect of ramp slope so other ramp slopes were investigated in hopes of achieving a better match with Dr. Arcand's LCD and discharge capacity values.

A shallower ramp slope was selected, 26.7 ma/min, and the cell was retested with the results shown for test 6 in Table 1-8.

These data indicate that reducing of the ramp slope reduced the limiting current density, but caused the capacity discharged to exceed 501 ma-minutes.

Based on the results obtained for Test 5 and 6, a series of tests were run with various current ramp slopes in order to further investigate the influence of ramp slope on limiting current density and capacity discharged. These data are summarizes in Table 1-9.

Table 1-9

Current Ramp Tests on Task 1 Cell - Vertical Position

Test No.	Limiting Current Density ma/cm^2	Time To Passivation min.	Ramp Slope ma/min.	Anode Discharge ma-min
7	114.7	3.57	32.1	205
8	114.8	2.72	42	156
9	197.9	1.64	119	163
10	173.8	2.81	61.7	245
17	171.0	2.77	61.7	237
25	188.0	8.53	24	802
*5	180	5.1	35.3	459
*6	173.4	6.5	26.7	564

* As shown on Table 1-8.

With two exceptions, tests 7 and 8, all the tests performed gave similar LCD's which, to first order, appear to be independent of ramp slope. For example, changing ramp slope by a factor of approximately 5 appeared to have little effect with the associated LCD falling within the range 177 to 199 ma/cm^2. The reason for the wide variation in the two tests (Nos. 7 and 8) is not known exactly but may be partly explained in terms of test equipment limitations. Refinements of the current ramp generator circuit discussed in Section 3.2 have been undertaken to eliminate this possibility in future tests. All reported test data were obtained with fresh electrode surfaces.

A second series of tests were made with the test cell in the horizontal position to simulate 0 G. At low ramp rates, lower LCD values were obtained

but minor difficulties with equipment made some of these results questionable. These measurements will be reported on later once the equipment difficulties have been overcome.

1.4 Conclusions and Recommendations

Based on the exploratory results obtained to date the following conclusions can be reached:

1. We have received sufficient additional information on previous testing at JPL to provide for maximum correlation of data, as required.
2. We believe we have a fair understanding of the processes and parameters which determine the g-dependence of this particular cell design.
3. The cell designed and tested for this task performs satisfactorily.
4. In the interest of a less complex automated programming it was decided to use a linear current ramp for determining the limiting current density of the zinc-electrode.
5. Preliminary results obtained on vertically oriented zinc electrodes with current ramps are encouraging.
6. Circuitry and other minor difficulties encountered in connection with horizontal testing prevented us from getting significant results to date.
7. Renewed testing with improved semi-automatic equipment will be resumed in June, using two ramp speeds.

It is recommended that work on this task be continued without any change in objective. It is further recommended that the existence of possible temperature gradients inside the cell and their effect on natural convection of the electrolyte inside the cell be explored.

2.0 Task 3 - Testing of Commercial Secondary Silver-Zinc Cells

2.1 Introduction

According to the Statement of Work of this contract the breadboard programming for Task 3 should comprise measurements of the electrical capacity and the limiting current capability (E-I curve) of a commercial secondary silver-zinc cell as a function of charge-discharge cycling on an automated basis.

There are various constraints which narrow down the choice of cells which can be used for these tests. For example the entire system shall operate, using not more than 50 watts of power for all operations. Consequently, it is felt that, during the charging part of the cycle, any input power to the cell should not exceed 25 watts in order to allow for power consumption of the control system and recorders. Furthermore the selection of the commercial cell to be used for this task should be restricted to components used in space batteries, and they must be readily available for early delivery to meet the stringent time requirements imposed for this contract. For these and other reasons the following additional specifications were agreed upon with JPL:

1. Our first choice test cell shall be the Yardney silver-zinc cell HR5, having a nominal capacity of 5 ampere hours. This choice makes it possible to compare our test results with other test data generated elsewhere for JPL.

2. Test cycles shall simulate a 90 minute orbit, comprising a charging time of 60 minutes and a discharge time of 30 minutes.

3. The electrical power necessary for charging the cells shall be made available at the 2.5 volt dc level with adequate regulation.

4. During cycling a depth of discharge, not to exceed 65%, shall be selected, which is consistent with the power availability of 25 watts. It would be desirable for such cycling to produce a 20% to 40% reduction of cell capacity after 5 cycles.

Rapid cycling of the type specified is known to constitute a substantial stress to cell performance stability, particularly if the depth of discharge is not too small. Keralla and Lander* for example investigate the cycle life of their zinc-silver oxide batteries as a function of the depth of discharge, which was limited to 21%, 30%, and 40%. They find their cycle life to be a very sensitive function of the depth of discharge. Degradation is measured only in terms of a terminal discharge voltage during cycling with a cutoff of 1.3 volt. No standardized electrical capacity and polarization data, measured before and after cycling, to determine permanent damage to the cells, were given. Nevertheless, the fact that Keralla and Lander restricted their test series to discharge levels below 40% should caution us not to start off our first cycling experiments at too high a percentage level. Consequently, for the purposes of our exploratory tests we chose the 35% depth of discharge level as the one to be used for our first cycling experiments.

2.2 Selection of Battery

At the start of this program, a meeting was held with Dr. Paul Howard, president of P. L. Howard Associates, Inc., a battery consulting firm. His advice was sought relative to the sizes of the batteries to be used in Task 3 and the possible suppliers of such batteries. Charging sources, charging methods, discharge depths, and cycling times were also

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* J. A. Keralla and J. J. Lander, "Sealed Zinc-Silver Oxide Batteries", Proceedings of the 16th Power Sources Conference 1962, page 105.

discussed in light of the task requirements. As a result of our meeting with Dr. Howard, twelve items were developed regarding Task 3 which required clarification before any definitive selection could be made. These items were:

1. The capacity of the cells
2. The manufacturer
3. Vented or sealed cells
4. Maximum allowable charging time
5. Maximum allowable discharge time
6. Type of battery charging source
7. Stability of the charge voltage
8. Discharge cutoff voltage
9. The possibility of a floating or sustaining charge
10. Definition of limiting current capability
11. Degree of correlation to be obtained between Task 3 and Tasks 1 and 2
12. Expected depth of discharge of the cells in actual use.

The most basic constraint on selection is power limitations for battery charging. At this time, with minor exceptions, we have succeeded in defining test requirements and objectives more precisely so that a battery choice has become possible. Prior to meeting with Dr. Howard, and in keeping within the 25 watts estimate as maximum power allowable for cell charging purposes, calculations were made for charging of four standard size commercially available silver zinc cells.

Of the two types of cell charging methods normally used; the constant current method, and the modified constant potential method, the modified constant potential method was selected. The reasons for this

choice are that the modified constant potential method is more suitable for automatic charging circuitry, it requires less complex charging equipment, and is less subject to thermal problems since the input current is regulatable during the entire charge, and finally it is a relatively efficient charging method.

The requirements for a modified constant potential charging system are a constant voltage source and resistor which is placed in series with the charging source and the cell being charged.

For charging a silver oxide zinc cell the constant voltage source is normally 2 to 2.5 volts. The value of the series resistor is selected which will prevent the charging current from exceeding the C-rate of the cell. For example:

$$\frac{E-E_c}{I_{max}} = R_r + R_c \qquad (1)$$

where:

E = Constant voltage source (2.2 volts)

E_c = Voltage of a discharged cell (1.0 volts)

I_{max} = Charging current at the C rate (5 amps max for a 5 amp hr cell)

R_r = Load Resistance

R_c = Internal cell resistance

Substitution of the indicated values in (1) gives:

$$\frac{2.2 - 1}{5} = 0.24 \text{ ohms} = R_r + R_c$$

Since the cell resistance is normally of the order of 0.002 ohms, this may be neglected, hence

$R_r = 0.24$ ohms

If I_{max} is determined on the basis of the discharge capacity of the cell, I_{max} and R_r are variable. Using equation (1) one can determine load resistance and peak power during charging for several cell sizes as shown in Table 2-1.

Table 2-1

Current Limiting Series Resistance and
Maximum Charging Power for Various Capacity Cells

Discharge Cap-AH	Max I	R_r	$W = 2.2V \times I_{max}$
12	12	0.100	26.4
10	10	0.12	22
5	5	0.24	11
1	1	1.2	2.2

From Table 2-1 it is apparent that the initial charging current surge for charging fully discharged (1v) silver oxide-zinc batteries with a capacity in excess of 10 AH at the C rate exceeds the 25 watt maximum allocation. However, lower charge rates could be used providing the charge time is not too long.

Examining the charging process in more detail, one notes that the cell voltage, E_c, also changes during charge because of the monovalent and divalent silver steps which occur during charge.

For example, a silver oxide zinc cell having a discharged voltage of 1 volt quickly rises to 1.6 volts (approx.) for the monovalent silver plateau. At approximately 30% of charge the cell voltage rises to 1.90 volts (approx.) for the divalent silver plateau. Near the end of charge the cell voltage

again increases to 1.92 volts and then increases sharply due to oxygen and hydrogen gassing from the cathode and anode respectively. The cutoff voltage is adjusted ot occur at or just below the gassing potential depending upon whether or not a vented cell is used.

As the cell voltage rises during charge, the cell current decreases. Near the end of the charge the charging current is relatively small.

Data in the following Table 2-2 illustrate the relationships between percentage input capacity, cell voltage, cell current, ampere hours, and elapsed charging time for 4 cell sizes charged by the modified constant potential method. In all cases the cell is assumed to be completely discharged at the beginning of charge and the initial charging current is limited to the C rate of the cell. Since the charging efficiency is assumed to be 90 percent, each cell is charged 110 percent of its discharge capacity. The total elapsed time is in each case the minimum allowable charging time for a cell charged from a 25 watt source under the conditions stated above.

From Table 2-2 it is shown that in all cases the charging time is approximately 4 hours and that the ratio of the initial charging current to the final charging current is 6 to 1. From this it becomes apparent that maximum charge rates in excess of the C rate are necessary if relatively short charging times are required, e.g., such as a 60 minute charge simulating an earth orbit application.

From the twelve items developed in our meeting with Dr. Howard and the data in Table 2-1, tentative decisions were made concerning minimum charging times, the charging method, the initial charging currents, the constant voltage source desired, and the possible battery sizes in keeping with the 25 watts power available for charging sources.

Table 2-2 Cell Charging Characteristics--Modified Constant Potential Method

		12 AH Cell			10 AH Cell		5 AH Cell		1 AH Cell	
% Max. Cell Capacity	Ec, Cell Volts On Charge	T, Time In Hours At I_c*	I_c, Charge Current Where R_r = 0.1 Ω	AH, Ampere Hours Input Capacity	I_c, Charge Current Where R_r = 0.120Ω	AH, Ampere Hours Input Capacity	I_c, Charge Current Where R_r = 0.240 Ω	AH, Ampere Hours Input Capacity	I_c, Charge Current Where R_r = 1.2 Ω	AH, Ampere Hours Input Capacity
	1.00		12		10		5.00		1.00	
0	1.60	0	6	0	5	0	2.50	0	.50	0
10	1.60	.2	6	1.2	5	1	2.5	.5	.50	.1
20	1.60	.2	6	2.4	5	2	2.5	1	.50	.2
25	1.75	.114	4.5	3.0	3.75	2.5	1.88	1.25	.375	.25
30	1.90	.114	3.0	3.6	2.5	3	1.25	1.5	.250	.3
40	1.90	.40	3.0	4.8	2.5	4	1.25	2.0	.250	.4
50	1.90	.40	3.0	6.0	2.5	5	1.25	2.5	.250	.5
60	1.90	.40	3.0	7.2	2.5	6	1.25	3.0	.250	.6
70	1.90	.40	3.0	8.4	2.5	7	1.25	3.5	.250	.7
80	1.90	.40	3.0	9.6	2.5	8	1.25	4.0	.250	.8
90	1.92	.414	2.8	10.8	2.33	9	1.17	4.5	.233	.9
100	1.92	.429	2.8	12.0	2.33	10	1.17	5.0	.233	1.0
110	2.00	.500	2.0	13.2	1.67	11	.84	5.5	.167	1.1
		3.971 hrs.								

*I_c is charging current

Concurrence was sought regarding these parameters from the Jet Propulsion Laboratory at a meeting held on February 28, 1968. Official approval was granted in JPL Technical Direction Memorandum No. 121-1, dated 3/27/68. The following items were included:

1. The cell size would be 5 ampere hours which would correlate with the size being used by Crane Naval Ammunition Depot for a study being conducted for the Jet Propulsion Laboratories (Yardney HR5).

2. The manufacturer of the cells would be Yardney Electric for the same reason as stated in 1.

3. The cells would be vented.

4. A ninety minute orbiting time would be simulated.

5. In addition to five ninety minute cycles, there would be an initial deep discharge and a recharge.

6. Two polarization curves would be measured before and after cycling.

7. Following the ninety minute cycles, a final deep discharge would be made to measure the change in cell capacity from the initial deep discharge.

8. Maximum charging time would be 60 minutes during the cycling phase.

9. Maximum discharge time would be 30 minutes during the cycling phase.

10. Maximum depth of discharge would be 65% of rated cell capacity during the cycling phase.

11. Charging power limit would be 25 watts average with allowance for surge peaks above this value, with an attempt made to limit the surge current to the C rate of the cells.

12. Electrical power would be available as:

    a. 2.5 v dc $\pm$ 10% at 25 watts

    b. 28 v dc $\pm$ 10% at 25 watts

The overall approach to Task 3 cycling was predicated toward an accelerated cell life test.

The final choice of battery size was based primarily on charging power restrictions. Table 2-3 lists the important parameters and the basis for the calculation. From this it is apparent that a cell with a 5 AH capacity is about the maximum size possible within a 25 watt charging power limit.

On March 5, 1968, Mr. Sheldon Feld of Yardney Electric was called regarding our requirements for Task 3. He recommended the Yardney HR5-DC-7A cell equipped with a 5 psi relief valve and a minimum electrolyte volume. Since we are interested in a maximum of five cycles, he indicated that we might be able to exceed discharge depths of 25% in 1/2 hour with correspondingly increased charging rates. He also indicated that since cell performance is so heavily dependent on immediate past cell history, our requirements would necessitate a test program such as we had planned.

2.3 Test Procedure

A detailed test program for Task 3 cells was developed in keeping with the task requirements and, insofar as possible, with the manufacturers recommendations.*

Task 3 Test Program

(35% Discharge Depth During Cycling)

1. Fill cell with 16 cc of electrolyte
2. Let cell soak for 72 hours
3. Measure and note cell voltage

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* Bulletin: 1000 Series - Service and Operating Instructions For The Yardney Silvercell Battery, August, 1961.

4. Charge by modified constant potential method until cell voltage equals 2.05 volts where 1.82 is the initial cell voltage and the current limiting resistor. is 1 ohm.

$$\frac{2.05 - 1.82}{1} = .23 \text{ amp, initial current}$$

5. Discharge at 0.29 amps constant current until the cell voltage drops to 1.0 volt.

6. Charge by modified constant potential method until the battery voltage equals 2.05 volts where 1.5 is the anticipated recovered cell voltage and 0.32 is the initial charging current.

$$\frac{2.05 - 1.5}{0.32} = 1.71 \text{ ohms}$$

7. Discharge 20%, or 1AH, (2 amps for 1/2 hr.) at constant current.

8. Measure polarization curve from open circuit to 1.2 volts in 2 amp steps holding each current value for 1 minute.

(0, 2, 4, 6, 8, 10, etc. amps)

9. Charge by modified constant potential method until the cell voltage equals 2.05 volts where 1.5 is the anticipated recovered cell voltage and 0.88 is the initial charging current.

$$\frac{2.05 - 1.5}{0.88} = .625 \text{ ohms}$$

10. Discharge 35%, or 1.75 AH, (3.5 amps for 1/2 hr.)

11. Charge until the battery voltage equals 2.05 volts after 1 hr.

12. Same as 10

13. Same as 11

14. Same as 10

15. Same as 11

16. Same as 10

17. Same as 11

Table 2-3

Charge Power Load Versus Battery Capacity

Capacity AH.	R_s* Series Resistance Ohms	I_s** Surge Current Amps	P_s** Surge Power Watts	P_{av}** Average Power Watts
5	0.098	9.2	23	15.5
10	0.049	18.4	46	31

* Based on 60 min. charge, 2.25 v supply, 65% DOD, 90% charge efficiency

$$R_s = \frac{2.25 - 1.90}{1.1\ (0.65)\ C} = \frac{0.49}{C}$$

** Based on 2.50 v supply, 1.6 volt cell voltage at start of charge

$$I_s = \frac{2.5 - 1.6}{R_s} = \frac{0.9\ C}{0.49} = 1.84\ C$$

$$P_s = 2.5\ I_s = 4.6\ C$$

$$P_{av} = \frac{V_s(V_s - 1.9)\ C}{0.49} = \frac{2.5\ (0.6)\ C}{0.49} = 3.1\ C$$

18. Same as 10

19. Same as 11

20. Same as 7

21. Same as 8

22. Same as 6

23. Same as 5

Note: Calculations shown in the above program are based on typical data.*

2.4 Test Results

Figures 2-1 and 2-2 comprise a voltage, current, time profile obtained on a HR5-DC-7A cell tested in accordance with the Task 3 test program. Figure 2-1 covers steps 1 through 6 above while Figure 2-2 covers the remainder.

Since the Task 3 test program was designed as a life test, particular emphasis was placed on cell voltages and charge and discharge capacities throughout the test program. In Table 2-4 will be found data pertinent to the analysis of the Task 3 test program for discharge cycle depths of 35%.

2.5 Discussion of Test Results

Capacity Balance

A dry charged battery having a rated capacity of 5 ampere hours but of an unknown actual capacity was placed on charge until its terminal voltage was 2.05 volts. A total of nine charge steps and 12 discharge steps were made. Summing charge and discharge capacities gives:

Charge Capacity (Input): 24.59 AH

At an estimated charge efficiency of 0.9 the actual useful capacity input is: 22.13 AH

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* Vinal, Secondary Batteries

(1)		Fill	
(2)		Soak 72 Hours	
(3)	(4)	Mod. Const. Pot. Charge to 2.05 V.	A
(4)	(5)	Const. Cur. Discharge to 1.00 V.	B
(5)	(6)	Mod. Const. Pot. Charge to 2.05 V.	A
(6)	(7)	Const. Cur. Discharge - 20%	C
(7)	(8)	Polarization Curve - 0-10 Amps	D
(8)	(9)	Mod. Const. Pot. Charge to 2.05V	A
(9)	(10)	Const. Cur. Discharge - 35%	E
(10)	(11)	Mod. Const. Pot. Charge to 2.05 V.	A
(11)	(12)	Const. Cur. Discharge - 35%	E
(12)	(13)	Mod. Const. Pot. Charge to 2.05V.	A
(13)	(14)	Const. Cur. Discharge - 35%	E
(14)	(15)	Mod. Const. Pot. Charge to 2.05 V.	A
(15)	(16)	Const. Cur. Discharge - 35%	E
(16)	(17)	Mod. Const. Pot. Charge to 2.05V.	A
(17)	(18)	Const. Cur. Discharge - 35%	E
(18)	(19)	Mod. Const. Pot. Charge to 2.05 V.	A
(19)	(20)	Const. Cur. Discharge - 20%	C
(20)	(21)	Polarization Curve - 0-10 Amps	D
(21)	(22)	Mod. Const. Pot. Charge to 2.05 V.	A
(22)	(23)	Const. Cur. Discharge to 1 V.	B

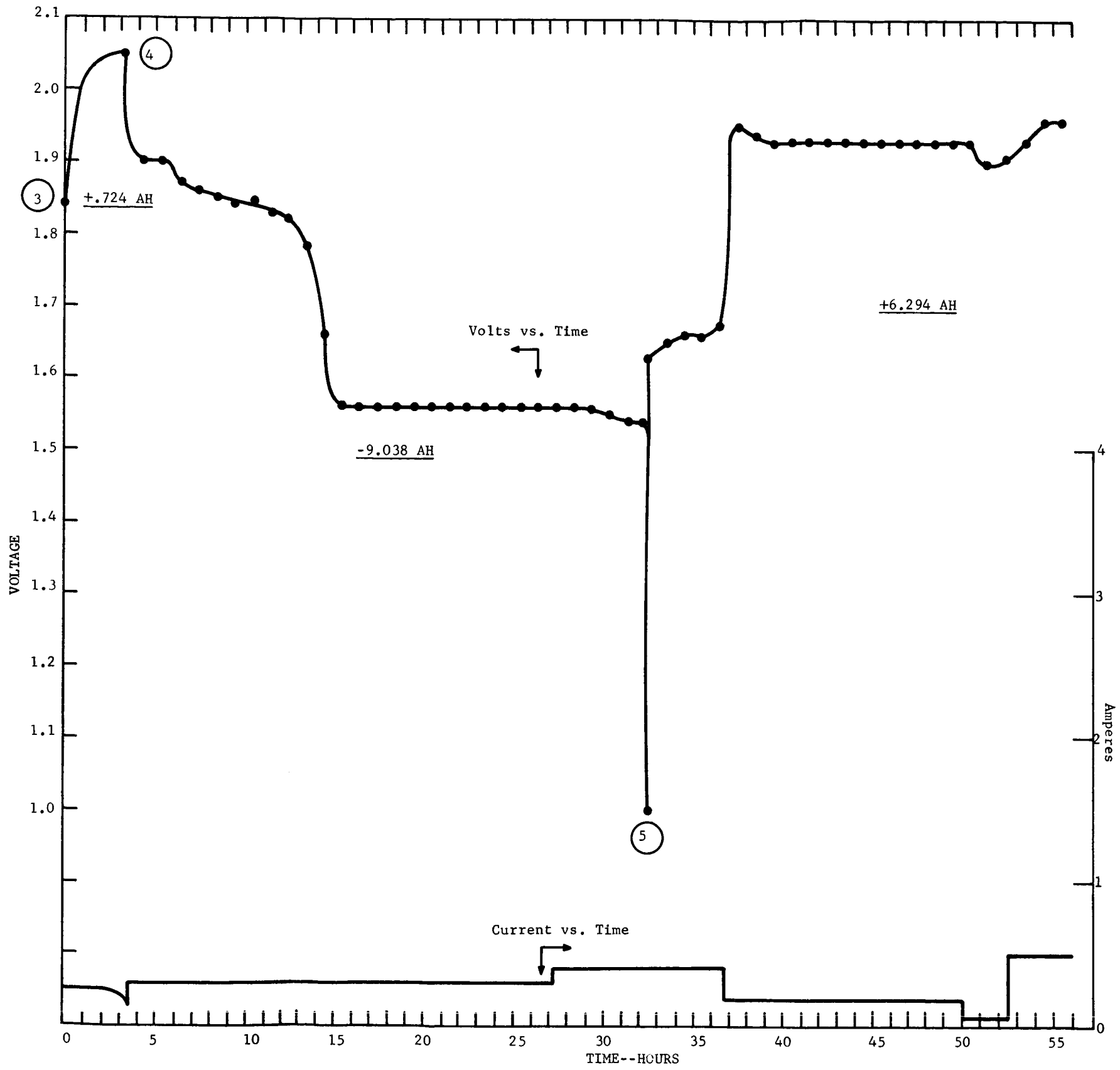

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Figure 2-1 Results of Task 3 Test Program Using a Yardney HR5-DC7A Silver-Zinc Secondary Cell - Part 1

35-A

35-B

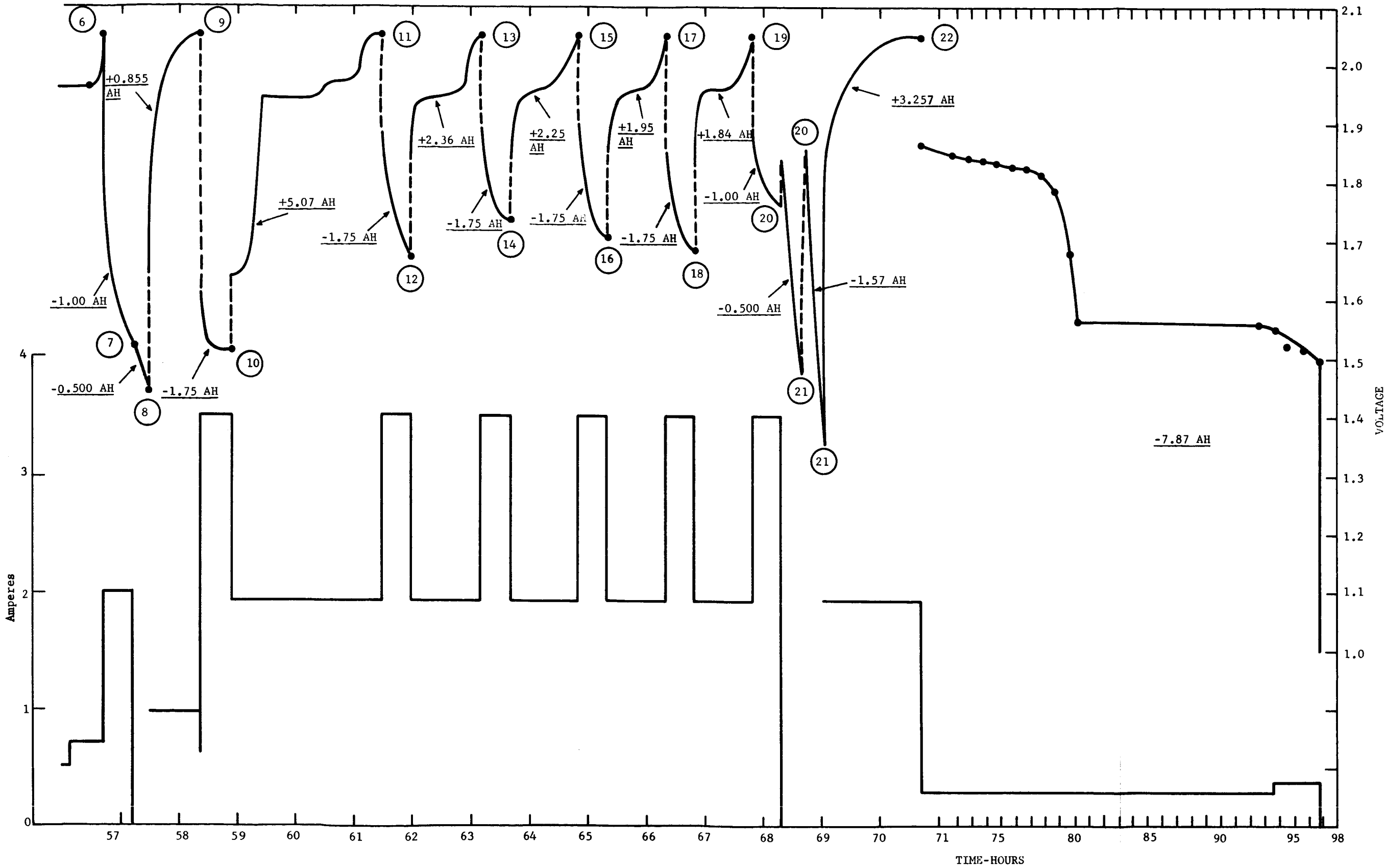

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Figure 2-2 **Results of Task 3 Test Program Using a Yardney HR5-DC7A Silver-Zinc Secondary Cell - Part 2**

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36-A

36-B

Table 2-4

Salient Parameters Measured in Test of Yardney HR5-DC-7A Cell

Step No.	Event	Starting Voltage	Final Voltage	Starting Current	Final Current	Capacity Input	Capacity Output
3	Cell Voltage Check	1.84	1.84	-	-	-	-
4	Charge to 2.05 V	1.84	2.05	0.23	0.13	.724	
5	Discharge to IV	2.05	1.00	0.29	0.40		9.038
6	Charge to 2.05 V	1.00	2.05	0.40	2.00	6.294	
7	Discharge 20%	2.05	1.60	2.0	2.0		1.06
8	Polarization Curve	1.60	1.44	0	10		.500
9	Charge to 2.05 V	1.64	2.05	.96	.96	.855	
10	Discharge 35%	1.61	1.51	3.5	3.5		1.75
11	Charge to 2.05 V	1.64	2.05	1.9	1.9	5.07	
12	Discharge 35%	1.85	1.67	3.5	3.5		1.75
13	Charge to 2.05 V	1.85	2.05	1.9	1.9	2.36	
14	Discharge 35%	1.88	1.74	3.5	3.5		1.75
15	Charge to 2.05 V	1.82	2.05	1.92	1.92	2.25	
16	Discharge 35%	1.9	1.71	3.5	3.5		1.75
17	Charge to 2.05 V	1.85	2.05	1.92	1.92	1.95	
18	Discharge 35%	1.86	1.68	3.5	3.5		1.75
19	Charge to 2.05 V	1.83	2.05	1.92	1.92	1.84	
20	Discharge 20%	1.88	1.76	3.5	3.5		1.00
21	Polarization Curve	1.84	1.47	0	10		.500
21a	" "	1.86	1.35	0	10		1.570
22	Charge to 2.05 V	1.83	2.05	1.93	1.93	3.25	
23	Discharge to IV	1.86	1.00	0.30	0.40		7.87

Discharge Capacity (Output): 30.29 AH

Since the starting capacity is unknown, subtracting the input capacity from the output capacity gives:

30.29 - 22.13 = 8.16 AH

This may be taken as the actual capacity of the cell in the dry charged state.

Comparing the discharge capacity obtained in the first deep discharge, step 5, with the discharge capacity obtained in the second deep discharge, step 23:

step 5 9.04 ampere hours
step 23 -7.87 ampere hours
1.17 loss of capacity in ampere hours

or 12.9% loss in capacity is associated with this testing regime.

Since the 90 minute orbit simulations are of primary importance steps 10 through 19 shown in Figure 2-2 will be considered, since these simulate 5 such ninety minute orbit simulations during these charging periods. 13.47 ampere hours of charge were applied. Estimating a 90% charging efficiency:

.9 x 13.47 = 12.12 ampere hours of useful charge were applied. The capacity discharged from the cell during the 5 discharge cycles is:

5 x 1.75 AH = 8.75 AH.

12.12 - 8.75 = 3.37 AH the capacity loss during the 5 ninety minute orbit simulations.

Because the apparent loss in capacity during the five 90 minute orbit simulation cycles exceeds the net loss for the entire test program, it is concluded that the deep discharge in step 5 was inordinately high due to the low discharge current used. In subsequent tests the deep discharge steps

5 and 23 will be shortened so that less of the excess zinc capacity will be removed from the cell. This follows from the fact that a HR5-DC-7A cell contains approximately 11 ampere hours of zinc capacity.

It is also noted that the end-point voltages measured during the 30 minute discharges during the 90 minute cycles actually increase from 1.51 to 1.74 volts during the first three discharges and then dropped to 1.68 volts for the fifth cycle, indicating a partial restoration of battery capacity. The input capacities during the charge portions progressively diminish from 5.07 to 1.84 ampere hours before the cutoff voltage of 2.05 volts is reached indicating a progressively earlier gassing with a consequent loss of charge acceptance.

The polarization curves obtained in steps 8 and 21 show virtually no differences thus indicating that the cell in a 20% discharged state at the beginning of the testing porgram is essentially the same as at the end of the testing program. It is possible that the polarization curves terminating at 10 ampere are not deep enough to indicate change in cell characteristics. Subsequent polarization curves will be made to terminating currents of 15 amperes or 1 volt, whichever occurs first.

From the above data it is concluded that a HR5-DC-7A cell can be cycled 5 times or more in a 90 minute orbit with a 35% discharge in 30 minutes followed by a 1 hour recharge and have a terminal voltage in excess of 1.2 volts at the end of the fifth discharge.

The same type of testing regime will be used for discharge depths between 35% and 65% in future tests.

2.6 Conclusions and Recommendations

As stated earlier the conclusions to be derived from the exploratory hand operated test series completed to date are based on:

1. Transient capacity and voltage measurements during 90 minute cycling.
2. Polarization measurements before and after cycling.
3. Discharge capacity measurements before and after cycling.

None of these signals appear to indicate the degree of degradation desired for this type of accelerated life test program performed at the 35% discharge depth level. It is therefore recommended, that:

A. The test program for Task 3 be continued using, in addition to the HR5 cell, some of the automatic switching equipment to be described in the next section.

B. The capacity measurements before and after cycling be performed at a higher current level to bring such capacities more in line with the nominal value of 5 AH.

C. The depth of discharge level be increased beyond the 35% level.

3.0 Control Logic and Switching

This section of the report will cover essentially three aspects of the control logic and switching. These are:

1. The selection of the approach to the control logic and switching.
2. The control circuits necessary to make the limiting current density measurements in Task 1.
3. The control circuits and logic design necessary to make a complete sequence of tests on the Task 3 commercial cells.

The control logic and switching for the Task 2 tests will be covered in a later report. The Task 3 sequence logic is, perhaps, the most complicated of the logic necessary for the three tasks. The results obtained from working with the Task 3 logic will be applicable to the logic necessary for the other Tasks.

3.1 Selection of Approach

3.1.1 Preliminary Considerations and Requirements Affecting the Choice of Approach

The switching circuits of the breadboard must have four functions. These are:

1. Provide a set of preprogrammed contact closures that will be used to start and stop specific tests on a cell.
2. Provide a method of transferring the test circuits from one cell to another.
3. Provide the necessary switching of the measurands onto the proper tape recorder channels as well as control the period of operation of the recorder and
4. Provide a fail safe mechanism so that the test program can continue if one or more of the cells tested should fail to function properly.

These functions must be provided using components that are flight qualified or components whose design and construction are such that there is every reason to believe that they can survive the expected environment and could therefore be flight qualified.

From the beginning of the program, it appeared that these were two basic approaches that could be used for the switching design. The first approach uses a mechanical device such as stepping switch to provide both the program and contact closures. The second approach was to use logic circuitry to follow the switching program and to use relays for the contact closures.

There are several requirements which affect the choice of the approach. These are:

1. Flight qualification of components
2. Ease of changing test program sequence
3. Power consumption
4. Noise immunity
5. Space and weight

The most critical requirement is the flight qualification of components. The breadboard should use electronic components which have been flight qualified. If a type of device is needed where there is no flight qualified substitute it is permissible to use an unqualified unit as long as there is no reason to believe that the type of device in question could not become qualified.

The circuits should be designed so that it is fairly easy to change the test sequence at least while the circuits are in an experimental stage. On the final breadboard, the test sequence would be fixed but certain

parameters should be easily changeable.

The average power consumption of the switches, circuits, camera, and tape recorder should be held to a maximum of 25 watts. This allows 25 watts to be used for charging cells during various portions of the tests and still keep the total power consumption to the required 50 watts.

The circuits should be free from the effects of noise sources in and around the breadboard. This will assure that in a later flight version, the breadboard will be unaffected by noise in the spacecraft or by signals generated by other tests on the spacecraft.

While there are as yet no specific space and weight requirements, it would be desirable to keep these quantities to a minimum.

3.1.2 Comparison of Alternatives

The mechanical stepping switch approach would probably result in the simplest circuit arrangement. A multiposition switch which is made up of several ganged sections could provide the switching to follow the program plan as well as provide the switching for the tape recorder functions. The average power consumption of a stepping switch is relatively low since power is required only during the stepping operation. The space required and the weight of the switch would be relatively great. For example, the sequence logic for Task 3 weighs approximately 7 ounces. A stepping switch to perform the same function would weigh about three times as much.

The main disadvantage of the stepping switch however is its sensitivity to shock and vibration. Those vendors contacted expressed real concern over the ability of their switches to survive the shock and vibration levels specified in JPL specification 30250B. In the absence of any units which were flight qualified, the cost of testing, coupled with the high probability

of failure, and high development cost of an acceptable stepping switch made this appear like a relatively unfruitful approach.

Another disadvantage is the lack of flexibility when using a stepping switch for programming. If the test program were to be changed, the switch would probably require rewiring.

An investigation was made of the applicability of mechanical commutators in place of stepping switches. It was found that, in general, the commutators were not designed to handle the currents that must be switched in this type of program.

The two major disadvantages of the stepping switches are eliminated if integrated circuit logic and relays are used. There are several integrated circuit logic units that are flight qualified. In addition, there are many other integrated circuits that are manufactured to military specifications for which there is no apparent reason why they couldn't also become qualified. There are several models of flight qualified relays available and also a few more military models that could probably be qualified if their use were necessary.

The use of solid state switches in place of relays was investigated and it was concluded that a solid state switch might be useful in high impedance switching applications but that their equivalent contact resistance was too high for them to be useful in low impedance cell switching applications.

Utilizing the integrated circuit approach, a change in the program plan would result in only a few relatively minor changes in the overall logic. Additions could be made to the test plan that would not require major component changes, at least while the logic is in an experimental

stage. The power consumption is nominal and the test plan circuitry should dissipate less than the allowed 25 watts.

Integrated circuits operate on low voltages and are high speed devices. This combination of factors makes these circuits somewhat sensitive to noise. However, the noise is no real problem if the situation is recognized and proper precautions are made to minimize it.

3.1.3 Selection

We have therefore concluded that the use of integrated circuit logic to provide the program plan, and relays to provide contact closures is the best method of implementing the breadboard test and the subsequent flight unit. These devices should be more reliable in the expected environment, they stand a much better chance of passing the tests necessary for flight qualification; they are smaller and lighter providing a saving in space and weight, and promise to be more versatile in their applications.

This is the switching method that we have chosen to use. Much of the logic for the Task 3 test sequence has been built and tested and there is every indication that the choice made is a good one. A description of the logic and some of the test results are given in Sections 3.3.2 and 3.3.3.

3.2 Task 1 Control Circuitry

A functional block diagram of Task 1 is shown in Figure 3-1. Tests are performed on six silver-zinc cells in a sequential manner. The cells are connected to a cell switch which is composed of both relays and integrated circuit logic. The measurands are fed to their proper channels on the tape recorder through a calibration circuit. This circuit provides a check of the calibration and zero drift of the tape recorder amplifiers.

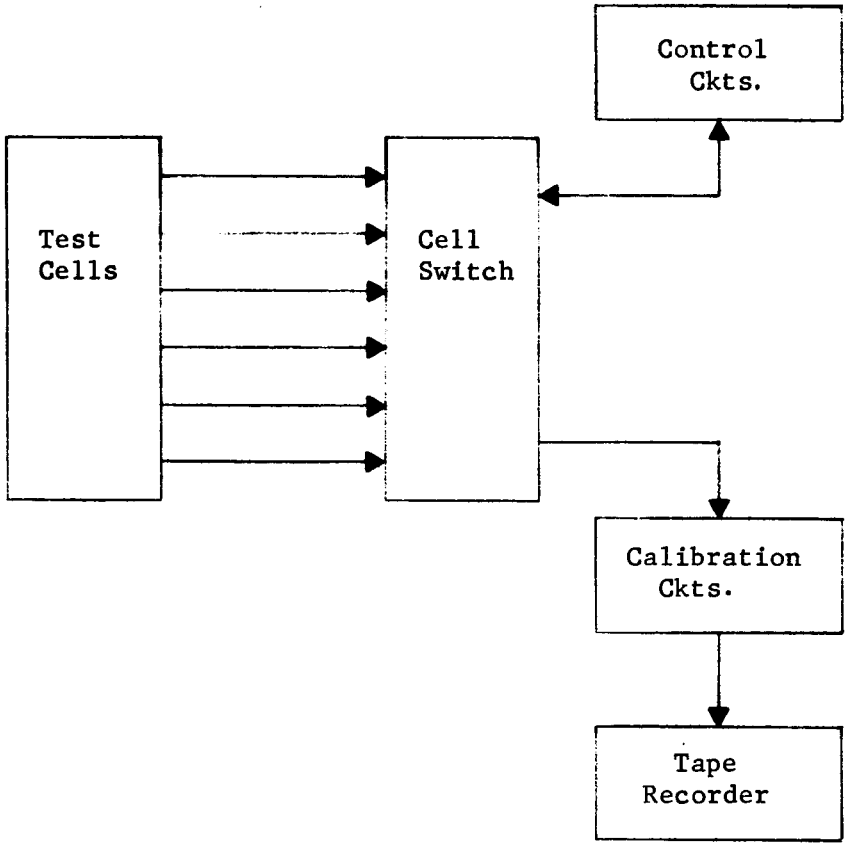

Figure 3-1 Task 1 Functional Block Diagram

The control circuitry provides the test plan and also provides the functions that are used to load the cell in various ways. This section will deal only with a description of the control circuitry. The other circuits will be covered in a subsequent report.

3.2.1 Requirements

The testing program for Task 1 involves measurements of limiting current density (LCD) on a number of silver-zinc cells of a design previously tested at high g levels by JPL. The LCD measurement is to be made by discharging the cell using a calibrated current ramp. The control circuits to accomplish this consist of two parts. The first is a current control circuit which discharges the cell at a discharge current rate that is directly proportional to the control voltage input. The second is a circuit which generates the requisite control voltage input for the first. The latter circuit is designated a voltage ramp generator. When the output of the voltage ramp generator is connected to the input of the current control circuit, a current ramp discharge of the cell is produced.

The potential difference between the zinc working electrode and a zinc reference electrode is measured during the current ramp discharge. The LCD is defined as the current density when this potential reaches 1.0 volts. It may be noted that the actual potential across the working cell will be on the order of 0.5 volts at the LCD. The cell design provides a 1 cm^2 electrode area so that a current measurement is directly relatable to the average current density of the electrode.

3.2.2 Description of Circuit

The discharge current control circuit is shown in Figure 3-2. An NPN transistor is connected across the cell and is used as the load. The

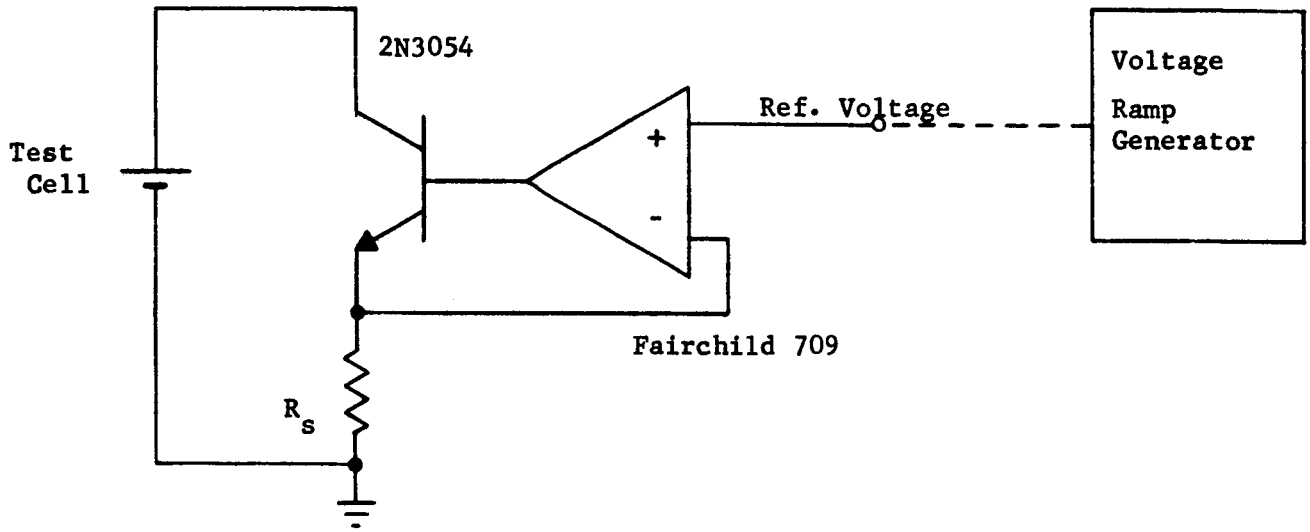

Figure 3-2 Task 1 Discharge Current Control Circuit

bias on the transistor determines its impedance and therefore the load on the cell. A small resistance R_s, in series with the transistor and the cell is used to measure the discharge current. The transistor bias is controlled by a high gain operational amplifier. The inverting input of the amplifier is connected across R_s so that a feedback voltage is applied which is proportional to the discharge current. The voltage at the non-inverting input is a reference voltage and sets the discharge current level. The voltage on the inverting input is equal to the discharge current multiplied by R_s. This voltage is essentially held equal to the reference voltage applied to the noninverting input by a suitable level of discharge current. If the reference voltage is varied, the discharge current will also vary and at any time will be equal to V_{ref}/R_s. Thus if the reference voltage supplied by the voltage ramp generator increases with time at a constant rate, the discharge current control circuit acts to make the discharge current increase with time in a similar fashion.

As the cell polarizes, the cell voltage drops. The LCD occurs when the approximate cell voltage is 0.5 volts. This requires that the sum of the saturation voltage of the transistor (V_{CE}) and the voltage drop across R_s at LCD be less than 0.5 volts. In practice, the sum of these potentials can be on the order of 0.2 to 0.3 volts so that the discharge current control circuit will function adequately over the entire range of cell voltages expected.

The voltage ramp generator for the Task 1 control system utilizes an operational amplifier in an integrator circuit. A circuit diagram of this is shown in Figure 3-3. The operational amplifier is a Bell and Howell type 20-008-01 and has field effect transistors (FET) in its input stages. The FET's provide a very high input impedance to the amplifiers which is

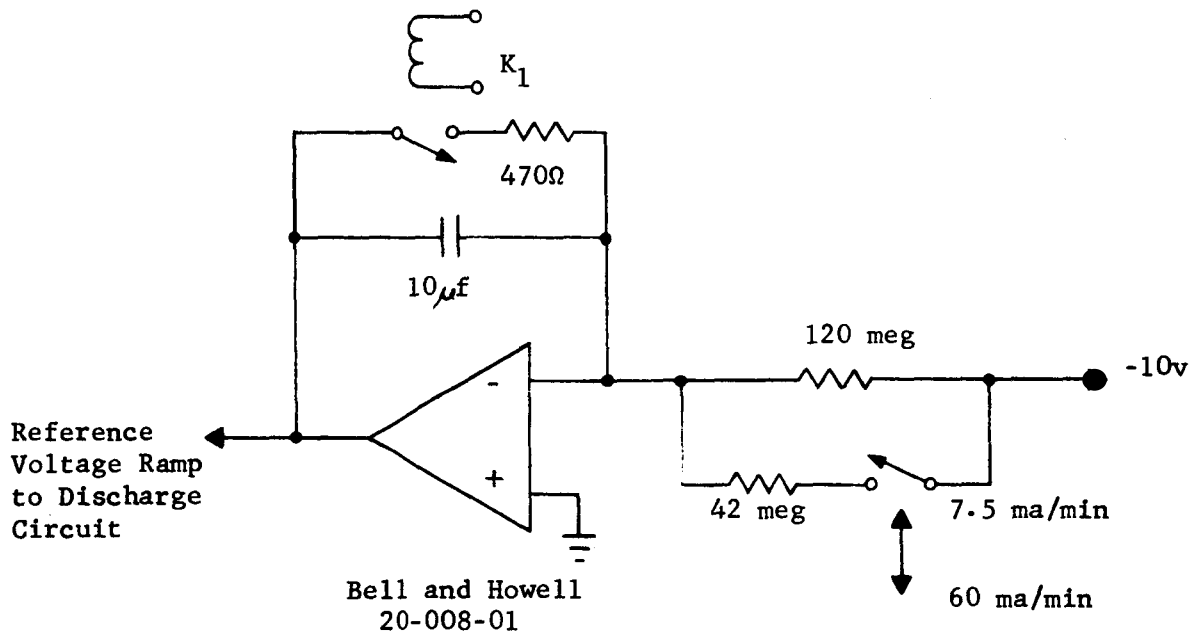

Figure 3-3 Task 1 Voltage Ramp Generator

necessary to achieve stability with the large series resistances necessary to achieve the required voltage ramp slopes.

This ramp slope is determined by the RC time constant and since two different slopes are necessary, two values of the series input resistance are provided. The relay contacts across the integrating capacitor C, are used to stop and reset the ramp output voltage to zero. The combination of the discharge current control circuit and the voltage ramp generator provides two alternate current ramps; one with a rate of 7.5 ma/min up to a maximum of 150 ma, and the second with a rate of 60 ma/min up to a maximum of 250 ma.

3.2.3 Results to Date and Status

Two different voltage ramp generators and discharge current control circuits have been built for obtaining experimental data with Task 1 cells. The first was an adaptation of a similar circuit built for Task 3 cells where a current ramp with a maximum discharge current of 10 amps was required. Useful data were obtained with Task 1 cells using this circuit, but since it was not designed specifically for Task 1 cells, the ramp rate was not adequately stable at the lowest slopes of interest.

A second circuit has been designed specifically for Task 1 measurement and provides the ramp rates given at the end of the last section. Temperature stability measurements have been made on this ramp generator and the ramp slope varies less than 0.3%/^{o}C over the range from 10^{o}C to 40^{o}C.

3.3 Task 3 Control Circuitry

3.3.1 Requirements

The sequence of events that takes place during the Task 3 program

to test commercial cells is much more complicated than the rather simple LCD measurement of Task 1. A complete description of the test sequence is given in Section 2.2. The 21 test steps listed there include a number of different operations including three rates or levels of discharge, two rates of charge and a current ramp polarization.

A functional block diagram of the Task 3 program is shown in Figure 3-4. The test cell switching and the calibration circuit will be discussed in a later report. The discharge circuits are very similar to those described in Task 1 except that they are designed to handle higher currents. The charge circuits and test sequence logic voltage level sensors and interval timer will be covered in detail in this section.

As stated above, there are 21 test steps in the logic sequence. The shift from one step to another is initiated when cell voltage reaches some preset level in the case of the deep discharge capacity measurement and for the two different charge rates which is detected by the voltage level sensors. The shallow discharge cycles are constant current discharges that proceed for 30 minute timed intervals. In this case, the shift to another test step is initiated by the end of the 30 minute time period. In some test steps, overrides are necessary to insure against test interruption in the event of cell failure. For example, a 60 minute timed override operates during the shallow charge cycle. Thus if a cell does not reach the charged state as indicated by cell voltage within 1 hour the timed override will provide for the test sequence to continue. This insures that the maximum elapsed time for a complete shallow discharge and charge is 90 minutes. The deep discharge voltage level sensor also acts as a voltage level override on the shallow discharge cycle. Thus if cell voltage were to drop to some preset level before the 30 minute discharge

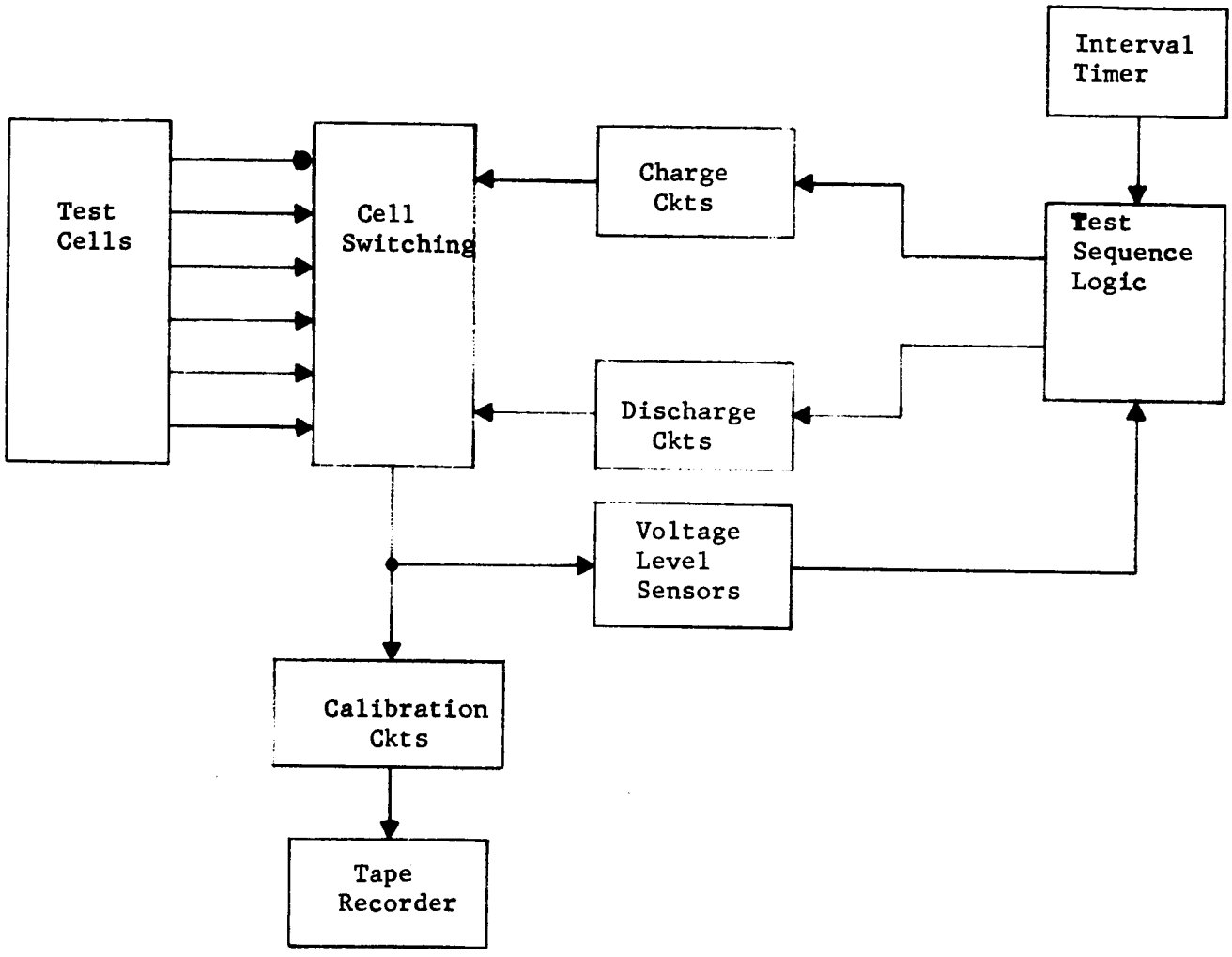

Figure 3-4 Task 3 Functional Block Diagram

was completed, the voltage overide would terminate the discharge cycle.

Integrated circuit components are used to build the logic necessary to control the test steps and to govern the order in which the tests are made.

3.3.2 Description

The discharge current control circuit and voltage ramp generator used in Task 3 for polarization measurements are very similar to those described in Section 3.2.2. The major difference is that much higher current levels must be controlled for Task 3 tests and therefore the load transistor must dissipate a maximum of 10 to 15 watts during discharge. The cells are charged by a modified constant potential method the circuit for which is shown in Figure 3-5. Two series resistances, R_1 and R_2 govern the two different charge rates possible. Relays (K_2 and K_3) determine which resistance is switched into the charging circuit.

The voltage level sensors provide the logic with a signal when the cell has reached a preset voltage (or current) level. There are three of these, each set for a different voltage level. The upper voltage level sensor indicates when the cell has reached its charged voltage of 2.05V. The center level sensor indicates when the cell has been discharged to capacity or 1.2 volts. The lower voltage level sensor receives a voltage signal from the voltage ramp generator output which is used to indicate when the maximum current has been reached during polarization tests.

The level sensors are designed around Fairchild type 709 operational amplifiers. Their circuit diagram is shown in Figure 3-6. The positive feedback from the output to the noninverting input makes the amplifier switch quickly whenever the measured voltage input exceeds the reference

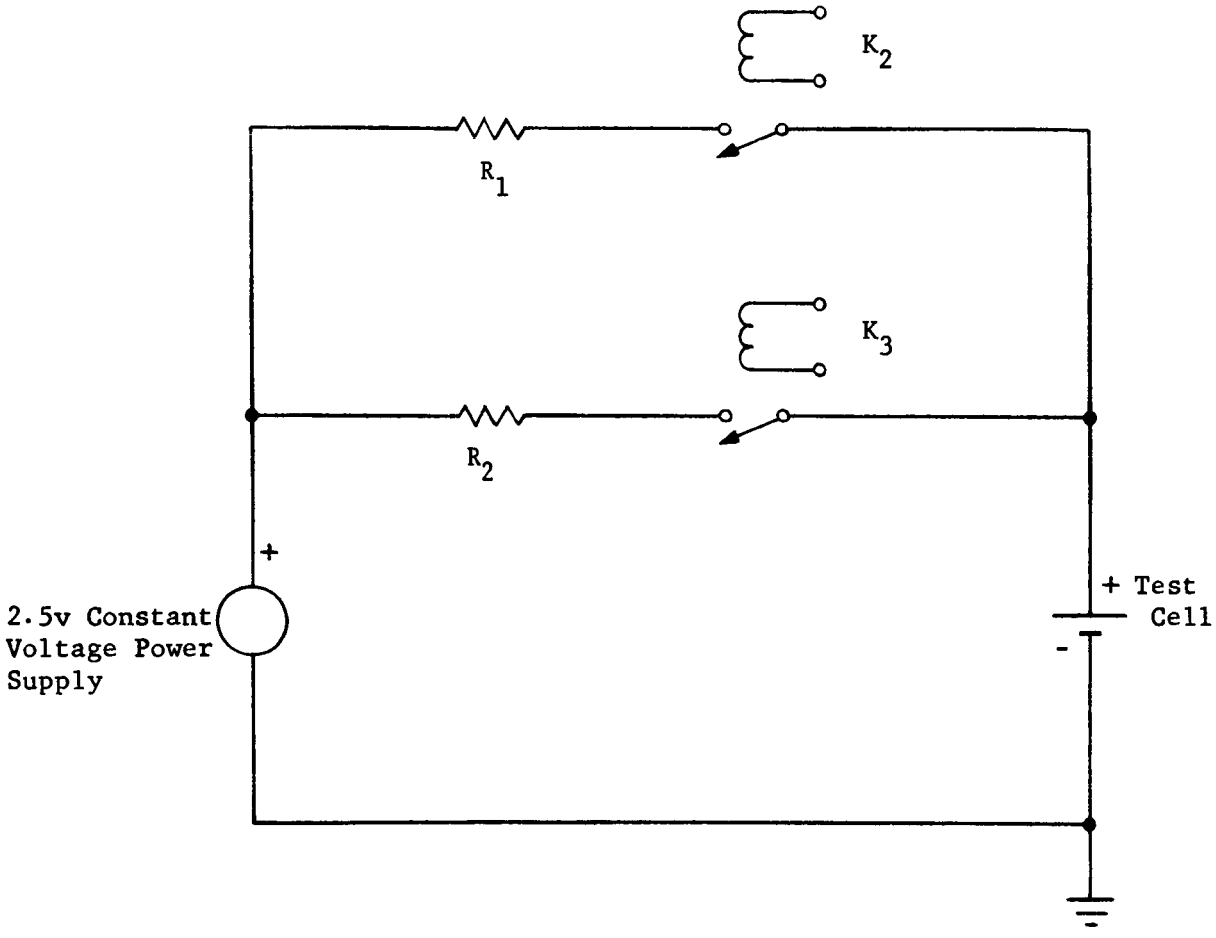

Figure 3-5 Task 3 Modified Constant Potential Charge Circuits

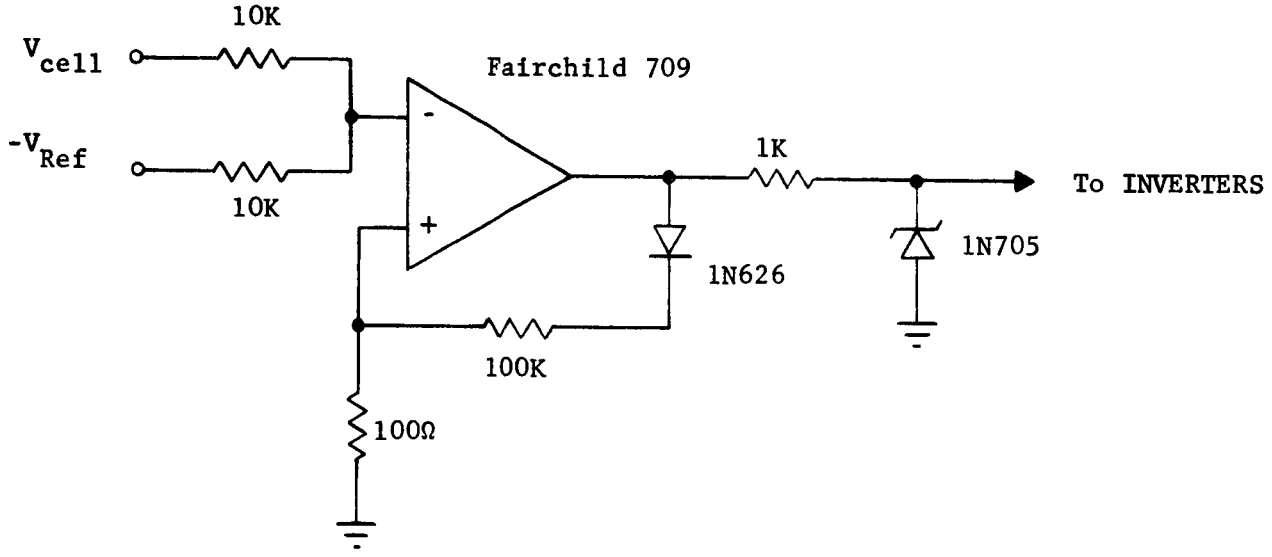

Figure 3-6 Task 3 Level Sensor

voltage input. The rise and fall times for the output are on the order of 200 nsec. The cell voltage to be measured is compared to a reference voltage which is equal in magnitude but opposite in sign to the cell voltage. These voltages are summed at the inverting input to the amplifier. The amplifier output is positive when the magnitude of the reference voltage is greater than the cell voltage. The amplifier output is negative when the magnitude of the reference is smaller than the cell voltage. A 4.7 volt zener diode on the output adapts the amplifier output to the necessary logic levels. Referring now to the complete logic diagram for Task 3 shown in Figure 3-7, the voltage level sensors are shown at the left, and the other functions are labeled across the top and bottom of the diagram.

The inverters (actually 1 input NAND gates) fed by the level sensor outputs are used to provide the correct phase of the level sensor output and also reduce the fall time of the output signals to $\sim$ 50 nsec as required by the logic. The output of each level sensor is used to trigger a monostable multivibrator. The monostable vibrator produces a pulse to trigger the binary counter. The output of each monostable is connected to a negative logic NOR gate in such a way that an output pulse from any monostable produces an output pulse from the NOR.

The binary counter is used to count the number of signals received from the level sensors and timing circuits and thereby keep track of the tests during the course of the test program. The counter is reset to zero at the start of the program. The program is manually started with a switch which places a 00001 in the counter. In the final breadboard, the program will be initiated by the completion-of-test pulse from Task 2. Any time a level sensor indicates that the cell has reached the preset

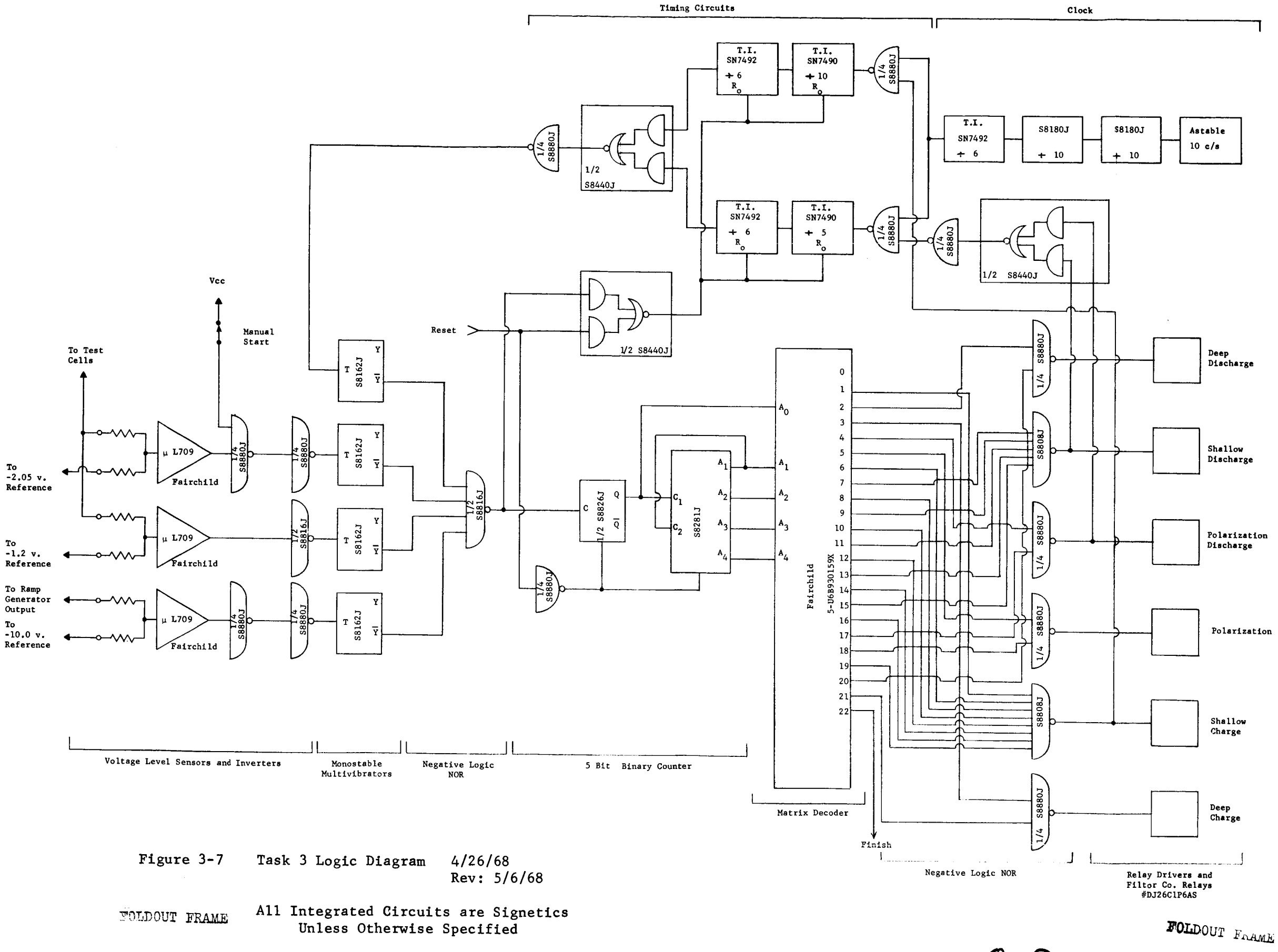

Figure 3-7 Task 3 Logic Diagram 4/26/68
Rev: 5/6/68

FOLDOUT FRAME All Integrated Circuits are Signetics Unless Otherwise Specified

58-A

58-B

FOLDOUT FRAME

level, another count is added to the counter. When one of the timing circuits produces an indication of the completion of an elapsed time period, the counter advances one count. Therefore, the binary number present in the counter at any given time uniquely describes the test that should be in progress.

The number in the counter is used to control the test sequence by decoding it in a matrix decoder composed of 5 Fairchild 9301 1 of 10 decoders. This matrix has 32 outputs. When a particular number is present in the counter, a particular output of the decoder is activated. When the counter proceeds from binary zero to binary 32, the 32 outputs of the decoder are serially activated with only one activated at a time. A table of the test steps initiated by the various binary inputs to the matrix decoder is given in Table 3-1.

Each test function is assigned a negative logic NOR gate. This gate produces an output signal whenever any one of the inputs is activated. By connecting the proper decoder output to the proper NOR gate, the test sequence is established. For example, the first three outputs of the decoder are connected to the shallow charge, deep discharge and deep charge NOR gate. This means that binary number 1 will be a shallow charge, binary number 2 a deep discharge and binary number 3 a deep charge.

Each NOR gate activates a relay through a relay driver circuit. The contact closure on the relay activates a specific cell test. A 20 second time delay is built into each relay driver so that 20 seconds elapses between the activation of the NOR gate and the contact closures. This gives the test cell a recovery period in which the open circuit cell voltage can be measured.

Table 3.1 Test Steps Initiated by Various Binary Counts at Input of Matrix Decoder

Binary Count	Test Step
00000	Reset-None
00001	Shallow Charge
00010	Deep Discharge
00011	Deep Charge
00100	Polarization Discharge
00101	Polarization
00110	Shallow Charge
00111	Shallow Discharge
01000	Shallow Charge
01001	Shallow Discharge
01010	Shallow Charge
01011	Shallow Discharge
01100	Shallow Charge
01101	Shallow Discharge
01110	Shallow Charge
01111	Shallow Discharge
10000	Shallow Charge
10001	Polarization Discharge
10010	Polarization
10011	Shallow Charge
10100	Deep Discharge
10101	Deep Charge
10110	Finish-End of Test Signal

The shallow discharge and polarization discharge steps are both constant current discharges that proceed for 30 minutes. The shallow charge rate has a time override of 60 minutes. These timed sequences make a clock necessary.

The clock which is shown at the upper right is an astable multivibrator operating at 10 Hz. Three integrated circuit frequency dividers with a division of 600 are used to provide an output with one count per minute. Two timing circuits are provided. One has a frequency division of 30 to provide an output pulse after an elapsed time of 30 minutes and the other has a frequency division of 60 to provide an output pulse after 60 minutes when fed by the clock. The clock is connected to the two timing circuits through two NAND gates. Activating the input to the NAND gate, gates the clock signal into its respective timing circuit. After the specific 30 or 60 minute delay, an output pulse from the time circuit (through an OR function) triggers the binary counter to the next count and the next test. The inputs to the 60 minute NAND gate are connected to the output of the shallow charge NOR. The input to the 30 minute NAND is derived from and OR function which is actuated by an output signal from either the shallow discharge NOR or the polarization discharge NOR.

Most of the integrated circuits used are manufactured by Signetics Corp. though a few Fairchild and Texas Instruments units are used. The Signetics units are part of their S8000J series and all are compatable. A list of the devices used is given in Table 3-2.

Table 3-2 Integrated Circuit Logic Units

Manufacture	Quantity	Type	Function
Signetics	4	S8162J	Monostable
	2	S8280J	Decade Counter
	1	S8281J	Binary Counter
	2	S8440J	AND-OR-INVERT Gates
	4	S8808J	NAND Gate
	1	S8816J	NAND Gate
	1	S8826J	J-K Binary
	2	S8880J	NAND Gate
Fairchild	3	709	Operational Amplifier
	4	9301	1 of 10 Decoder
Texas Instruments	2	SN7490N	Decade Counter
	2	SN7492N	Divide by 12 Counter

These units are designed for the temperature range from -55°C to +125°C. In addition, the Signetics units are tested on a 100% basis for thermal shock and to 30,000 g in a centrifuge test.

3.3.3 Results and Status

The sequential test logic described above has been built on a preliminary breadboard and is operating satisfactorily. The power dissipation is on the order of 2.5 watts not including a relay which requires 225 mw. The logic is relatively insensitive to noise when it is unshielded and open on a bench top. It is somewhat susceptible to strong local field such as those produced by an electric drill operating within a few inches of the circuit and on the same power line. This is considered to be a rather severe noise source. The circuits are presently being incorporated into a shielded box in order to increase the noise immunity.

The voltage ramp generator and discharge current control circuitry has been used with Task 3 cells with satisfactory results. As soon as the noise immunity tests are completed, the logic, discharge circuits and charge circuits will be combined so that a complete sequence of tests can be made on Task 3 cells automatically.

3.4 Conclusions

The control systems for Tasks 1 and 3 and the switching logic for Task 3 have been built and separately tested. All have been operated to their design specifications. The Task 3 control system and switching logic have not yet been operated together but this should be accomplished by June 1.

The logic for Task 1 should be quite similar to the logic for Task 3 except that it will be much simplier since there are fewer specific test functions in Task 1. The logic for Task 2 should be similar also but the requirements are less clear at this time.

There will also be logic and switching involved in the changing of test cells in all tasks as well as changing the tasks themselves. This logic will be similar to the Task 3 logic and use primarily the same types of components.

3.5 Recommendations

The major design work that remains to be done is the logic involved with the Task 2 test. This will be reported in the next quarterly report. The tape recorder control will also be designed during the next quarter.

An important item which will be covered during the next quarter is a failure analysis of the test cells and the various circuits so that appropriate steps can be taken to design fail safe features into the breadboard.

4.0 Tape Recorder Selection

4.1 Introduction

An essential part of the breadboard unit for the Reduced Gravity Battery Test Program is the tape recorder. Since tape recorders qualified for space use are expensive instruments, and development of special tape recorders for space use is even more so; in the interest of economy certain constraints have been imposed on the choice of a tape recorder for the breadboard. A basic premise adopted in this program was to design the breadboard around an existing model of a flight qualified recorder. This would insure a minimum of changes when a subsequent flight model of the breadboard unit was designed and built. Another restriction was to employ a suitable commercial type of tape recorder with the breadboard as a substitute for the recorder to be used in space flight. This was desirable because of the approximately 5x greater cost of the flight qualified type and the fact that the breadboard model will not be flown.

These constraints required that a commercial quality tape recorder be found for the breadboard unit which could be used to simulate the performance of the flight qualified type.

In order to permit a rational choice to be made, two parallel surveys have been conducted to gather data on available tape recorders. The first covers tape recorders for space use and the second covers commercial types. This section reports on the findings of these surveys and makes recommendations concerning the tape recorder to be purchased for use in the breadboard. It also contains descriptive information and specifications of the tape recorder which could be employed in the flight model.

4.1.1 Flight Recorder Requirements

The recording is to be made so that it can be retrieved manually at the end of the flight by an astronaut together with a photographic film cartridge used to record gas-liquid phase distribution in Task 2 tests. It is desirable that the entire tape recording be on one reel or cartridge and that the system require a minimum of attention by the astronaut. The recorder is not required to operate at launch but must withstand the launch environment. The recording is to be made only during orbit under the zero or low gravity conditions existing during corrections in the flight path.

It is required that the entire battery test system operate using a maximum of 50 watts of power for all operations. It is desirable that the tape recorder use only 10 watts of power at 28 volts dc. Basic environmental operating conditions are 70°F in a mixed atmosphere of oxygen and nitrogen at 5 psi. Final environmental specifications are not yet available for the flight unit. However the following specifications are to be taken as typical of the type of application and as guides in specifying requirements.

The system design shall have the objective of meeting the environmental requirements as set forth in JPL specification 30250B, entitled "Environmental Specifications, Mariner C Flight Equipment," dated March 15, 1963, including amendment No. 1 dated October 11, 1963; amendment No. 2 dated January 29, 1964 and amendment No. 3 dated April 22, 1964.

Parts and processes shall conform to requirements set forth in JPL specifications 30261, entitled "General Specification, Materials, Processes and Hardware Equipment," dated June 7, 1962, including one (1) amendment,

20028, entitled "General Specification Terminal Board Fabrication," dated August 16, 1960, including one (1) amendment and Change B, and ZPP2061 PPL, entitled "JPL Preferred Parts List," dated July 1, 1966, including Letter Change H.

4.1.2 Breadboard Unit Recorder Requirements

This is to be a commercially available laboratory tape recorder preferably in a portable or semi-portable version. It will be used only in a terrestrial laboratory environment and powered by 115 volts, 60 Hz without any limit on power consumption. A prime consideration is that its mechanical and electrical operating characteristics should be as functionally similar as possible to those of the flight recorder. A recorder of this type costs ~ $10,000 in contrast to ~ $50,000 for a flight qualified type.

4.1.3 Measurement Requirements

The three tasks outlined in the work statement have determined what parameters are to be measured. All required measurements can be made on a 7 channel recorder. These are shown in Table 4-1. The only parameter that differs greatly from task to task is the current to be measured on the charge and discharge cycles. Proper shunt resistors will be used in each circuit to provide ~ 40 millivolts at the maximum permissible current. Tasks II and III will require several shunts to cover the current ranges. The reference electrode on the cells in Tasks I and II requires a high input impedance (1 megohm) voltage measuring system but this same system can be used on Task III. All voltage measurements are in the range of 0 to 2.1 volts. Temperature measurements will be made over the range of ambient to 70°C. This will require measurement of voltages in the range of about 200 millivolts. Channel 5 is reserved for speed compensation and Channel 6 will record the test identification. The test identification

will be provided by serial binary coding of the task number, cell number, and test event.

Table 4-1 Recorder Measurement Requirements

Channel No.	Input Rating	Function	Task Requirements I	II	III
1	0 to 5V @ 1 MegΩ	Zn-Zn (ref) Volts	1.2	1.2	2.1
2	0 to 5V@ 1 MegΩ	Ag-Zn (ref) Volts	2.2	2.2	
3	0 to 40 mv	Current	200 ma	20 ma	15A(max)
4	0 to 400 mv	Temperature	Amb.	x	70C
5	0 to 5 volt	Speed Control	x	x	x
6	0 to 5 volt	Test Coding	x	x	x
7	0 to 5 volt	Spare	x	x	x

The recording test schedule for each task is summarized in Table 4-2. The schedule is still subject to modification and it is presented to show the relative duration of each of the tasks and main events in the test tape recording program. The short duration tests will be recorded continuously. The longer duration tests will be recorded by sampling measurements taken at 1 minute intervals. A 10% duty cycle is used for the sampling calculations. This allows 6 seconds of equivalent tape time in each sample measurement for the start-stabilize-measure-stop function. Thus each sample in the test requires 1/10 minute of equivalent tape time.

4.2 Technical Discussion

It is the purpose of this section to present the technical considerations pertinent to the recording requirements of these tests. Reference is made to Application Note 89 published by the Hewlett Packard Company titled "Magnetic Tape Recording Handbook" for general tape recording information.

Table 4-2 Recording Test Schedule Summary

Event	Task I Minutes	Task II Samples	Task II Minutes	Task III Samples	Task III Minutes
Calibration	1		1		1
Charge Cycles		1260		1035	
Discharge Cycles		120		210	
Polarization Meas.			10		10
Capacity Meas.				360	
Lim. Cur. Dens. Vert.	8				
Lim. Cur. Dens. Horz.	11				
Total, Per Cell	20	1380	11	1605	11
No. of Cells	6	2	2	6	6
Total	120	2760	22	9630	66
Equivalent Minutes	120	276	22	963	66

Total Tape Time = 1447 Minutes (24.1 hours)

Of the three basic recording methods; direct, frequency modulation (FM), and digital; the FM method has been selected for these measurements. Direct recording is not applicable to d-c measurements, and digital recording while applicable, is considerably more expensive than FM. A 7 channel recorder using 1/2 inch tape fits well with the data requirements listed in Table 4-1. Channels 1-4 are used to record the measurands and therefore require more accurate electronics than Channels 5-7 in which the signal magnitude is not of prime importance.

The test schedule in Table 4-2 when run on a continuous basis will require 210 hours or approximately 8.5 days. Such long duration tests logically require

the sampling method which reduced the equivalent tape time required to 24.1 hours. The lowest tape speed normally available on laboratory recorders is 1 7/8 inches per second (ips) which is equal to 1.75 hours per 1000 feet of tape. This would require 13,000 feet of tape for the complete schedule. At the 15/16 ips. speed available on special order on some recorders, the requirements are 6500 feet. This compares to a typical tape capacity for a flight qualified recorder of 500 feet. Thus to stay within available tape capacities, lower tape speeds must be employed. A tape speed of~0.1 ips fits the needs of this application.

The principle reason why most flight recorders are limited to a few hundred feet of tape capacity is that the large shock and vibration forces to which they are subjected present design problems on large heavy reels. Another reason is that most recorders are designed only for orbital tape capacity, and the tape is an endless loop which is telemetered to ground stations and erased once every orbit. The maximum flight recorder tape supply found in the survey was 1750 feet and that was on a recorder not suited to the application.

It is important in FM recording that the carrier frequency have a fixed relationship to the tape speed. The IRIG (Inter Range Instrumentation Group) standards are stated in the Application Note 89 previously cited on page 2-8. Table 4-3 provides an extrapolation of these values to the low tape speeds needed in this application. When these standards are followed, it is possible to reproduce an FM recording made at one tape speed e.g. 0.06 ips at a higher speed such as 1 7/8 ips either on the same recorder or another FM recorder without using special electronics.

The main penalty paid for use of the lower tape speeds is the lower

frequency response obtained. However in the present application all data recorded is essentially DC so that the frequency response listed in Table 4-3 for even the lowest tape speed would be adequate.

An advantage of FM recording is that is is readily adaptable to an analog readout of the test results for a visual analysis. It can be reproduced in analog form on a multi-channel strip chart recorder. The chart speed of the strip chart recorder can be operated at whatever speed is appropriate for the reproduce speed selected on the FM recorder. This provides a wide choice in the time scale selected for the analog presentation.

Table 4-3 Single-Carrier and Wideband Fm Record Parameters

Tape Speed Low Band (ips)	Relative Speed Factor	Carrier Center F (Hz)	Modulation Frequency (Hz)
3 3/4	62.5	3375	DC-625
1 7/8	31.2	1688	DC-313
15/16	15.6	844	DC-156
15/32	7.8	422	DC-78
0.1	1.7	90	DC-17
15/160	1.6	84.4	DC-16
0.06	1.0	54	DC-10
0.03	0.5	27	DC-5

By way of contrast, it is worth considering briefly the characteristics of an incremental digital tape recorder. In this type, all input data is converted to binary code which is then recorded in serial fashion on tape. It is essentially a sampling or commutating system although sampling rates can be quite high, and a very large number of variables can be recorded on a single channel in sequence. This type of recorder is very efficient

regarding tape utilization since tape transport occurs only during the recording of a data word. With a suitable choice of format, such tapes can be made computer compatable, that is they can be read directly into a computer program for data processing. This is particularly advantageous where much data is being handled and calculations or corrections are to be made on the recorded data. To obtain an analog plot from the data, suitable plotting routines would have to be programmed into the computer.

In the present application, the small number of variables, the low frequency response requirements, and the requirements for analog output presentations against a time scale do not represent a good fit with the characteristics of an incremental digital recorder. Only a small fraction of the capabilities of such an instrument would be utilized and the cost would be significantly higher than the sampled FM system. However, if it becomes apparent later that a suitable digital recorder could be time shared with other experiments during the flight, it may be worth re-examining the recorder choice made here.

The main reason for sampled recording in the breadboard unit is to simulate flight recording conditions and their reproduce requirements. A two second stabilized measurement "on" time recorded at 0.06 ips would be a 2/31 second "on" time when reproduced at 1 7/8 ips. (See Table 4-3). Any critically damped multi-channel strip chart recorder having a frequency response of 40 Hz or more would be satisfactory for use at speeds up to 3 3/4 ips. Figure 4-1 shows a representative bar graph curve plot such as that which would be obtained from a sampled recording reproduced at a continuous speed. The time axis is a function of tape speed and chart speed. Speed settings can be made such that the bars merge into a solid block of

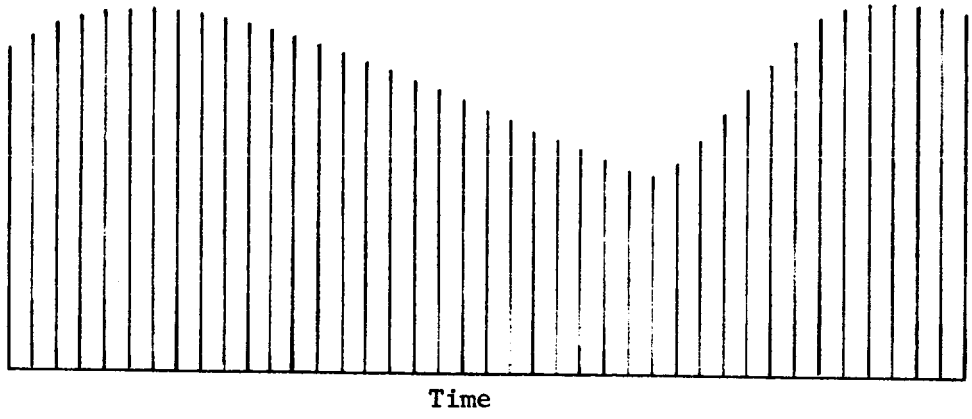

Figure 4-1 Bar Graph Sampled Data Presentation

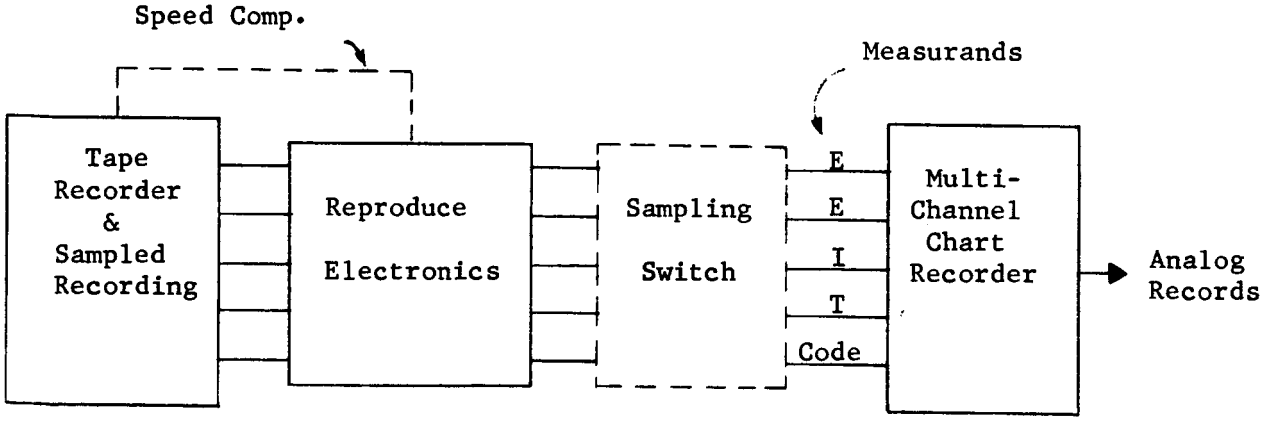

Figure 4-2 Recording-Reproduce System

the pen color and the curve is the chart-ink demarcation line.

Figure 4-2 is a functional diagram of the reproduce system for a sampled or continuous recording. The reproduce electronics are often part of the FM record - reproduce equipment. Speed compensation may not be required but the steady frequency recorded on Channel 5 can be used if required. The sampling switch would be used only on the sampled recordings.

4.3 Recorder Survey

An extensive survey was made of space qualified and commercially available recorders for both the flight and breadboard applications in both FM and digital versions. Manufacturers actually surveyed for the breadboard unit recorder were:

A & D Data Systems, Inc.	*Geo Space Corporation
Ampex Corporation	Hewlett Packard Company
*Astro Science	*Leach Corporation
Beckman Instruments	*Lockheed Electronics
Consolidated Electro Dynamics Corp.	Parsons Electronics Company
Digi Data Corporation	Precision Instruments Company
Fairchild-Winston Company	*Sanders Associates
Geotech-Teledyne Company	Sangamo Electric Company

Those marked with an asterisk were also surveyed for their flight recorders. In addition, Cook Electric Company and Kinelogic Corporation were surveyed for flight recorders. Table 4-4 summarizes the characteristics of four recorders representing four different categories of laboratory type magnetic tape recorders. The low speed FM recorder listed is the best surveyed in that category. The portable FM recorder is representative of the best surveyed in that category. The semi-portable FM recorder

Table 4-4

Summary of Laboratory Recorders

Item	Frequency Modulated			Digital
	Low Speed Geotech Model 17373	Portable Lockheed Model 417	Semi Portable Consol.Electro. Model VR-3300	A & D Data Sys. Special 10M
Size (in.)	18.5x22x8	14x15x6 1/2	22x16x30	22x26 1/2x42
Weight (lbs)	36	30	186	200 est.
Channels	7	7	7	5
Speed (ips)	0.06	15/16 spec.	15/16	incremental
Tape Cap. (ft)	7200	3100	4600	2000
Record Time (hrs)	400	11	16	48
Start/Stop (sec)	10/20	5/5	3/1	N.A.
Speed Acc (%)	0.25	0.25	0.25	N.A.
Flutter (%)		2.0	1.2	N.A.
Linearity (%)	0.1 & 1.0	1.0	0.5	N.A.
S/N Ratio (db)	40	34	36	
Signal Volts	0.04-5.0	1.4	0.5-10.0	0.05
Power (watts)	21	13	450	
Cost ($)	9,000	10,000	11,500	12,500
Delivery (days)	60	60 est.	90	60

is representative of the type made by several manufacturers such as Ampex Corp., Hewlett Packard Company and Sangamo Electric Company in addition to the Consolidated Electro Dynamics Corp. model listed.

Table 4-5 summarizes the specifications on the two basic types of recorders applicable to flight conditions. The FM miniature model made by Cook Electric operates at the same speed (0.06 ips) as the Geotech Model 17373 and has very similar FM electronic characteristics. The Cook Electric FM miniature recorder has the FM carrier frequency recorded in one channel so that speed compensation for flutter correction is available. Their recommended reproduction unit is the Precision Tape Recorder Model PS-207A at 3.75 ips. A signal/noise ratio of more than 35 db is available on compensated reproductions.

The digital recorder listed is a special start-stop Kinelogic model for this application that would be housed in their RSL case. The long recording time required presents similar procurement limitations in both the FM and digital recording methods.

4.4 Summary

The analysis of the magnetic tape recorder requirements for the Reduced Gravity Battery Test Program in relation to the survey of commercially available recorders is summarized in the following statements.

a) A major consideration in the flight recorder is the long duration (8.5 days) of the test and the proper use of the available recorder tape supply to accommodate the test program. It has been shown that a combination of continuous and sampled measurements can provide the test information and that suitable FM and digital flight recorders are commercially available.

Table 4-5 Summary of Flight Recorder Characteristics

Item	Freq. Mod. Cook Electric FM Miniature	Digital Kinelogic Model RSL(spec.)
Size (in.)	8 x 11 x 2.25	6 x 5 x 5
Weight (lb.)	5	5.5
Channels	7	5
Power (watts)	3	6
Speed (ips)	0.06	4
Tape Cap. (ft.)	580	400 actual 4800 equiv.storage
Bit Capacity		2.9×10^8
Record Time (hr.)	29	50 max.
Start (sec.)	0.1	0.1
Speed Acc. (%)	1.0	0.5
Linearity (%)	0.75	
S/N Ratio (db)	25*	
Signal Volts	0.04	0.05

*without speed compensation

b) FM recording presents the most economical visual analog readout possibilities and it is available in a space flight proven unit.

c) The advantages of digital recording could not be fully utilized with the modest data capacity requirements of this program alone. However it may be worth considering if a digital recorder could be time shared with other experiments in space. Use of digital recording requires computer processing of data and suitable computer programs for plotting the results.

d) A commercial FM recorder is available for the breadboard test unit that is compatable in tape speed and FM electronics with that required for the flight recorder. It also has a tape supply that will accommodate the entire breadboard test program on a continuous measurement basis when it is required.

e) A commercial incremental digital recorder is available that will record the entire breadboard test program. It will require the use of considerable "in house" computer facilities and programming for analysis of test results.

f) The use of a commercial laboratory recorder for the breadboard unit presents a cost advantage of several fold over the use of a qualified flight recorder.

4.5 Conclusions and Recommendation

The FM magnetic tape recorder when used in the combination of continuous and sampled measurement recording fulfills all the task requirements at the lowest investment cost and requires the least additional reproducing equipment. Compatable low speed FM tape recorders are commercially available for both the breadboard unit and flight application. It is recommended that the Geotech Model 17373 magnetic tape recorder be obtained and used as the recorder for the breadboard unit.

SECTION III - CONCLUSIONS

The use of stepwise current increases to obtain polarization data on the Task 1 cell has given inconsistent results in the tests performed. In contrast, good repeatability was obtained using a current ramp circuit to control discharge current from the cell. Analytical and experimental results indicate that the current ramp slope is an important parameter which must be considered in the overall experiment design. Where convection occurs in the cell, use of too large a value of current ramp slope suppresses the effect of convection which has a certain characteristic time response.

As a result of exploring the effect of ramp slope on limiting current density (LCD) values using cell orientations where convection was either favored or suppressed, it appears that most information would be obtained from an experiment where two different ramp slopes were used. One value being used for 1 g tests, and the second or lower value being used for the 0-g test. Such an arrangement has the added advantage of permitting matching the discharged capacity of electrodes in the two tests.

At present, because of some minor equipment limitations, we have not covered the full range of current ramp slopes of interest for the two cell orientations. Therefore, we do not have complete experimental verification of the analytical predictions. In particular more experimental work is required using a horizontal electrode simulating the zero gravity condition.

In the Task 3 testing of commercial Ag-Zn batteries, it is concluded that a 5 AH capacity is the largest that can be handled within the power restrictions being observed for the breadboard.

The Yardney HR5-DC-7A has been selected as the commercial cell to be tested in this experiment. This battery has been subjected to a cyclic charge-discharge test using a 35% depth of discharge. These tests showed a smaller loss in capacity than would be desirable in the experiment and future testing will be done at higher depth of discharge. An initial deep discharge made at the beginning of the test sequence to measure cell capacity was done at too low a discharge rate with the result that the apparent capacity measurements exceeded the rating of the cell by a factor of approximately 2. In future tests of this type a higher discharge rate will be employed.

Another defect uncovered in this first test sequence was the inadequacy of a polarization test on this type of battery when the current was limited to 10 amps max. Tests to this current level were insensitive to any changes which occurred in the cell. In future tests, we intend to raise the limit to 15 amps in hopes of raising the sensitivity of the polarization test as an indicator of cell damage.

As a result of an investigation of switching method alternatives it is concluded that a system using available digital integrated circuit logic components combined with relays for handling current offers the advantages of reliability, light weight and power consumption, and flexibility in the programming of experiments. Additionally a digital system of the type proposed has the advantage of "built in" test codes which can be readily recorded on tape along with cell data for test identification purposes. A bench top model of both the logic circuits and the test control circuits for Task 3 has been built and successfully tested. These circuits are representative of those needed in the other tasks also.

A survey of available tape recorders both for flight use and for use with the breadboard indicates that a seven channel F.M. system with low tape speed (0.06 ips) operated intermittantly best suits the needs of this test series. Suitable models of this type of recorder are available for flight use, as well as a commercial version suitable for use in the breadboard model. The latter, Geotech Model 17373, has adequate tape capacity for continuous recording if this should become desirable.

SECTION IV - RECOMMENDATIONS

In the tests of the research cell in Task 1 it is recommended that limiting current density be measured using the current ramp approach, and that ramp slope be adjusted for tests at 0 and 1-g to yield approximately the same discharge depth of the anode at the limiting current density.

In the Task 3 experiment, it is recommended that further testing be deferred until a bench top model of the logic and control circuits is completed. Then further testing can be done concurrent with evaluation testing of the circuits. Additional testing should be done using greater depth of discharge in the cyclic charge-discharge portion of the test in an effort to increase the loss of capacity to approximately 30%. Other changes from the initial test procedure which are recommended include:

a. The use of greater current levels during the initial and final deep discharge cycle used to determine capacity.

b. The use of the current ramp approach for measuring polarization of the cell.

c. Raising the current limit during the polarization measurement from 10 to 15 amps to determine if this will make the polarization measurement more responsive to cell degradation.

It is recommended that the logic and control system used to conduct the test sequence be designed using available digital integrated circuits combined with relays to accomplish switching where necessary.

The Geotech model 17373 appears to be the commercial instrumentation recorder best suited for the needs of the breadboard model. It is recommended that one be purchased for this project.

SECTION V - NEW TECHNOLOGY

There are no "New Technology" items to be reported at this time.