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STUDY OF FAILURE MODES OF MULTILEVEL LARGE SCALE INTEGRATED CIRCUITS

May 1968

Prepared Under Contract NAS12-544
by
Philco-Ford Corporation
Microelectronics Division
Blue Bell, Pennsylvania

Electronics Research Center

NATIONAL AERONAUTICS AND SPACE ADMINISTRATION

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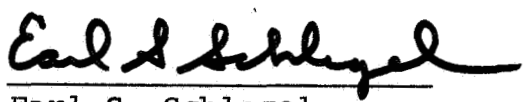
National Aeronautics and Space Administration
Failure Mechanisms Branch
Qualifications and Standards Laboratory
Components Research
Cambridge, Massachusetts 02139

Interim Scientific Report No. 2

This report describes studies performed in accordance with Contract No. NAS12-544, dated April 15, 1967, and Modification No. 1 to that contract, effective October 15, 1967. The report covers work performed between October 15, 1967 and April 14, 1968.

Submitted by:



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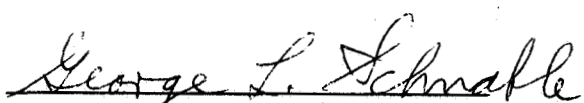

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CONTENTS

CONTENTS (Continued)

LIST OF ILLUSTRATIONS

LIST OF ILLUSTRATIONS (Continued)

SUMMARY

Empirical and theoretical investigations have resulted in techniques for improving the reliability and performance of large-scale multilevel microcircuit arrays. The detailed behavior and effects of surface ions have been measured as a function of applied voltage, temperature, time, humidity and the testing history of the device. The model for surface ion behavior has been extended to include the case in which the surface ion density is a function of the surface potential of the oxide. Vapor deposited oxides have been extensively studied to establish their value as second-layer oxides for multilevel microcircuitry. The use of phosphorus as an additive to vapor plated oxide layers has been shown to improve the reproducibility and the stability of the electrical properties of vapor plated oxides.

A broad review has been prepared of each of the factors that should be considered in a program to develop and produce highly reliable large scale multilevel microcircuit arrays. A number of ways are suggested for including test structures in production microcircuit wafers for process control, and for analyses of yield and reliability problems.

INTRODUCTION

Large-scale integration (LSI) offers the potential of improving the reliability, cost, and performance of complex electronic systems containing silicon integrated circuits. LSI circuit arrays containing thousands of components will have multilevel metalization patterns in contrast to currently used integrated circuits, both bipolar and MOS, which contain a single-level metalization pattern over a thermally-grown SiO_2 layer. Therefore, multilevel LSI arrays require additional processing steps for dielectric deposition and photolithographic delineation and for second metal layer deposition and delineation. These additional steps, and the procedures and conditions by which they are accomplished, can produce significant changes in the electrical performance and reliability of silicon integrated circuits.

A necessary part of the successful development of LSI circuitry is the development of practical means for insuring the highest level of reliability. This reliability is affected by metal and contact problems and by factors that influence the fundamental properties of the insulator-silicon interface. This report presents the results of a program to investigate techniques for improving the reliability and performance of large-scale multilevel arrays by improving the fundamental properties

and the stability of the insulator-silicon interface.

The fabrication of large-scale multilevel arrays requires a number of new materials and fabrication processes. Different materials and processes must be used to form a second or third insulator layer than those used to form the first insulator layer. The first layer is formed by thermal oxidation of the silicon in order to form an insulator-silicon interface with a low density of surface states. Additional insulator layers can only be formed by techniques other than thermal oxidation because they must overlie metal in some areas, and because the temperatures required for thermal oxidation are well above the aluminum-silicon eutectic temperature (577°C). The new processing steps, materials, and processes can introduce failure modes that are entirely new, and they can cause previously recognized failure modes to appear more frequently. The probability of failure may increase because of a decreased stability, or because of a change in the initial characteristics which provides less tolerance for instability.

It is the purpose of our investigation to uncover all of the potential surface-related failure modes of multilevel LSI circuitry and to develop techniques for minimizing the probability of their occurrence. An important part of this work is the development of sensitive techniques for detecting and for measuring each of the types of instability that are known to

degrade LSI circuits. The results of the program will be applicable to both MOS and bipolar arrays.

The First Interim Report, dated November 1967, covered the following:

1. A basic understanding of the fundamental electrical properties of the Si-SiO_2 interface of structures having a dielectric layer over delineated metal layers in multilevel microcircuit structures.
2. A useful model which provides an overall view of all of the influences on these electrical properties.
3. A number of oxide layers of various materials and deposited by various processes were experimentally evaluated for their possible use as second-layer insulator materials for multilevel LSI circuitry.
4. Feasibility was demonstrated for a set of test structures, equipment, and techniques for evaluating various insulator materials and deposition processes.
5. An extensive array of data was compiled on both n-on-p and p-on-n test structures, both with and without a vapor-plated SiO_2 second insulator layer.

The work covered in the First Interim Report was basically exploratory. Problem areas were identified, and test structures, equipment and procedures were developed for studying the mechanisms associated with failure modes of multilevel LSI structures. The work covered in this Second Interim Report has been directed at the following objectives:

1. Improvement of the understanding of the detailed nature of the important types of instability.
2. Development of practical procedures for the most effective means for making sensitive measurements of the stability of devices made by various processes and of various materials.
3. The formulation of techniques for assuring the maximum reliability for LSI circuitry at the lowest cost.

In order to maintain a broad familiarity and understanding of the relevant work in this field being reported by other investigators, we continually maintain an updated bibliography of MIS studies. Appendix A is a bibliography that has been updated to April 1, 1968. Most of the papers listed were in a bibliography distributed at the 1968 Semiconductor Interface Specialists Conference in March. The paper in Appendix A has been accepted for publication in the next special MIS issue of the IEEE Transactions on Electron Devices to

supplement the paper that was published[1] in the previous special MIS issue in November 1967.

EXPERIMENTAL STUDIES

Oxide Preparation

The oxides studied in this program were prepared by techniques that were developed in connection with company-sponsored programs. These techniques are similar to those used generally in the industry. Vapor plated SiO_2 layers are prepared at 400°C by the reaction

$$SiH_4 + 2O_2 \longrightarrow SiO_2 + 2H_2O.$$

The process is relatively simple and is accomplished by placing the integrated circuit wafer on a heated substrate in a well controlled stream of SiH_4 and dry O_2 diluted with dry N_2. A reaction occurs at the surface of the heated wafer and deposits a film of SiO_2. The apparatus is shown in Figure 1. Further information on the process, and on the properties of films obtained has been published (Ref. 2,3,4 and 5).

Physical properties of these vapor-deposited SiO_2 layers that have been measured include:

Stress- - - - - - - -	3×10^9 dynes/cm^2 (tensile)
Density - - - - - - -	3.2 gms/cc
Index of refraction -	1.456 (Na_D)
Etch rate - - - - - -	80 Å/sec, at 30°C ±0.1°C, in an etchant prepared in the proportions 1500 cc DI H_2O, 1000 gms NH_4F and 275 cc HF (49%).

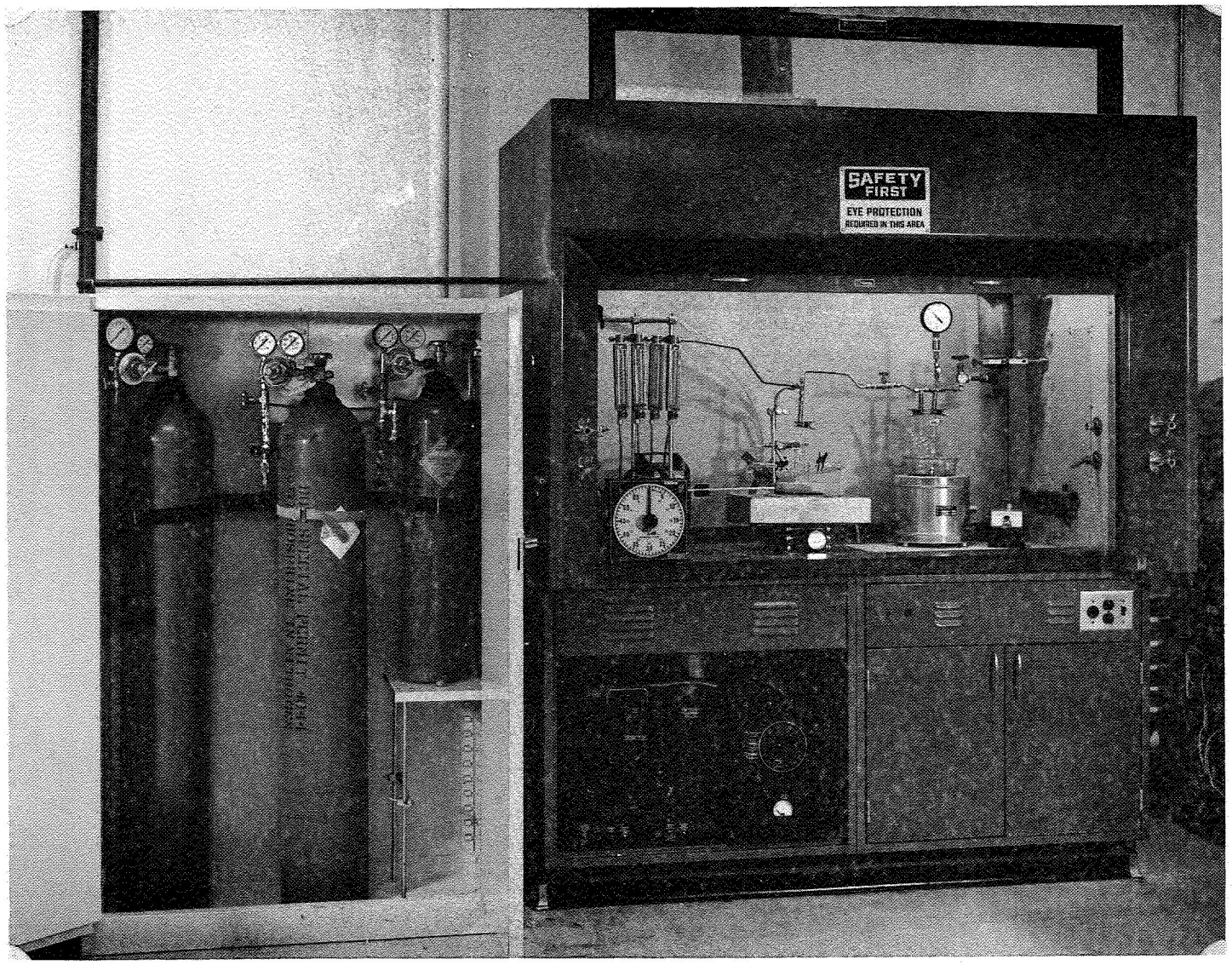

Figure 1. Vapor plating system.

Because of the well known stablizing affect of phosphorus in oxides formed at high temperatures, we have developed, on a company-sponsored program, techniques for depositing phosphorus-containing vapor plated SiO_2 at 400°C. The process is similar to that for vapor plating pure SiO_2, but with PH_3 being added to the reactant gas mixture. The proportion of the phosphorus contained in the deposited oxide is controlled by the proportion of the PH_3 in the reactant gas mixture. The percentage (weight) of the phosphorus in the deposited films was measured on an emission spectrograph and was correlated with the composition of the reactant gas mixture as shown in Figure 2.

We have measured the following physical properties of the phosphorus-containing vapor deposited films.

Density - - - - - - - - - - - 2.2 gms/cc

Index of refraction - - - - 1.50 (Na_D)

Etch rate - - - - - - - - - - 166 Å/sec*

These parameters are fairly insensitive to the phosphorus content. For that reason, we have measured the absorption of monochromatic infrared light as obtained by reflection as a function of the relative phosphorus content in the films, and as function of the thickness of the mixed oxide film. Figures 3 and 4 summarize this data. The infrared absorption technique promises to

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*In the etchant described on Page 5.

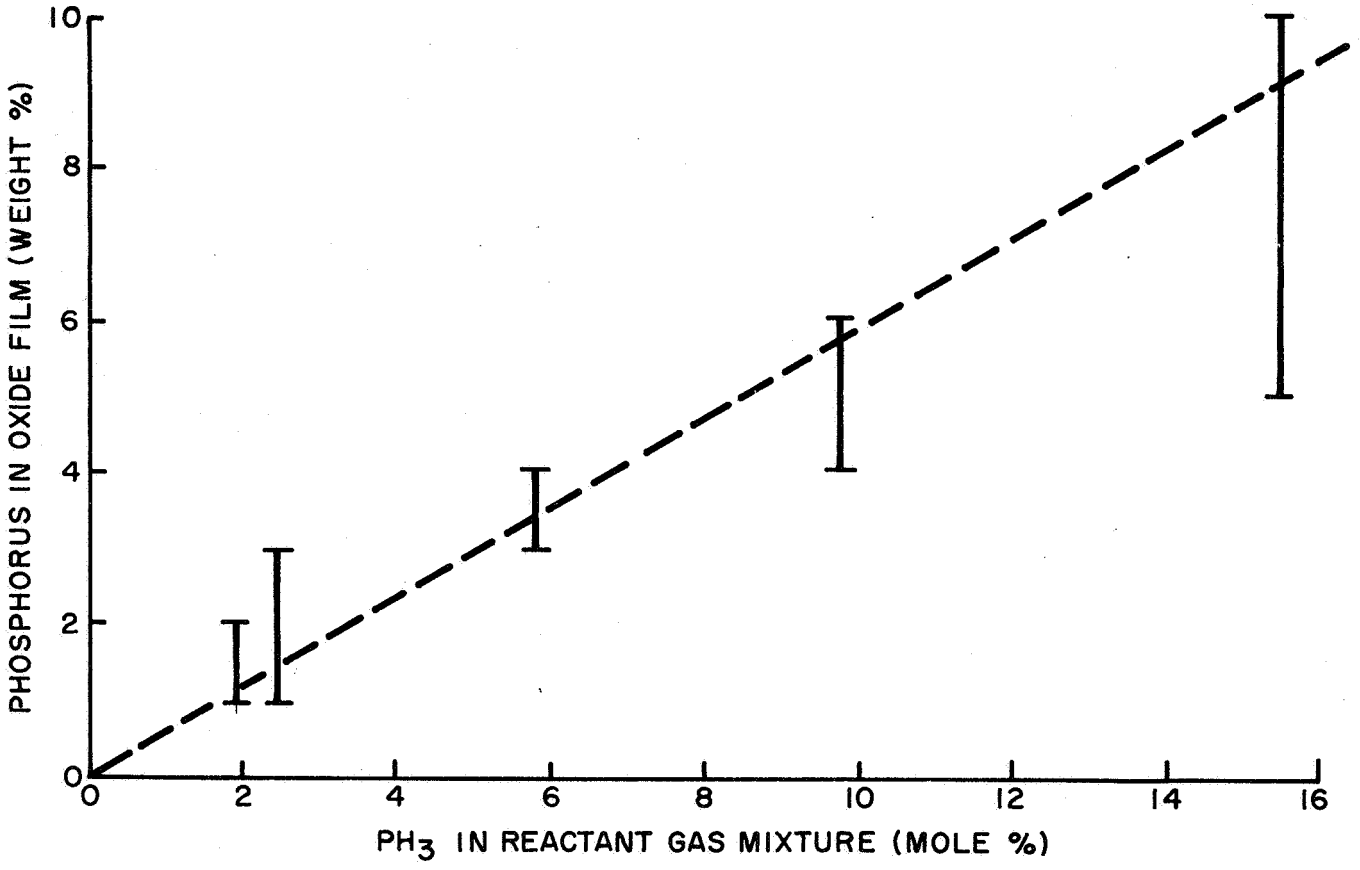

Figure 2. Phosphorus in oxide film vs. PH_3 in reactant gas mixture.

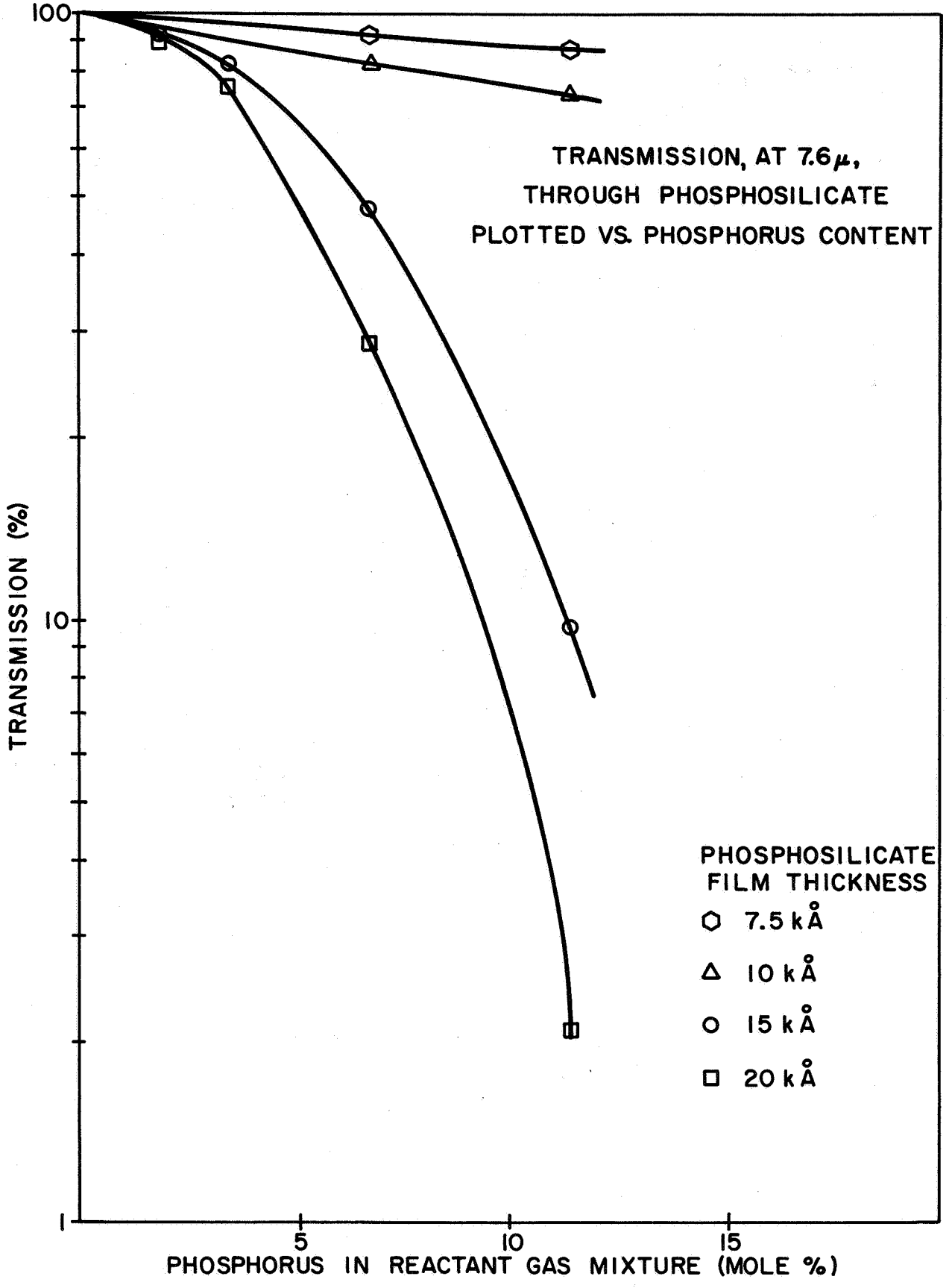

Figure 3. Transmission, at 7.6 μ, through phosphosilicate vs. phosphorus content.

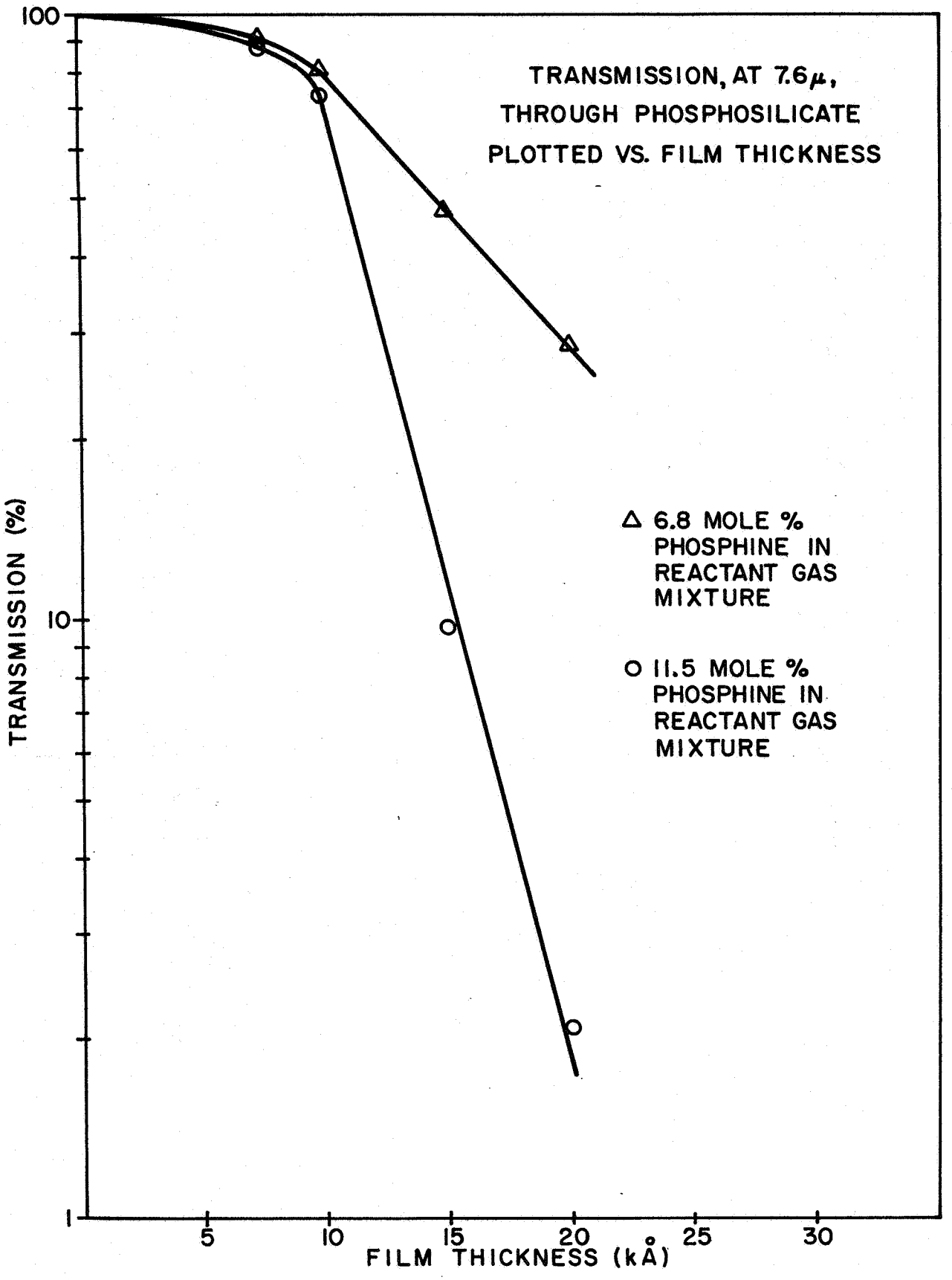

Figure 4. Transmission, at 7.6 μ, through phosphosilicate vs. film thickness.

provide a good means for monitoring and controlling the phosphorus content of the oxide layers. Nanda et al. (Ref. 6) have reported that an IR absorption line at 7.6 μ is a measure of density of P=O bonds in the oxide.

A second means for measuring the phosphorus content of the oxide involves a diffusion process. A 5Ω-cm, p-type-silicon wafer with a uniform phosphorus-containing vapor plated oxide is heated to 1200°C for 1/2 hour. The oxide is then etched away and the sheet resistivity of the n-type diffusion layer is measured with a 4-point probe. Table I gives the dependence of the sheet resistivity ρ_s, and the diffusion depth on the mole percentage of the PH_3 in the reactant gas composition. The first column in Table I gives the mole percent of PH_3 in the reactant gas mixture.

The reproducibility of the phosphorus content is indicated by the data in Table II.

The deposition of r-f sputtered oxides was discussed in a paper by Birk (Ref. 7).

TABLE I

DIFFUSION OF PHOSPHORUS INTO SILICON
FROM DEPOSITED OXIDE

PH_3 in Reactant Mixture (Mole %)	Sheet Resistivity of Diffused Layer (Ω/□)	Depth of Diffused Layer (NaD Fringes)
10.5	2.5	7
7.5	2.5	6
5.8	4.5	5
4.3	8.1	4
2.7	47.0	3
2.1	962.0	1½

TABLE II

SHEET RESISTIVITY OF THE DIFFUSED LAYER VS. THICKNESS
OF VAPOR PLATED PHOSPHOSILICATE

Thickness of Vapor Plated Phosphosilicate Layer (Å)	Sheet Resistivity (Ω/□)
2000	48
8000	50
16000	50

Preliminary Evaluation of Possible Candidates for Second Layer Insulator Materials and Processes

A second layer oxide should have stable electrical properties and it should not change the surface potential of the silicon.

We have supplemented the work reported in the First Interim Report by measuring the charge densities in additional samples of oxides that have been considered as candidates for second layer insulators. Each of these samples was formed into MOS capacitors with all of the oxide layers beneath the metal. Half of each wafer was metalized with aluminum from an electron-gun evaporator and half was metalized with Al from a resistance-heated tungsten coil.

If not otherwise specified, the phosphosilicate layers discussed in this report were deposited from a reactant gas mixture containing 4% (mole) phosphine. This yields layers containing approximately 3% phosphorus by weight.

The results are summarized in Table III. We conclude from this data that:

1. The phosphorus-containing vapor plated SiO_2 has yielded low levels of both immobile and of mobile charge.
2. The presence of phosphorus in the vapor plated oxide has immobilized the sodium that was introduced by the tungsten coil evaporation.

TABLE III

CHARGE DENSITIES IN CANDIDATES
FOR SECOND LAYER INSULATOR

	10^{11} Charges/cm^2		
	Immobile	Mobile (300°C)	Mobile (25°C)
Thermally grown SiO_2 (#587)			
Electron gun	3.2	1.0	1.0
Tungsten coil	3.3	8.0	12.0
6000 Å vapor plated SiO_2-Al_2O_3 on 2000 Å thermally grown SiO_2 (#586)			
Electron gun	20.0	30.0	<1.0
Tungsten coil	20.0	>30.0	---
6000 Å vapor plated phosphorus-containing SiO_2 on 2000 Å thermally grown SiO_2 (#585)			
Electron gun	1.9	0.5	0.3
Tungsten coil	1.9	0.2	0.1
5000 Å of vapor plated SiO_2 on 1000 Å of vapor plated phosphorus-containing SiO_2 on 2000 Å of thermally grown SiO_2 (#590)			
Electron gun	9.0	2.5	<1.0
Tungsten coil	12.0	1.5	<1.0

3. The Al_2O_3-SiO_2 has very high immobile and mobile charge densities. This result does not confirm the result reported in the First Interim Report in which a 2000 Å thick layer of vapor-plated SiO_2-Al_2O_3 on a 2000 Å thick layer of thermally grown SiO_2 showed a flat band voltage range of -3 to +3 volts. (This is roughly equivalent to an immobile charge density of 1.5×10^{11} negative charges/cm^2 and a mobile charge density of 4×10^{11} positive charges/cm^2.

4. There is a high immobile charge density in samples having a vapor plated layer of pure SiO_2 over a phosphorus containing vapor plated layer.

In the First Interim Report, we reported that r-f sputtered SiO_2 contains a high density of mobile charge. Since then we have taken more data on other samples of r-f sputtered SiO_2. Table IV summarizes our data. Because we do not know whether negative mobile ions exist in these oxides we list the limits of the range in the effective charge density that were measured after drifting at 300 C for 12 minutes under an applied bias of plus or minus 12 volts in the metal.

TABLE IV

CHARGE DENSITIES IN R-F SPUTTERED OXIDES

	10^{11} Charges/cm^2		
Sample #	After -12V	After +12V	Δ
528A	+4.0	+28.	24
529A	+2.0	+37.	35
609	-2.0	+18.	20
613	+3.3	+39.	36

Samples 528A and 529B have single 5000 Å thick layers of sputtered oxide on bare silicon. Samples 609 and 613 had a first layer of 1400 Å of thermally grown oxide and a second layer of 2000 Å of sputtered oxide.

Effects of Polarization of Phosphosilicate Glass

The polarizability of phosphosilicate layers has been described by Snow and Deal (Ref. 8 and 9) for samples that were formed by thermal oxidation and diffusion at high temperatures. Because of the potential instability that this polarization could introduce to microcircuits containing

thick layers of phosphosilicate, we have studied the polarization of phosphosilicates prepared by the vapor plating process at 400°C. Table V summarizes data taken on MOS capacitors having a first layer of 2000Å of thermally grown SiO_2 and a second layer of 6000 Å of 4% vapor plated phosphosilicate. The drifting at ±12 volts shows there were very few mobile ions in the oxide. The strong dependence of the flat band voltage on the applied drift voltage provides good evidence that the shifts in flat band voltage are due to polarization of the phosphosilicate glass.

TABLE V

EVIDENCE OF POLARIZATION
IN PHOSPHORUS-CONTAINING VAPOR PLATED OXIDES

Bias Conditions Coil-Evaporated Aluminum	Average Flat Band Voltage
-12V, 300°C, 12 min.	(-) 7.0 V
+12V, 300°C, 12 min.	(-) 8.2
-200 V, RT*, 2 hrs.	(-) 4.8
-200 V, RT , 3.5 hrs.	(-) 2.2
-200 V, RT , 68 hrs.	(+) 2.5
+200 V, RT , 48 hrs.	(-) 7.0
+200 V, RT , 96 hrs.	(-) 16.7
-50 V, RT , 68 hrs.	(-) 5.7
Electron-Gun Evaporated Aluminum	
-12 V, 300°C, 12 min.	(-) 7.3
+12 V, 300°C, 12 min.	(-) 9.0
-200 V, RT , 2 hrs.	(-) 5.2
-200 V, RT , 3.5 hrs.	(-) 3.2
-200 V, RT , 68 hrs.	(+) 0.7
+200 V, RT , 48 hrs.	(-) 7.7
+200 V, RT , 96 hrs.	(-) 14.0
-50 V, RT , 68 hrs.	(-) 6.0

* RT - Room Temperature

Polarization effects become more pronounced as the applied voltages are increased. This can become a problem when voltage-accelerated testing is done with the surface ion test structure. For example, Figures 5 to 8 show data that was taken on the surface ion test structure. At first glance one might infer from the severe channeling shown in Figures 5 and 6 that surface ions were a problem on these oxides. However, the data in Figures 7 and 8 show that hardly any channeling occurred when the voltage was applied to electrode B. This leads to the conclusion that surface ions were not causing the channeling but that it was due to polarization of the phosphosilicate glass. The geometry of electrodes A and B is given in Figure 1 of Appendix B.

In order to understand instability problems due to this dipole polarizability it is important to understand the following physics.

1. The shift in flat band voltage due to polarization cannot be greater than the voltage that induces the polarization. Snow and Deal (Ref. 8 and 9) found the former to be no more than 16% of the latter.

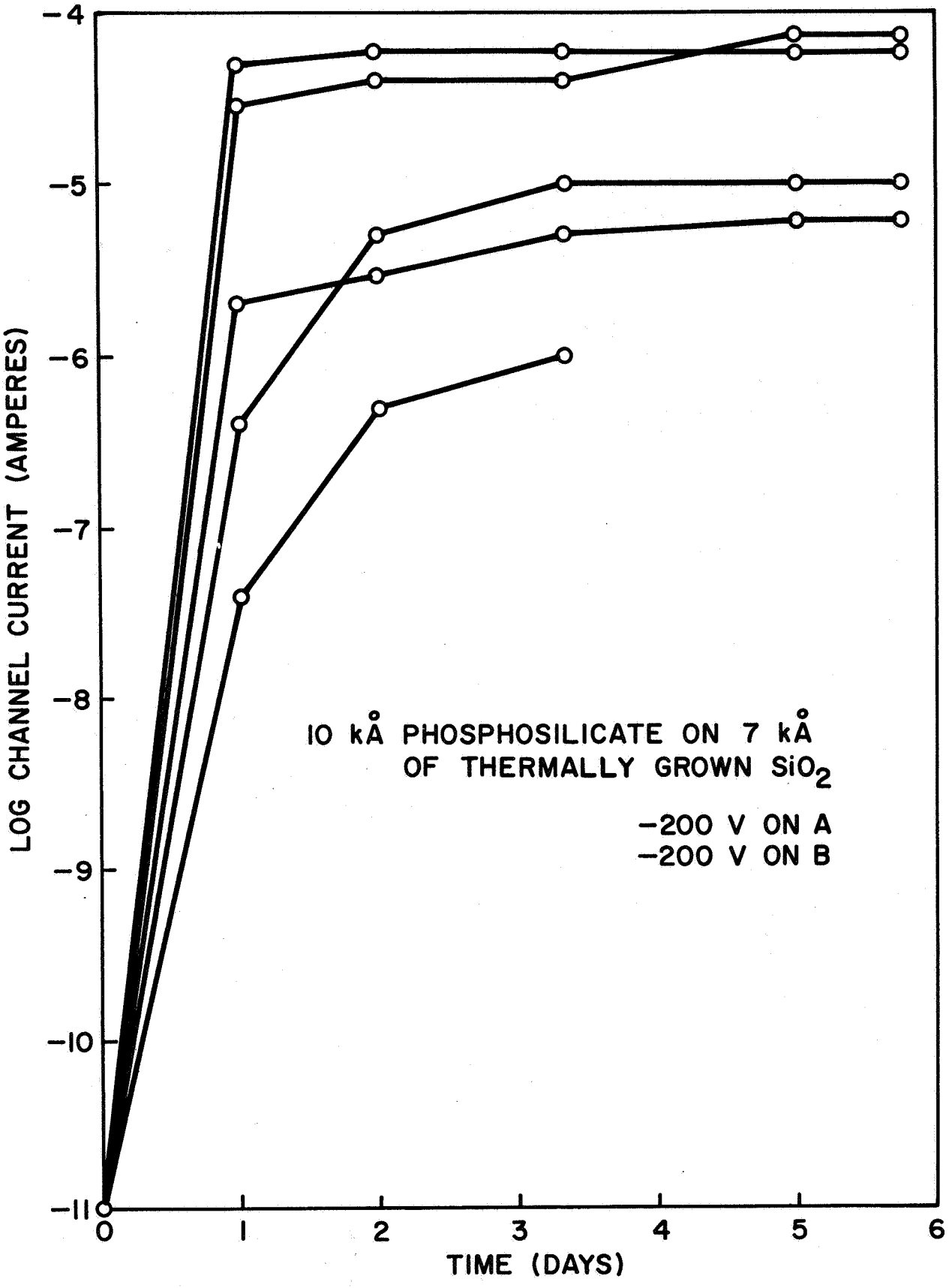

Figure 5. Channel current vs. time, phosphosilicate over SiO_2, -200 V on both A and B.

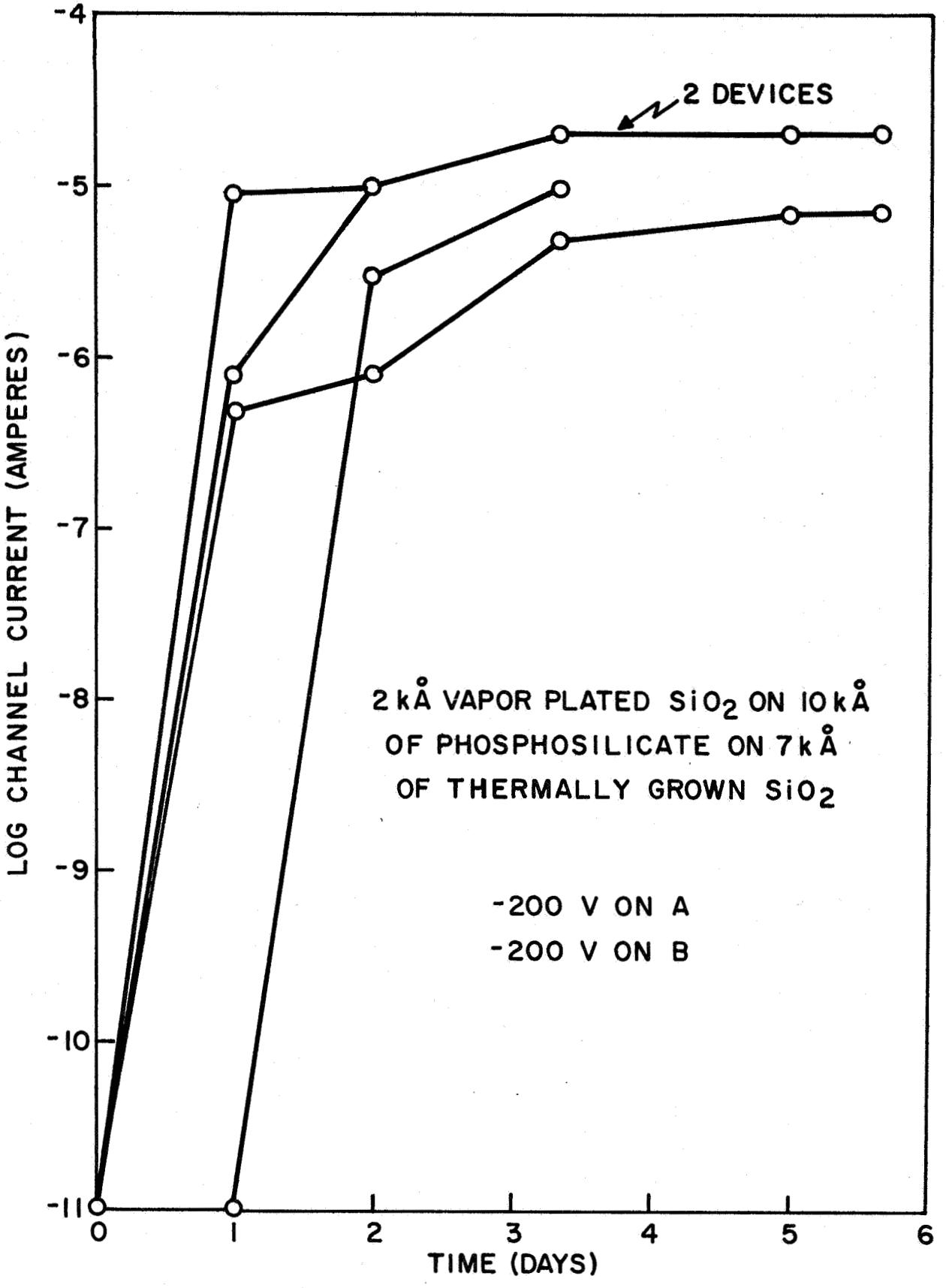

Figure 6. Channel current vs. time, SiO_2 over phosphosilicate over SiO_2, -200 V on both A and B.

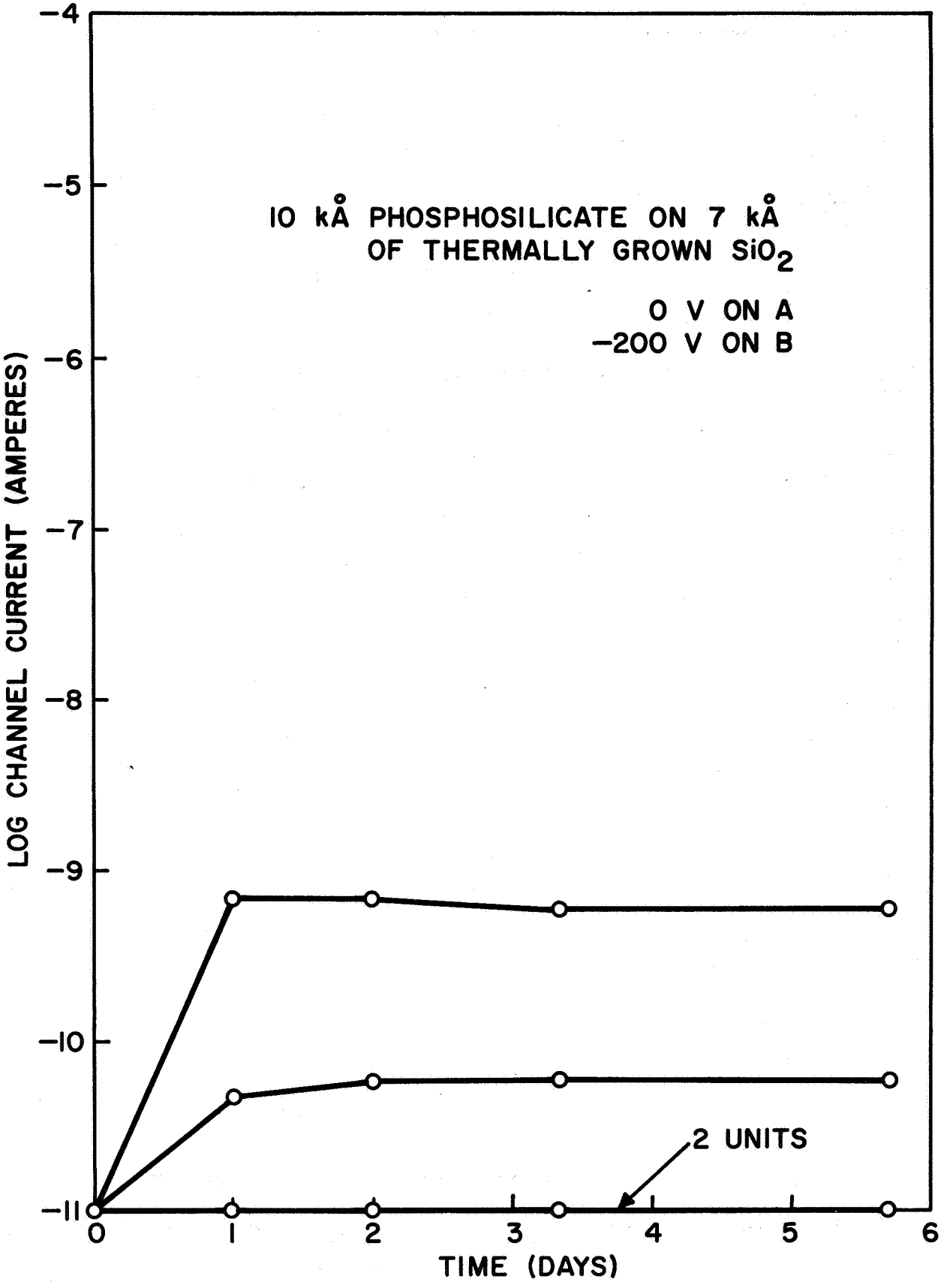

Figure 7. Channel current vs. time, phosphosilicate over SiO_2, -200 V on B.

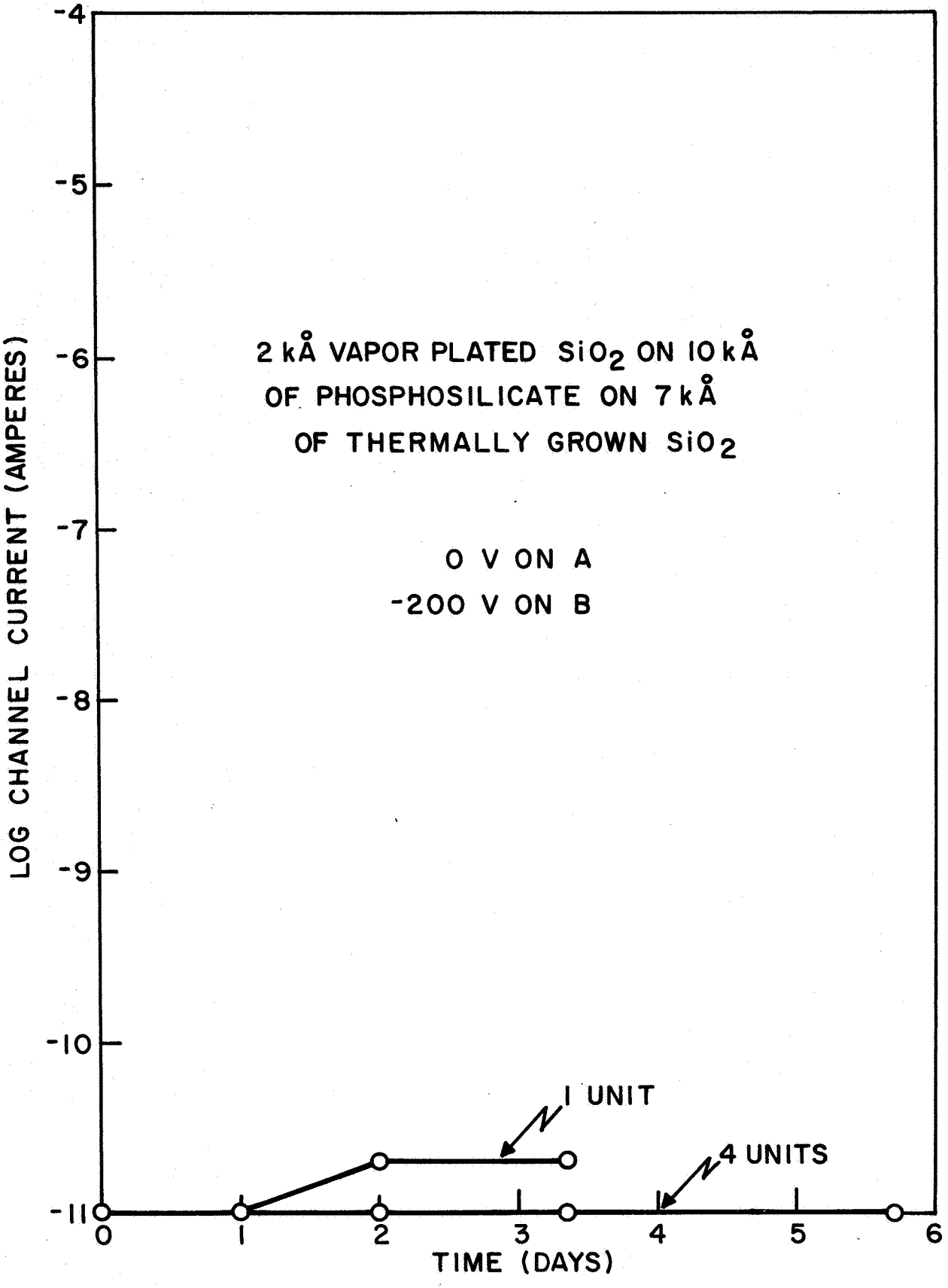

Figure 8. Channel current vs. time, SiO_2 over phosphosilicate over SiO_2, -200 V on B.

2. Since only the voltage across the polarization layer is effective in inducing polarization, the thinner the polarizable layer in relation to the total insulator layer thickness the less will be the effect of the polarization.

3. The amount of polarization is dependent on the electrical conductivity of each of the layers. The electric field in each layer is dependent, in the d-c case, on the conductance of the layers. Since the conductance of the phosphorus-containing layer is much higher than that of an SiO_2 layer without phosphorus, the electric field in the phosphorus-containing layer is correspondingly lower. This, in turn, causes the induced polarization to be correspondingly lower.

Migration of Mobile Charge from Areas Adjacent to Areas Beneath the Metal

A set of experiments with the MOS capacitors described in the First Interim Report has demonstrated the following:

1. The MOS capacitor with the high ratio of perimeter to area is useful for studying the migration of charge from regions adjacent to regions beneath metal layers.
2. Photolithographic processes have been found to contribute to the mobile charge density of microcircuits.
3. Significant differences exist in the mobile ion content of devices prepared by two different photolithographic processes.

Table VI shows the data taken on MOS capacitors that support the above statements. The resists used were Shipley AZ positive resist and Kodak Thin Film Resist (KTFR) negative resist. The test structures are the two MOS capacitors described in the First Interim Report. The test structures were prepared without a diffusion and without the photolithographic steps involved with making diffusion cuts or contact cuts. Each sample was given a short duration etch in buffered HF before the aluminum was evaporated by an electron beam.

TABLE VI

EFFECTS OF PHOTOLITHOGRAPHY ON CHARGE DENSITY

	10^{11} Charges/cm^2		
	Immobile	Mobile (300°C)	Mobile (25°C)
Capacitor, 30 x 30 mils			
AZ, Not Alloyed	2.2	0.1	0.1
AZ, Alloyed	2.0	0-1	0-1
KTFR, Not Alloyed	2.2	1.	0
KTFR, Alloyed	2.0	0.5	0
Capacitor with 0.2-mil Line Widths			
AZ, Not Alloyed	3-4	>20*	≈10*
AZ, Alloyed	2.0	≈15-25*	2*
KTFR, Not Alloyed	2.5	2.5	2.5
KTFR, Alloyed	2.0	6.	5.

*The C-V curves exhibit a very gradual slope and so the values are rough estimates.

Both resists were stripped (with J100) at 70 to 75°C for 10 minutes followed by an acetone spray and a water rinse. In each case the aluminum was etched in a PNA etch at 75°C followed by a water rinse. (PNA is a mixture of phosphoric, nitric and acetic acids) Both resists were baked prior to the aluminum etch at 160°C for 45 minutes.

Table VII shows data from other experiments of a similar nature. These devices were different from those in Table VI in that in these devices the oxide in the MOS capacitor had been used as a mask for a boron diffusion. The resist used for delineating the aluminum was Shipley AZ resist. The aluminum was evaporated with an electron gun.

TABLE VII

EFFECTS OF OXIDE TYPE ON MIGRATION OF CHARGE FROM AREAS ADJACENT TO AREAS BENEATH METAL

	10^{11} Charges/cm^2		
Capacitor, 30 x 30 mils	Immobile	Mobile (300°C)	Mobile (25°C)
7000 Å Thermal SiO_2	2.1-2.9	0.6-3.2	0.0-1.4
5000 Å Vapor Plated SiO_2 on 2000 Å Thermal SiO_2	2.0-2.6	1.5-2.0	0.5-1.3
5000 Å Vapor Plated SiO_2 on Diffused Phosphosilicate Layer on 2000 Å Thermal SiO_2	3.0-10.8	0.0-1.0	0
Capacitor with 0.2-mil Line Widths			
7000 Å Thermal SiO_2	2.0-3.2	≈20	CNM*
5000 Å Vapor Plated SiO_2 on 2000 Å Thermal SiO_2	2.2-2.8	≈20	CNM*
5000 Å Vapor Plated SiO_2 on Diffused Phosphosilicate Layer on 2000 Å Thermal SiO_2	3.6-6.3	0.5-1.0	0.5

*CNM -- Can Not Measure

We can conclude from Table VII:

1. Mobile ions migrate from regions adjacent to regions beneath the metal layers.

2. Devices with only thermally grown oxide and devices having two layers - a thermally grown layer and a vapor plated layer of pure SiO_2 - behaved similarly under these test conditions.

3. The addition of a layer of diffused phosphorus between two SiO_2 layers serves to getter mobile ions.

4. That vapor plated oxide overlying a phosphosilicate layer apparently causes a high immobile charge density. This is also indicated in the data represented in Table III.

Surface Recombination Velocities

Measurements in addition to those reported in the First Interim Report, were made of surface recombination velocities. The measured volumes of the surface recombination velocity depend somewhat on the bias voltage on the p-n junction and therefore we have made each measurement at an applied bias of both 0.5 and 5 volts. Table VIII shows our results taken at 29°C on samples having a boron diffused p-n junction on 5 Ω-cm n-type <111> silicon.

TABLE VIII

SURFACE RECOMBINATION VELOCITIES

Sample Type	Surface Recombination Velocity (cm/sec)	
	0.5 V	5.0 V
7000 Å Thermally Grown SiO_2		
Wafer 564	23-27	---
Wafer 579	36	62-93
5000 Å Vapor Plated SiO_2 on 2000 Å Thermally Grown SiO_2	42	37-110
5000 Å Vapor Plated SiO_2 on Phosphorus Diffused Layer on 2000 Å Thermally Grown SiO_2	14-30	37-72

These data indicate that the second layer oxides, either with or without a phosphorus diffused layer, do not seriously degrade the surface recombination velocity. These surface recombination velocity levels are fairly high in each case, and they could be decreased by a gettering operation. Future work should include similar measurements on gettered samples.

Surface Ion Studies

The surface ion test structure that was described in the First Interim Report has been utilized to collect a body of fundamental data to establish in detail the behavior and

effects of surface ions on planar devices. The paper in Appendix B presents the results of our work. It was presented at the 1968 Silicon Interface Specialists Conference and has been submitted to the IEEE Transactions on Electron Devices for consideration for publication in a forthcoming special MIS issue.

The work discussed in the paper provides a significant improvement in the understanding of the behavior of surface ions in planar devices. The model for the kinetics of surface ion behavior has been extended to include the case in which the total surface ion density is dependent on the surface potential of the oxide. We show that the observation that a channel builds-up as the square root of time does not necessarily indicate that the surface conductivity is time and voltage independent as earlier investigators (Ref. 10, 11 and 12) had concluded.

Our work shows that the parameter that should be used for comparing different samples having the same geometry but different surface conductivities is the time dependence of the build-up of channels. After long periods of time under bias the determining factors for whether a device develops a channel are the thickness and dielectric constant of the oxide, the resistivity of the silicon, the applied voltage and the

effective charge density in the oxide. The surface conductivity influences the rate at which surface ions move but does not affect their final distribution.

Our data shows that the most significant variable that influences the kinetics of surface ion behavior is the ambient humidity. Surface ion behavior has been observed to change drastically in less than one second due to changes in the relative humidity of the ambient. Depending on the amount of humidity in a hermetically sealed package, surface ions can move faster at room temperature than at 125°C, presumably due to differences in the amount of water adsorbed on the oxide surface. On the other hand, on other similar devices temperature appears to have very little effect on surface ion behavior. This might suggest that a tunneling mechanism is involved in which carriers hop between localized islands on the oxide surface.

We find that surface ion behavior is strongly dependent on the testing history of the device, that is, surface ions move much faster the second time they are drifted (within a period of tens of hours).

We have found also that positive surface ions move an order of magnitude faster than negative surface ions.

The literature shows numerous examples of charge separated on the oxide surface at the region where a pn junction intercepts the silicon surface. From this one might infer that the important factor influencing surface ion migration is the electric field strength along the oxide surface due to a difference in potential between two adjacent metal lines on the surface of the oxide. One might expect surface charge to accumulate between two metal electrodes as shown in Figure 9. However, a study of the physics involved leads one to believe that this distribution is unlikely to occur between two metal electrodes. Charge accumulation of the type shown would only occur if one of the following conditions existed:

1. If there were barriers to prevent the accumulated surface charge from drifting to the metal where it is effectively neutralized. Such barriers are not known to exist.
2. During a transient situation before all the mobile charge is swept from the region between the metal layers. We have been unsuccessful in our efforts to demonstrate this case.
3. If there is a steady state situation in which mobile ions are generated on the oxide surface and they drift in such a way as to establish the net charge distribution shown.

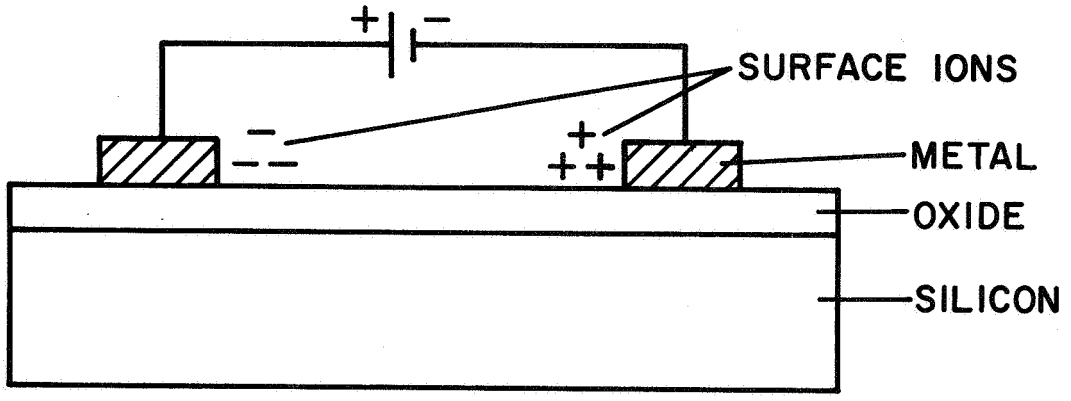

Figure 9. Improper model for surface ion migration.

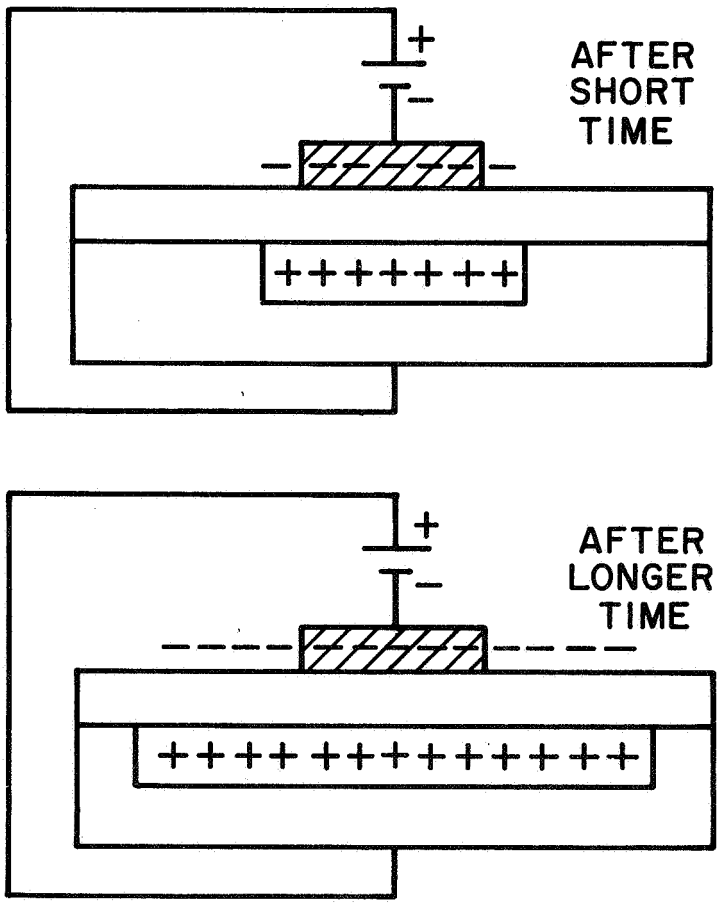

Figure 10. Surface charge migration after the application of a voltage to the metal relative to the silicon.

A surface ion behavior model must take the following into account. Basically, the net surface ion density and the voltage across a thickness of oxide on silicon are interdependent. That is, a given net charge density establishes a field of a given strength which establishes a given voltage across the oxide thickness and induces a given charge density per unit area in the silicon. The silicon is practically an equipotential region if one ignores the presence of p-n junctions. Even in an MOS capacitor, because of the formation of an inversion layer, the potential can be altered by no more than a fraction of a volt.

On this basis, then, it is clear that the determinant of net surface ion density is the surface potential of the oxide relative to the underlying silicon. Taking this into account, the kinetics of surface ion motion can be described as shown in Figure 10. At t = 0 the application of a negative voltage on the metal relative to the silicon induces a net negative charge density in the metal at the oxide interface and a positive charge density in the silicon at the oxide interface. Because the metal is smaller in area than the silicon there are lines of force extending laterally at the edges of the metal. This causes ions to drift to develop a net negative charge density on the surface of the oxide in regions adjacent to the metal.

(This net negative charge may be due to a migration of mobile negative ions from the metal or of mobile positive ions from the oxide.) This process of ion migration continues and the surface charge density and the layer of net charge density in the silicon increase in area, extending farther and farther away from the metal until eventually the entire top surface of the oxide becomes an equipotential surface. The time dependence of this surface charge migration is quantitatively described in Appendix B of this report.

This analysis assumes an infinite supply of surface ions, the absence of p-n junctions in the silicon and that there are no other metal electrodes having different potentials. These assumptions merely simplify the discussion and do not affect the validity of the model. Any valid model for surface charge behavior must be consistent with this model.

The final steady state condition is symmetrical so far as polarities of voltage and charge are concerned except that, depending on the polarity of the applied voltage and the silicon conductivity type, the charge in the silicon may be in an accumulation layer or in depletion and inversion layers. The difference is one of exact location of the charge in the silicon and is not relevant in this discussion of the model

for surface ion behavior. Considering the transient condition, there is a slight difference due to the difference in the mobility of the ions.

Ambient Effects

In connection with a company-sponsored program, sensitive test structures were packaged in several types of plastic encapsulants and in hermetic TO-5 packages to study the effects of different ambient materials. These packaged test structures included samples containing several types of second-layer oxides.

In this report, we show the results taken on two insulator types:

1. A first layer of 7000 Å of thermally grown SiO_2, with a second layer of 10,000 Å of phosphorus-containing vapor plated SiO_2.
2. Same as 1, with an additional layer of 2000 Å of vapor plated SiO_2.

These oxides are referred to hereafter as Type 1 and Type 2 oxides, respectively.

Packages involved in the test include:

1. Hermetically sealed TO-5 packages. The devices were given a 200°C bake for 1 hour in a vacuum before they were sealed in dry (<15 ppm) N_2.
2. Plastic packages of two types.

The test structures included:

a. MOS capacitors with high perimeter-to-area ratio,

b. MOS transistors,

c. Surface ion test structures,

d. Diffused p-n junction diodes.

These devices were aged at 75°C under an applied voltage of plus or minus 60 V. Voltages of both polarities were applied to the metal of the MOS capacitor, the gate of the transistor, and the metal electrode overlying the diffused regions of the surface ion test structure. Minus 60 V was always applied to the p+ region of the p-n junction. The electrical characteristics of these devices were then measured.

We found that, after 242 hours at 75°C under an applied bias of -60 V, or after 480 hours at 75°C under an applied voltage of +60 V,,we found no significant change in the effective charge density in the MOS capacitor with the high perimeter-to-area ratio and no significant change in the threshold voltage or the transconductance of the MOS transistors.

The aging temperature of 75°C was chosen because it was believed that the plastic encapsulants should not, under normal stress conditions, be subjected to temperatures higher than 125°C and because there is the possibility that plastic encapsulants will retain more moisture at 75°C than at 125°C.

Our standard testing procedure for mobile ions includes an ion drift temperature of 300°C and a drift time of 12 minutes. If an activation energy of 32 kcal/mole (Ref. 13, 14, and 15) is assumed, an equivalent test at 75°C would require 9×10^8 minutes or 1700 years. If the activation energy were the lowest reported value of 7.6 kcal/mole, the equivalent test would require 1000 minutes or 16.8 hours. For this reason, the usual test for mobile ions is impractical. A practical approach for measuring surface ions in this case is to measure the total effective charge density in MOS capacitors after aging at 75°C under both positive and negative bias for the aging period.

Significant changes were observed in three of the other measurements taken on the test structures - the channel current in the surface ion test structure, and the diode breakdown voltage and reverse current of the p-n junction.

Figure 11 shows the measured channel currents taken on the surface ion test structure, at 1.5 V after minus 60 V was applied to electrode A for the given periods of time. The threshold voltage on the MOS transistors with Type 1 oxides was 11 V and therefore the inversion voltage in regions having the total oxide thickness of 17,000 Å would be about 18 V (assuming that the effective charge density in the oxide was not changed in the regions where there is no metal between the

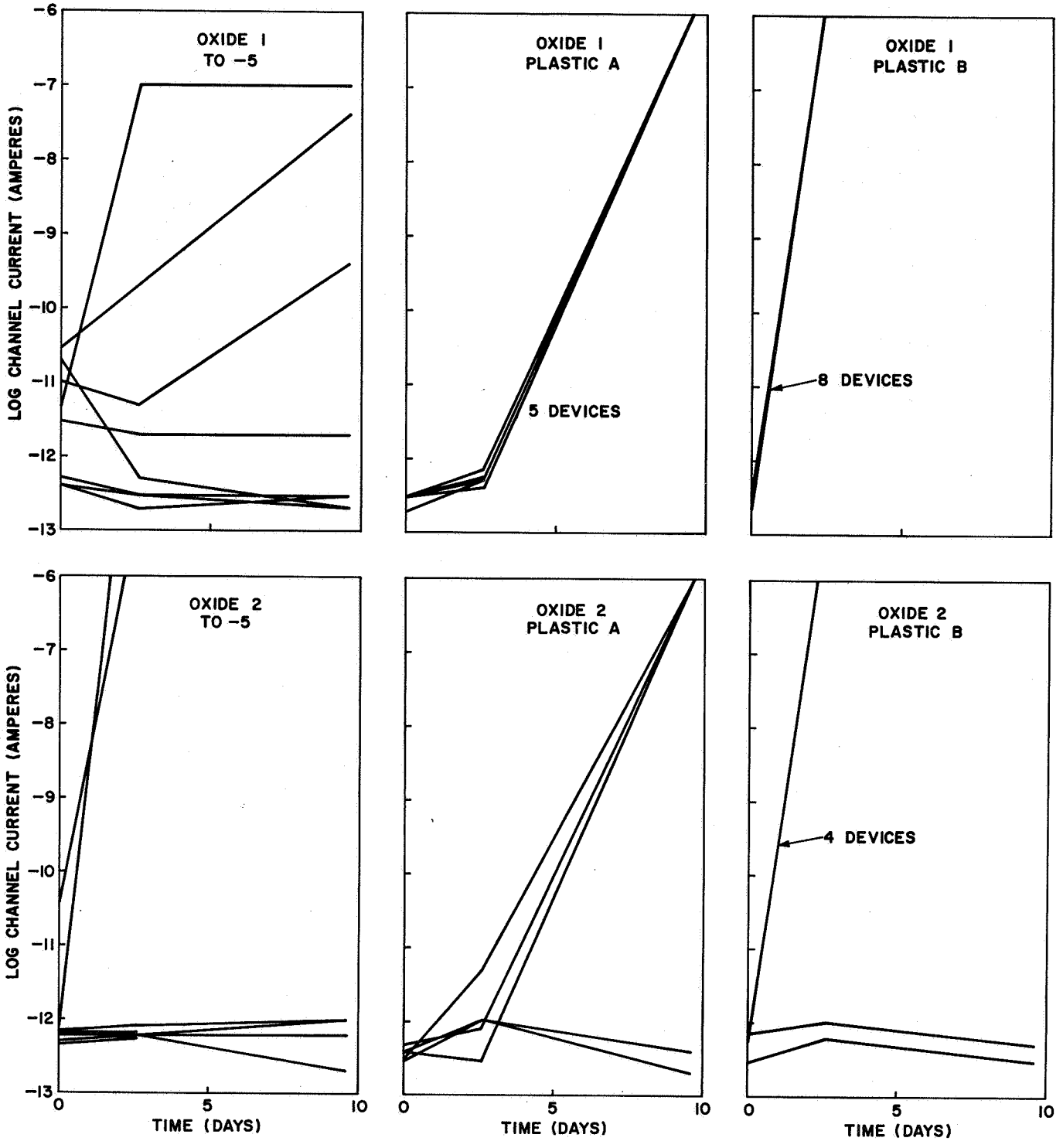

Figure 11. Channel current in surface ion test structure.

first- and second-layer oxide). Similarly the devices with Type 2 oxides have a threshold voltage of 13 V and an expected field inversion voltage of 25 V at 19,000 Å.

The data in Figure 11 can be interpreted as follows:

1. Distinctive differences are observed for samples in different packages.
2. The data is consistent with our belief that any plastic package is likely to contain a supply of mobile ions capable of moving on the microcircuit surface.
3. The rate at which a particular plastic package releases these ions is different for different samples of plastic.

The reverse current of the p-n junction diodes exhibited the behavior shown in Figure 12 and diode breakdown voltages exhibited the behavior given in Figure 13. These three measurements -- the channel current of the surface ion test structure, the diode reverse current and the diode breakdown voltage -- are consistent with each other and with the model described below.

A negative applied bias will cause negative ions to move out over the surface of the oxide over the n-type silicon. These negative surface ions increase the reverse current of

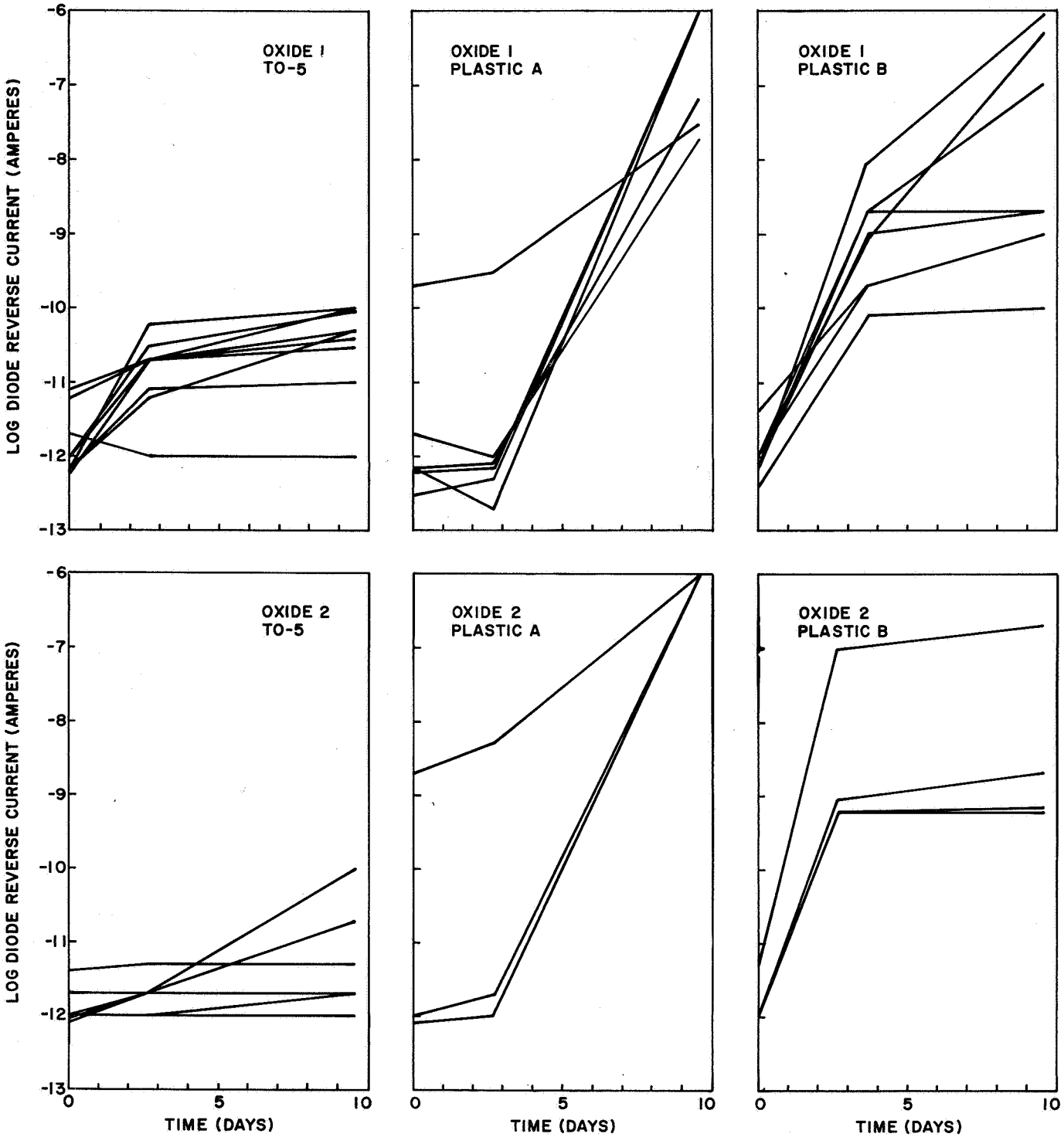

Figure 12. Reverse current in diode test structure.

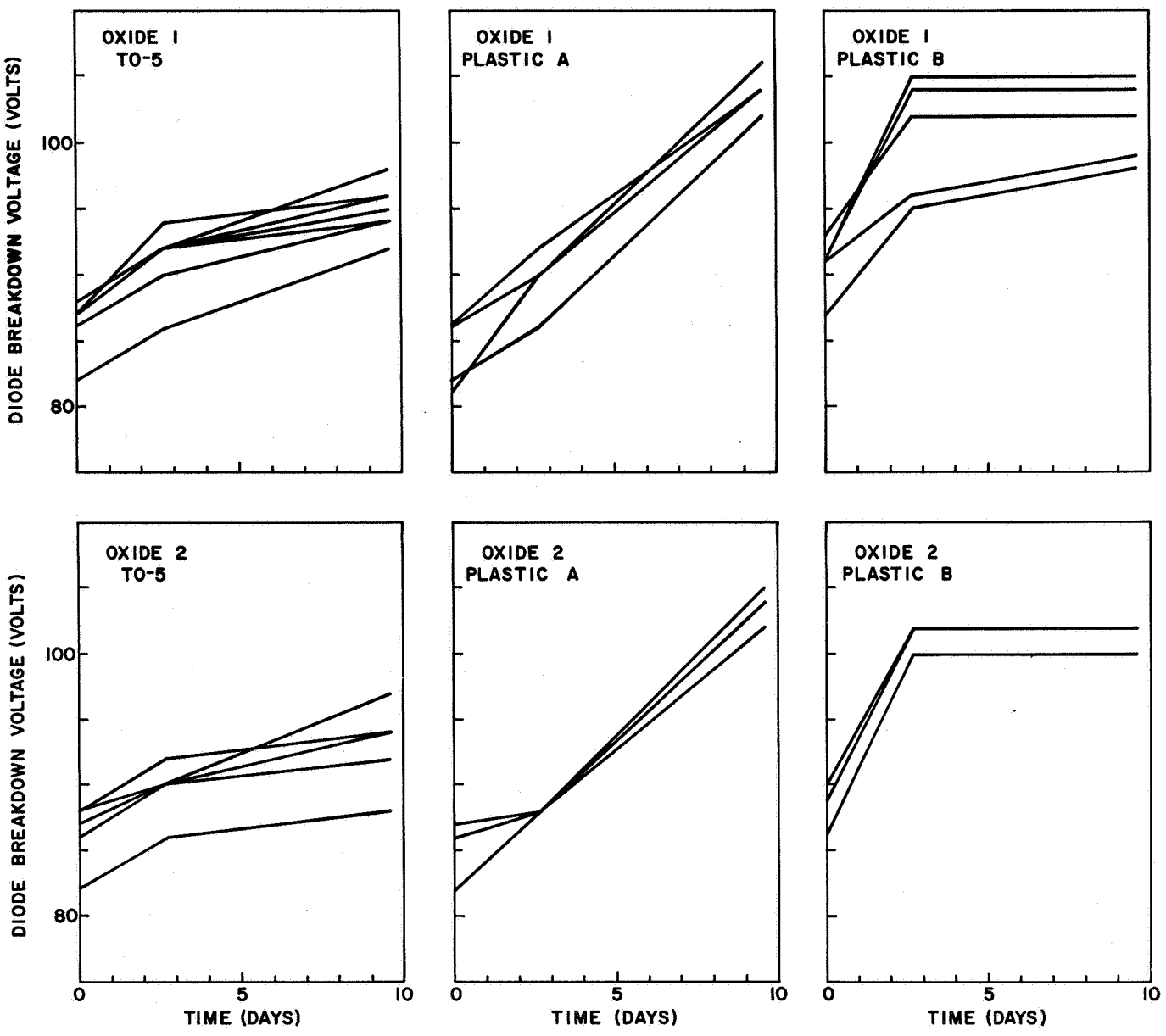

Figure 13. Breakdown voltage of diode test structure.

the diode. This increase is either due to an inversion layer which effectively increased the diode area or to change in the surface potential which increases the surface recombination velocity. Negative surface charge over the n-type region decreases the electric field in the region where the depletion layer intercepts the silicon surface and this increases the diode breakdown voltage.

Study of Effects of Variations in Phosphorus Content in Vapor Plated Oxide

A determination was made of the effects of the phosphorus content in second-layer vapor plated oxides. In each case the first layer oxide was 2000 Å of SiO_2 thermally grown in dry O_2 at 1200°C and then 8000 Å of SiO_2 was vapor plated in 400°C. These vapor plated layers contained different concentrations of phosphorus which was incorporated into the oxide during the vapor plating process by including phosphine in the reactant gas mixture. The percentage of phosphine in the reactant gas mixture was varied from 1 to 4%. The approximate percentage of phosphorus in the layer can be obtained from Figure 2. Aluminum was evaporated with either an electron gun or a tungsten coil.

The charge densities measured on MOS capacitors are given in Table IX. The data shows that:

TABLE IX

EFFECTS OF VARIATIONS IN PHOSPHORUS CONTENT

PH_3 in Reactant Mixture (Mole %)	Type of Metal Evaporator	10^{11} Charges/cm^2 After -25V, 300°C, 30 min.	After +25V, 300°C, 30 min.	Δ
Control*	Electron gun	+2.2	+3.3	1.1
0	Electron gun	+2.3	>+22.	>20
1	Electron gun	+4.0	+20.	16
1	Tungsten coil	+4.0	>+22.	>18
2	Electron gun	+4.2	+7.3	3.1
3	Electron gun	+4.2	-1.4	5.6
4	Electron gun	+4.7	-1.7	6.4
4	Tungsten coil	+4.7	0.0	4.7

*Only the 2000 Å of thermally grown oxide.

1. Second layer oxides made by vapor plating processes present a number of problems that can seriously degrade microcircuits.
    a. Vapor-plated SiO_2 contains a high density of mobile positive ions.
    b. Trapping has been found in some phosphorus-containing vapor plated oxides (the 3% and 4% samples).
    c. There is evidence that samples change with either the testing process or with age alone.
2. The presence of phosphorus in the vapor plated layer increases the fixed charge content of the oxide.
3. The level of phosphorus content significantly influences the type and magnitude of the variable charge content of the oxide.
    a. At low phosphorus levels some mobile charge is apparently immobilized.
    b. At higher phosphorus levels it would appear that trapping is introduced. Further work is necessary to determine the cause of this unusual behavior.

Polarization of Phosphosilicates

When relatively thick layers of phosphosilicate are involved, one must be alert to the effects of polarization of the type described by Snow and Deal (Ref. 8 and 9). The data presented in Table X was taken on samples having 4% phosphine in the reactant gas mixture. We believe that the observed instability is due to polarization of the phosphosilicate layer. The observation that there is less instability in the samples made with tungsten coil evaporation than those made with electron gun evaporation indicates that sodium reduces the polarizability of phosphorus-containing oxides. This would be expected if the dipoles are involved in the sodium gettering. Each of these samples was made with a first layer of 2000 Å of thermally grown oxide and a second layer of about 4000 Å of phosphorus-containing vapor plated oxide. The samples were all made at the same time and in the same way except that each wafer was scribed into two parts and one half was aluminum metalized by evaporation from a tungsten coil and the other half by evaporation with an electron gun.

TABLE X

POLARIZATION OF PHOSPHOSILICATE

Sample No.	Type of Metal Evaporator	10^{11} Charges/cm^2 After -12 V 300°C, 12 min.	After +12 V 300°C, 12 min.	Δ
631 (Control)*	Electron gun	2.4	2.7	0.3
	Tungsten coil	2.7	30.0	27.3
655	Electron gun	1.2	3.7	2.5
	Tungsten coil	1.9	3.4	1.5
656	Electron gun	1.6	2.6	1.0
	Tungsten coil	1.8	3.0	1.2
657	Electron gun	1.7	3.3	1.6
	Tungsten coil	2.1	3.1	1.0

*Only the first layer of oxide.

Evaluation of Oxide Test Techniques

As testing of oxides is extended to thicker oxides, multi-level oxides and different oxide materials, it is important to recheck the adequacy of the conditions of voltage and the time used to drift the electrical properties of the oxide. For this reason we conducted a concentrated effort to fabricate a number of types of multilayer oxides and to test them under various conditions of applied drift bias, time and temperature. The entire test was then repeated with a second complete set of samples.

The results are summarized in Table XI. Four types of oxides are represented. The measurements on each sample were taken in the order they appear in each column in the Table. The test conditions were varied for the following reasons:

1. Test voltages were varied to keep the field across each oxide more nearly the same from sample to sample.
2. Where phosphosilicate was present the test was conducted at two voltages because polarization is a function of voltage and this would provide a means for at least partially separating polarization and mobile ion effects.

TABLE XI

MATRIX TEST SHOWING REPRODUCIBILITY OF OXIDES
AND REPEATABILITY OF MEASUREMENTS

Type of Oxide	Drift* Voltage (volts)	10^{11} Charges/cm^2 First Group -	First Group +	First Group Δ	Repeat Group -	Repeat Group +	Repeat Group Δ
2000 Å thermal	±12,	2.3	2.6	0.3	2.3	2.5	0.2
	±12	2.3	2.6	0.3	2.3	2.5	0.2
2000 Å thermal	±36,	5.4	10.0	4.6	0.6	25.0	24.4
5000 Å vap. dep.	±36,	5.1	8.0	2.9	0.6	12.0	11.4
SiO_2	±12,	7.3	11.0	3.7	0.6	23.0	22.4
	±36,	6.9	15.0	8.1	---	--	--
	±36	7.1	15.0	7.9	---	--	--
2000 Å thermal,	±12,	3.8	9.6	5.8	3.2	7.0	3.8
1000 Å vap. dep.	±12,	3.4	8.7	5.3	3.3	7.3	4.0
phosphosilicate,	±36,	8.2	9.3	1.1	3.6	14.0	10.4
5000 Å vap. dep.	±36	8.3	10.4	2.1	3.7	14.0	10.3
SiO_2							
2000 Å thermal,	±12,	2.3	2.8	0.5	2.3	2.6	0.3
5000 Å vap. dep.	±12,	2.4	2.8	0.4	2.4	2.6	0.2
phosphosilicate	±36,	2.6	3.1	0.5	2.3	3.1	0.8
	±36	2.7	3.1	0.4	2.6	3.1	0.5

*300°C, 12 minutes at each drift voltage

3. Each set of drift conditions and measurements was repeated to establish that a sufficient time had been used to obtain saturation of the effects.

The phosphosilicate was deposited from a reactant mixture containing 4% PH_3.

The data in Table XI supports the following interpretive comments relative to vapor deposited SiO_2 and phosphosilicate dielectric layers over pure thermally grown SiO_2.

1. In most cases, the test conditions are sufficient to saturate the shift in the charge density.
2. Vapor plated SiO_2 layers in some cases exhibit poor reproducibility from sample to sample. This is at least partly due to a nonrepeatability of measurements on a single sample.
3. The addition of phosphosilicate layers can improve the stability and reproducibility of dielectric layers.
4. The apparent effect of the drift voltage on the mobile charge density is not understood.

Results of a Matrix Experiment Involving Variations in Phosphorus Content, Annealing, Sodium Content and the Drift Voltage

A set of data was collected to evaluate the effects of phosphorus in vapor plated oxides and of a heat treatment at

the end of the vapor deposition process on the electrical properties of the oxide-silicon interface. In each sample the first oxide is 2000 Å of thermally grown oxide. The second oxide was vapor plated to a thickness of 4500 Å. Half of these vapor plated oxides contained phosphorus and half did not. Half were removed from the oxide vapor plating apparatus while the reactants were still flowing, whereas half (referred to as "annealed" in Table XII) were left in the apparatus in dry N_2 for ten minutes after the reactants were turned off. The aluminum metalization for half of the devices was evaporated with a tungsten coil; for the other half with an electron gun. The charge densities were measured in MOS capacitors after the drift voltage was applied for 12 minutes at 300°C. The measurements were taken in the following sequence:

1. The -25 V measurement was taken on every device;
2. Then half were measured at -12 V and half at +12 V;
3. Then the same devices that were measured at -12 V were measured at -36 V, and those that were measured at +12 V were measured at +36 V.

The results of the above measurements are summarized in Table XII. The results permit the following interpretive comments:

TABLE XII

EFFECT OF PHOSPHORUS CONTENT, ANNEAL, TYPE OF EVAPORATOR

Phosphorus in Second Layer Oxide?	Annealed?	Type of Metal Evaporator	10^{11} Charges/cm^2					Difference (±36)
			-25 V	-12 V	+12 V	-36 V	+36 V	
No	No	Tungsten coil	6.6	6.4	29.0	8.3	>32.0	>24.0
No	No	Electron gun	6.6	6.1	11.4	7.6	25.0	17.0
No	Yes	Tungsten coil	2.2	3.5	30.0	3.4	>30.0	>27.0
No	Yes	Electron gun	4.3	4.4	15.0	4.7	28.0	23.0
Yes	No	Tungsten coil	3.1	3.2	3.2	3.2	4.0	0.8
Yes	No	Electron gun	3.3	3.7	4.2	3.7	4.7	1.0
Yes	Yes	Tungsten coil	2.1	2.3	2.3	2.3	2.3	0.0
Yes	Yes	Electron gun	2.0	2.4	2.4	1.6	2.2	0.6

1. The phosphorus greatly reduces the mobile charge content in the oxide, including both mobile ions from the vapor plated oxide and from the coil evaporation.
2. The anneal in N_2 decreases the immobile charge density (the effective charge following a drift under negative bias). This may be due to a removal of moisture from the oxide.

TECHNIQUES FOR FACILITATING THE PRODUCTION OF RELIABLE MICROCIRCUITS

In this section, we present our current understanding of the most practical approach now possible for building the maximum reliability into the semiconductor and insulator parts of large-scale multilevel integrated circuitry consistent with a realistic consideration of the costs. We base this presentation on:

1. A familiarity with the work of other investigators as reported in the printed literature (Ref. 1) and at the technical meetings;
2. The results of our experimental efforts reported in this report and in the First Interim Report.

3. A comprehensive review of the current state of the relevant knowledge, an attempt to predict the most practical approach to maintaining and controlling microcircuit reliability in the design and fabrication stages, and attempts to uncover the areas that require further work.

Fundamentally, stable devices can be created in two ways. One way is to develop techniques and materials that yield devices containing few mobile ions. A second way is to design and build devices in such a way that a fairly large change in charge distribution can occur without causing large changes in the electrical characteristics of the devices. In either case, a prerequisite for the development, demonstration and production of reliable devices is the availability of practical test structures, equipment and techniques for measuring and characterizing the basic electrical parameters of the oxide layer and the oxide-silicon interface.

The reason that the emphasis is on the properties of the oxide layers and its surfaces and interfaces can be described as follows. A given change of the electric charge distribution, such as the ionization of a state or the migration of a charge, has a more significant influence in regions (the insulator and the semiconductor regions) where the density of mobile charge carriers is low.

Therefore, the first step to more reliable microcircuitry involves the creation of sensitive means for evaluating the electrical properties of insulator layers and of their surfaces and interfaces. A good basic set of test structures, measuring equipment and evaluation techniques for evaluating these electrical properties must include a capability to measure:

1. The surface potential of the semiconductor;
2. The stability of this surface potential over a period of time, under definite conditions of applied voltage and of ambient temperature and composition.
3. The density of various types of states capable of changing their state of charge. This general category includes the surface recombination velocity.
4. The mobility of carriers in the inversion layers.

Figure 14 of the First Interim Report describes a single 30 x 30 mil test structure chip, which contains: (1) a large area MOS capacitor to measure surface potential under the metal; (2) an MOS capacitor with a high ratio of periphery to area to measure changes in the surface potential beneath a metal layer due to the migration of contaminants from regions adjacent to regions beneath a metal layer; (3) a surface ion test structure to measure changes in surface potential (as evidenced by the developments of channels)

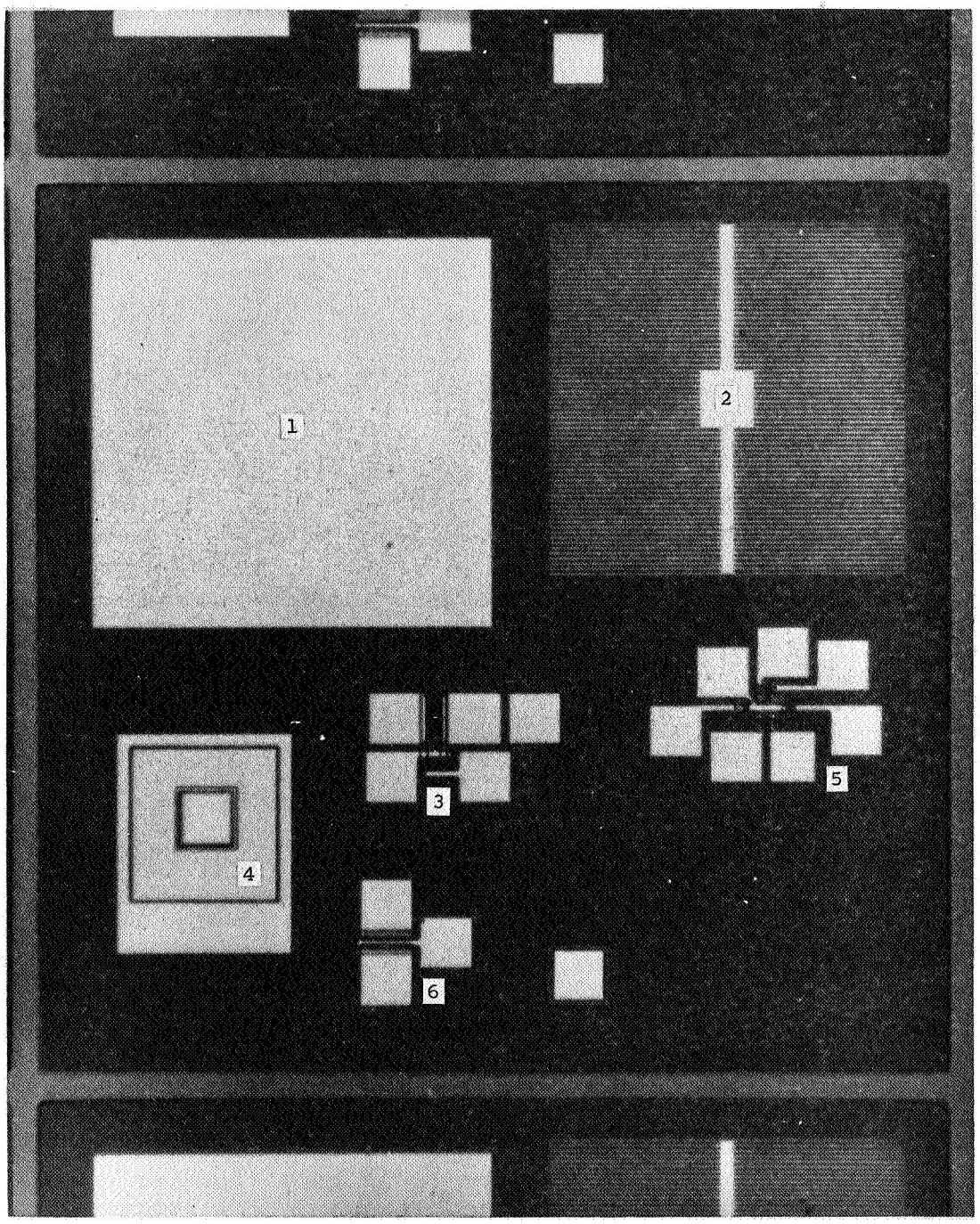

Figure 14. Test structure chip.

due to ionic migration on the oxide surface, (4) a structure for measuring surface recombination velocity by the technique described by Grove & Fitzgerald (Ref. 16), (5) a structure for measuring the Hall mobility of carriers in an inversion layer, (6) an MOS transistor, and (7) a junction diode.

Since the writing of the First Interim Report we have developed better measuring procedures for these test structures and have conceived some ideas concerning test structures that might be made in the future. Based on this accumulated experience we discuss below the following questions concerning test structures for evaluating insulator-semiconductor surfaces:

1. How does one most effectively use the present test structures?
2. How could the present set of test structures be improved?
3. How should test structures be used for process control and for analyses of yield and stability problems?
4. How can test structures be used in a production operation to fabricate reliable LSI circuitry?

Effective Use of Existing Test Structures

The existing test structures can be most effectively used as follows:

Large Area MOS Capacitors. - Capacitance-voltage (C-V) measurements of MOS capacitors are very useful for simple and rapid evaluations of the effective charge density in insulator layers on semiconductors.

Insofar as the circuit performance and stability are concerned, the important information is the range of the flat-band voltage. The variation within this range is a measure of the stability of the effective charge density in the oxide, and the absolute value is a measure of the inversion voltage level. It is useful in many cases to separate more definitely the types of charge existing in a given sample. This can be done by studying the effects of temperature and voltage on the effective charge density.

We typically separate fixed charge and variable charge by measuring the effective charge density after subjecting the capacitors to ±12 V (for oxide thickness of ≈2000 Å) for 12 minutes at 300°C. A substantial body of evidence indicates that all of the mobile ionic charge is positive. On this basis, we assume that the charge density after a negative applied bias is the fixed charge density, and the shift in effective charge density under the positive applied bias is due to positive

mobile ions. These assumptions and conclusions are probably valid for simple layers of thermally grown oxide. On the other hand, if phosphosilicate layers are present, they polarize in either polarity and the true fixed charge would be a value approximately midway between the two extremes. If trapping were present, one could tell little about a true fixed charge density.

In many cases, it is likely that some combination of trapping and fixed charge and, in the case of phosphosilicate layers, polarization is present. These various types of charge would be difficult to separate completely but their existence can be clearly demonstrated and they can be partially distinguished by measuring the same oxide under different conditions of applied bias and temperature.

Mobile charge should move to the same saturated effective charge level independently of the applied voltage. The change in flatband voltage due to mobile charge can be greater than the voltage applied to induce the change in flatband voltages. On the other hand, polarization of a phosphosilicate layer would be proportional to the applied polarizing field, and the change in flatband voltage can be no higher than the applied voltage that induces the polarization.

The polarity of the shift in flatband voltage is the same for mobile ions and polarization; applied positive voltage

on the metal shifts the flat band voltage to more negative values.

Trapping can be distinguished from polarization and mobile ions because the polarity of its shift is of the opposite type; i.e., an applied positive voltage to the metal causes the flatband voltage to shift in the positive (algebraically) direction.

The effect of voltage on trapping is unknown because the exact distribution of traps (both in space and in the energy diagram) is unknown.

Temperature would be expected to affect the measurement of variable charge as follows. Snow and Deal report that the activation energy for polarization of phosphosilicates is 1 eV as shown in Figure 6 of Ref. 8. Activation energies for mobile charge range from 0.3 to 1.4 eV. The activation energy for trapping is not known.

MOS Capacitors With a High Perimeter to Area Ratio. - The simplicity and utility of the MOS capacitor can also be used to study instability due to contaminating mobile ions from a second insulator layer (e.g., vapor plated or r-f sputtered SiO_2) that migrate from areas adjacent to areas beneath metal layers. Although similar data might be taken on MOS transistors having short gate lengths, high P/A capacitors are easier to make since they require no diffusion or alignment.

MOS Transistor. - MOS transistors are very useful test structures. Simple measurements of the threshold voltage and transconductance yield information concerning trapping and the mobility of carriers in the inversion layer. Trapping is determined by a comparison of the voltage required to conduct current in the inversion layer of the MOS transistor and the voltage required to create the inversion layer in the MOS capacitor. The mobility of the carriers in the inversion layer can be calculated from the transconductance of the MOS transistor.

Surface Ion Test Structure. - The surface ion test structure provides a good measure of the behavior and effects of surface ions on device performance and stability. The surface ion test structure is described in the paper in Appendix B.

One of the advantages of this test structure is that it permits one to measure the degree to which surface ions cause instability problems in microcircuits. These problems include channeling, effects on diode characteristics and on the characteristics of lateral bipolar transistors. While our measurements were concentrated on channeling, the test structure could be used to study the effects of surface ions on diode characteristics of lateral bipolar transistor behavior.

Further, this test structure does not require the complex experimentation of the vibrating reed electrometer used by Shockley et al. (Ref. 10 and 11) or even the capacitance measurements used by Snow (Ref. 12). Some might argue that a direct measurement of surface conductivity would provide a more fundamental measurement. In reply, one can argue that it is possible to obtain a measure of surface conductivity from our test structure and with much less concern about parallel conducting paths over package or micromanipulator surfaces. Direct surface conductivity measurements are difficult and require much larger chip areas than do measurements on the surface ion test structure. Furthermore, if the operating voltages are sufficiently high to influence the surface charge density and surface conductivity, a simple measurement of surface conductivity might be hard to relate to an actual device problem.

The surface ion test structure is very useful today for studying microcircuit stability problems. It will become even more useful as the problem of mobile ions in the interior of the oxide are solved. Plastic packages, which decrease the cost of microcircuits, increase the problems of surface ions and therefore increase the need for good surface ion test structures.

The surface ion test structure could also be used as a lateral bipolar transistor to study effects on surface recombination.

Junction Diode. - Measurements of reverse currents and breakdown voltages of diffused p-n junction diodes have been and are a very useful and sensitive means for detecting and studying instability due to either mobile ions on the insulator surface or in the interior of the insulator.

Surface Recombination Velocity Test Structure. - Grove and Fitzgerald (Ref. 16) have described a useful technique for measuring surface recombination velocity. The measurement of surface recombination velocity could play an important role in efforts to develop circuits designed to operate at lower power levels, or circuits containing lateral bipolar transistors. Degradation modes involving bipolar transistor action between regions not designed to be transistors, such as, for example, between a diffused resistor and an isolation region, might also be studied with surface recombination velocity measurements.

Inversion Layer Hall Measurement Test Structure. - To date, the capability to make Hall measurements on inversion layers in small areas has not been found to be especially advantageous for studying failure or stability problems. The measurement is fairly complex, and without a nonmagnetic package the mounting and handling of the device is quite awkward. Also, there is little evidence to suggest that the mobility of carriers in the inversion

layer is at this time an important factor in degrading circuit stability.

General Statements Pertaining to Test Structures. - Having developed an understanding of the utility and the limitations of each of the existing test structures, one should choose the test structures to be used in a particular experimental effort with the expected problem areas in mind. For example, a new insulator material or process should be evaluated first on simple large-area MOS capacitors. The effects of plastic coatings or encapsulation would be much more likely to be found by measuring the reverse current and the breakdown voltage of the p-n junction diode, the channel current of the surface ion test structure and, perhaps, the flatband voltage of the high P/A MOS capacitor.

Improved Test Structures

Having the benefit of the experience from developing the first set of test structures, the following improvements could be suggested:

1. The large-area MOS capacitor could be reduced in size by at least 50% so as to conserve chip area.
2. More efficient use could be made of the chip area by reducing the spacing between test patterns and using common expanded contacts for more than one

test structure.

3. A lateral bipolar transistor without an overlying metal plate (such as that of the gate of the MOS transistor) could be added.
4. A surface ion test structure could be added having a geometry which is more effective with samples having a built-in inversion layer.
5. An extra mask could be added to the set to form an overlying metal field plate over the test structures to provide a barrier to mobile ions from the outer insulator layers or from the ambient, to prevent the effects of surface ions, and to determine whether mobile ions at an insulator-insulator interface can migrate laterally to influence device stability.

The Use of Test Structures for Process Control and for Analyses of Yield and Stability Problems

As microcircuitry is made more and more complex, there is a greater need for discrete test structures for analytic and control purposes.

Test structures can be used in connection with microcircuit (of all levels of complexity) production processes in at least three ways as described below.

Test Structures on Each Chip. - A few small-area test structures can in many cases be designed onto each chip. Each complex microcircuit chip should have a discrete device of each principle type which is included in the circuit.

Philco-Ford uses this technique in the production of some MOS microcircuits. Each chip has two discrete MOS transistors - one with an oxide under the gate like that under the gates of the transistors in the circuit and one with an oxide like that in the field between the elements of the circuit. These devices provide a capability to measure the threshold voltage and transconductance of the transistors, the field inversion voltage (a measure of how easily circuit-degrading channels can develop) and diode characteristics.

Complex bipolar circuits should include discrete bipolar transistors on each chip to provide a similar monitoring capability.

Each chip, of either MOS or bipolar type circuitry, should contain a surface ion test pattern.

With a little ingenuity, one might combine a discrete MOS transistor and a surface ion test structure into a single simple device. This combined test device might be designed as a simple MOS transistor in which the gate covers only half of the width of the channel formed by the source and the drain.

MOS capacitors are generally not practical on each chip because they take up a fairly large area. For example, to have a capacitance of only 5 pF on a 5000 Å thick oxide, the area would have to be 115 $mils^2$.

In some cases, additional pads to those needed for the standard circuit could be added to permit discrete device testing of some of the circuit devices.

In the case of circuits having more than one insulator level, the mask set should be designed to provide a means for measuring the thickness of each insulator level. This is most conveniently accomplished by using masks designed to leave, in the finished chip, regions with only one layer of insulator of each type. To make the thickness of each of these regions easy to measure, they should be adjacent to a region of bare silicon. The scribing region is bare silicon.

Test Structures Formed by Modification of Standard Metalization Pattern. - Test structures can be formed on standard microcircuit chips by changing the metalization pattern.

For example, a diffused resistor and an isolation region in a bipolar microcircuit can be used as source and drain regions of an MOS transistor when a metal gate is provided across these regions. This provides a means for measuring threshold voltage which provides a measure of the effective

charge density on the oxide in a smaller area than would be needed for an MOS capacitor. The same structure can also be conveniently used to measure surface ion effects.

This technique can be improved by making slight changes in the diffusion patterns under the metal pattern. These changes appear on every chip, while those in the metal pattern appear only on the test structure chips. Note that row-on-row, or column-on-column, alignment is not needed in this case. Philco-Ford is presently using this technique on microcircuits in production.

Threshold or inversion voltages on a given oxide thickness are frequently different in areas beneath a metal layer and in adjacent areas not covered by metal. One might be able to measure inversion voltages in regions not covered by metal by measuring the minimum voltage that is required on the metal to produce significant increases in channel current in structures designed to study surface ions.

Of course, as the number of levels of metal and insulator increases, the number of test structures should be increased. For example, whenever an additional layer of metal is designed into a multilevel insulator microcircuit structure, it permits one to test the flatband voltage or the inversion voltage on each type of region in the chip with metal located at an additional level. This provides a means for evaluating the effects of both first layer and second layer insulators on the same type of underlying silicon.

Other test patterns should also be included on each wafer to measure properties other than electrical properties, for example, pinhole densities, dielectric strength, dielectric constant and loss factor. These test patterns are beyond the scope of the present program.

Universal Test Structure Chip. - A universal test structure chip that can be included on the wafer for a large variety of types of microcircuits provides the following advantages:

1. It can easily be included on the wafer with microcircuits of many kinds.
2. Standard techniques can be developed for mounting and testing these test structures.
3. Information taken from test structures made with one microcircuit process can be more easily compared with information taken from test structures made with another process.

Test Structures for Use in Production

We suggest the following as a good practical way to use test structures to improve the reliability and performance of production quantities of complex LSI circuits.

1. Within the limits of practicality, discrete test structures should be included on each chip to permit determination of the exact nature of performance, yield and stability problems.

2. Several chips on each wafer should have a metalization pattern that permits the measurement of discrete transistors in the chip.
3. Several chips in the wafer should have a set of test structures that permit the measurement of the fundamental electrical properties of the oxide-silicon interface.
4. The R&D and product development groups that provide fundamental technical support to production should have a capability to build the test structures, to develop a good understanding of the effects of variations on materials and processes on the characteristics measured on the test structures and to correlate this fundamental knowledge with the testing data of production circuits.

The availability of appropriate test structures, test equipment and procedures is a necessary but not a sufficient condition for the successful production of reliable microcircuits. The test structures must be used diligently and intelligently. It is important that those persons using the test structures clearly understand the purpose and the limitations of each test. Hopefully, the reports on this program can be used to develop such understanding. It is important that the number of samples undergoing testing is chosen so

that the results are statistically valid and properly representative of the devices that are being produced. It is important that irrelevant measurements and tests be avoided; for example, there is little to be gained by measuring large-area MOS capacitors to study a problem of contamination from sources of ions, such as plastic coatings or encapsulants, that would not be expected to contaminate regions beneath the metal layers.

Finally, the evaluation of instability in test structures should be performed on a time scale, at applied voltages and in ambient temperatures and humidities that are like those to which the product devices may be subjected. Care must be taken in the design of accelerated tests. Surface ion effects have been observed to proceed at a slower rate at 125°C than at room temperature, presumably because there can be less adsorbed surface moisture at the higher temperature. Surface ion effects can also be accelerated by increasing the applied voltage, but it is important to recognize that, theoretically, given a supply of surface ions and a sufficiently high voltage on a given oxide layer, almost any silicon surface can be inverted. There is little to be gained by increasing the voltage to a level much higher than that to which the actual device can be expected to be subjected.

Improved Reliability by Improvements In Device and Process Designs

From the results of the work reported to date on this program, we conclude that the following steps associated with device and process design lead to reliable microcircuitry.

1. Minimize contamination, especially sodium, at all steps in the fabrication process. This is most important for MOS integrated circuits.
2. Minimize the moisture content on the outer surface of the microcircuit.
3. Include a phosphorus-containing layer in the oxide layer to getter mobile ions in the oxide. This can be done by diffusion at high temperatures when this is compatible with the rest of the fabrication process or it can be done in a low-temperature vapor plating process.

   Insulator layers with a capability to getter mobile ions (phosphosilicates) from adjacent regions provide more positive stability than layers (such as aluminum oxide) that are merely impervious to sodium ions. For example, a thin barrier layer will not provide stability if ions migrate in the insulator layer outside of the barrier layer.

4. Use controls to insure that the proper amount of phosphorus is present in the finished devices to assure the desired results and that this amount is being reproduced.
5. Design the process to provide a net charge density in the oxide that makes the circuit most tolerant of the effects of mobile charge.
6. Avoid the use of processes, materials and structural designs that yield results that are difficult to reproduce.
7. Build the device with an oxide of sufficient thickness that the inversion voltage is higher than the operating voltages of the device.
8. Include in the processing specifications a specified allowable range on the effective charge density in oxide layers at particular points in the microcircuit, just as lifetime, resistivity and other parameters are now specified for the silicon.
9. To minimize surface ion problems, the design rules should forbid areas having thinner oxides in regions not covered by metal than the oxides in nearby regions covered by metal. Visual inspection should be used to insure that this condition does not occur due to misalignment.

CONCLUSIONS

A good understanding has been developed of the fundamental electrical properties of the Si-SiO_2 interface in structures having two or more dielectric layers on silicon. This understanding will improve the capability to build large scale integrated circuitry with high yield and reliability at a relatively low cost.

Specifically, conclusions include the following:

1. Vapor plated SiO_2 (deposited at 400°C) is the most promising second-layer oxide material, of those studied in this program. However, further work is necessary to establish the causes of variation in both the fixed and mobile charge density from lot to lot.
2. The inclusion of phosphorus in SiO_2 vapor plated at 400°C on thermally grown SiO_2 stabilizes and improves the reproducibility of the electrical properties of the oxide and of the silicon-oxide interface.
3. The polarization of phosphosilicates prepared at 400°C is similar to that reported for phosphosilicates made by diffusion at much higher temperatures. At

higher voltages on relatively thick layers of phosphosilicate there might be a stability problem due to polarization of the phosphosilicate.

4. Sodium appears to reduce the polarizability of low-temperature phosphosilicates.
5. R-f sputtered SiO_2 can contain a high density of mobile charge.
6. Vapor plated SiO_2-Al_2O_3 can be a source of large amounts of ions that are mobile in underlying thermally grown SiO_2.
7. Second layer oxides should be a getter for mobile ions.
8. The deposition of a second-layer dielectric can increase or decrease the effective charge density in an underlying oxide layer. It is possible that a second layer oxide could getter mobile ions and reduce surface charge densities and migration rates but still degrade the stability of devices because of a change in the fixed charge density that causes the device to be more sensitive to small amounts of mobile charge.
9. An MOS capacitor with a high perimeter-to-area ratio is useful for studying ion migration from areas adjacent to areas beneath metal layers. It has been shown that this type of contamination can be caused by photolithographic processes.
10. A very useful test structure has been developed for

studying the kinetics and effects of surface ion migration.

11. The recognition of surface ion effects becomes more important as techniques for minimizing the density of mobile ions in the insulator become more effective and better understood. Surface ion effects are especially important in samples having high resistivity silicon and low Q_{ss} densities in the oxide.

12. The model for the kinetics of surface ion migration has been improved and extended to include the situation in which the density of surface ions is dependent on the surface potential of the oxide.

13. Surface ion migration is slower when the surface has a minimum of adsorbed moisture.

14. Surface recombination velocities have been compared on samples consisting of a single layer of thermally grown oxide, on samples consisting of vapor plated SiO_2 on thermally grown oxide, and on samples consisting of vapor plated SiO_2 on a phosphorus-diffused thermally grown oxide. No significant differences were found.

15. Studies of the effects of a junction coating and of plastic encapsulation show that the main cause of

instability is mobile surface ions in regions adjacent to the metal. Mobile ions were not found in the oxide.

16. The most effective test structures for studying the effects of ambient materials are the junction diode and the surface ion test pattern.

17. The present state of knowledge concerning techniques for building the maximum reliability in microcircuits in production includes:

    a. The design and understanding of a useful set of test structures for measuring fundamental properties of the $Si-SiO_2$ interface. This understanding includes a knowledge of the advantages and disadvantages of each specific test structure.

    b. Further suggestions for improving test structures.

    c. A number of specific approaches for using test structures for process control and for the analysis of LSI yield and stability problems.

    d. From a broader view, understanding of the most effective role for test structures in the manufacture of reliable microcircuitry.

RECOMMENDATIONS

The following objectives should be pursued in future work.

1. The effectiveness of thicker oxide layers to reduce surface-ion-related instability should be determined.
2. The values of Al_2O_3 and TiO_2 as second-layer oxides should be established.
3. Investigations should be conducted to determine whether r-f sputtered SiO_2 can be made more stable by the use of purer source materials or possibly by the inclusion of phosphorus in the source.
4. The causes of nonreproducibility and instability of vapor plated SiO_2 layers should be determined.
5. The effects of second layer oxides on microcircuit structures having oxides modified by prior diffusions such as those used in the fabrication of all types of integrated circuits should be determined.
6. The possibility that a second layer metal field plate can be used to stabilize LSI circuitry should be investigated.
7. The effects of second layer oxides on microcircuit structures having ⟨100⟩ oriented substrates should be compared with those on ⟨111⟩ oriented substrates.

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JOURNAL ARTICLES/ORAL PRESENTATIONS

Appendix A consists of an updated version of a paper that was distributed to the attendees of the 1968 Semiconductor Interface Specialists Conference in Las Vegas, Nevada. It has been accepted for publication in the forthcoming special MIS issue of the IEEE Transactions on Electron Devices.

Appendix B consists of a paper that was orally presented at the 1968 Semiconductor Interface Specialists Conference. It has been accepted for publication in the forthcoming special MIS issue of the IEEE Transactions on Electron Devices.

APPENDIX A

ADDITIONAL BIBLIOGRAPHY OF METAL-INSULATOR-SEMICONDUCTOR STUDIES*

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ABSTRACT

A supplementary bibliography containing 158 papers in the field of metal-insulator-semiconductor theory and technology updates the bibliography previously published in these transactions (ED-14, 728-749).

The classifications are as follows:

MOS transistor behavior

Physics

Preparation of oxide layers

Techniques for evaluating insulator layers

Device fabrication technology

Radiation effects

Alternative materials to SiO_2

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ADDITIONAL BIBLIOGRAPHY OF METAL-INSULATOR-SEMICONDUCTOR STUDIES*

Earl S. Schlegel, Member IEEE
Philco-Ford Corporation
Microelectronics Division

This bibliography has been prepared to update the bibliography that was published in the November 1967 special MIS issue of these transactions (ED-14, 728-749).

The purpose and scope are the same as stated for the first bibliography.

The papers have been classified according to the same groupings as those of the first bibliography. Summaries of the information in the items of this additional bibliography have not been prepared.

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*This bibliography has been in part supported by the Electronics Research Center under NASA Contract NAS12-544.

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APPENDIX B

BEHAVIOR OF SURFACE IONS ON SEMICONDUCTOR DEVICES

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ABSTRACT

A study of the effects and behavior of surface ions on planar semiconductor devices has extended the theoretical understanding to include the case in which the total mobile surface ion density is determined by the net surface ion density induced by the surface potential on the oxide. We describe a useful test structure for the measurement of surface ion behavior and cite its advantages. We have measured the effects of time, humidity, temperature, voltage, and the previous testing history of the device on the behavior of surface ions.

INTRODUCTION

Mobile ions on the outer surface of oxidized silicon have an important influence on the stability and performance of microcircuits. In 1959, Atalla et al.[1] reported on the influence of surface ions on the characteristics of oxidized diffused silicon

junctions. They observed drifting in the reverse current due to the formation of channels resulting from surface ion migration. They explained the observed phenomena as being due to the drift of ions on the surface of the oxide in the fringing field where the junction intercepts the silicon surface. Shockley et al.[2,3] used the Kelvin vibrating condenser to measure potential differences across the oxide layer and they integrated currents to show that the formation of channels and changes in diode characteristics are caused by the accumulation of charge on the surface of the oxide. Surface ion effects and several techniques for minimizing them have also been discussed by Metz[4], Schnable et al.[5], Schroen[6,7], and Kang[8]. Surface ions can be an important cause of instability in LSI structures in which the densities of mobile ions and immobile charge (Q_{ss}) in the oxide have been minimized.

Snow[9], Shockley et al.[3], and Schroen[7] have developed a theoretical analysis of surface ion motion based on an assumption that the density of surface ions is independent of time and distance. They derived the equation

$$\frac{\partial V}{\partial t} = \frac{1}{C_o R_\square} \frac{\partial^2 V}{\partial x^2} \quad , \tag{1}$$

for which the solution is

$$V = V_o \operatorname{erfc} \left(\frac{R_\square C_o x^2}{4t} \right)^{1/2} \tag{2}$$

Having observed that surface-ion-induced inversion layers formed in proportion to the square root of time, they concluded that their assumption of a constant surface resistivity, $R_\square$, was justified. They calculated values for $R_\square$ from their data.

In the following discussion, we describe an extension to the model and consider its implications. We also describe a very useful and simple test structure that we have used to obtain the body of data that is presented here.

THEORY

In the previous analysis it was assumed that the surface conductivity is constant and that the time-dependent behavior of the surface charge is determined by the surface resistivity, $R_\square$, and the oxide capacitance, C_o. We have considered the possibility that the net mobile ion density is essentially equal to the total mobile ion density and then this total ion density is dependent on the electrostatic potential on the surface. In this case, the time-dependent behavior is dependent on the ionic mobility which determines the ionic transit time.

When the total mobile ion density is a significant function of the surface potential of the oxide, it will be shown that the differential equation takes the form

$$\frac{\partial V}{\partial t} = \frac{1}{C_o R_\square} \frac{\partial^2 V}{\partial x^2} + \frac{\mu}{2} \frac{\partial^2 (V^2)}{\partial x^2} \quad . \tag{3}$$

Assuming one-dimensional geometry, the equation for charge conservation can be written in the form:

$$\frac{\partial \sigma}{\partial t} = \frac{-\partial j}{\partial x} \quad , \tag{4}$$

where σ = the net charge density per unit area,

t = time,

j = the current density per unit width,

x = the distance.

And $$j = \sigma \mu E \tag{5}$$

where μ = mobility of the surface charges,

E = electric field along the surface.

Therefore,

$$\frac{\partial \sigma}{\partial t} = \frac{-\partial (\sigma \mu E)}{\partial x} \quad . \tag{6}$$

Let

$$\sigma = \sigma_o + \sigma_1 = \frac{1}{\mu R_\square} + C_o V \tag{7}$$

where σ_o = total mobile surface charge density at an oxide surface potential of 0 volts relative to the underlying silicon,

σ_1 = net charge added to σ_o by a surface potential (V) on the oxide,

$R_\square$ = surface resistivity at V = 0,

C_o = capacitance per unit area of a capacitor having the dielectric constant and thickness of the oxide,

V = surface potential of the oxide relative to the silicon.

Equations (3) and (4) combine to yield

$$\frac{\partial\left(\frac{1}{\mu R_{\square}} + C_o V\right)}{\partial t} = \frac{-\partial}{\partial x}\left(\frac{E}{R_{\square}} + \mu C_o V E\right) \quad . \tag{8}$$

This can be rewritten as

$$C_o \frac{\partial V}{\partial t} = \frac{1}{R_{\square}} \frac{\partial^2 V}{\partial x^2} + \mu C_o \frac{\partial}{\partial x}\left(V \frac{\partial V}{\partial x}\right) \tag{9}$$

and as

$$\frac{\partial V}{\partial t} = \frac{1}{R_{\square} C_o} \frac{\partial^2 V}{\partial x^2} + \frac{\mu}{2} \frac{\partial^2 V^2}{\partial x^2} \quad . \tag{10}$$

Note that when $\sigma_o \gg \sigma_1$, the equation reduces to that used by Shockley et al.[3], Snow[9], and Schroen[7], i.e., equation (1).

On the other hand, when $\sigma_o \ll \sigma_1$, the equation reduces to

$$\frac{\partial V}{\partial t} = \frac{\mu}{2} \frac{\partial^2 V^2}{\partial x^2} \quad . \tag{11}$$

It can be shown that the solution to equation (11) is

$$V = V_o \operatorname{erfc}\left(\frac{x^2}{\mu V_o t}\right) \quad . \tag{12}$$

This is the solution for the voltage (V) distribution on an oxide surface overlying a conducting material such as silicon, near a metal conductor overlying the oxide. The distance from the metal is x. The voltage on the metal, relative to the silicon, is V_o. The mobility of the surface ions is μ. The time since the voltage on the metal was increased from zero is t.

Note that the rate of growth of the inversion layer is proportional to the square root of the time in either solution [equation (2) or equation (12)]. Therefore, an observation that an inversion layer grows as the square root of time does not necessarily indicate that the surface conductivity is constant.

It should be possible to distinguish between the two conditions by determining the effect of the applied voltage on the time dependence of the inversion layer build-up. If the surface conductivity is constant, the time that it takes to build up a given percentage of the inversion layer would be independent of the applied voltage on the metal. In this case, the time rate of growth of the inversion layer can be used[3,7,9] to calculate the surface resistivity, $R_{\square}$. On the other hand, if the surface conductivity and the total surface charge density depend on the potential on the surface, the time it takes to build up a channel will be inversely proportional to the applied voltage on the metal. In this case, the time rate of growth of the inversion layer can be used to calculate the mobility of the surface ions.

The appropriate model in a particular case depends on the ambient humidity, the cleanliness of the surface, the oxide thickness, and the applied voltage. One should expect that at lower voltages and on thicker oxides the net surface charge density would be relatively lower. Therefore, the total surface

charge density is more likely to be constant and the analyses of Snow, Shockley et al., and Schroen should apply. At higher voltages, on thinner oxides and cleaner oxide surfaces, the net charge density will become significant in comparison with the total surface charge density, and then our extended model reported here is required. The possibility exists that on a given sample one might determine the surface conductivity from data taken at low voltages and the ionic mobility from data taken at high voltages. Having found the conductivity and the mobility from data taken, one could calculate an effective charge density for the region where $R_{\square}$ is constant.

Surfaces should be compared on the basis of the relative time dependence of their net surface charge density and not on their relative saturation level. The saturation level does not depend on the properties of the surface. It depends on the geometry of the device, on the dopant density of the semiconductor, and on the dielectric constant and thickness of the insulator. The time rate of change of the net surface charge density is a measure of the ionic density and mobility.

TEST STRUCTURE

We have developed a useful simple test structure for studying surface ion behavior. Figure 1 is a photograph of the top view of the test structure. Two p-n junctions are diffused

into the silicon wafer. These diffusion cuts are 5.25 mils long and 0.50 mil wide. They are spaced one mil apart. Contact cuts are made through the oxide over these diffused regions; then aluminum is evaporated over the wafer. This is then delineated into the pattern shown to form contact lands and two metal electrodes that lie over the oxide.

Functionally, surface ions are drifted by the application of voltages on the two metal electrodes, A and B. When a sufficiently large net surface charge density is accumulated on the oxide in the region between the two diffused junctions to invert the underlying silicon, the electrical resistance between the diffused junctions is greatly decreased. This is determined by measuring the current flow between the junctions under a low applied voltage.

The substrate was 5 Ω-cm, n-type, and of <111> orientation. The oxide was thermally grown to a thickness of 7000 Å, had a Q_{ss} of 2.4×10^{11} cm^{-2}, and was essentially free of mobile ions. Advantages of this test structure are:

1. It bears a close relationship to microcircuit structures,
2. It can be built into production wafers for simple monitoring of surface ion problems,
3. It can be subjected to accelerated testing.

EXPERIMENTAL DATA

The equipment for measuring surface ion behavior is shown in Figure 2. The silicon substrate is connected to the diffused region that is biased as the source.

As previously stated, the parameter that is most useful for comparing different surfaces is the time that it takes to develop a channel rather than the level at which the channel saturates. We therefore measure the channel current, at an applied channel voltage of 1.5 V, as a function of time for a given condition of applied voltages to electrodes A and B. We measured the time dependence of the development of the channel with an ion drifting voltage on either electrode A or electrode B, while the voltage on the other electrode was zero. Typical data has the form shown in Figure 3. If the voltage is applied to electrode A, there is an immediate increase in channel current because of the channel induced under electrode A. Immediately, after the voltage is applied, net ionic surface charge builds up on the oxide adjacent to the metal and the channel widens into the region not covered by the metal. The growth of the channel is shown in Figure 3. An analysis of the data shows that the channel current increases as the square root of time. Alternatively, one can apply the voltage to electrode B and record data such as that illustrated by the second curve shown in Figure 3. In this case, there is a

delay time before the channel is detected because the surface ions spread out from electrode B and a finite time is required to produce a channel between the diffused junctions. The availability of two electrodes, located as these are, for drifting the surface ions provides both a slow and a fast way for measuring a given surface condition, a useful choice when very fast or very slow effects are being studied. It also provides for additional ways in which the model can be checked.

Moisture is known to produce orders of magnitude change in the surface conductivity. It is also known that ambient relative humidity significantly influences the kinetics of channel formation and degradation of semiconductor devices. The effectiveness of the test structure described in this paper in revealing the effects of moisture is shown in Figures 4 to 6. Figure 4 shows the channel build-up for 31% and 80% relative humidity. The device was unsealed. The measurements were taken at 28°C. In each case, there was -50 V on B and 0 V on A.

To determine how quickly surface ionic behavior and levels of adsorbed water can be influenced by changing the relative humidity of the ambient, data was taken in room air under conditions in which a stream of dry nitrogen could quickly be directed onto the device and quickly removed. Figure 5 shows that surface ion behavior can be drastically altered in less than one second

by quickly changing the relative humidity of the ambient from 48% to dry (<15 ppm H_2O) nitrogen and back to 48%.

Figure 6 presents further evidence that water is an important determinant of surface ion behavior. This device was sealed in dry (<15 ppm) nitrogen in a TO-5 package. It was not baked before sealing. A channel was created by biasing for 15 hours with -50 V on A and 0 V on B at 125°C. The voltage on A was then reduced to zero and the decay of the channel was monitored at 125°C. After nearly two hours, the temperature was lowered to 25°C merely by taking the device from a well in a heated aluminum block on a hot plate. Nothing else was done; the unit was continuously in the measuring circuit. As the device cooled, the channel disappeared very quickly. We interpreted this to mean that there is an adsorbed layer of water at room temperature that contains mobile surface ions and that at 125°C this water is in the gaseous state and does not contribute as strongly to surface ion effects.

Figure 7 shows the result of another attempt to determine the effects of temperature. This device had 7000 Å of thermally grown SiO_2. It was sealed in a hermetic package in dry nitrogen without the vacuum bake. This data shows that the effect of temperature on surface ion behavior is negligible. The only effect of temperature appears to be on the mobility of the

carriers in the inversion layer. The effect of temperature is probably quite complicated. Temperature changes might influence the ion density, the ion mobility, and the amount of adsorbed moisture.

Another important variable is the testing history of the device. The time dependence of the channel current depends on whether an induced accumulation of surface ions from a preceeding measurement had been returned to the initial condition before the next set of data was taken. We find consistently that the first time we drift surface ions, they move more slowly than they do in subsequent measurements within a period of up to five or ten hours. After 24 hours, the rate of motion was almost as slow as it was originally. Figure 8 demonstrates this effect. One might infer that trapping or recombination is involved in the surface ion behavior.

Figure 9 again illustrates the effect of the testing history on surface ion behavior. In this case, the decay of the channel is observed after the voltage on A has been lowered to zero. The variable from curve to curve was the time that the voltage had been on A before it was decreased to zero.

From the form of our solution, equation (12), one can infer that if the time required to build up a channel is inversely proportional to the voltage on the metal electrode, the charge

density is proportional to the surface potential of the oxide. If this time is independent of the applied voltage, then one can infer, as did the previous investigators, that the surface conductivity is a constant, independent of the surface potential. We have attempted to take data that would clearly permit distinguishing between these two possibilities. We found the same square root of time dependence for the build-up of a channel as that reported by previous investigators. Figure 10 shows data from which one might infer that at low voltages the surface charge density is fairly constant and at high voltages it is proportional to the surface potential of the oxide. This device was sealed in dry N_2.

Two additional points can be made with the data in Figure 10. First, the 50-volt curve started to level off at a surprisingly low current. We find that at the 50-volt level, the saturation level of channel current depends on whether the 1.5 V is on the channel during the drifting of the surface ions. Without the 1.5 V on the channel during the time when the ions were being drifted, saturation would have occurred at a current two orders of magnitude higher. Second, this data can be used to make an estimate of the mobility of the surface ions. Assuming that the turn-on time is a measure of the transit time of the surface ions under the applied voltage, and that the path

length (ℓ) is the distance (17.5 μ) from the edge of electrode B to the ends of the diffused junctions, one can roughly calculate a mobility by the equation:

$$\mu = \frac{v}{E} = \frac{\ell^2}{tV} \quad , \tag{13}$$

where μ = mobility,

v = average velocity,

E = average field,

ℓ = 17.5 microns,

t = turn-on time,

V = voltage.

In this case, μ is calculated to be roughly 10^{-11} $cm^2/V\text{-sec}$. Shockley et al.[3] reported that their mobility was less than 10^{-8} $cm^2/V\text{-sec}$. Similar data for another device yielded a calculated mobility of approximately 10^{-12} $cm^2/V\text{-sec}$.

Figure 11 shows the results of other efforts to determine the effect of the voltage on the turn-on time of the channel current. In these results, the voltage dependence is much less clear. It may be that at 69% relative humidity, the total surface ion density before a drifting voltage is applied is higher than it is in a sealed package in dry nitrogen, and therefore the net charge may not contribute as significantly to the total charge as it did in the sealed package. Secondly, the relative

number of two or more types of ions with differing mobility may change with large changes in humidity level, and therefore the voltage dependence of the turn-on time may be different in situations with different relative humidity levels.

SUMMARY AND CONCLUSIONS

A test structure has been described that provides a useful and simple means for studying both the behavior and the effects of surface ions on planar semiconductor structures.

The theory of surface ion behavior has been extended to include the situation in which the surface ion density is dependent on the applied potential. It was shown that the criterion used by previous investigators for demonstrating that the surface conductivity is constant is invalid. The previous model, which assumed a constant surface conductivity, is most likely to be valid at low applied voltages, on thick oxide layers, and with relatively unclean oxide surfaces. The extension of the model described herein, which takes into account a changing surface charge density due to a changing surface potential of the oxide, is more likely to apply at high applied voltages, on thin oxides, and on oxides with clean surfaces. A criterion is given for determining which model best describes a given oxide in a given set of test conditions. A technique has been presented for obtaining a rough estimate of the mobility of surface ions. Mobility values of 10^{-12} to 10^{-11} cm^2/V-sec were measured.

Experimental data taken with this test structure show the dependence of the kinetics of surface ion behavior on time, humidity, temperature, voltage, and the previous testing history of the device. Ambient humidity is the most important variable influencing the kinetics of surface ion behavior. Surface ion behavior has been observed to change drastically in times shorter than one second, due to changes in the relative humidity of the ambient. On some hermetically sealed devices, surface ions have been observed to move faster at room temperature than at 125°C. This may be due to differences in the amount of water adsorbed on the oxide surface at the two temperatures. On the other hand, on other similar devices, temperature appears to have very little effect on surface ion behavior. We find that surface ion behavior is strongly dependent on the testing history of the device, that is, surface ions move much faster the second time they are drifted (within a period of tens of hours) than the first time.

ACKNOWLEDGEMENTS

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We also acknowledge the assistance of M. Selser of our Santa Clara R & D Department, particularly for his helpful discussion of the manuscript.

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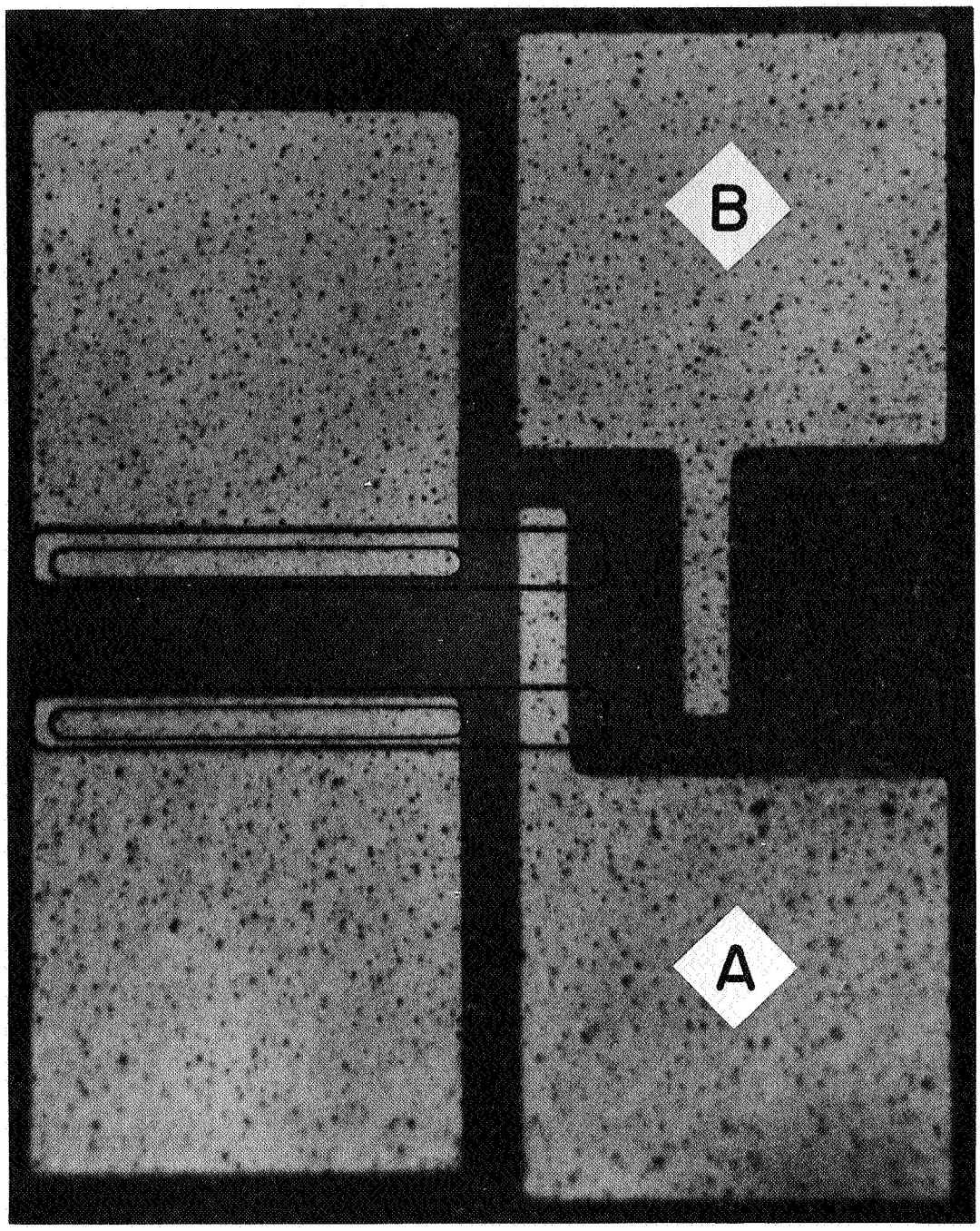

Figure 1. Top view of surface ion test structure.

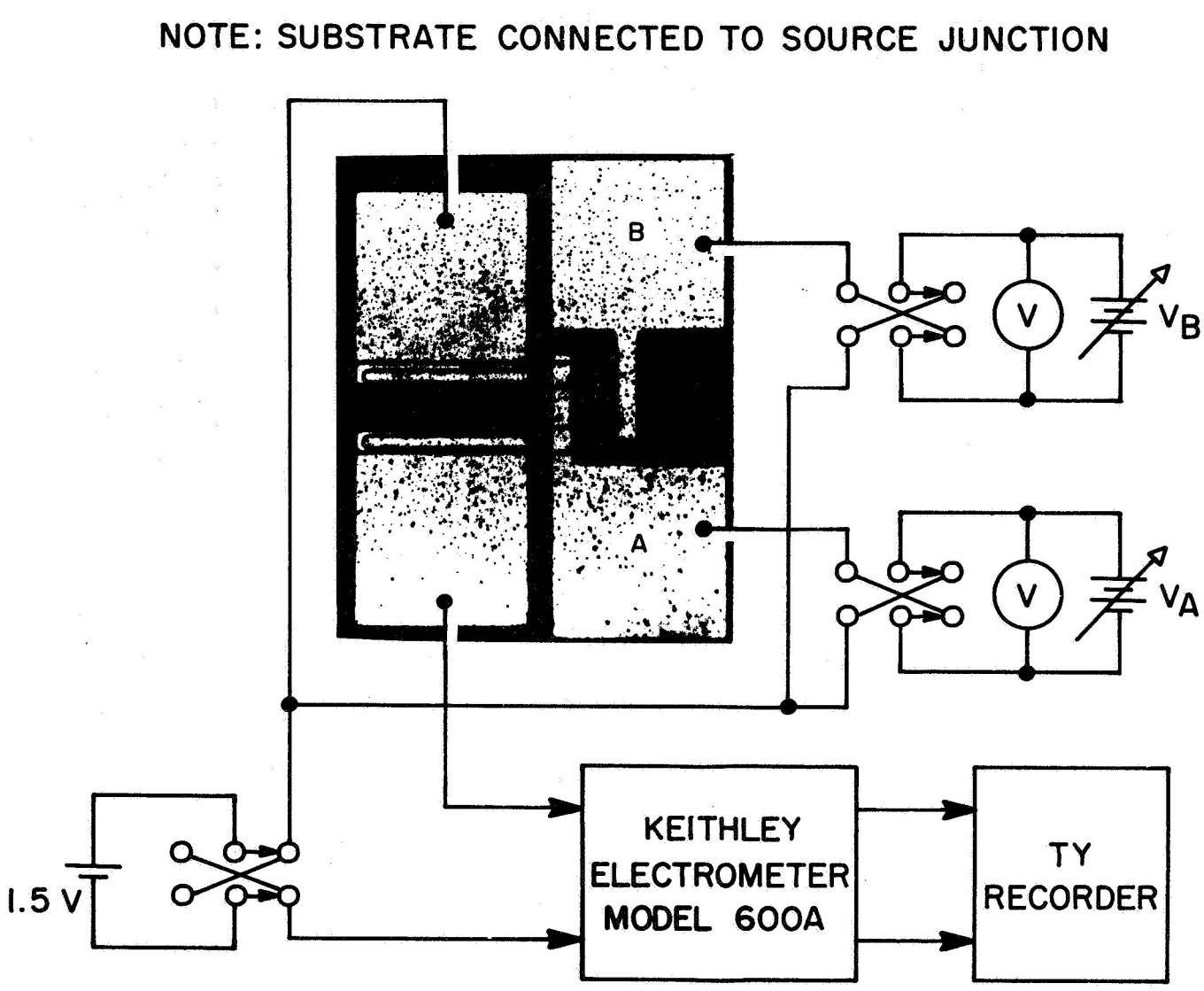

Figure 2. Surface ion measurement equipment.

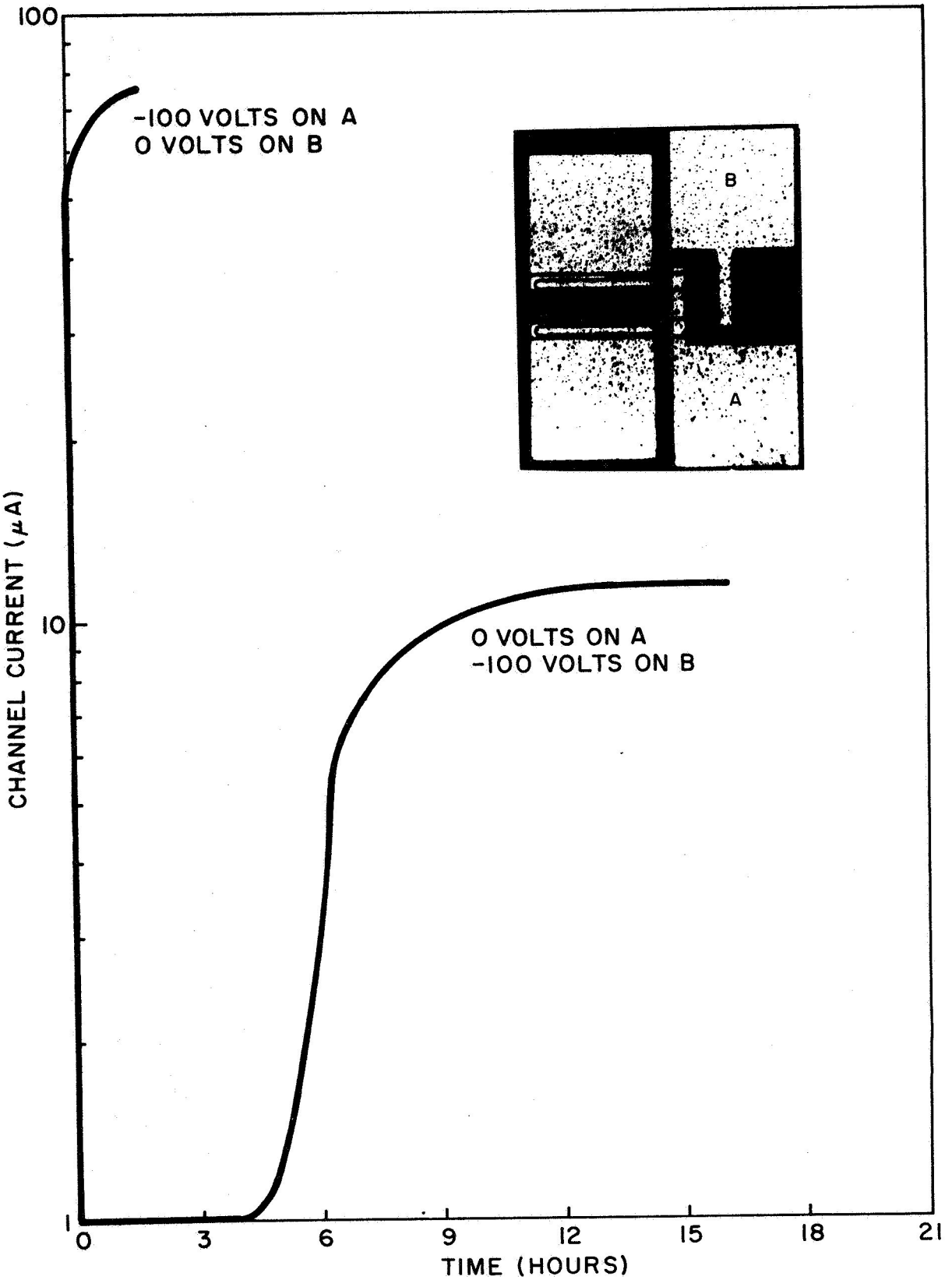

Figure 3. Dependence, at 28°C, of channel current on time.

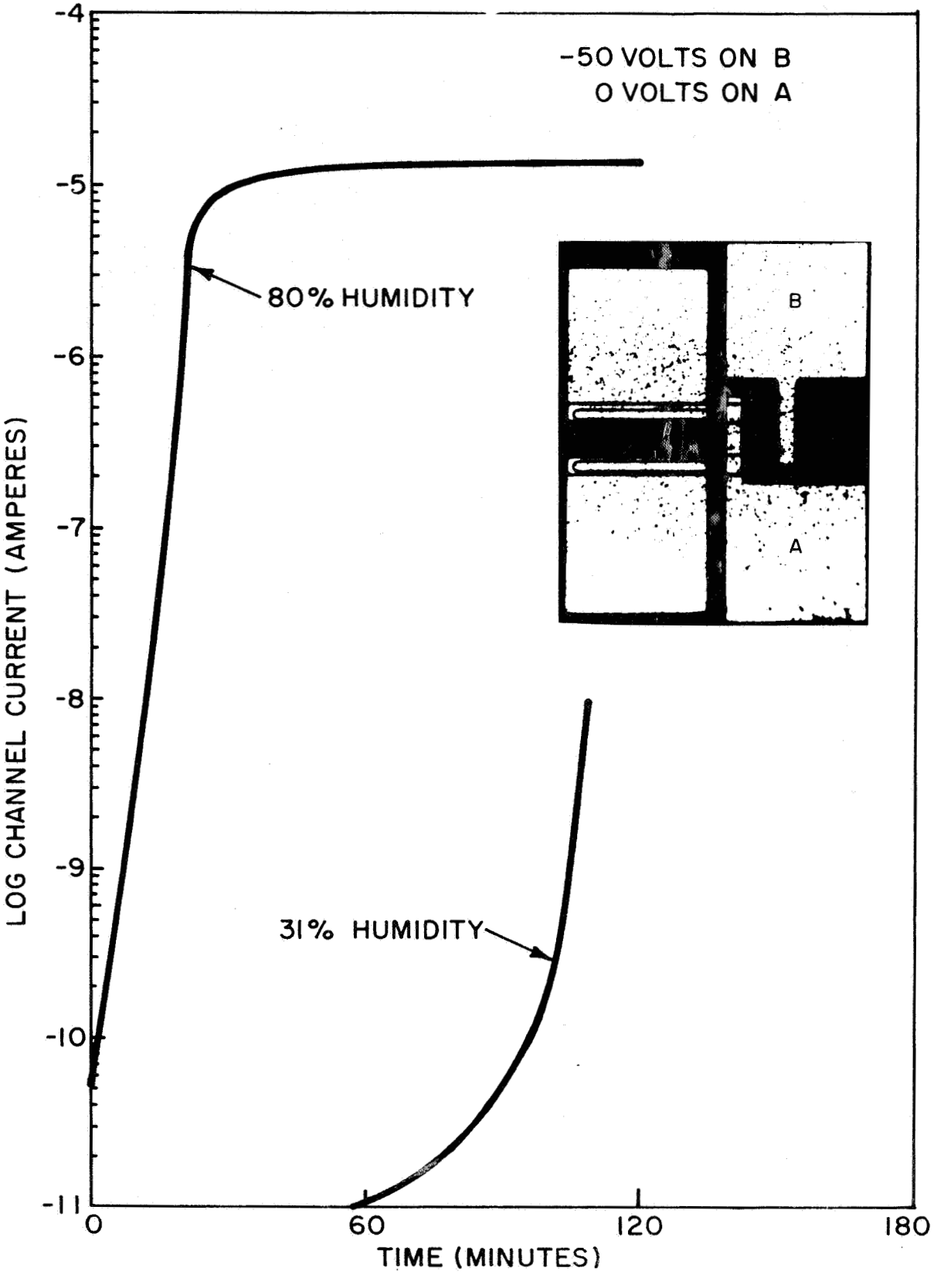

Figure 4. Dependence, at 28°C, of channel current on relative humidity.

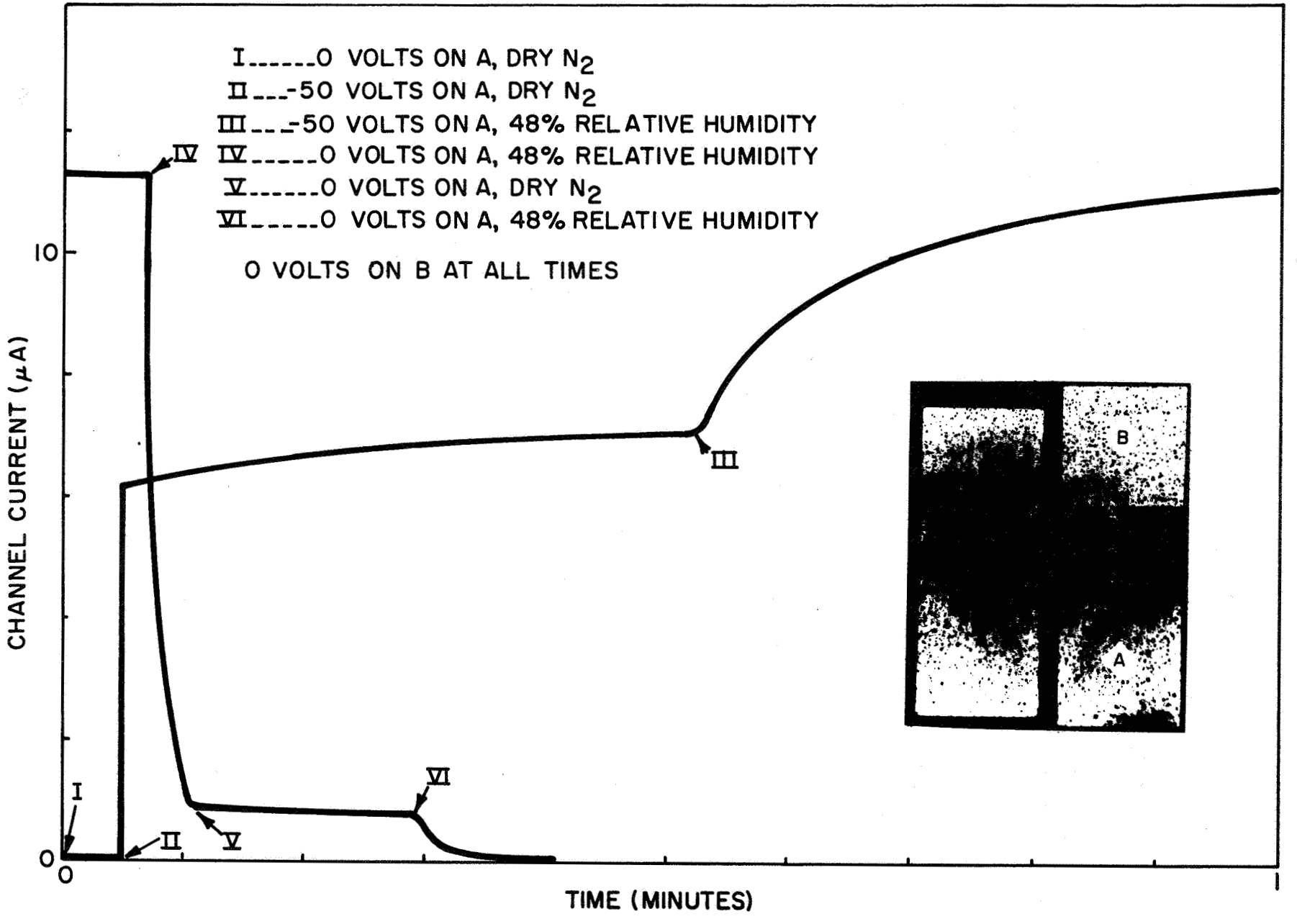

Figure 5. Changes in surface ion behavior, at 28°C, due to rapid changes in relative humidity.

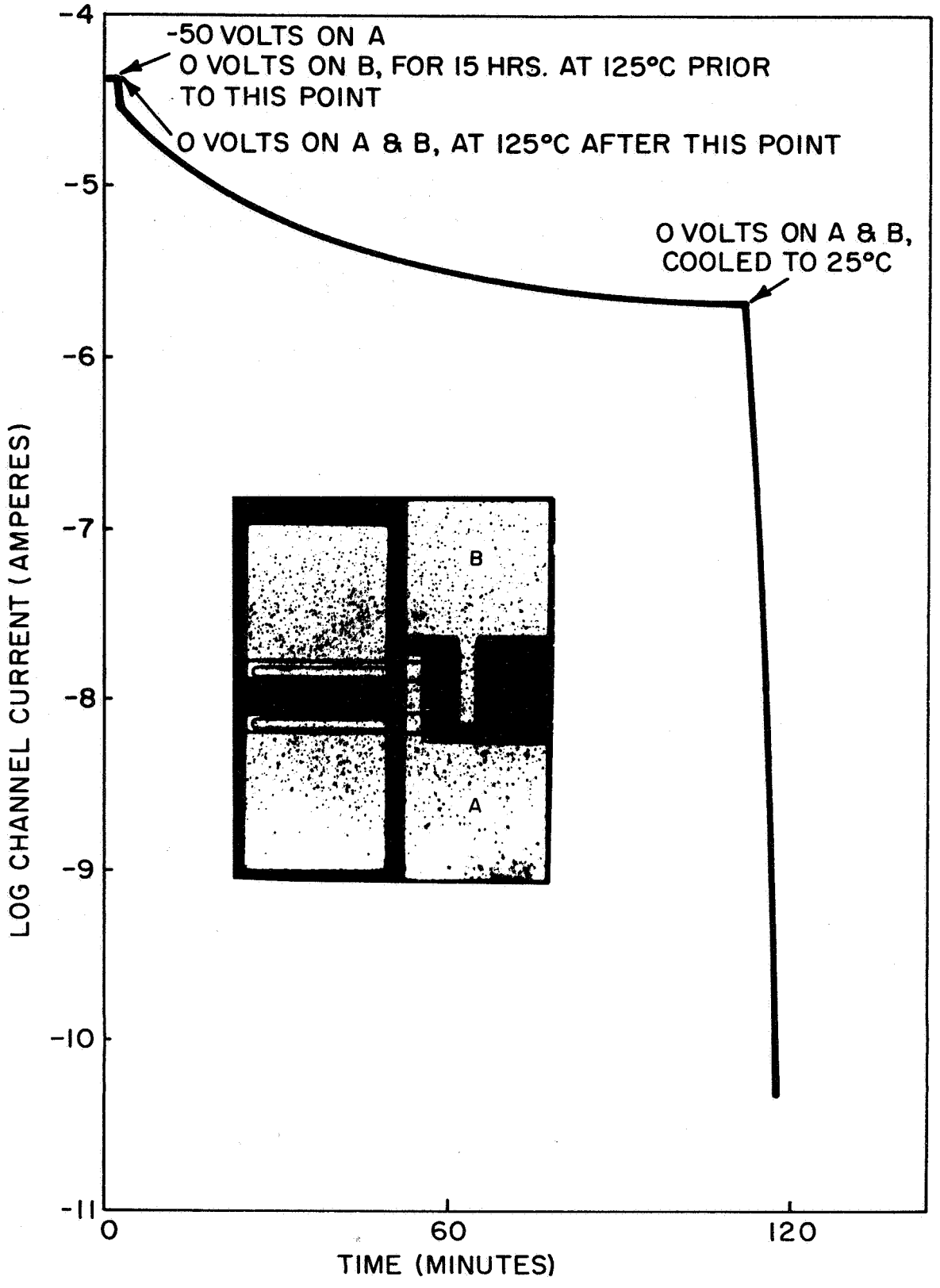

Figure 6. Effect of temperature on the rate of disappearance of a surface-ion-induced channel in a hermetic To-5 packaged device.

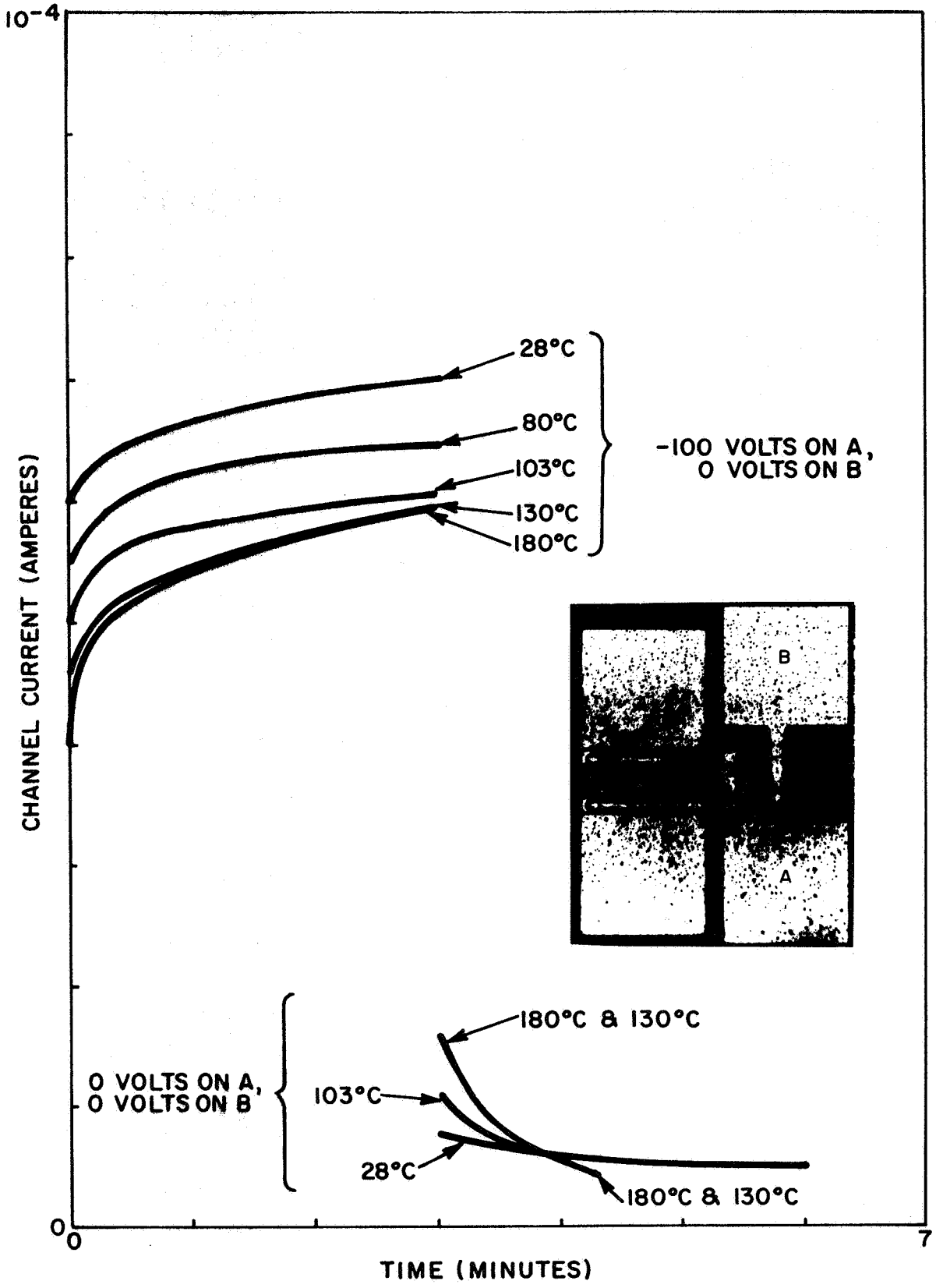

Figure 7. Effect of temperature on channel formation and extinction in a hermetic TO-5 packaged device.

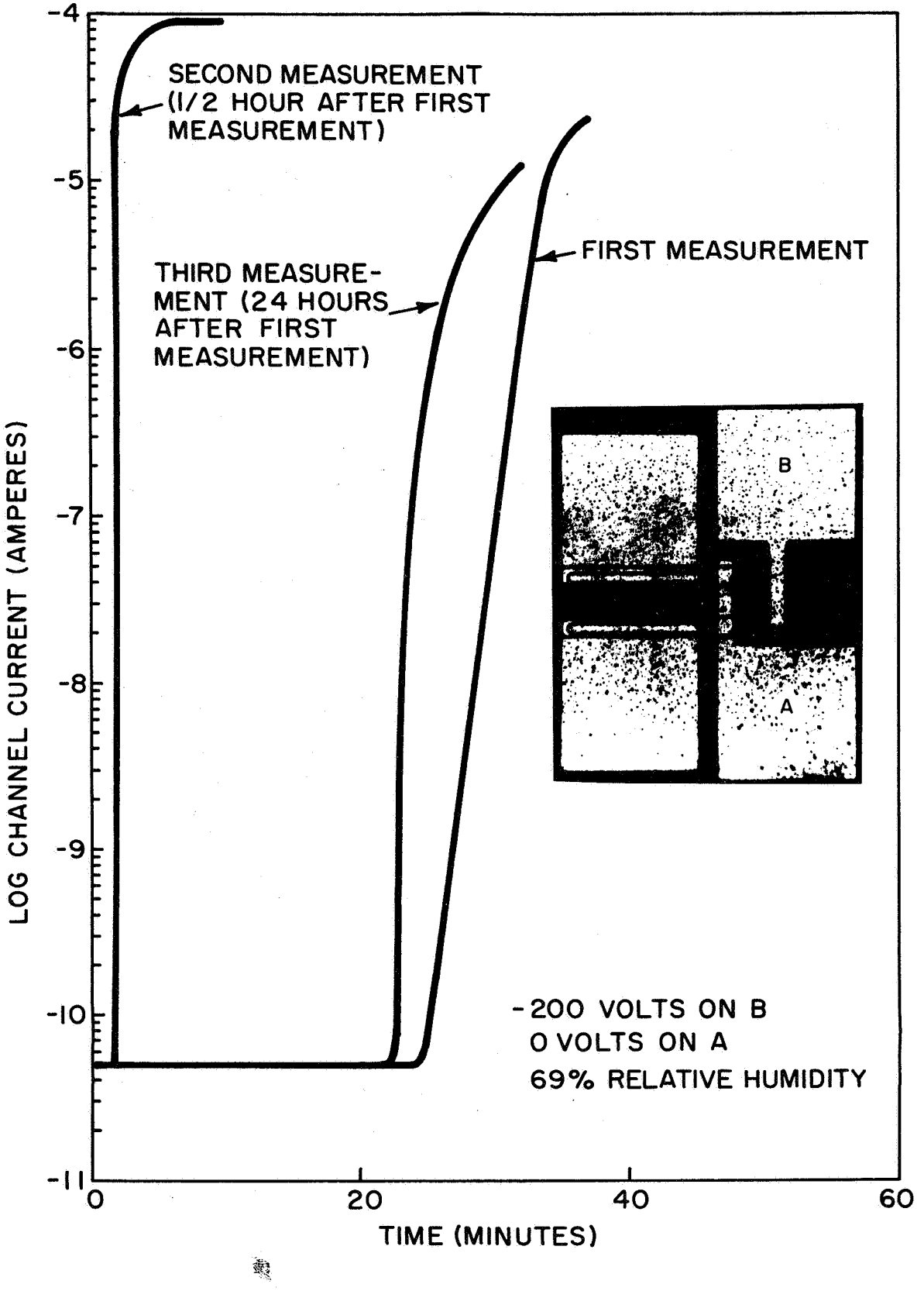

Figure 8. Effect of testing history on channel formation, at 28°C, in a hermetic TO-5 packaged device.

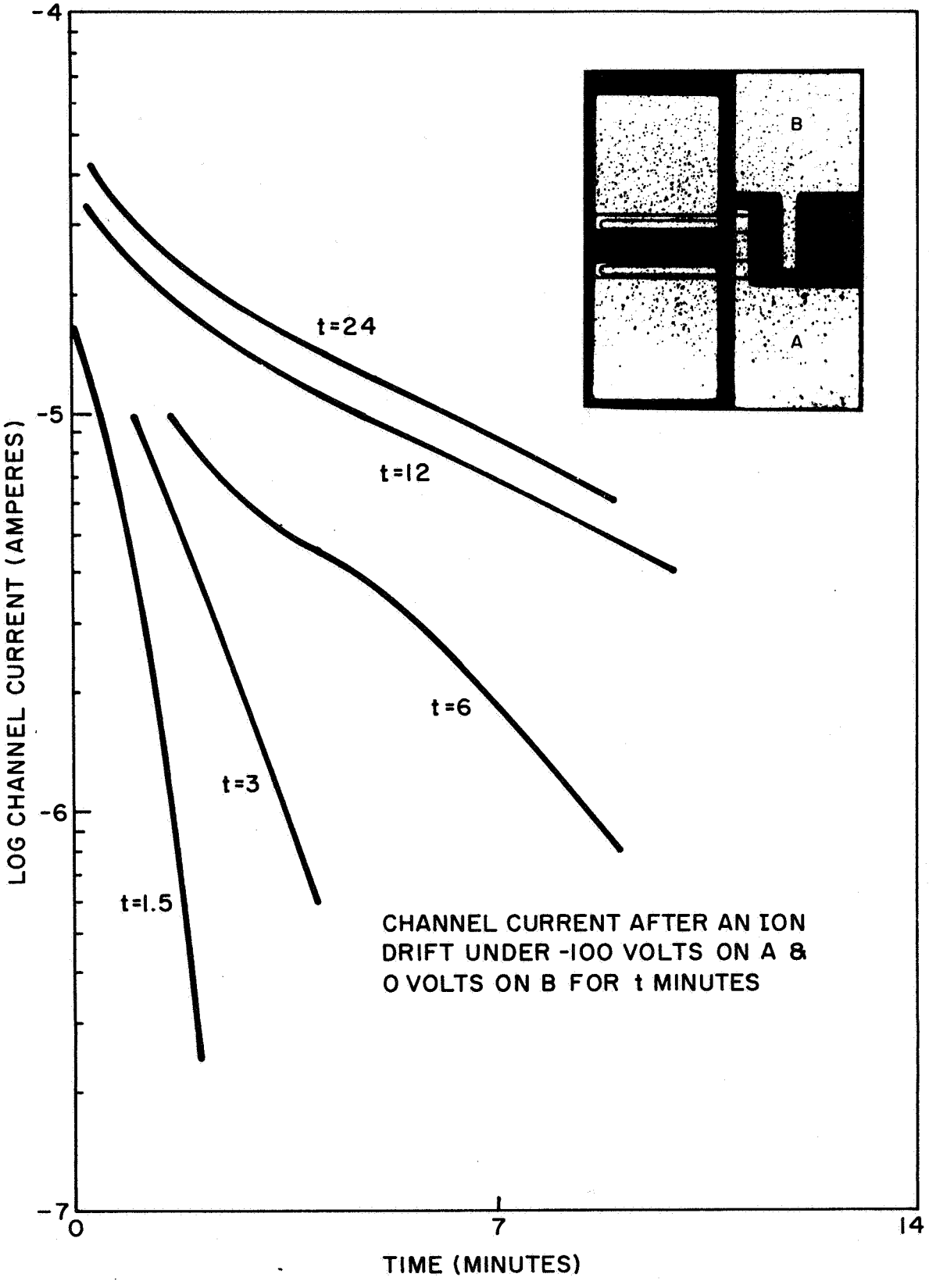

Figure 9. Effect of testing history on channel extinction, at 28°C, in a hermetic TO-5 packaged device.

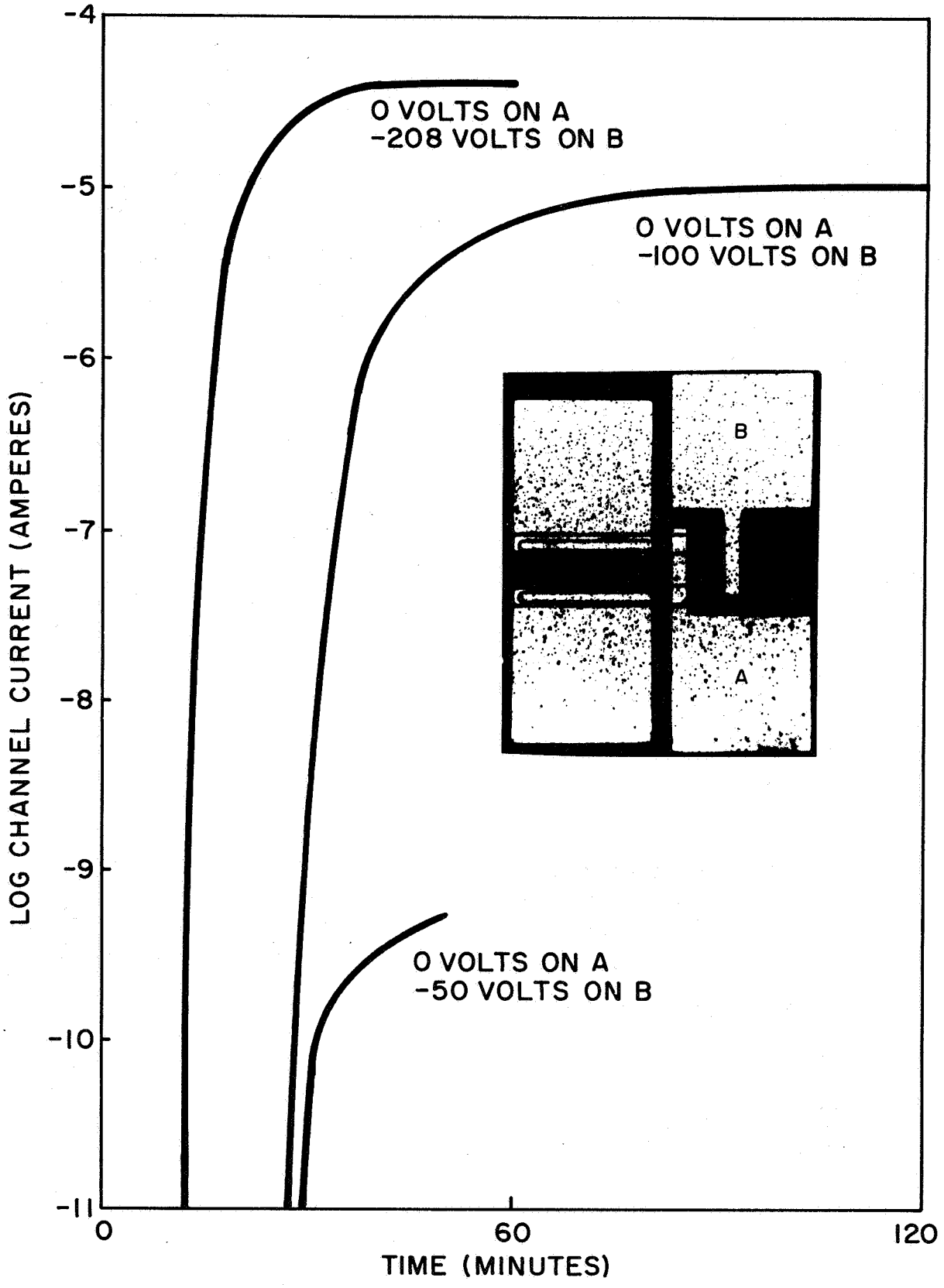

Figure 10. Dependence, at 28°C, of channel turn-on time on voltage (sealed in dry N_2).

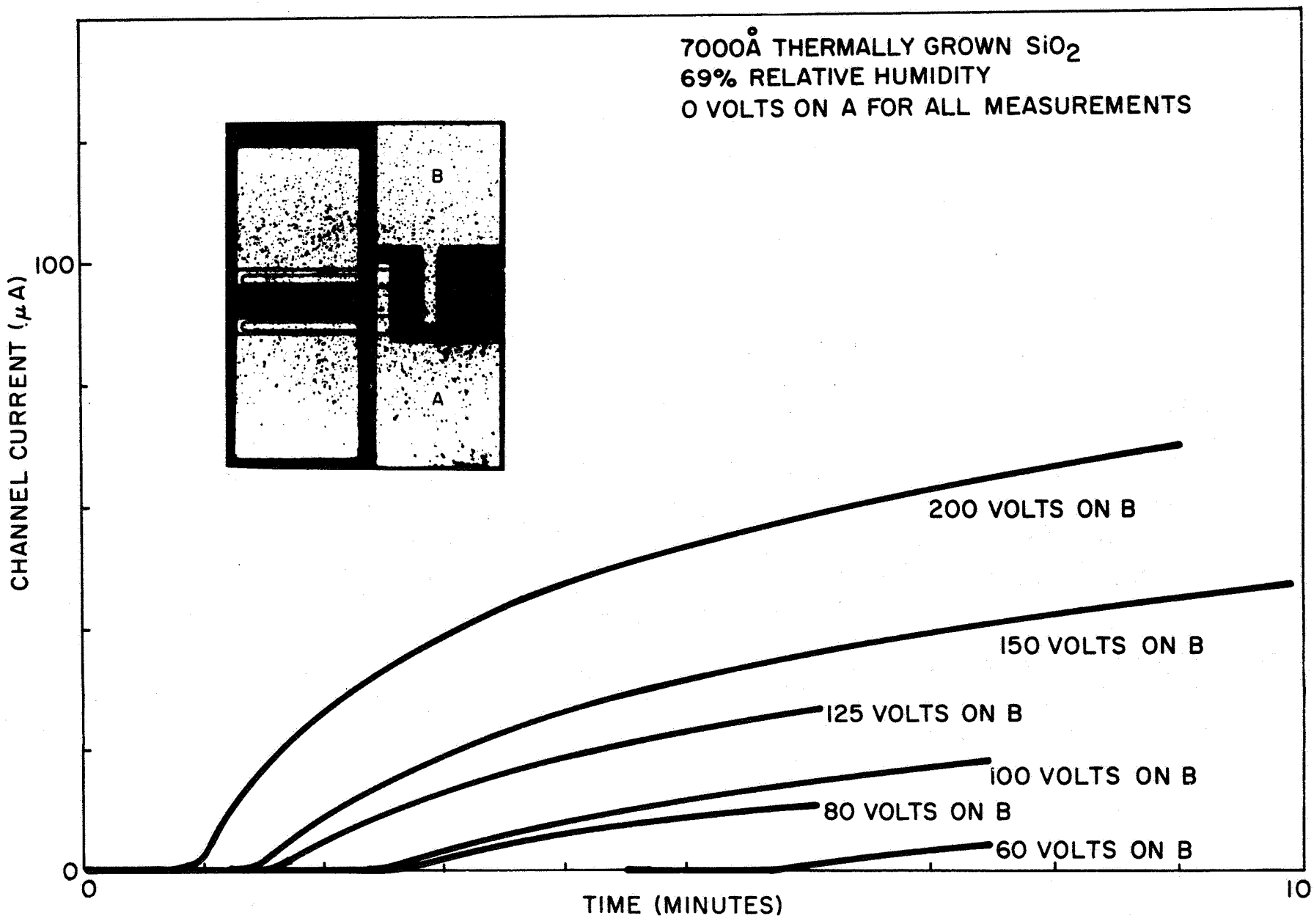

Figure 11. Dependence, at 28°C, of channel turn-on time on voltage (nonsealed device).

APPENDIX C

NEW TECHNOLOGY

To conform to the requirements of the New Technology clause of the Contract NAS12-544, a review meeting was held to determine the reportable items. Personnel participating in the review included G.L. Schnable, the Program Manager, and E.S. Schlegel, the principal investigator on the program.

A list of reportable items is given below. The items are innovations or improvements in the technology. No inventions were made during the performance of the work under the contract and no invention disclosures have been prepared. Philco-Ford does not consider these items to be susceptible to protection under United States patent laws and thus does not consider the provisions of parts (1) and (2) under paragraph (h) of Section III of the New Technology clause to be applicable.

No subcontracts were let under this contract.

1. Improved model for the kinetics of surface ion migration. (Pages 28-35; Appendix B).

Based on theoretical and empirical studies an improvement has been made in the model for the kinetics of ion migration on the outer surface of a microcircuit. The previous model

assumed that the surface conductivity is a constant. We have extended the analysis to take into account the dependence of the density of surface ions on the surface potential of the oxide. In this case the surface conductivity is time- and space-dependent. We have also demonstrated that the criterion used for testing the validity of the earlier assumption is not valid.

2. Low temperature phosphosilicate getters mobile ions. (Pages 13-14; 16-17.)

It has been demonstrated on this program that phosphosilicate layers that are vapor deposited at 400°C, getter mobile ions. It was previously known that phosphosilicate layers, formed by diffusion at much higher temperatures, effectively getter mobile ions. However, it is not possible to diffuse phosphorus into second layer oxides because the underlying aluminum layer forms an Al-Si eutectic which melts at 577°C. Vapor deposition of phosphosilicate at a temperature such as 400°C makes it possible to deposit a gettering second layer oxide material over aluminum metalization.

3. Low temperature phosphosilicate improves the reproducibility of the electrical properties of oxide layers. (Pages 47-52.)

Experimental data taken on this program indicates that

the inclusion of phosphorus in vapor deposited (400°C) SiO_2 significantly improves the reproducibility of the electrical properties of structures consisting of vapor deposited SiO_2 over thermally oxidized silicon.

4. Increasing dielectric thickness to reduce surface ion caused instability. (Pages 71-72.)

During this program, in connection with a detailed study of surface ion kinetics, it became apparent that surface ion effects can be best prevented by increasing the total thickness of the dielectric layers in the LSI structure. Flat band and inversion voltages are proportional to the total thickness of the dielectric layer. The surface potential that can be developed on the dielectric surface, at the dielectric-ambient interface, is determined by the voltage applied to the device. Therefore for a given operating voltage the problems of surface ions can be decreased by the use of dielectric layers having a greater total thickness.