PROCESS TECHNIQUES STUDY OF INTEGRATED CIRCUITS INTERIM SCIENTIFIC REPORT NO. 1

By

James E. Meinhard

May 1968

Prepared under Contract No. NAS 12-4 by
NORTH AMERICAN ROCKWELL CORPORATION
Anaheim, California

Electronics Research Center

NATIONAL AERONAUTICS AND SPACE ADMINISTRATION

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By James E. Meinhard

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SUMMARY

The purpose of this program is to investigate and resolve some of the dominant problems of modern planar technology, particularly those tending to impede its evolution into a large scale integration and ultimate reliability. A further purpose is to provide instrumental support services to NASA-ERC in failure analysis and instrumental capabilities. Categories of investigation are as follows:

Investigational Activities:

1. Failure Mechanisms Related to Oxide Passivation.
2. Failure Mechanisms Associated with Packaging.

Services:

1. Failure Analysis Service and Consultation.
2. Instrumental Capability Profile.

Past program activities on oxide passivation have provided insights into the origin of atomic species contributing to inversion and the origin of dielectric defects. Current activities are concentrated primarily on the latter problem where it has been shown that most of the dielectric defects in oxide layers are developed during the cooling of wafers after oxidation and follow an exponential decay with increasing oxide thickness. Current experiments show that diffusion barriers introduced prior to oxidation, or other means for slowing initial growth, tend to reduce virtual defect densities.

Previous packaging investigations have been confined to gas ambient studies in which the effects of hydrogen and of water were evaluated on the performance of various transistor samples. The program has been extended to other failure problems of importance to packaging as well as to environmental studies on integrated circuits. The present report summarizes the results obtained on exposing groups of integrated circuits to various ambient conditions. Effects of hydrogen are found to be non-specific and are deleted from further investigations on bipolar planar devices.

Failure analysis on Case Number CQF-101, comprising 89 npn transistors has been completed.

An initial instrumental capability profile was provided at an early stage of this program, a current version of which appears in the present report. Problems associated with the leak testing of integrated circuit packages are discussed.

Reproduction of this report has been referenced informally by North American Rockwell Corporation Autonetics Division Document Number C5-1471.12/501.

INTRODUCTION

Objectives

The primary objective of the investigations under Contract NAS 12-4 has been, from its inception, the development of advanced process techniques for the fabrication of high reliability silicon integrated circuits. This objective initially was formulated under two task items. The first item called attention to an instrumental investigation of planar processing techniques, with special emphasis on device surfaces, for the purpose of discovering and correcting failure modes in the following seven categories:

1. Effects of gas ambients during fabrication
2. Effects of traces of materials deposited during fabrication
3. Application of photoresist and photoetch techniques
4. Processing of the oxide
5. Scribing
6. Contact attachment
7. Effects of contact between the processing tools and the wafer during fabrication.

The second item formulated specific studies relating to interactions between the silicon and the highly insulating material in contact with it, and to the effects of such interactions on integrated circuit performance, including long term drift, which is of major concern in extended space missions.

The broad area of activity covered by this statement of work was made so deliberately, to provide flexibility in the attack on emerging problems in a rapidly advancing field, such as those relating to large scale integration, and to provide latitude in the assessment of the relative importance of such problems so that the work could be directed at all times to meaningful ends. A further advantage of this philosophy lay in the opportunity it afforded in the full utilization of the considerable instrumental capabilities and interdisciplinary skills of Autonetics without risking compartmentalization in specific areas. This type of approach is indeed necessary in dealing with a technology as complex and sensitive to minor perturbations as silicon planar processing. The broad approach also brings to bear Autonetics extensive operations and industrial knowledge viewpoint on reliability problems, a factor which is crucial to its satisfactory performance on major contracts with the Government. As a result, the massive records and compilations of data developed on previous component reliability programs have been accessible to serve as guidelines for investigations under the present program.

Redefinitions of Objectives

As work progressed, however, objectives were crystallized in certain areas and phased out in others, either because a satisfactory conclusion had been reached or because a solution to the problem had been reached within the industry itself. In general, these new Statement of Work items were drawn to more specific areas which could, however, still be categorized within the broader range first formulated, the intent being to reflect more precisely the content of current program activities and to provide a formal mechanism for support of new and important problem investigations. A case in point is the shift of major attention from the problem of sodium and hydrogen ions in silicon dioxide, which was being successfully attacked by Carlson at Texas Instruments, and others, to the equally ubiquitous but much less well understood problem of oxide dielectric defects. It is indeed gratifying to be able to report sound progress in the understanding of this important problem, particularly in view of its antecedent significance to the success of large scale integration.

In time, however, the rate of accumulation of new task items began to exceed their rate of completion. The apparent resulting extension of available personnel over many areas was, to a certain extent, exaggerated because of the presence of a certain degree of overlap among some items. While this attested to the consistency of the overall program it also created a somewhat over-ambitious picture of the activities undertaken which could lead to a potential dilution of accomplishment. Consequently the objectives of the program were redrawn into four categories of investigation as follows:

Investigational Activities:

1. Failure Mechanisms related to Oxide Passivation
2. Failure Mechanisms associated with Packaging

Services:

1. Failure Analysis Service and Consultation
2. Instrumental Capability Profile.

These categories reflect the overall purpose of the program, which is to investigate some of the dominant problems confronting planar technology and to seek solutions to these problems, as well as to provide NASA-ERC with instrumental support and consulting services. At the same time the reporting format was changed to reflect more clearly the resulting program consolidation.

In accordance with the principles stated above, previous accomplishments on contract NAS 12-4 are reviewed in this report in the context of the overall program objectives adopted in the original Statement of Work, and in subsequently adopted task items, as well as in relation to the current technological problems listed in the section below. The relevancy of each activity is thereby established. Documents evidencing these accomplishments are included in the Appendixes.

CURRENT PROBLEMS IN PLANAR TECHNOLOGY

The need for high reliability in the complex electronic systems required for space missions has motivated a significant investigation into the physical nature of failure in electronic devices. The necessity of such a study is a consequence of the rapid commercial exploitation of solid-state technology founded on the available understanding of the essential physics, chemistry, metallurgy, and crystallography. Consequently, the technology has evolved largely on a liberal application of empirical techniques in the development of manufacturing processes, leaving many gaps in the knowledge of atomic and molecular mechanisms capable of causing parameter drift or abrupt failures in devices. Such deficiencies necessarily have led to the frequent introduction of incompletely defined process changes for the improvement of reliability, performance specifications, and yields without recognition of many consequences of these perturbations on succeeding process steps and ultimate device performance.

Frequently the current literature offers over-optimistic solutions to current problems. A critical analysis of such reports often reveals claims that are either unsupportable or out of the context of present technology and lacking in the documentation necessary to produce hardware for systems use. Considering the number and variety of process treatments required for the manufacture of a single device it is not surprising, therefore, that the foregoing situation of conflicting data and over-optimistic evolutionary claims is currently a problem area.

In the list of problems that follows no attempt is made to give an exhaustive survey or to accommodate current process innovations of promise, such as beam lead technique or stacked layer technique. The list is derived essentially from Autonetics' current interaction with electronic component suppliers and its commitment to developing sources of highly reliable devices.

1. Cracked die

2. Unsatisfactory gross leak test of packages (see below)

3. Oxide dielectric defects

(Note: Items 1, 2, and 3 reflect a significant proportion of the failure modes currently prevailing in components utilized by Autonetics).

4. Sonobonding, aluminum/aluminum.

5. Packaging: leads are too long, often broken.

6. H_{FE} degradation under reverse bias. Degradation increases with temperature and is aggravated in shallow diffused devices.

7. Inferior heat sink: produces local overheating which may contribute to h_{FE} degradation, mass transport of metallization (see item 10) and, by heat-induced mechanical stress, cracked die.

8. Packaging: lack of hermeticity allows ingress of contamination, such as sodium. Entrance of moisture may produce lead corrosion (see below).

9. Corrosion of leads in an environment of 85 percent relative humidity at 85 F. Contamination and electrochemical effects are implicated.

10. Mass transport in conductors due to high current density. This is a self diffusion phenomenon, severe in aluminum but minimal in molybdenum/gold conductors. Advanced technology may have to abandon aluminum in some types of planar devices. In other types improvements in heat sink combined with more massive metallization may suffice.

The above list is considered to represent existing dominant problems of integrated circuit technology. The list undoubtedly will change as new processing concepts are introduced and various problems are overcome. Because of the reliability requirements demanded of its major manufactured products Autonetics of necessity must maintain a continuing awareness of these problems, and seek solutions therefor, as they arise. Consistency is thus clearly evident between the concerns of Autonetics regarding the procurement and analysis of high reliability components and program objectives under Contract NAS 12-4. Accomplishments under this contract are discussed in the following section.

ACTIVITIES COMPLETED

Failure Mechanisms Related to Oxide Passivation

Tasks completed in this area or discontinued for priority reasons, include the Statement of Work Items 1, 2, 3, 6, 7, 8, 9, 10, 11, 12. Tasks remaining are re-defined in continuing Item 15. Accomplishments and continuing efforts are discussed under the two general categories of inversion and dielectric defects.

Inversion model investigation. - The objectives of this investigation were to employ isotopic tracers to determine the contribution of mobile positive ions to inversion and to use EPR spectrometry to discover whether oxygen vacancies are present and potentially able to participate in inversion. At the time the original proposal was prepared no definitive experimental evidence existed capable of distinguishing between the positive ion model and the oxygen vacancy model. It was believed that more exact knowledge of the mobile species causing inversion would provide a basis for a solution to the inversion problem. Subsequently a number of investigators demonstrated electromigration of sodium ions through oxide layers, and precautions taken to exclude sodium from processing environments were found to yield devices more resistant to inversion. The general improvements due to sodium control made logical a decreasing emphasis in this area on Contract NAS 12-4. The following results have been accomplished on this program and were presented at an Electrochemical Society Meeting (Appendix A) in 1966.

Entrapment of hydrogen in thermal oxide grown in a moist ambient was demonstrated by using tritium tracer of 1000 millicuries/gram specific activity in the process gas and counting the weak beta activities in the resulting oxide samples. The oxides were found to contain approximately 10^{17} atoms of hydrogen/cm^3 oxide. The oxide beta activities were stable over a long period ot time, showing little or no tendency to exchange with atmospheric water. A later experiment by Burgess and Fowkes using a much lower specific activity gave a value of 10^{20} H atoms/cm^3, a result that was found to be experimentally unrepeatable on Contract NAS 12-4. The essential objective of the investigation was achieved, however, and later substantiated by the work of others. Hofstein (Ref. 1) has since demonstrated the contribution of hydrogen ions to drift instability in MOS devices.

Sodium ion occurrence in the oxide was investigated by neutron activation analysis of specimens from the tritium tracer runs. Sodium levels in the range of 10^{18} atoms/cm^3 were found. This result was in substantial agreement with those of Carlson, and others, and the investigation was closed.

Deuterated planar transistors were selected for inversion study with the initial intention of detecting electrochemically liberated deuteruim in the package ambient by mass spectrometry. A positive result would implicate hydrogen ion transport in inversion. Following the availability of the tritium tracer results, however, calculations showed that the available deuterium, even if completely freed, would be beyond the limit of mass spectrometric detection. The deuterated transistors then were

investigated through their activation energies of recovery from inversion. A difference between them and comparable hydrated transistors again would indicate hydrogen ion participation. An apparent difference between the two sets of transistors indeed was observed initially but was not substantiated in later experiments because repeated inversions and deinversions produced changes in the activation energies. Although the original objective was thereby thwarted the changes observed were in the direction of increasing inversion resistance and led to a proposed process innovation of "inversion hardening" by thermal and bias cycling (Appendix B), later published as Tech Brief 67-10176. The activity in this area was terminated with the achievement of this result.

The electron paramagnetic resonance experiments were performed on thermally grown silicon dioxide to investigate the oxygen vacancy model. Resonance data were taken on many samples grown wet or dry under varying conditions of temperature, ambient, and chemical contamination. Three resonance signals were detected from these oxides. One was from hydrogen entrapment and another from a possible electrode reaction between aluminum and the oxide that has been postulated to generate oxygen vacancies by Burkhardt at IBM. The third signal was shown to be related to both sodium and fluorine retention in the oxide. A detailed report of this work is given in Appendix C.

A further accomplishment in this area of effort was the preparation and delivery of a paper on the subject at the American Physical Society Summer Meeting, Seattle, Washington, 31 August to 2 September, 1967. An abstract of this paper is given in Appendix D.

Oxide dielectric defect investigation. - Most aspects of this investigation constitute a continuing effort and will be dealt with in detail in the "Continuing Activities" section of the report. Accomplishments include a paper delivered in 1966 (Appendix E) which evolved from earlier investigations (Appendix F) (Appendix G). A short technical note relating defect incidence with thermally induced mechanical stress (Appendix H) also has been prepared.

Failure Mechanisms Associated with Packaging

Tasks completed in this area, or discontinued because of a lack of conclusive results, are identified as Statement of Work Items 1-a, 4, and 13. The bulk of the work in this area has been directed toward an evaluation of the effects of hydrogen ambients on the performance of integrated circuits, partly because of various, and sometimes conflicting, reports of such effects and partly because analytical results at Autonetics frequently have disclosed the presence of hydrogen in integrated circuit packages. However, a significant degradative effect due to hydrogen was not found, and efforts to induce such an effect were abandoned. A further result of this program was a thermodynamic analysis of ambient gas effects (Appendix I) on materials normally present in packaged devices which corroborated the above results with respect to hydrogen interaction with silicon, silicon dioxide, aluminum, and aluminum oxide. Nevertheless, materials compatibility problems continue to plague the packaging art and are the subject of investigation under continuing Statement of Work Item 16. A more detailed report of this activity therefore is deferred to the section on "Continuing Activities".

Failure Mechanisms in Heteroepitaxial Systems

Action in this area, which was specified under Statement of Work Item 5 and designated as a low priority effort, was not taken. This decision followed an analysis of the potential impact of silicon on sapphire, and other hetero systems, on the immediate future of integrated circuit technology. It was concluded that the somewhat primitive state-of-the art, compared with conventional planar technology, would render highly uncertain the selection of meaningful device reliability problems for study.

Scribe and Break Damage

Activities in this area were specified under Statement of Work Items 1-e, 4, and 13 and were terminated after brief investigation. The objective of this investigation was to determine by defect etching or X-ray topographic techniques to what extent normal scribing operations introduced crystal damage capable of propagating into adjacent device areas. It was suspected that damage from this source could give rise to cracked dice during breaking operations or subsequent steps, such as packaging and lidding. If a correlation of this sort could be found, at least one origin of the cracked die problem could be recognized and corrected.

Scribe damage was investigated by etch-pit count technique but no evidence of defect propagation into surrounding lightly doped areas was found. The investigation was repeated at a later data but the highest observed total etch width was less than 0.004 in. in confirmation of earlier results. Although these results scarcely can be regarded as conclusive it was tentatively decided that scribe damage would constitute, at most, only a sporadic source of cracked dice.

Nonuniform Diffusion Doping

Effort in this area was covered by Statement of Work Items 1-ab and 13 and, although not dealt with in a conclusive fashion, was terminated after obtaining essentially negative results from a brief analysis of one potential source of difficulty. The objective of this investigation was to determine whether incomplete mixing of input gas compositions employed in diffusion steps led to persistent concentration gradients at wafer surfaces and nonhomogeneous doping. If such an effect were found to be present it would indicate a requirement for a process modification, such as a baffle system, to assure complete mixing, or a means to assure uniform wafer exposure as, for example, by mechanical wafer rotation. Calculations showed, however, that complete mixing occurs in the first 4 in. of furnace tube. Because the unoccupied input tube section employed by most processors is three to four times this distance it was concluded that incomplete vapor phase mixing was not a substantial source of doping irregularities and the invesitgation was abandoned. It is recognized, however, that nonuniform doping is a continuing problem and may become a deterrent to the development of large scale integration after other more pressing problems are resolved.

Failure Analysis Service

This service was defined in Statement of Work Item 14 and was terminated with the completion of the analysis of 89 npn transistors comprising Case Number CQF-101 (Appendix J). The objective of this service was to examine, on request, state-of-the-art components for inhomogeneities arising from process techniques. These analyses were to be performed in detail on components important to the Failure Mechanisms Branch, Qualifications and Standards Laboratory, NASA-ERC. This effort constituted a support function which was expected to reveal hitherto unsuspected inadequacies associated with fabrication steps as well as to characterize salient reliability problems peculiar to components from specific sources. Component anomalies were examined by established failure mechanism techniques from which performance predictions could be derived appropriate to the long term reliability and environmental requirements applicable to NASA missions.

Instrumental Capability Profile

This activity was sponsored originally under Statement of Work Items 1, 4, and 13 which have been terminated in favor of a more specific redefinition of the effort under continuing Item 17. The objective of this effort is to apprise NASA-ERC of optimum instrumentation and test sequences from which maximum insight into failure mechanisms may be gained. Original tabulations were presented in the second Monthly Report and Quarterly Report Number One, giving instrumental capability ranges, applications to failure mode and failure mechanism investigation, and references to pertinent process steps. Supplementary instrumental data have been presented in succeeding reports. Continuing efforts in this area are intended to ensure the awareness of NASA-ERC of current instrumental innovations for extracting maximum failure information. This is being accomplished through periodic updating of previous compilations, the most recent of which was compiled during the current year (Appendix K).

A further objective of this effort is to supply NASA-ERC with critical reviews and analyses of current test techniques. A prominent problem area presently exists in the leak testing of hermetically sealed packages which is summarized under the Continuing Activities section.

CONTINUING ACTIVITIES

Failure Mechanisms Related to Oxide Passivation
(Statement of Work Item 15)

The occurrence of dielectric defects, or "pinholes", constitutes a significant failure mode in modern oxide-passivated devices and is probably the largest remaining barrier to large scale integration. Although numerous remedial innovations in materials and process techniques have been attempted, no reliable solution to this problem has yet been found. Because of the general convenience and superiority of thermally grown oxide for most masking and passivating purposes, and because this application of silicon dioxide has been successfully optimized in most other respects, it seems important to take full advantage of these characteristics by determining the process requirements needed to remove this remaining major problem in its use. The objectives of this effort, therefore, are to discover why structural defects are produced in thermally grown oxides and to learn how they may be prevented.

Previous activity on this program has sought to relate the origin of dielectric defects to various process factors and structural considerations. These results may be summarized as follows:

1. Factors tending to increase dielectric defects

    a. Extended processing (generally)
    b. Higher compressive stress in the oxide
    c. Embedded lapping grains in the substrate
    d. Superficial HF etching
    e. Abrupt oxide steps
    f. Thermal cycling
    g. Mechanical wiping
    h. Removal of back oxide layers

2. Factors tending to decrease dielectric defects

    a. Growth of oxide to higher thicknesses
    b. Chemical etch of initial wafer
    c. Pyrolytic oxide, uniformly applied and properly densified
    d. Additives tending to reduce bond strain in silica glass
    e. Addition of steam to oxidation process gas, or termination of any dry oxidation step with a wet oxidation

3. Factors having little or no effect on defect incidence:

    a. Wafer cooling rates after oxidation
    b. Mineral content of water used as steam source
    c. Oxide growth rate

d. Substrate doping (generally)
e. Crystal defects (dislocations and stacking faults)
f. Certain non-reactive particulate contaminants (such as alumina) which do not stick to the oxide during growth

Electron photomicrographs (Figure 1) show pile-ups of oxide layers at defect sites, thereby indicating compressive stress in the oxide as the major cause of defects. This idea was confirmed by comparing oxide defect densities existing at the oxidation temperature with those existing after cooling. Briefly, the technique consists of terminating an oxidation with a short HCl etch which attacks any exposed silicon (Figure 2), producing an etch pit at each defect site. After cooling the additional defects are located by electrophoretic decoration (Figure 3). In an oxide layer grown to 8000Å the ratio of defect densities before and after cooling was found to be 1:195 (Appendix H). Most of the above findings have been reported previously (Appendixes E and F) and all are consistent with the compressive stress model advanced as the originating agency of oxide defects.

The approaches to continued investigation on this program consist of examining in detail the inhomogeneities in oxide distribution evidently present at the initial stages of oxidation using the techniques described above. Experiments have shown that a significant number of defects may exist at the processing temperature after only a brief oxidation period, thus predisposing oxides to a distribution of thin spots at later stages of oxidation. It is postulated that a portion of these thin spots yield to the compressive stress produced on cooling and that the remainder constitute the latent defect sites opened up by light etching in hydrofluoric acid. It is further postulated that if initial oxidation irregularities could be removed through appropriate process control the finished oxide layers would be free of thin spots and capable of withstanding the existing stresses without rupture.

More quantitative investigations were conducted to compare defect densities at no stress (i.e., before cooling), at full stress (i.e., after cooling) and at partial stress relief (i.e., after removal of the back oxide layer). These data were obtained for a series of oxidation times to yield growth dependent plots as typified in Figures 4 and 5. Conventional oxide growth technique was used (N_2: 245 cc/min; O_2: 245 cc/min passed through water at slightly less than 100 C; temperature: 1180 C) followed by HCl-He etching before removal from the growth zone. Defect densities were evaluated by standard etch pit and decoration counts. The observed dependence on $t^{1/2}$ is characteristic of a diffusion controlled process and has been confirmed by other investigators (Refs 3-9) for the oxidative growth of silica. The exponential decrease in the number of defects with oxide growth also is apparent from Figures 4 and 5. Decay of this number, N, may be expressed either in terms of growth time, t, or layer thickness, z, according to

$$N = N_t e^{-\lambda t^{1/2}} = N_z e^{-\phi z} \qquad (1)$$

where N_t and N_z are the corresponding preexponential factors (ordinate intercepts) and λ and ϕ are the respective decay factors. Decay factors appropriate to Figures 4 and 5 are listed in Table I.

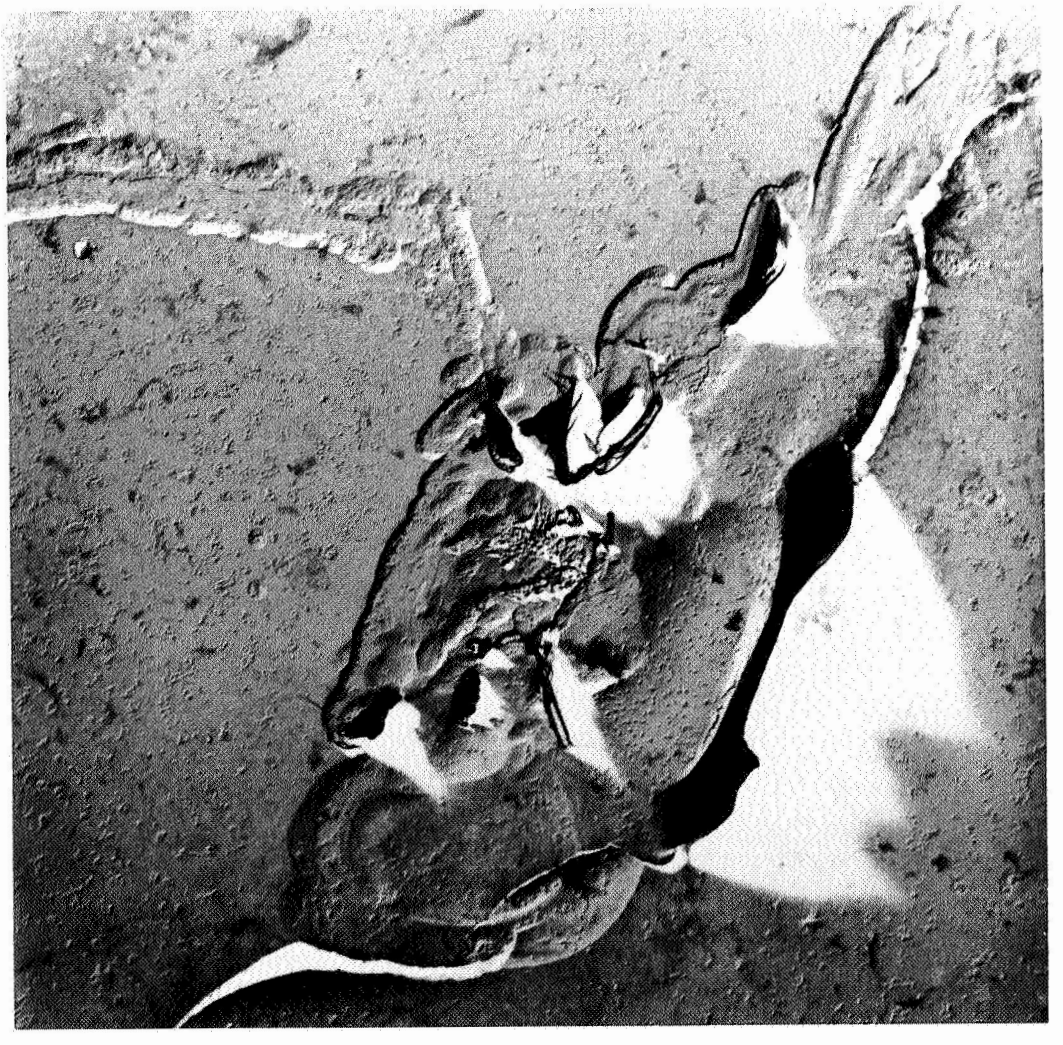
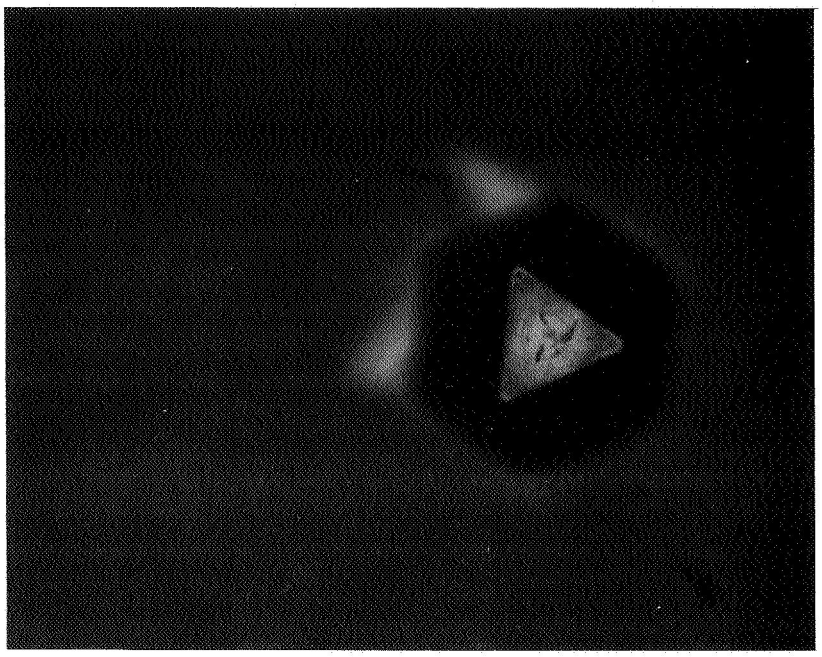
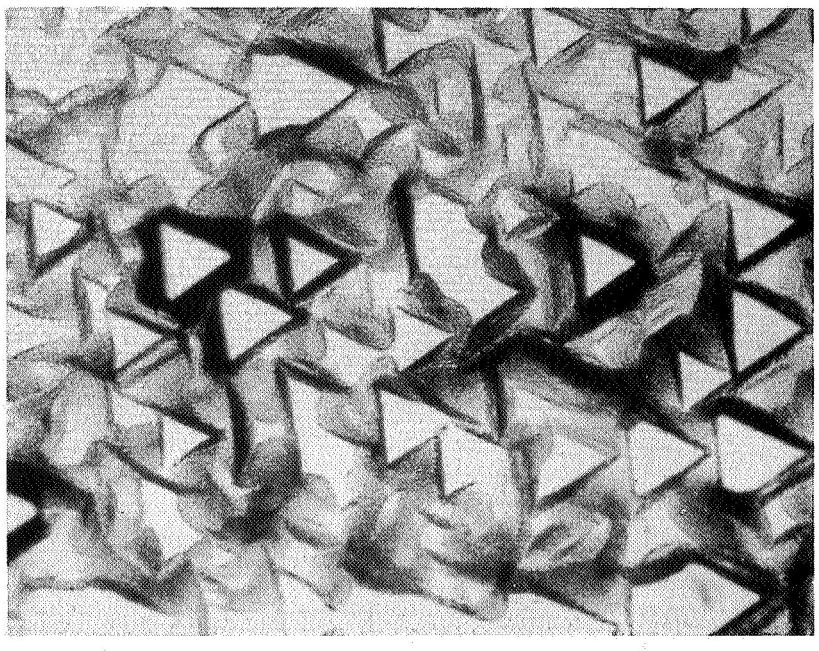


Figure 1.- Electron Photomicrograph of Replica of an Oxide Defect (Black Region). Approximate Length: Twelve Microns.



a. Silicon Etching of Oxide Defect Site



b. Etch Pattern of Unoxidized "Control" Wafer

Figure 2.- High Temperature HCl Etching Test

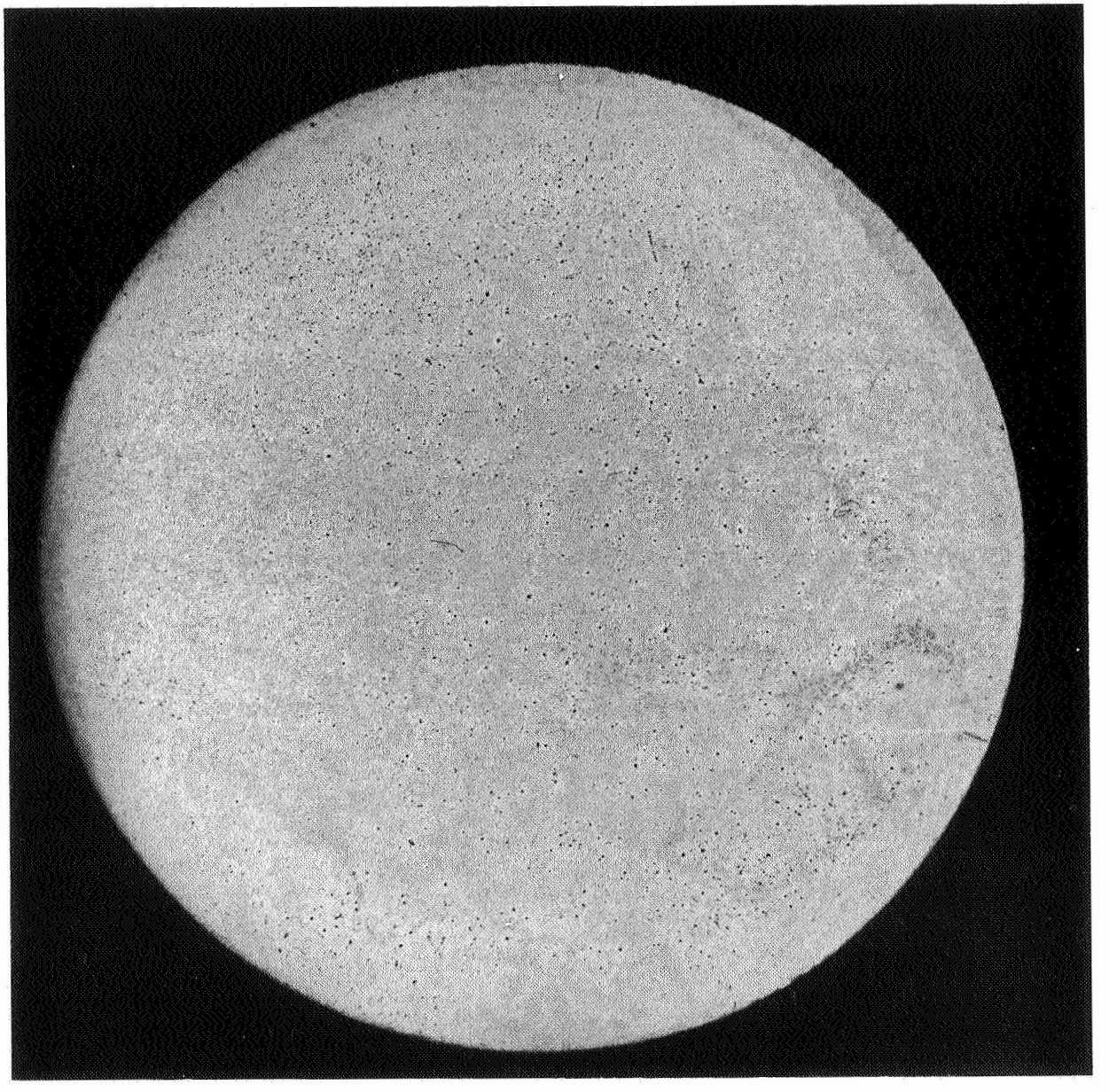


Figure 3.- Electrophoretically Decorated Wafer of Very High Oxide Defect Density (see Appendix F).

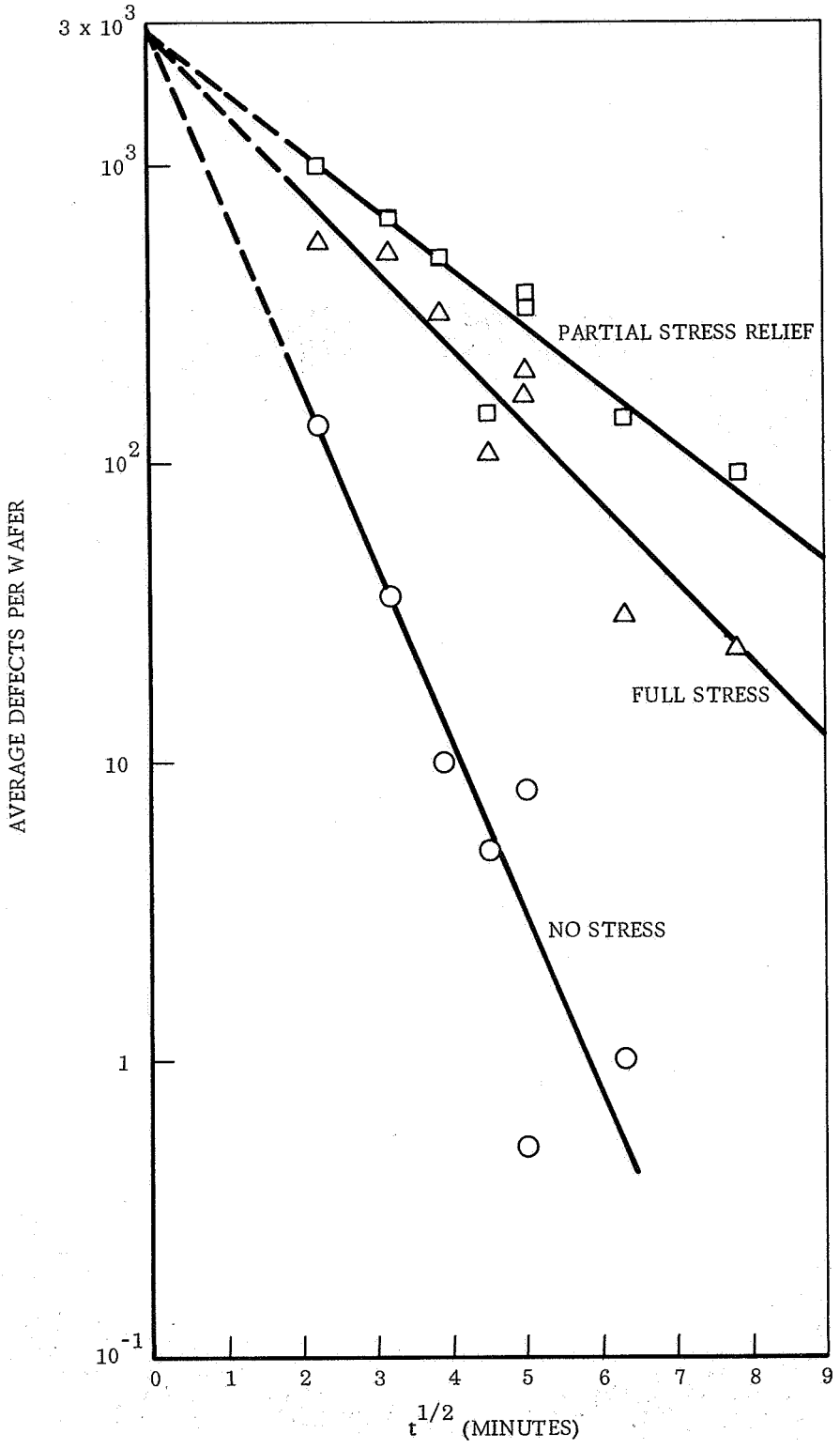


Figure 4.- Defects as a Function of Oxidation Time for Various Stress Conditions

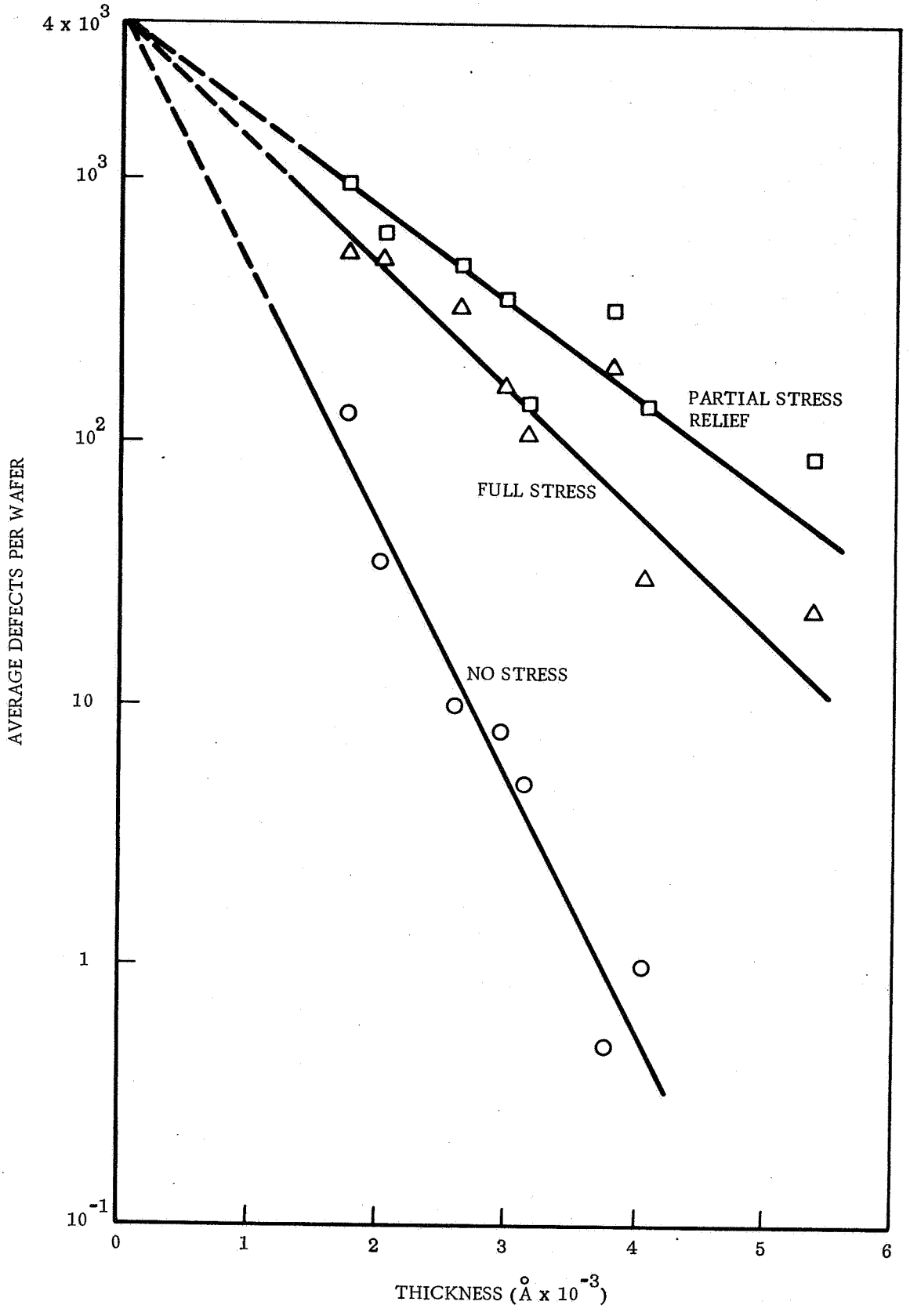


Figure 5. –Defects as a Function of Oxide Thickness for Various Stress Conditions

TABLE I
OXIDE DEFECT DECAY FACTORS

Condition	λ(minutes$^{-1/2}$)	ϕ(per 1000 Å)	λ/ϕ
No stress	1.37	2.22	0.62
Full stress	0.60	1.08	0.55
Partial stress	0.45	0.83	0.54

Internal consistency between the time and thickness data is given by the ratios, λ/ϕ, and is better than 94 percent.

Obviously the smaller the decay factor the greater the defect density and the more serious the pinhole problem. Merely by cooling from the oxidation temperature to room temperature the decay factor is reduced by more than 50 percent and the defect density increased by roughly an order of magnitude. Simultaneously with cooling the compressive stress is developed in the oxide layers which, for the set of wafers under discussion, was found by Proficorder analysis to be uniformly 4.1×10^4 psi over the range of thicknesses grown (Appendix L). It is this magnitude of stress that differentiates the "full stress" condition (middle curve) from the "no stress" condition (lower curve) existing at the oxidation temperature (Figures 4 and 5). And it is the difference in slopes of these two curves that links the occurrence of dielectric defects with compressive stress.

In the upper curve, stress in the oxide layer has been partially relieved by etching off the opposite oxide layer. The relief mechanism is through strain of the silicon substrate, yielding an observable warp curvature in the wafer. As a result the remaining oxide layer assumes a conformal convex curvature which, it is postulated, opens up oxide fracture sites previously held together in the more planar "full stress" state. Thus, the "partial stress relief" condition is believed to introduce still more defects, as evidenced by the slope of the upper curve in Figures 4 and 5, because of the unbalanced nature of the relief. It would appear from these results that an integrated circuit technology that allowed the back oxide to remain on the chip would be somewhat less prone to pinhole problems.

A more serious problem, however, remains. This is the existence of a virtual defect density (N_t, of Equation 1) of the order of $10^3/cm^2$. Admitting that this extrapolated value is fictitious, one still must assume a very large defect density at some small $t > 0$ which increases exponentially with thinner oxides. This problem is especially critical to MOS-FET technology where gate oxides of 1000 Å, or less, are generally required. It seems more important, therefore, to understand the physical basis for the virtual defect density, so that it can be manipulated downwards, rather than attempting to increase defect decay factors.

From a comparison of Figures 4 and 5 it is seen that the preexponential defect density is approximately 50 percent higher for the thickness dependent curves than for the $t^{1/2}$ dependent curves. This difference is significant within the experimental limits of error and indicates the presence of a kinetic anomaly during the initial phases of oxidation. Such an anomaly might be associated with the initial nonhomogeneous oxide distribution indicated by these plots. If so, process steps or modifications tending to moderate, or reverse, this condition might also reduce the virtual defect density with a consequent improvement in oxide quality.

Accordingly, wafers were pretreated in a manner designed to produce diffusion attenuation layers on the surfaces. These layers consist primarily of silicon dioxide in the 200 Å or less thickness range produced by a wet chemical method consisting of treating the wafers with HF (to remove old oxide), KOH solution (to remove residual flouride), and hot concentrated nitric acid (to remove residual KOH and initiate uniform oxidation). Each step is followed by thorough rinsing with distilled water. The exact nature of the layers so produced still is unknown. Boundaries in such layers produced by controlled (masked) HF etching are readily revealed by moisture condensation from a humid environment. Attempts to measure the thickness of the layers by Proficorder and Tally-Surf tracing, and by interferometry, however, failed. Although the layers are suspected of being a porous and partly hydrated silicon dioxide, the possibility of a small component of nitride cannot be ruled out.

High temperature oxide defect densities on wafers so treated (termed hereinafter "oxidative precleaning") were found to be practically nonexistent, even for oxidation time as short as 2.5 minutes. Room temperature decorated defects, however, were significant and are listed in Table II.

TABLE II
FULL STRESS DEFECT DENSITIES IN OXIDATIVELY PRECLEANED WAFERS

Run	Oxidation Time (Minutes)	Oxide Thickness (Angstroms)	Defects per Wafer (Average)
K	2.5	1300	213 ± 18
L	5	2000	172 ± 29
M	10	2700	88 ± 11
N	15	3000	75 ± 6
O	20	4100	50 ± 3
P	30	5000	40 ± 3

A plot of the defect densities against both thickness and $(\text{time})^{1/2}$ (Figure 6) shows that the time dependent plot now has a higher virtual defect density than the thickness dependent plot - a reversal from the corresponding relation shown in Figures 4 and 5. The fact that the oxidative precleaning indeed moderates the initial high temperature attack is more clearly shown by plotting thickness vs $(\text{time})^{1/2}$ for both the oxidatively precleaned and normally cleaned ("untreated") wafers (Figure 7). The concavity of the "treated" curve at the origin is in the expected sense for an initial attenuation of oxidation.

A comparison of Figure 6 with Figures 4 and 5 also indicates that the oxidative precleaning produced a significant reduction in virtual defect densities. Whether this reduction was due to the initial oxide layer or to the additional cleansing action was, of course, not determined by this set of experiments. Therefore, an extended non-oxidative precleaning technique was worked out in the hope of separating the two effects. Additionally, other process variables are available for manipulation in securing initial slow growth without recourse to oxidative precleaning, such as initial reduction in temperature, or in the oxygen content of the process gas. Initial pilot tests showed the latter method to yield more reproducible results in the present equipment.

A systematic investigation of the above process parameters therefore was undertaken with special emphasis on defect incidence in the region of thin oxide layers. In this series only the oxidative and the extended non-oxidative pretreatments were used. Slow growth was achieved by limiting the oxygen to 4 percent of the process gas composition and by reducing the temperature of the water reservoir. The oxidation temperature, however, remained at 1180 C. All data was taken as a function of oxide thickness grown, as measured (in most cases) by Proficorder tracing. All defect readings are recorded on a cm^{-2} basis as a result of changes in counting technique explained below. In addition the ratio of etch pits (high temperature defects) to decorations (room temperature defects) were computed for each series, where applicable, as a further test of internal consistency. Current data thus obtained are compiled in Table III.

Comparison of Sets A and B in Table III plotted against oxide thickness (Figure 8) indicates that there may be little or no difference in how the initial oxidation rate is moderated. The effect of both on the virtual defect density appears to be significant. Compared with earlier results, which yield a virtual defect density of $\sim 4 \times 10^3$ per wafer ("Full Stress" curve, Figure 5), or $> 10^3$ cm^{-2}, the present treatments yield an order of magnitude improvement ($\sim 1.1 \times 10^2$ cm^{-2}). Although the defect decay rate is somewhat smaller than that applicable to Figure 5, this potential modification in process technique may have important implications for thin oxide applications, such as MOS gates. At 1000 Å oxide thickness, for example, Figure 5 yields a density of 410 defects cm^{-2} (taking the wafer area as 3.2 cm^2) while Figure 8 yields a density of 70 cm^{-2}.

Sets C, D and E of Table III were undertaken primarily to explore defect decay behavior in the first 1000 Å of oxide growth and are plotted in Figure 9. It is evident, first of all, that a substantial spread in data exists in this region. This spread is due in part to a less homogeneous defect distribution in thin oxides and in part to counting error resulting from the substantially higher defect densities encountered. In spite of these difficulties it is seen that measures taken to moderate the initial

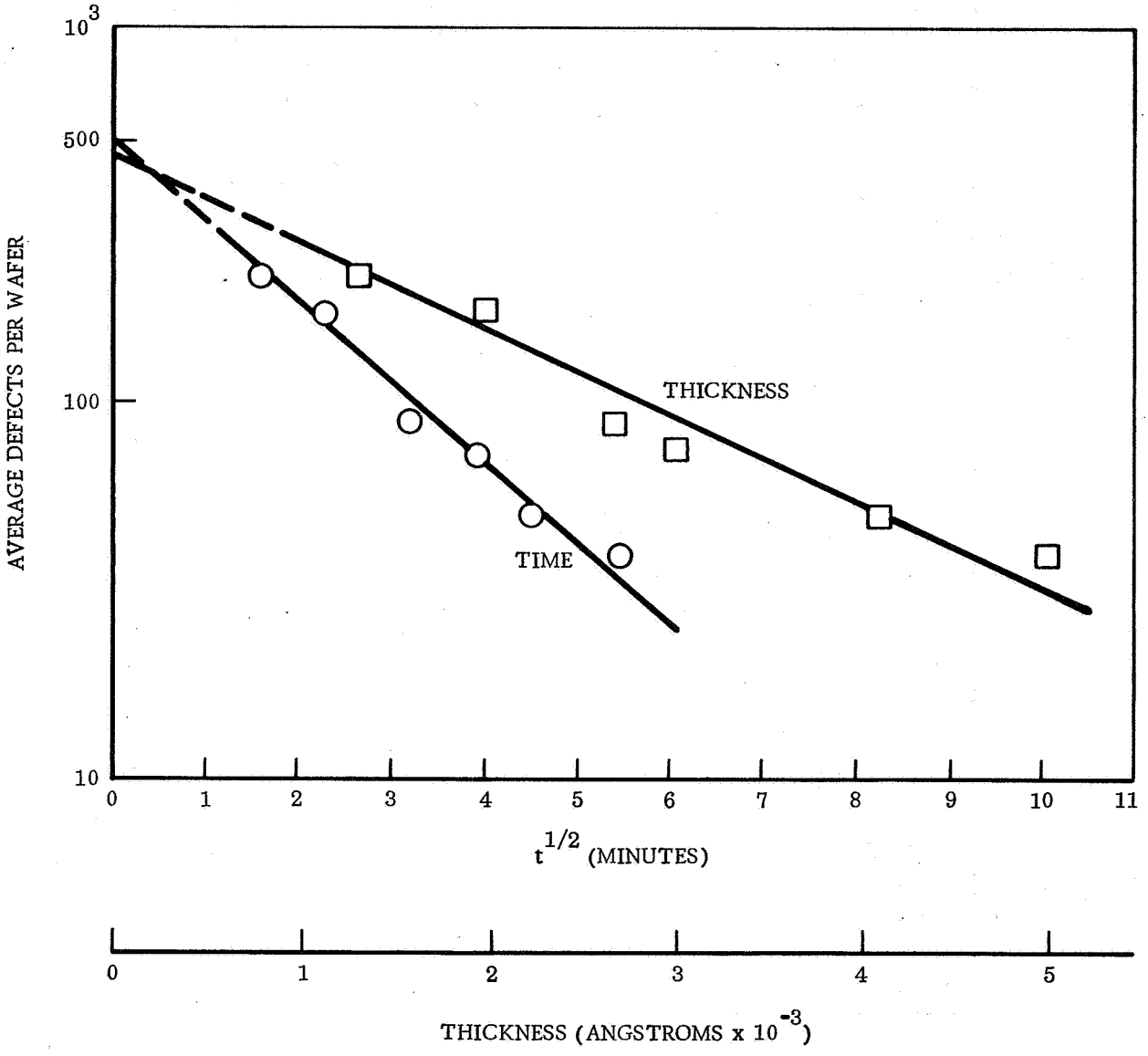


Figure 6.- Oxide Defects as a Function of Growth for Oxidatively Precleaned Wafers

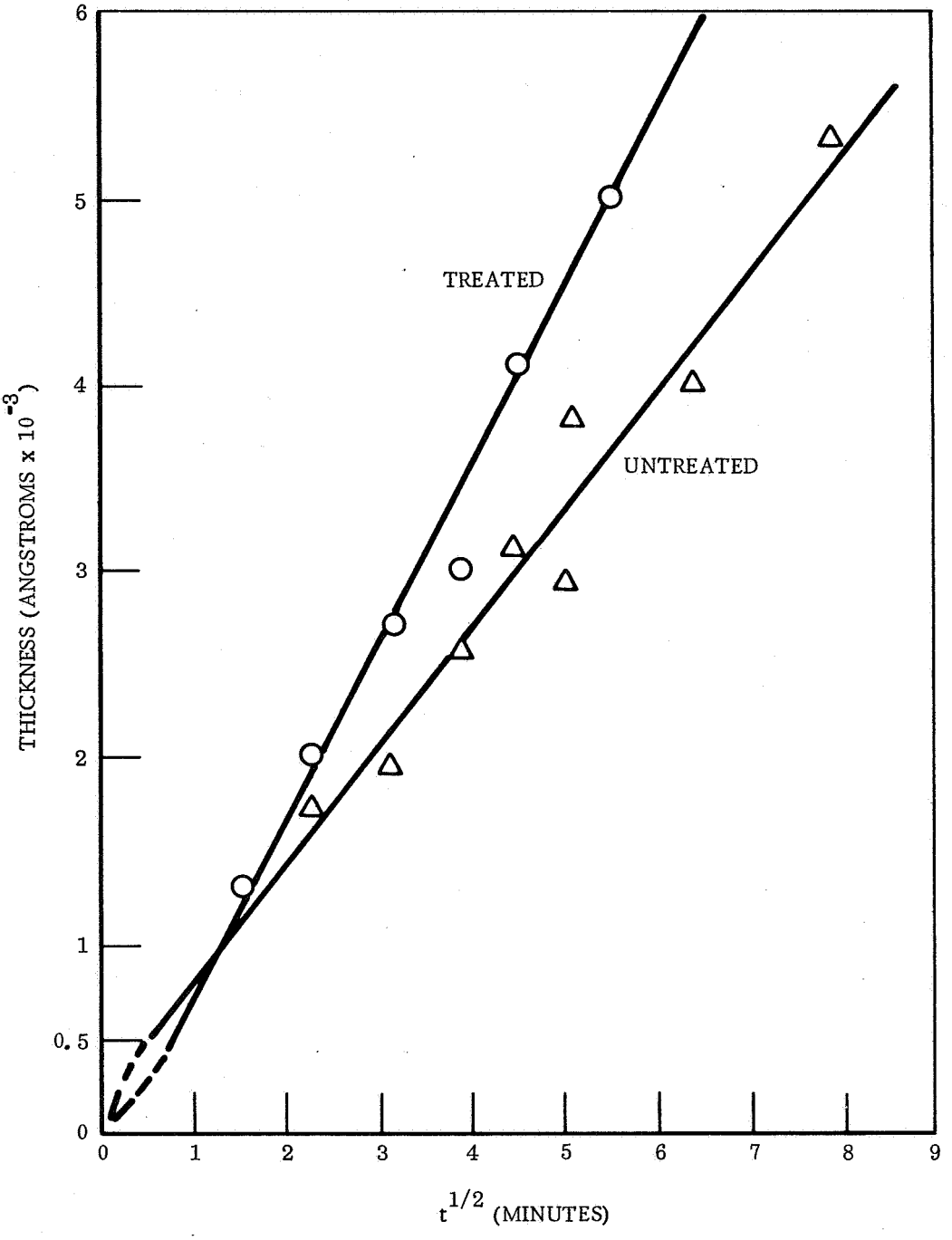


Figure 7. - Oxide Thickness Dependence on Time for Treated and Untreated Wafers

TABLE III
DEFECT DENSITIES AS A FUNCTION OF PRETREATMENTS AND GROWTH RATE

Set	Wafer Precleaning	Water Temperature (Deg C)	Oxide Growth Rate	Oxide Thickness (Angstroms)	Etch-Pit Density (cm^{-2})	Decoration Density (cm^{-2})	Etch-Pits/ Decorations
A	Ox.	95	Normal	1300		67.0	
	Ox.			2000		54.0	
	Ox.			2700		27.6	
	Ox.			3000		23.5	
	Ox			4100		15.7	
	Ox			5000		12.6	
B	Non-Ox.	34-35	Slow to	1600	0	47.4	
	Non-Ox.		400 Å	1800	0.079	43.6	0.0018
	Non-Ox.		then	2800	0	37.7	
	Non-Ox		Normal	3600	0.079	20.0	0.004
	Non-Ox.			4600	0	11.3	
C	Non-Ox.	34-35	Slow	300	110	356	0.31
	Non-Ox.			500	48.3	129	0.37
	Non-Ox.			600	4.1	91.0	0.45
D	Non-Ox.	34-35	Slow	470	7.9	122	0.089
	Non-Ox.			570	13.2	142	0.091
	Non-Ox.			610	29.5	194	0.150
E	Non-Ox.	50	Slow	470	29.8	860	0.0346
	Ox.			280	69.6	776	0.0898
	Non-Ox.			650	0	121	
	Non-Ox.			480	3.5	390	0.0090
	Ox.			390	6.3	610	0.010
	Non-Ox.			600	4.1	314	0.013
	Ox.			650	4.4	222	0.020

TABLE III (Cont)

Set	Wafer Precleaning	Water Temperature (Deg C)	Oxide Growth Rate	Oxide Thickness (Angstroms)	Etch-Pit Density (cm^{-2})	Decoration Density (cm^{-2})	Etch-Pits/ Decorations
E	Non-Ox.			710	3.1	164	0.019
	Ox.			830	6.3	266	0.024
	Non-Ox.			1030	1.6	84	0.019
	Ox.			1050	2.5	115	0.022

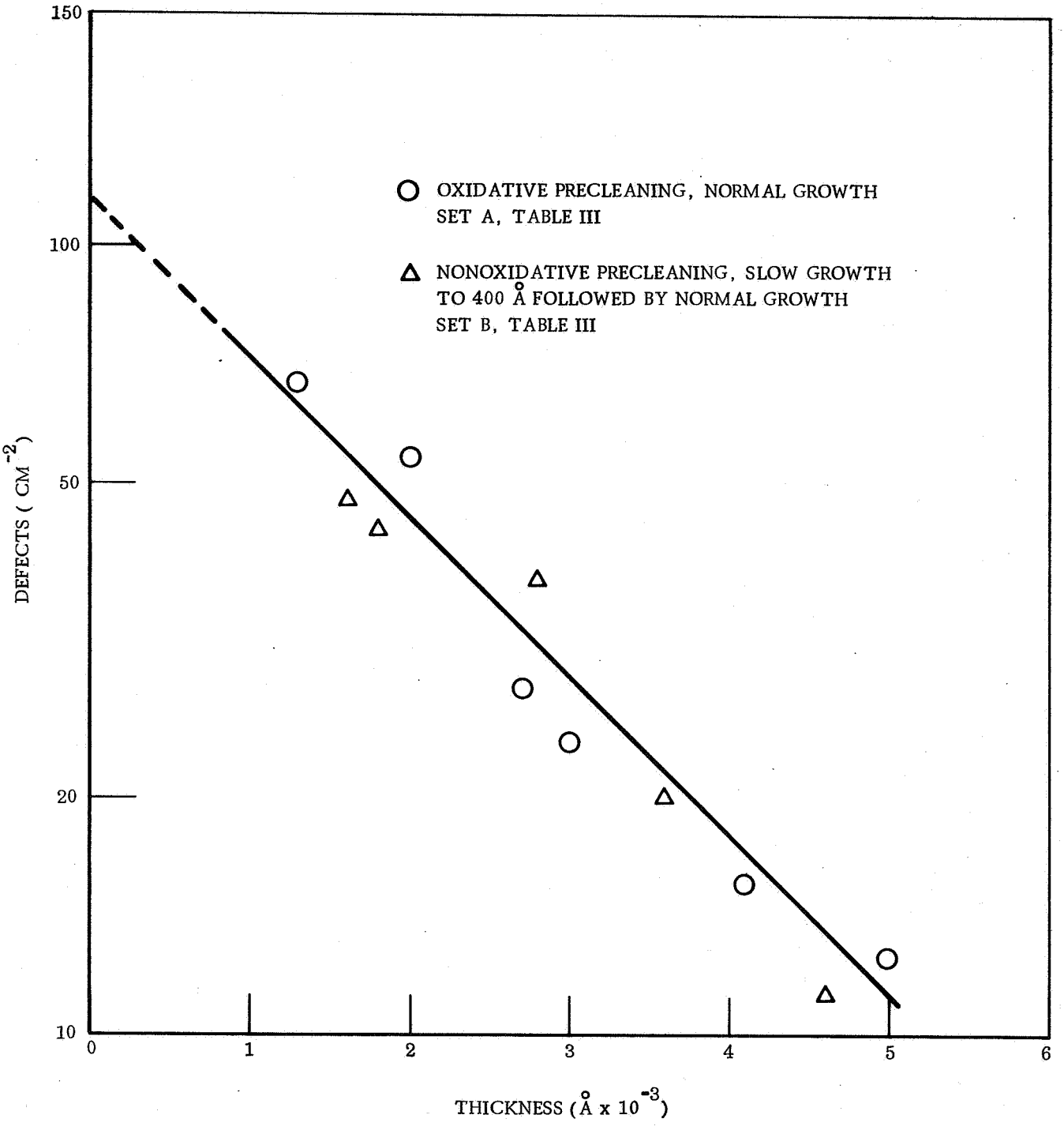


Figure 8. - Comparison of Oxidative Precleaning With Nonoxidative Precleaning Plus Initial Slow Growth

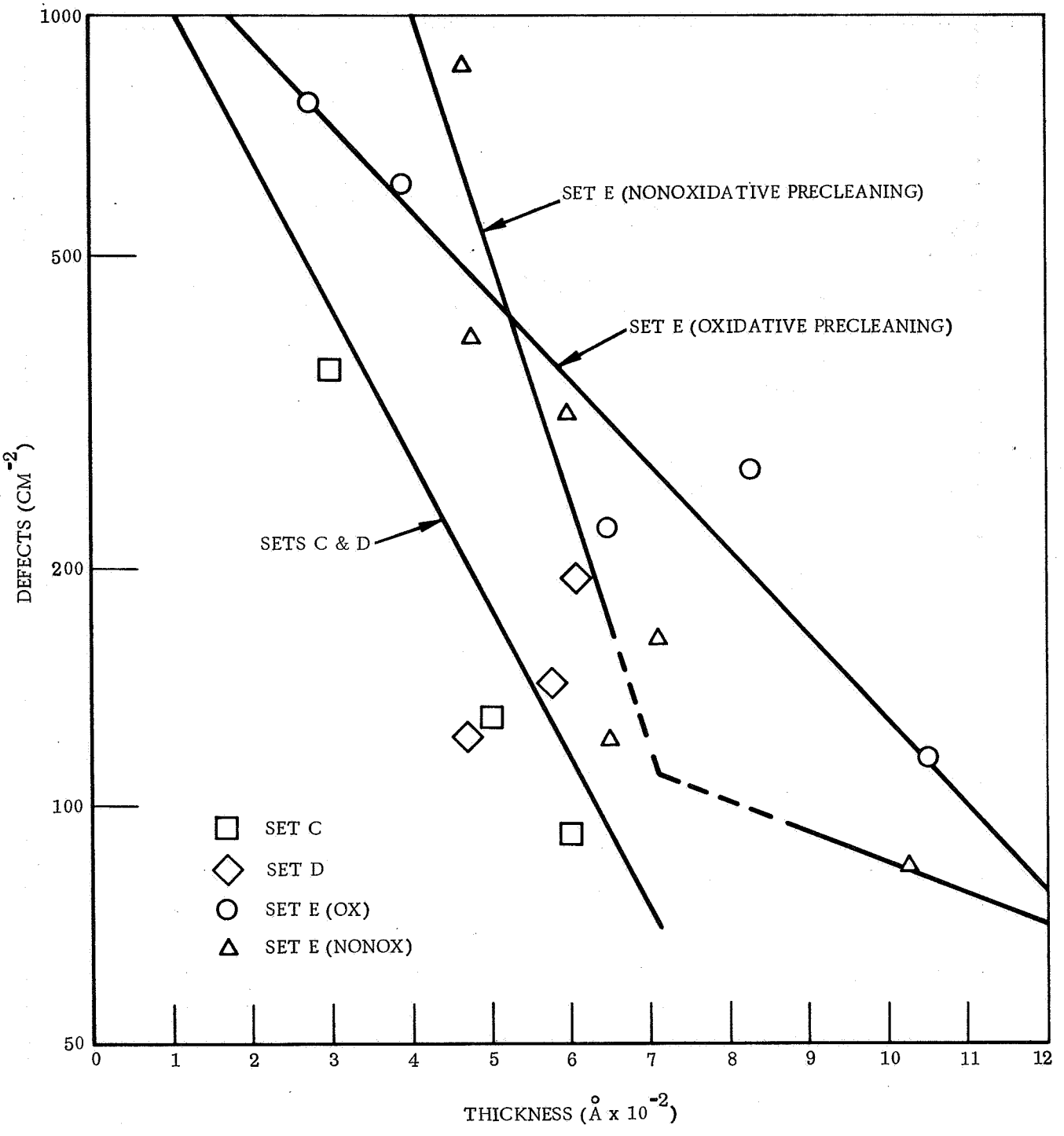


Figure 9. - Decay of Oxide Defects in the First 1000 Å Under Various Treatments

oxidation rate result in extremely steep (25 to 50 percent per 100 Å) defect decay curves in the first 700 Å of growth. Beyond 1000 Å the curves appear to level out in a manner consistent with that of Figure 8. It also would appear that initial slow growth is only about half as effective following oxidative precleaning (Sets E) than it is in its absence. Finally, lowering the water content of the process gas (Sets C and D vs non-oxidative Set E) further increases the abruptness of defect disappearance.

Although a mechanistic explanation of these effects is somewhat doubtful at the present time, an empirical prediction of optimum process conditions may be possible. All indications appear to point to the desirability of a very slow initial oxidation stage. This might be achieved by introducing a small increment of oxygen, preferably dry, at the beginning, followed by a prolonged baking in pure nitrogen before proceeding with normal (moist) oxidation. Alternatively, provision could be made for very slow introduction of the wafers into the hot zone of the furnace using a standard gas composition throughout. The general concept here would be to allow sufficient time for the development of an equilibrium distribution of the first few hundred Angstroms of oxide. Continuing investigations will be aimed at testing this hypothesis.

The etch-pit to decoration ratios given in Table III show considerable consistency within sets but not between sets. This is most clearly indicated by Set D which was intended to duplicate Set C. The E/D ratio of Set C is 0.38 ± 0.05, and of Set D, 0.11 ± 0.04. It might be concluded that the higher the E/D ratio the lower the vulnerability of existing thin spots to the compressive stress developed in the oxide on cooling to room temperature. This would imply an earlier filling in of defects, and thus a steeper drop in defect densities, at the beginning stages of oxidation. This appears to be borne out in a comparison of combined curves C and D (Figure 9) and curves E, with their respective E/D ratios (Table III). However further investigation is required to establish unequivocally the physical significance of these ratios.

The spread in room temperature defect decoration counts (Table III) attests to the counting error caused by copious electrolytic hydrogen evolution in the presence of the high defect densities characteristic of the thin oxides grown in the present series. It was decided, therefore, to abandon bubble source counting in favor of counting the metal salt deposits which collect around each defect site as a result of anode dissolution. These salts were rendered more visible by addition of a colorimetric agent, such as dimethylglyoxime or rubeanic acid, to the alcoholic phase. Counting then could be done in the absence of electrolytic effects after only a short period of applied voltage. A 1:1 correspondence between decorated sites and bubble sites has not been achieved yet, but rubeanic acid was found to be superior to dimethylglyoxime for use with a nickel anode. Further tests are underway to establish the correct conditions and appropriate reagents for this improved defect counting technique.

Continued activities in this area will proceed along the lines established above with special emphasis on thin oxide layers and initial oxidation kinetics manipulated in a manner to achieve equilibrium distribution of initial oxide layers.

Failure Mechanisms Associated With Packaging
(Statement of Work Item 16)

Gas ambient effects on integrated circuits. - The objectives of continuing investigations in this area are directed toward potentially corrosive contaminants, such as chlorinated solvents, and potentially conductive condensates, such as those from aromatic solvents, which may interact catalytically on the oxide surfaces to produce current leakage paths. The effort is based on results from ambient analyses by gas chromatography and mass spectrometry which have revealed a variety of organic contaminants, such as those given in Appendix I. Investigation of the effects of hydrogen or integrated circuits has been discontinued, as indicated previously, a detailed summary of which is given in Appendix M.

Materials compatibility. - The objective of investigations in this area are directed toward an analysis and correction of failure modes associated with the physical contact of incompatible materials, such as inferior heat sinks, cracked dice, and nonhermeticity.

The problem of inferior heat sinks will require the development of improved materials or process techniques for die-to-header bonding that will assure uniformly rapid heat dissipation from devices under operating load. Factors contributing to this problem are poor thermal conductivity, thickness variations, and voids due to maldistribution of ceramic adhesive layers. Thermal excursions resulting from poor heat dissipation may, in turn, contribute to other significant problems such as cracked die, degradation of h_{FE} under bias, and mass transport of metallization. A useful approach is to locate voids in adhesive bonding by X-ray, analyze the chemical and thermal properties of the adhesive employed and map thermal emission from devices under various electrical loads by means of infrared microscopy. Parallel investigation of alternate adhesive compositions and process techniques of applying adhesives and mounting dice also should be made.

The problem of cracked dice is complicated by artifacts which may not be caused basically by the potential incompatibility of the associated materials. In the past, occasional "examples" of the cracked die problem are suspected to have resulted from inept delidding procedures. Other such examples may have occurred through package deformation on mechanical removal of the device from its bonding to a printed circuit board or through other maltreatments. Both of these problems are aggravated by the unusually thin-gauge metal used in the packages of certain manufacturers. In light of these uncertainties it is necessary to reassess the cracked die problem using methods that do not introduce mechanical stress in the die. Beyond this problem lie the very real possibilities that stresses sufficient to cause cracking may be introduced by lead bonding and lidding operations and by the mechanical, thermal, distributional, and curing properties of the ceramic adhesive used in bonding die to header. Aside from dimensional changes during curing, improper distribution of adhesive is often found which causes an inferior heat sink and allows excessive thermal excursions to occur in the die during operation. Thermal expansion of the die is not matched by the adhesive which, if rigid, introduces severe mechanical stresses in the die. This type of problem is less likely where dice are scrubbed to the package, but thermal expansion mismatch between the die and the casing still is a potential source of fracture. In addition to assessing the over-all cracked die problem it is proposed that program effort in this area be focused on the mechanical stresses inherent in the various methods of die-to-header bonding.

Lack of hermeticity also may arise from the incompatibility of rigidly bonded materials and requires examination of available evidence of dimensional, lid component assembly and thermal variations characteristic of current practice. It also is important to seek evidence of oxides, or other contaminants, which may cause incomplete wetting of interfaces during sealing. Breaches in hermeticity may arise from accidental package damage or misalignment of components prior to sealing, or from inadequate temperature and environmental control during sealing. In ceramic packages, improper distribution or inherent porosity of adhesives also may lead to hermetic flaws. Accidental flexure of leads or other mechanical stresses often aggravate inherent incompatibilities and produce cracks in-glass-to-metal seals causing a further source of leaks. Alternatively, hermeticity may be lost at glass-to-metal interfaces through the accidental presence of contaminants, such as oxides, or through accidental exposure to etchants.

In view of the large variety of leak sources it is necessary to limit the objectives to those of dominant frequency. Although it is possible to infer the cause of many leaks by metallurgical sectioning, electron microprobe analysis and other instrumental investigations of nonhermetic packages, a more direct approach is to examine critically the packaging techniques of specific manufacturers which generally provides prompt clues to hermeticity problems. Having thus narrowed the possibilities, it is then possible to confirm the source (or sources) of nonhermeticity by instrumental analysis. As in the case of gas ambients, however, general conclusions in this area will not be applicable without qualifications concerning specific manufacturers.

Investigations in the area of materials compatibility will be governed by the selection of problems of crucial importance as revealed by Autonetics' continuing analysis of integrated circuit packages from various manufacturing sources.

Instrumental Capability Profile
(Statement of Work Item 17)

The major objective of this effort has been defined in a previous section of this report and a current compilation of instrumental capabilities is given in Appendix K. A further objective of this program is to provide NASA-ERC with critical reviews of current test techniques. In the present section leak test techniques applicable to hermetically-sealed integrated circuit packages are brought under scrutiny. Methods presently in use, including their advantages and shortcomings, are considered as well as new approaches under development designed to improve on those now employed. Because of the previous absence of a single test applicable to the entire leak-rate range, applicable techniques conventionally are categorized as "fine leak" and "gross leak" tests. For convenience these categories are followed below although they may become obsolete in view of a new technology now being evolved.

Fine leak testing. - All of the test methods reviewed and outlined herein, with two notable exceptions, employ the technique of inoculating the package with a tracer gas, usually helium, after it has been sealed, then conducting a leak test of the device with a helium leak detector. The pressure and duration of the tracer gas inoculation varies among users but is of problematical effect on the leak test accuracy. The average pressurization period is four hours at 60 psig. The practical upper limit for helium leak testing appears to be 1×10^{-8} to 1×10^{-9} Std cc/sec He. The practical lower limit appears to be 1×10^{-5} to 1×10^{-6} Std cc/sec He.

The technique of inoculating a package after sealing with a tracer gas in actuality produces a questionable leak rate number which is the product of the leak rate of an unknown gas fraction pressured into the package, and of that fraction of gas in turn being evacuated from the package and tested during the leak test-cycle. Furthermore the helium leak test machine is calibrated for 100 percent helium. The fraction of helium (tracer gas) within the package is obviously unknown. The only way to assure the validity of a tracer gas leak test is to seal the devices to be tested in a gas ambient with a known fraction of the tracer gas to be used.

A new leak test method developed at the North American Rockwell Corporation Science Center requires no special pre-pressurization to inoculate a package with a tracer gas. The packages may be sealed with dry nitrogen or dry air. This leak test method is based on the principle that helium atoms excited to the metastable state will transfer energy to the nitrogen or oxygen atoms presumably leaking from the package under test. The excitations of these N_2 or O_2 molecules can thus be detected either by a change in conductivity or by detection of photoemission. Leak tests conducted utilizing this principle have demonstrated that leaks as fine as 1×10^{-8} Std cc/sec He and as gross as holes 0.090 in. diameter can be detected. Thus utilizing this new principle, "fine" leaks and "gross" leaks are detected with one test.

The leak test method reputedly used by Raytheon is one which inoculates a package under pressure with Freon or similar liquid. It is reported that a weight gain of 50 μgram will fail a device. Based on DuPont Corporation, corrosion rate studies of Freon type compounds on aluminum, it has been determined that at room temperature Freon will corrode through the average integrated circuit interconnection in 10 months. This method appears to be a reliability hazard.

It is theorized that all leakage at rates less than 10^{-6} Std cc/sec He is by diffusion and that leakage due to viscous flow is negligible. The fraction of ambient exchange is therefore independent of total and partial pressures, although the absolute amount of exchange of a particular gas is directly proportional to the difference between the partial pressure within and without the package. A 14-lead integrated circuit flat pack with an internal volume of 0.005 cc and a leak rate of 5×10^{-7} atm cc He/sec thus exchanges 10 percent in 0.77 hours, 50 percent in 5.2 hours, and 90 percent in 17.2 hours. The time for exchange is inversely proportional to the leak rate and, for example, is 50 times as great for a leak rate of 10^{-8} atm cc He/sec. The time for an equivalent proportion of exchange in a larger package is greater and is directly proportional to the volume of the package.

Gross leak testing. - Most gross leak detection methods reviewed and outlined herein, and used on opaque packages, employ the simple technique of detecting gas bubbles escaping from a leaking package while immersed in a hot liquid. One method stipulates that the device to be tested be placed in liquid and then a vacuum should be applied while the observer watches for bubbles indicating a leak. This is merely a slight ramification of the basic principle employed.

There is little agreement on how sensitive the bubble test is. It has been variously rated from $>10^{-3}$ to $> 10^{-5}$ Std cc/sec He.

There is agreement however on the fact that this test is very much affected by operator efficiency and operator fatigue. It is recommended that an operator should not work at this test for more than two hours continuously.

More specifically, the formation of bubbles depends on the thermal expansion of the contained gas. Their appearance, however, is easily overlooked by operators in the early stages of familiarization; even among experienced personnel results are likely to vary between individuals and with the same individual at various stages of fatigue. In part this is due to the transient nature of the phenomenon, the fact that not all surfaces of the device can be observed at the same time, the fact that light reflections from the package sometimes may be confused with bubbles and the fact that rechecks of test results are not reliable. A more basic problem is the fact that the internal gas pressure must compete with and exceed the liquid capillary filling pressure due to surface tension. Thus, below a certain pore size no gas exit is possible and the pore fills with the glycol. Multiple pores below the minimum detectable size could result in an extremely leaky package which would pass undetected. Furthermore, operator A using a bath at 150 C would pass a particular device that operator B using a bath at 160 C would reject because at the higher temperature the internal gas pressure is higher and the liquid surface tension lower, thus favoring gas exit in the minimum pore size region. It should be remembered, further, that this minimum pore size region is considerably above the upper limit of the conventional helium leak test.

Tests conducted by NAR have proved that the bubble test is not reliable and not repeatable if ethylene glycol is used as the test liquid. Even at relatively high temperatures (125 C) glycol has a high viscosity and high surface tension which causes erroneous leak indications. It is conjectured that mineral oil produces similar problems.

FC-43 has been shown to be an ideal substitute for glycol and mineral oil as a bubble test medium.

Summary. - Presently used leak test techniques are summarized below and are compared in Table IV.

MIL-STD-833 (Proposed) Method 1014

A. He Fine Leak

1. Pressurize device to be tested in 100 percent He one hour minimum at 5 atmospheres minimum.

2. Transfer time between (1) and (3) is 30 minutes maximum.

3. Test device in a mass spectrometer calibrated for Helium.

4. Devices shall have a maximum leak rate of 1×10^{-7} Std cc/sec He Sensitivity Range 10^{-5} to 10^{-9} estimated.

TABLE IV
COMPARISON OF VARIOUS LEAK TEST TECHNIQUES

Process Step	Rocketdyne SF_6	Science Center	Raytheon	MIL-STD-883 Method 1014 "A"	MIL-STD-883 Method 1014 "B"	MIL-STD-883 Method 1014 "C"	MIL-STD-883 Method 1014 "D"	Autonetics AC477-0005 (Procurement)	Autonetics AA115-079 AA0607-010 (Process)	MIL-STD-202A	MIL-STD-202B	MIL-STD-202 III A
Evacuate	1 Hour		170 °C Vac Bake 4 Hours		0.5 MM Hg	1 Hour 1 Torr						
Pressurization Inoculation	60 psig SF_6		Freon Time Unknown	5 ATM He	5 ATM KR-85	FC-113 90 psig	100 psig Dye Penetrant	65 ±5 psig-He	65 ±5 psig-He			Unspecified
Pressurization Time	1 Hour			1 Hour	12 Minutes Minimum	3 Hours Minimum		4-1/2 Hours He	4-1/2 Hours He			Unspecified
Evacuate	He Flush	He Flush			0.5 MM Hg						1.5 inches Hg	
Transfer Time				1/2 Hour Max	4 Hours Maximum			20 Minutes	20 Minutes			Unspecified
Test Method	Gas Chromotograph	Metastable Helium	Weight Gain	He Leak	Geiger Counter	FC-43 Bubble Test	Examine for Dye Penetration	He Leak Bubble Test	He Leak Bubble Test	Bubble Test Bath	Bubble Test Bath	Tracer Gas
Test Limit	5×10^{-7} Std cc/sec	5×10^{-7} Std cc/sec	50 μgram gain	1×10^{-7} Std cc/sec	1×10^{-8} Std cc/sec	Observe for Bubbles	$>10^{-5}$ Estimate	5×10^{-7} Std cc/sec	5×10^{-7} Std cc/sec	Observe for Bubbles	Observe for Bubbles	Unspecified
Sensitivity Range	0.013 Hole to 1×10^{-7}	0.090 Hole to 1×10^{-8}		10^{-5} to 10^{-9}	10^{-5} to 10^{-10}	$>10^{-5}$ Std cc/sec	10^{-2} to 10^{-5} Estimate	10^{-2} to 10^{-7} Estimate	10^{-2} to 10^{-7} Estimate	$>10^{-5}$ Estimate	$>10^{-5}$ Estimate	
Temperature						FC-43 at 125 C		Glycol at 125 C	Glycol at 150 ± 10 C	Oil at 125 C	25 C	

B. Radioisotope Fine Leak

1. Devices are to be placed in chamber and chamber evacuated to 0.5 mm H_8 - time unspecified.
2. Chamber then filled with Kr-85/N_2 mixture to pressure at 5 atm absolute for 12 minutes minimum.
3. Kr-85/N_2 evacuated from chamber to 0.5 mm H_8.
4. Chamber refilled with air to atmos pressure.
5. Devices are then leak tested via scintillation counter within four hours of steps 1, 2, 3, 4.
6. Maximum leak rate allowable 1 x 10^{-8} atmos cc/sec of Kr-85 Sensitivity Range 10^{-5} to 10^{-10} estimated.

C. Freon Gross Leak Test

I. Leaks > 10^{-3} std cc/sec

1. Immerse device two in. below surface of FC-43 fluid maintained at 125 C ± 5 C.
2. View device immediately through a magnifier against a black background.
3. A single bubble or stream of bubbles from package constitutes a failure. No evidence of bubbles constitutes a good device.

NOTE: Sensitivity Range 10^{-2} to 10^{-3} estimated.

II. Leaks > 10^{-5} std cc/sec

1. Evacuate devices in vacuum chamber 1 hour (vacuum 1 Torr).
2. Backfill chamber with FC-113 without prior loss of vacuum.
3. Apply pressure of 90 psi for 3 hours minimum.
4. Remove devices and dry 3 ± 1 minutes in air.
5. Repeat steps 1 and 2 and 3 of Item C-I.

NOTE: Sensitivity Range 10^{-2} to 10^{-4} estimate.

D. Penetrant Dye Gross Leak Test

1. This test to be used on transparent glass encased devices only.
2. Devices shall be placed in chamber and completely covered with dye solution.
3. Chamber shall be pressurized to 100 psig for 2 hours minimum.
4. Remove pressure and wash devices with acetone, then with Alcohol, and then air-jet dry.
5. Examine devices with magnification 7 - 20X using UV light as illumination.
6. Any evidence of dye penetration is cause for rejection.

NOTE: Sensitivity range 10^{-2} to 10^{-5} estimate.

Raytheon Corp. leak test. - Information at this time is sketchy and not considered completely reliable.

1. Devices are baked in a vacuum oven at 170 C for 4 hours then weighed.
2. Devices are then immersed in a fluorochemical liquid (presumably freon) for an unstated time at an unstated pressure.
3. Devices are removed from liquid externally dried and weighed again.
4. A weight gain of 50 μgram per device constitutes a failure.

NOTE: Sensitivity - Unknown.

North American Rockwell Corporation - Rocketdyne Division proposed leak test (SF_6). -

1. Place devices one hour in Vac chamber.
2. Backfill vacuum chamber with SF_6 gas without first losing vacuum.
3. Pressurize chamber to 60 psig for one hour.
4. Open pressure chamber.
5. Place test device in test chamber and Helium flush for 5 sec.
6. Evacuate test chamber containing device to be leak tested through a gas chromatograph.
7. Any SF_6 gas escaping from "leaking" test device is detected and analyzed quantitatively by the gas chromatograph.

NOTE: Sensitivity Range = 0.013 in. diameter holes in package to 10^{-7} std cc/sec.

North American Rockwell Corporation Science Center Division proposed leak test. -

1. Place device to be tested in test chamber.
2. Flush lines and test chamber with He at 5 psig.
3. Determine background noise.
4. Read/record leak rate.
5. Remove device.

NOTE: Sensitivity Range = 0.090 in. hole to 10^{-8} std cc/sec He leak.

6. Watch for bubbles. Any sign of escaping bubbles or growing bubbles shall constitute a leaky device.

NOTE: FC-43 may be substituted for glycol per Spec AA0607-010. Bath temperature is 125 ± 5 C.

MIL STD 883 (Proposed)

Method A

1. Maintain bath of clear mineral oil at 125 ± 5 C.
2. Immerse device to be tested 1 in. below surface 1 minute minimum duration.
3. Any indication of escaping bubbles shall be cause for rejection.
4. Clean devices after test with suitable solvents.

NOTE: Sensitivity Range $> 1 \times 10^{-5}$ estimated.

Method B

1. Place devices in clear mineral oil bath 1 in. below surface in a vacuum chamber with a suitable viewing window.
2. Draw a vacuum not greater than 1.5 in. H_8 over bath and hold for at least one minute.
3. Any indication of escaping bubbles from devices shall be cause for rejection.
4. Clean devices with suitable solvents after test.

NOTE: Sensitivity Range $> 1 \times 10^{-5}$ std cc estimate.

Method C

1. Quite similar to MIL-STD-883 Method 1014 A.

Autonetics Procurement Spec No. AC 477-0005

1. Fine leak - in accordance with MIL-STD-202 Method 112, condition C, Procedure III A.

2. Gross leak - in accordance with MIL-STD-202, Method 112, Condition A, except use ethylene glycol or H_2O instead of mineral oil.

3. The allowable leak shall not exceed 5×10^{-7} cc/sec.

Autonetics Process Spec AA0607-010 and AA0115-079

1. Pressure bomb in He at 65 ± 3 psig for 4 ± 1/2 hours.

2. Leak test devices within 20 minutes of removal.

3. Leak limit is 5×10^{-7} std cc He/sec

4. Units passing He test are then bubble tested.

5. Immerse device 1 in. below surface of ethylene glycol maintained at 150 C ± 10 C. Hold 10 sec.

CONCLUSIONS

The objectives achieved under Contract NAS 12-4 have been significant in a diversity of investigational areas. In many instances potential innovations and improvements in process techniques have been clearly indicated. In others certain conclusions, though currently useful, should be regarded as temporary because of the viable nature of planar technology as a whole. In still other areas, potential conclusions are emerging as a result of progress in the solution of specific problems or as a result of reports of such progress in evoking additional investigations elsewhere. The complexity of integrated circuit processing, which is a direct result of the multiplicity of scientific and engineering disciplines on which the technology has been erected, generally has proved an effective stimulant to these advances. These accomplishments, and their process implications, are enumerated below:

1. Accomplished: Proof of strong entrapment of hydrogen from steam, by radiotracer technique, in thermally grown silicon dioxide layers. Process implications: The trapped hydrogen may contribute to the inversion of planar pnp transistors and to the instability of MOS-FET gate threshold voltages by proton migration. Proton migration recently has been confirmed (Ref 1).

2. Accomplished: Demonstration of sodium contamination, by neutron activation analysis, in silicon dioxide layers grown by conventionally "clean" methods. Process implications: Steps should be taken to exclude sodium in planar processing as an additional contributor to inversion. This effect has been abundantly confirmed elsewhere.

3. Accomplished: Demonstration of a slight initial difference in inversion recovery kinetics between a group of deuterated transistors and a comparable group of hydrated transistors. Process implications: Proton migration may be a source of inversion in planar transistors using oxides grown under moist conditions.

4. Accomplished: Development of progressive resistance to inversion by repeated inversion and deinversion of planar transistors. Process implications: Tends to confirm an electrochemical ion transport model for inversion, thereby achieving improved long-term reliability (Appendix B).

5. Accomplished: Proof of a strong EPR signal from the interaction of vacuum-deposited aluminum on silicon dioxide layers, indicating reduction by the aluminum and the formation of oxygen vacancies. Process implications: The formation of oxygen vacancies by this mechanism can be avoided by using less active metals (e.g., gold) for intraconnections, thereby reducing the possibility of inversion and contributing to long-term reliability.

6. Accomplished: Demonstration of an absence of an EPR signal corresponding to oxygen vacancies at the $Si-SiO_2$ interface. Process implications: Inversion from this specific source is highly improbable.

7. Accomplished: Demonstration of the same characteristic EPR signal from either sodium or fluoride contamination of silicon dioxide. Process implications: Traces of fluoride, as well as sodium, produce similar defect structures in the oxide that may act as trapping states and contribute to inversion. Steps should be introduced after etching treatments to remove residual fluoride.

8. Accomplished: Proof that the effect of hydrogen on transistor betas, by environmental testing, is nonspecific and tends to be curative rather than degradative. Process implications: The presence of hydrogen in package atmospheres is not inimical to the long-term reliability of planar bipolar transistors.

9. Accomplished: Demonstration that propagation of significant crystal damage, by etch-pit count technique, into adjacent sensitive device areas as a result of conventional scribing procedure is improbable. Process implications: Scribing done with appropriate equipment, combined with precise registry and proper maintenance, does not appear to constitute a reliability hazard. Continued alertness in this area, however, is recommended as the investigation was not exhaustive and did not cover such contingencies as diamond wear, registry deviations, etc.

10. Accomplished: By calculation, in diffusion steps complete mixing of input gases occurs in the first 4 inches of furnace tube. Process implications: Introduction of baffles, or other mechanical means to create turbulence, will not avail in improving the uniformity of diffusion doping as conventionally practiced. This exercise, however, ignores potential streaming effects across the wafers themselves, particularly in situations where the diffusant is an extremely dilute component of the gas phase.

11. Accomplished: Demonstration that dielectric defects in oxide layers generally are cumulative with processing. Process implications: Innovations should be sought that minimize the thermomechanical flexing caused by high-temperature treatments.

12. Accomplished: Demonstration that the higher the compressive stress in an oxide layer, the higher the defect abundance. Process implications: Compressive stress can be moderated by additives that reduce the glass set temperature and the thermal expansion mismatch with silicon. This approach, however, is beset with certain difficulties, such as the avoidance of unwanted impurity (trapping) states and the exact control of composition. Rather than attempt to manipulate the compressive stress in this fashion, it is recommended that defect occurrence be brought under control by identifying and eliminating the physical irregularities which activate local ruptures in the oxide.

13. Accomplished: Demonstration that a higher defect incidence in oxide grown on mechanically polished than on chemically polished substrates. Process implications: One of the physical irregularities contributing to oxide defects may be embedded lapping grains or crystal damage sites caused by lapping. Wafer pretreatments therefore should be terminated by some form of chemical polish.

14. Accomplished: Demonstration that superficial etching by HF increases significantly the oxide defect population to thickness ratio. Process implications: Control of MOS gate oxide thicknesses, which are typically of the order of 1000Å, should be accomplished by growth techniques rather than HF thinning techniques. This would require additional precautions to prevent or remove outer-skin sodium contamination normally eliminated in HF thinning.

15. Accomplished: Observation that a significant localization of defects at abrupt steps in oxide thickness. Process implications: Fortunately a large proportion of such steps are located at windows where metallization contact with the substrate is desired. However, cognizance of this potential failure mode should be a factor in integrated circuit design. Metallizations, where possible, should be routed to avoid sharp changes in oxide thickness, and oxide overlap at contact windows should be sufficient to provide impervious protection to surrounding junctions and substrate.

16. Accomplished: Proof that repeated heating and cooling of oxidized silicon wafers in an inert ambient produces a substantial increase in defect density. Process implications: This observation provides some insight as to why continued processing contributes to defect incidence (item 11) as well as arguing against manufacturing decisions to reprocess in an effort salvage, for example, the results of an inadequate diffusion.

17. Accomplished: Demonstration that gentle mechanical wiping of oxide layers increases the incidence of dielectric defects. Process implications: As in Item 16 this provides further insight into the structural character of oxide defects, inplying that a spalling effect is involved that loosens material sufficiently at certain sites to render it susceptible to subsequent removal by mechanical means. It also indicates that the handling of wafers during manufacture must be minimized as much as possible and done with great care. This would apply to almost any tool used in handling, since the referenced wiping experiments were done with cotton swabs.

18. Accomplished: Proof that removal of one oxide layer (by etching) produces a significant increase in the defect density of the oxide layer remaining on the opposite face of the wafer. Process implications: The wafer is mechanically flexed by this treatment, as amply demonstrated by experiment, imparting a convex curvature to the opposite layer, which contributes to the postulated spalling effect adduced in Item 17, above. If a wafer could be processed completely symmetrically, using the same masks, etching steps, etc, on both sides, dielectric defects from this source could be minimized. A more practical recommendation is to process only one side while maintaining intact oxide on the other.

19. Accomplished: Proof that defect density decreases exponentially with increasing oxide thickness and with the square root of oxidation time. Process implications: Use as thick oxide layers as economically feasible where other design criteria are not thereby compromised.

20. Accomplished: Demonstration that existing defects in thermal oxides often can be reduced significantly by a pyrolytically deposited oxide. Process implications: This procedure is an expensive extra step and does not really solve the basic defect problem. The effectiveness of this procedure varies considerably among processors. Uniform thickness control of the deposited oxide is difficult to achieve.

21. Accomplished: Proof that the presence of water during oxidation, or at the termination of a dry oxidation, produces a lower defect incidence than in oxides grown dry. Process implications: This effect of water is interpreted as a result of a reduction of bond strain from the introduction of hydroxyl groups into the silica network in a manner analogous to that of other oxide additives. The so-called hydroxyl groups, however, are really acidic and capable of yielding protons that may contribute to inversion, as indicated in Items 1 and 3. Nevertheless, the use of water as an oxidation additive is recommended for most planar processing on the basic that proton migration is a minor problem relative to that of oxide defects.

22. Accomplished: Demonstration that variation in wafer cooling rates after oxidation has a negligible effect on dielectric defect incidence. Process implications: Control of cooling rates is unessential. This effect is consistent with a thermal expansion mismatch mechanism that is dependent only on ΔT and not the derivative of ΔT with respect to time. However, heat soaking at a phase transition temperature within the ΔT interval may produce a beneficial bond rearrangement and is being investigated further.

23. Accomplished: Demonstration that addition of nonvolatile mineral salts to steam source does not increase defect densities. Process implications: Water quality with respect to nonvolatile constituents is not critical. Spray carryover either is negligible or is trapped by the hot furnace tube before reaching the wafers.

24. Accomplished: Proof that oxide growth rate variations do not affect defect densities significantly. Process implication: Control of such parameters as oxidation temperature, or steam concentration in the process gas, is not critical from the standpoint of defect densities. However, such control remains critical for other reasons, such as control of layer thickness, diffusion boundaries, etc. Moreover, oxidation rate at the very beginning of oxidation is emerging as an important parameter affecting defect densities in very thin oxides.

25. Accomplished: Demonstration that substrate doping has little effect on defect densities. Process implications: None of significance, unless high boron doping is encountered (Appendix E-8, 9).

26. Accomplished: Proof that oxide defect densities are not associated with dislocation densities or stacking faults pre-existing in the substrate. Process implications: Adjustments in substrate crystal perfection, or epitaxial deposition perfection, will not avail in improving oxide defect densities, probably because oxide defects generally are at least a thousand times larger than the substrate crystal imperfections. More

recent work indicates that macro defects in the substrate may determine the loci of subsequent oxide rupture.

27. Accomplished: Demonstration that particulate contamination on silicon wafers, unless exceedingly dense or reactive, does not contribute significantly to oxide defects. Process implications: In process lines where an oxide defect problem exists, the origin of the problem probably need not be sought in air particle counts or potential dust deposits on wafers prior to oxidation. Other wafer contaminants of a more adherent character, however, may be contributing factors. The above recommendation should not be construed as suggesting the relaxation of general cleanliness standards. In photolithographic procedures, for example, ambient dust may become a source of "artificial" dielectric defects created in subsequent etching steps. The essential purpose here is to rank failure sources according to their relative probability in order to save costly engineering time in real situations.

The above experimental observations were compiled on the basis of their more or less direct relevance to process techniques. Many additional experiments, however, were directed toward questions of mechanism which, if properly answered, might provide direct, logical process improvements. Some of the more important observations are especially pertinent to the successful evolution of large scale integration because they deal with the physical nature and origin of oxide dielectric defects. These are summarized below:

1. Accomplished: By replicate electron photomicrography, the detailed definition of the morphology of oxide defects identified independently by electrophoretic decoration. Mechanism implications: Pileups of oxide at the defect site (see Figure 1) suggest a process of compressive upheaval.

2. Accomplished: Demonstration of initial (virtual) defect densities of the order of 100 to 1000 per cm^2. Mechanism implications: Suggests an initial distribution either of substrate surface irregularities or of process induced inhomogeneities.

3. Accomplished: Proof of a kinetic anomaly at the initiation of oxidation. Mechanism implications: Initial distribution of defects may be oxidation rate dependent.

4. Accomplished: Demonstration of a typical defect decay rates versus growth in oxide layers of 750 Å or less. Mechanism implications: Not clear, but suggests manipulation of oxidation rates during the first few hundred Å of growth may have a controlling effect on subsequent growth.

5. Accomplished: Demonstration that oxidative precleaning of wafers (with HNO_3) prior to oxidation tends to reduce defect densities except in the very thin oxide range. Mechanism implications: This was first regarded as an indication that moderation of the initial oxygen diffusion rate would become an important defect control parameter. However, see below.

6. Accomplished: Special nonoxidative precleaning techniques equal to oxidative treatments in reducing defect densities and superior in the very thin oxide range. Mechanism implications: Initial diffusion rate (or thin oxide distribution) is not an important control parameter, but oxidation rate control still may be important on the basis of achieving an initial "equilibrium" distribution of oxide.

7. Accomplished: A chemical polish pretreatment with HCl which tends to reduce defect densities. Mechanism implications: Present results are not yet quantitative but indicate that macroscopic promontories (of the order of one micron) may be substrate features that determine subsequent oxide defect sites.

Other accomplishments on this program are related to the accumulation of information associated with process techniques or with the process origins of component reliability problems. As such, these compilations are of more general applicability to process problems than the discrete observations derived from experimental studies as outlined above. The information in these compilations is derived in part from previous failure analysis programs at Autonetics and in part from the current literature. They are summarized briefly below:

1. Accomplihsed: "Instruments for Failure Analysis" (Appendix K). Process implications: Tabulation provides instrumental techniques applicable to the examination of component abnormalities and failure modes. The compilation should be of particular assistance to management decisions required in initiating failure investigations in established processes.

2. Accomplished: "Sensitivities of Instruments" (Appendix K). Process implications: This is a companion tabulation of Item 1 above, which will assist in the choice of instrumentation for particular analytical problems by providing senstitivities, spectral ranges, limits of resolution, etc, of available instruments.

3. Accomplished: "Thermodynamic Analysis of Ambient Gas Effects" (Appendix I). Process implications: Useful in settling questions of materials compatibility, particularly at the design stage, by specifying, among those materials in most common use, those gas-solid interactions which are, and those which are not, thermodynamically allowed. Also useful in discovering or predicting possible slow reactions that may contribute to long-term drift.

4. Accomplished: List of leak test methods currently in use of under development (pp 29-36). Process implications: As long as conventional packaging techniques are used, hermeticity will continue to be a problem, and analytical methods for its evaluation will be required. The compilation aids in the selection of method and/or helps to assess the reliability of results reported elsewhere. Potential directions of continued test improvement are indicated.

It is clear that the observations and conclusions enumerated above pertain to a still vigorously evolving technology. Also obvious is the corollary fact that reliability and process control problems will continue to abound in such a dynamic situation. One of the more important problems, and an item of particular concern to this program, is the reproducible achievement of the compositional uniformity and physical integrity of dielectric layers. Once this objective is achieved, the foundation for large scale integration will have been laid. It is believed that significant progress in this direction has been made and that further efforts will be extremely rewarding. On a more general scale, however, there is no doubt that new problems will arise and that constant vigilance should be maintained for their detection and ultimate correction.

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APPENDIX A. HYDROGEN ISOTOPE INVESTIGATION OF PASSIVATION SILICON OXIDES*

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The silicon dioxide passivation layers utilized for dielectric isolation in planar silicon devices are subject to two general types of failure: dielectric anomalies which give rise to shorts between metallizations and the silicon substrate, and field induced accumulations of positive charge which produce inversion in bipolar transistors and gate threshold voltage instability in MOS-FET's. The present study attempts to shed light on the latter problem by identifying positive charge accumulation with the electromigration of specific positive ions.

Conventional thermal oxidation procedures employ a small proportion of steam in the process gas to promote favorable mechanical and dielectric properties in the resulting oxide[1]. Although these procedures are conducted at elevated temperatures (1000-1200 C), opportunity nevertheless exists for the oxide entrapment of hydrogen derived from the steam. This can be understood from the schematic representation of the process postulated in Figure A-1. Most of the initially produced --- Si-O-H groupings should interact with equivalent nearest neighbors with the elimination of water and the formation of Si-O-Si bridges. A small proportion of such groupings, however, will be isolated from reactive neighbors in the process and will remain randomly distributed in the oxide. The residual --- Si-O-H groupings may be regarded as acidic sites capable of releasing protons under the influence of an applied electric field, or of exchanging protons for other monovalent cations, such as sodium ions, analogous to the function of ion exchange zeolites. The density of residual acidic sites will then be a function of the base concentration (HOH, NaOH) present during oxidation, and they will act as reservoirs of positive ions which may contribute to the inversion phenomenon.

In order to demonstrate whether residual hydrogen was present in the oxide a tritiated oxidation run was performed on boron-doped high resistivity silicon wafers using one gram of water containing 100 ± 5 millicuries of tritium. Oxidation was conducted at 1150 C in the apparatus shown schematically in Figure A-2. Gases were metered and purified by conventional means using an N_2:O_2 flow ratio of 3:2. Tritium labeled water was picked up by the O_2 stream from a reservoir maintained at 95 C This reservoir was a single, bypass fitted U-tube of sufficient internal diameter to permit evaporation of the water without mechanical carry-over by the gas stream. The process was timed to produce approximately 2000 Å of oxide on the wafers which utilized the entire charge of water in the reservoir. The entire procedure was designed to duplicate as closely as possible conventional methods of silicon oxidation for planar devices.

[1]Delivered at the Electrochemical Society Meeting, Cleveland, Ohio, 3 May 1966.

Several techniques were used to measure the level of tritium present in the treated samples. A 2 π counter was employed without any indication of H^3 activity. Similar results were obtained with a liquid scintillation counter. A 4 π counter was then utilized with the results given in Table A-1. The plus-or-minus value represents one standard deviation determined from counting statistics only. In this case, this represents an 82-percent probability that H^3 was detected. An approximate hydrogen level of 10^{10} atoms/cm^2 in 2000 Å of oxide was tentatively inferred from this result.

TABLE A-1
TRITIUM ACTIVITY IN OXIDE DERIVED FROM 100 MC/GRAM WATER

	Counting Time, Minutes	Total Counts	Net Counts per Minute
Background	450	52667	
Treated Disc	913	108054	1.32 ± 0.93

In view of the somewhat inconclusive nature of these results, it was decided to examine the oxide for other impurities that might displace hydrogen from the oxide matrix and to repeat the experiment using a higher tritium activity. Sodium ions were sought, therefore, by neutron activation analysis of a five-wafer sample. An additional five-wafer sample from which the oxide had been stripped also was activated. The composite samples and a sodium standard were irradiated 1/2 hour at 250 kw in a Mark I TRIGA reactor with a thermal neutron flux of 1.8×10^{12} cm^{-2} sec^{-1}. The activated oxide was stripped off the first sample, concentrated by evaporation, and counted overnight in a NaI well detector coupled to a multichannel pulse-height analyzer. The irradiated sodium standard was counted in identical geometry. The 2.75 Mev photopeak of Na^{24} was used for analysis because of the comparative freedom from interference by other residual activities (e.g., Si^{31}) present in the samples. Other peaks attributable to Au^{198}, Cu^{64}, and Mn^{56} also were found. The etch solution concentrate (0.9799g) was found to contain 0.0196-0.004 ug Na which indicates an average concentration of approximately 8×10^{17} atoms/cm^3 in the original oxide. Sodium in the stripped wafers was found to be indistinguishable from a slight Cu^{64} background indicating a level ≤ 0.73 ppb, or 4×10^{13} atoms/cm^3, Na in the original silicon. It was presumed from these results that the sodium in the oxide originally had boiled out of the quartz tube during the oxidation or had been introduced by the gas stream.

The tritium labeled oxidation was repeated with the following modifications:

1. On the day prior to the run, the quartz reaction chamber was purged 8 hours at 1200 C with an O_2/N_2 mixture containing HCl in an attempt to extract out available sodium (as NaCl) from the quartz surfaces. The quartz wafer holder also was included in this treatment.

2. Specific activity of tritiated water was increased to 1 curie/gram. Total quantity remained 1 gram.

3. After initial purging prior to the oxidation, the O_2/N_2 carrier gas flow was reduced to a negligible value (about 5 ml/min), while the tritiated water was distilled into the reaction chamber. When transfer of the water was complete (about 40 min), gas flow was shut off producing an open-ended static system. The intention here was to extend the catalytic effect of the water for a longer period while maintaining the selected ratio of oxygen to nitrogen. The volume of the system was such that the uptake of oxygen by the silicon would have a negligible effect on this ratio.

4. Treatment was prolonged (to 2.5 hours) in order to produce thicker oxide (9000-10,000Å) and a more significant sample activity.

Oxide thickness on the treated wafers was estimated visually to be uniformly about 9000 Å and confirmed interferometrically at 9140 Å. Net area of wafer surfaces was 3.38 cm^2 per side, giving an oxide volume (2 sides) of 6.19×10^{-4} cm^3/slice.

Four wafers (of a total of 24 treated) were counted using 4-π geometry with an estimated counting efficiency of 50 percent. The loss of 50-percent efficiency was due to the combined absorption of the 9000 Å oxide layer on both sides and the 10,000 Å sample support film on one side of the sample. Calibration for tritium was derived from a polymethylmethacrylate H^3 standard from New England Nuclear Corporation. The net H^3 count rates of the four samples had a standard deviation of about 1 percent of the value in each case. The atomic ratio of H^1:H^3 in the tritiated water employed was 3390:1. Total hydrogen content in the silicon oxide of each wafer, computed from the observed count rates and the data given above is presented in Table A-2.

TABLE A-2.
TRITIUM ACTIVITY IN OXIDE DERIVED FROM 1 CURIE/GRAM WATER

Sample	Net CPM, Total	DPM H^3 per cm^2	H^3 Atoms per cm^2	Total H Atoms per cm^2	Total H Atoms per cm^3
1	360.5	103	9.8×10^8	3.4×10^{12}	3.7×10^{16}
2	345.4	101	9.5×10^8	3.3×10^{12}	3.6×10^{16}
3	225.2	67	6.2×10^8	2.1×10^{12}	2.3×10^{16}
4	199.1	59	5.5×10^8	1.9×10^{12}	2.1×10^{16}
Average				$2.7 \pm 0.7 \times 10^{12}$	$2.9 \pm 0.7 \times 10^{16}$

The spread in these results is somewhat higher than expected and difficult to explain inasmuch as differences in oxide geometry (i.e., wafer area and oxide thickness) were relatively insignificant. However, this variation could not be attributed to differences in surface absorption of tritium labeled water because the oxidation run was terminated by a tracer-free nitrogen purge in excess of 1 hour at the oxidation temperature. Entrapment of hydrogen during formation of the oxide at 1150 C was thereby established.

The last three specimens given in Table A-2 were re-assayed for beta activity in the 4- π counter after 550 hours exposure to a laboratory environment ranging from 20- to 40-percent relative humidity.

The average hydrogen concentration in the oxide layers was found to be relatively unchanged, as shown in Table A-3, indicating negligible exchange of the tritium with ambient moisture.

TABLE A-3.
TRITIUM EXCHANGE WITH HUMID ENVIRONMENT

Period	Sample	Net CPM, Total	Total H Atoms per cm^3	Average
Initial	2	345.4	3.6×10^{16}	2.7×10^{16}
	3	225.2	2.3×10^{16}	
	4	199.1	2.1×10^{16}	
After 550 hours humid exposure	2	354.6	3.7×10^{16}	2.7×10^{16}
	3	270.1	2.8×10^{16}	
	4	142.7	1.5×10^{16}	

Assay for sodium in the oxide layers of these wafers was then carried out by the neutron activation method previously described. The average sodium population was found to be 1.1×10^{18} atoms/cm^3. This result is not substantially different from that observed in the first tritiated oxidation sample, and the HC1 pretreatment was deemed ineffective.

Beta assay on the remaining 20 wafers was performed 5 months after their initial treatment. Results are compared with earlier assays in Table A-4.

TABLE A-4.
STABILITY OF TRITIUM LABELED PASSIVATION OXIDE

Elapsed Time (Days)	Number of Samples	Average Net Beta Count/Wafer C/M	Calculated H Content ($\times 10^{16}$ Atoms/cc)
0	3	257 ± 59	2.7 ± 0.6
23	3	253 ± 74	2.7 ± 0.8
150	20	186.7 ± 58.8	1.96 ± 0.60*

* Corrected for radioactive H^3 decay

Loss of activity due to H^3 exchange with the environment cannot be inferred from the last entry because of the spread in results (about 33 percent). Nevertheless, a wrapper (paper) from one of the specimens was analyzed in the 4- π counter. No evidence of H^3 exchange was detected.

Tritium activity distribution likewise was examined for internal consistency by inverting the first three wafers (of the group of 20) on the aluminized mylar support film and recounting. Deviation of beta activity between opposite sides was found to be relatively insignificant compared to deviation between wafers, as shown in Table A-5.

TABLE A-5.
BETA ACTIVITY VERSUS COUNTING ORIENTATION

Sample Number	Side Supported	Activity (C/M)	Average	Deviation, Percent
1	A	88	94	6
	B	100		
2	A	279	284	1.4
	B	288		
3	A	120	118	3.3
	B	114		

It was concluded from these results that significant amounts of hydrogen are retained in the oxide matrix if steam is present in the oxidation process gas, and that it does not exchange readily at room temperature with covalently bonded ambient hydrogen.

In order to investigate whether hydrogen trapped in passivation oxide was capable of contributing to inversion, fabrication of thirty small geometry pnp planar silicon transistors was requested from an established manufacturer* prepared under identical conditions except that the initial oxide on half the specimens was grown in the presence of 99-percent D_2O. These devices were subjected to inversion stress (temperature and collector-base reverse bias) and the kinetics of inversion recovery (baking at timed intervals under zero bias) determined. Thermal activation energies of recovery were calculated from the kinetic data according to a previously described method[2], and the results for hydrated and deuterated specimens compared. A greater activation energy was expected to be associated with the diffusion of the isotope of higher mass.

All 30 of the transistors were electrically good as-received. Their response to inversion stress, however, was variable. Consequently, they were subjected to initial inversion stress of 200 C at 40 V_{CB} for various lengths of time in order to classify them in terms of usefulness for recovery experiments. In order to be useful, the inverted device was required to show a leakage about 1×10^{-9} amps (with available instrumentation) and have a region where I_{CBO} was independent of voltage. This would indicate surface leakage as distinguished from bulk leakage. Of the 30 specimens, only eight were found to undergo inversions suitable for study, five of which were deuterated.

*Fairchild Semiconductors

The group of eight transistors was subjected to two complete evaluations, each of which involved from four to eight inversions and recoveries. The thermal activation energies associated with the recoveries are presented in Table A-6. Results from the first treatment indicate that the deuterated values may be higher than the hydrated values, as expected, but the spread in results does not permit definite conclusions to be drawn. The activation energy of the last listed result may, in fact, be a result of a trace of sodium for contamination rather than deuterium. Omitting this value, the remaining four deuterated samples yield an average recovery activation energy of 0.67 ± 0.06 cv.

TABLE A-6

INVERSION RECOVERY KINETICS OF HYDRATED AND DEUTERATED TRANSISTORS

Process Steam, Initial Oxidation	Thermal Activation Energy of Recovery (e.v.)		
	First Treatment	Second Treatment	Third Treatment
H_2O	0.46	0.86	
	0.54	0.50	
	0.74	0.56	
Average	0.58 ± 0.08	0.64 ± 0.15	
D_2O	0.56	0.72	
	0.68	0.40	
	0.70	0.74	
	0.74	0.45	
	1.29	0.82	0.55
Average	0.79 ± 0.19	0.60 ± 0.16	

Results from the second treatment appear to be generally more uniform between the two groups but are more erratic. Assuming that inversion is produced by an electrochemical transport of positive ions, one might also expect a contribution from electrode processes. Discharge of such ions in the form of neutral species at the cathodic surface would tend to remove them from participation in the charge transport process. If more than one type of ion is present in the rigid SiO_2 electrolyte, their ratios should change in succeeding inversion treatments, thus introducing variations in the kinetics of inversion recovery. Moreover, the deuterium, undoubtedly present as a minor component since it was employed only in the first oxidation, should discharge and escape by normal diffusion ultimately into the can atmosphere leaving residual normal hydrogen as the major participant. This type of proton transport in SiO_2 has been considered in detail previously by Collins[3]. Thus, the increasing spread in results and the apparent decrease in difference between the two isotopic groups with succeeding inversions can be explained. Additional evidence of these effects is indicated by the third inversion recovery treatment on the last deuterated specimen given in Table A-6.

It can be concluded from these experiments that hydrogen is definitely trapped in conventional steam grown silicon dioxide, that the phenomenon of inversion probably is electrochemical in nature, and that hydrogen ion migration probably is a contributing factor in inversion.

Acknowledgements

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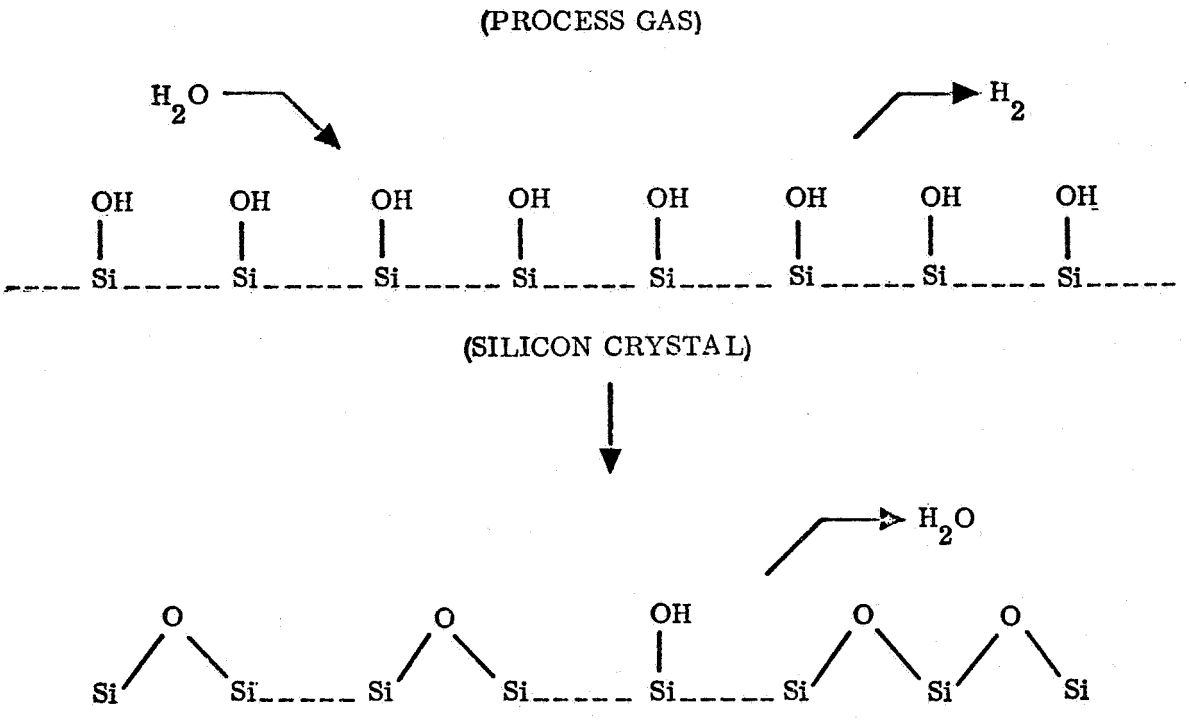


Figure A-1. - Interaction of Water With Silicon (Schematic)

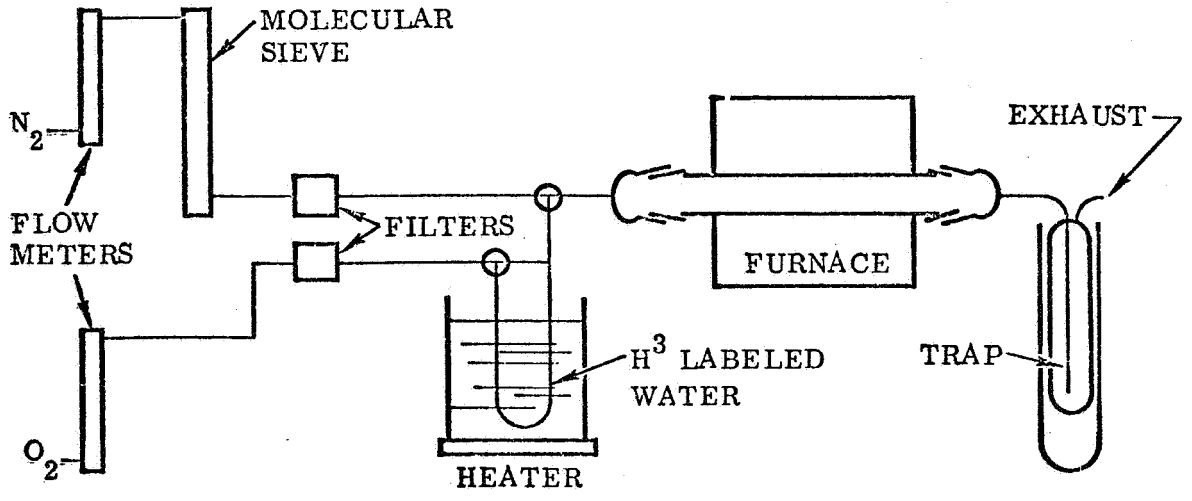


Figure A-2.-Silicon Wafer Oxidation Equipment (Schematic)

APPENDIX B. INVERSION HARDENING: TECH BRIEF 67-10176

Evidence is presented in Table B-I to show that repeated inversions are capable of producing "inversion hardening" in planar transistors. This effect is potentially desirable because it reduces the possibility of long-term drift in transistor performance. Thus inversion hardening may be of some utility in deep space missions where reliable transistor function is needed over extended periods of time.

It should be recognized that these data are preliminary in nature and do not necessarily represent the maximum inversion resistence that may be possible with this technique. It also is evident from the data that considerable variability in response to the treatment exists between transistors. This variability could be used for screening purposes in selecting components for missions of long duration. Some transistors, of course, show no initial tendency to invert, which indicates good process control in their manufacture. Further investigation of inversion phenomena is required before this effect can be assigned a mechanistic model.

TABLE B-1
INVERSION HARDENING OF 2N2412 SMALL SIGNAL PNP TRANSISTORS

Unit	Initial Inversion Leakage (na)*	Number of Inversions	Total Time Under Inversion (hours)**	Final Inversion Leakage (na)*	Inversion Hardening (%)
1	108	8	96	17.4	84
2	900	8	96	375	58
3	19	6	6	50	None
4	80	2	2	34	58
5	96	2	2	27	72
6	50	8	96	25	50
7	3.5	4	4	1.65	53

*At 40 V_{cB}, 25 C
**At 40 V_{cB}, 200 C

APPENDIX C. EPR INVESTIGATION OF THERMALLY GROWN SiO_2

Introduction

The employment of integrated circuits in electronic systems has shown that a major failure mode is excessive current across reverse biased p-n junctions. The two main conditions that cause this excessive current are silicon surface inversion and contamination of the passivation oxide surface. Silicon dioxide is almost universally used for surface passivation. The basic problem is one of oxide purity and its control during the processing of the integrated circuits. The thermal oxidation of the silicon surface has been found to induce a negative charge near the silicon surface causing it to become more n type. This is thought to occur by charge trapping in fast states related to chemical impurities or structural defects in the interface region and in slow states related to oxide impurities. Several oxide models have been postulated in the literature to explain the integrated circuit surface inversion problem. These include oxygen vacancy migration, impurity redistribution during oxidation, metallic ion migration, hydrogen or hydroxyl ion migration, oxide surface charge separation, precipitation near bulk oxygen, interface states, and a heterojunction formation. Several recent review articles describe these in detail (Ref C-1, C-2). A comprehensive bibliography was recently published (Ref C-3). The defect structure of silicon dioxide showing its complexity is shown in Figure C-1 (Ref C-4).

In this study, electron paramagnetic resonance has been used on thermally grown silicon dioxide to investigate the oxygen vacancy model. Four resonance signals have been detected from silicon dioxide samples prepared under various conditions of temperature, ambient, and chemical contamination. These data were taken at the X-band frequency of 9.3 GHz and 3400 gauss using a dual cavity operating between -180 C and +300 C. In addition to the known silicon line at $g = 2.006$, several others have been found after oxidation of both intrinsic and extrinsic silicon powder. These have been associated with sodium or fluorine retention in the oxide and hydrogen entrapment. Signals also were obtained from single crystal samples with high purity aluminum vacuum deposited over the oxide. This resonance may be due to oxygen vacancies generated by an electrode reaction between the aluminum and the oxide.

Silicon Dioxide Sample Preparation

The silicon crystals used for oxide growths in this study were obtained in wafer form from major suppliers. They were either chemically or mechanically polished prior to oxidation. A wide range of resistivity was used, which included acceptor type (boron), donor type (phosphorus), and intrinsic material. These parameters are listed in Table C-1. Single crystal samples, with various oxides grown up to 20,000 Å thickness showed no resonance absorption, so powdered samples were then used. The powdered samples provide a much larger ratio of silicon dioxide to silicon for the sample tubes used in the resonance cavity. A few oxide samples were made on float zone silicon while most were on the more common Czochralski type. From the resonance data, it was shown that the signal characteristics found depended only on the oxidation method and not on the silicon resistivity or type dopant. No signals,

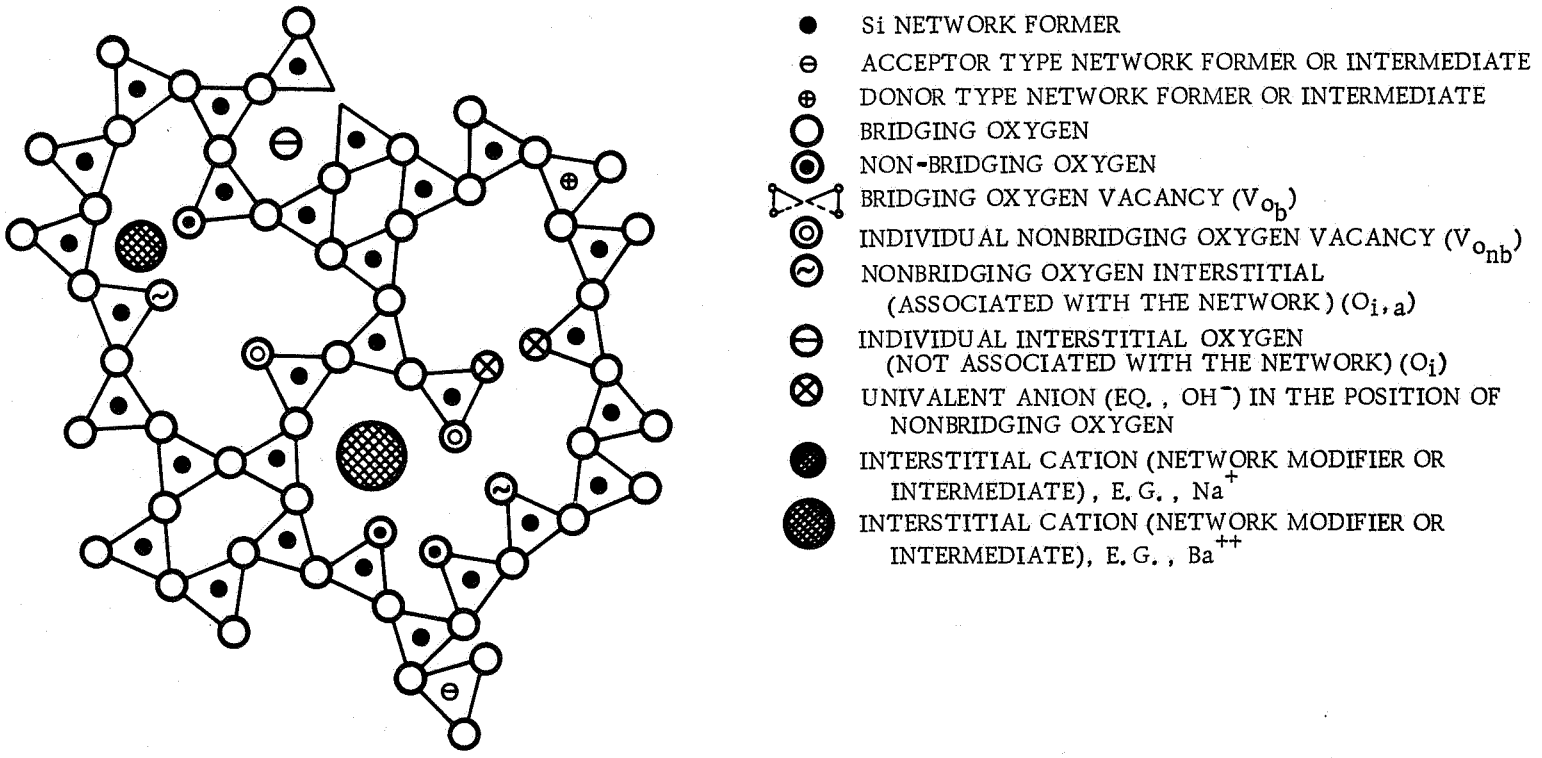


Figure C-1.- Schematic Model of Some Defects in a Two-Dimensional Model of the Silicon Dioxide Network. The Si-O Tetrahedra Are Shown as Triangles.

TABLE C-1
SILICON MATERIAL PARAMETERS OF SAMPLES USED FOR OXIDE GROWTH

Source	Original Form	Dopant	Resistivity ohm-cm
Texas Instruments	Wafer	Phosphorus	8 - 12
Monosilicon	Wafer	Boron	31 - 34
	Wafer	Boron	0.004 - 0.005
	Polycrystalline	Intrinsic	> 500
Dow Corning	Wafer	Boron	75 - 125
	Wafer	Boron	5 - 10

however, were found using the heavily doped 0.004 ohm-cm silicon material which is most likely due to the large microwave energy losses expected in a conductive material.

The oxides studied here were thermally grown by the conventional methods being used for integrated circuit manufacturing. The silicon was usually oxidized at temperatures between 1100 C to 1150 C in dry oxygen or wet oxygen. The water bath temperature was at 99 C for the steam or wet oxide growth. The silicon powder was usually etched in HF, rinsed with deionized water, and dried in a nitrogen stream. The powder was carried in a small quartz boat inside the furnace. For the wet oxide growth the silicon was usually exposed to dry oxygen and dry nitrogen for 5 minutes at 1150 C before introduction of wet oxygen for various growth periods. The oxidation time was used to control the oxide thickness. For wet oxides the period was usually extended to 6 hours because resonance signals recorded on thinner oxides had less intensity. For dry oxides the oxidation period was extended to 90 hours to achieve an equivalent thickness. These two methods gave oxides of thickness between 14,000 and 18,000 Å. For comparative data a single crystal of silicon was sometimes placed near the powder samples during oxidation. Capacitance - voltage measurements were made on these single crystal oxide samples after oxidation. Weight measurements were also made before and after oxidation on a few of the initial samples.

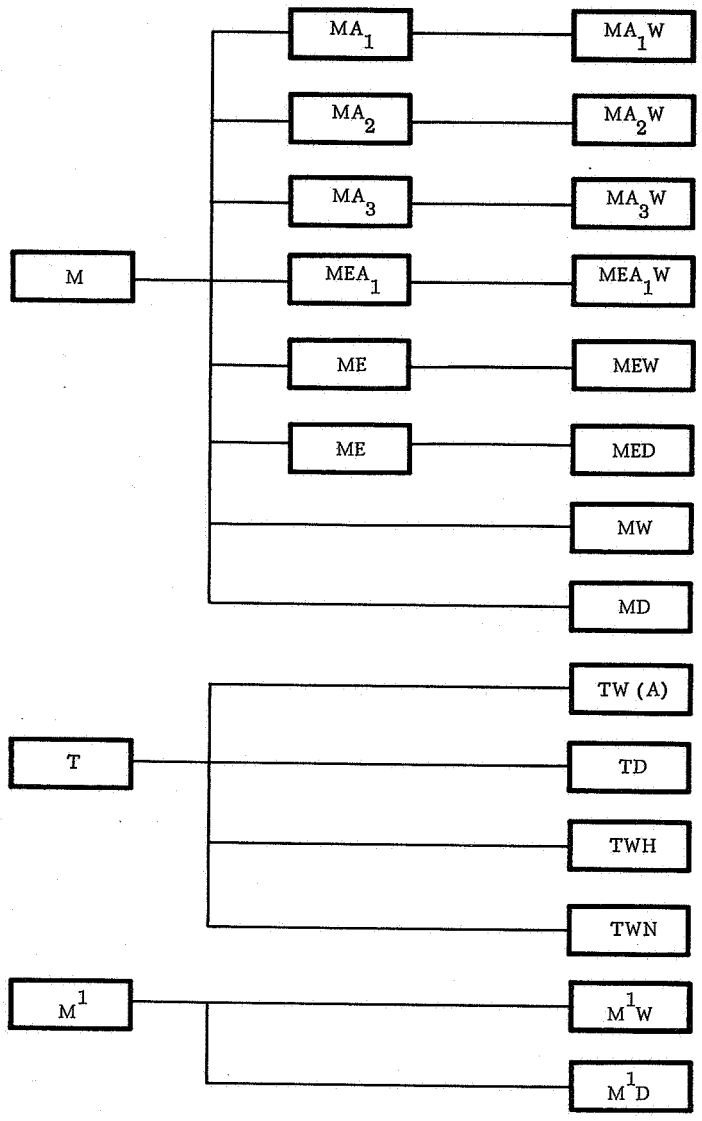
After resonance data had been taken on the silicon and silicon dioxide samples prepared in the conventional way, a number of special treatments were made on the samples to generate comparative data. These thermal and chemical treatments are listed in Table C-2. The controlled chemical contamination of the samples before and after oxidation had the greatest effect on the resonance spectra. Two other types of samples were briefly studied. One was silicon dioxide baked in hydrogen at 1150 C. The other samples had high purity aluminum vacuum deposited on single crystal oxides. The breakdown of sample treatments for the first set of samples is shown in Figure C-2. Each letter shown denotes the material type or process step taken.

TABLE C-2
SPECIAL SAMPLE TREATMENTS

	Thermal	Chemical	Etch
Preoxidation Treatment	Anneal in nitrogen between 800 C and 1200 C for periods up to 96 hours	NaOH NaCl HCl P_2O_5	$HF + HNO_3$
Postoxidation Treatment	Anneal in nitrogen at 1150 C for various periods	NaCl HCl H_2 HF	HF

Resonance Spectra

Electron spin resonance technique.- The theory of electron paramagnetic resonance is well developed and the technique widely used to study chemical structure and bonding of paramagnetic materials. The interactions that the unpaired electrons have in real materials are generally complicated. It is through these interactions which perturb the magnetic states of the system, that the materials can be studied by electron spin resonance. A system of free electrons has its electron spins and associated magnetic moments distributed randomly in all directions each with the same energy. If a steady magnetic field is applied to the system the electrons will align themselves either with or opposite to the applied field. These two system states will have different energy levels in the applied field. By superimposing a microwave radiation on the sample field electron transitions can be made to the higher energy state and this loss in microwave energy detected as a resonance condition. Those electrons in the higher energy state will emit photons and return to the lower energy state. Other mechanisms allow these electrons to give up their energy also and these lead to a study of relaxation processes between the electrons and the lattice or other spins. The simplest condition for microwave absorption of energy is that the microwave frequency f satisfy $hf = g \mu H_o$ where H_o is the applied constant magnetic field, g is the spectroscopic splitting factor (a tensor in general), with h and μ constants. The factor of interest is usually the g-factor. It is analogous to the Lande g-factor which describes the addition of spin angular momentum to orbital angular momentum to give the total angular momentum. The free electron g-factor has a value of 2.0023. Measured g-factors which differ from this valve are a measure of interactions involving the orbital angular momentum of the unpaired electron. Since this momentum depends on the chemical environment the g factor also depends on this environment. In a solid the energy levels of the unpaired electrons cannot be taken as the Zeeman splitting mentioned above since the electron is coupled with many other fields from its surrounding environment in addition to the applied magnetic field.



LEGEND:
- M - MONOSILICON INTRINSIC SILICON
- M^1 - MONOSILICON SILICON (31-34 OHM CM) BORON
- T - TEXAS INSTRUMENTS (8-12 OHM CM) PHOSPHORUS
- A_1 - ANNEALED 6 HOURS AT 800C IN N_2
- A_2 - ANNEALED 96 HOURS AT 800C IN N_2
- A_3 - ANNEALED 4 HOURS AT 1150C IN N_2
- E - ETCHED IN HF + HNO_3 TO REMOVE 750 MICRONS
- W - WET OXIDE 6 HOURS AT 1150C
- D - DRY OXIDE 72-87 HOURS AT 1150C
- N - NaOH ADDED DURING OXIDE GROWTH
- H - HC1 ADDED DURING OXIDE GROWTH

Figure C-2.- EPR Sample Preparations

The equipment used in this study was an X-band Varian Model 4500-10A EPR spectrometer with 100 Kc modulation. The powdered samples about 1.5 cm in length were put in a 3 mm diameter quartz tube, and initial experiments were performed at room temperature. The maximum sample width that will fit into the microwave cavity is one cm; however, it was found necessary to use the thinner samples because of large energy losses when the silicon dioxide sample extended into the electric field in the cavity.

To induce electron spin flipping the silicon dioxide sample is simultaneously subjected to a dc magnetic field H_0 and a weak microwave field whose frequency is near the precessional frequency of the electron. A block diagram of the Varian EPR spectrometer used in this investigation is shown in Figure C-3. A Klystron oscillator provides the microwave field at 9.5 Kmc while a large electromagnet provides an H_0 of about 3400 gauss for this type sample. The EPR cavity is tuned to resonance with the microwave field with the sample in place inside the cavity. The cavity is connected to one arm of a microwave bridge, another arm of which contains a crystal detector, and the bridge is adjusted for balance in the absence of electron resonance. During spin flipping energy is absorbed from the microwave field which unbalances the bridge and is sensed by the crystal detector.

The resonance data taken in this study was recorded on either a single or a dual channel recorder with the sample temperature between -180 C and + 300 C. Use was made of a dual cavity with the second one providing a reference standard. The resonance spectra to be shown below were recorded by sweeping the field H_0 about one hundred gauss on each side of 3300 gauss keeping the microwave frequency fixed at about 9.3 GHz. The data recorded as the intensity of the resonance signal is the radio frequency magnetization $X''H$ rather than the susceptibility X'' or the power absorbed $1/2\ (\omega H^2 X'')$ due to the crystal detectors employed in the type equipment used here. These resonance absorption signals do however represent the first derivation of the energy absorbed as a function of applied dc field strength. Precise g values can be determined by measuring the microwave frequency and magnetic field strength at resonance or by comparison of the unknown signal with that of a known sample. This latter method was used in this investigation by employing a dual sample cavity.

Signal types detected. - Three basically different electron spin resonance absorption signals were recorded from the powder samples investigated on this part of the program. A fourth type was recorded from single crystal samples with aluminum deposited over the oxide and might be caused by oxygen vacancies.

The first or main type of signal was detected from all silicon and silicon dioxide powder samples. This signal has been reported by others investigating the properties of silicon alone (Ref C-5 and C-6). The silicon signal is attributed to an oxygen-vacancy pair on the surface formed by the capture of an oxygen atom (or ion). This oxygen is adsorbed in a vacancy created by the mechanical damage when the silicon is crushed into a powder.

The second signal is the one of main interest in this investigation. Both it and the first signal are shown in Figure C-4 for Sample A (TW) on which it was first detected. These signals were recorded at room temperature from silicon dioxide

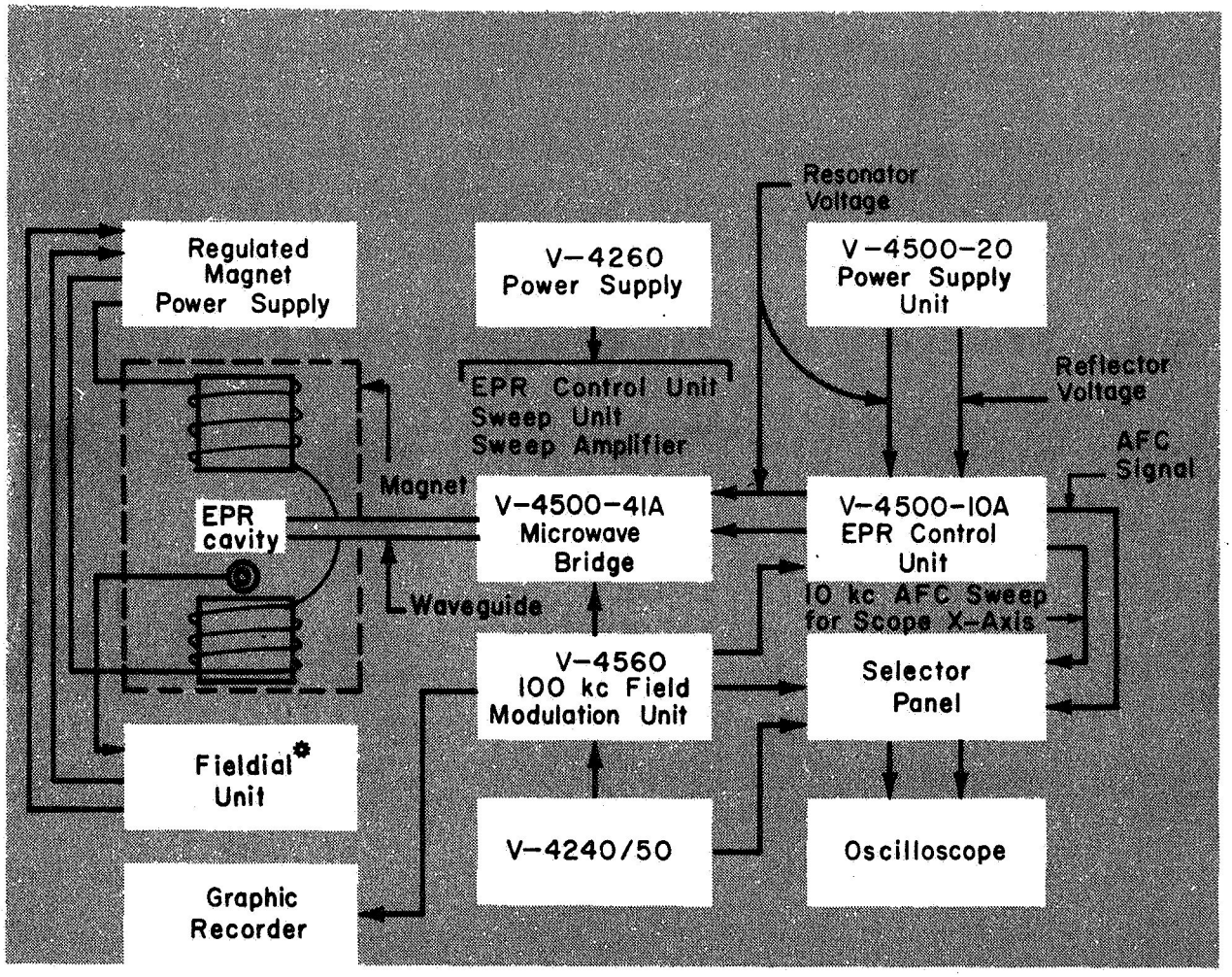


Figure C-3.- Block Diagram of the Varian V-4502 EPR Spectrometer Systems

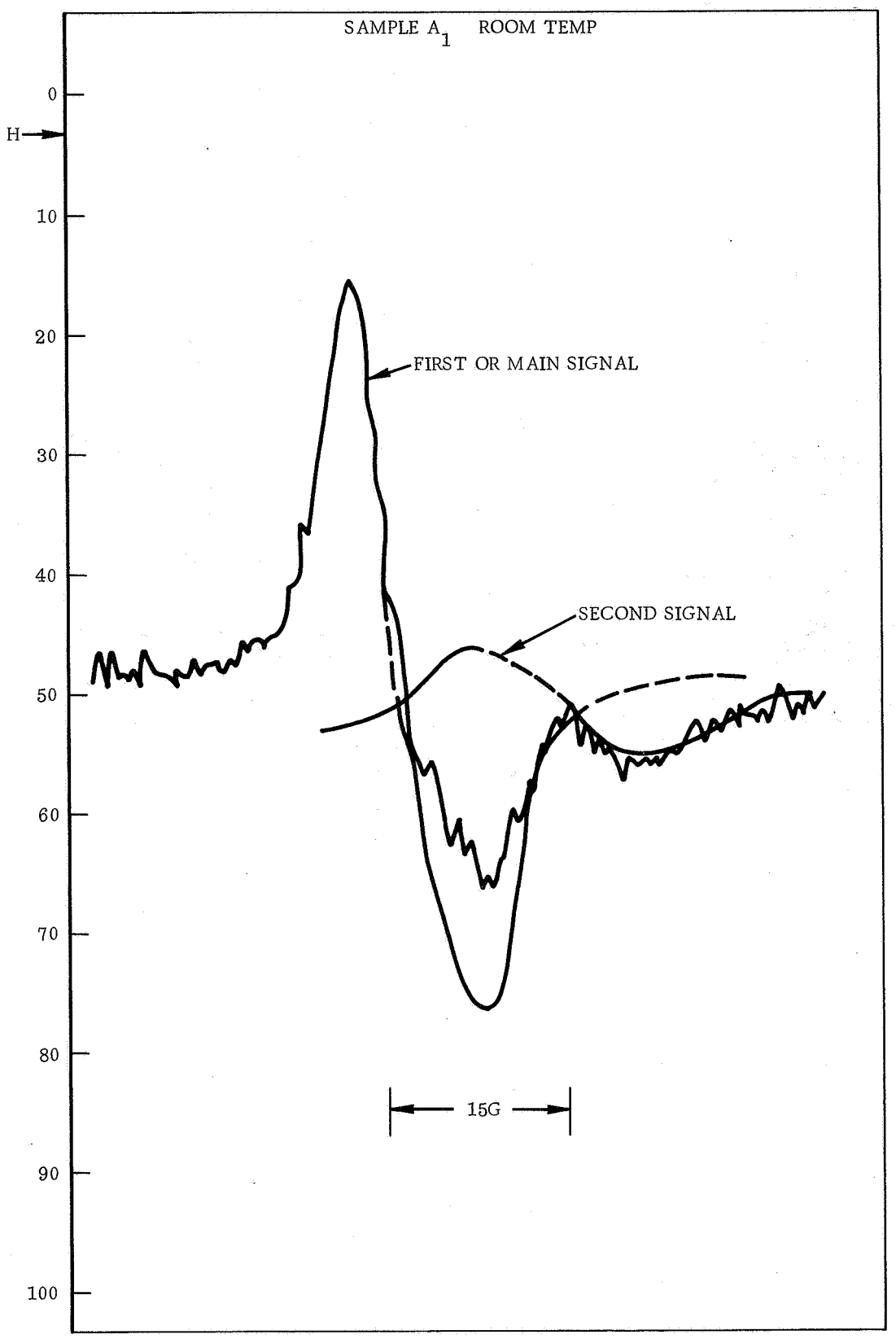


Figure C-4.- Discovery of Second Signal or Silicon Dioxide Grown Wet by Convection Method

grown wet at 1150 C to a thickness of 12,000 Å. The second signal will be discussed below in more detail. It is normally only recorded from oxide samples grown wet.

The third signal was found with silicon dioxide baked in hydrogen for one hour at 1150 C. It had been reported earlier by another investigator (Ref. C-7) performing the same type study as being done on this program. He did not detect any signal from silicon dioxide so he baked his sample in hydrogen and then found an additional resonance. This signal is not related to the second one being investigated here and will be only briefly discussed later.

Signal characteristics. - There are many factors which can affect the character of EPR signals made on the silicon dioxide samples. The impurity atoms in the unoxidized silicon for the cases of both donors and acceptors do not alter the absorption curves. After oxidation the sample has oxygen interstitials, thought to be the predominant diffusing agent during oxidation and leading to acceptor states, as well as trivalent silicon and oxygen vacancies which are considered to produce donor states. These should contribute to the character of the absorption curves, along with the electron spin interactions with neighboring nuclei and the resulting local magnetic fields that alter the symmetry and lead to hyperfine splitting. Silicon is mostly (92 percent) Si^{28}, but the Si^{29} (4.7 percent) atoms, for example, have a nuclear spin of 1/2 while Si^{28} has zero nuclear spin. Thus, even the Si^{29} unpaired electron spins can interact with their nuclei and alter the absorption curve. The unoxidized silicon samples produced a strong symmetric absorption curve of about 25 gauss full width, while the oxidized sample showed an asymmetric complex curve indicative of multiple absorptions. The large signal to noise ratio with the unoxidized sample permitted a scan of 50 gauss in 10 minutes, and showed the absorption derivative curve was symmetric and without hyperfine splitting. The detected resonance absorption with the first oxidized sample was at the lower limits of detection of the equipment. Figure C-5 is the resonance absorption curve for a wet oxide sample, which more clearly shows both the first and second signals at room temperature.

The thermally grown silicon dioxide on powdered silicon produced a multiple absorption curve in contrast to the single symmetric absorption curve obtained from bare silicon. To factor out any effect of the dopant (mainly phosphorus) in initial silicon samples, intrinsic silicon was then used. The absorption curves with intrinsic silicon were found to be nearly identical with the earlier 8-12 ohm-cm n-type samples. Thus the main absorption mechanism observed in both cases appears to be associated with surface damage in the silicon caused by the pulverizing of the single crystal wafers. This was also verified on the oxide samples by using HF to remove the oxide from one sample and comparing its absorption intensity with a bare sample. The use of powder samples was found to be necessary to provide enough surface area for detectable energy absorption.

As noted above, it is thought that the main absorption curve is caused by oxygen-vacancy pairs produced at vacancy defects by pulverizing the silicon. A 100 cm^2 surface area of silicon contains about 10^{17} atom sites with the surface mostly (111), the main cleavage plane for silicon. This main absorption curve is reported to disappear if at least 10^{-4} cm of the silicon surface is removed by HF plus HNO_3 but is

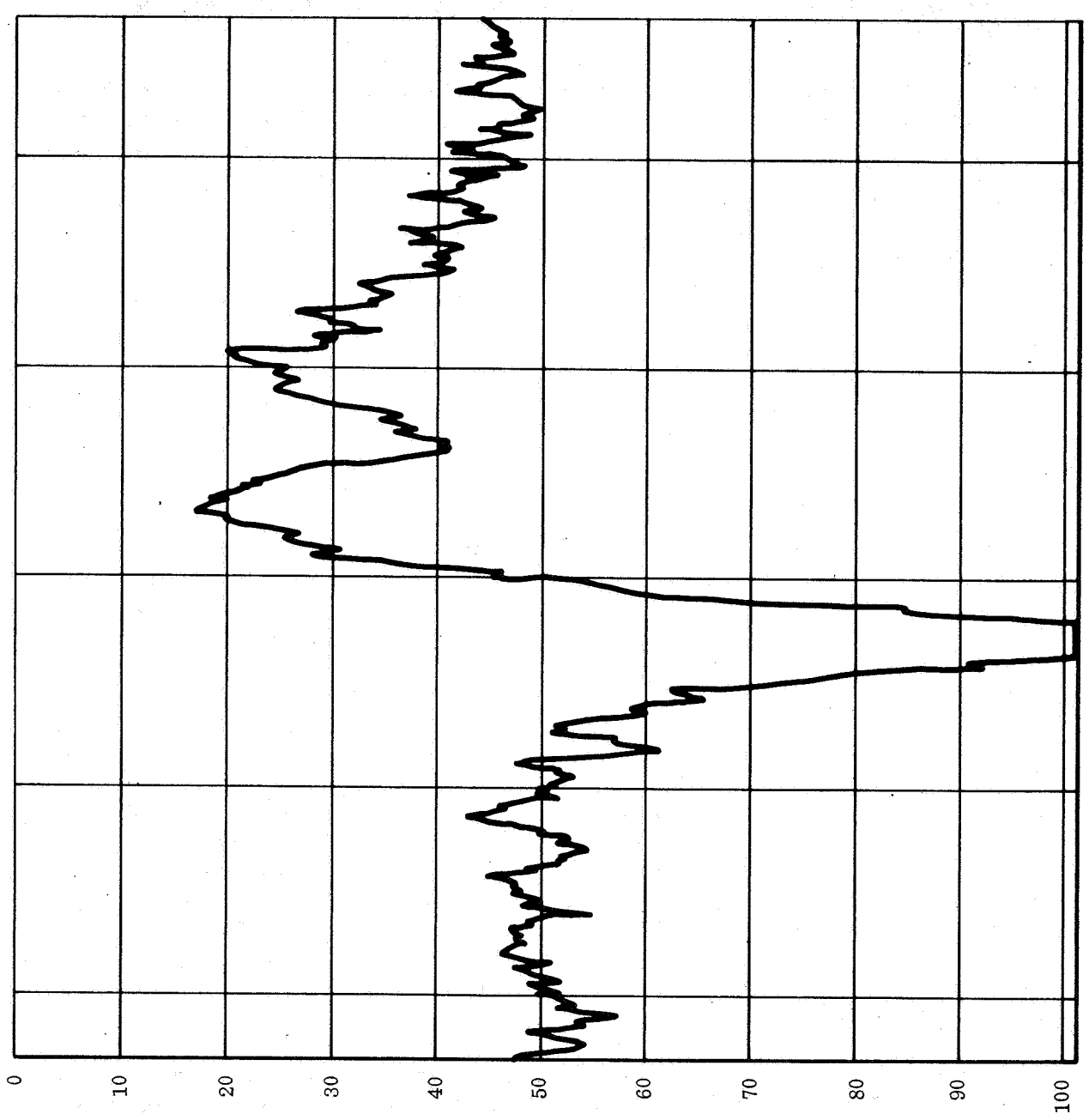


Figure C-5. - Sample A Showing Second Signal at 20 C

not removed by treatment with concentrated HF, HNO_3, or HCl acting alone (Ref C-8). Thus the main absorption appears to be associated with the silicon and the silicon surface which has an estimated ratio of ruptured bonds to surface atoms of 1:5 in these samples. The reduction in intensity of this main signal after oxidation may be caused by annealing effects during the high temperature oxidation process.

A large number of samples with various surface preparations were made in this study to investigate several phenomena reported in the literature. Two of these are the removal of surface damage by etching and the atomic surface reconstruction produced by annealing (Ref C-9). As mentioned above, a removal of more than one micron of silicon surface causes the EPR signal due to silicon surface damage in the powder samples to disappear. Samples ME and MEA had 750 microns of silicon removed from the surface, and yet a relatively strong symmetrical absorption was still present. This signal is still observed, along with the second signal, after growth of an oxide on these samples. It should be noted that the EPR spectrometer used here is one of the best available and has close to the theoretical detection limit of about 3×10^{11} ΔH spins per gauss where ΔH is the signal width. The second phenomenon on the effects of annealing was difficult to determine because of some very broad (1-2 Kg) drift lines recorded from the annealed samples which obscured any detailed line structure.

Figure C-6 shows the second signal (shifted to the left of the main signal) of sample MA_1W (Monosilicon intrinsic, Annealed 6 hours in N_2 at 800 C, and a Wet oxide grown) taken at -160 C that still has a relatively large second signal intensity after annealing. Figure C-7 shows the second signal being brought out on sample MA_1EW at -150 C, which indicates how it could be overlooked at low gains while taking this type of data. Figure C-8 shows the second signal on two other samples that were etched prior to oxidation in a and annealed after etch in b.

Two samples, TW and M, were subjected to heat treatment in dry nitrogen during EPR scanning to seek any changes in the absorption curves. Data were recorded from 0 C to 300 C in 50 C steps. No qualitative change in the shape or character of the curves was noted. The effect of heat treatment on silicon has been shown by low energy electron diffraction experiments to cause a surface rearrangement of silicon atoms (Ref. C-10). Several surface models have been postulated on the basis of these experiments. It is of interest to note that upon admitting oxygen during the low energy electron diffraction study at elevated temperatures the pattern shifted to show that the silicon atoms arranged themselves back to the diamond configuration of the bulk crystal. After a few hundred Angstroms of oxide form on the silicon the diffraction patterns disappear.

To more fully study the second signal of the oxides grown wet a temperature controller and a dual cavity were employed. The temperature of the oxide sample could be varied from -180 C to +300 C while continuously scanning. A reference sample of either pitch in KCl or DPPH was used in the reference cavity which remained at room temperature.

Samples A (TW) and MEA_1W were cooled to -180 C to improve the absorption signal intensity and help in resolving the second peak. A rather unusual and interesting phenomenon was observed as the samples cooled, namely, the second peak appeared to shift position with respect to the main peak. This shift of about 30 gauss is shown for sample A in Figures C-9 and C-10. The physical origin of this second

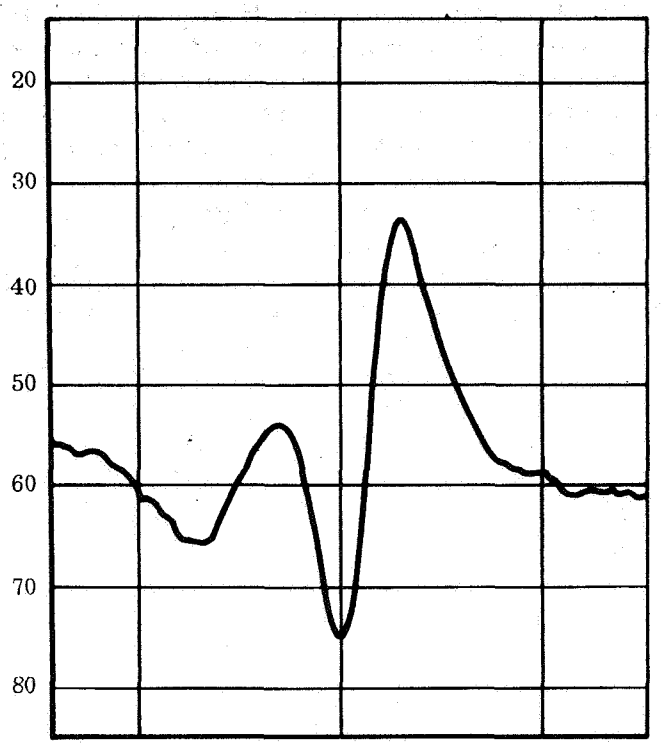


Figure C-6.- Sample MA_1W at -160 C

peak and the temperature dependent shift mechanism were considered with known interactions which affect the g values. There are two types of magnetic dipole interactions that might be considered here since silicon is about 5 percent Si^{29}, which has a nuclear spin I = 1/2. One is called the anisotropic dipolar hyperfine interaction caused by the ordinary coupling of the electron magnetic moment with the nuclear magnetic moment. The other is the Fermi contact, or isotropic hyperfine interaction, arising from the relativistic treatment necessary when the electron motion is near the nucleus, causing a very large kinetic energy increase. This again couples the dipoles and shifts the energy levels. The second signal does not appear to be due to the dipolar hyperfine interaction since this usually produces two separate peaks about the main one, nor is it characteristic of the signals reported in the literature for silicon surface damage or surface reconstruction due to heat treatment of the silicon. Since it has been observed only with the SiO_2 samples and for both the phosphorus doped and intrinsic silicon, it definitely appeared to be a signal originating from the oxide. It is possible that one of the signals is broadened with the temperature variation and only appears to shift.

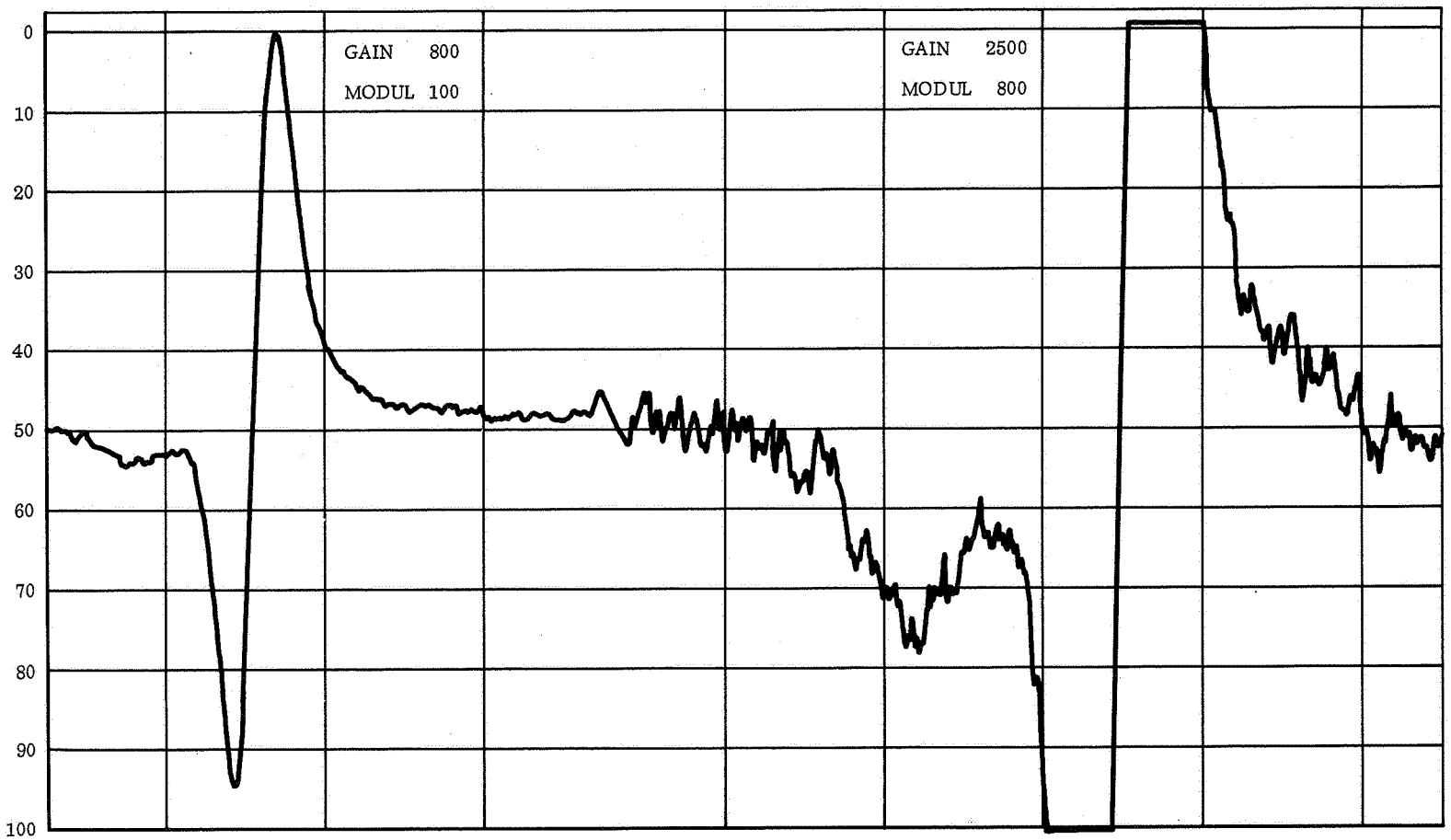
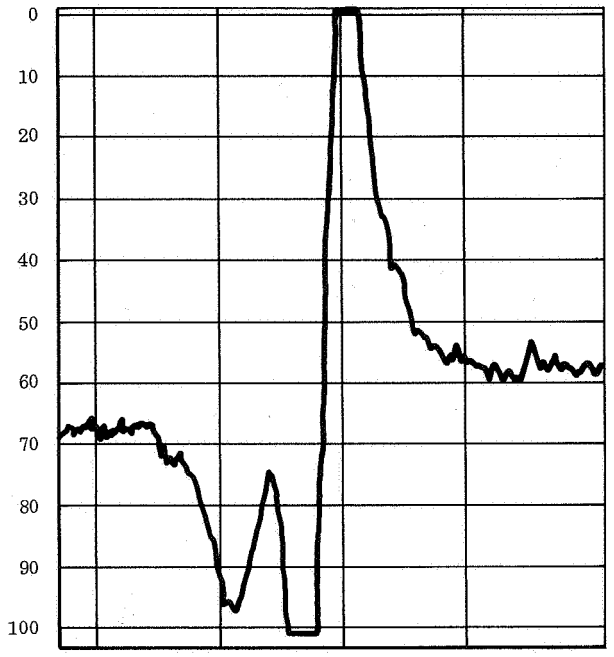
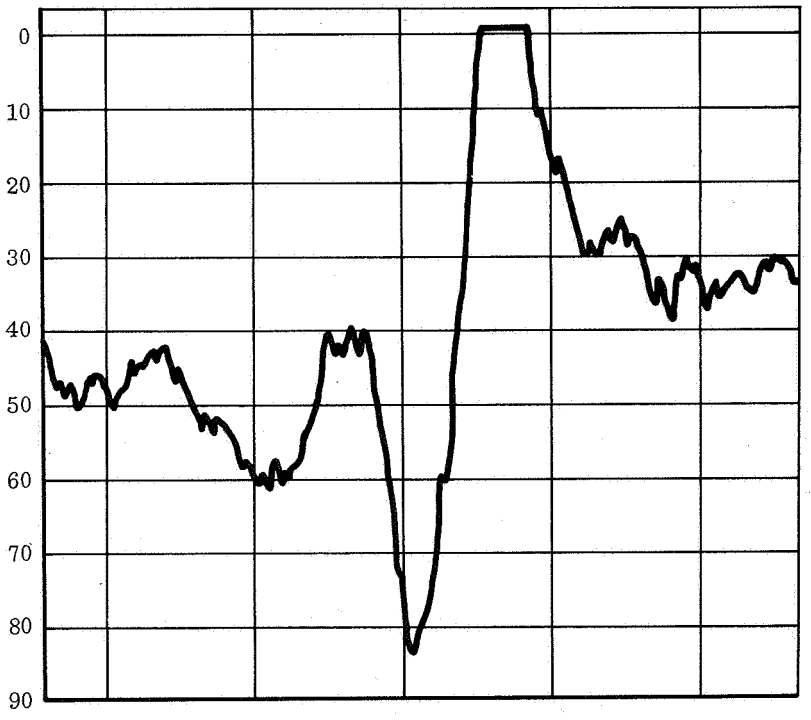


Figure C-7.- Sample MA_1EW at -150 C Showing How Second Signal Is Brought Out by Increased Gain

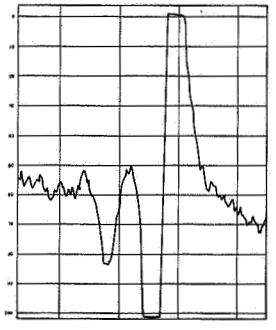


a. Sample MEW

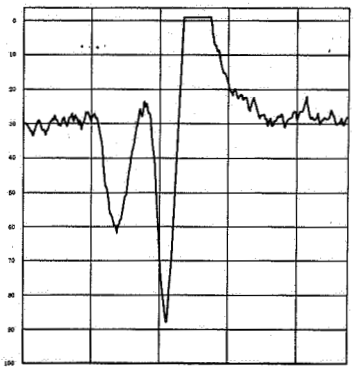


b. Sample MEA_1W

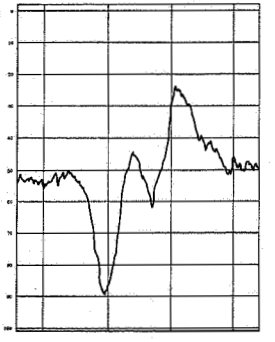
Figure C-8. - Second Signal at -160 C



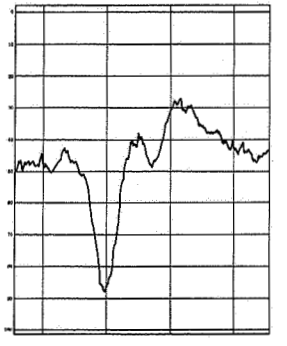
-164 C



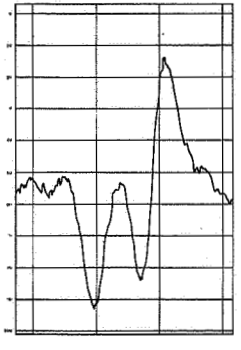
-125 C



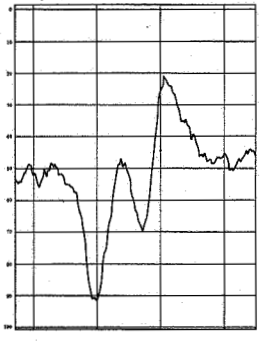
-50 C



-30 C

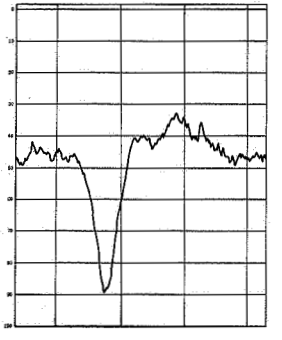


-90 C

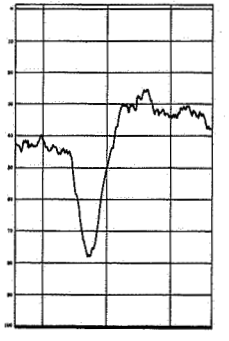


-70 C

Figure C-9.- Sample A Going From
-164 C to -70 C



-10 C



+40 C

Figure C-10.- Sample A Going From
-50 C to + 40 C

Line shape and spin concentrations. - Another factor in analyzing resonance spectra is the line shape. The shape of the absorption curve is influenced by many internal interactions that the unpaired electrons undergo and lead to two classes of lines. One class is called homogeneously broadened which arises when all the electron spins have the same local environment. The second class is called inhomogeneously broadened and refers to electron spins interfacing through a variety of different environments, such as local impurities and defect centers. In EPR of solids most powdered materials exhibit inhomogeneous broadening depending on the anisotropies of the spin interactions. Two approximate line shape equations are the Lorentzian and Gaussian:

$$I = \frac{I_o}{T^2 (H - H_o)^2 + 1} \qquad \text{(Lorentzian)}$$

$$I = I_o e^{-b (H - H_o)^2 T^2} \qquad \text{(Gaussian)}$$

where I_o is the intensity of the absorption line at its center, H_o is the magnetic field intensity at the center of resonance, and b and T are constants related to half-widths of the two type curves. By differentiating these equations the maxima are found and the experimental data normalized for comparison. Figure C-11 shows the plots of theoretical position (TP) on the curve versus the experiment position (EP) for a sample of intrinsic powdered silicon. If a straight line results for a given absorption spectrum, then the absorption is either Lorentzian or Gaussian. As can be seen, the line shape in this case is Lorentzian, and lines having this shape are usually homogeneously broadened. Similar calculations on data for oxidized samples did not produce a straight line for either plot. Physically, the Lorentz shape arises in a manner similar to a harmonically bound electron which, during the emission of radiation, is randomly and rapidly perturbed in its motion, producing a Lorentzian distribution of frequencies. In EPR measurements this perturbation can occur through the exchange of equivalent electrons between different paramagnetic silicon atoms when the electron wave functions overlap. For the sample here this would obviously lead to the case of homogeneous broadening. The Gaussian line shape will arise when each paramagnetic electron sees a slightly different internal magnetic field from neighboring nuclei or electrons. An example of this would be a substitutional impurity producing a variation of the total field the electron sees during the spin flip process. There is no reason to expect that the SiO_2 samples should produce a Gaussian line shape since in general the data from complex systems such as this rarely fit either line shape.

It is possible to measure the number of unpaired electron spins for a given absorption signal by comparing it to the signal of a known standard. This has been done only on a silicon sample using its signal. A standard sample of 0.1 percent pitch in KCl was used in the reference side of the dual cavity and the dual data recorded. The standard has 3×10^{15} electron spins per centimeter of length. The

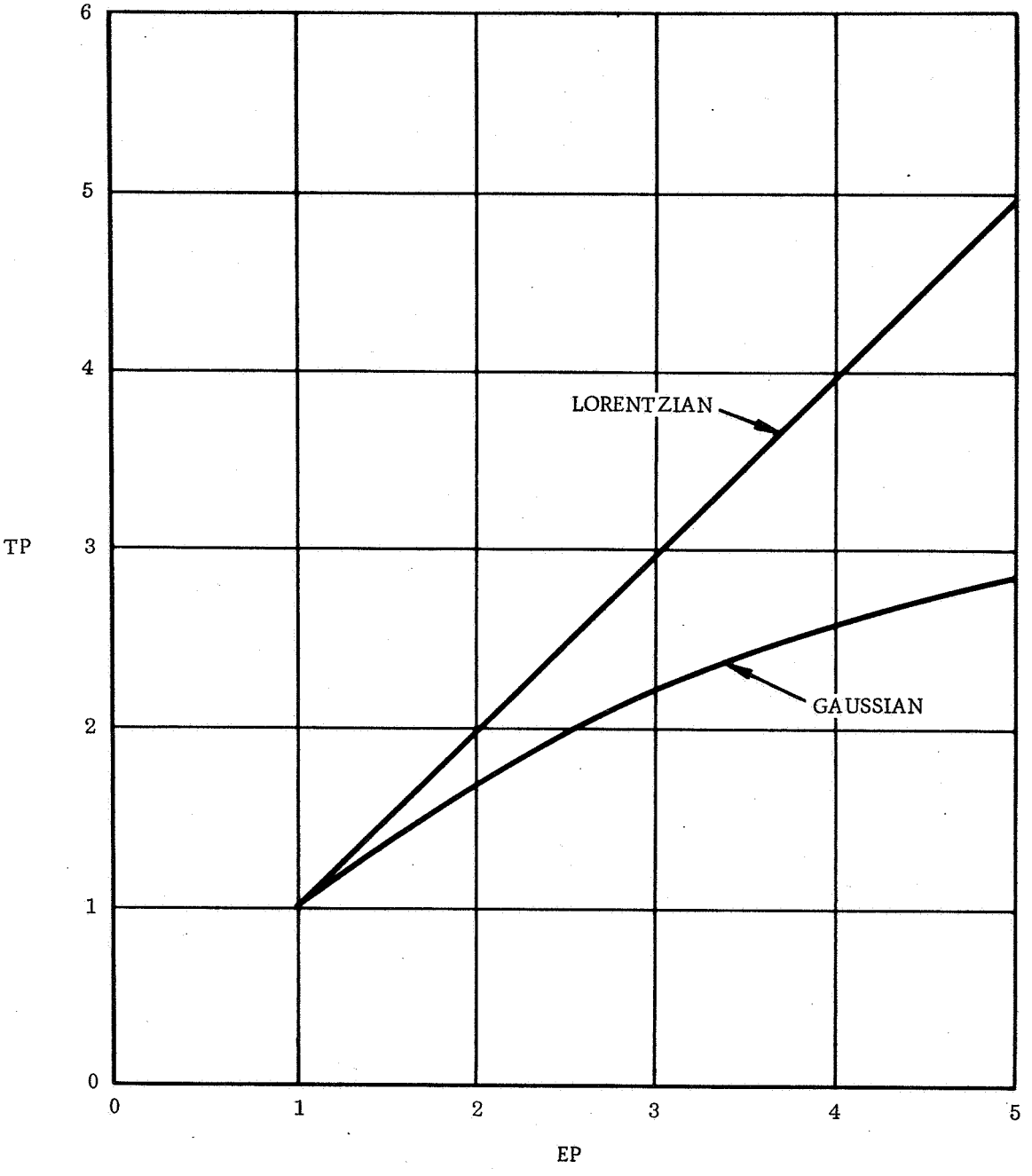


Figure C-11.- Line Shape Calculations

two samples were scanned then interchanged and scanned again. Using the observed gain settings and the measured first moments of the absorption derivative curves the spin concentration of the silicon was calculated to be 3.3×10^{14} spins per cm or a total of 8.4×10^{14} spins with an estimated accuracy ±25 percent. This information provides a qualitative comparison os spin concentration for the silicon dioxide samples where it is not possible to measure their moments because signal one and signal two overlap each other.

Treated oxides. - As the large number of articles in the literature indicate, there are many effects such as ambient (Ref C-11), thermal (Ref C-12), chemical and oxide growth parameters which can cause changes in the electrical characteristics of silicon devices passivated with silicon dioxide. Most of these are associated with either oxide states, interface states or oxide defects acting as trapping sites. To gain more experimental data on the oxide samples and the second signal studied here, a number of them were treated with chemical contamination. The first samples to be treated were those in which the silicon powder was contaminated with HF, NaOH and NaCl prior to oxidation. The second signal was found to have increased in size with these contaminated samples.

It appears from the data that both HF and NaCl contamination produce a larger second signal which exhibits the same thermally activated g value shift or line broadening. Bare silicon contaminated with NaCl or HF gave resonance signals with quite a bit of drift and it was not possible to ascertain the presence of a second signal from them. Information relevant to these samples and the resulting EPR data is given in Table C-3 where the notation (MW+HF) means the oxide was grown wet on type M silicon and then HF was added directly to the sample for temperature and time shown. The symbol (M^1+NaCl) W means silicon type M^1 was soaked in NaCl and the oxide then grown wet on the contaminated oxide.

From the data it was found that silicon contaminated with NaCl and silicon dioxide contaminated with HF gave an increased second signal. This increased second signal is shown in Figure C-12 for sample (M^1 + NaCl) W.*

This sample was prepared by soaking 32 ohm cm powdered silicon in a 10 percent solution of NaCl. After the solution had dried the sample was placed inside the oxidation furnace at 1150 C and a wet oxide grown for 8 hours. EPR data recorded at various temperatures between -184 C to 300 C showed a marked decrease in the signal quality above 0 C.

The scan for -120 C was run in the single cavity while the others were taken with the dual cavity during the same run using pitch in KCl for a reference. The noise is large from the reference cavity because of the low frequency modulation of 200 cps used on it.

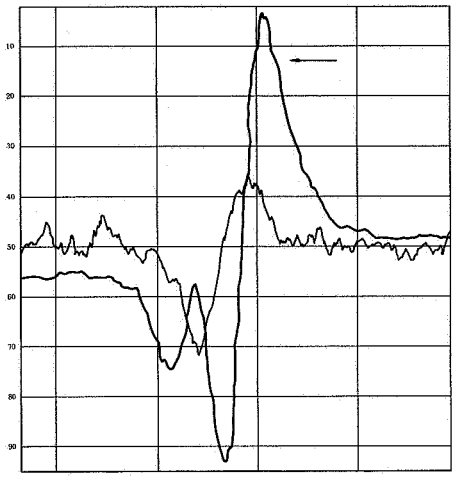
*(Note that dual cavity data was taken in red and blue ink. The oxide sample is identified in the figures here by the arrow.)

TABLE C-3
EPR SAMPLE DATA AND RESULTS

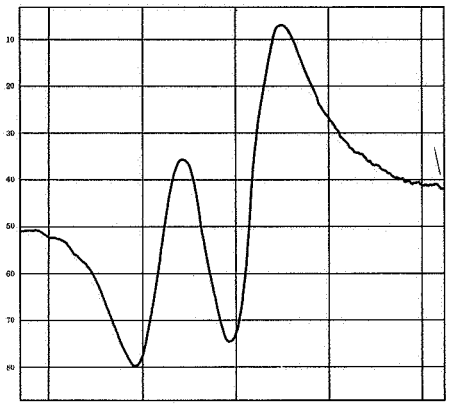
Sample Preparation	Oxidation Period	Oxidation Temperature	Contam-ination Period	Contam-ination Temperature	Type of Silicon ohm-cm	Signal Data (See Key)
(M+HF) W	8 hr	1150 C	-	-	Intrinsic	2M
(MW+H_2)	8 hr	1150 C	1 hr	1150 C	Intrinsic	2M, 3M
(MW)	8 hr	1150 C	-	-	Intrinsic	2M
(MW+HF)	6 hr	1150 C	6 hr	40 C	Intrinsic	WS
(MW+NaCl)	6 hr	1150 C	6 hr	40 C	Intrinsic	WS
(M+HF+ NaCl)	-	-	6 hr	40 C	Intrinsic	WS
(MW+HF) W	6 hr	1150 C	-	-	Intrinsic	N2
(MEW)	6 hr	1150 C	-	-	Intrinsic	2S
(MEA_1W)	6 hr	1150 C	-	-	Intrinsic	2S
(MA_1W)	6 hr	1150 C	-	-	Intrinsic	2S
(MD)	87 hr	1150 C	-	-	Intrinsic	N2
(MED)	87 hr	1150 C	-	-	Intrinsic	N2
(M^1W+D*)	6 hr	1150 C	-	-	p 32	ND
(M^1W+HF)	6 hr	1150 C	1 hr	1200 C	p 32	2L
(M^1+NaCl) W	8 hr	1200 C	-	-	p 32	2L
(M^1+NaCl) D	90 hr	1200 C	-	-	p 32	2S
(M^1W+NaCl)	6 hr	1150 C	10 min	1200 C	p 32	ND
(TW)	6 hr	1150 C	-	-	n 10	2S
(TD)	87 hr	1150 C	-	-	n 10	N2
T (HC1+W)	7 hr	1150 C	-	-	n 10	WS
(T+NaOH) W	6 hr	1150 C	-	-	n 10	2M
(TW+A*)	6 hr	1150 C			n 10	N2

Key

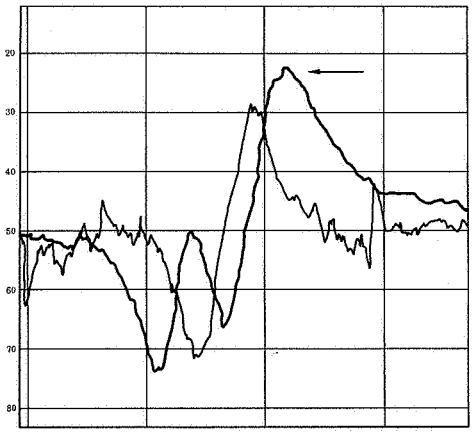
2S - 2nd Signal small
2M - 2nd Signal medium
2L - 2nd Signal large
3M - 3rd Signal medium
WS - Wavy data, inconclusive
N2 - No, 2nd Signal
ND - 2nd Signal not detected
D* - Dry growth 2 hr, 1150 C
A* - Anneal (N_2), 2 hr, 1150 C
E - Etched silicon
A_1 - Annealed (N_2) 6 hr, 800 C



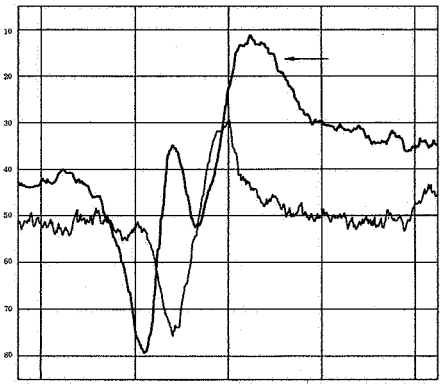
-120 C



-150 C

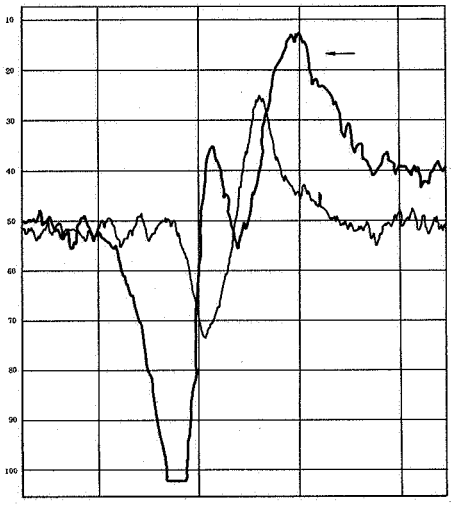


-20 C

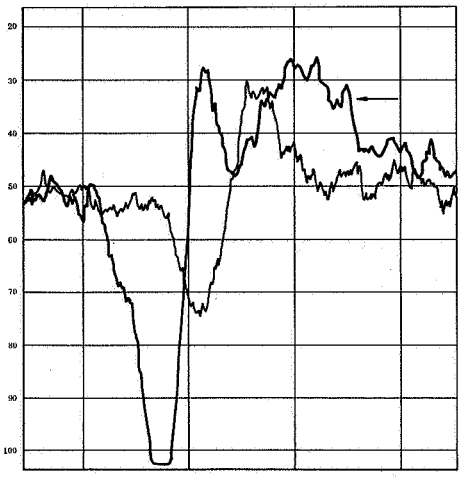


+10 C

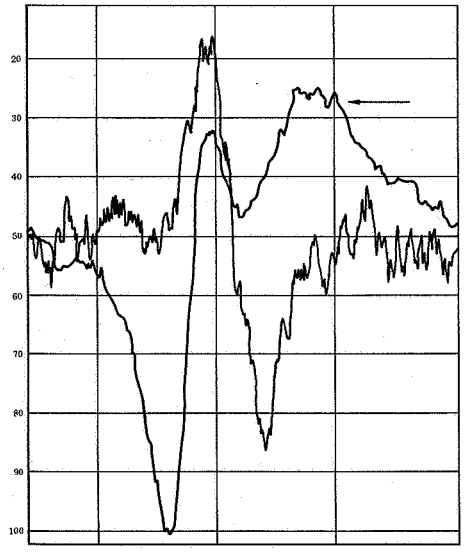
Figure C-12. - Resonance Spectra of Silicon Dioxide Sample (M^1 + NaCl) W at Temperatures Between - 180 C and +100 C



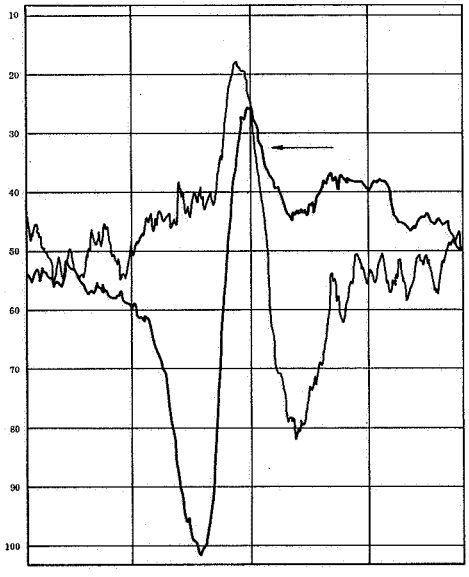
+30 C



+50 C



+60 C



+100 C

Figure C-12.- (Concluded)

From the data taken on sample (M^1 + NaCl) W, it is seen that going from -150 C to -80 C produces little change in the position of the two signals. At temperatures above 0 C it is more difficult to interpret the data because of decreased sensitivity. Sample (T+NaOH) W produced the same type second signal at -180 C as (M^1+NaCl) W as shown in Figure C-13, indicating that sodium deserves serious consideration in determining the chemical structure of these oxides. An oxide structure with sodium ions bonded to trivalent silicon atoms near the silicon-silicon dioxide interface has been recently proposed from data on MOS capacitance experiments and is among those being studied for correlation with these EPR results (Ref C-13). It appears that the second signal doesn't shift much until the temperature is near 0 C and then it shifts rapidly above 0 C and perhaps broadens out above 40 C.

To compare effects of contamination after oxide growth several samples shown in Table C-3 were contaminated with NaCl at both 1150 C and 40 C after oxidation and EPR runs made with them. The recorded signals were all very poor in that much drift and wavy patterns were found. It is not yet possible to conclude that the second signal is present on these samples even though a peak was usually found where it would be expected, along with many other nearby peaks. This is in contrast to contamination with HF. Samples contaminated with HF were made by either soaking the silicon prior to oxidation in a 0.5 percent solution of HF, followed by drying at 180 C, or by soaking a silicon dioxide sample in a 0.5 percent HF solution before insertion into the furnace at 1150 C or 40 C. The data were different from those with NaCl contamination above in that the strongest second signals were found with silicon dioxide soaked in HF. Figure C-14 shows the large second signal recorded on (M^1W+HF) at -180 C.

Figure C-15 shows a small second signal present for sample (M^1+NaCl) which is unique in that no second signal had ever been found with an oxide grown dry. This signal appears in the same location as the second signal on wet oxide samples and also changes shape with temperature.

With the experimental data recorded here it is still very difficult to postulate the identity or origin of the second signal because many substances have g values near this one and the physical system under consideration is quite complex. Even silicon-silicon surfaces without any heat treatment are not well understood. However, it appears that the second signal is related to the presence of sodium in the oxide for those samples contaminated with NaCl or NaOH prior to oxidation. The effect of baking in hydrogen, annealing in an inert ambient such as nitrogen and growing a dry oxide is to reduce the intensity of this second signal. For those oxides contaminated with HF it is possible that the HF reacts with bare silicon, either by etching through the oxide, or by acting on bare silicon caused by incomplete oxidation at points where the silicon particles were in contact with each other during oxide growth.

Additional EPR data were taken on samples (M^1W + HF), (M^1 + NaCl) and (TW). Of particular interest are the results on sample (M^1W + HF) under atmospheric and reduced pressures shown in Figure C-16. It is evident from the figure that outgassing of the HF treated sample (at 4 x 10^{-2} Torr) produces a significant reduction in the second signal. The second signals of the other two samples, however, were unresponsive to outgassing. The evidence appears to implicate the HF + Si system as a source

Figure C-13.- Sample (T + NaOH) W at -180 C

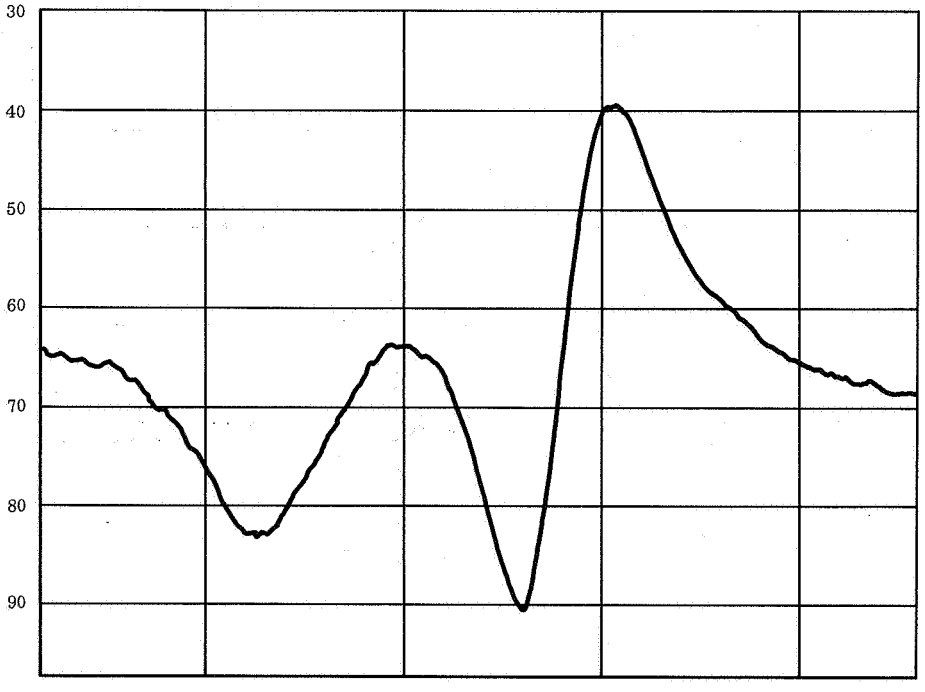


Figure C-14.- Sample (M^1W + HF) at T = -180 C

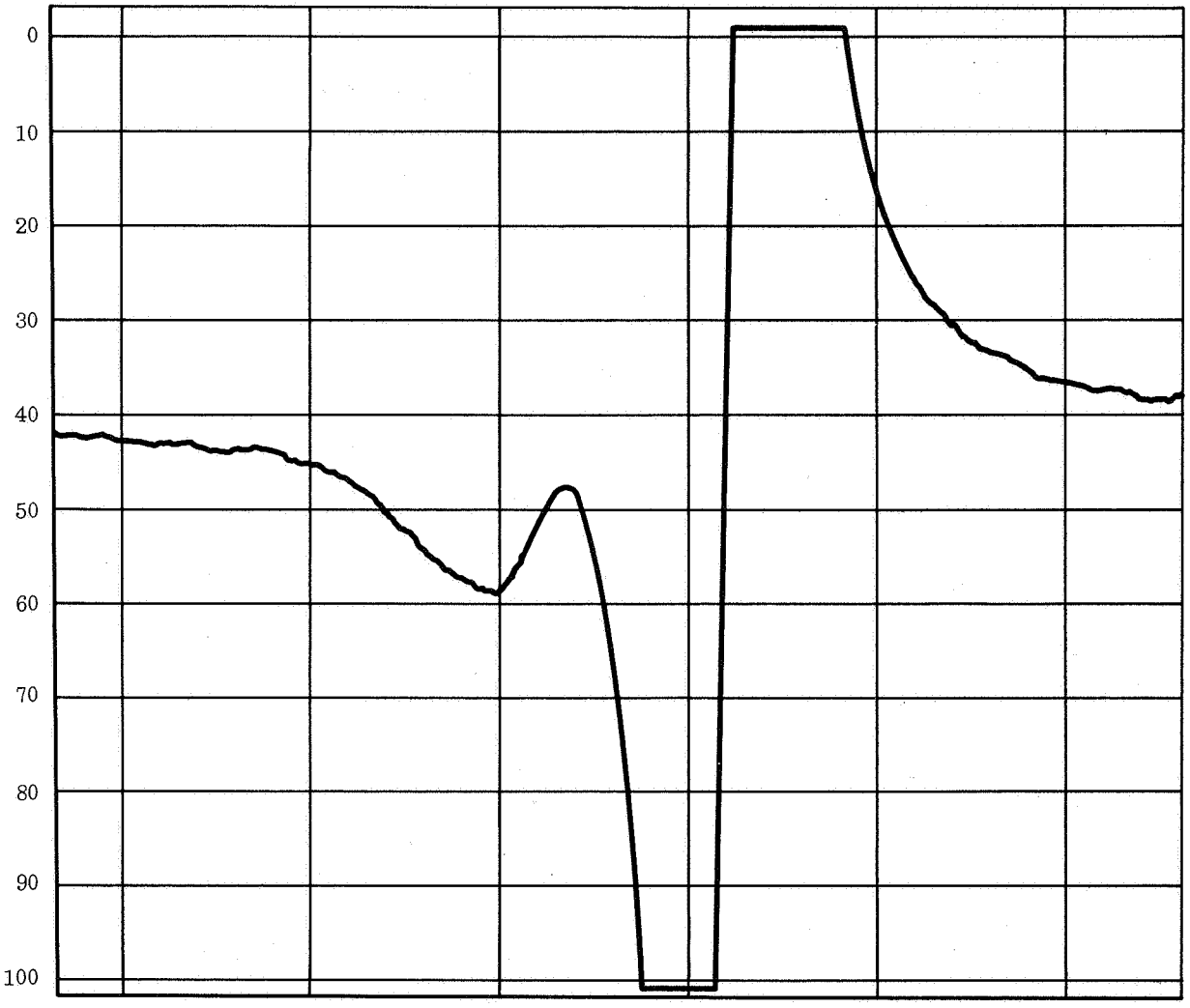
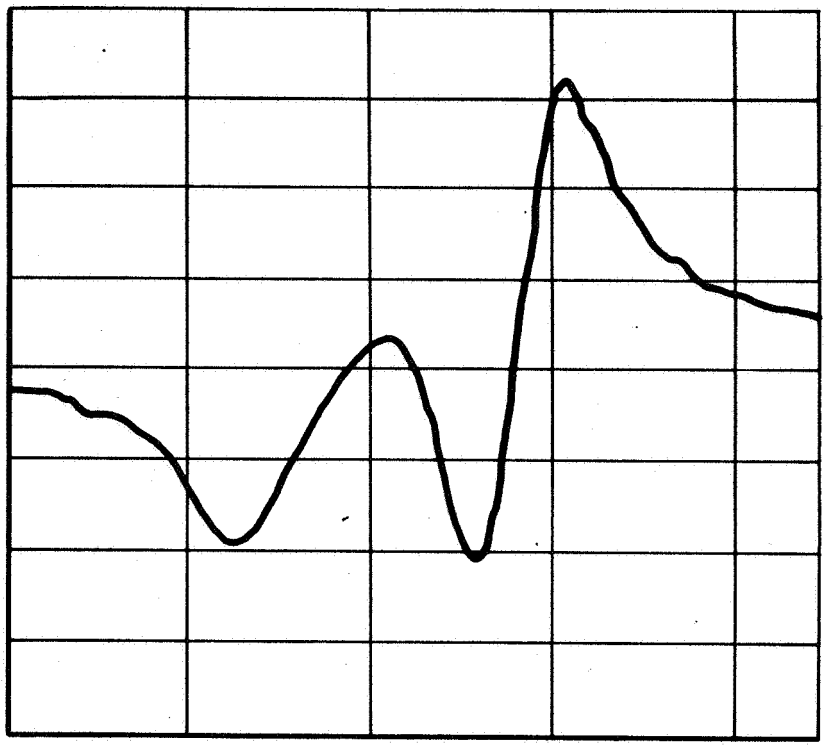
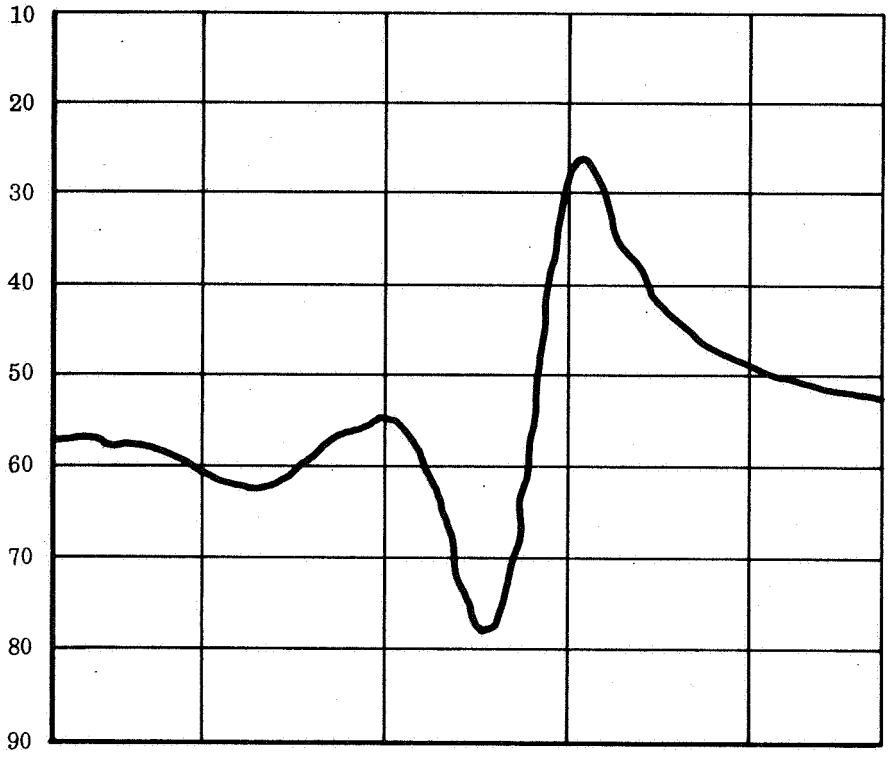


Figure C-15. - Small Second Signal at -180 C Detected From Oxide Grown Dry on Silicon That Had Been Contaminated With NaCl



a. Room Pressure



b. On Vacuum of 10^{-2} Torr

Figure C-16.- Second Signal of Oxide Treated by HF Shown at -180 C Under Room Ambient and Then Under Small Vacuum

of the second signal. It is known, for example, that SiF_4 (formed in the present experiment by HF + SiO_2) interacts with silicon at elevated temperatures to produce the biradical Si_2F_4 containing unfilled silicon orbitals. However, the reverse of this reaction at still higher temperatures should result in release of SiF_4 and deposition of "atomic" or finely divided silicon. This possibility fits well with the experimental conditions employed because the specimen (M^1W + HF) was baked for ten minutes at 1150 C in an inert atmosphere after treatment with 0.5 percent HF solution. The residual finely divided silicon then could act as adsorption sites for condensable gases during EPR Spectrometry. This also is a real possibility because the EPR Spectra were taken at -185 C, and the second signal reappeared on admission of room air to the outgassed sample. Although the possibility of residual contamination by fluorinated species cannot be ruled out, the reversibility of outgassing effects on the EPR signal appears to be associated with the sorption of atmospheric components on surfaces rendered sensitive by the HF treatment.

The implications of this finding with respect to integrated circuit processing may be significant because of the extensive utilization of pattern etching with HF followed by diffusions or other high temperature treatments. If the EPR second signal can be associated with positively charged atomic vacancies the present evidence indicates that HF may play a role in causing inversion and that steps should be introduced to remove it after it has served its function.

The independent main signal on silicon powder has been shown (Ref C-14) to be somewhat sensitive to various ambients and pressures, possibly as a result of residual surface damage. The lack of main signal change may be due to intact oxide passivation or to prior removal of surface damage by etching. According to earlier evidence it is highly unlikely that this main signal is associated with defects in the oxide structure.

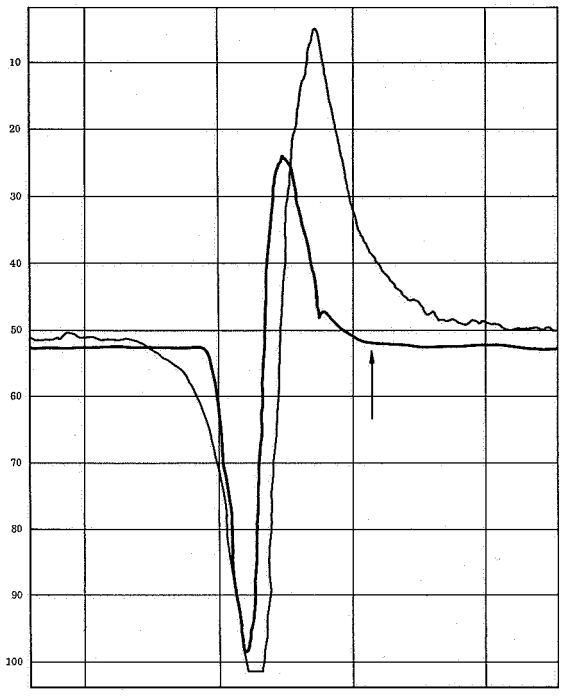
Oxides baked in hydrogen. - Only one other investigator has reported a study of silicon dioxide by EPR (Ref C-7). Silicon powder was made from p-type float zone silicon with a specific resistivity of more than 500 ohm cm. No signals other than the main one were found on these samples after they had been oxidized for two hours at 1200 C in dry oxygen. The samples were then baked in hydrogen at 1000 C for 10 minutes and a new signal found at liquid nitrogen temperature. This second signal disappears if the sample is annealed at 1200 C in dry oxygen after the hydrogen bake. It was postulated from a defect model by Revesz (Ref C-4) that the hydrogen at high temperature causes the formation of broken oxygen bridges and trivalent silicon with resulting unpaired electrons. This new signal found by Nishi is not one of those found during our investigation except that we were able to reproduce his signal by baking sample MW in hydrogen for one hour at 1150 C. Nishi's failure to find signals relatable to the silicon dioxide is due to several reasons. His oxide was only 2000 Å thick, it was grown dry on float zone silicon and the oxide area was small because of the large silicon particles used. The signal found with sample (MW + H) here, referred to as the third signal, did not show any temperature dependence. Since it has a lower g value than the main signal, while the second signal studied here has a higher g value, this third signal has not been pursured further. Many factors associated with heat treatments are possible in silicon-silicon dioxide samples that receive heat treatments (Ref C-15).

It is also of interest to note that Balk at IBM (Ref C-16) is reported to have performed EPR experiments on thermally-grown silicon dioxide with the results that a signal was found only when the final preparatory step did not include a hydrogen-containing species. This is opposite to the results of this study since only the wet oxides show additional spectra.

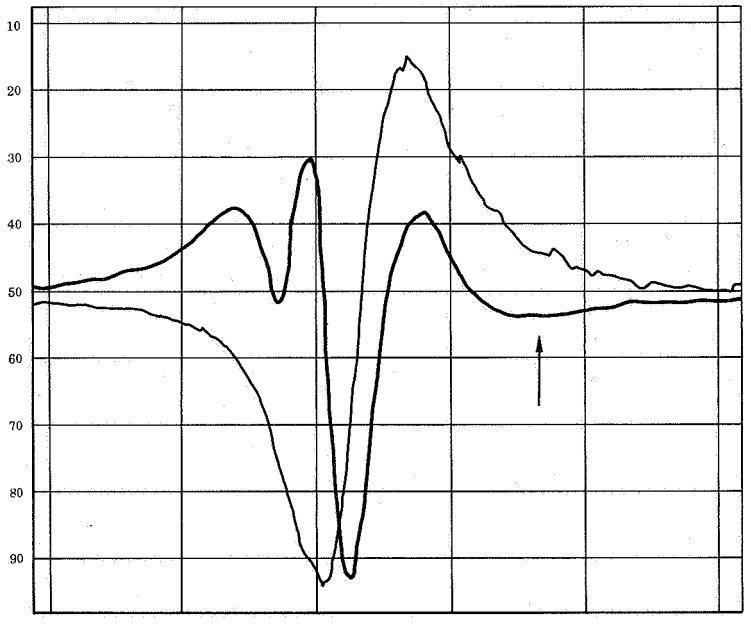
Metallized oxides. - Several silicon dioxide samples have been grown on single crystal silicon and then metallized with aluminum dots to measure possible oxygen vacancy generation as proposed by Burkhardt (Ref C-17). EPR data taken on these samples has produced a very strong single signal. This signal is not thought to be from the aluminum itself since it will be paramagnetic only if ferromagnetic impurities are present in the aluminum. It does appear likely that this absorption peak may be a result of unfilled atomic orbitals arising from competition between aluminum and silicon for oxygen atoms originally linked only to silicon atoms.

Burkhardt's experiments on the dielectric relaxation of silicon dioxide led him to rule out sodium ions as a source of oxide instability and to postulate an oxygen vacancy generation mechanism based on a reaction of deposited metal with the silicon dioxide. To explore this possibility by EPR several samples of 800 Å oxide grown on single crystal silicon (10 ohm-cm, n type) with aluminum dots deposited on them by E-beam evaporation were prepared. The wafers were scribed into strips one in. long and 3 mm wide. Although the sample area was small (2.5 cm x 0.15 cm) the absorption signal was much larger than any recorded previously, including those of bare silicon powder with its much larger surface area. Silicon dioxide samples grown on single crystal silicon without aluminum have previously produced no signal even at high gains. This sample, (TW + Al), was only run at room temperature and produced only the single signal.

It has been reported (Ref C-18) that no resonance signals are obtained from aluminum between 4K and 300K unless ferromagnetic impurities are present. The aluminum used here was 99.999 percent and had been analyzed by emission spectrography, showing copper, iron and magnesium present in levels between 0.001 - 0.0001 percent. For the iron this represents about 10^{16} spins per cm^3. On a total volume basis the aluminum present in this sample was calculated to have about 3×10^{11} spins which is too small to produce a detectable absorportion signal with the available equipment. It appears, therefore, that the present signal is derived solely from an interaction between the aluminum deposit and the oxide surface, in substantial agreement with Burkhardt's model. The g value of this single signal has been calculated using the dual cavity and found to be 2.0023 ± 0.0004 at -180 C. It does not appear to be temperature dependent. To check for possible trace impurities these samples where analyzed with the electron microprobe. No elements above atomic number four other than aluminum were found on the oxide. Two of these samples were etched in HCl and then tested. These gave a multiple signal at zero C while only showing a single one at -180 C as shown in Figure C-17. This effect was reversible. Electron microprobe analysis of these two samples revealed carbon and chlorine around the residual aluminum dots. The origin of this carbon contamination of more than 2 percent by weight is unknown and has not been pursued further.



a. T = -180 C



b. T = -50 C

Figure C-17. - Spectra of Single Crystal Silicon With the Aluminum on Oxide Partially Dissolved by HC1.

Summary

From the data taken on many oxide samples in this study it appears that sodium and fluorine can be retained in the thermally grown oxides in relatively large amounts. Figure C-18 shows the possible defect structures that can exist in the silicon dioxide samples studied here. Table C-4 presents a summary of the signal types detected.

Attempts have been made to determine g values for these signals by comparison with either pitch in KCl or DPPH. The main obstacle to this has been the partial overlap of the second signal with the main one due to the silicon. It appears from the data taken with the dual cavity and plots of ΔH vs g that the second signal has a g value of 2.011 ± 0.001 at -180C with $\Delta H_{p-p} = 9$ gauss which overlaps the reported main signal at $g = 2.006$. The second signal is either temperature - dependent and shifts 17 gauss past the main signal when going from -180 C to +50 C or one signal has much line broadening with temperature. Introduction of trace contaminants during oxidation increases this signal intensity markedly and leads to the postulated retention of sodium and fluorine impurities as the origin of the second signal.

The unexpected resonance signal for the samples with aluminum over the oxide is considered important because aluminum is widely used as interconnections over the oxide on integrated circuit surfaces. This type oxide sample is actually simplier to investigate than the powder samples since it is on a single crystal of silicon. It could be electrically biased during EPR scanning to provide further data on the capacitance voltage behavior of the oxide. It is recommended that this type sample be further studied rather than the silicon powder samples which are very difficult to analyze because of the overlapping temperature dependent behavior of the resonance signals and the more difficult nature of powdered silicon material. The relevance of this type sample to modern planar technology further supports this recommendation.

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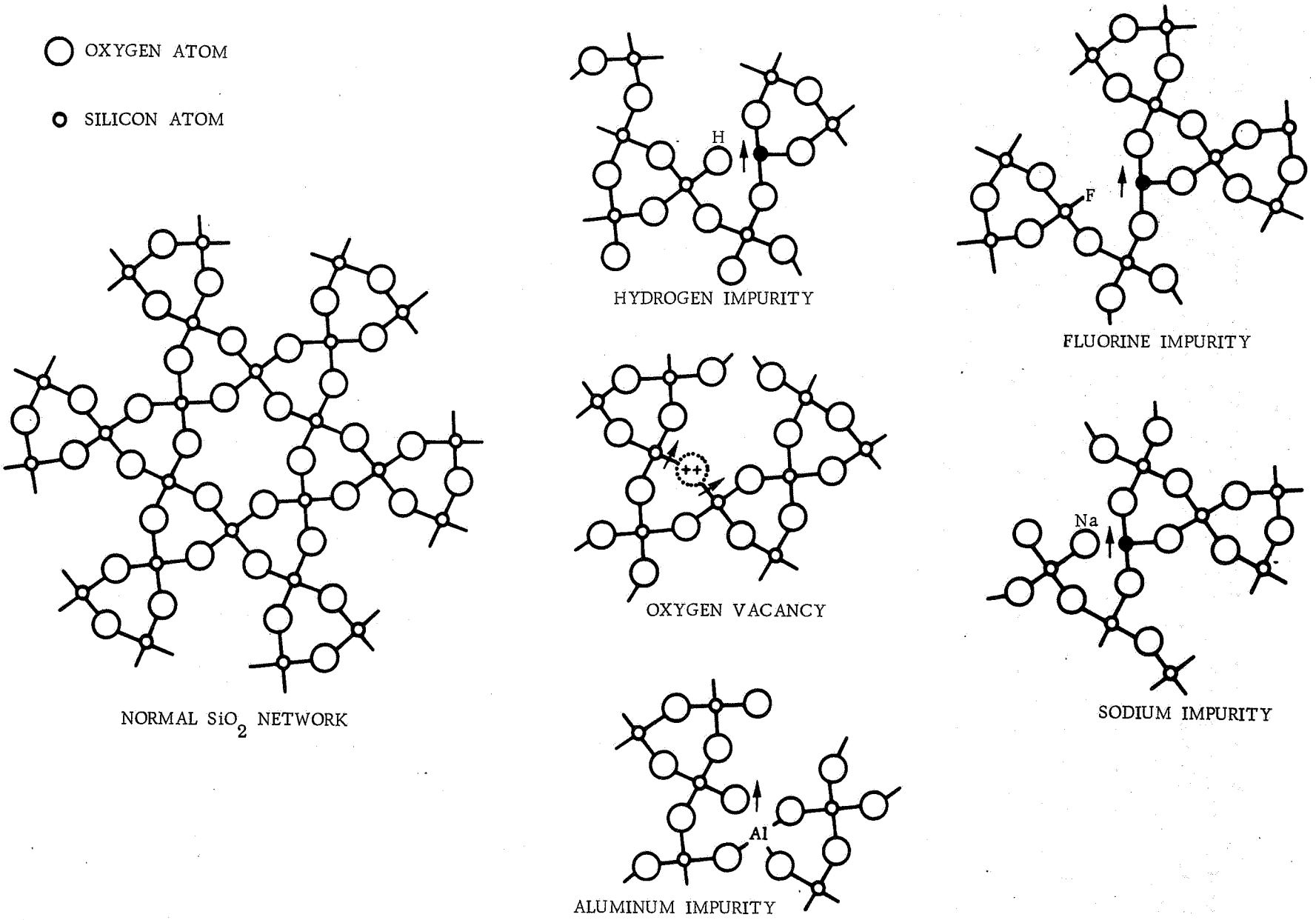
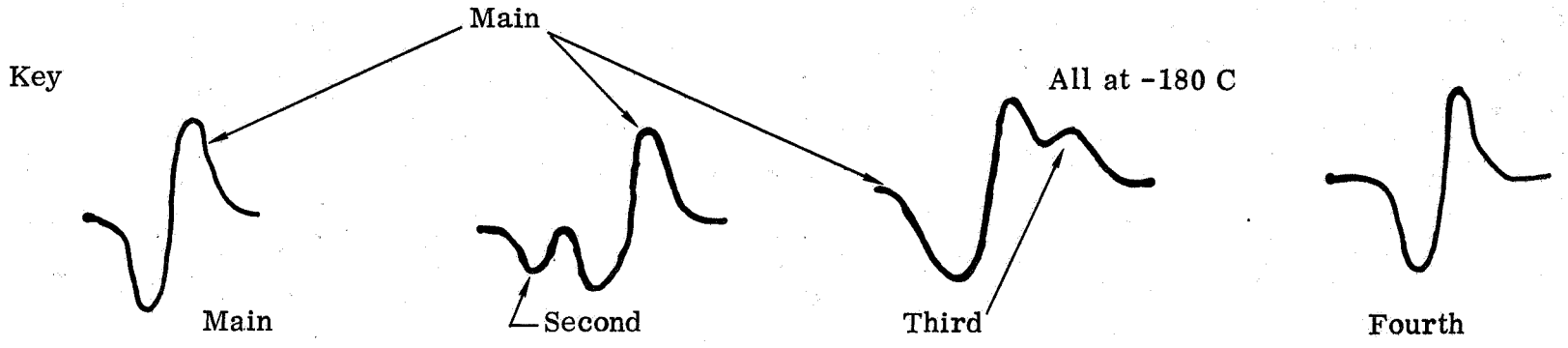


Figure C-18.- Possible Impurity Structures and Oxidation States in S_iO_2

TABLE C-4
SIGNAL SUMMARY FOR Si-SiO_2 SYSTEM

	Silicon Dioxide on Powered Silicon (Boron, Phosphorus and Intrinsic)						Single Crystal Al on $Si O_2$	
	Wet	Dry	Na OH (Wet)	Na CI (Wet)	HF (Wet)	H_2 Bake (Wet)	Wet	Dry
Main	Yes	Yes	Yes	Yes	Yes	Yes	No	No
Second	Yes	No (except Na CI)	Yes	Yes	Yes	No	No	No
Third	No	No	No	No	No	Yes	No	No
Fourth	No	No	No	No	No	No	Yes	Yes



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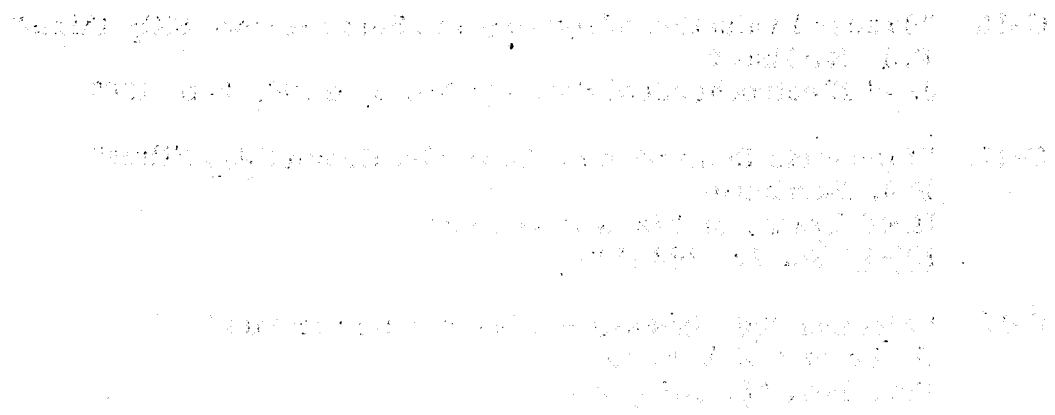

APPENDIX D. ELECTRON SPIN RESONANCE SPECTRA OF IMPURITIES AND OXIDATION STATES IN THERMALLY GROWN SILICON DIOXIDE*

BY
C. W. SCOTT AND J. E. MEINHARD

A previously unreported electron spin resonance signal has been identified with the Si-SiO_2 system produced by partial thermal oxidation of silicon which may be associated with the trapping states characteristically observed by other techniques. Oxide samples were prepared by pulverizing single crystal intrinsic silicon and exposing them to wet or dry oxygen at 1150C. X-band measurements at 77 K on samples prepared under moist conditions revealed an absorption at $g = 2.011 \pm 0.001$ with $\Delta H_{p-p} = 9G$ which partially overlapped the silicon crystal defect absorption at $g = 2.006$. The g value of the signal at 2.011 was found to be temperature dependent and shifted 17G through the silicon crystal signal in going from 77 K to 350 K. Inroduction of trace contaminants during oxidation, such as sodium or fluorine, increased the signal intensity and led to the postulation of the presence of radical species as the origin of this absorption. Additional independent signals have been detected from samples annealed in hydrogen and from samples with high purity aluminum deposited on the oxide. These have been tentatively associated with the presence of incomplete oxidation states.

(Abstract of talk delivered at the American Physical Society Meeting, University of Washington, September 1967)

*Work supported by NASA-ERC

APPENDIX E. FACTORS INFLUENCING DIELECTRIC DEFECTS IN SILICON OXIDE LAYERS*

BY
P.J. BESSER, J.E. MEINHARD, AND P.H. EISENBERG

Abstract

The incidence of dielectric defects in thermally grown silicon oxide films has been investigated utilizing previously developed defect detection techniques. The oxide layers exhibited a strong dependence of dielectric defect density on film thickness, on moisture content of the oxidizing ambient and on type and concentration of the substrate dopant. Characterization of the defects indicates that they are primarily pores in the oxide layer. Mechanical stress resulting from the mismatch in thermal expansion characteristics of the silicon and the oxide is postulated as an important defect-producing mechanism and the experimental results are interpreted on this basis.

Introduction

In modern silicon planar technology, silicon dioxide layers are required to perform the threefold function of surface passivation, diffusion masking and electrical insulation. Extensive experimental and theoretical consideration has been given to the first two capabilities which are concerned with the migration of atoms, molecules, and ions on or within the oxide layers. Comparatively little effort has been devoted to the determination of the frequency of incidence, process origin, microscopic nature, and structural basis of regions of anomalously low dielectric breakdown in oxide films. This lack of emphasis has been due partly to the greater urgency attached to the solution of the migration problems, which lead to gross degradation of electrical device parameters, and partly to the lack of adequate techniques for dielectric defect detection. However, it is now evident that oxide dielectric failures represent a serious threat to the reliability and yield of monolithic silicon microelectronic devices. (see Ref E-1.) The advent of MOS technology with its stringent requirements on gate oxide purity and dielectric integrity, coupled with the interest in the development of large scale MOS and bipolar arrays, has made the requirement for large areas of dielectrically sound oxide on a silicon slice even more critical.

In view of the present and imminent demands on the electrical insulation properties of oxide layers, a systematic investigation was undertaken to examine the physical and chemical processes which influence oxide dielectric quality and to determine the nature and origin of dielectric defects and their relation to the oxide structure. The ultimate objective was the achievement of an understanding of the nature and mechanism of defect formation and the establishment of optimum conditions, compatible with device requirements, for reduction or elimination of dielectric flaws. The factors whose influences on defect incidence were considered are the condition of the silicon substrate, the growth conditions of the oxide, and the process treatments undergone by the wafer during device fabrication.

*Delivered at the Electrochemical Society Meeting, Philadelphia, Pennsylvania 13 October 1966.

Experimental Method

Silicon substrates. - The silicon wafers used in the portion of the program dealing with effects of silicon substrate condition and oxidation techniques were single crystal Czochralski grown samples with (111) surfaces. Both acceptor (boron) and donor (phosphorus, antimony) doped wafers were examined. The carrier concentrations were in the range from $5 \times 10^{14}/cm^3$ to $5 \times 10^{19}/cm^3$. Some wafers with an n-type epitaxial layer on a p-type substrate were studied, but the majority of the samples were nonepitaxial. Several different silicon surface preparation techniques were utilized including chemical polishing, chemical-mechanical polishing sequences, HCl vapor etching, and preoxidation cleaning. Although no particular degree of crystalline perfection was specified or maintained on the crystal slices, all specimens were obtained from sources meeting standard criteria for device fabrication.

For the investigation of the influence of process treatments during device fabrication, groups of wafers were obtained from three major integrated circuit vendors. The wafers were selected from various points in the process of fabrication of a digital integrated circuit and are thus representative of the state-of-the-art in industry processes.

Oxidation conditions. - The slices were oxidized at temperatures from 1050 C to 1180 C in dry oxygen, wet oxygen, and wet nitrogen. The water bath temperature for the wet nitrogen growth was 25 C and for the wet oxygen case was either 25 C or 99 C. The latter condition is referred to as steam growth during the remainder of the paper. Films were grown in the thickness range from 850 Å to 12,000 Å. Thickness determination was made by color comparison with previously calibrated standards.

Defect detection. - As previously indicated, a prerequisite of any study of this nature is the availability of an adequate means of detection of dielectric defects. Previously utilized techniques such as a high temperature HCl etch (Ref E-2) or Cl etching around 900C (Ref E-3 and E-4) are not conveniently applicable. Consequently, a program was initiated to attempt development of a nondestructive, reproducible, recordable, convenient, and functional test for oxide defects. The results of that program have been previously reported (Ref E-5) and the two techniques which were found to be suitable, electrophoretic decoration and electrochemical autograph, were utilized in this study for the observation of oxide defects. In the decoration method, a probe voltage of 5 v, a probe-to-wafer spacing of 2 mm, and a probe material of Ni were used. In the autograph technique a 5 to 15 volt potential was applied for 5 to 10 minutes. Defect values were obtained by counting decorations or autograph sites under a microscope.

Relationship of Experimental Parameters and Dielectric Defect Incidence

Film Thickness. - The experimental data demonstrated that the dielectric integrity of virgin thermal oxides is strongly thickness dependent. This variation with thickness is shown in Figure E-1 for the average of a typical group of samples oxidized under the same conditions. All of the oxides studied show this same functional dependence of defect density and thickness; but the position and shape of the curve are influenced by a number of factors, some of which are considered in this

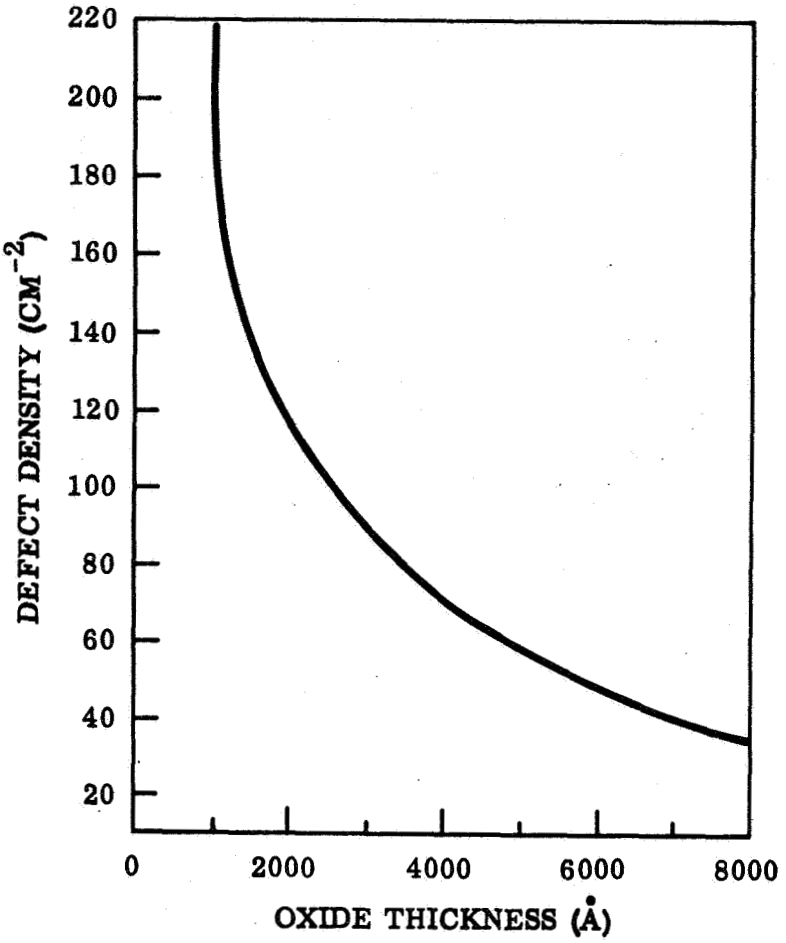

Figure E-1. - Defect Density Variation in Virgin Thermal Oxide

paper. The number of defects is relatively independent of thickness in the range greater than 4000 Å but generally begins to increase gradually in the 2000-4000 Å range with a very rapid increase below 2000 Å.

Moisture content of oxidizing ambient. - For oxides of a given thickness, the number of defects/cm^2 is dependent on the amount of water vapor in the oxidizing ambient. The data in Table E-1 shows this effect on samples consisting of oxidized

p-type substrates and n-type epitaxial layers on p-type substrates. The doping level in these wafers was $\approx 10^{16}$ carriers/cm^3 and there was no significant difference between the readings obtained on the various samples. It can be seen that the presence of water vapor in the growth ambient has a beneficial effect on the oxide defect incidence. Consideration of only the steam and dry O_2 conditions might lead to the alternate conclusion that it is the rapid growth rate of the steam oxide which is the significant factor. However, the wet O_2 and wet N_2 situations require growth times comparable to that of the dry O_2 and yet their defect density is essentially equivalent to that of the steam grown oxide when film thickness corrections are made. Thus, it appears an oxide grown in a moist ambient will have fewer defects than one grown dry if all other conditions are the same. This effect was observed for all dopant types and concentrations studied, and for both expitaxial and nonepitaxial wafers.

Etched oxide layers. - The same functional dependence of defect density on thickness that was determined on virgin oxides was also observed in oxide layers as they were thinned by etching. However, the defect density at a particular thickness was greater for the thinned oxide than for the unaltered oxide which is in agreement with the results of Lopez (Ref E-6). Our data, however, does not reveal as great a difference between the virgin and etched oxides of the same thickness as is indicated in his results since even the virgin oxide has a high density of defects in the 3000 Å range. When the etched layer is regrown to successively greater thicknesses, the defect density decreases in a manner closely approximating the etch-back curve rather than the curve for the as-grown oxides. The growth, etch-back, and regrowth variations are shown for a steam grown oxide on one ohm-cm boron-doped substrates in Figure E-2. The points on the growth curve represent measurements made on individual wafers grown to the indicated thickness while the etch and regrowth were performed on the slice on which the initial oxide was 8000 Å thick. This type of variation is typical of that obtained on dry oxides as well. Thus regrowth provides somewhat of a curative effect in going from thin to thicker oxides, but the resulting oxide at a given thickness has more defects than one originally grown to that specific thickness.

TABLE E-1
EFFECT OF MOISTURE ON DEFECT DENSITY

Growth Condition	Oxide Thickness	Defect Density (cm^{-2})
Steam	3650 Å	.23
Wet O_2	3100 Å	41
Wet N_2	3950 Å	22
Dry O_2	3850 Å	60

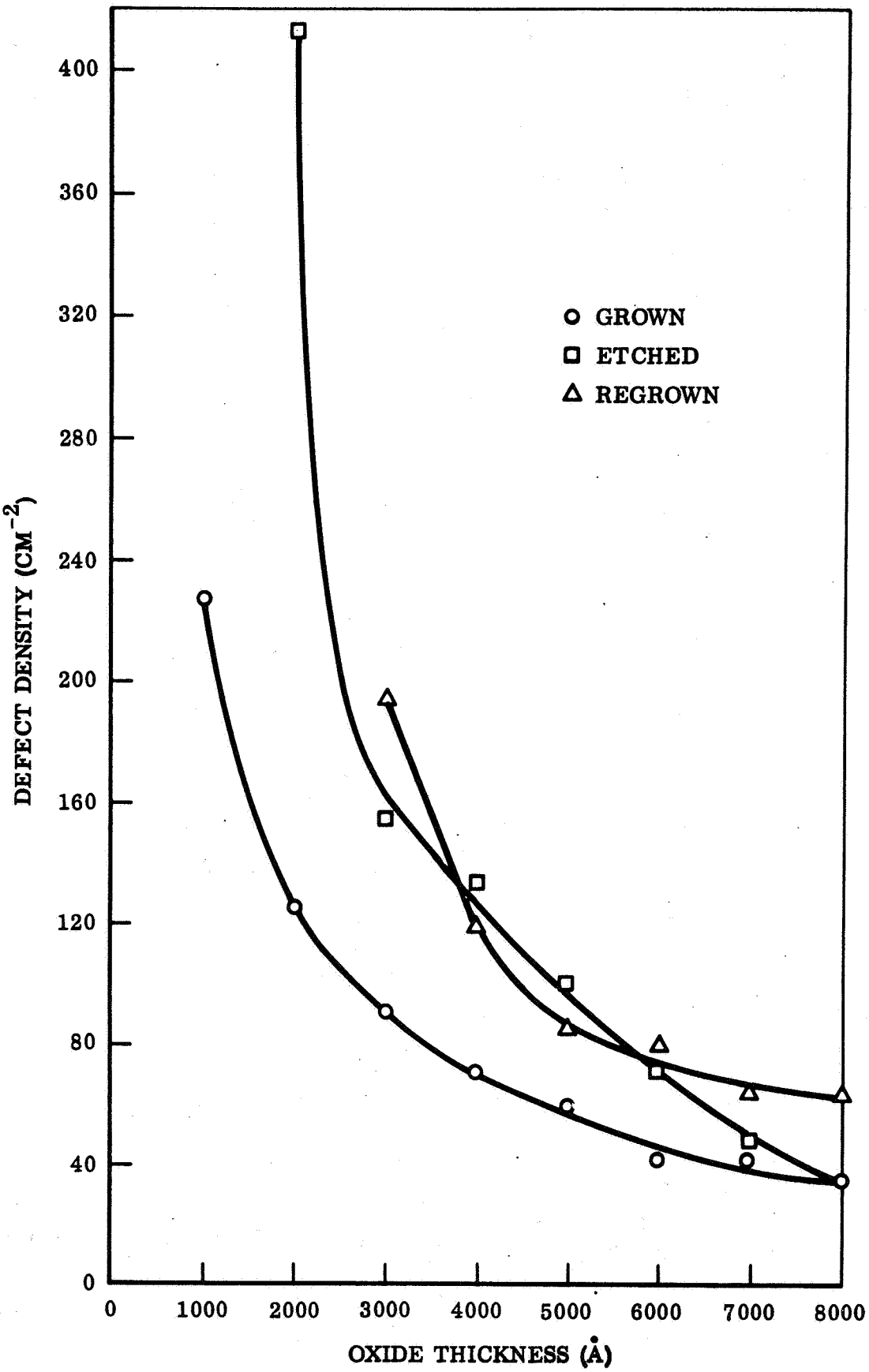

Figure E-2. Comparison of Defect Densities in Grown, Etched Back, and Regrown Oxides

Silicon surface preparation. - The effect of preoxidation surface treatment of a silicon substrate on defect density was also investigated on the wafer groups shown in Table E-2. The wafers were oxidized under identical conditions and the defects measured on each group. The oxide thickness was 1200 Å and the results indicate that the effect of surface preparation on oxide dielectric integrity is relatively small in this thickness range. The general trend, however, was that oxides grown over surfaces in which the chemical polish was the final step contained fewer defects than those grown on wafers with a final mechanical or mechanical-HCl vapor polish. It has been shown (Ref E-7) that mechanical polishing results in a certain amount of structural damage to the silicon surface and may leave particles of the polishing compound embedded in the polished surface. This may be the origin of the somewhat higher defect density in the oxide grown on such wafers. Work is proceeding on the evaluation of particulate contamination and substrate crystal defect contributions to oxide flaws, and these results will be reported in a future paper.

Oxidation temperature and growth rate. - A dependence of dielectric integrity upon growth temperature (or growth rate) was observed for oxide layers less than 2000 Å thick grown in dry O_2 over heavily boron-diffused regions. The layers grown at lower temperatures contained more defects than those of the same thickness grown at higher temperatures. The variation with growth temperature became less as the film thickness increased. These results are shown in Figure E-3. The results of the steam and wet N_2 oxidations shown in Table E-1 also indicate an absence of growth rate effects in thicker layers although it may be that the presence of moisture is the dominant influence in wet oxides. The substrates in Table E-1 were also more lightly doped than those in which the growth rate influence was seen.

Substrate impurity type and concentration. - Preliminary work in other phases of this investigation indicated that oxides grown over heavily boron-doped regions in dry O_2 were more defect-free than those grown over regions of low boron concentration or over phosphorus-doped regions. This suggested a possible influence of substrate impurity type and concentration on the integrity of the grown oxide. Since the amount of impurity incorporated in the oxide and the degree of partition of impurity between the oxide and silicon are partially dependent on the growth conditions, it was decided to vary impurity type, impurity concentration, and oxidation conditions on a group of samples to determine the combined influences of impurity and oxidation procedure.

TABLE E-2
SILICON SURFACE PREPARATION

Wafer Group	A	B	C	D	E
Surface Preparation	Chemical Polish Clean*	Chemical Polish Mechanical Polish Chemical Polish Clean*	Chemical Polish Mechanical Polish HCl Vapor Etch	Chemical Polish Mechanical Polish Clean*	Chemical Polish Mechanical Polish HCl Vapor Etch Clean*

*The cleaning was in deionized water and organic solvents.

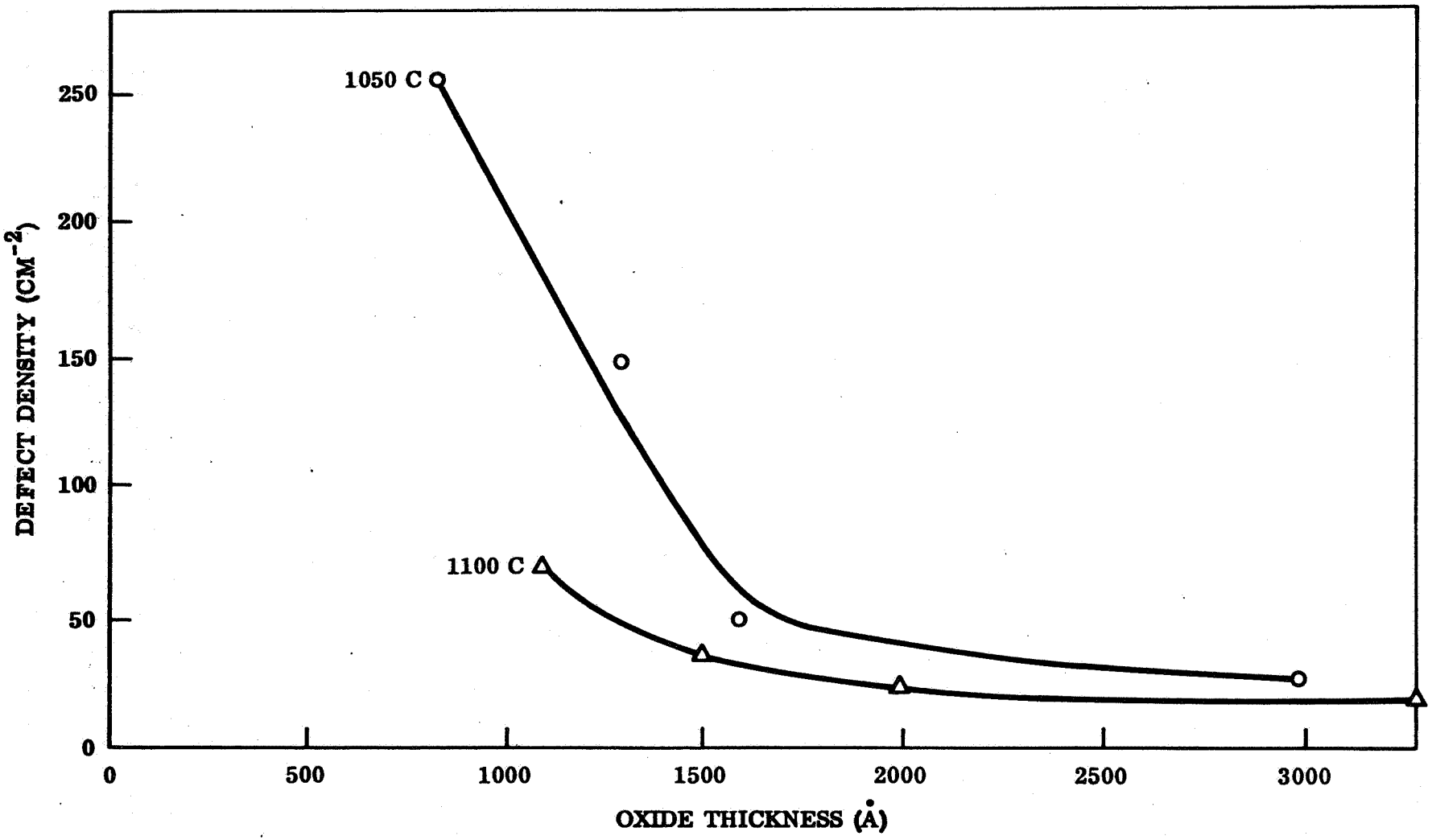

Figure E-3.-Defect Density vs Thickness Variation With Oxidation Temperature

The silicon samples consisted of the four groups of wafers shown in Table E-3. A wafer from each group was subjected to each of the oxidation conditions shown in the table.

A chemical-mechanical-chemical polishing sequence was used on the wafers and the oxidation temperature was 1150 C. The defect densities were measured and recorded on each sample after which each film was etched back to 2000 Å and the defects remeasured. The results are shown in Table E-4.

The values labeled "etched" are the defect densities in each oxide after the layers had been chemically thinned to 2000 Å. There are a number of observations and conclusions that may be drawn from these data:

1. In the steam and WD oxides, the heavily boron-doped sample has a much higher defect density than the others initially, but a substantially lower density than the others after etching.

2. The heavily boron-doped sample has a lower defect density in the dry oxide than in the stream oxide in contrast to the other three samples. The densitities in the initial oxides of Group C are considered to be anomalously high for reasons which will be presented in the Discussion section.

3. The WD sequence produces the best overall oxide when evaluated on the basis of freedom from both initial defects and fast-etching imperfections.

4. Each boron-doped sample has essentially the same density of defects in the initial oxides formed by WD and DW sequences, but the DW etched oxides have more defects than the WD etched oxides. The superior etch-resistance of the WD oxide compared to the DW is also evident in the n-type samples, but the initial defects were higher as well.

TABLE E-3
SUBSTRATE IMPURITIES AND OXIDATION CONDITIONS

Wafer Group	Dopant	Carrier Concentration (cm^{-3})
A	Antimony	10^{17}
B	Phosphorus	5×10^{14}
C	Boron	5×10^{19}
D	Boron	10^{15}

Oxidation Conditions

1. 8000 Å grown in steam (W)
2. 8000 Å grown in dry O_2 (D)
3. 4000 Å grown in dry O_2, followed by 4000 Å in steam (DW)
4. 4000 Å grown in steam, followed by 4000 Å in dry O_2 (WD)

TABLE E-4
EFFECT OF SUBSTRATE DOPANT AND OXIDATION CONDITIONS ON DIELECTRIC DEFECT DENSITIES IN SiO_2 LAYERS

Wafer Group Dopant Concentration (cm^{-3})	Defect Density (cm^{-2})			
	A 10^{17} (Sb)	B 5×10^{14} (P)	C 5×10^{19} (B)	D 10^{15} (B)
Oxidation Conditions:				
1. Steam				
A. Initial	20	12	126	7
B. Etched	549	516	281	449
2. Dry Oxygen				
A. Initial	28	29	21	21
B. Etched	-(1)	670(2)	216	335
3. Steam-=Dry Oxygen (WD)				
A. Initial	15	15	35	15
B. Etched	527	428	195	297
4. Dry Oxygen-Steam (DW)				
A. Initial	71	44	38	19
B. Etched	663	469	414	388

(1) Oxide destroyed by etching.

(2) Etched to 1850 Å rather than 2000 Å. Comparison of this value with 2000 Å films is not completely valid because of the sharp increase in defect density with decreasing thickness in this region.

5. Oxides from sample group C are consistently better than those from the other groups after etch-back except in the case of the DW sequence where they are comparable to Group D oxides.

6. The phosphorus- and antimony-doped wafers have consistently poorer oxides after etch-back than the boron-doped wafers.

The interpretation of these results is deferred to the Discussion section.

Integrated circuit fabrication processes. - The wafer samples obtained from commercial manufacturers of integrated circuits were subjected to evaluation to determine the variation of defect density with processing and to compare the vendors' processes. The data are shown in Table E-5.

The difference in defect variation with process stage is a manifestation of the difference in techniques between vendors and points out the sensitivity of oxide integrity to changes in processing.

One of the most significant points of this evaluation which does not appear explicitly in the table is the observation that a significant portion (30-90 percent) of the total defects after the initial oxide stage occur at abrupt transitions in the oxide thickness such as diffusion window perimeters.

As can be seen in the case of vendor A, a suitable pyrolytic oxide can be effective as a late process step in reducing defect density to a low level while a thermally regrown oxide appears to be relatively unsatisfactory.

Previously reported data (Ref E-5) on stress levels in oxide films as a function of process steps undergone indicated that defects generally increase with stress level and amount of mechanical flexing due to repeated temperature excursions from room temperature to the vicinity of 1000 C.

TABLE E-5
COMPARISON OF DEFECT DENSITY (cm^{-2}) AMONG PROCESSORS

Process Step	Vendor A (non-epi)	Vendor B (epi)	Vendor C (epi)
Initial Oxide	5*	23	1.6
After Isolation Diffusion		3.4	10
After Collector Diffusion	5		
After Etch Prior to Base Diffusion		2.0	
After Base Diffusion		3.1	
After Emitter Diffusion		3.1	0.8
After Contact Opening and Thermal Oxide Regrowth**	250		
After Contact Opening and Oxide Deposition	3	4.7	

*Each numerical entry represents the average of the counts on a group of wafers.

**Experimental run only; not characteristic of present product.

Nature and Origin of Dielectric Defects

A number of possibilities can be visualized as the source of regions of anomalously low dielectric breakdown in insulating layers. These would include actual holes or pores in regions of surrounding continuous oxide, high conductivity or fast-etching loci in sound oxide due to foreign inclusions or intrinsic structure anomalies, and thin spots or depressions in a nominally uniform thickness layer.

Techniques such as optical microscopy, Nomarksy phase contrast microscopy, preferential etching, and replicate electron miscroscopy were used in conjunction with the developed detection techniques in an attempt to characterize the dielectric defect loci. The evidence, as reported previously (Ref E-5) and in a forthcoming paper (Ref E-8) indicates that dielectric failures are a result primarily of actual physical openings in the insulating layer rather than regions of enhanced conductivity in uniformly thick oxide. In some cases the fissures occur in mound-like elevations in the oxide which may be a result of foreign particle inclusion or buckling of the oxide. Electron microscope replica photographs of typical defects are shown in Ref 8.

One of the origins of dielectric defects is felt to be the mechanical stress in the oxide layer as a result of the difference in coefficient of thermal expansion between Si and SiO_2. This effect is considered in detail below in conjunction with a proposed model to explain the experimental results. Other possible sources of dielectric defects, such as particulate contamination of the wafer surface and crystal defects in the substrate, are being investigated; but the results are incomplete at present.

Discussion

Consideration of the experimental data from this investigation in conjunction with the present knowledge and conception of the silicon oxide structure and the results of other studies on the properties of SiO_2 and silicate glasses leads to a consistent picture of the nature, structural roots, and process origins of regions of anomalously low dielectric breakdown.

Basic to our understanding of the oxide properties is the concept of an intrinsic oxide. Revesz (Ref E-9) has pointed out the ideal amorphous network of silicon-oxygen tetrahedra can be considered as an intrinsic or defect-free material and any deviation from it as a structural defect. This definition will obviously include some structural defects which are unrelated to dielectric breakdown loci. It will be seen, however, that certain types of oxide structural modifications are intimately connected with oxide dielectric integrity.

The intrinsic silica structure is quite rigid with strong bonding between the Si and O atoms in the tetrahedra and with the tetrahedra joined at the vertices. The thermal expansion characteristics of Si and SiO_2 are quite different in the range from room temperature to diffusion-oxidation temperatures (1000-1200C), and consequently mechanical stresses resulting from this differential are expected in the oxide and the substrate of silicon wafers thermally oxidized and subsequently cooled to room

temperature.* The linear thermal expansions of silicon, bulk amorphous fused silica and a borosilicate glass are shown as a function of temperature in Figure E-4. The silicon data are taken from Ref E-10 and the silica and glass data from Ref E-12. It can be seen that the expansion of the oxide is smaller than that of the silicon below 700 C. Thus, a compressive stress would be expected in the oxide layer at room temperature. Rupture of the oxide as a result of this stress could produce dielectric flaws in the oxide layer. This stress has been experimentally verified (Ref E-5 and E-11) and is found to be in the range from 30,000 to 60,000 psi. The expansion characteristic of silicon apparently exhibits unusual behavior (Ref 13) above ~ 1000 C. However, no measurable stress can develop in the Si-SiO_2 structure until the temperature drops to a value where the oxide becomes essentially rigid. This setting point is generally taken to be between the strain and annealing points for a glass (Ref E-12) 990 C and 1050 C respectively for pure SiO_2. The actual value is not sharply defined and depends on the thermal history of the sample. Thus, the significant region to consider in the thermal expansion characteristics is below the setting point of the silica (~1000 C). If curves such as shown in Figure E-4 are plotted to intersect at the setting point a display of the expansion mismatch at lower temperatures is obtained.

The effect of structural defects such as hydroxyl groups and network forming or modifying cations is to alter the silica structure producing a less rigid network. This alteration is reflected in changed physical and electrical properties. For example, the introduction of either boron (Ref E-12) or hydroxyl (Ref E-14) into the SiO_2 structure increases the thermal expansion coefficient and decreases the viscosity (lowering the setting temperature) of the modified material relative to the intrinsic oxide. The low temperature (0-400 C) expansion coefficient and setting point for a borosilicate glass such as Corning 7740 are 33×10^{-7} and ~500 C respectively as compared to 5.5×10^{-7} and ~1000 C for pure SiO_2. Such a glass would provide a better match to the thermal expansion characteristics of Si than the pure oxide. A similar improvement would be obtained by the introduction of hydroxyl groups into the intrinsic silica. It is seen therefore that both of these structural modifications should lower the low temperature compressive stress in an oxide layer formed on a silicon substrate at temperatures in the vicinity of 1000 C. The properties of phosphorus-modified silica are not as well known, but it is expected that they would follow the same general tendency toward a less rigid structure having greater thermal expansion and less viscosity than pure silica.

It has been demonstrated that hydroxyl groups can be introduced into silica by high temperature exposure to water vapor (Ref E-15), that oxides grown in steam or wet ambients contain measurable amounts of hydrogen (Ref E-16, E-17, and E-18) and that thermally grown oxides incorporate varying amounts of the substrate dopant into the oxide structure (Ref E-19 and E-20). Therefore, the substrate dopant will be responsible for a defect structure in the thermal oxide under both wet and dry oxidation conditions with hydroxyl groups included in the former case. The experimental data are considered below in terms of these concepts of oxide structure.

*There is no assurance that the detailed structure of bulk silica glass is identical to that of amorphous oxide films grown on silicon substrates. However, the published properties of silica glass and thermally grown oxide films are in sufficient agreement to allow the assumption of approximately identical expansion characteristics.

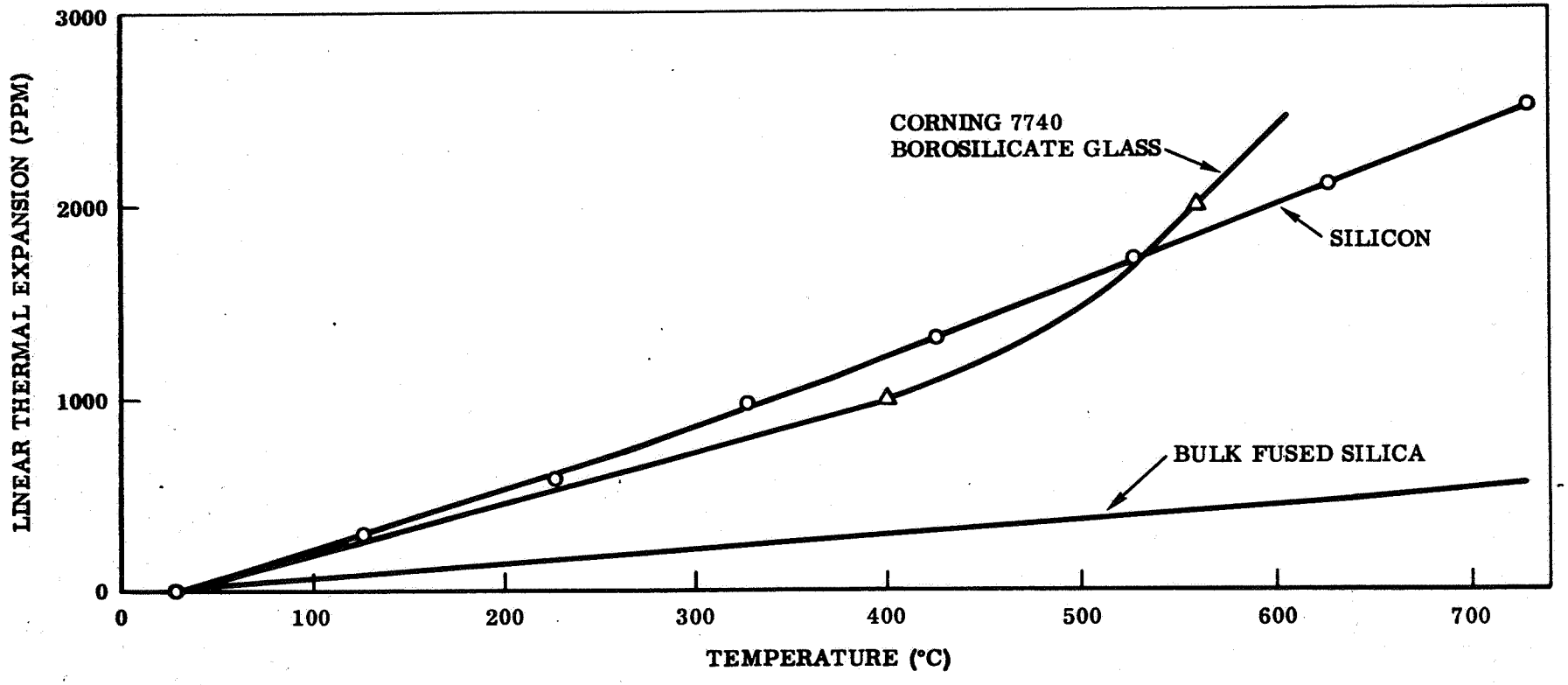

Figure E-4.- Comparison of Thermal Expansion Characteristics

When a uniformly doped silicon wafer is thermally oxidized, there occurs a partition of the substrate dopant between the oxide layer and the substrate, and the final distribution of the dopant in each material is essentially dependent upon the following factors:

1. The ratio of the equilibrium concentrations of the dopant in the oxide and in the silicon

2. The diffusion constants of the dopant in the oxide and the silicon

3. The oxidation rate and temperature

It has been determined (Ref E-20) from a consideration of the above factors that the growing oxide has an affinity for boron but rejects phosphorus and antimony. Therefore, oxidation of doped silicon wafers results in impurity profiles in the oxidized wafers as summarized in Figure E-5. The depletion of boron from the substrate is a considerably stronger effect than the pile-up of phosphorus and antimony. Consequently we neglect changes in the substrate impurity profile for phosphorus- and antimony-doped wafers and consider only the redistribution of boron. The profile in the silicon is strongly dependent upon the temperature and rate of oxidation. The least deviation from the uniform bulk distribution occurs when the oxidation temperature is high and the oxidation rate is low. These conditions are best met by high temperature (>1100 C) growth in dry oxygen. The conditions which produce the smallest perturbation of the bulk profile also result in the incorporation of the greatest amount of impurity in the oxide layer. This means that more boron should be present in dry oxides than in steam oxides. It is expected, therefore, that the impurity concentrations in the oxide layers on boron-doped substrates, as a result of the oxidation techniques used in this experiment, will be as shown in Figure E-6.

In addition to the substrate dopant level and profile in the oxide, there are other factors which must be considered in attempting to understand the experimental results. These are the effect of hydroxyl groups, substrate crystalline imperfections, and particle contamination on the oxide structure and dielectric quality. Previous discussions indicated that modification of the oxide by hydroxyl groups would be beneficial to the dielectric quality of the silicon oxide. The presence or absence of a definite relationship between oxide dielectric defects and substrate crystal defects and/or surface particle contamination has not yet been established so it is not possible to eliminate these factors from consideration as defect sources.

It can now be seen that most of the experimental data can be explained by considering oxide dielectric defects to result from microscopic cracks or fissures in the layer produced by the mechanical stress resulting from the differential thermal expansion characteristics of the $Si-SiO_2$ system. It should be pointed out that glass always fails from a tensile component of stress even when the loading is compressive. Since the stress originates at the interface between the silicon and the oxide, it is expected that ruptures in the oxide will occur at this boundary and propagate toward the outer surface of the oxide. In thicker films the propagating stress, which should be partially relieved by the rupture of the oxide, may not be sufficient to allow all of the defects to penetrate the entire thickness of the layer. This would account for the observed decrease in defect density with increasing oxide thickness. In an oxide grown to any thickness on a silicon wafer, there is presumably a distribution in the local stress levels. Those regions which are just below the rupture level or see only

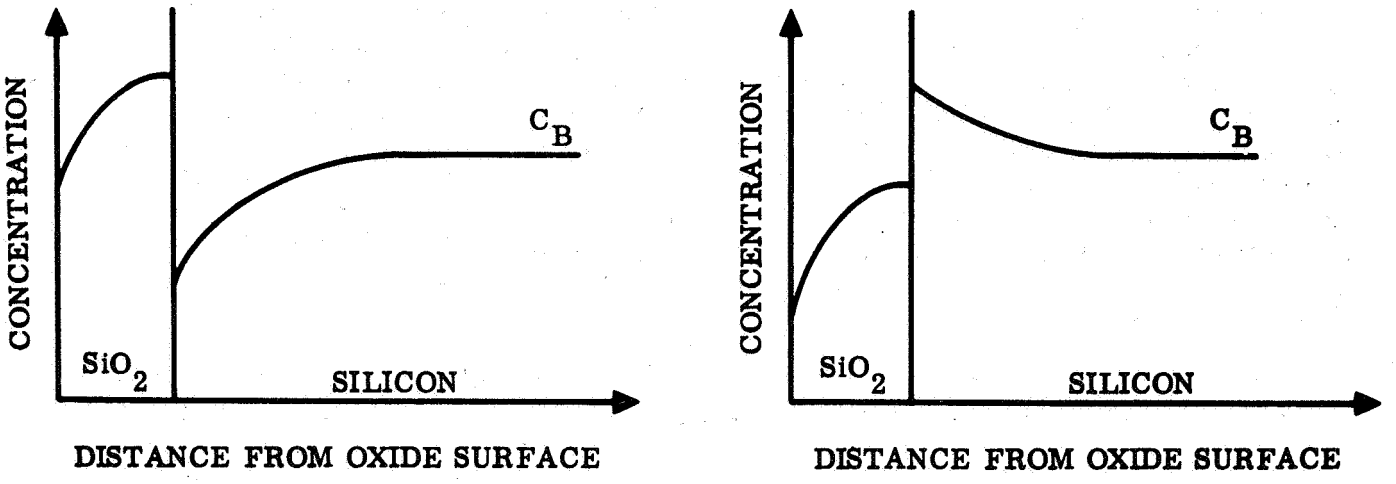

Figure E-5.- Impurity Profiles in Oxidized Silicon Wafers. C_B denotes bulk impurity concentration. (From Grove, et al, Reference 20)

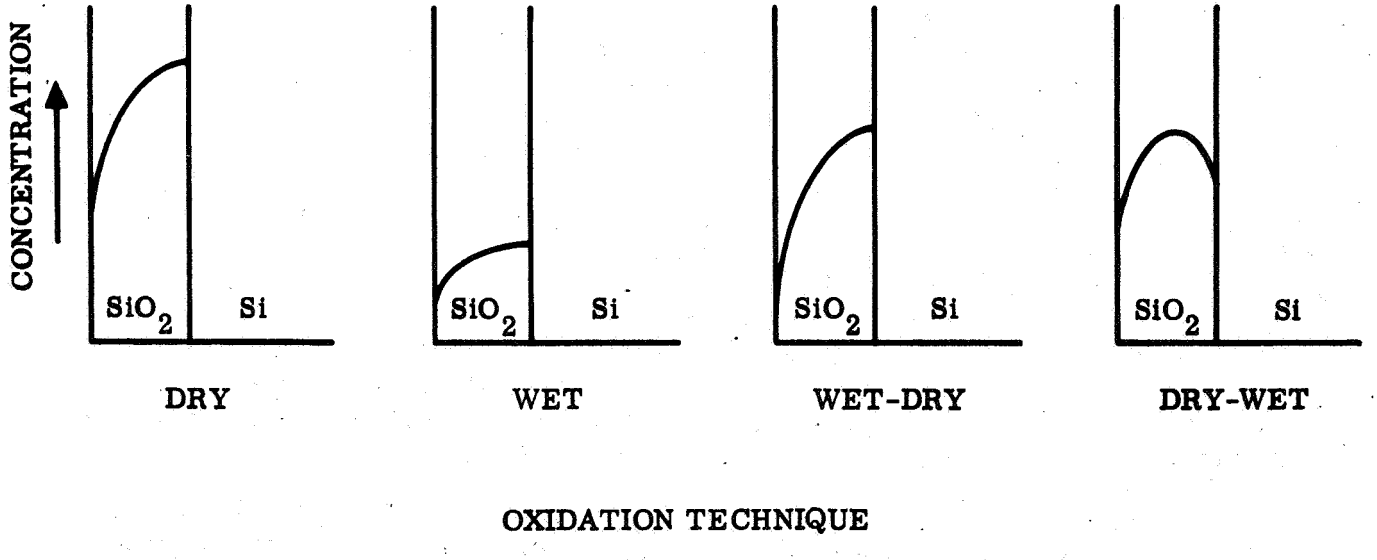

Figure E-6.- Postulated Boron Distributions in Thermally Grown Oxides

compressive components of stress would be attacked more rapidly by chemical etching. This is thought to be the basis of the higher density of defects in an etched film as compared to a virgin layer of the same thickness. Since diffusion of impurities may also be enhanced in a strained region, the fast etching imperfections described by Lopez (Ref E-6) may be high stress sites in the oxide. The ineffectiveness of thermal regrowth of oxide as a defect elimination technique is apparently a result of the appearance of additional defects in previously sound oxide as a result of the thermal (and stress) cycling. This was demonstrated by measuring the defects on an initial oxide, taking the wafer through five temperature cycles from room temperature to 1150 C in an inert atmosphere, and remeasuring the defect density. It was found that the temperature cycling produced an order to magnitude increase in the number of dielectric flaws.

The beneficial effect of moisture in the oxidizing ambient is attributed to the incorporation of hydroxyl groups in the oxide and the resulting improvement in the oxide thermal expansion characteristics relative to the silicon. The contribution of this factor to improved oxide dielectric quality can be partly offset by the ion trapping characteristic associated with the exchange of protons for other positive ions at these sites. The variation of the defect density versus thickness characteristic with growth temperature shown in Figure E-3 can be explained on the basis of incorporation of more boron in the oxide grown at the higher temperature. This is a result of the increased ratio of oxidation rate constant to diffusion coefficient of the impurity in the silicon as the temperature is increased. Since the setting point of the oxide is ~1000 C, the temperature range over which the mechanical stress develops is the same for each oxidation temperature and may even be less for the more heavily boron-doped oxide. The 1100 C oxide should also have a higher expansion coefficient resulting in a lower stress level and fewer ruptures in the film as experimentally observed. Also, as shown in Figure E-5 and E-6, the impurity profile in the oxide is such that the best match in expansion characteristics occurs at the oxide-silicon interface where the stress originates.

The data in the samples described in Table E-2 indicate that the surface preparation techniques investigated had relatively little influence on the oxide integrity. Preliminary work on wafers deliberately contaminated with particles at levels differing by an order of magnitude has shown little variation of oxide integrity with particulate contamination. However, it will be seen that not all the results of Table E-4 can be explained readily without postulating defect-producing mechanisms in addition to mechanical stress. No attempt was made here to confirm the results of Nassibian and Whiting (Ref E-21) that particulate contaminations on the oxide surface act as loci for the formation of high concentration regions of P_2O_5 during a depostion of phosphorus. In the subsequent diffusion, the phosphorus is considered to penetrate the oxide preferentially beneath these high concentration sources, doping the silicon substrate in localized regions under the oxide. It is possible that Lopez, in his utilization of a phosphorus deposition and diffusion as a defect detection method, obtained contributions from such sources.

The variation of defect densities shown in Table E-4 is regarded as arising mainly from stress produced cracks or fissures in the oxide layer. The modifying factors are incorporation of substrate dopants and hydroxyl groups in the grown oxide. However, from the previous discussion we would expect the samples from group C to contain the fewest defects in the initial oxide layer since these oxides have the highest boron content. It was also expected that the wet oxide of group C would be the best

since both structural modifications should reduce stress-induced defects. The high defect values found in the initial oxides of group C are therefore considered to be a result of other defect-producing mechanisms such as particle contamination or substrate crystalline imperfections. This possibility is supported by the observation that the oxides of group C are quite sound after etch-back, indicating that the high density in the initial oxide results from certain localized imperfections. The average of all our previous and subsequent measurements has shown that oxides grown on heavily boron-doped substrates have fewer defects than those grown on more lightly boron-doped slices. The preliminary work on contamination tends to promote the conclusion that its contribution to defect incidence is relatively small. If substrate crystal imperfections are sources of oxide flaws, the defect density obtained on a heavily doped wafer would represent a compromise between the two competing tendencies of boron incorporation and silicon cyrstalline perfection. This would seem to be the case in group C with its poor initial layers which are relatively sound after etching. Also, if localized crystal defects are dielectric defect sources, their contribution would tend to be greater during a rapid oxidation than during a slow one in which lateral rearrangement of structural groups could take place in the plane of the oxide. This "annealing" would account for the superiority of the group C oxides in which the final oxidation was dry rather than wet. Since the grown oxide will contain more boron than phosphorus or antimony, it would be expected that stress produced failures would be more prevalent in the inital oxides in groups A and B than in groups C and D. It can be seen that this is indeed the case. The difference in oxide impurity content would also explain the variation in etch resistance between the n- and p-type samples since oxides on groups A and B will more highly stressed during cooling and thus more susceptible to etch-produced defects by the processes previously described. An additional factor in the quality of the etched layers is the more rapid etching of phosphorus-doped silica in comparison to boron-doped and pure silica. (See Ref E-22 and E-23.) Boron-doped SiO_2 etches somewhat faster than pure SiO_2 but would be less strained and so could be sounder after etching as shown by the data on the etched layers of groups C and D which differ considerably in boron content.

The data on the layers formed by sequences WD and DW provide additional verification of the proposed model for defect origins since they produce a disparity in the impurity profile in the oxide and in the interface structure. Consider first the layers grown by the WD sequence. These are expected to be somewhat freer from substrate related defects (particles and crystal imperfections) than the totally wet oxide since the dry portion of the cycle would be expected to "anneal" some of the particle or crystal defect sources of the oxide flaws. Thus, the WD sample in group C is expected to have fewer defects than the corresponding W sample as shown. The etch-back characteristics of C and D are comparable to those for the dry oxide as expected. Again, the heavily boron-doped sample has the best resistance to etch-produced defects, indicating a generally uniform and sound oxide with localized imperfections.

Superficially, it might be anticipated that the DW sequence would produce essentially the same results as the WD sequence. Reference to Figure E-6, however, indicates that the former case could produce an impurity distribution in the oxide which is significantly different from that of the other three cases in that it is not monotonically decreasing with distance from the $Si-SiO_2$ interface. The D, W, and WD oxidations produce impurity profiles in the oxide in which the best match to the thermal expansion characteristic of the silicon occurs at the oxide-silicon interface, but this is not the case in the DW film. This would account for the higher initial

densities found and the poorer quality of the etched layers. Also, from previous discussion, terminating with a wet (rapid) oxidation step may produce in the lower portion of the film a higher incidence of substrate-related oxide defects. This is thought to be an additional reason for the generally poorer quality of the etched DW films in comparison to the WD films, especially in the case of the etched group C sample.

The observations on the wafers obtained from commercial integrated circuit vendors were invariant with respect to source and support the proposed mechanism of mechanical stress as a principal origin of oxide dielectric defects.

Summary

Application of previously developed methods for the detection of dielectric defects to silicon oxides formed on silicon wafers has made possible a determination of the dependence of dielectric integrity on various factors involved in device fabrication. Most of the results can be consistently explained by a model which postulates the mechanical stress developed as a result of the thermal expansion mismatch between Si and SiO_2 as a principal source of dielectric failures by the mechanism of film rupture. Other possible defect origins are being investigated but have not been verified.

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APPENDIX F. INVESTIGATION OF METHODS FOR THE DETECTION OF STRUCTURAL DEFECTS IN SILICON OXIDE LAYERS

BY
P. J. BESSER AND J. E. MEINHARD

INTRODUCTION

Present information indicates that passivation oxide is subject to two general process-dependent structural anomalies; ionic impurities in sound oxide (device failure modes: high or unstable MOS gate threshold voltages, inversion in bipolar devices), and unsound oxide penetrated by local dielectric defects (failure mode: metallization to substrate shorts). Although the latter problem has been cited frequently in the past, it has received comparatively little intensive study, partly because of the lack of adequate detection methods and partly because of the urgency to resolve the ionic impurity problem. The incidence of oxide dielectric defects, often called pinholes, is now recognized as a serious reliability problem, particularly with respect to MOS gate structures, metal intraconnections over thinned oxide regions, and abrupt thickness transitions in the oxide. The structural discontinuities comprising such defects offer far less resistance to electrical discharge than sound oxide which is capable of supporting fields up to 10^{-1} V/Å as compared with breakdown fields of about 10^{-4} V/Å for air. MOS gate voltage parameters seldom involve fields in excess of 10^{-2} V/Å which is well within the dielectric capability of sound oxide but considerably higher than that of gaseous insulation at ordinary pressures. Thus, shorting may occur regardless of whether the overlying metallization has penetrated a crack or pinhole in the oxide.

A major purpose of this investigation was to develop and evaluate test methods for the detection of dielectric defects in passivation layers. Selection of methods was based on the following performance criteria: nondestructiveness, reproducibility, recordability, and convenience of use as a process screening technique. Previously described techniques, such as the high temperature HCl etch[1] or chlorine etching at around 900C[2][3], fall short of this goal in terms of convenience and nondestructiveness. Metallization techniques likewise are impractical and lack the resolution necessary for the accurate location of defects. Both methods were useful, however, in corroborating results obtained with the new techniques under study.

Additional objectives were to gain an understanding of the physical nature of the defects and to determine, if possible, their process origins. For example, the presence of fast-etching loci in grown silicon dioxide, as reported by Lopez[4], would appear to contraindicate etch-thinning procedures for adjustment of oxide thickness. Defects therefore may be classified as inherent or latent, and may consist of physical openings in the oxide (pores, microcracks), thin spots, foreign inclusions (e.g., glass-forming metal oxides), or abrupt variations in SiO_2 density. The latter three categories would be more vulnerable to HF attack (fast etching) than adjacent sound oxide, and more subject to electrical breakdown as well. Likewise factors contributing to the formation of dielectric defects would include the inherent mismatch in thermal expansion between the oxide and the substrate, as well as initial and subsequent

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processing irregularities. Some of these process origins are: etch undercutting of oxide due to mechanical strains originally present or to poor adhesion of photoresist, localized etch spots due to mask flaws or variations in photoresist quality and application, local excesses of dopants or contaminant particles capable of forming silicate glasses at oxidizing temperatures, high temperature attack of active metals on oxide layers, and mechanical flexing of wafers by repeated growth and unbalanced removal of oxide layers. Conceivably, therefore, the elimination of dielectric defects might involve scrutiny of a large part of the major processing operations - a very difficult task without the availability of simple, recordable defect test methods.

TEST METHODS

Direct observation of oxide dielectric defects is hampered by their small physical size (approximately 2 to 20 μ diameter), the high reflectivity of the silicon and oxide surfaces, the lack of inherent color contrasts, and the apparent absence of a characteristic morphology for differentiating dielectric defects from other defects which are dielectrically sound. It became evident therefore that a suitable test method would require a combination of visual enhancement and transmission of charge at defect sites. Two of the more promising techniques, electrophoretic decoration and electrochemical autograph, are described below, followed by other techniques of more limited application. Succeeding sections deal with intertest correlations and process applications.

Electrophoretic Decoration

This technique provides a functional test (transmission of charge) and a visible record of the oxide anomalies sought. A passivated wafer, whose reverse side is etched and connected to a dc circuit, as shown in Figure F-1, is immersed in a dissociable dielectric fluid and the circuit completed by a copper probe situated in the fluid above the oxide surface. A mechanical stage is employed to adjust the relative position of the wafer under the probe. With a negative polarity (10-100 v) on the wafer, electrolysis at oxide anomalies is observed, under low power magnification, as trains of fine bubbles (identified as hydrogen by gas chromatography) associated with the electrochemical decomposition of the fluid or of minute traces of dissolved water. Concurrently, anodic attack of the copper probe releases colloidal particles of insoluble oxysalts of copper which are propelled by the potential gradient toward the oxide defects. This was confirmed by chemical and electron beam microprobe analysis of deposited material. Instead of plugging the defects, the insoluble matter accumulates on the surface of the surrounding oxide, covering areas ~100 diameters larger than those of the original holes. Figure F-2 shows the decorations on a portion of a wafer after removal from the cell and drying. The deposits were readily removed by acid treatment. A photograph of a decorated defect, and a microprobe photo of Cu radiation corresponding to the decoration, are shown in Figure F-3.

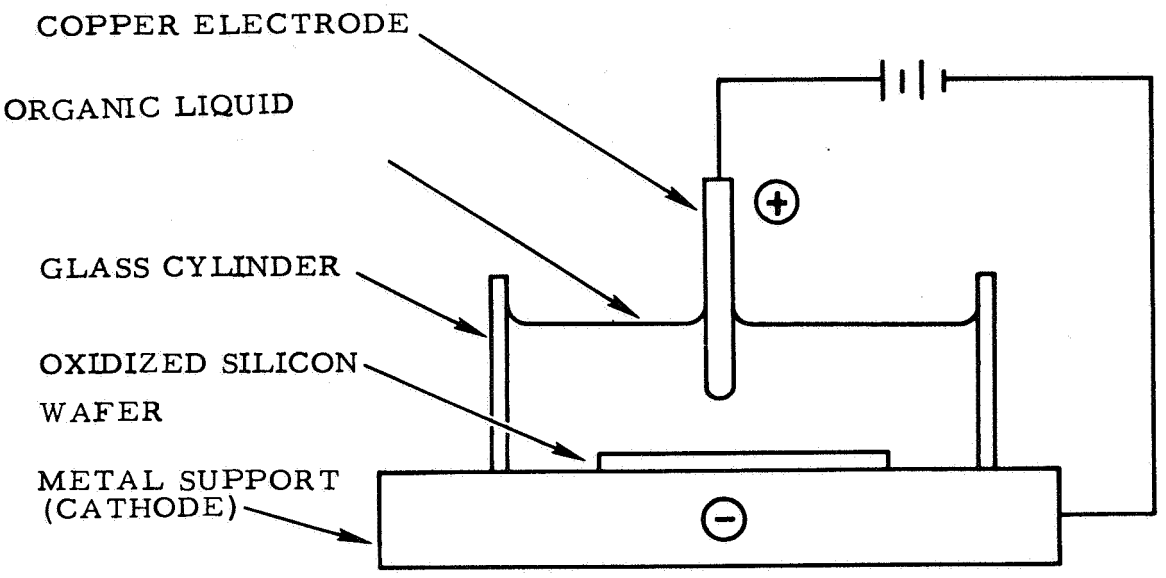


Figure F-1. -Electrophoretic Decoration Test Assembly

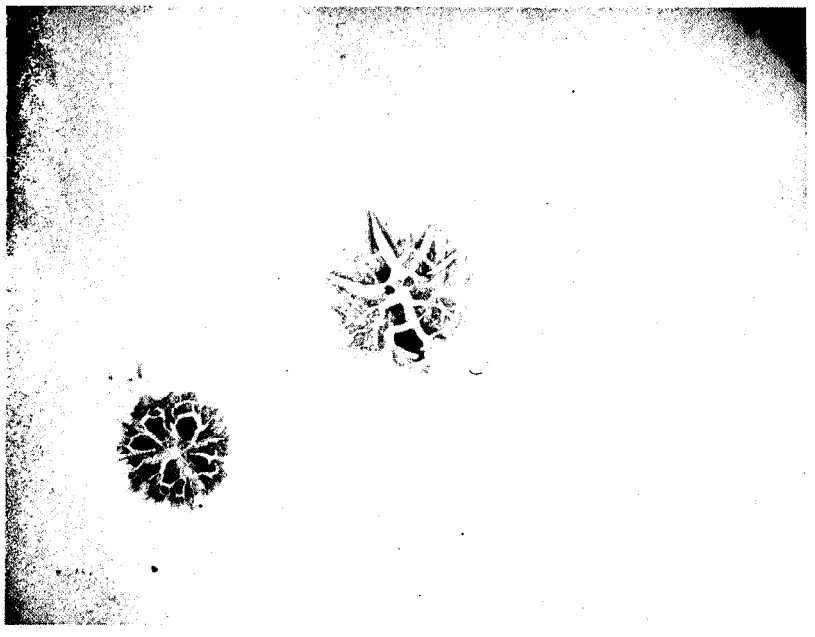
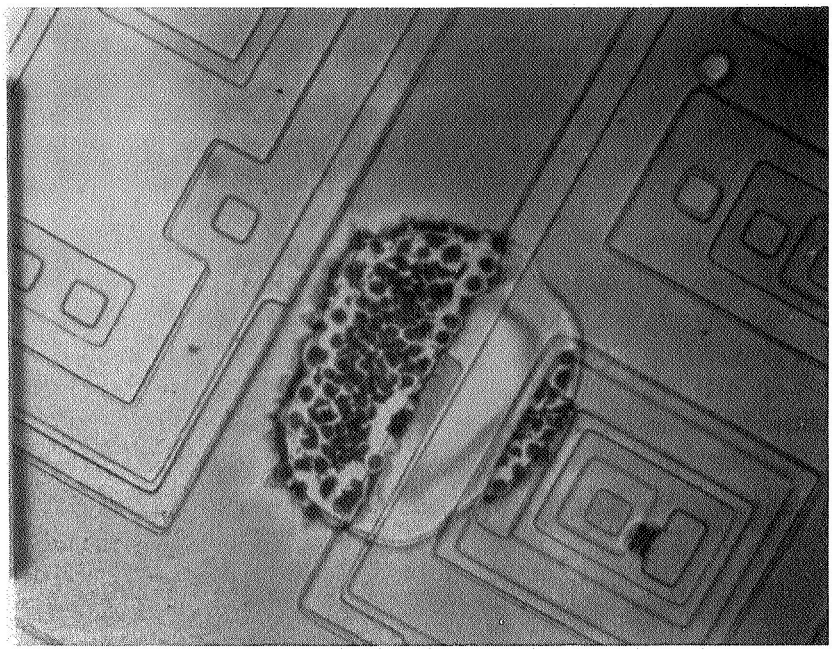
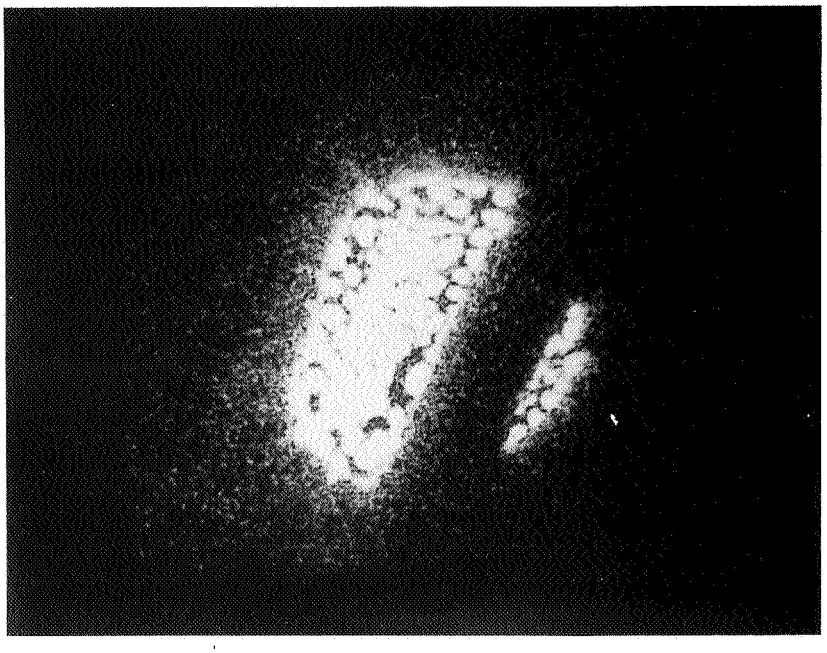


Figure F-2. - Oxide Defect Decoration After Fluid Evaporation. 100X



a. Photograph of decoration, 190X



b. Cu radiation from decoration

Figure F-3. - Photograph of Decoration and Cu Radiation From Electron Beam Microprobe of the Decoration

Verification of the method was obtained by correlation with other test methods. Reproducibility was checked by rinsing off the deposited material with dilute sulfuric acid and resubmitting the wafer to test. A typical sequence of this type on initial oxide is shown in Figure F-4. In its present form, this method employs a 20-point probe which decorates the complete wafer in 5-10 minutes. It is applicable as a pilot test and potentially useful as a screening test. The complete removal of copper by an acid wash has not yet been experimentally verified, and the potential gradient across the oxide and substrate has not been determined. The method is not yet completely qualified therefore as a nondestructive test. Further work is underway to characterize the nature of the decorated defects. Preliminary observations indicate that the decorated sites are actual pores in the oxide rather than regions of high conductivity.

In an earlier version of the test, attempts were made to achieve a visible record of the defects utilizing the electrolytic rather than the electrophoretic aspect of the reaction. A thin film of gelatin was applied to the wafer prior to immersion in the fluid. The electrolytically generated gas was trapped under the film causing delamination of the film from the oxide in the regions of gas evolution which revealed the characteristic oxide thickness color. The wafer could be removed from the cell with the film and trapped gases still intact. A photograph of a typical trapped gas pattern thus obtained is shown in Figure F-5. Subsequent tests, however, revealed a lack of reproducibility probably due to a nonuniform lifting of the gelatin film by the evolved gas. Various weakly acidic organic fluids such as acetone, isopropanol, and methanol are suitable for this process. Deionized and tap water were not found to be suitable.

Electrochemical Autograph

A simple electrochemical screening test for oxide defects is in the final stages of development. It can be applied to a wafer prior to final metallization or at any preceding process step, and shows promise of becoming a generally applicable technique for the location of oxide defects. It does not introduce metallic impurities and does not require large potential gradients. The method consists of making the silicon substrate an anode of an electrochemical cell and of revealing openings in the oxide by anodic oxidation of the electrolyte wherever it is in electrical contact with the underlying silicon.

The electrolyte employed consists of an aqueous solution of a benzidine salt (e.g., acetate or chloride) containing an organic nonsulfonated surfactant and a protective colloid. The function of the surfactant is to assist penetration of the electrolyte into small oxide pores. The protective colloid inhibits deposition of crystalline benzidine salts which tend to blur boundary definition. The colloid also promotes image sharpness by inhibiting lateral diffusion of dye. In principle other redox reagents will serve the same purpose as benzidine in this technique.

The electrolyte, soaked in a Millipore filter paper, is applied to the oxide surface and the assembly outgassed under vacuum. This treatment removes residual gas that might otherwise prevent pore penetration by the electrolyte. The assembly is then placed face down on a porous flexible support also soaked in electrolyte and situated on a stainless steel plate, as shown diagrammatically in Figure F-6. The purpose of the flexible support is to achieve conformal contact with the wafer surface,

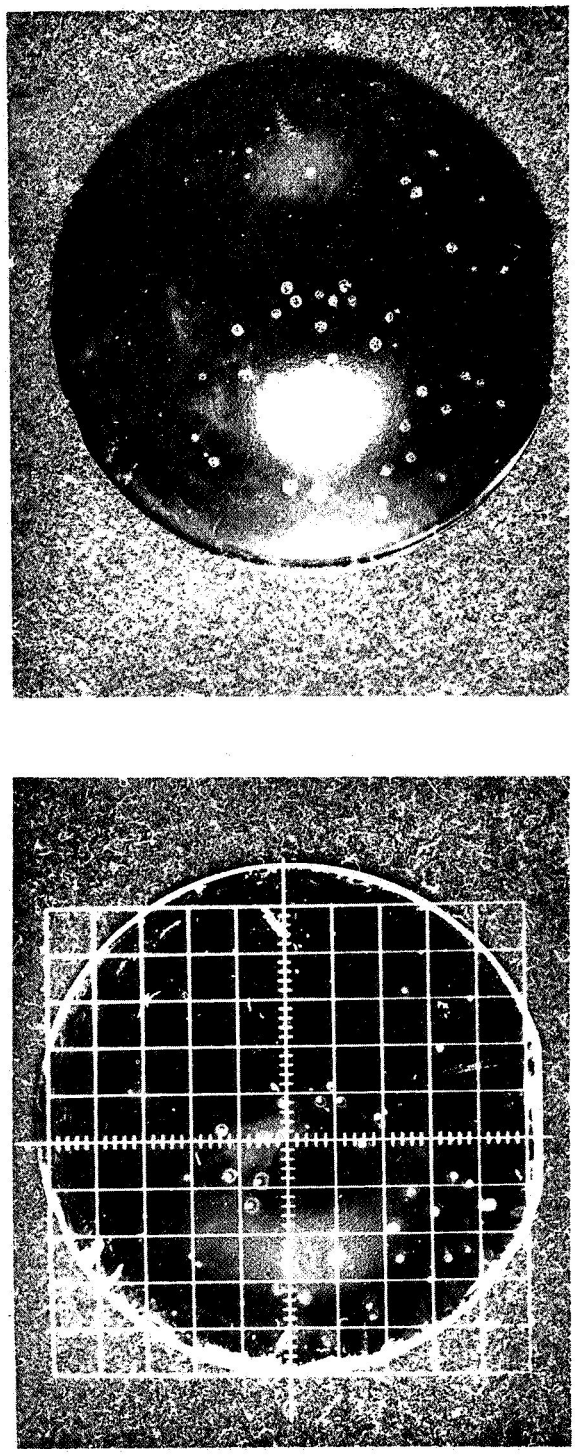


Figure F-4. - Sequential Electrophoretic Decoration of the Same Wafer

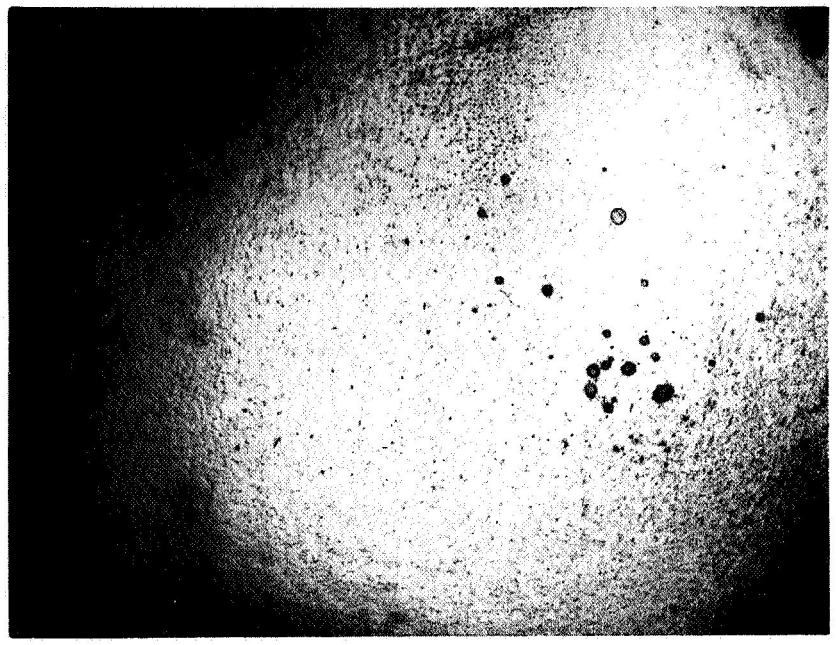


Figure F-5. - Trapped Gas Pattern Under Gelatin Film

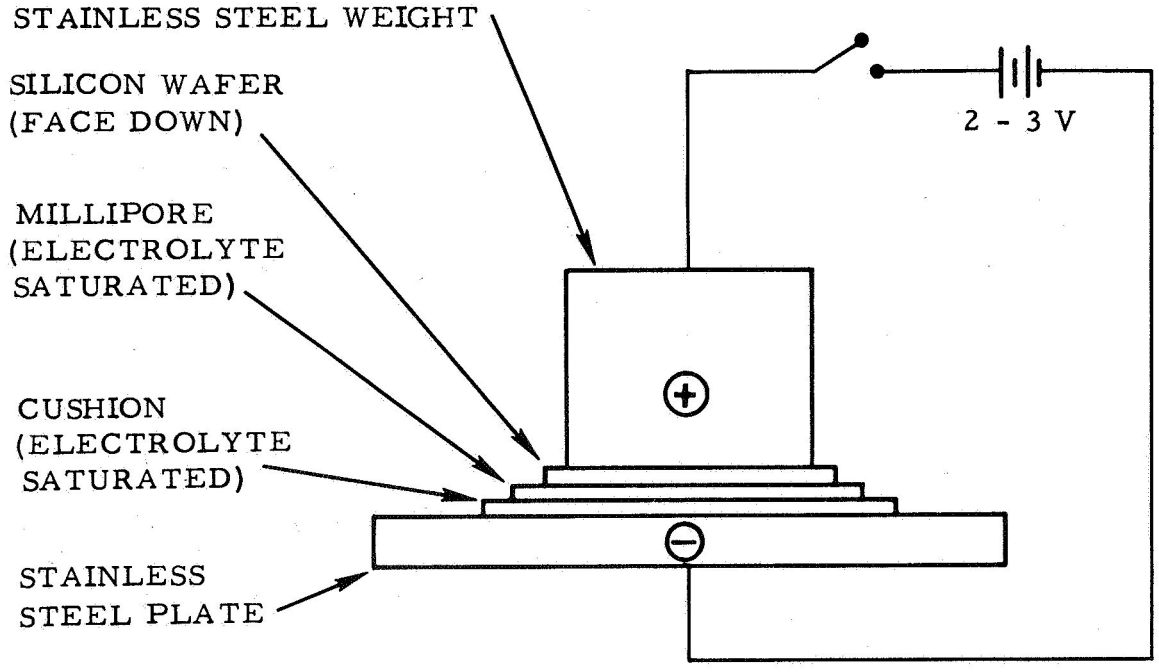


Figure F-6. - Electrochemical Autograph Assembly

which is not quite planar, and to minimize the possible transmission of a bending moment to the wafer through electrode pressure. The top stainless steel electrode, which is of sufficient mass to ensure intimate electrical contact between the assembled layers, is then placed on the oxide-free back (upper surface) of the wafer and external electrical connections made as illustrated.

Electrolysis is conducted at a potential of 2 to 5 volts for a 5-minute period. Anodic oxidation of the benzidine to a blue-black product stains the filter paper at points corresponding to openings in the oxide such as pinholes, contact and diffusion windows, and scribe lines. Following electrolysis, the apparatus is disassembled, and the Millipore filter paper is removed for microscopic examination and photography.

A photomicrograph of a typical wafer pattern after oxide removal prior to a diffusion step is shown in Figure F-7a and an enlarged view of the same pattern with an arrow indicating an oxide defect in Figure F-7b.

Substantial correlation has been obtained between this test and the electrophoretic decoration technique. Consecutive repeatability also has been confirmed many times. The detection limit is approximately 2 microns in hole diameter. This limit may be extended by more prolonged electrolysis. The wafer is easily cleaned from the electrolyte components with deionized water.

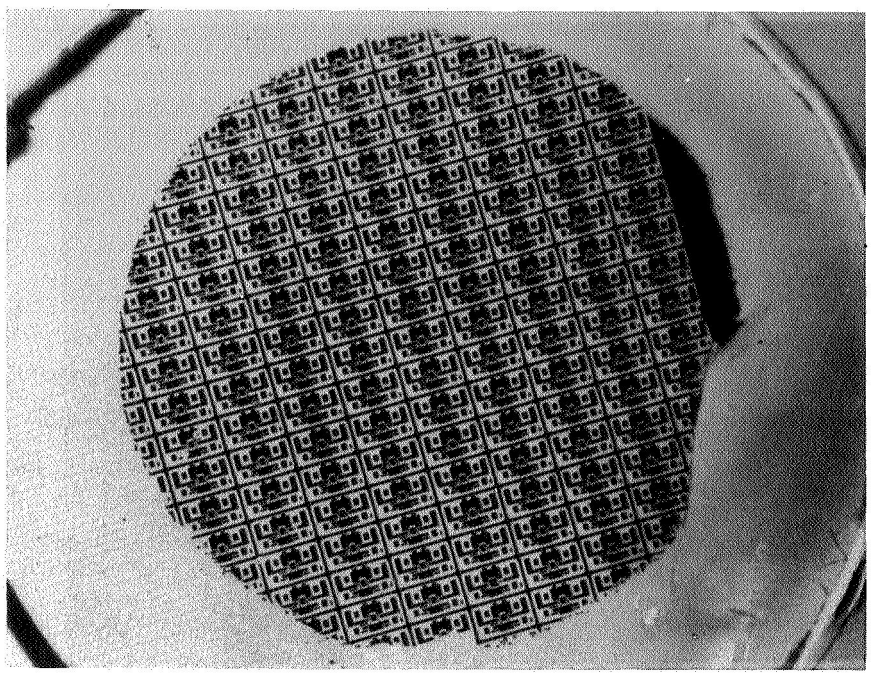
Electric Field Excitation Photography

Direct photographic recording of oxide defect sites was attempted using an alternating electric field to stimulate electron or photon emission from defect loci in or under the oxide placed in direct contact with a photographic film. Preferential exposure of the film was obtained, giving a light emission pattern that is developed only on oxidized wafers.

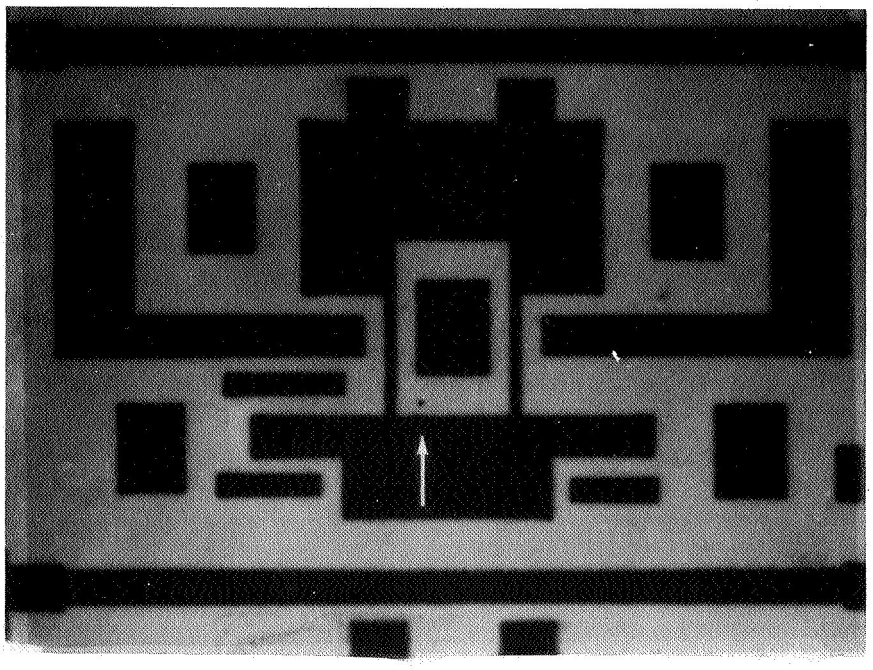
The field across the oxide and the silicon layers are unknown but may be high enough to damage device junctions in the silicon. Such damage would not necessarily occur only at oxide defect sites. Until direct evidence of non-destructiveness is obtained and the required exposure periods (1/2-2 hours) are substantially shortened, the method cannot be recommended as a screening test. It is a potentially useful tool in the investigation of oxide defect origins. Its correlation with the electric probe method is described in the following section.

Replicate Electron Microscopy

Although electron microscopy is impractical as a screening technique, it is capable of minute definition of surface morphology which may give clues to the process origins of oxide defects. The replica technique employed in this investigation involved the attainment of a large area replica. Such a replica can be used to study the original specimen after laboratory testing destructive to the original surface character. Thus, replicas made before and after a particular detection test can be examined to determine the effect of the test on the oxide.



(a)



(b)

Figure F-7. - Oxide Openings Displayed by Electrochemical Autograph Technique

The richness of detail produced by this technique poses a problem of interpretation. Only a very small percent of the observed structure is likely to delineate oxide defects capable of dielectric failure. Therefore, correlations of this technique with known sites of dielectric breakdown are especially important. Achieving such correlations, however, is a serious problem because of the minute field area covered at high magnification. Although many photographs were made, it was not possible to correlate unequivocally an observed structure with a dielectric anomaly. One correlation was made, however, by ordinary light microscopy of a replica prepared for for electron microscopy and is reported in the following section.

Microscopy

Observations by dark field, normal lighting (metallurgical illumination), and Nomarsky phase contrast were made in an attempt to develop a direct nondestructive procedure. Small defects in the oxide were readily observable at 500 to 1000 X. Covering an entire 1.25-inch diameter wafer by this method, however, is impractical because of the small field diameters (0.35 mm or 0.014 inch at 500 X; 0.17 mm or 0.007 inch at 1000 X) involved. Interpretation of observed structures also is difficult and requires correlation with other visual enhancement detection techniques. It is not yet possible to make any structural generalizations describing dielectric defects in the oxide. The method ultimately should be applicable to the inspection of single integrated circuit dice where topographical detail is available as landmarks. Automatic computerized scanning of whole wafers is foreseeable.

Preferential Etching

Chemical attack of silicon provides a direct visual enhancement of oxide holes where silicon is exposed. The etchant employed (25:3 HNO_3:HF) also corrodes the oxide to a significant degree, and probably causes a widening and deepening of the defects present as well as exposing silicon at fast etching sites as previously observed[4]. The test is therefore destructive. Defects are readily visible under dark field illumination at 500 X. The method suffers from the same limitations indicated above and is not applicable as a screening test. It holds promise, however, as a failure analysis test on defective integrated circuits. It also should be useful in stress-corrosion investigations of the origins of oxide defects.

Dye Autograph

This method was expected to locate oxide anomalies through dye or pigment color reactions similar to histological and biological staining techniques. The reasons for employing dyes are analogous in the two cases: to make morphological detail visible to ordinary light microscopy by the development of color contrasts. Although many experimental approaches were undertaken, no methods deserving continued investigation were found. The high reflectivity of the surfaces, and the chemical and physical inertness of the silica (in contrast to biological specimens) rendered ordinary staining methods ineffective.

Staining was attempted by applying soluble dyes, dye suspensions, pigment suspensions, in situ chemical reactions, commercial dye penetrants, and x-ray absorbers. Vacuum outgassing and pressurization were utilized as inoculation adjuncts, and visual enhancement was sought by applying monochromatic illumination and by ultraviolet excitation of fluorescent dyes.

Thermal Plotter

The infrared thermal plotter was considered a potential means of discovering "incipient" dielectric breakdown through an oxide defect covered with metallization. The heating effects associated with this phenomenon were found to be too small and too rapidly dissipated to be observed experimentally. Previously broken down loci dissipating approximately one watt (rms) were unambiguously detected and, almost without exception, could be related to readily discernible anomalies on the surface. Based on these negative results, the effort to detect incipient breakdown was discontinued.

Other techniques such as visual or photographic observation of defects in a low pressure gas discharge and luminescence of electrophoretically deposited phosphors were investigated but did not prove fruitful.

VERIFICATION OF METHOD

Inter-and Intra-Test Correlations

Verification of test methods under development required an independent proof relating analytical observations to anamolously low dielectric breakdown regions. Two techniques were used to induce dielectric breakdown: a bare metal probe in point contact with the oxide and vacuum-deposited metallizations on the oxide.

A potential was applied to the metal probe to break down sound oxide at known locations on the wafer. These were used as functional checks on other methods. Metallizations were deposited in the pattern shown in Figure F-8. The Al dots are 13 mils in diameter with an on-center spacing of 40 mils. Metal coverage is ~ 15 percent within the pattern boundaries.

The central test employed in this investigation was the electrophoretic decoration test. It was therefore essential to check its validity against dielectric breakdown distribution. Results employing the aluminized dot pattern are shown in Table F-1.

The results clearly indicate a correlation between defect density and dielectric breakdown. With only about 15-percent coverage by the dot pattern, a low coincidence with defects at low density is expected, as indicated for the first two samples. The high defect density in the third sample is reflected in the dielectric breakdown distribution.

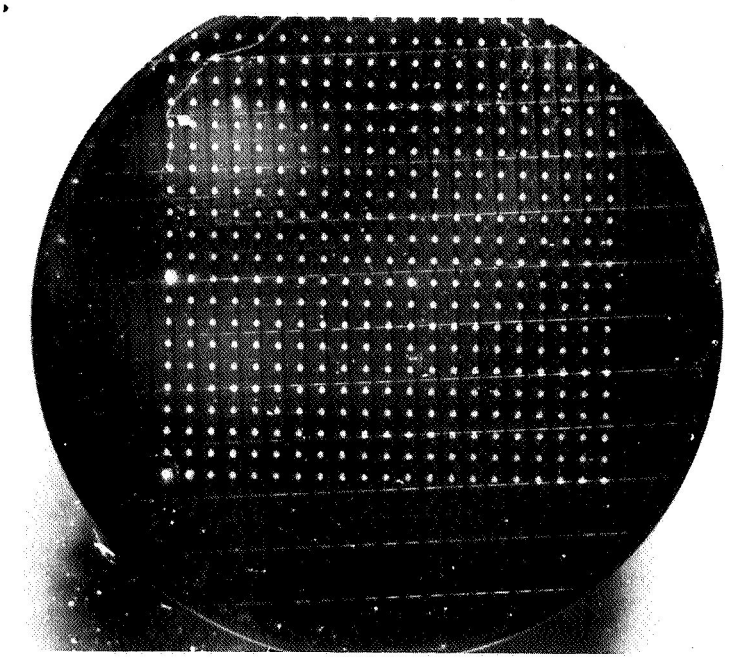


Figure F-8. -Metallization Pattern for Dielectric Breakdown Test

TABLE F-1
DIELECTRIC BREAKDOWN VS DECORATED DEFECT DENSITY

Wafer Description	Defect Density (cm^{-2})	Dielectric Breakdown Distribution
8000 Å Initial Oxide	< 5	% > 600V % > 500V % > 400V 72 89 100
4000 Å Initial Oxide	< 5	% > 350V % > 300V 0 100
Processed through contact oxide removal step, then 2000 Å of additional steam oxide regrown	400-600	% > 300V % > 200V % > 100V % > 40V 11 44 89 100

Further verification of the electrophoretic decoration technique was obtained on known breakdown sites deliberately introduced by the bare metal probe. Positive identification of the breakdown sites by decoration was obtained in every case.

Correlation of the electrophoretic decoration technique with electric field excitation photography also was obtained, as represented in Figure F-9. Not all of the defects decorated with copper salts are successfully reproduced in the decoration photograph. However, the number density of spots on the field excitation photograph was still higher than that detected by decoration and may be due to the presence of thin oxide spots not detected by the probe method. Further investigation is required to establish correlation limits.

Cross-correlation between the electrophoretic decoration technique and the electrochemical autograph technique was performed on two wafers with initial steam grown oxide. One wafer was first decorated and photographed, and then subjected to the electrochemical autograph test while the reverse sequence was followed for the second wafer. Comparison of apparent defects determined by the two methods resulted in a significant, but not complete, correlation between the two methods. Extraneous sites were observed by both techniques. The autograph sites which did not correspond to decorations were, in general, very minute and may have been experimental artifacts unrelated to oxide defects, or to oxide defects of a size beyond the limit of detection by the electrophoretic decoration method. The absence of autograph sites at some decorations may be due to incomplete wetting of the wafer by the autograph electrolyte, a problem that has persisted in this technique, or an indication of induced breakdown at thin oxide regions by the higher fields employed in the decoration test. At the time of this writing, significant improvement in electrochemical autograph pattern coverage has been achieved, and it is expected that the correlation between the autograph and decoration techniques will improve. Since the decorated defects have not been definitely characterized solely as physical openings in the oxide, some of the decorations may correspond to regions of normal oxide thickness but of high conductivity, which might not be detected by the autograph.

Evidence of the Nature of Dielectric Anomalies

Some characterization of the microscopic structure of a defect was obtained using a surface replica prepared for electron microscopy. A photo-micrograph of this replica under normal illumination (at $\sim$ 1000X) is shown in the upper photograph of Figure F-10. The centrally located oxide blemish (about 10 microns in diameter) in this photograph was indicated as a dielectric defect by the electrophoretic decoration method. The lower photograph shows the same defect after the decoration test. The oxide structure is seen to be relatively undisturbed by this treatment, but the underlying silicon has acquired a triangular etch-pit. Such etch-pits frequently have been observed after decoration testing. Since the silicon is at a negative potential during the test, the etch-pit formation cannot be associated with anodic oxidation. More detailed investigation may reveal that the etch-pits result from impurities or precipitates originally embedded in the silicon which act as precursors of the oxide defects and are expelled during the test. This result, plus the observation that deliberately induced breakdown loci are always detected by the decoration technique, apparently indicates that the test is not likely to introduce oxide defects where none previously existed, with the possible exception of unusually thin oxide regions noted above.

A preferential etch (25:3 HNO_3:HF) was applied to one of the two wafers used in the cross-correlation between the autograph and decoration methods. Considerable correlation between decoration sites and etch-pits in the silicon was found. However,

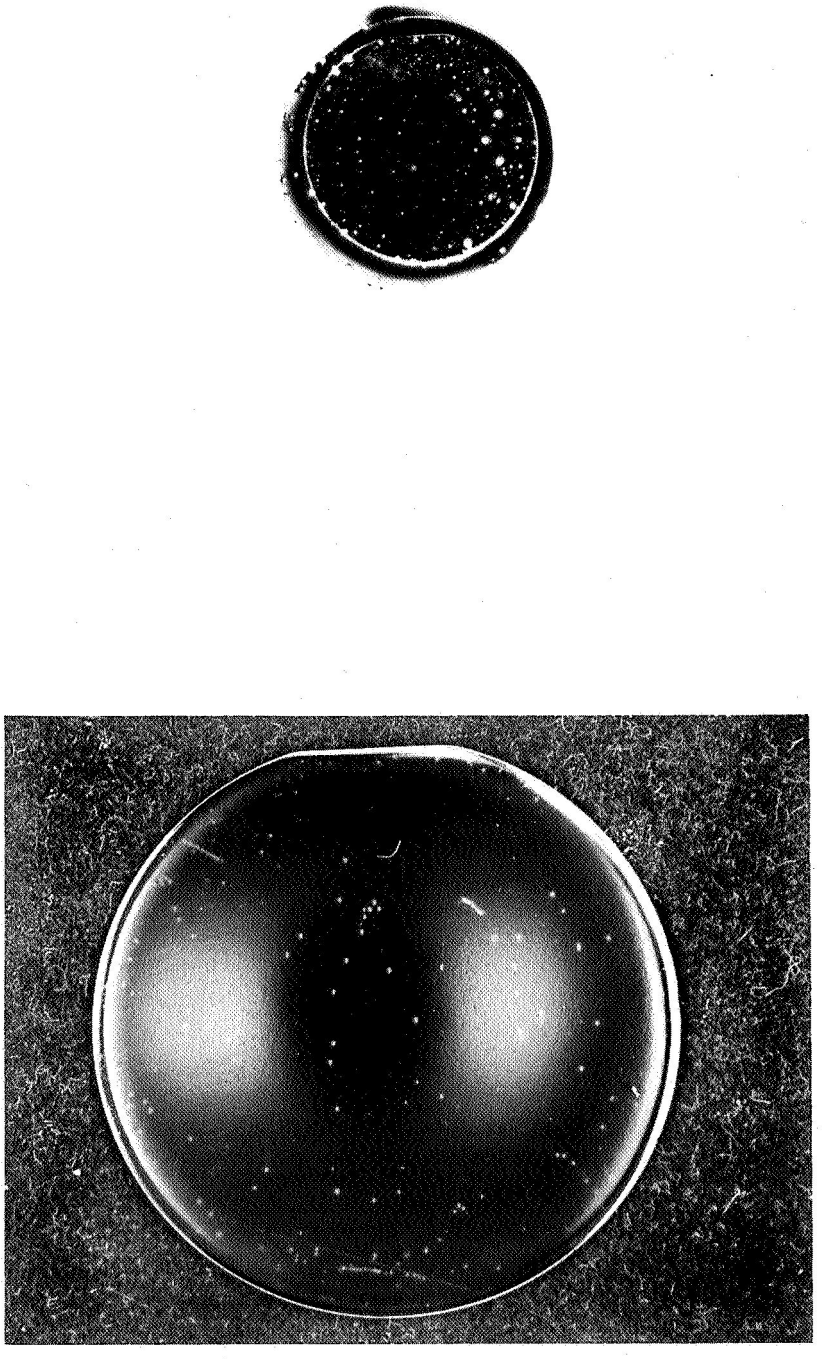


Figure F-9. - Top: Wafer Photographed by Electric Field Excitation; Bottom: Same Wafer Treated by Electrophoretic Decoration Method

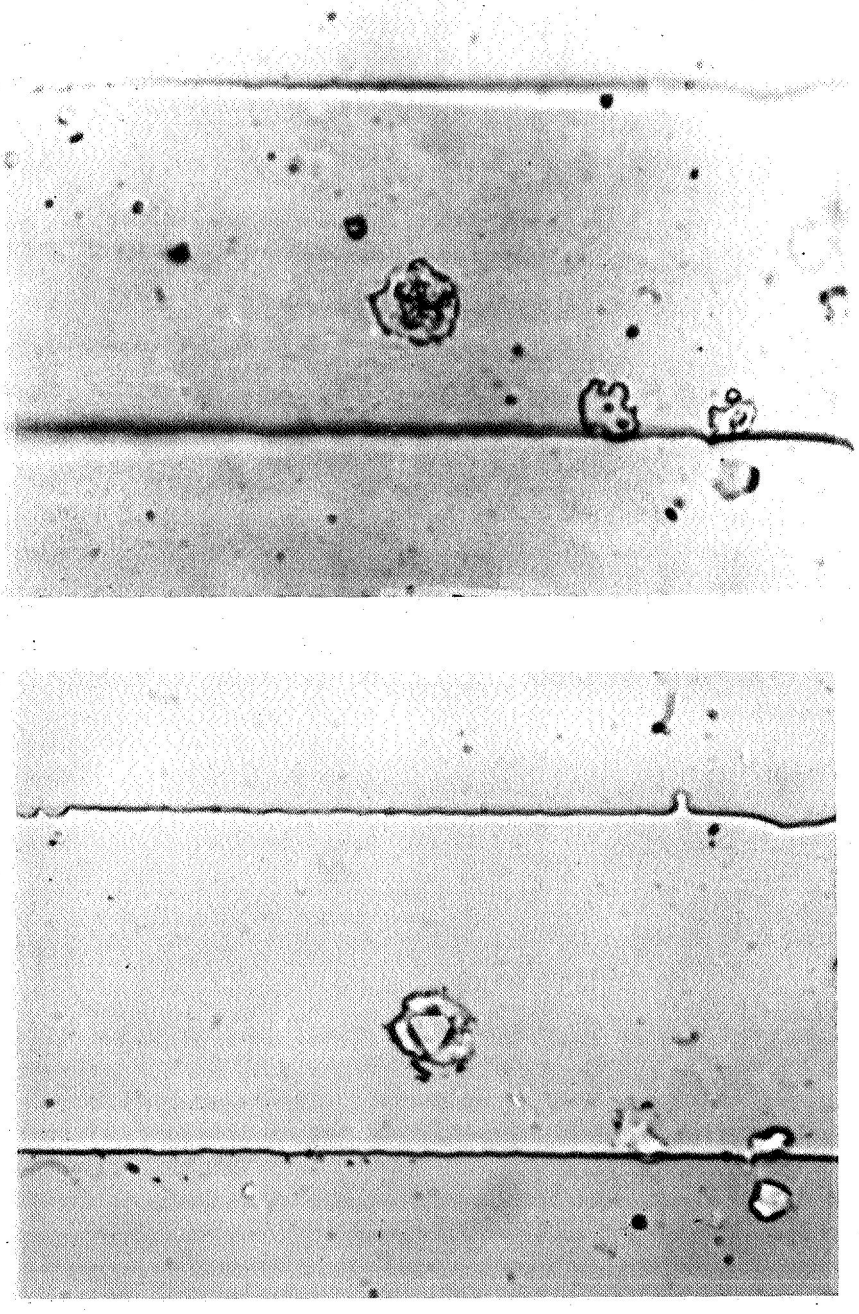


Figure F-10. - Oxide Defect Before (Top) and After Electrophoretic Decoration Test (Bottom). Top Photograph from Replica.
Parallel Boundary Interval: 42 Microns

since this etchant does attack the oxide to some degree, it does not resolve unambiguously the question of whether the decorated points correspond to actual oxide pores or to other anomalies such as fast-etching imperfections or thin spots.

The other wafer from the cross-correlation was subjected to a high temperature (1150 C, 10 minutes) HCl vapor etch which should not attack the oxide but preferentially etches any Si exposed by holes in the oxide. The etch pattern actually observed had a high degree of coincidence with the decoration pattern, but there were extraneous points in each case leaving the complete characterization of the defect nature unresolved.

Study by replicate electron microscopy is being continued in order to learn more about the physical nature of oxide defects and whether the electrophoretic decoration test induces defects at increasing probe voltages.

PROCESS CORRELATIONS

An additional objective of this program although somewhat ambitious for the allotted time and manpower, was at least partially fulfilled. The test data consisted principally of decorated defect counts and mechanical stress measurements on wafers selected at various stages of processing. The results are presented in Table F-2. Stress measurements were obtained from strain gage data, and Proficorder traces, before and after removal of one oxide layer from the wafer.

A number of inferences can be drawn from this tabulation. Most significant, perhaps, is the apparent gradual increase of both stress and defect density with processing (cf. wafer groups 1, 2, 5) and the defect healing effect of deposited oxide (wafer group 6). The deposition of uniform oxide, however, may be a continuing process problem, as indicated by wafer 6-B. The presence of an additional thermally grown oxide layer prior to final contact oxide removal was not very beneficial in reducing the defect count (cf. group 5).

The possible contribution of mechanical stress as a process origin of dielectric defects is somewhat subtle. A correlation of increasing stress with decreasing thickness (wafer groups 1, 3) is not accompanied by a corresponding increase in defect density in single-step oxides. Multiple-step oxides, however (wafer groups 2, 5), show a positive correlation between defect density and stress. To explain these observations, it can be postulated that mechanical stress induces dielectric defects through localized spalling of the oxide which serves to relieve a portion of the stress. Thus, highly stressed oxides, such as those in wafer group 5, would be under still higher stress at lower defect densities. The occurrence of such spalling would be expected to require a threshold stress for initiation which would decrease with increasing thickness of oxide. Thus, thinner oxides should tolerate higher stresses. Multiple heating and cooling, however, would be expected to increase spalling significantly through mechanical flexing (due to thermal expansion mismatch). Consequently, multiple-step oxides would be expected to display higher defect densities, as appears to be true from Table F-2.

TABLE F-2
OCCURRENCE OF DIELECTRIC DEFECTS AND MECHANICAL STRESS IN OXIDE AS A FUNCTION OF PROCESSING

Wafer Group	Description	Defect Density (cm^{-2})	Distribution	Average Stress (psi)
1A	8500 Å initial steam grown oxide	< 5	Random	29,000
1B		< 5	Random	
1C		5-10	Random	
2A	8000 Å steam grown in	15	Random	39,000
2B	2000 Å increments	45	Random	
2C		25	Random	
3A	4000 Å initial steam grown oxide	< 5	Random	38,000
3B		< 5	Random	
4A	8500 Å - 2000 Å steam grown after first diffusion	< 5	Random	40,000
4B		< 5	Random	
5A	Wafers after contact oxide removal step + additional steam grown oxide	90-100	Almost all along grid lines and at diffusion windows	62,000
5B		400-600		
6A	Wafers after contact oxide removal step + additional deposited oxide	1-2	Random	
6B		2-4*	Random except where deposited oxide very thin; one area > 2000 cm^{-2}	

*Excluding high density region of thin deposited oxide.

Probably most of the inferred spalling does not produce dielectric defects directly, but small surface pits. Such pits would be especially vulnerable to etchant attack at later processing steps because of localized high surface energies. It would be possible therefore for such pits to grow into dielectric defects under succeeding chemical treatments. This conclusion is suggested by comparison of wafer groups 2 and 5. The former group experienced no intermediate chemical treatments, and the average defect density is only slightly higher than single-step oxide of the same thickness.

All of the data in Table F-2 were obtained on nonepitaxial wafers. Measurements on oxidized epitaxial layers have shown that the defect density and stress in thermally grown initial oxides ~ 8000 Å thick are not significantly different from those of oxides grown on nonepitaxial surfaces.

CONCLUSIONS

The electrophoretic decoration test provides a recordable, reproducible test for sites of anomalously low oxide dielectric strength. The test was checked by independent dielectric breakdown measurements and was used extensively in seeking process correlations with the incidence of dielectric defects. The test provides enormous visual magnification of the defects which are estimated from optical microscopy to be pores a few microns in diameter. Optical observation of a defect site before and after the probe test indicated that the test is not destructive to adjacent oxide although regions of thin oxide may be vulnerable to this treatment as suggested by other test correlations.

The electrochemical autograph test has overcome early problems of technique and is now capable of providing completely reproducible replicas of openings in oxide layers. It does not provide any appreciable magnification but appears to be nondestructive and noncontaminating. Complete correlation with the decoration technique has not been achieved but is expected to improve with present refinements and the continued characterization of oxide defects.

The contact photography test shows promise, but additional development and correlation will be needed before it can qualify as a useful screening or detection technique. The other methods and approaches that were investigated in some cases assisted in the verification of techniques and the interpretation of results, but have not appeared promising enough as screening tests to warrant continued development.

The decoration and autograph techniques are most applicable to testing at the wafer level. Although either is potentially available for use at any process stage, they are more efficiently applied in a complementary manner. The decoration technique is generally superior when applied to an oxide with no intentional openings (i.e., initial oxide or after a diffusion-oxide growth step), whereas the electrochemical autograph technique is more convenient when applied to a wafer with diffusion windows, grid lines, or contact windows opened in the oxide to provide a reference pattern for the location of defects on the autograph. The resolution of the methods is unknown but is at least of the order of a few microns.

Analysis of the test observations indicates an increasing incidence of dielectric defects with processing. The results also showed that deposited oxide is effective in reducing such defects but may be a difficult process to control. Evidence that residual mechanical stress in the oxide plays a significant role in the incidence of defects was obtained. Interpretation of this evidence led to an oxide spalling hypothesis as a possibly significant source of defect sites. It was also concluded that high stresses associated with thinner oxides do not necessarily portend increases in defect density. No particular processing step was indicated as a predominating source of dielectric defects.

Continued investigations are expected to reveal more clearly the physical structure of the observed defects and their process origins. Further examination of the nondestructive and noncontaminating aspects of these tests, and additional intercorrelation of test results, also are needed to define completely the limits of applicability and resolution of these methods.

Acknowledgements

Valuable suggestions and experimental contributions were made by the following: J. L. Kersey, J. P. McCloskey, C. G. Jennings, C. W. Scott, and S. Merrill.

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APPENDIX G. ELECTROGRAPH METHOD FOR LOCATING PINHOLES IN THIN SILICON DIOXIDE FILMS

BY
J. P. McCLOSKEY

I. INTRODUCTION

The electrochemical procedure (Ref 1) described in this paper enables simple nondestructive determinations of the precise location of pinholes or other oxide anomalies in thin dielectric material that has been superimposed on and is in contact with a conductive substrate base. The basic principles of the method were first disclosed in a presentation by P.J. Besser and J.E. Meinhard (Ref 2). The particular application presently described relates specifically to a technique used for locating oxide anomalies in thermally grown silicon dioxide passivation layers formed on both phosphorus and boron doped silicon wafers. A need exists in the industry for locating the surface defects at an early stage in production, since electrical failures subsequently occur when vacuum deposited interconnects placed over the holes are short circuited to the conductive substrate beneath. If the faulty areas could be located in the early processing stages, great cost savings and improved reliability would be realized.

An apparatus and technique for carring out the electrograph method is given in detail in Scott (Ref 3). This apparatus could very well be used to advantage for the present application if a sensitive pressure gage were included to permit accurate control of contact pressure and thereby prevent possible damage to the wafers. The objective of the method, as described in (Ref 3), is to obtain qualitative identification of surface components by anodic dissolution in order to chemically transfer small amounts of the surface elements to a suitable medium, usually paper. Distinctive color reactions then occur at specific areas reflecting the compositional differences in the surface. The present electrograph method, however, utilizes a different principle in that a colorless organic reagent, namely benzidine, is anodically oxidized to a colored product only at conductive sites, and does not form a colored compound with any reacting species dissolved from the surface. Since conductive sites represent areas of exposed substrate, the method is conveniently applied to the location of holes in passivation layers.

Experimental

Apparatus. - The apparatus used (see Figure G-1) consists of an electrochemical cell using an aqueous acidified solution of benzidine hydrochloride as an electrolyte. The cell is provided with a supporting stainless steel cathode, 1.5 inch in diameter by 1.5 inch high or slightly wider than the 1.25 inch silicon safers electrographed, and an anode of the same material, 1.0 inch in diameter by 6 inch in length, or slightly smaller in diameter than the wafers. As a support pad, a soft cloth such as felt, velvet, certain broadcloths and the like, proved satisfactory. Plain white "Millipore" membrane filter papers were used for recording the electrographs. The 47 mm diameter papers with a 0.45 micron pore size furnished excellent results for the 1.25 inch silicon wafers.

*Journal of the Electrochemical Society Vol 114, No. 6, June 1967

Procedure. - Cover the top of the cathode base of the electrograph assembly with a soft cloth pad. Add the benzidine-hydrochloride electrolyte dropwise to the pad until it is completely saturated with the reagent. Immediately place a suitable size membrane filter paper saturated with the electrolyte on top of the pad. The membrane paper may be conveniently saturated by immersing it in a small petri dish containing the electrolyte. Add a few drops of electrolyte to the paper after placing it on the pad to ensure complete saturation. Immediately place the silicon wafer, oxide surface down, on top of the membrane paper. The oxide layer of the wafer should have previously been degassed by immersing, oxide surface up, in a petri dish containing sufficient electrolyte to cover the wafer, and evacuating for 5 minutes or longer under a vacuum of at least 20 mm of mercury. The evacuation step removes entrapped air from pinholes in the oxide and fills them with electrolyte. Place the anode rod on top of the conductive side of the wafer. Remove all excess electrolyte from around the anode base using an absorbent paper, such as a Millipore pad. If the excess electrolyte is not removed, it will tend to cause external short circuits around the wafer. Apply sufficient potential to produce a current of about 1 milliampere (usually about 5 to 10 volts) at the start, and maintain at this voltage for 5 to 10 minutes. Turn off the power supply, disassemble the apparatus, then remove the membrane paper for microscopic examination. Open areas in the oxide will be replicated on the paper with black markings or patterns corresponding exactly in size and shape to a mirror image of the conductive areas present in the wafer.

If repetitive electrographs are to be made of the same wafer, place the previously electrographed wafer in a large plastic beaker cover, preferably Teflon. Cover the wafer with a few ml of 6NHCl and allow 2 to 3 minutes for reaction. Rinse well with pure water to remove most of the benzidine hydrochloride. Repeat this operation once more. Cover the wafer with a few ml of 0.5 percent HF etchant and allow to react for exactly one minute. This treatment removes about 25 angstroms of silicon dioxide in this time period and should be sufficient to remove all of the oxide formed during the electrographing process. Rinse well with pure water to remove the etchant and reaction products. The wafer is now ready for producing another electrograph. If, however, the wafer is now to be returned to the production line, the final pure water rinse must be of 18 megohm or better quality.

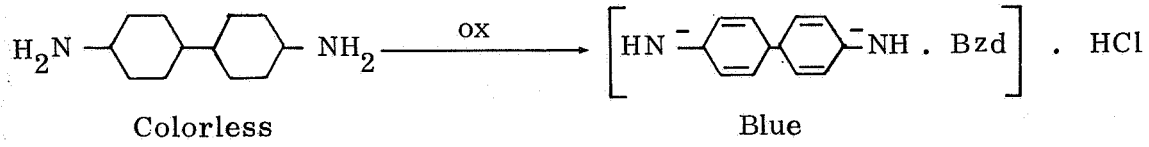
Preparation of Reagents

Benzidine-hydrochloride electrolyte. - To a small beaker add 50 ml of pure water, 10 ml of concentrated hydrochloric acid and 10 grams of ACS grade benzidine. Warm on a hot plate until completely dissolved. In another beaker prepare a 5 percent solution by adding 5 grams of gelatin to 100 ml of boiling water. Boil for three to five minutes. Combine and mix the contents of the two beakers. Filter through a Whatman No. 40 filter paper into a one liter dark glass bottle. Dilute the filtrate to approximately one liter. Stopper bottle then invert to mix well. The reagent may be used for long periods of time if filtered each time before use.

Hydrofluoric acid etchant. - Prepare an approximately 0.5 percent hydrofluoric acid etchant solution by diluting 10 ml of 48 percent hydrofluoric acid to about one liter with pure water in a plastic bottle.

Discussion

Benzidine in acid solution can be oxidized electrochemically to a blue oxidation product (Ref 4), in accordance with the following chemical reaction:



Colorless Blue

The above sensitive reaction is the basis of the electrochemical method described in this paper.

The simplified drawing of Figure G-1 illustrates the principle of the technique as applied to the determination of the location of conductive areas or holes through the silicon dioxide dielectric of silicon wafers. When a suitable anodic potential is applied to the silicon wafer, oxidation of the colorless benzidine occurs only at conducting areas such as at unwanted pinholes, etched microcircuitry and the like. The dark blue to black oxidation product formed at the conductive sites produces markings or patterns on the paper having the same size, shape, and location as a mirror image of the conductive areas of the wafer electrographed.

Figure G-2 is a photograph of an electrograph prepared on a "Millipore" type membrane paper. The silicon wafer electrographed contained 280 complete integrated circuits etched into the silicon dioxide passivation layer. It will be noted that the uniformity of the pattern is broken in two areas, one to the right of center and the other in the upper left hand area. Successive electrographs duplicated the same incomplete pattern in the identical areas. The broken pattern areas represent faulty etching of the microcircuitry patterns in the oxide produced during processing of the wafer. A faulty circuitry pattern, pinhole or other oxide anomaly recorded on an electrographed membrane is not considered as such until it has been duplicated at least once.

Figure G-3 is a photomicrograph (50x) of one of the individual integrated circuits selected from the electrograph shown in Figure G-2. The pinhole designated by an arrow illustrates the appearance of an oxide anomaly of this type when observed by microscopic examination of an electrograph.

Figure G-4 is an electron micrograph replica of an oxide anomaly on an actual wafer magnified 5000 diameters. The anomaly on the wafer was located by means of the electrograph shown in Figure G-3.

During the course of the development of the electrolyte for the process, the benzidine was first dissolved in a slight excess of acetic acid. It was later discovered that when hydrochloric acid was substituted for the dissolution of the benzidine, a dark blue to black pattern was achieved instead of the light blue color resulting with the former acid. To further improve on the quality of the electrograph produced, a protective colloid such as gelatin was incorporated into the electrolyte to inhibit crystallization of the benzidine and thereby enhance the definition obtained.

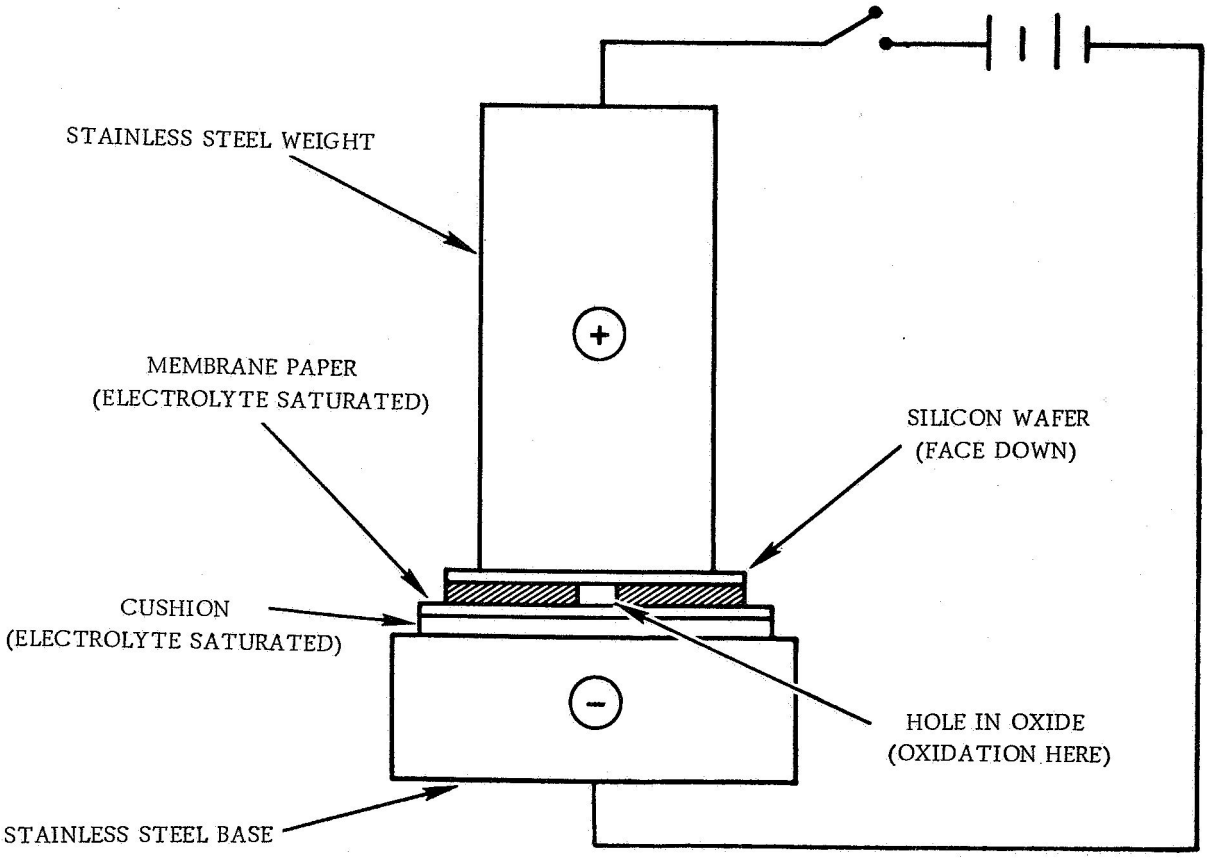


Figure G-1. Electrograph Assembly Diagram

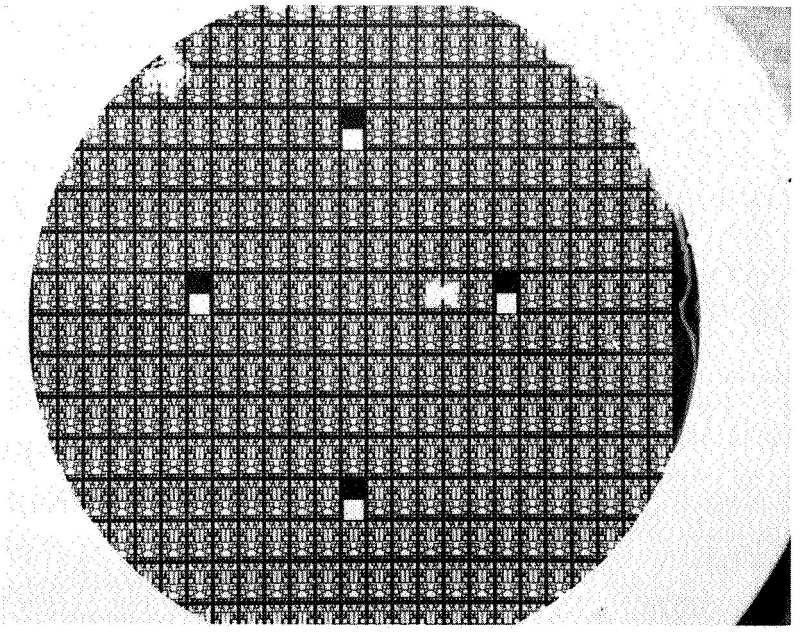


Figure G-2. Electrograph of Silicon Wafer Containing Etched Microcircuitry Patterns

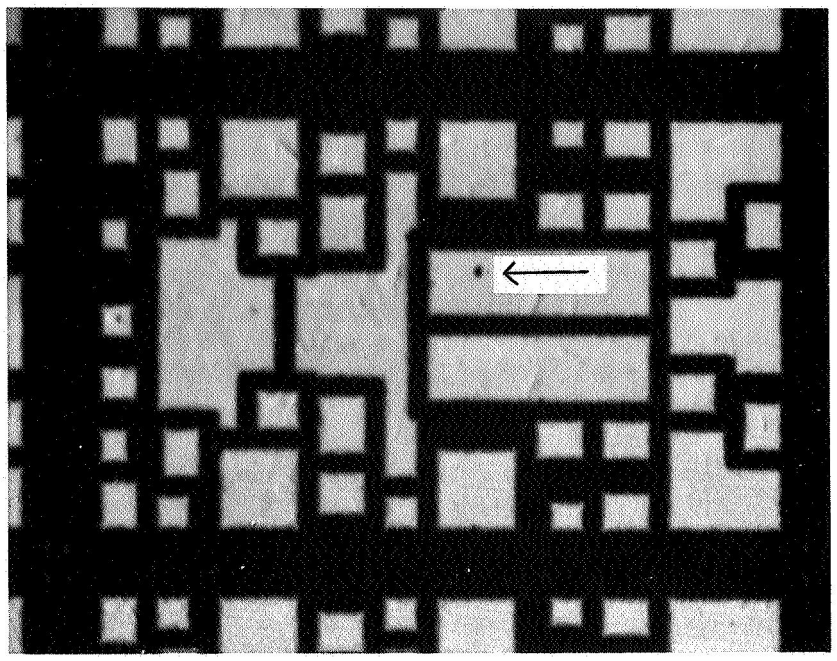


Figure G-3. One of Individual Integrated Circuits of the Electrograph of Figure 2 Showing Pinhole Location

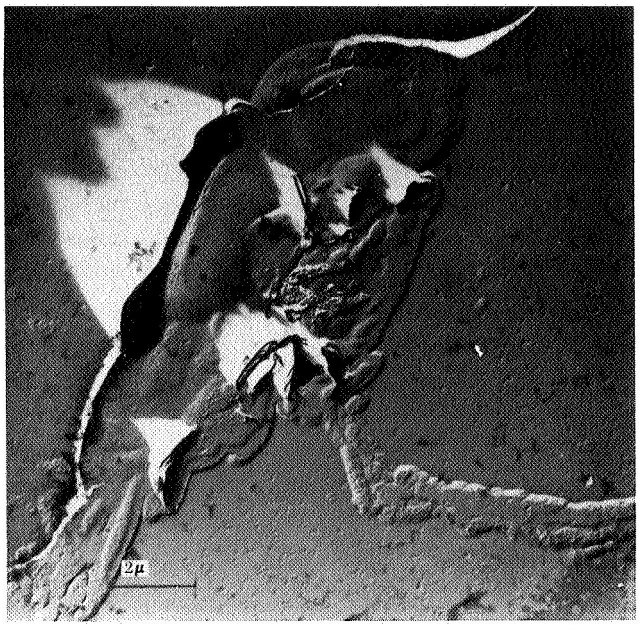


Figure G-4. Replica Electron Micrograph of Oxide Anomaly Located by Means of the Electrograph Method

Successive Electrographs

When a silicon wafer is electrographed, it is made the anode of an electrochemical cell and therefore some anodic oxidation of the exposed silicon occurs. If a second electrograph of the same wafer is attempted, no dark areas will form on the membrane paper since the formerly conductive sites are now covered with a thin oxide film. Chemical tests indicate that this developed oxide has an approximate thickness of about 25 angstroms. In order that successive electrographs may be processed on the same wafer, a mild etchant was developed which would remove this ultra-thin oxide without serious attack of the main passivation layer. The etchant found suitable was an aqueous 0.5 percent hydrofluoric acid solution. Figure G-5 shows the relationship between the thickness of silicon dioxide removed by the acid per unit contact time. It will be noted that the etching rate was linear in the time interval studied. The data for preparing the graph were obtained by treating a wafer having a silicon dioxide passivation layer of approximately 8500 angstroms thickness, with sufficient etchant to just cover the oxide layer side for successive one minute intervals. The amount of dissolved silicon in the etchant was then determined by a spectrophotometric chemical procedure developed for this purpose. The thickness of the oxide removed was then calculated from the micrograms of silicon dissolved in the etchant, the measured surface area in cm^2 and an assumed density of 2.15 for the silicon dioxide.

Summary

A simple nondestructive electrograph procedure has been developed for locating pinholes or other oxide anomalies in silicon dioxide passivation layers of silicon wafers. The method is most suitable for the determination of oxide anomalies in silicon wafers that contain etched patterns, such as for microcircuitry, which serve as reference guide lines in establishing the precise coordinates of the defects in the passivation layer. It is estimated that pinholes as small as 1000 angstroms in diameter can be located by the method.

The electrograph procedure described should find applicability in the determination of surface defects in any thin dielectric material that is superimposed on and is in contact with a conductive substrate base. For example, it should be possible to determine surface defects in silicon nitride dielectric over silicon, germanium oxide over germanium, aluminum oxide over aluminum, and many others.

Acknowledgements

The author wishes to acknowledge the help derived from useful discussions with Drs. J.E. Meinhard and P.J. Besser, during development of the process. He also wishes to thank Dr. R. Nolder for the replica electron micrograph shown in Figure G-4. Also, Mr. J. Kersey is thanked for preparing the photomicrographs of the electrographed membrane papers.

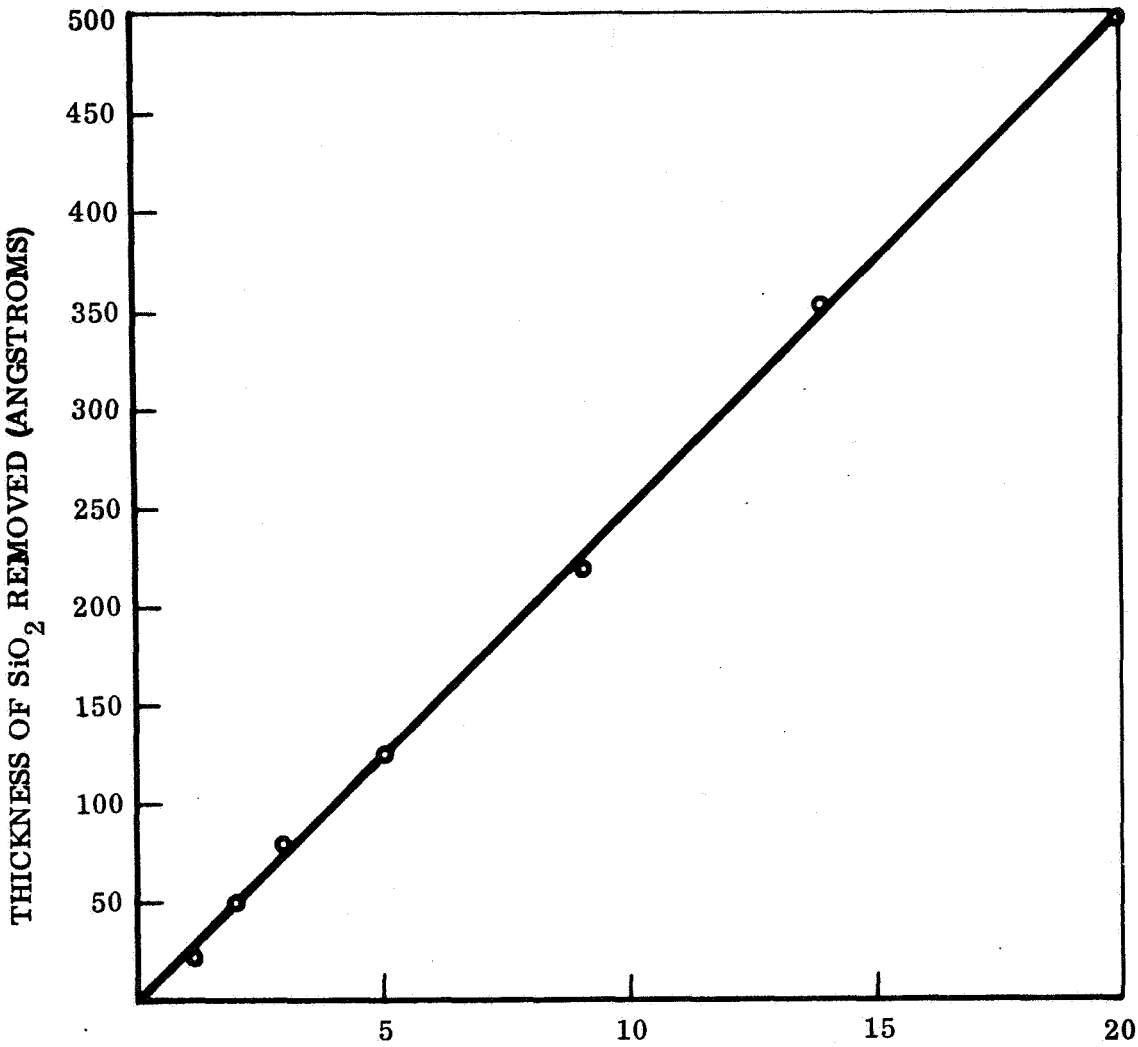


Figure G-5. Etching of Silicon Dioxide
With 0.5 Percent Hydrofluoric Acid

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APPENDIX H. EVIDENCE OF MECHANICAL STRESS AS A CAUSE OF DIELECTRIC DEFECTS IN SILICON DIOXIDE LAYERS

The presence of compressive stress in room temperature specimens of silicon dioxide grown on silicon at elevated temperatures has been previously recognized (Ref H-1). The effect of this stress has been considered insufficient to affect the band gap and, therefore, the performance of planar silicon devices passivated by such oxide layers (Ref H-2), and correlations with other effects, such as the presence of interface surface states, have been regarded as purely conjectural (Ref H-3). More recently the existence of residual mechanical stress in oxide layers grown on silicon has been confirmed (Ref H-4), and evidence has been advanced implicating this stress in the formation of structural defects in the oxide that are susceptible to dielectric breakdown under the influence of a potential gradient (Ref H-4, 5). Such defects have the practical effect of severely limiting the fabrication of large area planar arrays on a single silicon chip. Until now no single definitive experiment associating oxide dielectric defects with mechanical stress has been performed.

Compressive stress in grown silicon dioxide layers originates in the fact that the coefficient of linear thermal expansion of silicon is a factor of $\sim$10 higher than that of vitreous silica, and in the fact that oxide layers are grown at temperatures $\geq$1000 C followed by cooling to room temperature. Therefore, an etching test for defects on freshly grown oxide prior to cooling, followed by a decoration test (Ref H-4) of defects present after cooling, should yield a direct indication whether a correlation exists between dielectric defect incidence and thermal contraction-induced mechanical stress.

Eight mechanically polished silicon wafers with (111) surfaces were oxidized in a conventional processing furnace in a 1:1 O_2/N_2 atmosphere. Water vapor was carried by the O_2 stream from a reservoir maintained at 100 C. The treatment was continued for 1.5 hours at a temperature of 1150°C producing 8000Å vitreous oxide layers as determined subsequently be conventional optical interference technique. Water injection then was discontinued and HCl gas introduced into the N_2 line at a flow rate sufficient to provide a 0.1 mole ratio in the process gas. However, residual water in the system was present during this treatment. Vapor phase etching in this ambient was continued for ten minutes followed by a forty-minute flush with N_2 alone. Wafer temperature was held constant within $\pm$0.5 C during the entire sequence, after which the oxide-coated wafers were cooled to room temperature in an inert ambient. Dielectric defects in the oxide layers of each wafer were revealed by a previously developed (Ref H-4) electrophoretic decoration procedure. The defect locations appear as roughly circular deposits as shown in Figure H-1. After photographing and counting the defects on each wafer, the decorations were removed with an acid rinse and the vitreous silica layers with hydrofluoric acid. The thoroughly cleansed wafers were then examined microscopically for etch-pits that may have formed in the silicon during the HCl treatment.

The results of electrophoretic oxide defect decorations are given in Table H-1. However, in all of the wafers only one etch-pit in the silicon was found by microscopy after removal of the oxide layers. A photomicrograph (Nomarsky phase contrast) of the etch-pit is shown in the center area of Figure H-2. This etch-pit corresponds to

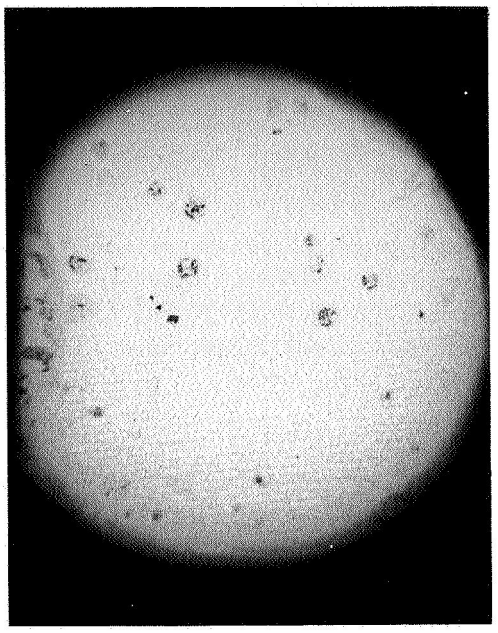

Figure H-1. - Oxide Defect Decorations on Silicon Wafer Specimen No. 4 of Table H-1 (outer diameter 2.3 cm).

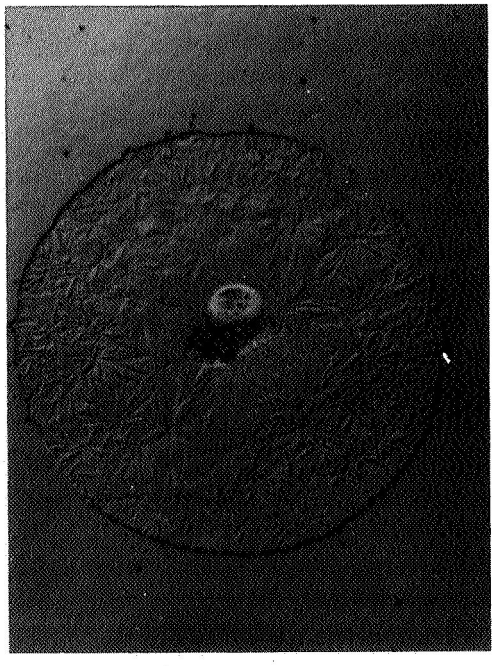

Figure H-2. - Etch Pit in Silicon (center) and Surrounding Structure (outer diameter 600 microns).

TABLE H-1
OXIDE DIELECTRIC DEFECTS LOCATED BY ELECTROPHORETIC DECORATION*

Wafer Specimen	Total Defects
1	33
2	27
3	15
4	24
5	28
6	18
7	13
8	27
Total	195

*Procedure given in Reference H-4.

one of the total of 195 decorated spots and may have originated from one or more lapping grits originally embedded in the wafer. At present, the crow-foot structure surrounding this pit is an unexplained experimental artifact. However, this pattern has been observed previously (Ref H-6) in studies of HCl etching at 1150 C through oxide "pinholes" deliberately introduced by photolithographic procedure. In these previous studies a five-minute rather than a ten-minute treatment with HCl was used. The structure appears to adopt a three-fold symmetry pattern induced by the (111) surface orientation and may be a region of redeposited (epitaxial) silicon. No evidence of the more characteristic triangular etch-pits was found.

It is clear from the foregoing results that there is a better than 99 percent correlation between the formation of silicon dioxide structural defects and the process of wafer cooling from >1000 C to room temperature. The only obvious origin of this effect is the thermal contraction mismatch between the respective layers. A substantial amount of less direct evidence exists (Ref H-4, H-5) in support of this conclusion.

Thanks are due Dr. P.J. Besser and T.E. Hagey for experimental support, and to NASA-ERC for funded support under Contract NAS 12-4.

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APPENDIX I. THERMODYNAMIC ANALYSIS OF AMBIENT GAS EFFECTS

Introduction

Silicon device and integrated circuit technology, which represents one of the major areas of progress in electronics, depends heavily on the sophisticated use of highly specialized materials. The juxtaposition of such materials needed to produce the desired electronic function also often contains the seeds of long-term drift or deterioration of that very function. The mechanistic reasons for this frequenctly are unobvious because of the specialized nature of the materials and the intricate manner in which they are assembled. As a first step in anticipating such long-term interactions it should at least be determined which of them are thermodynamically permissible and which can be eliminated from further consideration. The present analysis attempts to do this for gaseous components that have been encountered by instrumental techniques, such as gas chromatography and mass spectrometry, in the packages of integrated circuits.

Gases considered were: nitrogen, hydrogen, argon, helium, methane, oxygen, water vapor, carbon dioxide, carbon monoxide, benzene, toluene, methylcyclohexane, and freon. Additional gases will be included as they are revealed by instrumental analysis.

Solid surfaces under examination were: silicon, silicon dioxide, aluminum, and aluminum oxide. Other surface compositions will be added in order of frequency and general reactivity.

Chemical reactions for the foregoing gases and solids were considered in terms of the simple thermodynamic free energy of reaction.

A literature survey concerned with integrated circuits and ambient gases is appended.

Free Energy Values

An important thermodynamic property is the free energy of reaction, for it is the magnitude and algebraic sign of this quantity which describes the chemical species which will exist under equilibrium conditions at a given temperature. Thus, the free energy of reaction or the change in free energy for a chemical reaction and its sign offers a means for the prediction that ambient gases will or will not chemically react with the solid surface materials present in packaged integrated circuits. With this connotation in mind Tables I-1 and I-2 summarize pertinent standard free energy values for temperatures, 298, 500 and 1000 K. The standard state is 298^{0} K at atmospheric pressure. For gases a correction must be made for fact that a real gas is not a perfect gas (Ref I-1). Furthermore, it is important to note that the standard free energy of formation of an element is, by definition, zero for the standard state. It is through application of an equation that the standard change in free energy is calculated for possible chemical reaction between ambient gases and solids in packaged integrated circuits.

TABLE I-1
THERMODYNAMIC VALUES FOR AMBIENT GASES [2] [3]

Gaseous Species	Standard Free Energy of Formation Kcal/Mole and ev					
	298°K	500°K	1000°K	298°K	500°K	1000°K
	Kcal/Mole			ev		
N_2, H_2, A, He, O_2	0	0	0	0	0	0
CH_4	-12.1	-7.8	+4.6	-0.53	-0.34	+0.20
HCl	-23.0	-24.0	-25.0	-1.00	-1.04	-1.09
H_2O	-54.6	-52.0	-46.0	-2.38	-2.26	-2.00
CO	-32.8	-37.1	-47.9	-1.43	-1.61	-2.08
CO_2	-94.3	-94.4	-94.6	-4.10	-4.11	-4.12
Benzene, C_6H_6	+31.0	+39.2	+62.3	+1.35	+1.71	+2.72
Toluene, C_7H_8	+29.3	+41.8	+76.3	+1.27	+1.82	+3.54
Methylcyclohexane, C_7H_{14}	+6.5	+37.5	+119.0	+0.28	+1.63	+5.18
CCl_2F_2	-102.7	-96.4	-81.2	-4.46	-4.19	-3.53
$Si\theta_2$(g)	-76.5	-76.8	-76.9	-3.33	-3.34	-3.35
SiO(g)	-27.9	-30.1	-42.2	-1.21	-1.31	-1.83
SiH_4	+13.2	+17.3	+28.8	+0.58	+0.75	+1.25
AlC	+196.2	+186.9	+164.5	+8.54	+8.14	+7.17
AlH	+55.0	+50.6	+40.6	+2.39	+2.20	+1.77
$SiCl_4$	-132.0	-128.0	-108.0	-5.75	-5.56	-4.70
SiF_4	-360.0	-356.0	-340.0	-15.70	-15.50	-14.80

TABLE I-2
THERMODYNAMIC VALUES FOR AMBIENT SOLIDS [2][3][4]

Solid Species	Standard Free Energy of Formation Kcal/Mole and ev					
	298°K	500°K	1000°K	298°K	500°K	1000°K
	Kcal/Mole			ev		
SiO_2	-204.6	-186.0	-164.0	-8.99	-7.80	-7.12
Al_2O_3	-378.1	-362.9	-325.3	-16.49	-15.80	-14.16
Si_3N_4	-36.0	-56.0	-100.0	-1.57	-2.44	-4.35
AlN	-68.6	-63.5	-50.5	-2.99	-2.77	-2.20
SiC	-20.1	-19.7	-18.8	-0.88	-0.86	-0.82
$AlCl_3$	-150.7	-138.8	-110.3	-6.55	-6.04	-4.80
AlF_3	-337.4	-324.6	-293.9	-14.69	-14.11	-12.75

Conclusions

The results of free energy calculations are summarized in Table I-3. The data predict for the indicated ambient gas-solid surfaces in contact, at the indicated temperatures, chemical reactions in all cases where the standard free energies are negative. These are the reactions between solid silicon and oxygen gas, solid silicon and carbon monoxide or carbon dioxide, gaseous benzene and solid silicon to form silicon carbide and hydride, toluene vapors and solid silicon to form the carbide or hydride, and CF_2Cl_2 and silicon to form silicon fluoride, silicon chloride and carbon.

Silicon dioxide solid is very stable and much less reactive than silicon. Free energy calculations for solid silicon dioxide with ambient gases were negative in only one instance, i.e., the chemical reaction with difluoro-dichloro-methane.

Aluminum metal is a common component in integrated circuit technology. Accordingly, simple standard free energies of reaction were calculated for solid aluminum-ambient gas systems. These thermodynamic data disclosed that the formation of aluminum nitride solid, aluminum oxide solid, (from both water vapor and oxygen, as well as carbon monoxide and dioxide), are probable reactions which occur between ambient gases and solids in packaged integrated circuits. As in the case of silicon metal and silica, the freon, dichloro-difluoro-methane, reacts with aluminum to form halide salts and carbon.

Aluminum oxide, solid, showed no chemical reactivity with any of the ambient gases commonly found in circuit packages.

A few general statements can be made concerning the calculated data in Table I-3.

1. Only chemical reactions between ambient gases and solids most commonly used in packaged integrated circuits were considered. Other materials can be included.

2. Free energy calculations for methylcyclohexane reactions are not shown as the results show that these reactions are less favorable than those of benzene and toluene.

3. No limits of error were associated with thermodynamic values used as they were not available in many cases.

4. The predictions made concerning ambient gas-solid chemical reactions are for the equilibrium condition. The kinetic picture can be quite different. For example, the kinetic removal of one chemical product from the reaction at equilibrium can cause a complete shift in the equilibrium to form more of the reaction products. During this shifting condition the processes may be steady state and are kinetic in nature until the new equilibrium is achieved.

5. Only over-all chemical reactions were considered. The participation of potential chemical intermediates and/or activated states was omitted from consideration.

6. Reaction of hydrogen with Si, SiO_2, Al and Al_2O_3 is thermodynamically disallowed.

TABLE I-3
CHEMICAL REACTIONS FOR PROCESS INTRODUCED AMBIENT GASES AT GAS-SOLID INTERFACES IN PACKAGED INTEGRATED CIRCUITS

Reaction, Solid Silicon Ambient Gas	Free Energy of Reaction 298°K	500 °K	1000°K	Favored
	Kcal/Mole			
(1) $Si_{(s)}+2H_{2(g)} \rightleftarrows SiH_{4(g)}$	+13.2	+17.3	+28.8	No
(2) $Si_{(s)}+O_{2(g)} \rightleftarrows SiO_{2(s)}$	-204.6	-186.5	-164.0	Strongly
(3) $2Si_{(s)}+O_{2(g)} \rightleftarrows 2SiO_{(g)}$	-27.9	-30.1	-42.2	Yes
(4) $Si_{(s)}+CH_{4(g)} \rightleftarrows SiH_{4(g)}+C_{(s)}$	+25.3	+25.1	+8.6	No
(5) $Si_{(s)}+H_2O_{(g)} \rightleftarrows SiO_{(g)}+H_{2(g)}$	+26.7	+21.6	+3.8	No
(6) $Si_{(s)}+SiO_{2(s)} \rightleftarrows 2SiO_{(g)}$	+148.8	+115.8	+79.6	No
(7) $Si_{(s)}+2CO_{(g)} \rightleftarrows SiO_{2(s)}+2C_{(g)}$	-139.0	-111.8	-63.2	Yes
(8) $Si_{(s)}+2CO_{(g)} \rightleftarrows 2SiC_{(s)}+O_{2(g)}$	+25.4	+34.8	+58.2	No
(9) $Si_{(s)}+CO_{2(g)} \rightleftarrows SiO_{2(g)}+C_{(s)}$	-110.3	-91.6	-69.5	Yes
(10) $2Si_{(s)}+2CO_{2(g)} \rightleftarrows 2SiC_{(s)}+2O_{2(g)}$	+148.4	+149.4	+151.6	No
(11) $6Si_{(s)}+C_6H_{6(g)} \rightleftarrows 6SiC_{(s)}+3H_{2(g)}$	-151.6	-157.4	-177.1	Yes
(12) $Si_{(s)}+C_6H_{6(g)} \rightleftarrows SiH_{4(g)}+6C_{(s)}+H_{2(g)}$	-17.8	-21.9	-33.5	Yes
(13) $7Si_{(s)}+C_7H_{8(g)} \rightleftarrows 7SiC_{(s)}+4H_{2(g)}$	-170.0	-179.7	-207.9	Strongly
(14) $Si_{(s)}+C_7H_{8(g)} \rightleftarrows SiH_{4(g)}+7C_{(s)}+2H_{2(g)}$	-16.1	-24.5	-47.5	Yes
(15) $2Si_{(s)}+2CCl_2F_{2(g)} \rightleftarrows SiCl_{4(s)}+SiF_{4(s)}+2C_{(s)}$	-286.6	-291.2	-285.6	Strongly

TABLE I-3 (Continued)

Reaction, Solid Silicon Ambient Gas	Free Energy of Reaction 298°K	500°K	1000°K (Kcal/Mole)	Favored
(16) $3Si_{(s)}+2N_{2(g)} \rightleftarrows Si_3N_{4(s)}$	-82.0	-104.0	-150.0	Yes
(17) $SiO_{2(s)}+2H_{2(g)} \rightleftarrows SiH_{4(g)}+O_{2(g)}$	+217.8	+203.3	+192.8	No
(18) $SiO_{2(s)}+CH_{4(g)} \rightleftarrows SiH_{4(g)}+CO_{2(g)}$	+229.9	+211.1	+188.2	No
(19) $SiO_{2(s)}+2H_2O_{(g)} \rightleftarrows SiH_{4(g)}+2O_{2(g)}$	+327.0	+301.3	+285.0	No
(20) $2SiO_{2(s)}+2CO_{(g)} \rightleftarrows 2SiC_{(g)}+3O_{2(g)}$	+434.6	+406.8	+386.6	No
(21) $SiO_{2(s)}+CO_{2(g)} \rightleftarrows SiC_{(s)}+2O_{2(g)}$	+278.8	+260.7	+240.0	No
(22) $6SiO_{2(s)}+C_6H_{6(g)} \rightleftarrows 6SiC_{(s)}+3H_2O_{(g)}+9O_{2(g)}$	+880.9	+802.6	+670.9	No
(23) $7SiO_{2(s)}+C_7H_{8(g)} \rightleftarrows 7SiC_{(s)}+4H_2O_{(g)}+5O_{2(g)}$	+1044.4	+914.3	+760.2	No
(24) $2SiO_{2(s)}+2CCl_2F_{2(g)} \rightleftarrows SiCl_{4(s)}+SiF_{4(g)}+2CO_{2(g)}$	-66.0	-104.0	-131.8	Yes
(25) $3SiO_{2(s)}+2N_{2(g)} \rightleftarrows Si_3N_{4(s)}+3O_{2(g)}$	+577.8	+502.0	+392.0	No
Solid Aluminum-Ambient Gas				
(26) $Al_{(s)}+1/2N_{2(g)} \rightleftarrows AlN_{(s)}$	-68.6	-63.5	-50.6	Yes
(27) $Al_{(s)}+1/2H_{2(g)} \rightleftarrows AlH_{(g)}$	+55.0	+50.6	+40.6	No
(28) $2Al_{(s)}+3/2O_{2(g)} \rightleftarrows Al_2O_{3(s)}$	-378.1	-362.9	-325.3	Strongly
(29) $Al_{(s)}+CH_{4(g)} \rightleftarrows AlC_{(g)}+2H_{2(g)}$	+208.3	+194.7	+159.9	No

TABLE I-3 (Concluded)

Solid Aluminum-Ambient Gas	Free Energy of Reaction 298°K	500°K	1000°K	Favored
	Kcal / Mole			
(30) $4Al_{(s)}+CH_{4(g)} \rightleftarrows 4AlH_{(g)}+C_{(s)}$	+232.1	+210.2	+157.8	No
(31) $2Al_{(s)}+3H_2O_{(g)} \rightleftarrows Al_2O_{3(s)}+3H_{2(g)}$	-214.3	-206.9	-187.3	Yes
(32) $2Al_{(s)}+3CO_{(g)} \rightleftarrows Al_2O_{3(g)}+3C_{(s)}$	-279.7	-251.6	-181.6	Yes
(33) $6Al_{(s)}+C_6H_6 \rightleftarrows 6AlC_{(g)}+3H_{2(g)}$	+1146.2	+1082.3	+924.7	No
(34) $4Al_{(s)}+3CO_{2(g)} \rightleftarrows 2Al_2O_{3(g)}+3C_{(s)}$	-473.3	-442.6	-366.8	Strongly
(35) $8Al_{(s)}+C_7H_{8(g)} \rightleftarrows 8AlH_{(g)}+7C_{(s)}$	+410.7	+363.0	+248.5	No
(36) $4Al_{(s)}+3CCl_2F_{2(g)} \rightleftarrows 3C_{(s)}+2AlCl_{3(s)}+2AlF_{3(s)}$	-668.1	-637.6	-564.8	Strongly
(37) $Al_2O_3+N_{2(g)} \rightleftarrows 2AlN_{(s)}+3/2O_{2(g)}$	+240.9	+235.9	+224.1	No
(38) $Al_2O_{3(s)}+H_{2(g)} \rightleftarrows 2AlH_{(g)}+3/2O_{2(g)}$	+488.1	+464.1	+406.5	No
(39) $Al_2O_{3(s)}+2CH_{4(g)} \rightleftarrows 2AlC_{(g)}+3H_2O_{(g)}+H_{2(g)}$	+625.9	+596.3	+501.1	No
(40) $Al_2O_{3(s)}+H_2O_{(g)} \rightleftarrows 2AlH_{(g)}+2O_{2(g)}$	+542.7	+528.1	+452.5	No
(41) $1/2Al_2O_{3(s)}+CO_{(g)} \rightleftarrows AlC_{(g)}+5/2O_{2(g)}$	+418.0	+407.9	+375.1	No
(42) $3Al_2O_{3(s)}+C_6H_{6(g)} \rightleftarrows 6AlC_{(g)}+3H_2O_{(g)}+3O_{2(g)}$	+2116.7	+2013.9	+1766.6	No
(43) $2Al_2O_{3(s)}+C_7H_{8(g)} \rightleftarrows 4AlC_{(g)}+3CO_{(g)}+3H_2O_{(g)}+H_{2(g)}$	+1237.5	+1174.5	+628.0	No
(44) $7Al_2O_{3(s)}+6CO_2F_{2(g)} \rightleftarrows 6AlC_{(g)}+4AlCl_{3(g)}+4AlF_{3(g)}+210_{2(g)}$	+1253.9	+1164.4	+1067.3	No
(45) $2Al_2O_{3(s)}+3Si_{(s)} \rightleftarrows 4Al_{(s)}+3SiO_{2(s)}$	+142.4	+168.8	+156.6	No

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I-2. Stull, D. R., Proj. Director, Janaf Thermochemical Tables, Advanced Research Projects Agency Program. US Air Force Contract No. AF04(611)7554 Dow Chemical Co., Midland, Michigan.

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I-4. Chu, T. L., Lee, C. H., and Gruber, G. A., J. Electrochem. Soc., Solid State. 114, No. 7, 717-722 (1967).

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I-2. Leiby, C. C. and Chen, C. L., "Diffusion Coefficients, Solubilities and Permeabilities for He, Ne, H_2 and N_2 in Vycor Glass". J. Appl. Phys., 31, 268 (1960).

In 96% silicon dioxide glass (vycor) helium diffusion rate is higher than in pure silicon dioxide glass, but is lower in most other glasses. The higher diffusion rate in vycor is probably due to the method of fabrication leading to greater porosity.

I-3. Mouison, A. J., Roberts, J. P., "Water in Silica Glass", Trans. Brit. Ceram. Soc., 59, 388-399 (1960), Trans. Faraday Soc., 59, 1208-1216 (1961).

Diffusion measured by IR absorption at 2.7 microns. Some question as to whether water or hydroxyl is diffusing species.

I-4. Zaininger, K. H., Warfield, G., "Hydrogen Induced Surface States at a Si-SiO_2 Interface", Proc. IEEE, 52, 972-973, August (1964).

Hydrogen increases the inversion layer capacitance upon contact with an MOS structure at high temperature.

I-5. Haas, C. "The Diffusion of Oxygen Into Silicon," J. Phys. Chem. Solids 15, 108-111, August (1960).

Assumption is made that internal friction and diffusion, or both, due to the same relaxation phenomenon. The diffusion coefficient for oxygen in silicon is calculated from experimental data on internal friction. Diffusion constant: 0.21 cm^2/sec, energy of activation: 2.44 electron volts.

I-6. Logan, R. A. and Peter, A. J., "Diffusion of Oxygen in Silicon". J. Appl. Phys. 28, 819-820, July 19 (1957).

Experimental results on oxygen diffusion coefficient in silicon support Haas.

I-7. Frosch, C. J. and Derick, L. "Diffusion Control in Silicon by Carrier Gas Composition". J. Electro-Chem. Soc. 105, 695-699, December (1958).

Antimony tetroxide at 950°C, one hour diffusion at 1200°C produces a junction 1.5 microns deep in a 5 ohm-cm p-type silicon. The surface concentration depends upon the quantity of water vapor in the nitrogen flow gas, from 3.3×10^{19} atoms/cm^{-3} for dry nitrogen to 8×10^{17} atoms/cm^3 for nitrogen bubbled through water at 70°C.

I-8. Thompson, C. "The Effects of Ambients on Performance of CdS Thin Film Transistors". Science Abstracts B. Electrical Engineering 68, 11389 (1965); Japan J. Appl. Phys. 4, No. 3, 207-211 March (1965).

Describes the operating mechanisms of the thin film CdS transistor at several pertinent temperatures and ambients. The effects of the ambients are correlated to device parameters with further implications.

I-9. Lehman, H. S., "Chemical and Ambient Effects on Surface Conduction in Passivated Silicon Semiconductors". Science Abstracts B. Electrical Engineering 68, 9843 (1965); IBM J. Res. and Development (USA) 8, No. 4, 422-426 September (1964).

The effect of processing variables on the surface conduction properties of passivated silicon junction devices has been studied. Insulated gate field effect transistors fabricated in p-type silicon were used as an experimental tool. Varying the metal used as the gate electrode is shown to strongly influence the surface conductivity of the field effect device. The effects of heat treatment in various ambients and variation in the insulators used are also discussed. Surface conduction is shown to be a complex function of materials thermal history and processing.

I-10. Brattain, V. H. and Garrett, C. G. "Protection of Silicon Conductive Devices by Gaseous Ambients". (Bell Telephone Lab.) US Pat. No. 2,777,974, January 15, 1957.

The use of ambient atmosphere of oxygen to control the surface characteristics of junction devices by preventing or inhibiting the formation of undesirable conducting paths (channels) at or near the surfaces of these devices is discussed. The effects of the oxygen is to form a layer of p-type material on the surface of the crystal which prevents the formation of n-type channels on the p-type region.

I-11. Many, A. and Gerlick, D. "The Effect of Gaseous Ambients on the Interface Structure of Germanium. (Hebrew Univ.) Recent news abstracts of the Electrochem. Soc., Semiconductor Symposium, May (1957).

Simultaneous measurements of surface recombination velocity and trapped charge density in the fast state as a function of surface potential were reported. The surface potential was varied over a wide range by the application of large AC fields normal to the surface. It was found that the distribution and characteristics of the fast state were markedly affected by the surrounding ambients. Initially with the sample in vacuum, rapid changes in interface structure took place. After a few days stabilization was essentially reached. Following repeated exposures to the different ambients reproducible changes resulted which presisted for many weeks.

I-12. Jauffe, K. "Gas Reaction on Semiconducting Surfaces and Space Charge Boundary Layers". Semiconductor Surface Physics, Univ. of Pennsylvania Press, 259-282 (1957).

The Fermi potential of a catalyst is related to the electronic exhange level of the reacting molecules. Applying a three dimensional term scheme the relations are generalized. On the basis of results one can determine whether an n- or p-type catalyst must be used for a reaction. Furthermore, the important rule of the space charge in the catalyst is discussed with its effect upon the reaction kinetics.

I-13. Stattz, H., DeMars, G. A., Davis, L. Jr., Adams, A. Jr., (Raytheon Manufacturing Co.) Semiconductor Surface Physics (University of Pennsylvania Press) 139-168 (1957).

Steady state and nonsteady state inversion layer conductance on silicon and germanium are discussed in terms of two types of surface states. The second type state is located at the surface of the oxide with perhaps some states in the oxide film. The states result mainly from adsorbed gas molecules. Depending upon the surrounding gas they are either predominantly acceptor or donor type and it is principally the states which determine the directions in which the bands at the surface are bent. It is possible to determine the number and energy of the interface states from nonsteady state inversion layer conductance measurement. It is found that high fields across the oxide film can influence the density of these states in silicon lying above the middle of the gap. Anomalous inversion layer conductances are found when vapors of certain liquids are adsorbed.

I-14. Kozlouskaya, V. M. "Mass Spectrometric Determination of the Amount and Composition of Gases Adsorbed on the Surface of Germanium and Silicon Monocrystals". Solid State Abstract 1, 6046 (1960-1961); Soviet Phys., Solid State 1, 940-946 January (1960).

I-15. Gleason, F. R., Greiner, J. H. and Yetter, L. R. "Gas Absorption by Vacuum Evaporated Magnetic Films". Solid State Abstract 1, 6149 (1960-1961); (IBM) Vacuum 9, 301 November (1959).

Mass spectrometric determination of the types and amounts of gases absorbed during the deposition of vacuum evaporated thin films were reported. Most of the gases came from the oil pump. The absorbed gas molecules per metal atom degassed was independent of film thickness, indicating that the gas is trapped in the film structure as well as on the surface.

I-16. Kammere, H. C., "Thermal Evaluation of High Density Electronic Packages". Solid State Abstract 3, 16912 (1962) Electron Design 9, 121-122 December (1961).

A monograph to determine the design limitation of microminiature packages exposed to thermal stress. Five basic parameters investigated were: total temperature between ambient environment and the center of the package, thermal conductivity of package material, cooling technique and size and configuration of maximum.

I-17. Kislev, A. U. and Lygin, V. I. "University of Moscow". Solid State Abstract 5, 28828 (1964); Surface Science 2, 236-244 (1964).

The shift of the absorption band of silica surface hydroxyl groups on adsorption of mulecules of different electronic structures is in accordance with their heats of adsorption and ionization potentials. On the basis of vibrational theory the spectra of water and ammonia molecules adsorbed on silica and zeolites have been analyzed.

I-18. Boutin, H. and Prask, H. "Study of Water Vapor Absorption on Gamma Alumina and Silica by Slow Neutron Inelastic Scattering". Solid State Abstract 5, 28830 (1964); Surface Science 2, 261-266 (1964).

The energy spectrum of neutrons, inelastically scattered by hydrogenous groups adsorbed on the solid surface is able to provide information concerning the degree of mobility of those groups, the nature and strength of the binding with the adsorbent and the frequencies of rotational or vibrational motions ranging from 20 to 1,000 cm^{-1}. The principle of the technique is given and is applied to water adsorbed on silica and gamma alumina after the samples have been heated to a 150° under vacuum. Two types of water molecules exist on the surface: distorted molecules with hydroxyl groups hydrogen-bonded to oxygen atoms, and tetrahedral molecules similar to the liquid. Additional water layers on the surface become more water-like.

I-19. Volkenstein, F. F. and Karpenke, I. V. "Theory of Photoadsorptive Effect in Semiconductors". Solid State Abstract 5, 30709 (1964); STAR 2, 3457A December (1964) AD605733.

The sign of the photo-adsorptive effect in semiconductors depends on selection of the system, on the mode of experiment and the preparation of the sample for experiment. Report offers formulas for establishing basic criteria for determination of the photo-adsorption effect.

I-20. Farnsworth, H. E. and Campbell, B. D. (Brown University) "Study of the Surface Properties of Atomically Clean Metal and Semiconductors". Solid State Abstract 6, 37205 (1966); Contract DA28304 ANC 0029E US Government Research and Development Reports 40, 146A May 20, (1965) AD 31-699.

Oxygen adsorption on the (0001) matte surface was enhanced when an intense light was incident on the crystal. A 3-5 Torr-min oxygen exposure in intense light extinguished the diffraction pattern whereas a 759 Torr-min exposure in the dark had little effect upon the pattern, but did cause a slight decrease in conductivity of the surface. Ion bombardment increased the dark conductivity and greatly decreased the effect of intense light. Photo-adsorption of oxygen is indicated. Unlike matte surface (0001) specular surface was not effected by exposure to light.

I-21. Hobson, J. P. "A New Method for Finding Heterogeneous Energy Distributions from Physical Adsorption Isotherms". Solid State Abstracts 6, 41617 (1966); Canadian J. Phys. 4, 1934 November (1965).

A model is described which assumes that a hetergeneous surface has a distribution of adsorption energies for physical adsorption. A new solution is presented giving a number of step types: local isotherms, which are chosen to represent varying degrees of adsorbate-adsorbate interaction. The solution permits energy distributions to be obtained quite simply from isotherm data at one temperature. This solution may be used to calculate isotherms at other temperatures.

I-22. Howling, D. H. "Photoelectric Response of Metal Surfaces in Ambient Atmospheres". Solid State Abstract 7, 48029 (1967); J. Appl. Phys. 37, 1844 (1966).

Experiments are described which examine variations in the photoelectric response of metal surfaces immersed in gas atmospheres. Work function changes have been produced by gas bombardment, electrode heating, deposition of small amounts of K on the surface. By operating the electrode under study as the cathode of geiger muller photon counter, photocurrents as low as 10^{-21} A could be measured. Factors which influence irreversible changes in work functions have been explored. A less well known increase in work function which is thermally activated has been demonstrated. Systems included were: tungsten/hydrogen, nickel/hydrogen, iron/hydrogen, platinum/hydrogen, paladium/hydrogen, rhenium/hydrogen; also nitrogen, neon, argon and ammonia.

I-23. Logan, R. M. and Stickney, R. E., "Simple Classical Model for the Scattering of Gas Atoms from a Solid Surface". Solid State Abstract 7, 46668 (1967); J. Chem. Phys. 44, 195 (1966).

A simple classical model for the scattering of gas atoms from a solid surface is proposed and its characteristics discussed. Results are obtained for the angular distribution of scattered particles. The model correctly predicts the general appearance of the scattering pattern, and its dependence upon the angle of incidence of the beam and on the temperature and masses of the gas and surface atoms.

I-24. Lu, Wei-Kao, "The General Rate Equation for Gas Solid Reaction in Metallurgical Processes with the Restrictions of Reversibility of Chemical Reaction and Gaseous Equimolar Counter-Diffusion". Solid State Abstract 7, 46669 (1967); AIME. Trans. 236, 531 (1965).

An improved general rate equation for a one dimensional gas-solid system has been derived. The concentrations of gaseous reactant and product have been calculated with relations furnished by the following constraints on the system: quasi-steady state and equimolar counter diffusion of gases. The interfacial chemical reaction is taken as 1st order with respect to the concentration of the gases involved. The equation has proper dependence on gas composition and on solid structure through the relative values of Knudsen and normal diffusivities.

I-25. Micheletti, F. B., and Mark, P., "Effects of Chemi-sorbed Oxygen on the Electrical Properties of Chemically Sprayed CdS Thin Films". Electronics and Communications Abstracts 6, 4467 (1967); Appl. Phys. Letters 10, No. 4, 136-138 (1967).

Measurements with spray deposited semiconducting CdS films are reported that demonstrate the primary effect of oxygen chemi-sorption is the reduction of hall mobility.

I-26. Blum, J., Warwick, R. and Genser, M. "Surface Studies with Silicon Planar Junction Structures". Presented at the Spring Meeting of the Electrochemical Society, Toronto, Canada, May 3-7 (1964) (Gen. Prec. Aerospace., Kearfott Div.)

Changes in: emitter current gain, beta, with collector current. Surface recombination velocity limits beta and is in turn determined by the density of fast interface states and the surface potential. Changes in characteristics of silicon npn planar transistors were observed after heating for various times at temperatures between 300-350°C in forming gas (15% H_2, 85% N_2), oxygen, vacuum and nitrogen.

X-Radiography. - Components were examined for foreign particles, percent void area in the die to header bond and other anomalies. The void area data are given in Table J-1 and indicate an excess of 40 percent voids in 50 percent of the sample. Foreign particles were noted in seven devices using the Search-Ray. Typical findings are shown in Figures J-1 to J-3. Shake testing was performed simultaneously to determine particle mobility but no particle displacement was noted. Particles remained in position after cautious delidding.

Hermeticity. - The fine leak test (Veeco) revealed no failures per Autonetics procurement specification which requires a leak rate not to exceed 5.0×10^{-7}. All helium leak rates fell between 1×10^{-8} and 3×10^{-9}. However, 25 percent of the devices failed the gross leak test per specification using ethylene glycol at 150 C. These failures are identified in Table J-2.

Electrical parameters. - Electrical failures are listed in Table J-3. The parameters not meeting specifications are identified with an asterisk (*). The remaining devices performed according to specification.

Electrical dynamics. - Components were subjected to vibrational stress while observing electrical characteristics on a Tektronix 575 Curve Tracer. Eight components displayed an excessive forward voltage drop at high forward conductance (2 volts at 200 ma); one of these was intermittent. The components and failure modes are identified in Table J-4.

Optical examination. - Eight components were delidded for optical examination of surface anomalies. Evidences of tool damage, or other mishandling, prior to lidding resulting in damage to metallization on two devices are shown in Figures J-4 and J-5. The remaining devices were free of obvious anomalies except for No. 35 (Part No. 00995, Log No. 433) which had a detached post bond weld.

Metallurgical examination. - The eight components delidded for optical examination also were subjected to metallurgical sectioning and microscopy, revealing several previously unobvious anomalies. Partial post bonds are shown in Figures J-6 and J-7 with electrical contact constricted through intermetallic fragments. Figure J-8 shows approximately 60 percent of aluminum wire destroyed in welding and the presence of intermetallic formation at a base post bond. Cracks probably due to excessive deformation on an emitter pad bond are shown in Figure J-9. An interface between aluminum wire and aluminum pad is shown in Figure J-10; Figure J-11 indicates excessive wire deformation during welding and cracking from intermetallic formation. A partial base post bond with intermetallic formation is shown in Figure J-12. Each numbered figure represents a separate device identified by the caption.

Tensile strengths, Au/Al post bonds. - The metallographic anomalies enumerated above suggested the presence of a general bond reliability problem in this group of transistors. Accordingly, tensile strengths were measured on the post bonds of 25 delidded specimens using the test equipment shown in Figure J-13 at a pull angle of 45 degrees. Criteria of acceptance are defined in an Autonetics procurement specification which requires a minimum allowable breaking strength of 2.0 grams at

TABLE J-1
VOIDS OBSERVED BY X-RADIOGRAPHY IN SAMPLE CQF-101

Greater Than 40%	Part No.	Lot No.	% Voids in Bonding of Chip	Less Than 40%	Part No.	Lot No.	% Voids in Bonding of Chip
1	03750	437	27	2	03767	437	80
4	03749	435	30	3	03729	437	55
5	03748	435	25	6	03756	437	40
9	03742	435	20	7	03743	437	65
10	03711	437	15	8	03740	437	65
11	03703	435	15	13	03714	435	60
12	03747	435	30	14	03773	437	70
18	03681	435	20	15	03719	435	80
20	03698	435	20(FP)	16	03734	435	50(FP)
21	00125	433	25	17	03728	435	60
24	00153	433	15	19	03691	435	60
25	00156	439	20(FP)	22	00135	433	60
27	00285	439	30	23	00143	433	40
28	00399	433	20	26	00256	433	75
30	00542	436	20	29	00463	439	40
31	00556	436	30	33	00879	433	50(FP)
32	00821	433	25	39	00626	439	60
34	00943	433	30	41	00638	436	60
35	00995	433	30	42	00639	438	55
36	00032	433	25	43	00650	436	50
37	00617	436	25	44	00653	438	70
38	006260	436	30	46	00673	436	45
40	00630	438	35	49	00704	433	70
45	00666	438	20	50	00708	439	40
47	00675	438	30(FP)	54	00736	438	40
48	00686	433	30	56	00788	433	60
51	00727	436	20	59	01176	433	70
52	00731	438	30	60	01122	433	80
53	00732	438	20	61	01221	432	60
55	00738	439	25	63	01261	432	60
57	01002	439	20	67	01300	432	50(FP)
58	01065	439	30	71	02426	434	40
62	01222	432	20	74	02567	434	45
64	01262	432	30	75	02592	434	60
65	01282	432	15	77	05028	435	50
66	01291	432	30	78	05055	435	60
68	01310	432	20	79	05072	435	60
69	02259	434	30	81	05144	435	50
70	02322	434	20	82	05274	435	60(FP)
72	02458	434	20	83	05314	435	60
73	02475	434	20	84	05318	435	70
76	02620	434	35	85	03740	435	60
80	05079	435	20	86	03744	435	80
88	03739	435	20	87	03741	435	60
89	03750	435	30				

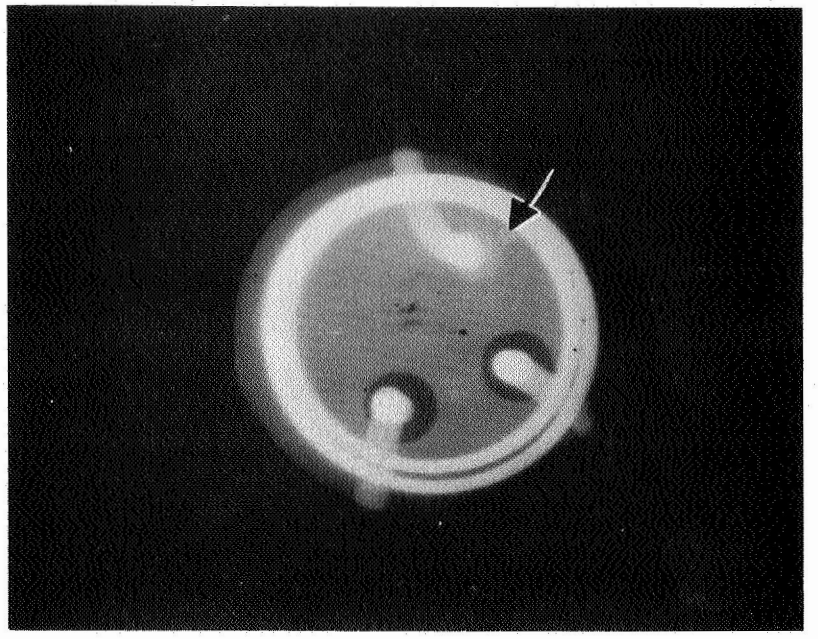

Figure J-1. Lot No. 435, Part No. 03698

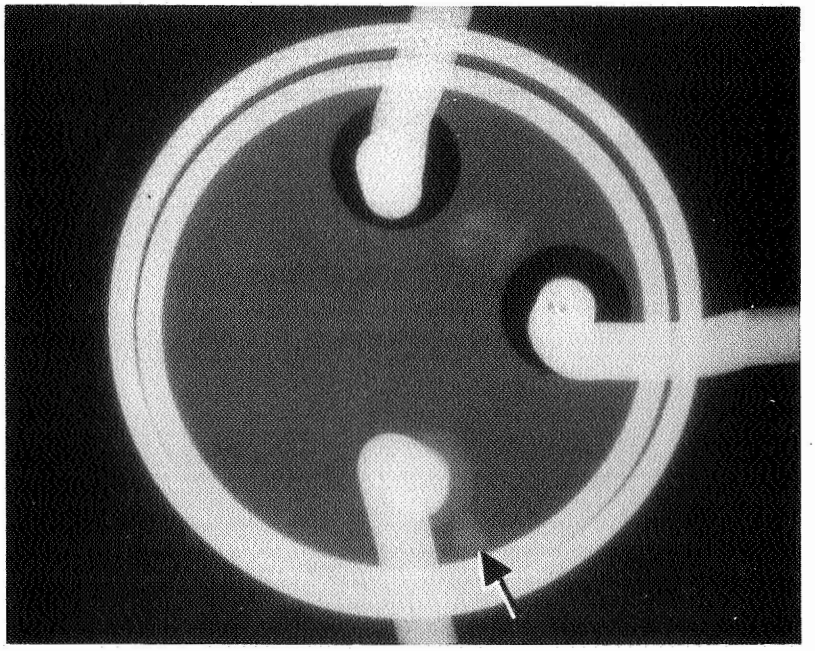

Figure J-2. - Part No. 03698, Lot No. 435

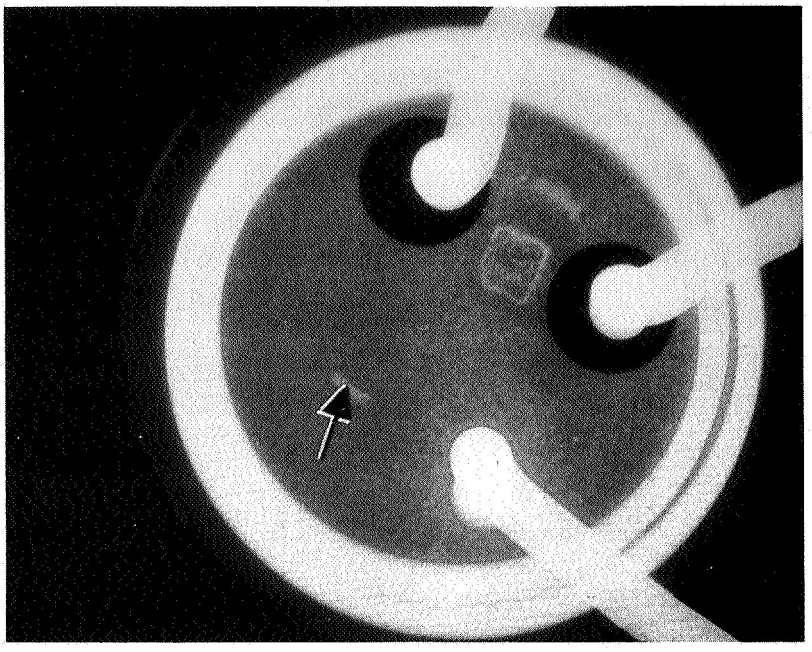

Figure J-3. - Part No. 00156, Lot No. 439

TABLE J-2
GROSS LEAK FAILURES

No.	Part No.	Lot No.
6	03756	437
8	03740	437
13	03714	435
14	03773	437
15	03719	435
18	03681	435
19	03691	435
20	03698	435
23	00143	433
26	00256	433
32	00821	433
34	00943	433
38	006260	436
43	00650	436
66	01291	432
67	01300	432
70	02322	434
74	02567	434
76	02620	434
82	05274	435

TABLE J-3
ELECTRICAL FAILURES

No.	Part No.	Lot No.	Parameter I_{CBO}	Parameter h_{FE}
1	03750	437		*
10	03711	437		*
13	03714	435		*
14	03773	437		*
19	03691	435		*
25	00156	439		*
29	00463	439		*
34	00943	433	*	*
41	00638	436		*
47	00675	438		*
61	001221	432		*
62	001222	432		*
75	02567	434		*
78	05055	435		*
81	05144	435		*
85	03740	435		**

TABLE J-4
DYNAMIC ELECTRICAL FAILURES

No.	Part No.	Lot No.	High Forward Voltage Drop	Intermittents
5	03748	435	*	
8	03740	437	*	
13	03714	435	*	
35	00995	433	*	*
40	00630	438	*	
44	00653	438	*	
58	01065	439	*	
61	01221	432	*	

the bond edge (BE) and 3.0 grams for a complete bond (CB) failure. Obviously a BE rupture below 3.0 grams could mask a potential CB failure. The parent strength of the aluminum lead wire was 12-15 grams.

The results of these tests are given in Table J-5 with the mode of rupture identified in each case as BE or CB except where detached leads or zero pull strengths were encountered. The BE failures are ascribed to a possible excessive pinching during bonding resulting in reduction of wire cross section at the bond edges. The CB failures may have resulted from insufficient weld interface, granule formations or oxide contaminations at interfaces.

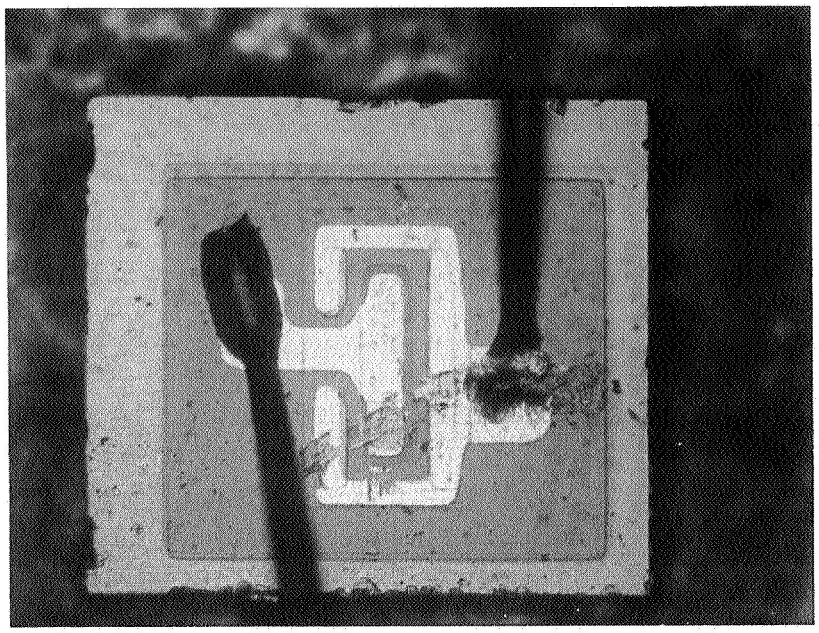

Figure J-4. Part No. 03748, Lot No. 435

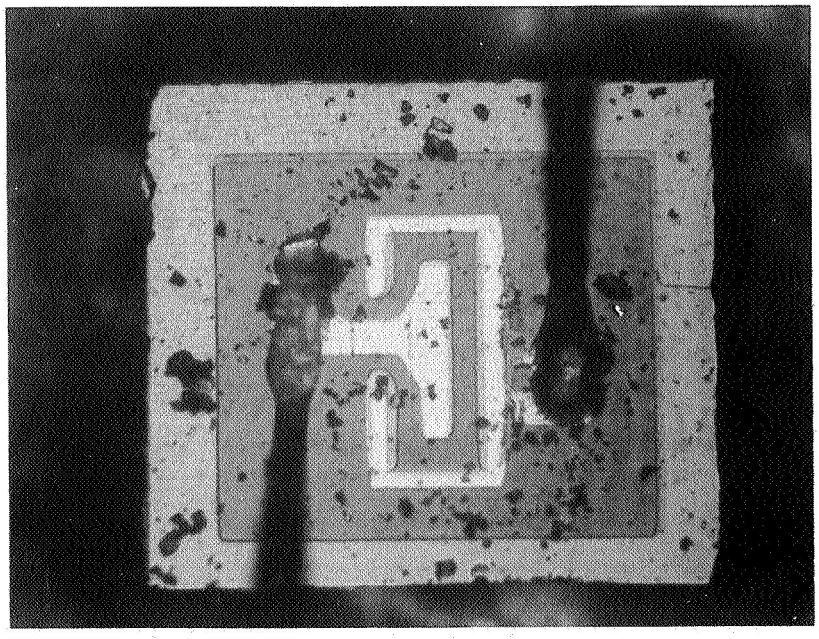

Figure J-5. Part No. 00653, Lot No. 438

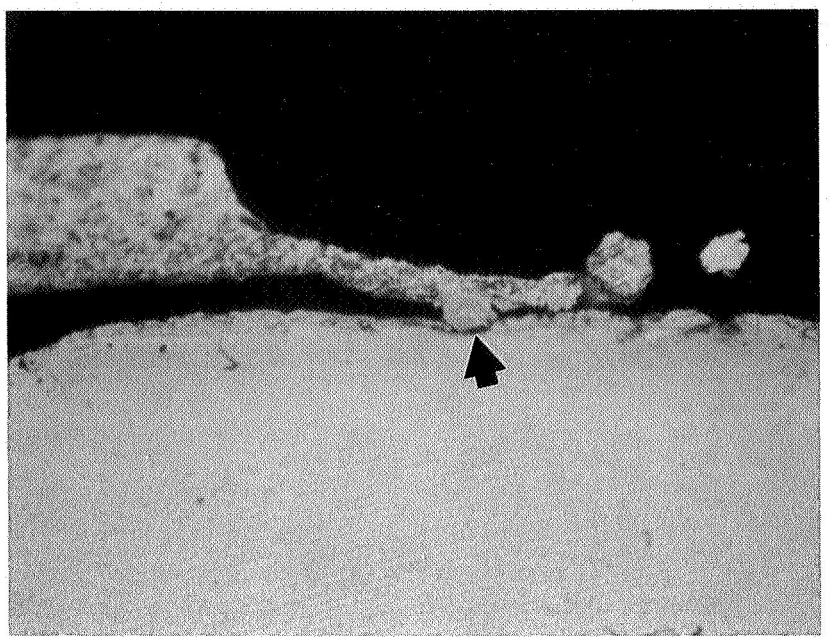

Figure J-6. - Part No. 03740, Lot No. 437

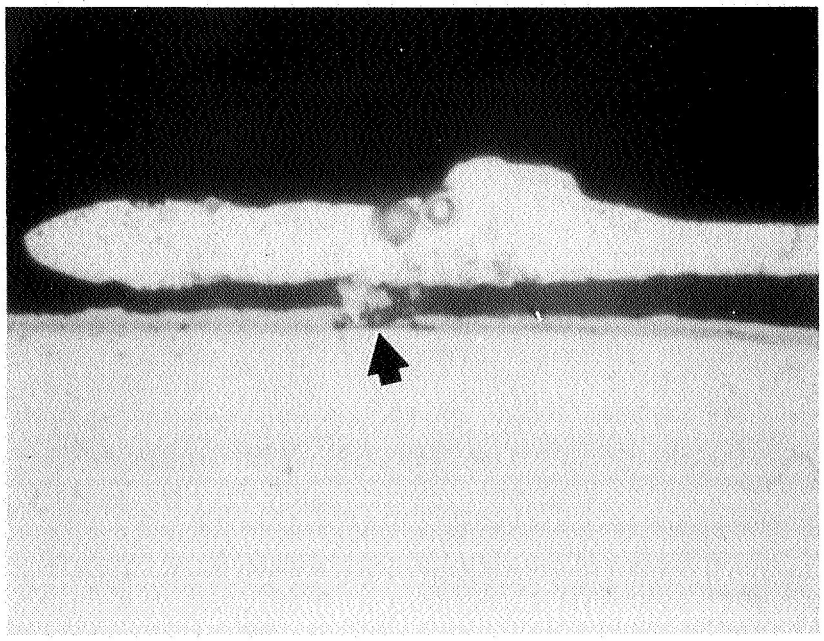

Figure J-7. - Part No. 03714, Lot No. 435

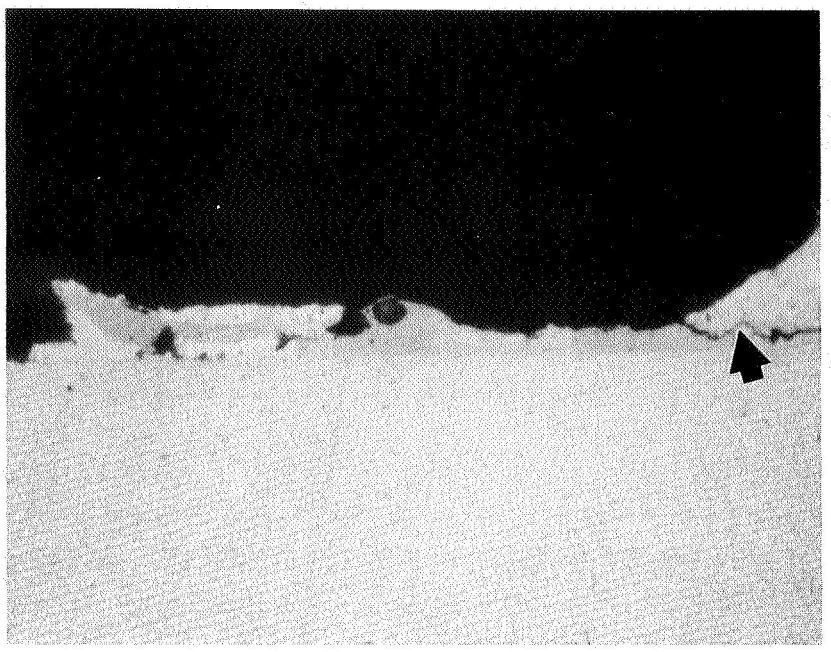

Figure J-8. - Part No. 00630, Lot No. 438

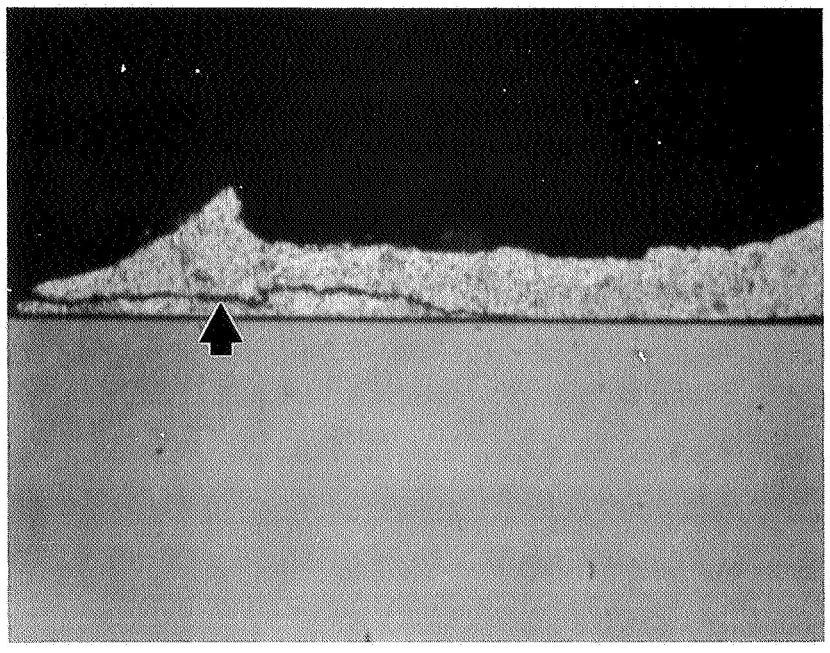

Figure J-9. - Part No. 00653, Lot No. 438

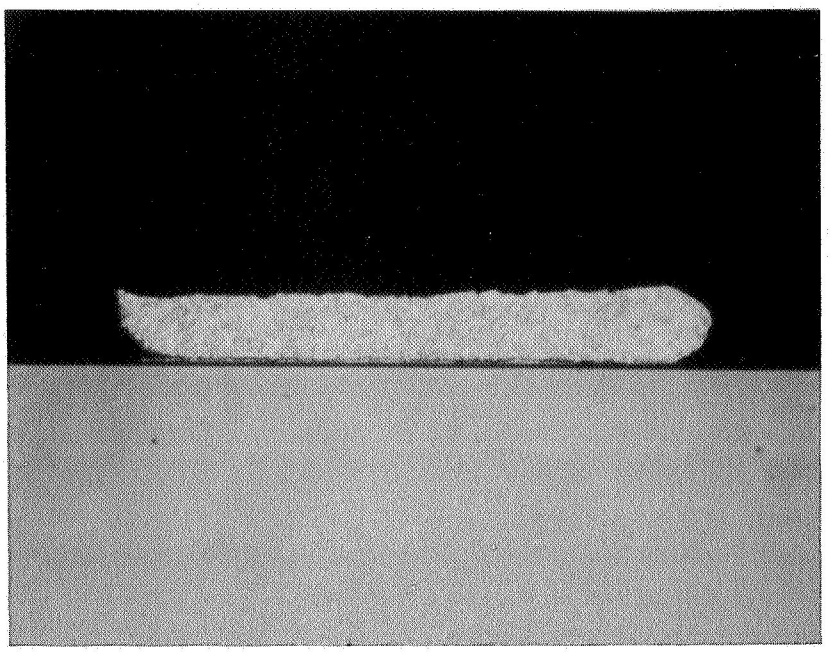

Figure J-10. - Part No. 01065, Lot No. 439

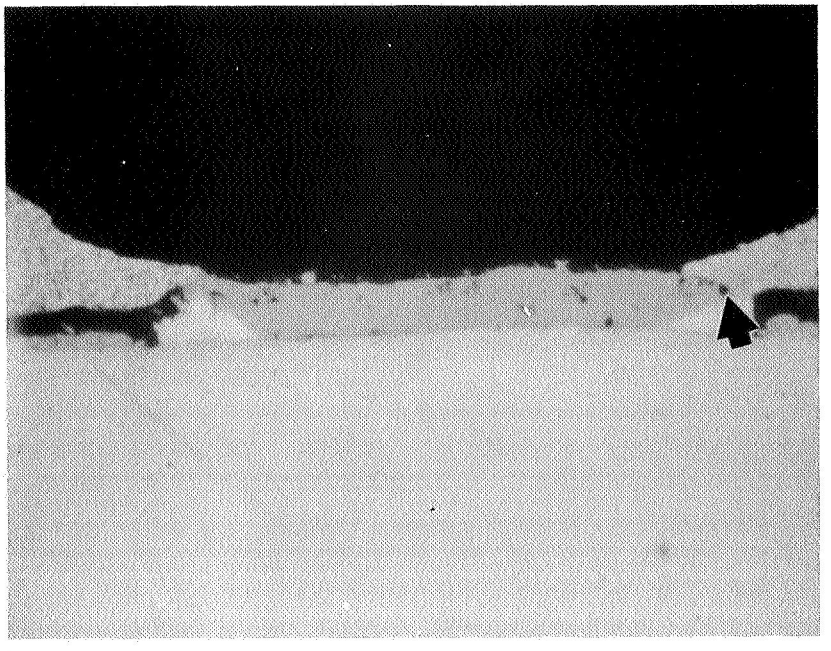

Figure J-11. - Part No. 01065, Lot No. 439

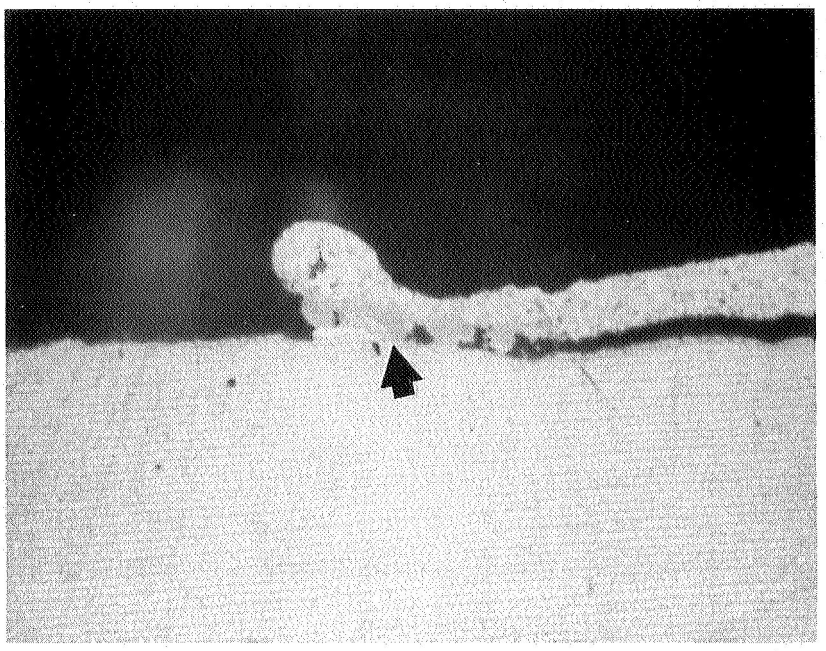

Figure J-12. - Part No. 01221, Lot No. 432

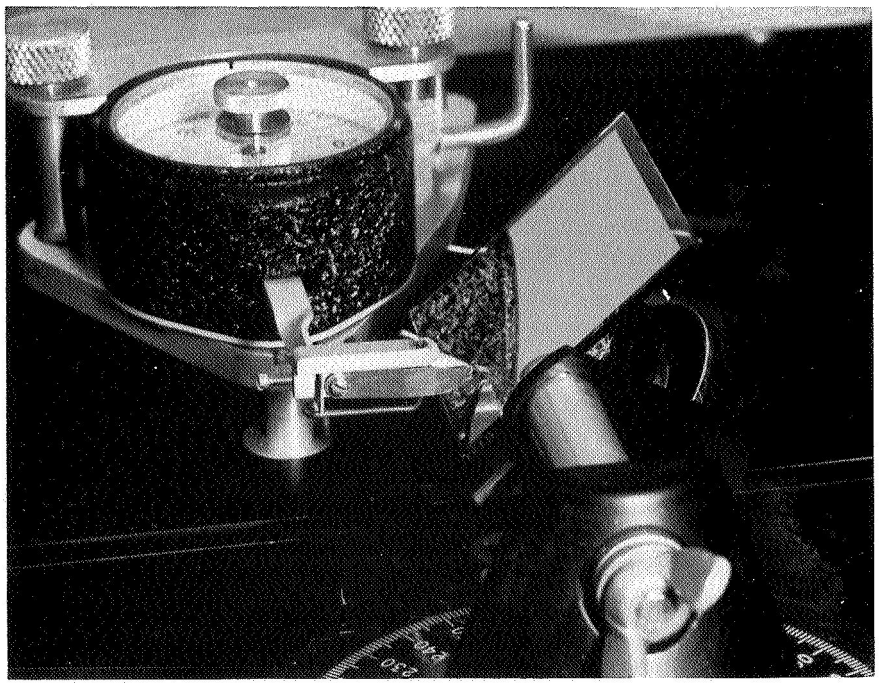

Figure J-13. - Lead Bond Tensile Tester

TABLE J-5
POST DATA YIELD STRENGTH DATA

No.	Part No.	Lot No.	Emitter Pull Strength (grams)	Mode of Failure	Base Pull Strength (grams)	Mode of Failure
63	01261	432	0	--	0	--
67	01300	432	1.7	BE*	2.0	BE
66	01291	432	3.3	CB*	2.0	CB*
70	02322	434	3.5	BE	1.7	CB*
89	03750	435	2.0	CB*	0	--
80	05079	435	3.5	CB	1.5	CB*
87	03741	435	2.6	BE	2.5	BE
62	01222	432	5.0	BE	3.7	BE
69	02259	434	3.2	CB	0	--
64	01262	432	3.7	BE	1.5	BE*
75	02592	434	3.5	CB	4.2	BE
79	05072	435	3.5	BE	5.3	CB
76	02620	434	1.0	CB*	1.3	CB*
74	02567	434	2.0	CB*	(detached)	--
68	01310	432	2.6	BE	3.3	BE
81	05144	435	4.0	BE	5.2	BE
86	03744	435	2.0	BE	2.0	CB*
83	05314	435	0	(detached)	0	--
78	05055	435	3.9	CB	0.5	CB*
65	01282	432	2.0	CB*	3.2	CB
85	03740	435	2.1	CB*	(detached)	--
77	05028	435	0	(detached)	3.5	CB
82	05274	435	2.0	BE	0	--
84	05318	435	3.0	BE	3.3	CB
88	03739	435	2.9	BE	4.1	BE

*Below specifications.

Tensile strengths, Al/Al pad bonds. - Ten devices were picked at random and delidded for investigation of the Al wire to Al pad ultrasonic bonds. Both the emitter and base pad bonds were tensile tested. These bonds were tested with the same equipment and at the same 45 deg angle as the post bonds. The results of these tests are listed in Table J-6. The average pull strength of these bonds is 2.2 grams which just exceeds the minimum per specification. Four of the ten devices are considered acceptable.

Moisture analysis of package ambient. - Moisture analyses were carried out on five devices mounted individually in a test holder designed specifically for the TO-18 package which was plumbed into the carrier gas system of a gas chromatograph. Sampling was accomplished by driving hollow pins through the case of the package and sweeping the ambient gas out of the package through one of the pins and into the instrument for analysis. Results obtained are presented in Table J-7.

TABLE J-6
PAD BOND YIELD STRENGTH DATA

No.	Part No.	Lot No.	Emitter Pull Strength (grams)	Mode of Failure	Base Pull Strength (grams)	Mode of Failure
15	03719	435	0	--	0	--
19	03691	435	2.6	BE	2.7	BE
18	03681	435	1.9	BE*	2.5	BE
14	03773	437	2.7	BE	0	--
23	00143	433	3.4	BE	2.8	BE
26	00256	433	3.1	BE	2.4*	CB
32	00821	433	0	--	3.0	BE
34	00943	433	2.1	BE	2.4	BE
38	00626	436	3.4	BE	4.2	BE
43	00650	436	5.1	BE	0	--

*Below specification.

TABLE J-7
MOISTURE CONTENT OF SELECTED DEVICES

Sample No.	Part No.	Lot No.	% Water by Weight	Absolute H_2O Content
11	03703	435	Lost	--
10	03711	437	85	1.51×10^{-4} grams
41	00638	436	77	1.29×10^{-5} grams
51	00727	436	53	2.0×10^{-5} grams
52	00731	438	88	1.47×10^{-5} grams

These moisture levels are considered to be intolerably high.

Package ambient analysis. - Analysis of package gas composition was performed on five TO-18 packages by gas chromatography using helium as a carrier gas. In view of the excessive moisture levels found in the five previous analyses, the water peak in this group also was estimated. All five devices had survived fine and gross leak tests and static and dynamic electrical tests. Chromatography was performed on a dual column system consisting of a 12 ft x 1/8 in. Poropak Q column and an 8 ft x 1/8 in. Molecular Sieve 5 A column. Conditions employed are as follows:

Columns	- Dual, Molecular Sieve 5 A, Poropak Q
Temperature	- 70°C
Carrier Gas	- Helium
Carrier Pressure	- 20 psi
Bridge Current	- 300 ma

The analytical results are given in Table J-8. These results indicate that the intended ambient was pure nitrogen. However, considerable contamination with oxygen is present, and the moisture levels are again excessive, in all cases exceeding the dew point of the contained gas. In view of this latter fact the moisture levels given in Table J-8 are split into gas phase content at 100 percent relative humidity (25 C) and liquid phase.

The gas ambient compositions in these devices appear to warrant investigation of their manufacture. The presence of oxygen suggests ineffective process control of lidding atmospheres. The presence of moisture is more difficult to explain (because the samples were hermetic) but may be due to incomplete curing of the Pyroceram prior to lidding.

Electron microprobe analysis of Al/Al bonds. After ambient analysis these devices were delidded and examined microscopically (optical) for corrosion. In spite of the excessive moisture no evidence of metal corrosion was found. Electron microprobe analysis of one of these specimens yielded no evidence of the presence of corrosive contaminants. Taken together these observations indicate that the manufacturer employs a clean process except for the anomalies noted in the previous paragraph.

In summary, this group of devices is characterized by several defective conditions which could impair long term electrical performance. These defects are: excessive voids in die-header bonds, gross leak failures, h_{FE} degradation, inferior post bonds and pad bonds and extreme moisture levels in packages. Other anomalous conditions are present to an extent of less than ten percent of the sample and do not necessarily portend serious reliability problems or indicate substandard control of process techniques. The manufacturer could avoid most of these problems by applying strict quality control measures.

TABLE J-8
GAS CONTENTS OF SELECTED DEVICES

Sample No.	Part No.	Lot No.	O_2% by Volume	N_2% by Volume	H_2O in Gas Phase	Gas Phase ppm H_2O (weight)	Excess H_2O Liquid
73	02475	434	42.7	54.4	1×10^{-6} gms	18000	3.2
71	02426	434	11.3	85.8	5×10^{-7} gms	18000	3.14
72	02458	434	5.1	92.0	4×10^{-7} gms	18000	2.84
45	00666	438	3.7	93.4	4×10^{-7} gms	18000	2.7
46	00673	436	11.5	85.6	2×10^{-7} gms	18000	2.8

Accuracy ± 5 Percent

APPENDIX K. INSTRUMENTAL CAPABILITY PROFILE

INSTRUMENTS FOR FAILURE ANALYSIS

Instrument	Abnormality Observed (physical)	Related Failure Modes	Probable Failure Mechanisms
Dye penetrant	Cracks in package seals	Leaks	Inversion (change in semiconductor type)
Etching and microscopy	Dislocation distribution	Soft junction (gradual rather than sharp increase in current characteristic across junction)	Electrical parameter drifts
	Pits, cracks, and chips	Opens	Mechanical failure
	Pinholes and cracks in oxide insulating layer	Shorts	Migrating of metallization
Binocular microscope (3-120X magnification)	Inhomogeneity (Oxidation, contamination, intermetallics or rub marks.)	Weak bonds or electrical leakage	Poor surface wetting Migration of charged contaminant causes inversion. Intermetallics form by diffusion. May have resulted from overheating.
	Opened bonds	Electrical open circuit	Mishandling, overheating, or contaminated surface.
	Cracked dice	Open circuit or shift in resistance	Pressure during die or lead bonding.
	Cracks in package lead seals	Leaks	Rough handling, misalignment, thermal mismatch, or bubbles in glass.

INSTRUMENTS FOR FAILURE ANALYSIS (Cont)

Instrument	Abnormality Observed (physical)	Related Failure Modes	Probable Failure Mechanisms
Binocular microscope (3-120X magnivication) (continued)	Pits and pyramids on dice	High leakage or hot spots at thinner base areas	Poor epitaxial growth control results in thin localized base areas (after diffusion).
	Poor registry or masking	High leakage, shorts or opens	Narrow insulating path may short, or inversion may cause high leakage current.
	Scratches on dice or intraconnects	Open or high resistance	Handling and testing.
	Microplasma in operating device	Soft junction	Current concentrates at stacking faults, dislocations, or thin spots in base.
Phase contract microscope	Stacking faults	Soft junctions	Shifting electrical parameters.
	Transparent contaminants	Surface inversion	Ionic contaminants migrate and result in reverse leakage.
	Improper oxide metallization topography	Electrical leakage, shorts, or opens	Misalignment creates narrow insulating paths which short or leak as result of inversion.
Dark field microscope	Photoresist residues, dust	Inversion	Diffusion of charged contaminants.
	Bubbles in Sealant glass	Leaks	Inversion.
Interferometer	Oxide and surface topography varies from design	Electrical leakage, shorts or opens	Misalignment creates narrow insulating paths which short or leak as result of inversion.

INSTRUMENTS FOR FAILURE ANALYSIS (Cont)

Instrument	Abnormality Observed (physical)	Related Failure Modes	Probable Failure Mechanisms
Interferometer (continued)			Meager contacts melt and open.
	Oxide thickness varies from design	Stray capacitance, electrical leakage or inversion	Metal diffuses through oxide and causes leakage.
	Metal thickness varies from design	Opens	Thin metal areas burn out.
Electron microscope (magnifies to 100, 000X)	Dislocation and stacking faults distribution	Soft junctions	Precipitates in bulk silicon.
	Contaminant and corrosion location	Weak bonds or electrical leakage	Electrochemical reaction.
	Etch pits, scratches dust, and deposit roughness	Opens, shorts, or parameter drift	Surface roughness cause thin spots in conductor deposits which may heat and melt.
	Pattern alignment and topology errors	Shorts or opens	Meager contacts burn open. Narrow isolation areas short across.
	Undercut etched edges	Opens or inversion	Contaminants cause corrosion and opens or migrate and cause inversion.
	Weld porosity	Contaminants	Contaminants cause corrosion and opens or migrate and cause inversion.
	Porous diffusion products	Contaminants or weak bonds	Contaminants cause corrosion and opens or migrate and cause inversion. Kirkendall effect (mismatched diffusion rates of dissimilar metals)

INSTRUMENTS FOR FAILURE ANALYSIS (Cont)

Instrument	Abnormality Observed (physical)	Related Failure Modes	Probable Failure Mechanisms
Electron Microscope (magnifies to 100,000X) (continued)			causes voids. Thin spots may heat and melt.
	Scribe cracks	Opens (if cracks propagate)	Thermal or mechanical stress causes cracks to propagate.
Radiographic equipment	Voids in welds	Leaks in package; opens if voids are associated with bonding of wires and package to IC die	Inversion corrosion, poor welding control.
	Metal migration	Shorts or opens	Kirkendall voids form weak bonds.
	Contaminant particles	Shorts	Mobile metallic contaminants shorts.
	Cracks	Opens or leaks	Cracks propagate and open connections.
	Long wires	Shorts	Wires sag, cause shorts.
	Misalignment of metal parts	Leaks, opens, or shorts	Misalignment causes weak bonds, shorts, opens, or leaky packages.
Controlled etching	Depth of inversion charge	Inversion	Inversion
X-ray diffraction	Identity of contaminant compounds or corrosion product compounds	Weak bonds or electrical leakage	Electrochemical reaction
	Identity of materials	Abnormal electrical parameters	Drift of electrical parameters.

INSTRUMENTS FOR FAILURE ANALYSIS (Cont)

Instrument	Abnormality Observed (physical)	Related Failure Modes	Probable Failure Mechanisms
Metallograph	Observes same abnormalities as binocular microscope; also:		
	Poorly adherent interconnects or bond structures	Opens	Improper deposition and/or bonding conditions.
	Abnormal junction depth (by angle lapping)	Improper electrical characteristics.	Bad junction depth.
	Voids in thermocompression bonds	Bond has high electrical and/or thermal resistance and may be mechanically weak	Hot spots, poor electrical characteristics or opens.
	Incomplete or poor welds	Leak in package	Faulty package seals.
	Thin or non-adherent plating	Poor joints	Opens bonds and/or package leaks.
Electron backscatter thickness meter	Thickness of oxide, plating or photoresist	Stray capacitance, electrical leakage, inversion or opens	Electrical parameter drift
Instrument	Abnormality Observed (chemical)	Related Failure Modes	Probable Failure Mechanisms
Hot stage metallograph	Contaminant melting point and reactivity (for identification)	Weak bonds or electrical leakage	Electrochemical reaction.
	Interdiffusion of metals, for example, Al-Au, Mo-Au, Ti-Au, Kovar-Au	Parameter drift	Intermetallics form from diffusion.
	Whisker growth	Shorts or opens	Metal whiskers grow and make shorts.
			Removal of metal leaves opens.

INSTRUMENTS FOR FAILURE ANALYSIS (Cont)

Instrument	Abnormality Observed (chemical)	Related Failure Modes	Probable Failure Mechanisms
Hot stage metallograph (continued)	Grain growth	Parameter drift	Drift in braze, bond, or interconnect resistance.
	Surface diffusion or metal films	Shorts, opens or parameter drift	Metal films cause shorts or inversion. Lack of diffusion barriers.
Electron diffraction	Contaminant crystal structure and identity of intermetallic compounds	Weak bonds or electrical leakage	Electrochemical reaction.
	Deposit crystallinity	Open, shorts, or parameter drift	
Low-energy electron diffraction	Presence of absorbed substances in surface	Inversion	Migration of charged absorbates causes inversion.
Electron microprobe (elemental chemical analysis)	Contaminant or rub mark residue identity and map	Weak bonds or electrical leakage	Migration of charged contaminants causes inversion.
	Dopant and Dopant concentration	Related to process control	
	Intermetallic analysis	Weak bonds or electrical leakage	
	Corrosion product identity	Weak bonds or electrical leakage	
	Deposit topography map by chemical element	Opens, shorts, or parameter drift	
	Deposit thickness map by chemical element	Opens	Thin areas melt and open.
	Crack, pit, and pinhole maps	Opens or shorts	Thin or narrow areas on interconnects open. Pinholes.

INSTRUMENTS FOR FAILURE ANALYSIS (Cont)

Instrument	Abnormality Observed (chemical)	Related Failure Modes	Probable Failure Mechanisms
Electron microprobe (elemental chemical analysis) (continued)	Junction misalignment or movement	Electrical leakage, shorts, opens, or inversion	Migration of metal is evidence of inversion.
	Opens, short and current and/or voltage nonuniformity map	Abnormal electrical parameters	Cause of abnormal electrical parameter may pinpoint failure mechanism.
Gas chromatograph	Abnormal package ambients	Inversion or grain drift	Absorption, then charge migration causes inversion.
	Leaks (by presence of air or test fluid)	Inversion or grain drift	Absorption, then charge migration causes inversion.
Mass spectrograph	Leaks. Also: reaction of device to ambient changes in the spectrograph	Inversion or grain drift	Absorption, then charge migration causes inversion.
Gas chromatograph and mass spectrograph in combination	Leaks. Also: reaction of device to ambient changes in the spectrograph	Inversion or grain drift	Absorption, then charge migration causes inversion.
Infrared absorption spectrograph	Thin oxide	Shorts or electrical leakage	Abnormal electrical parameters
	Abnormal oxygen content in silicon	Drift of electrical parameters	Recombination centers
	Abnormal epitaxy thickness	Slow switching, punch-through	Drift of marginal electrical parameters.
	Impure photoresist	Inversion	Migration of impurities.
	Water	Surface current leakage	Water vapor enters through leak.
Emission ultraviolet and visible spectrographs	Analysis and identity of contaminants	Parameter drift, opens, inversion	Contaminants migrate and change electrical properties or cause corrosion.

INSTRUMENTS FOR FAILURE ANALYSIS (Cont)

Instrument	Abnormality Observed (chemical)	Related Failure Modes	Probable Failure Mechanisms
Visible and ultra-violet absorption spectrographs	Analysis and identity of contaminants	Parameter drift, opens, inversion	Contaminants migrate and change electrical properties or cause corrosion.
Neutron activation analyzer	Same as emission spectrograph but at lower concentrations	Parameter drift, opens, inversion	Contaminants migrate and change electrical properties or cause corrosion.
Instrument	**Abnormality Observed (mechanical)**	**Related Failure Modes**	**Probable Failure Mechanisms**
Strain gauges	Loose headers or dice	Thermal	Nonadhesion of braze evident from thermal expansion of can. Poor thermal path causes overheating.
	Poorly brazed headers or dice	Thermal	Nonadhesion of braze evident from thermal expansion of can. Poor thermal path causes overheating.
Bubble tester	Gross leaks in packages	Channeling or inversion	Nonadhesion of braze evident from thermal expansion of can. Poor thermal path causes overheating.
		Opens or shorts	Corrosion causes opens or shorts.
Helium leak tester or Radioflo tester	Small leaks	Uncontrolled package ambient causes inversion and corrosion	Charged absorbates from ambient migrate and cause inversion. Corrosion by ambient causes opens or shorts.

INSTRUMENTS FOR FAILURE ANALYSIS (Concluded)

Instrument	Abnormality Observed (mechanical)	Related Failure Modes	Probable Failure Mechanisms
Thermal plotter	Hot spots due to voids	Excess currents	Material degradation.
	Hot spots due to thin base areas	Excess currents	Uneven diffusion and thin base areas.
	Hot spots due to dislocation or stacking faults	Excess currents	Faster diffusion along fault causes thin base area.
Curve tracer	Shorts	Shorts	Sagging wire, punch through or surface creep of metal.
	Opens or intermittent contacts	Opens or intermittent contact	Mishandling, intermetallic formation.
	Soft junctions	Soft junctions	Surface leakage.
	Abnormal resistance	Abnormal resistance	Mechanical damage or corrosion.
	Leakage currents and inversion	Inversion	Surface charge migration or surface contamination.

SENSITIVITIES OF INSTRUMENTS

(Physical Properties)

Instrument and Procedure	Parameters Measured	Sensitivity, * Resolution or Power
Optical microscope	Surface topography	3X to 2000X, 0.5 micron
Phase contrast	Stacking faults	To 1000X, 0.5 micron
Electron microscope	Crystal imperfections	10 angstroms, 300,000X
	Dislocations & stacking faults	100 angstroms apart
Interferometer	Film thickness or surface roughness	
Single beam		300 angstroms
Multiple beam		25 to 10 angstroms
Proficorder	Surface texture	100 angstroms
Contour projector	Surface contour along a line shadow	10 microns
Ellipsometer	Film thickness, dielectric	2 angstroms
	Film thickness, silicon	10 microns
Electron diffractograph		
Reflection	Crystal character	
Transmission	Crystal lattice parameters	0.01 angstroms
Low energy electron diffraction (400)	Surface structure (generally) indicates presence of absorbed materials	1 to 2 atomic layers deep
Scanning electron microscope	Device topography, voltage contrast	0.05 to 0.5 micron, 50,000X
Radiography unit	Inner topography	0.1 micron
X-ray diffraction	Phase analysis	0.5% to 10%
	Crystallite size	0.5 to 0.3 and 10 to 1,000 micron ranges
	Dislocation mapping	Over 5 microns apart 5,000 psi or 500 ppm strain over area 0.010 in. across

SENSITIVITIES OF INSTRUMENTS (Cont)

(Physical Properties)

Instrument and Procedure	Parameters Measured	Sensitivity, * Resolution or Power
Strain gauges	Strain, thus stress	1 ppm over 0.015 in, 100 pico strains
Tensile testers	Bond strength	0.1 gram
Thermal plotter	Surface temperature	2°C over 0.35 mil. 0.5°C over 1 mil diameter
Etching	Dislocations or stacking faults	10 microns apart
	(Electrical Properties)	
Oscilloscopes	Current and Voltage	10^{-9} amperes
Ammeters, electrometers	Current	10^{-17} amperes
Voltmeters, Potentiometer	Voltage difference	5×10^{-10} volts
Capacitance bridges	Capacitance	10^{-17} farads, static
Ohmmeter, bridge	Resistance, impedance	10^{-8} to 10^{14} ohms

SENSITIVITIES OF INSTRUMENTS (Cont)

(Chemical Properties)

Instrument and Procedure	Parameters Measured	Sensitivity, * Resolution or Power
Absorption spectroscopy atomic	Detection of metallic & semi-metallic elements	65 elements in ppm.
Infrared, attenuated total reflection	Surface composition	Depth is about 1 wavelength, depending on the angle of reflection.
X-ray spectroscopy	Chemical composition, oxidation state	10 to 1, 000 ppm
Emission spectroscopy	Chemical composition	
Visible		1 ppm of most elements
X-ray		10 ppm of most elements
Neutron activation	Concentration of impurities	1 ppb of most elements, 1 ppm of oxygen
Mass spectroscopy	Chemical composition	
Gas		0.02 to 200 ppm 10^{-13} torr
Spark		1 ppb of many elements 20 to 200 ppb of H, N, C, 0
Sputter		1 to 10 ppm in surface which is removed at 10 to 100 monolayers per second. Area 0.1 mm across may be analyzed.
Gas chromatography	Chemical composition	1 ppb hydrocarbons on milligram sample 1 ppm H, 10 ppm Ar, 50 ppm water
Electron spin resonance	Dangling bonds, free radicals, excited states	10^{11} H electron spins per gauss with 1 second integration time.

SENSITIVITIES OF INSTRUMENTS (Concluded)

(Electrical Properties)

Instrument and Procedure	Chemical composition	Sensitivity, * Resolution or Power
Nuclear magnetic resonance	Molecular structure	2, 000 ppm, 3×10^{18} spins/cm^3
Charged particle spectroscopy	Surface contaminant identification	Atomic number difference of 1
Electron microprobe X-ray mode	Identification & amount of chemical elements	10 ppm in bulk (1, 000 ppm for lightest elements)
Backscattered electrons	Relative At. No variations	0.5 to 1 micron
Speciment current mode	Device topography	
Wet chemistry	Chemical composition	
Colorimetric		10 picograms
Fluorimetric		1 picogram of most elements
Ion exchange		Concentrates ions 100X
Carbon analyzer	Carbon determination	10 ppm
Vacuum fusion	Chemical composition	50 ppb H, 200 ppb or 0 or N

*Sensitivities quoted are the highest given in apparatus maker's literature.

APPENDIX L. MEASUREMENT OF COMPRESSIVE STRESS IN OXIDE LAYERS

The compressive stresses associated with oxide layers of various thicknesses and defect densities are listed in Table L-1. Determinations were made by Proficorder tracing arranged to give both the step thickness of an etch mark and the delta curvature, or deflection, over a given trace distance produced by removal of an oxide layer. From the deflection data the compressive stress is computed using the following relation:

$$\theta_o = 4E_s Z_s^2 d_s / 3Z_o l^2 \qquad \text{(L-2)}$$

where E_s is the modulus of elasticity of silicon (27.3×10^6 psi), Z_s and Z_o are the thicknesses (inches) of the silicon and oxide layers respectively, d_s is the deflection produced by oxide removal and 1 is the length of Proficorder traverse, yielding the compressive stress, θ_o, in psi. Mutually perpendicular Proficorder traces were made on each wafer.

Error in these measurements arose from two sources: step thickness determinations (±250Å) and curvature irregularities in about 50 percent of the Proficorder traces. The thickness error is apparent from Table L-1where the calculated stresses deviate from the average most for the thinner oxides (i.e., where the measurement error is proportionately greater). There is, however, no apparent change in stress with oxide thickness, as was deduced earlier from more limited evidence. Curvature irregularities were dealt with by area summation technique applied to the regions enclosed by the pre- and post-oxide removal curve traces. This resulted in an improvement of about 50 percent (to ±6.4 percent) over earlier computations.

The magnitude of the compressive stress in the oxide (4×10^4 psi) is considered substantial enough to rupture a large proportion of existing thin spots in the oxide in cooling from the oxidation temperature. Other thin spots, although fractured, may be held together by the residual compressive stress and escape detection by electrophoretic decoration. These spots appear in turn to be opened up (i.e., they become detectable by decoration) by the convex curvature and relief of stress introduced by back oxide removal. The convex curvature is, of course, readily apparent from the Proficorder traces.

TABLE L-1
CORRELATION OF DEFECT DENSITIES WITH OXIDATION AND STRESS

Run	Oxidation		Defects vs Stress (No./Wafer)			Measured Stress[d] (Psi x 10^{-3})
	Time, $t^{1/2}$ (Minutes)	Thickness (Angstroms)	No Stress[a]	Full Stress[b]	Partial Stress[c]	
A	2.24	1720	131	545	987	40.3
B	3.16	1995	35	511	644	49.5
C	3.87	2590	10	343	479	36.8
D	4.47	3125	5	111	146	40.0
E	5.00	2945	8	170	353	42.1
J	5.00	3760	0.5	205	333	37.3
F	6.32	4010	1	31	140	41.4
G	7.81	5325	0	24	90	42.6
					Av:	41.3 ±6.4%

a. Silicon etch pit count produced before cooling.
b. Decoration count after cooling.
c. Decoration count after removal of back oxide layer.
d. By Proficorder trace method described in text.

APPENDIX M. EFFECT OF HYDROGEN ON INTEGRATED CIRCUIT PERFORMANCE

Present process control of packaging techniques is inadequate in several respects and fosters a variety of modes of failure. These include variations in gas ambient compositions, nonhermeticity, corrosion of leads, inferior heat sinks and cracked dice. These problems often are interdependent and augment each other or additional failure modes. Nonhermeticity may contribute to variations in package ambients and corrosion of leads; inferior heat sinks may contribute to cracked dice, degradation of h_{FE} and metallization mass transport, all of which are current reliability problems. Associated with the problem of nonhermetic package is the lack of an adequate gross leak test. The objective of this investigation is to locate the sources of these problems in process control techniques and to seek remedies therefor.

Previous program activities in this area have been limited mainly to the analysis of package ambients and the investigation of the effects of certain of these gases on transistor function. Using mass spectrometric and gas chromatographic techniques a large variety of gaseous species were detected in the packages of transistors and integrated circuits. It was shown that the presence of moisture seriously affected the low temperature performance of mesa transistors but not of planar transistors. It also was shown that baking for limited periods in a hydrogen ambient produced irreversible increases in the betas of some groups of transistors but not in others. General conclusions could not be reached because of the limited sampling and the insufficiency of available process histories.

Improved facilities were established for similar investigations on integrated circuits providing considerable flexibility in the selection of test ambient compositions, temperatures and pressures. Investigations also were extended to the major problems indicated above. The general approach to these problems consisted of examining current practice for clues to the process origins of component defects followed by chemical and instrumental failure analysis by established procedures.

Environmental testing on a first group of integrated circuits was inconclusive as a result of poor versatility of the external circuitry. A second group of 15 type 947 GPA integrated circuits were selected and prepared for environmental testing using an improved electrical connection network which permitted both beta and voltage breakdown measurements on the output section without the need to rebond any components inside the package. However, four separate connections were needed for each device which limited the number inside the vacuum chamber to seven plus two control devices.

The devices were placed on a special pyrex platen grooved to accept each device lead in a separate 0.010 inch deep by 0.025 inch wide slot (Figure M-1). Gold-plated Kovar 0.003 by 0.010 inch ribbon lead wires connecting the devices to the bakeable high vacuum feed-through connector inside the chamber were attached to the devices by thermal compression welding. Exact positioning of each device and lead wire on the platen was maintained by pyrex cover plates mechanically clamped to the base platen. Location and clamping is such that stress loads are not applied to

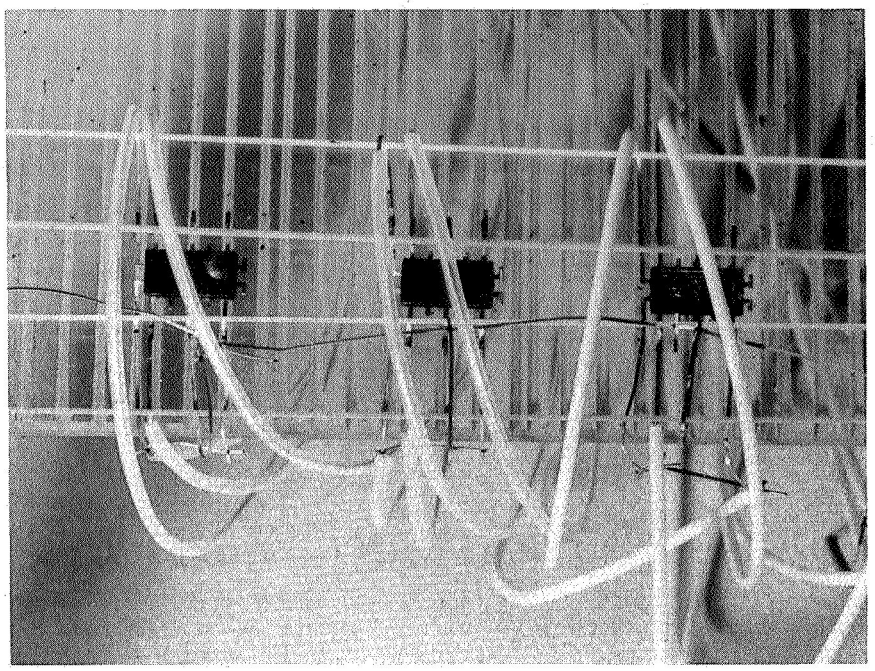

Figure M-1. – Integrated Circuitry Mounted on Paper Platen

either the device or lead. Insulation of leads between the vacuum feed-through connector and platen was teflon sleeving which had been punctured along each length to reduce virtual gas loads. This new mounting configuration eliminated the use of any bonding adhesives to attach either the devices or connecting leads.

It was found necessary to develop special methods of delidding and lead bonding to eliminate mechanical failures due to handling. These problems were solved by constructing a special furnace for freeing the lids from the packages and by adapting a split tip welder of Autonetics design to the bonding process. Electrical tests on a group of five IC's performed before and after the applications of both techniques revealed no change in BV_{ceo}, BV_{cer} and beta, thereby establishing nondestructiveness of the procedures.

The initial test sequence adopted for nine Norden IC's was designed to approach ambient survival limits cautiously. It was found that moderate heating in vacuum (100 C and 150 C) produced no significant change in the room temperature characteristics although large changes were noted at the elevated temperatures. The reversible nature of the high temperature effects indicate generally good device stability.

In a second test sequence, the nine IC's (two of which remained lidded) were thermally cycled from room temperature to 150 C in vacuum and in "forming gas" (15 percent H_2 and 85 percent N_2). Only two of the devices (both delidded) survived this treatment, both of which returned to their original room temperature characteristics. The performance (average beta) of the two devices is plotted in Figure M-2 as a function of ambient treatment and indicates that an ambient of 15 percent hydrogen at 150 C produces no irreversible change, even under a constant electrical load of potentially destructive magnitude. This result once again suggests that the effects of hydrogen on the characteristics of most planar devices is largely insignificant. Figure M-2 also indicates that high temperature performance in the presence of hydrogen is scarcely different from that in vacuum.

Optical examination of the seven failed devices revealed that failure invariably occurred at the transistor emitter-to-pad metallization (Figure M-3). The failure mode was an open circuit produced by fusion and parting of the metallization, followed by contraction of the molten metal by surface tension into a module adjacent to the pad bond. The evidence indicates excessive heat generation in the vicinity of the emitter-base region combined with inadequate dissipation. It also appears possible that the failures may have been initiated by prior mass transport of metallization because the devices had endured previous periods of treatment at 150 C under the same current load without evidence of change. The two lidded devices not exposed to hydrogen suffered the same failures.

The two unlidded devices that survived the above thermal treatments were remounted on the Pyrex platen as shown in Figure M-4 and reinserted in the environmental test chamber shown in Figures M-5 and M-6. In this figure the right-hand

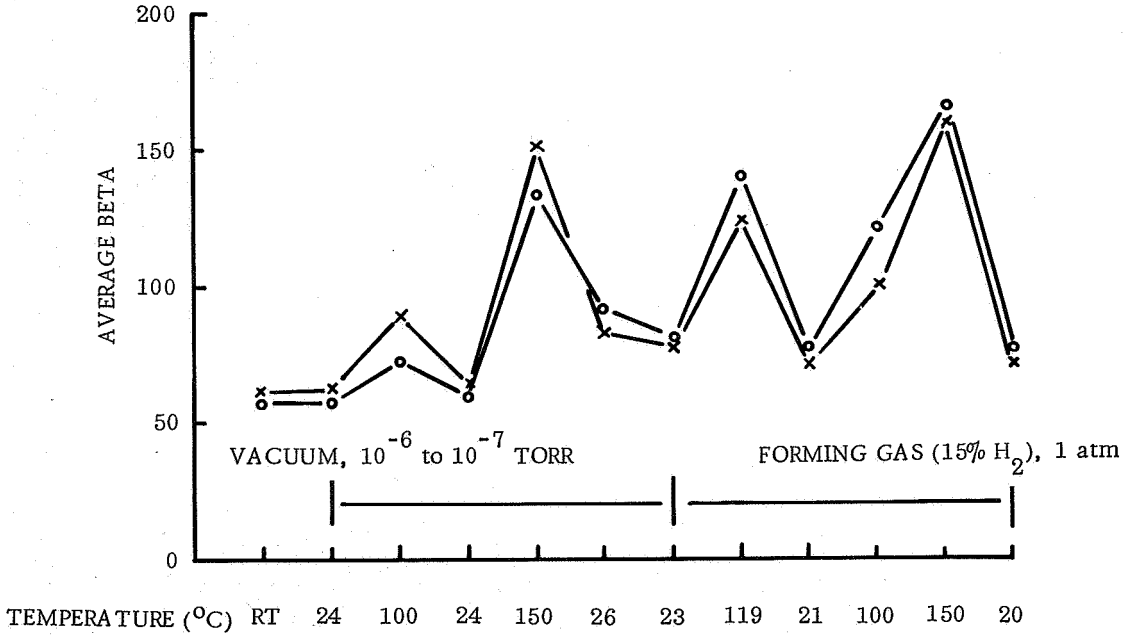

Figure M-2. – Behavior of Two Surviving Units in 15-Percent Hydrogen Ambient

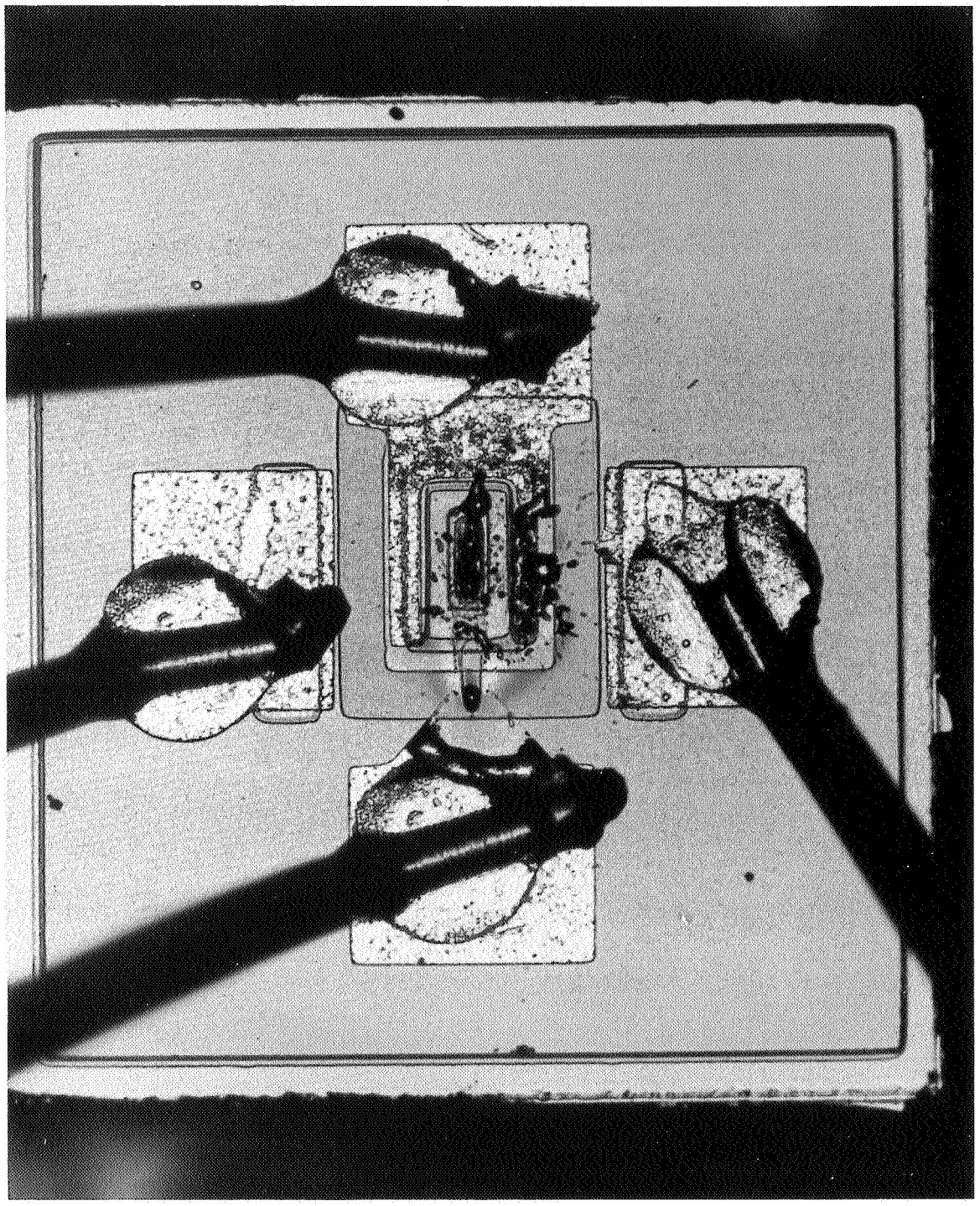

Figure M-3. – High Temperature Failure of Emitter-to-Pad Metallization

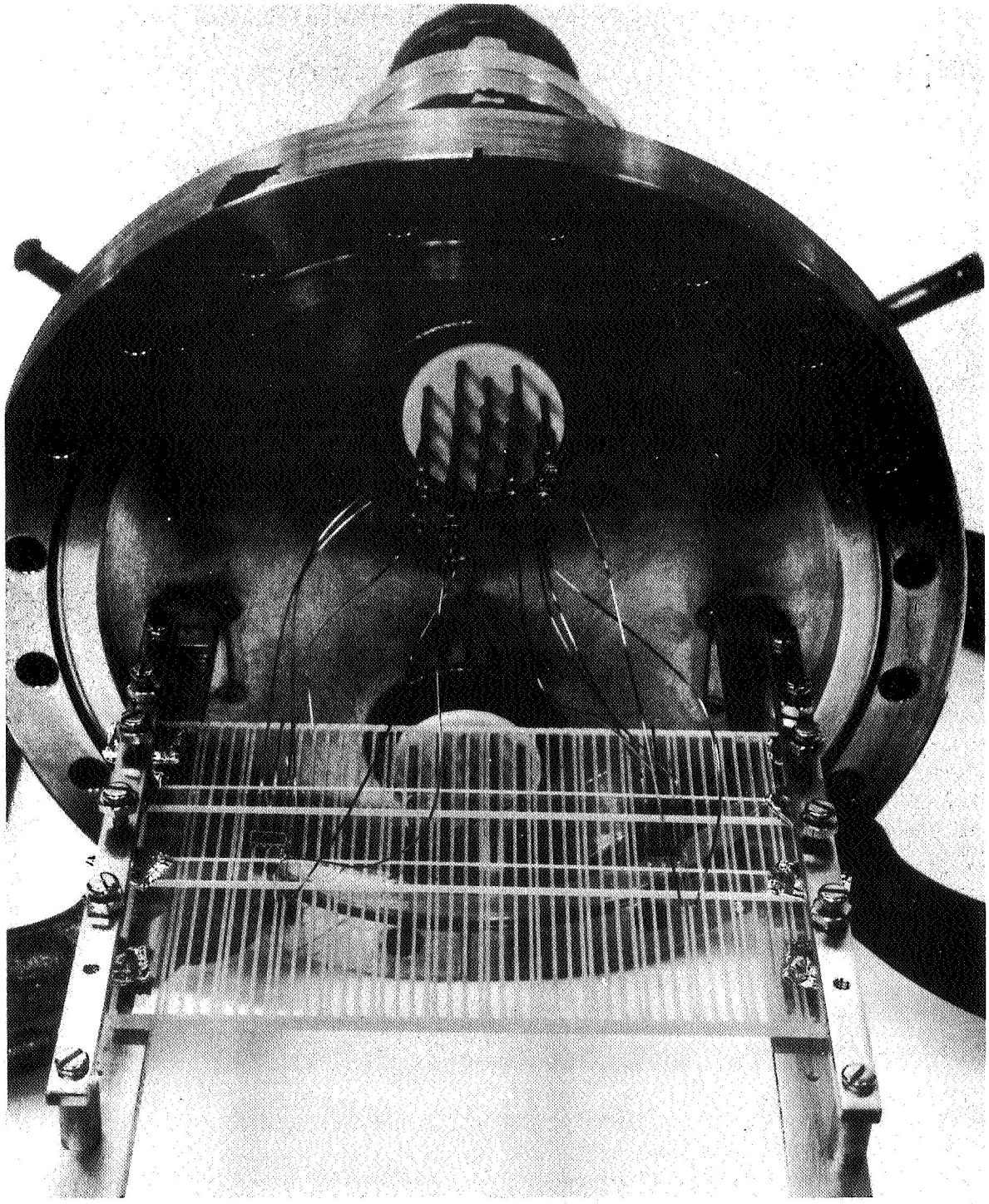

Figure M-4. – IC's Mounted on Platen

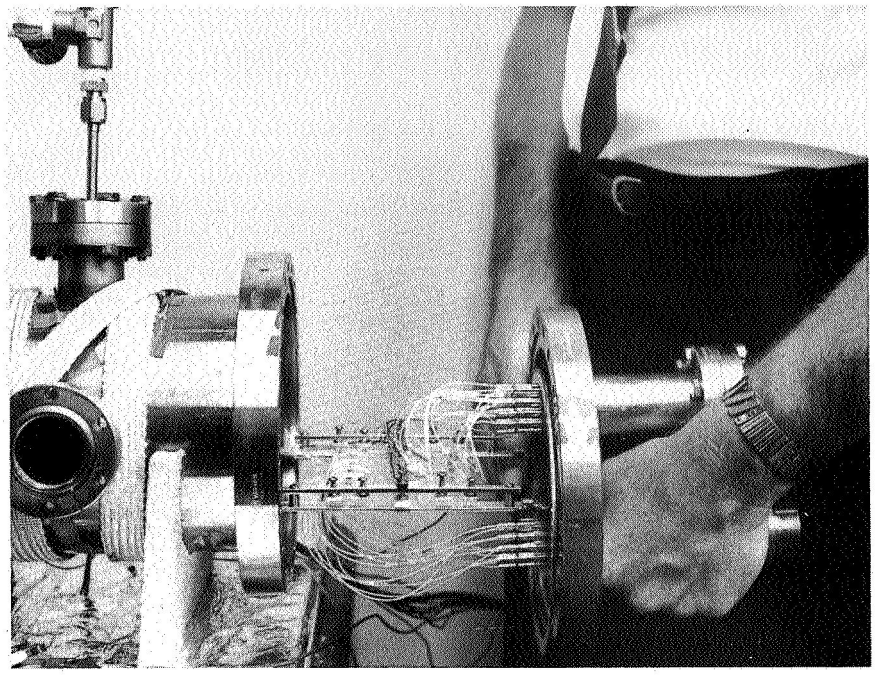

Figure M-5. – Insertion of Test Specimens Into Environmental Chamber

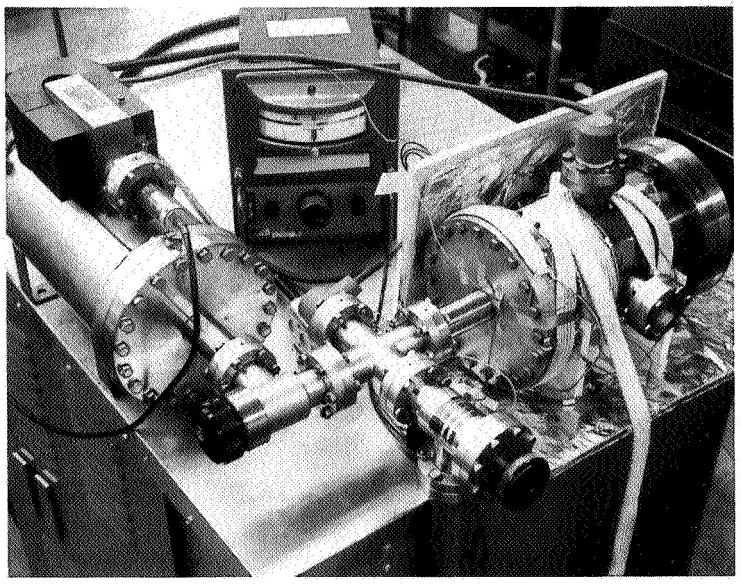

Figure M-6. – Environmental Test Assembly

cylindrical structure, mounted with thermocouples and heating tapes, is the assembled test chamber containing the devices and the left-hand cylindrical structure is the ion pump. Roughing pump, trap and gas metering devices are not shown. Thermal treatments to 350 C under vacuum and zero bias were conducted on the two IC's with the results shown in Figure M-7. All electrical measurements were made after cooling the chamber to room temperature but under continuous vacuum. The 350 C bake in vacuum was followed by a six hour treatment with forming gas at 250 C.

The upper curves (β-8 and β-13) in Figure M-7 represent the individual betas of the respective outboard transistors while the lower curves represent the combined betas simultaneously measured. It is seen that the individual betas are much more sensitive indicators of the effects of these treatments than the combined betas. Specifically, the individual betas drop significantly above 300 C. Heating in forming gas, however, tends to revive them, suggesting that the reason for the degradation in betas is a gas desorption process under vacuum at elevated temperatures. Rebaking the devices under vacuum again produced a drop in beta showing the process to be reversible. It was found in subsequent experiments that the transistor betas could be completely revived by baking either in a pure nitrogen atmosphere or a pure hydrogen atmosphere, thus eliminating hydrogen as a unique agent in the recovery of transistor betas. It is worth pointing out that this effect of hydrogen was observed on an earlier group of transistors as indicated in the second paragraph of this section. It is possible that this former group of transistors may have been vacuum baked prior to sealing, and that baking in nitrogen might have accomplished the same effect as hydrogen.

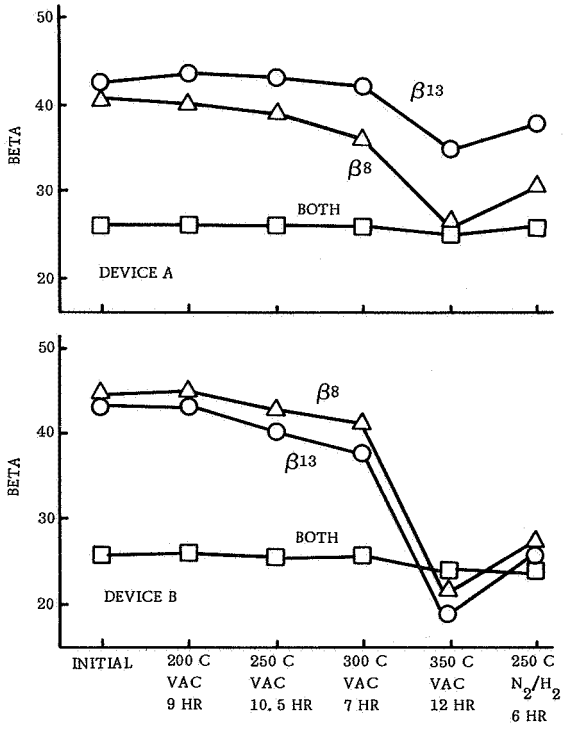

Figure M-7. – Effects of Vacuum and Forming Gas on Beta at Elevated Temperatures

A second group of five identical IC's was baked in nitrogen ambient without prior vacuum treatment. The baking was conducted at successively increasing temperature intervals with room temperature electrical testing after each bake. The final bake was at 525 C for nineteen hours. Except for one IC, which succumbed at a 375 C treatment (emitter/base short), these devices endured the entire sequence without significant degradation of room temperature electrical characteristics. Thus it was established that the thermal exposures used in earlier experiments were not excessive with respect to ambient temperature alone.

On the basis of present and earlier results it appears that the effects, if any, of hydrogen ambients on planar devices are curative rather than degradative and are not likely to occur at significant rates except at well above use temperatures. It also appears that hydrogen is not unique in this respect and that improvement in betas after vacuum baking may be effected by other "inert" gases, such as nitrogen. The precise reason for the effects of vacuum baking are not known at this time but should be further investigated in view of the deep space nature of NASA missions.

NEW TECHNOLOGY APPENDIX

A main innovation from the activities of this program has been the development and use of new techniques to locate and characterize structural defects in silicon dioxide layers used in the passivation of integrated circuit surfaces. These methods are described in Appendix F on page 113 under "Investigation of Methods For The Detection of Structural Defects in Silicon Dioxide Layers." Other process improvements investigated in this program are described in the section "Conclusions" on pages 37 through 43.