N 68 34253
NASA CR-66669

FINAL REPORT

THICK FILM ACTIVE DEVICES

Contract NAS 1-7340

June 1968

Prepared for

LANGLEY RESEARCH CENTER
NATIONAL AERONAUTICS AND SPACE ADMINISTRATION
HAMPTON, VIRGINIA

Prepared by

DEFENSE MICROELECTRONICS
DEFENSE ELECTRONIC PRODUCTS
RCA
SOMERVILLE, NEW JERSEY

Final Report

THICK FILM ACTIVE DEVICES

Contract NAS 1-7340

Prepared for

Langley Research Center
National Aeronautics and Space Administration
Langley Station
Hampton, Virginia 23365

Prepared by

Defense Microelectronics
Defense Electronic Products
RCA
Somerville, New Jersey

Author

Dr. W. Laznovsky

FOREWORD

The purpose of the study being performed under contract NAS 1-7340 is to continue to investigate the feasibility of thick film active devices fabricated solely by means of screen-printing techniques or other nonvacuum-deposition methods.

The main effort can be divided into the following tasks:

1) The development of precision printing processes to obtain the required dimensional accuracy of the TFT configuration.
2) The investigation of materials properties and compatibility. This includes an analysis of the functional characteristics of the various materials and component combinations in an effort to determine optimum parameters.
3) The preparation of a simple circuit as a vehicle to demonstrate the usefulness of thick film active devices as integral parts of all-printed thick film circuits.

This study was conducted by the Defense Microelectronics activity (DME) of RCA Defense Electronic Products in its Somerville, N. J., facility. Mr. M. R. Sherman was Project Leader for this program.

CONTENTS

THICK FILM ACTIVE DEVICES

By W. Laznovsky

Abstract Prepared by R. Stermer

The potential of randomly oriented screen-printed LdS layers as a basis for insulated gate field effect transistors has been established. The application of these layers in an all screened thick film transistor has had little success (very low gm and drain currents were obtained). The principal difficulties were surface layer roughness, and contamination of the channel region by electrode and dielectric layers during sintering.

A detailed analysis of these difficulties was made. Studies in screen printing dimensional control resulted in the development of a new precision press capable of depositing channel lengths of the order of 1 mil.

Section I

INTRODUCTION

This report covers the period from May 1967 to May 1968. The potential of using a screen-printed cadmium-sulfide layer as a semiconductor for field-effect amplification devices was established during the Applied Research in Thick Film Active Devices contract (see Final Report No. 66266, December 1966). The main emphasis of this program was then directed toward the development of techniques to deposit thick-film materials that are compatible with this type semiconductor. It should be noted that all TFT structures, whether called "thin film" or "thick film" TFTs when discussed in this report, are based exclusively on screen-printed layers of cadmium sulfide as semiconductor.

Various conducting and insulating pastes that are commercially available were used and evaluated with regard to their physical parameters.

In order to deposit the components whose dimensions are critical (i.e., source, drain, and gate electrodes) within the required accuracy, a precision-printing apparatus was built and evaluated. This printer utilizes an optical alignment system to ensure the proper accuracy. Source-drain gap widths approaching 1 mil were printed with a photo-etched metal-sheet aperture mask.

Several types of TFT structures were fabricated to evaluate form factors, materials, interfaces, etc. Extensive testing was conducted in order to analyze TFT structures and materials. These tests included X-ray diffraction, electron microscope photographs, mass spectrographic analysis, and measurements for Hall electron-mobility.

Section II

THIN AND THICK FILM TRANSISTOR STRUCTURES

A. THIN FILM TRANSISTOR

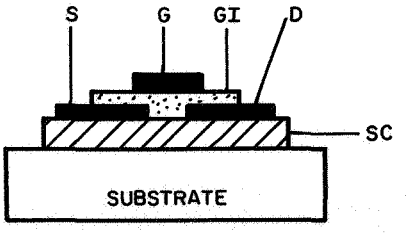
The original active devices based on screen-printed cadmium-sulfide semiconductors utilized vacuum-deposited aluminum films for the source, drain, and gate electrodes, and a vacuum-deposited silicon-monoxide film as a gate insulator. The basic arrangement of these elements is shown schematically in a cross-sectional view in Fig. 1; the elements are not drawn to scale. The following are the approximate thicknesses of the various elements:

Vapor-deposited metal films	1000 Å
Silk-screened CdS layer	2.5μm
Gate insulater	2000 Å
Substrate	25 or 40 mils
Channel width	varies between 0.1 mil and 10 mils

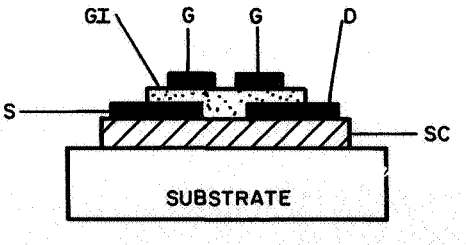
A channel width of 0.1 mil is produced by using a tungsten wire 0.1 mil in diameter as a masking element. A channel width of 10 mils is produced by utilizing separate evaporation steps for the source and drain electrodes; the same mask aperture is properly shifted and used in each of the two steps.

A precision mask changer that allowed all the various alignment steps to be performed was used in conjunction with a multiple-evaporation source, so that all thin film processing could be done in one pump-down cycle. The CDS layer was prepared by using conventional thick film methods that are described later in this report.

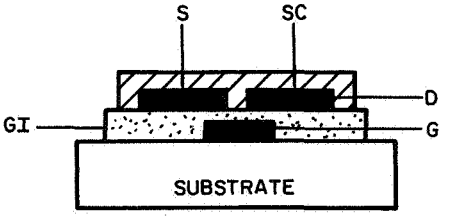
Whenever it was necessary to align patterns outside the bell jar, such as in the fabrication of intermediate structures (see Figs. 1d and 1e), a fixture that allowed the visual inspection of mask-substrate alignment for opaque substrate materials was used. Figures 2 and 3 show this alignment fixture without and with the mask-substrate holder on top of it.



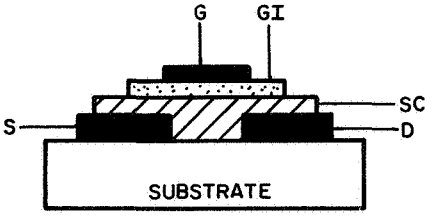
(a) "Thin film" TFT
S, D, G are vacuum-deposited Al
GI is vacuum-deposited Si O



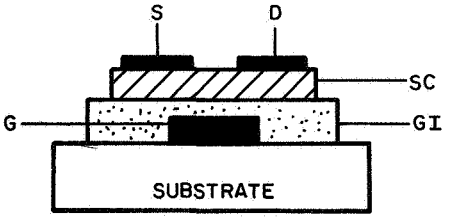
(b) "Thin film" double-gate TFT
S, D, G, GI are same as in (a)



(c) "Thick film" TFT
S, D, G are printed Au
GI is printed $BaTiO_3$



(d) Intermediate TFT
S, D are printed Au
G is vacuum-deposited Al
GI is vacuum-deposited Si O



(e) Intermediate TFT
G is printed Au
GI is printed $BaTiO_3$
S, D is vacuum-deposited Al

S = source electrode
D = drain electrode
G = gate

GI = gate insulator
SC = semiconductor
(screen-printed CdS in all cases)

Fig. 1. Cross-sectional view of various TFT structures.

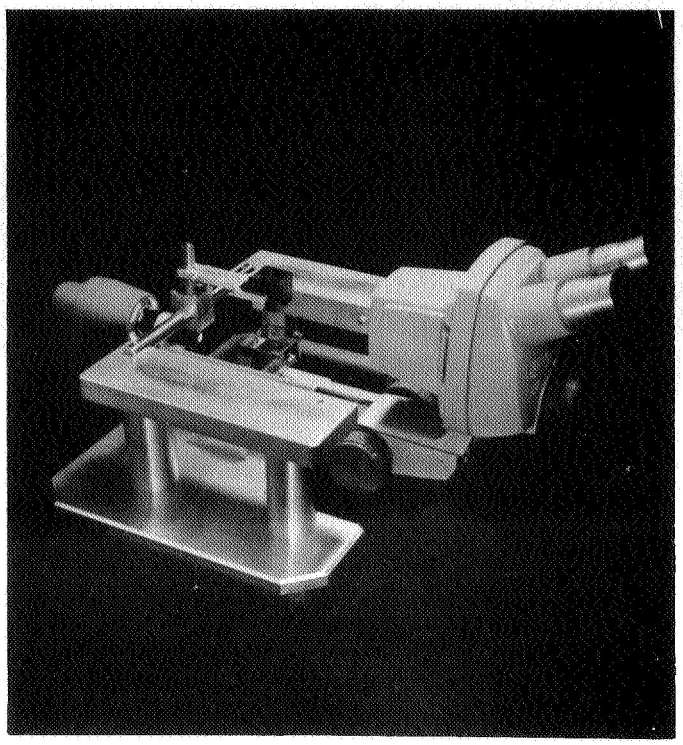


Fig. 2. Mask-substrate alignment fixture for opaque substrates (ceramic wafers).

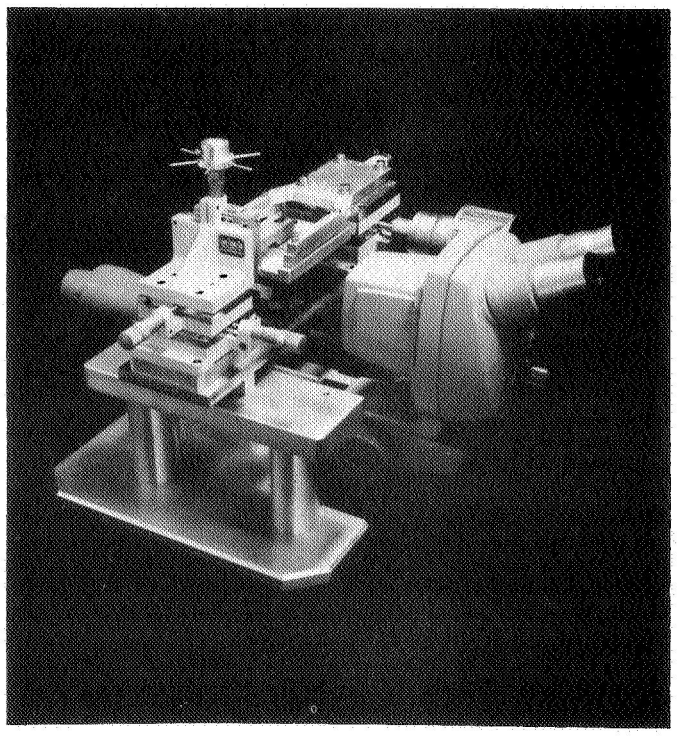


Fig. 3. Mask-substrate alignment fixture with mask-substrate holder in position.

The basic set-up is shown in Fig. 4. A light source illuminates the substrate from the bottom through the mask aperture. A beam splitter allows the visual inspection of the (opaque) substrate-mask alignment through a microscope without having to invert the substrate fixture or to use an inverted-type microscope.

The devices fabricated in this way showed surprisingly good results: transconductance values as high as 1000 microsiemens, with good saturation characteristics, and I_{DO} less than 1 microampere (as described in the 1966 Final Report[1]).

One modification of this TFT is indicated in Fig. 1b. A double-gate configuration replaces the single-gate configuration. It was found that the voltage of the gate over the drain area controlled the transconductance of the device (with the step voltage applied to the gate overlapping the source area of the channel).

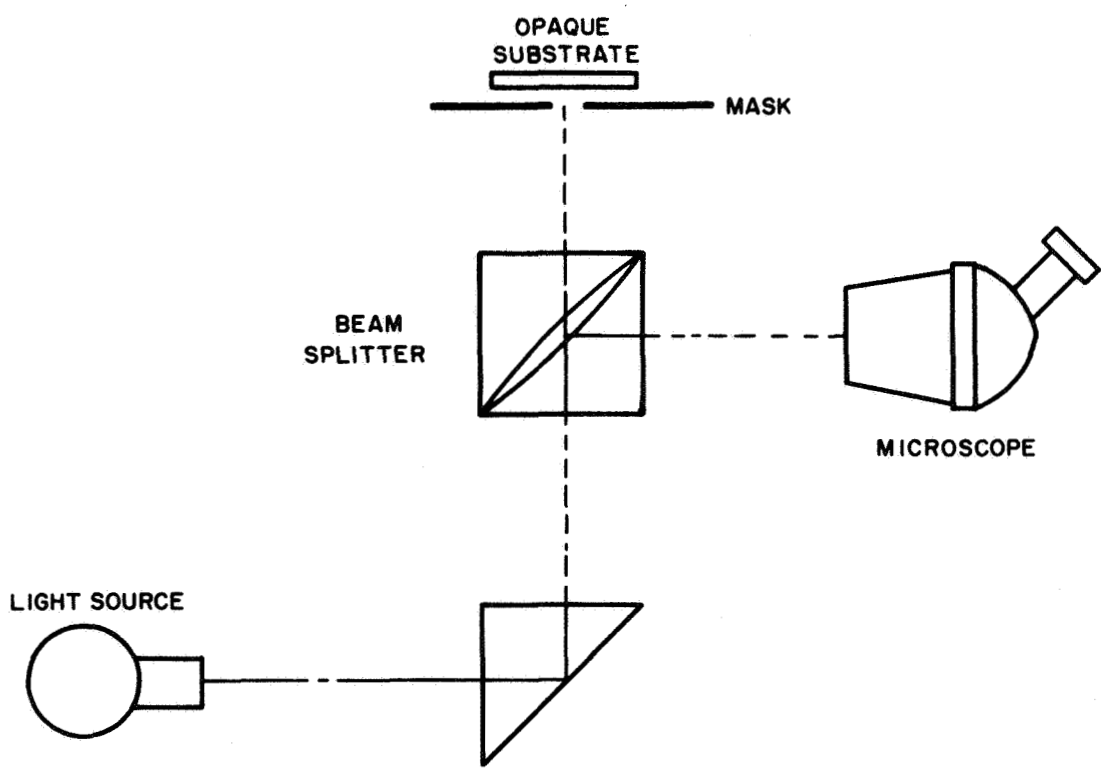


Fig. 4. Schematic of the mask—opaque-substrate alignment fixture.

The objective of this contract was the investigation of TFTs consisting of screen-printed and compatible structures, as well as materials and interfaces. Therefore, the experimental workwith thin film TFTs was discontinued when it was established that a screen-printed CdS layer could be used as a semiconductor for field effect devices.

B. THICK FILM TRANSISTOR

The basic configuration of the all-thick-film TFTS is shown in Fig. 1c. The electrodes and the gate insulator must be positioned under the CdS layer because the high-temperature firing cycles for these layers must be carried out before the CdS is deposited. However, this "inverted coplanar structure" cannot be used for the thin film device because the sintering process required for the CdS layer would corrode and destroy the thin film components.

The thickness of the electrode layers (generally fabricated of gold) and the gate insulator (barium titanate) is approximately 1 mil. The channel width is maintained between 1 mil and 3 mils by using the precision printer described later in this report.

Figure 5a shows the typical arrangement of three thick film active devices on an alumina substrate. The characteristics of the thick film transistors fabricated were less then desired. Typical characteristics of these devices can be seen in Figs. 5b and 5c.

C. INTERMEDIATE STRUCTURES

Typical intermediate structures are shown in Figs. 1d and 1e. These devices consist partly of thin film components made to pin-point certain difficulties connected with thick film processing. Almost all these structures were deposited onto ceramic substrates, primarily of alumina and 725 mils by 500 mils by 40 mils in size.

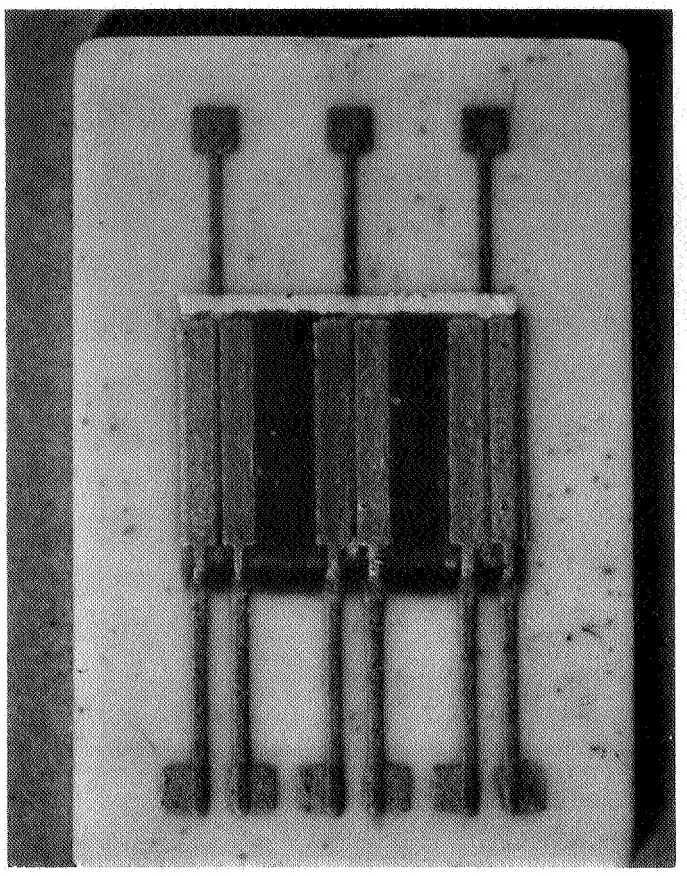


Fig. 5a. Three thick-film active devices on ceramic wafer. (Approximate magnification: 6X)

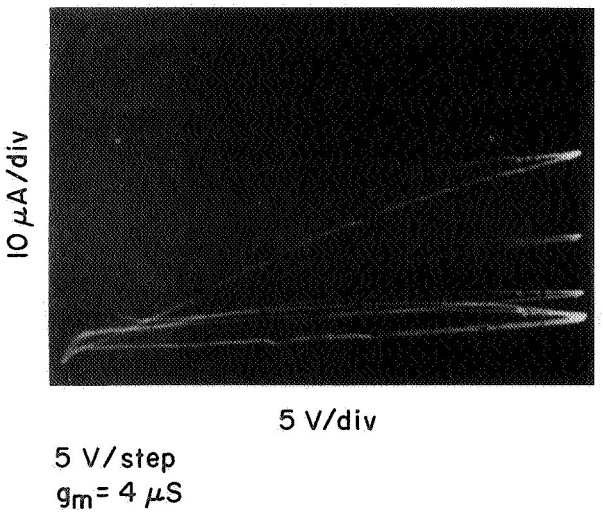


Fig. 5b. Typical characteristics of thick-film transistor.

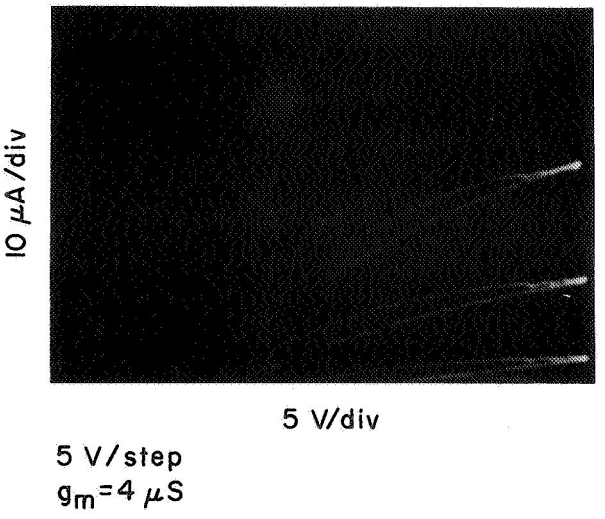


Fig. 5c. Typical characteristics of thick-film transistor.

Section III

PRECISION MASKING AND PRINTING

A. PRECISION MASKING

A precision mask changer was used for the fabrication of TFTs with thin film components. This changer is shown in Fig. 6. It is used in the following manner: (1) the substrate is mounted on a three-dimensional micropositioner, and (2) the mask is attached to a two-dimensional micropositioner. Both elements can be moved from outside the bell jar by means of vacuum-sealed rotary-motion feed-throughs. The substrate is in a vertical direction, and the mask is in a lateral, horizontal direction, thus allowing precise alignment of the channel with the gate electrode.

Figure 7 shows a typical TFT pattern. The masking elements for the source-drain channels were thin tungsten wires ranging from 0.1 to 1 mil in diameter.

B. PRECISION PRINTING

In order to achieve a pattern precision for screen-printed devices comparable to that achievable with vacuum-deposited films, it was necessary to find a new approach to precision thick-film printing.

A two-step process was implemented to replace the conventional one-step process. First, the principle of one-step deposition of the source-drain configuration by utilizing a channel-masking element, such as a thin wire, was abandoned. The two-step process first requires the printing, drying, and firing of one electrode. The aperture is then shifted laterally, and in a second printing step, the second electrode is deposited through this same aperture, so that the desired source-channel-drain configuration is achieved. This two-step method has a distinct advantage over the one-step process because the technician is free to print any channel width,

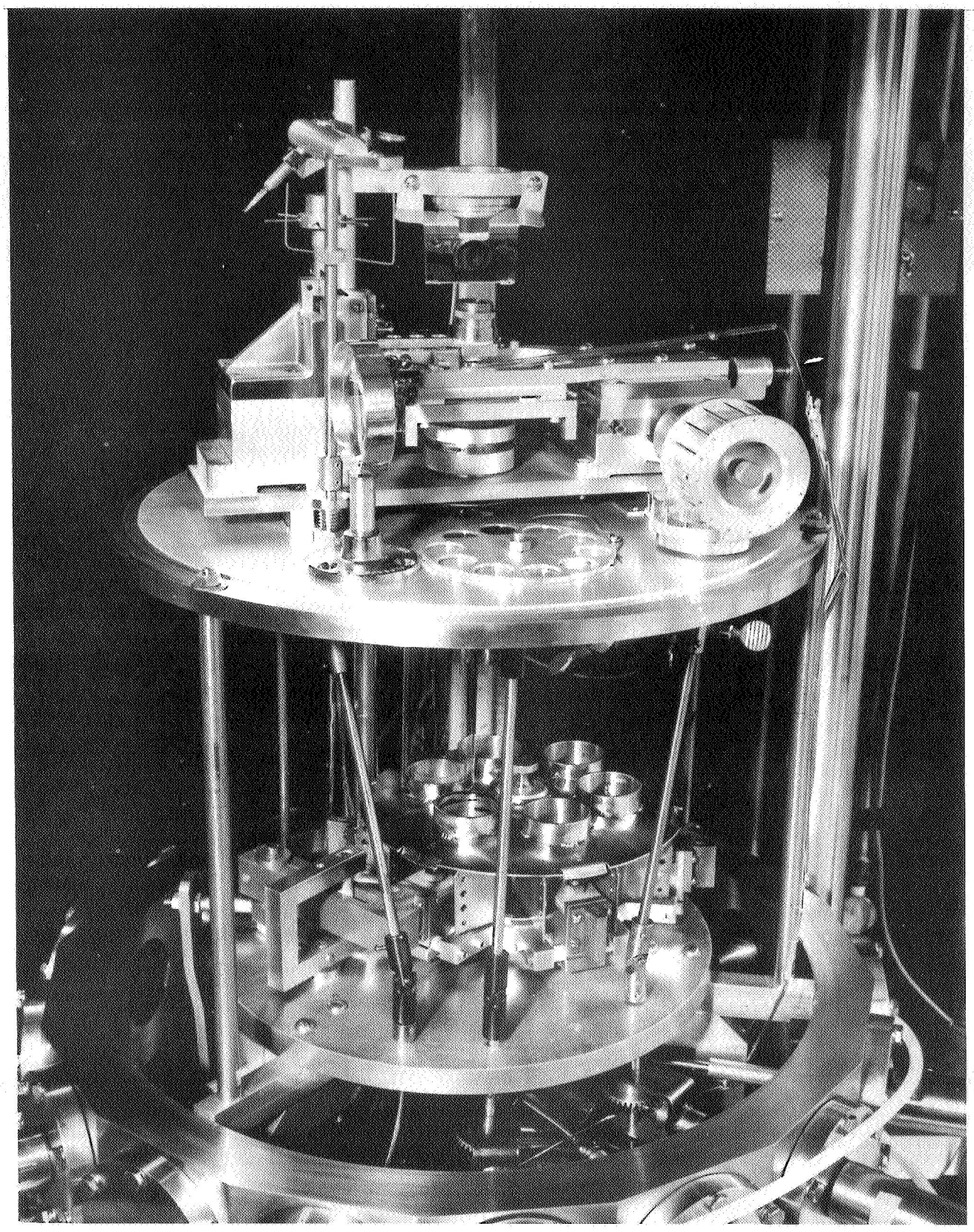


Fig. 6. Precision mask changer.

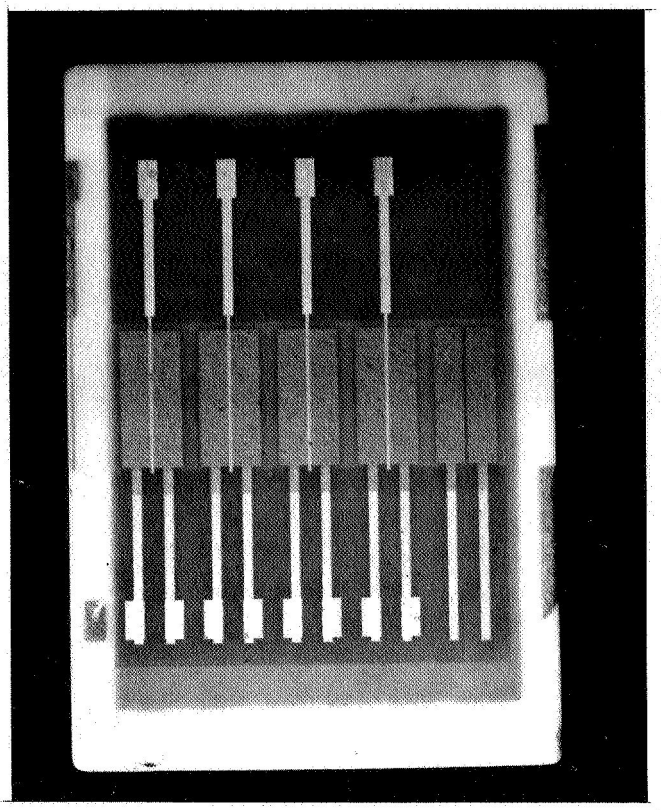


Fig. 7. TFTs with vacuum-deposited source, drain, and gate electrodes with SiO insulator on top of screen-printed CdS layer. (Approximate magnification: 5X)

regardless of ink flow, without having to provide a new mask for each channel dimension. This principle of consecutive source-drain deposition is, of course, applicable to vacuum deposition, and has been used in an effort to find a correlation between gap width and transconductance values of thin film TFTs.

The most critical step in this type process is the mask-substrate alignment for the second printing step. Since no commercial thick film printer available at this time provides accuracy sufficient for this purpose, a prototype precision printer with a simple optical alignment system was designed and used for the fabrication of all—thick-film TFTs in this program.

Figures 8 and 9 show this Precision Thick Film Printer. The printer is used in two basic positions. Figure 8 shows the printer set for alignment; Fig. 9 shows the printer set for printing. Figure 10 shows the optical system. Additional information on this printer is contained in the Appendix.

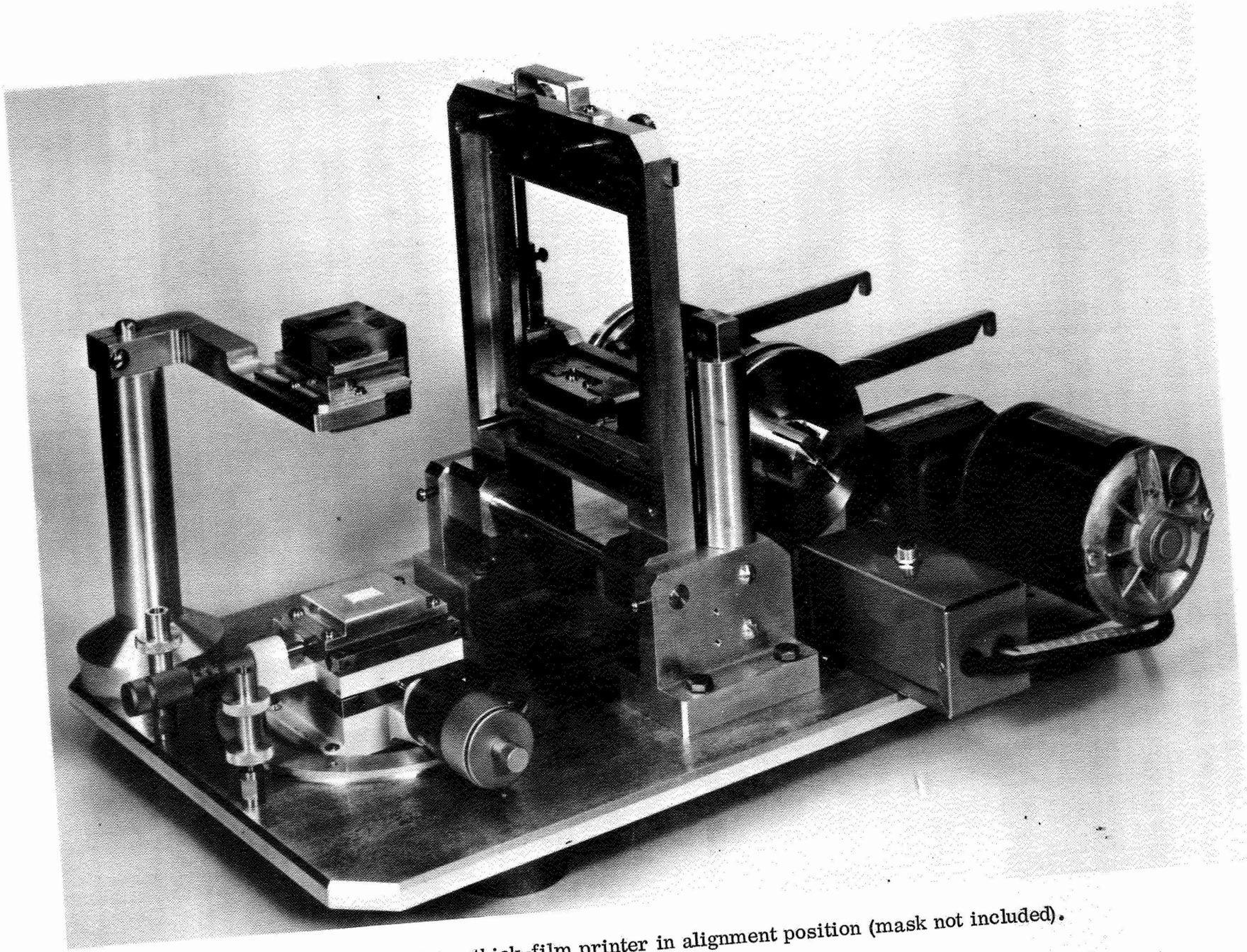


Fig. 8. Precision thick-film printer in alignment position (mask not included).

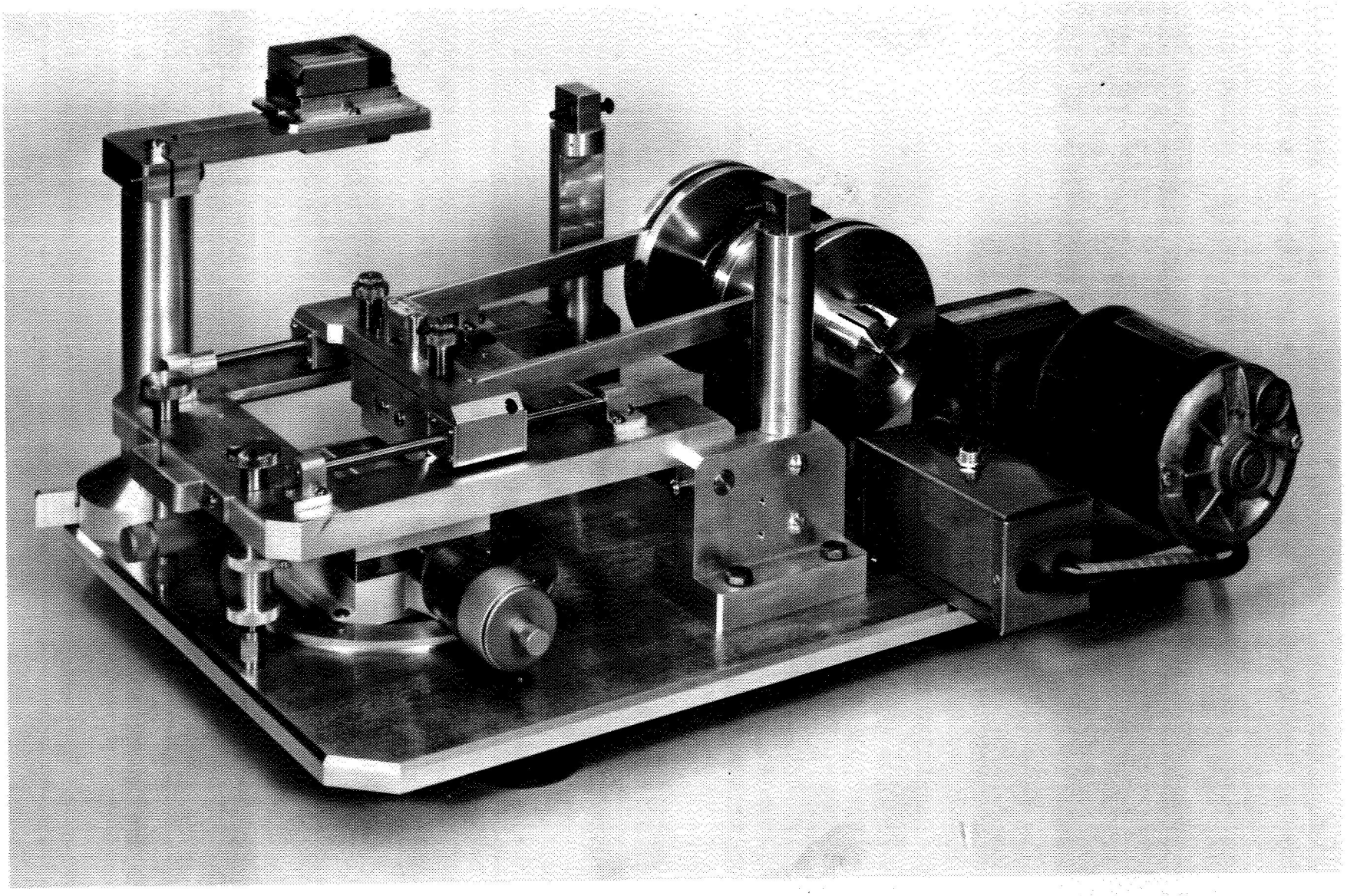


Fig. 9. Precision printer in printing position (mask not included).

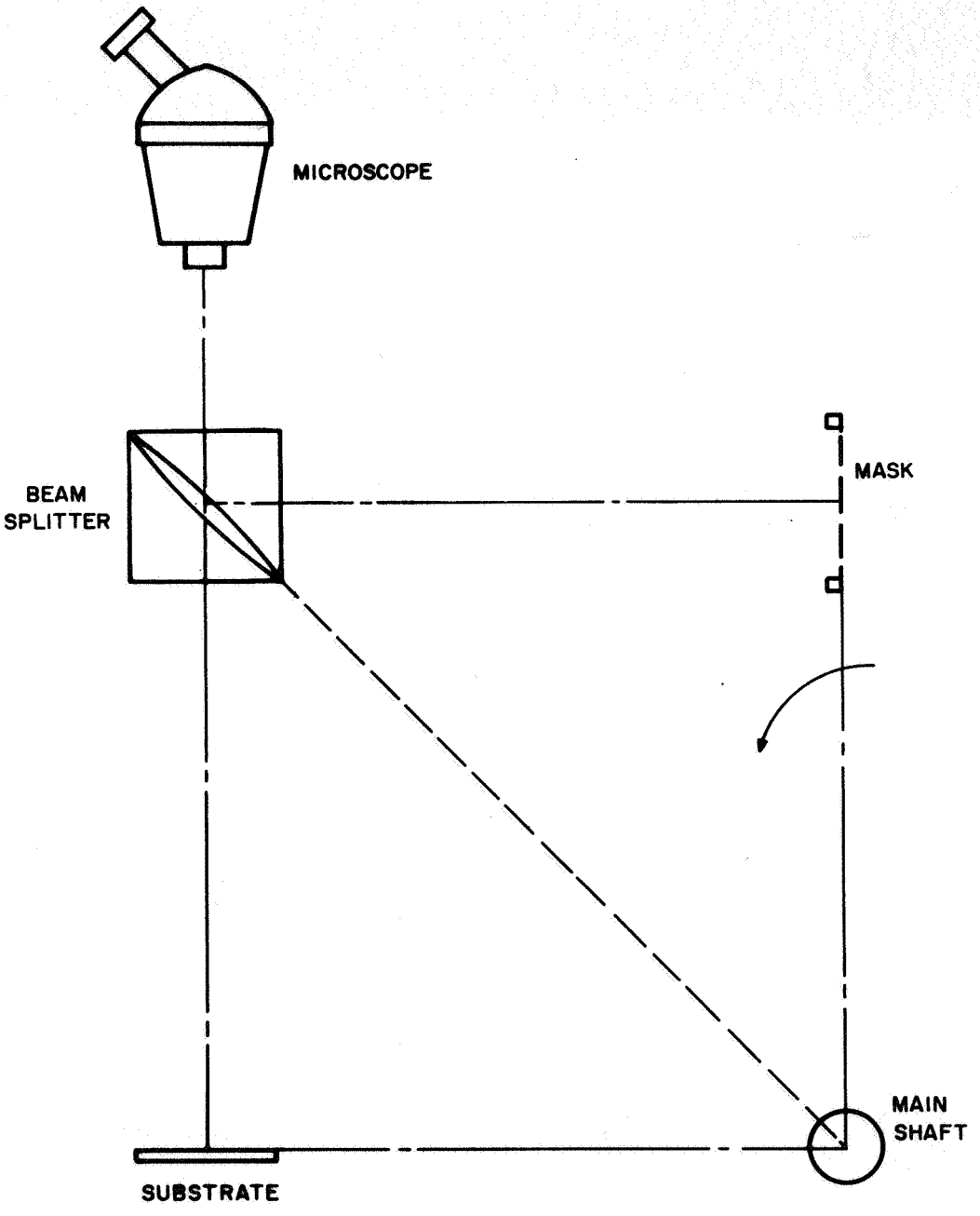


Fig. 10. Optical alignment of the Precision Printer (Side view).

The mask used with this printer consists basically of a molybdenum sheet 2 mils thick that is mounted on a frame 5 inches by 5 inches. The apertures are photoetched; the edges are defined by precision lines on the substrate side of the sheet; a mesh-type screen (also photoetched) is used to guide the squeegee edge on the top side of the molybdenum sheet (squeegee side). A cross-sectional schematic view is shown in Fig. 11. Although the photoetched mask is machined to extremely accurate tolerances, the precision of the printed pattern depends on various factors, such as ink viscosity, surface roughness, squeegee pressure, etc.

A procedure to evaluate the performance and usefulness of this printer was conducted by printing approximately sixty source-drain-gap patterns, similar to those shown in Fig. 12, and measuring the average channel width. The aim was a minimum gap width without electrically shorting the two gold layers.

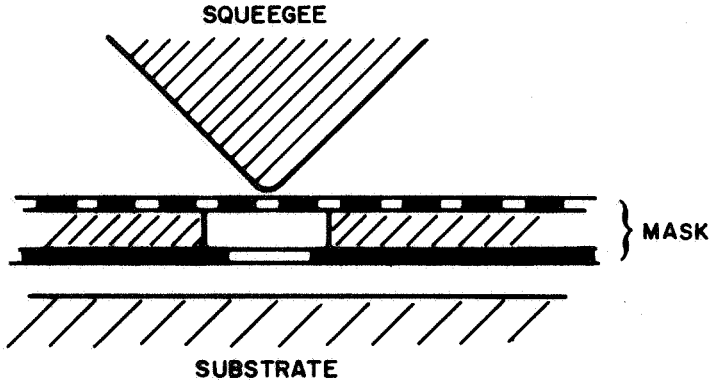


Fig. 11. Principal arrangement of squeegee, mask, and substrate. During the printing step, the mask is in contact with the substrate (not drawn to scale).

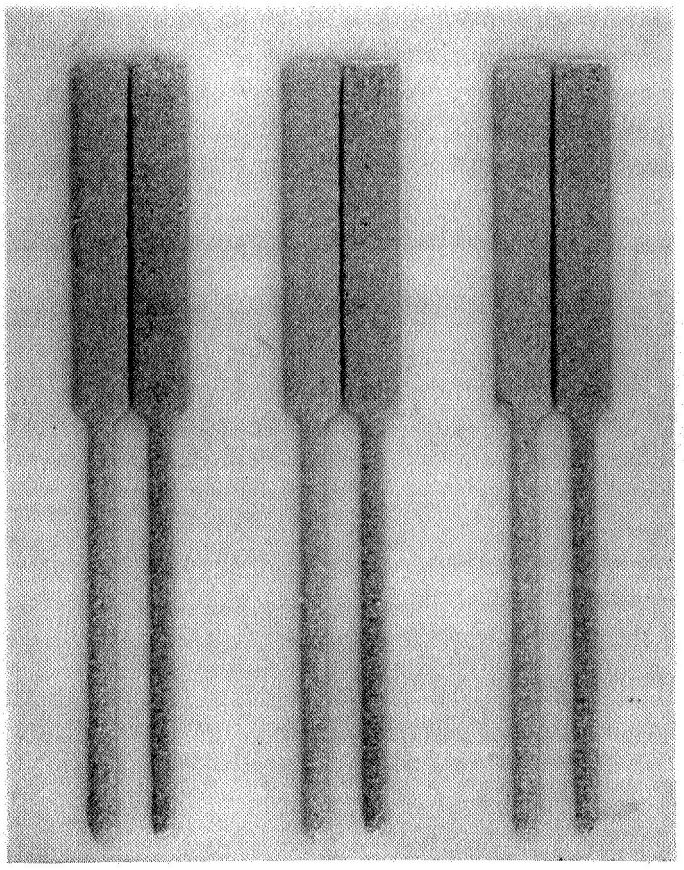


Fig. 12. Precision-printed gold layers forming source-drain gaps. (Approximate magnification: 9X)

As expected, a large number (about half of all patterns) were found to be shorted. The gap width distribution versus number of samples is shown in Fig. 13. A highly magnified picture of part of a gap is shown in Fig. 14.

From these data it can be concluded that the precision printer is a very useful tool for the fabrication of precision thick film patterns and that it provides accuracy of alignment. Optimized conditions, such as 1.) a smooth substrate surface; 2.) a thin wire mesh screen (instead of the relatively thick metal-sheet mask); and 3.) an ink with good viscosity are necessary to achieve the resolution possible with vacuum-deposited film patterns.

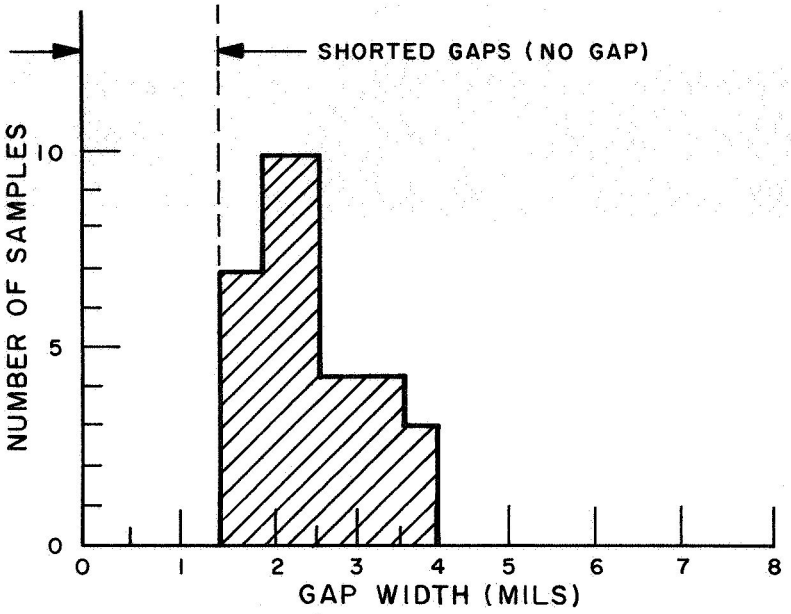


Fig. 13. Distribution of printed source-drain gap widths (approximately 50% of samples were shorted).

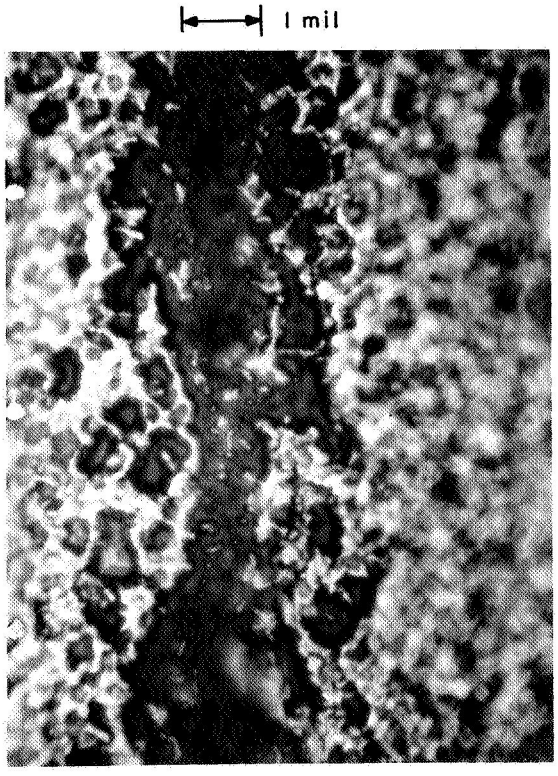


Fig. 14. Part of source-drain gap (400X).

Section IV

TFT COMPONENTS AND CIRCUIT

A. SUBSTRATE

Two types of ceramic substrates were used throughout this program. Each was basically of alumina from the American Lava Corporation.

The first type, measuring 725 mils by 500 mils by 40 mils, and designated AlSiMag 576 consisted of approximately 85% alumina. Its use gave good results and did not seem to have any detrimental effects on any of the film materials used, including the CdS. The surface roughness was measured with a Tallysurf instrument and found to be approximately 0.1 mil.

The second type, measuring 750 mils by 500 mils by 25 mils and designated AlSiMag 614, consisted of approximately 96% alumina. It was determined that the AlSiMag 614 contained impurities which contaminated the CdS films.

It was not possible to produce any working TFTs with these substrates.

B. CONTACTS

Aluminum was used exclusively as thin-film contacts on top of CdS layers, since the aluminum is known to give good ohmic contacts and since it provides the most stable and best insulating gate—dielectric-semiconductor combination. The thickness was monitored visually during the evaporation process to about 1000 Å (opaque film); it provided sufficient conductivity and stability. Gold films were not used as thin-film contacts, because gold is known to form blocking contacts on top of CdS layers, regardless of whether it is vapor-deposited or silk-screened.

Thick film contact layers can, of course, be applied only before the deposition of the CdS layer, because the required firing temperature for the metal layers would otherwise destroy the CdS semiconductor. Therefore, the gate electrode is deposited first, followed by the gate insulator and the source-drain electrodes. Experiments were made with thin-film gold electrodes instead of the silk-screened types. However, it was found that the corrosive vapor (mostly chlorine) released during the firing process for the CdS destroyed the thin films.

Efforts to apply thick vacuum-deposited films (more than 10,000 Å thick) encountered difficulties with regard to adherence, especially at higher temperatures.

Several types of inks were tried. These included DuPont gold paste No. 8115, DuPont gold-platinum paste No. 7553, DuPont gold-palladium paste No. 8083, and Engelhard gold-palladium paste No. 1132. DuPont gold paste No. 8115 gave the best results with regard to the uniformity of the insulator and semiconductor layer on top of it.

The printing process was performed with the precision printer and photoetched mask shown in Fig. 11. A bottom view of the apertures is shown in Fig. 15. The printing step was followed by a drying period of 30 minutes at 150°C in a drying oven. The firing cycle immediately after the drying step was carried out in a muffle oven at a temperature of approximately 1000°C. The resulting films were approximately 1 mil thick with a surface roughness in the same range as the ceramic substrate; i. e., about 0.1 mil.

In order to provide a smoother gate-insulator interface, several attempts were made to reduce this metal-layer surface roughness by etching it with aqua regia and polishing it with various materials. The most effective tool for this purpose was found to be a medium-hard pencil eraser of a motor-driven type (Bruning No. 87-100).

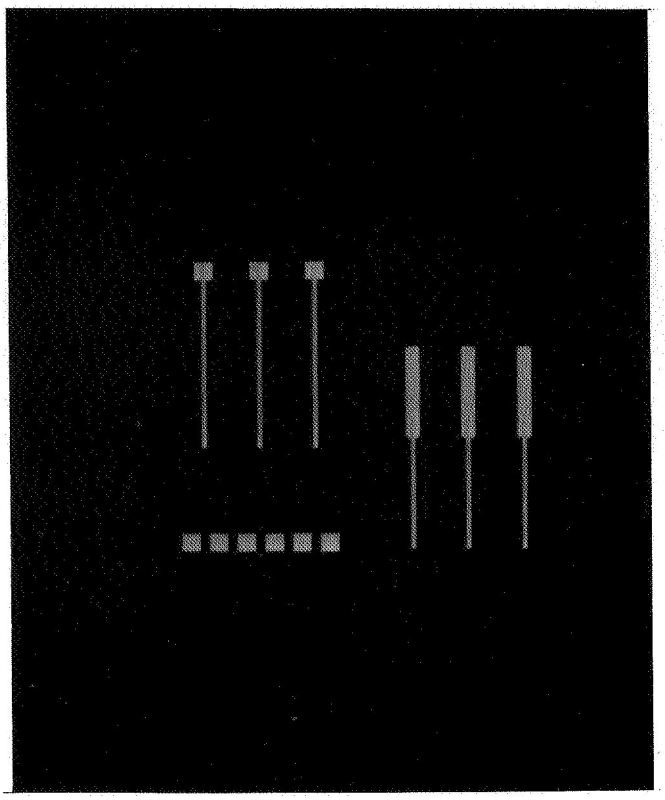


Fig. 15. Apertures on photoetched mask for printed TFT electrodes. (Approximate magnification: 2.4X)

The electrical contact properties of the Au-CdS interface were briefly investigated and found to present no major problem with regard to the function of the TFT. Although initially forming a blocking contact, the barrier breaks down irreversibly upon the application of a reverse voltage greater than one-half volt (see Fig. 16).

In order to eliminate any possible detrimental effects caused by the gold contacts, the intermediate structure (shown in Fig. 1e) was fabricated and tested. No measurable difference could be detected, whether the thick-film gold layers underneath the CdS layer or the thin-film aluminum contacts on top of the CdS layer were used as source and drain electrodes. This was confirmed by the fact that no measurable dark drain current could be detected at any gate bias up to 50 V.

Mass spectrometric analysis of the gold layer showed large amounts of impurity additives, mostly lead and silicon, which may play a significant role in the failure

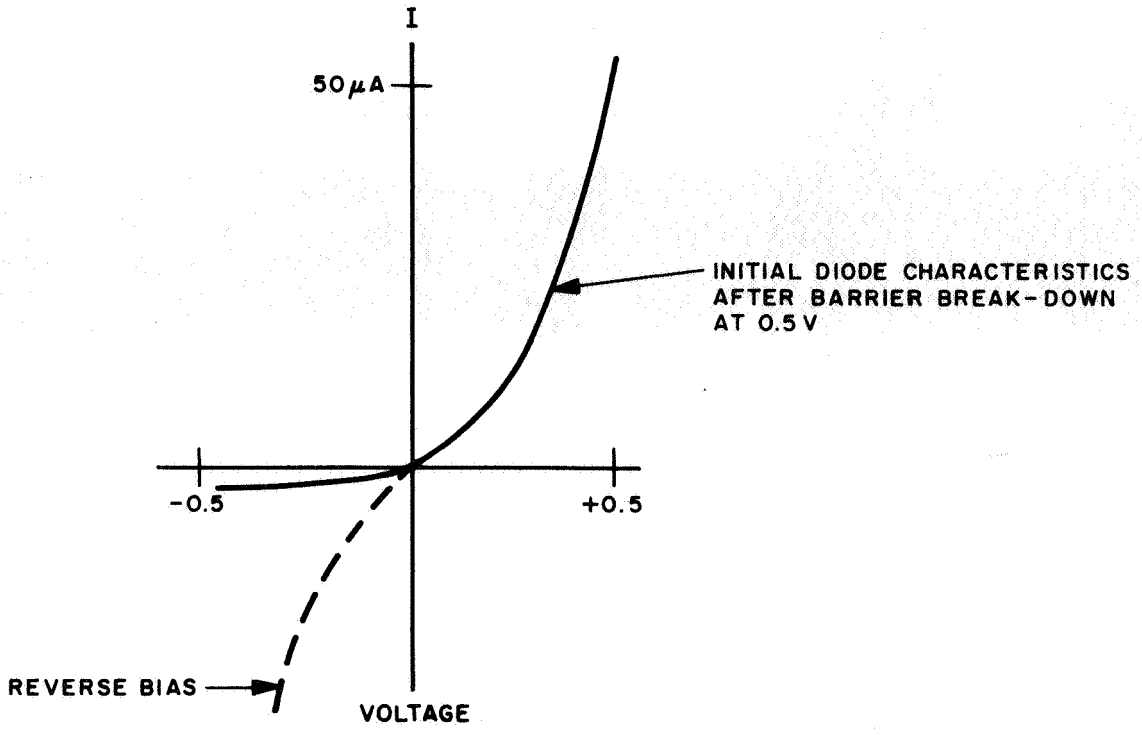


Fig. 16. Current-voltage characteristics of a printed Au-CdS contact.

mechanism of the final TFT. These contaminants are part of a lead-glass frit added purposely to the gold paste to achieve better adherence to the ceramic substrate.

C. DIELECTRIC GATE INSULATOR

The standard evaporation procedure for SiO high-vacuum deposition was employed for the formation of the gate insulator of thin film TFTs. The film thickness was monitored optically to three-quarter wave lengths of green light; i. e., 2250 Å thick. Pinhole-free layers were obtained. Gate voltages up to 20 V were insulated despite the considerable degree of surface roughness of the semiconductor. There seems to be, however, a correlation between atmospheric humidity and insulating characteristics of the SiO film. Very few cases of gate shorts were experienced during dry weather. However, it was practically impossible to obtain gate insulation during humid periods, especially during the summer, even when all thin-film

deposition steps were carried out in one pump-down cycle; i. e., without opening the bell jar immediately prior to or after the SiO evaporation.

With the dielectric constant around 6, an area capacitance of about 200 pF/mm^2 between gate and semiconductor was obtained. This permits a total gate capacity of 50 pF for a gate electrode measuring 140 mils by 3 mils.

An SiO film was applied under the CdS layer of an otherwise thick film TFT and tested. Samples of this nature failed because of the corrosive action of the chlorine vapor released during the CdS firing cycle. This process is similar to the thin-film metal-contact corrosion mentioned above.

In addition, experiments were carried out on SiO_2 deposited by the decomposition of silane: $SiH_4 + 2O_2 \longrightarrow SiO_2 + 2H_2O$. The structures fabricated using silane had shorted gates due to pinholes in the oxide.

Two materials were chosen for the preparation of the silk-screened dielectric insulator layer for the thick film TFT. These are DuPont inks No. 448-6950R and No. 448-8094R. Both materials were chemically analyzed and found to consist essentially of barium titanate. The dielectric constants were 400 and 800, respectively. Only the first type was actually used for this program, since it was available earlier. The ink was screen-printed with a commercial printer (Presco) through a 200-gauge wire-mesh screen, dried at 125°C for 15 minutes, and then fired in a muffle oven at 1000°C for 45 minutes.

Several test capacitors were prepared in the form of a gold-dielectric-gold configuration. The capacitances were found to be 100 pF/mm^2 for a dielectric film thickness of 1 mil. This is equivalent to a 4500-Å-thick SiO film. The loss factor was found to increase from 0.05 measured at a frequency of 1 kHz to 0.5 at 100 kHz.

Efforts were made to increase the gate capacitance by reducing the dielectric layer thickness. Butyl carbitol acetate was used to dilute the titanate ink, and a photoresist spinner was employed to thin out the layer in its wet state prior to drying

and firing. The thickness was finally decreased to about 0.1 mil; however, discontinuities and nonuniformities leading to poor dielectric strength were encountered. The surface roughness of the layers was also in the same range as the substrate roughness; i.e., about 0.1 mil.

D. SEMICONDUCTOR

The semiconductor material used exclusively during the entire program was screen-printed cadmium-sulfide developed previously for photo-cell fabrication at the RCA Mountaintop, Pa., facilities.

The semiconductor material is prepared as a viscous ink. In addition to the highly purified CdS, the ink contains cadmium chloride as a flux and copper chloride to provide acceptor levels in the final CdS thus reducing the dark current to a minimum. This type ink, as described by H. Bube,[2] provides an n-type photosensitive semiconductor on top of a ceramic substrate. Photo-cells fabricated with this material show a high photoconductive gain (several orders of magnitude) that indicates a relatively high electron mobility (up to 80 cm^2/Vs as well as a substantial carrier lifetime due to a low density of traps and recombination sites. The low density, especially of surface states that occur in combination with materials like SiO, makes the material extremely attractive for field effect devices, such as the thick film TFTs. Other advantages are the high dark resistivity (low I_{DO}) and the simplicity of fabrication. However, there are serious drawbacks, such as the inevitable surface roughness (in the micrometer range), and the corrosive action of vapors released during the sintering process (mainly chlorine dissociating from the chloride additives). This fact makes it mandatory that any thin films be applied only after the CdS is deposited.

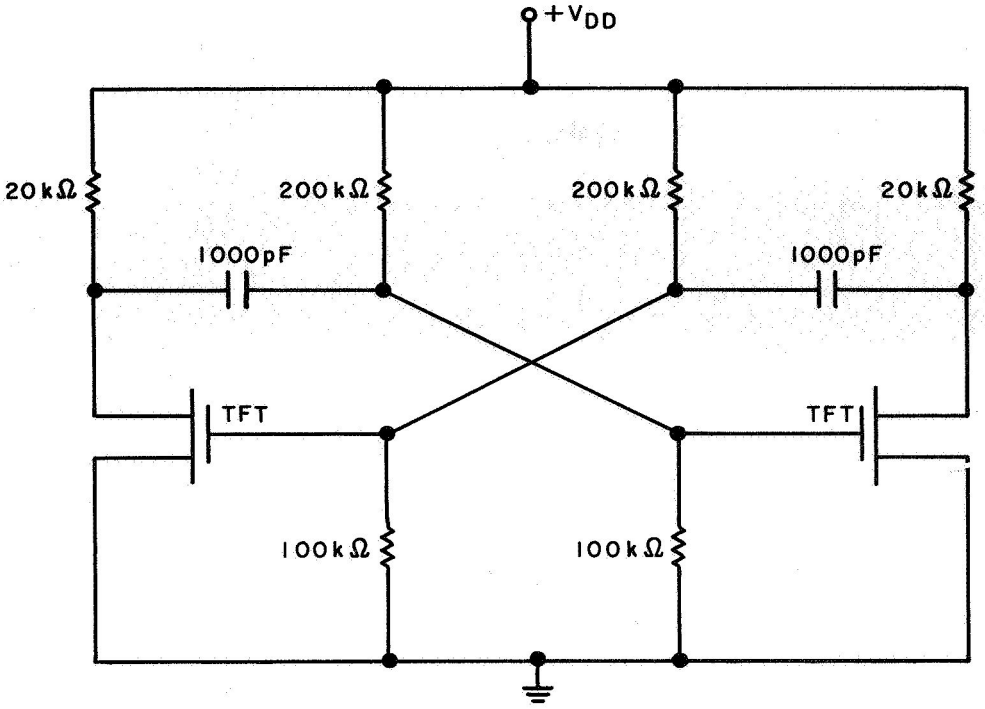
The CdS ink was printed with a commercial printer (Presco) through a 200-gauge stainless-steel wire-mesh screen and dried at 125°C for 15 minutes. The sintering step took place in a muffle oven at 600°C for 30 minutes in normal atmosphere. The thickness of the films obtained in this way was between 2 and 3 micrometers. The resistance varied with illumination, and was found to range from greater than 10^6 ohm-centimeters in the dark to approximately 10^3 ohm/centimeters at ambient light levels.

E. CIRCUIT

Although no working TFT models were achieved, a circuit incorporating two TFTs was designed.

A multivibrator circuit (shown in Fig. 17) was chosen as the vehicle which could simply demonstrate the utility of a TFT. The circuit contained two capacitors, six resistors, and two thick film transistors. The whole circuit consisted entirely of thick printed layers. This circuit is shown in Fig. 18.

The sequence of deposition was to first put down all passive components, and then the TFT semiconductor (the CdS layer), as the last element. By careful planning, the long delays usually associated with mask design and fabrication were avoided.



FREQUENCY RANGE IS APPROXIMATELY 25 kHz

Fig. 17. TFT multivibrator circuit.

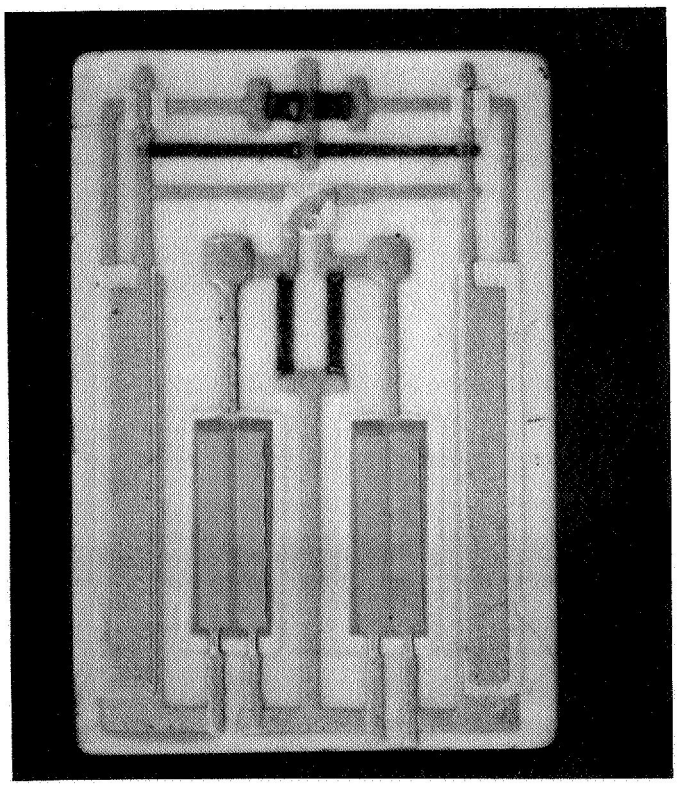


Fig. 18. All-thick-film multivibrator circuit (Approximate magnification: 5X).

Section V

ANALYSIS

The potential of CdS semiconductor as a basis for insulated-gate field-effect transistors has been proven by the fabrication and testing of active devices with screen-printed cadmium-sulfide layers and thin-film electrodes and insulators. The modification of these devices - i.e., the replacement of the thin film components with thick film layers - has not produced useful results thus far. A great deal of effort was devoted to the analysis of the thick-film transfer structure. Material interface problems that require further investigation have been detected.

There are a number of basic differences in the processing techniques as well as in the configurations of these two types of TFTs. The thin film devices utilize a CdS layer fabricated under well-proven and optimized conditions; all the subsequent fabrication steps are carried out at room temperature in an extremely clean vacuum environment. On the other hand, the CdS layer in the thick film devices is exposed to a variety of different materials, such as the impure gold layers and the barium-titanate dielectric layer during the sintering cycle. Analysis was made to determine diffusants, trapping sites, etc. The reaction of the various materials during processing was also explored.

Furthermore, it is important to realize that the active part of the semiconductor channel is only about 1000 Å deep (according to Waxman[3]), which means that the semiconductor insulator interface is more important than is the bulk of the semiconductor. In the thin film devices, this interface consists of the undisturbed CdS surface 100%-coated with the vacuum-deposited SiO film, regardless of the CdS surface roughness. In the thick film devices, however, the active area is near the

bottom surface of the CdS layer that is presumably in much poorer contact with the underlying and equally rough barium titanate layer underneath. In addition to these topological differences, it can also be assumed that the SiO film produces a significantly lower trap density, thus causing the formation of considerably fewer immobile charges in comparison with the $BaTiO_3$ layer. (How sensitive even the "undisturbed" CdS surface is with regard to the gaseous environment was shown by F. Micheletti[4] in a recent analysis.)

Several attempts were made by the RCA Laboratories to isolate and rectify the specific causes of failure. These are described in the following paragraphs.

A. MOBILITY MEASUREMENTS

The Laboratories tested a number of CdS layers fabricated under various conditions. Mobility measurements were conducted in an effort to determine whether a correlation exists between the electron mobility values and the fabrication procedures. The measurements were made according to a standard method: with the CdS brightly illuminated (to increase its conductivity) in a magnetic field of 3 kilogauss, Hall voltages were measured at both current directions and both field directions. Four basic structures were investigated:

(a) Plain CdS layer on a ceramic substrate;

(b) CdS layer on top of the $BaTiO_3$ layer;

(c) CdS layers co-sintered with wafers carrying Au layers; and

(d) CdS layers co-sintered with wafers carrying $BaTiO_3$ layers.

The procedure was the same for all measurements. The CdS layer (approximately 0.1 mil thick) and the other layers (approximately 1 mil thick) were deposited on a ceramic wafer measuring 725 mils by 500 mils by 40 mils (American Lava AlSiMag 576). Multiple contacts were made with liquid metals (Viking LS 232) based on a mercury-indium eutectic alloy.

Although previous tests of plain CdS layers made at the RCA photocell facilities in Mountaintop, Pa., showed mobility values up to 80 cm^2/Vs, measurements of samples prepared in Somerville (i.e., CdS ink obtained from Mountaintop but sintered in Somerville) showed electron mobilities between 40 and 50 cm^2/Vs. (Since the main point of this test series is to compare the mobility figures of the various samples (a) through (d), no effort was made to interpret the absolute value of mobility and its dependence on environmental conditions, such as illumination, atmosphere, etc.)

Samples (b) were prepared in the same way as samples (a) except that prior to the CdS deposition a 1-mil thick $BaTiO_3$ layer was printed, dried, and fired directly on the ceramic wafer. The CdS layer on top showed mobility values between 35 and 60 cm^2/Vs, a value not essentially different from that for the samples (a).

Samples (c) were prepared as were samples (a). However, during the firing of the CdS in the furnace a number of wafers carrying previously fired titanate layers (DuPont No. 448-6950 R) were also present in the furnace. This test was made in order to determine whether any gaseous interaction, caused possibly by the action of the extremely corrosive chlorine gas released from the CdS, takes place. The Hall electron mobility was found to be between 40 and 50 cm^2/Vs, again not different from that of samples (a) and (b).

Samples (d), co-sintered with wafers carrying gold layers (DuPont No. 8115), showed mobilities around 70 cm^2/Vs, quite contrary to expectations because of the large content of inpurities in the gold layers.

B. PHOTO-RESISTIVITY MEASUREMENTS

Although mobility measurements did not provide any clues to contamination effects, the degree of photo-sensitivity indicates some correlation between the mode of preparation and semiconductor property. Aluminum electrodes forming a 200 mils by 1 mil channel were vacuum-deposited onto CdS layers prepared under conditions as described above. When exposed to the light level of the ambient illumination in the laboratory, the following currents were measured at a channel voltage of 10 V:

Plain CdS on ceramic wafer	1000 μA
CdS on top of dielectric	700 μA
CdS on top of dielectric and gold gate	140 μA
CdS co-sintered with gold	80 μA
CdS co-sintered with dielectric	10 μA

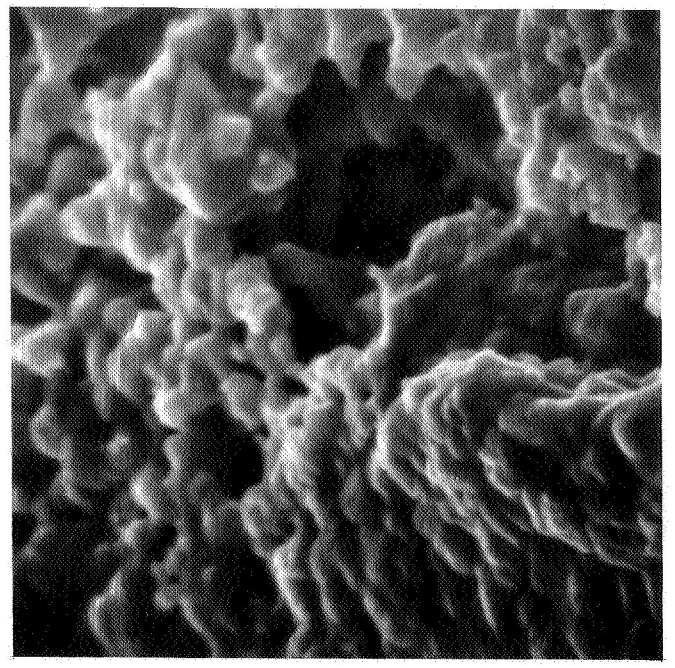
Although one cannot put too much weight on individual measurements since the CdS layers vary in their photosensitivity from one fabrication run to the next, it seems reasonable that the presence of "foreign" materials during the CdS sintering procedure is detrimental to the quality of the fabricated device. Further work in this area is important in order to gather more data which can lead to solutions to the materials interface problems.

C. ELECTRON MICROSCOPE PHOTOGRAPHS

A scanning electron-beam microscope was used to photograph the surfaces of the CdS layers prepared as outlined in Section IV. A. at a linear magnification of 5000X (see Fig. 19). As can be clearly seen, a marked difference in the surface texture exists between the surface of the CdS on top of the dielectric layer (Fig. 19b) or co-sintered with the dielectric layer (Fig. 19c) and the surface of the rest of the samples. It appears that part of the $BaTiO_3$ has diffused through the CdS layer, thus causing a substantially reduced surface roughness.

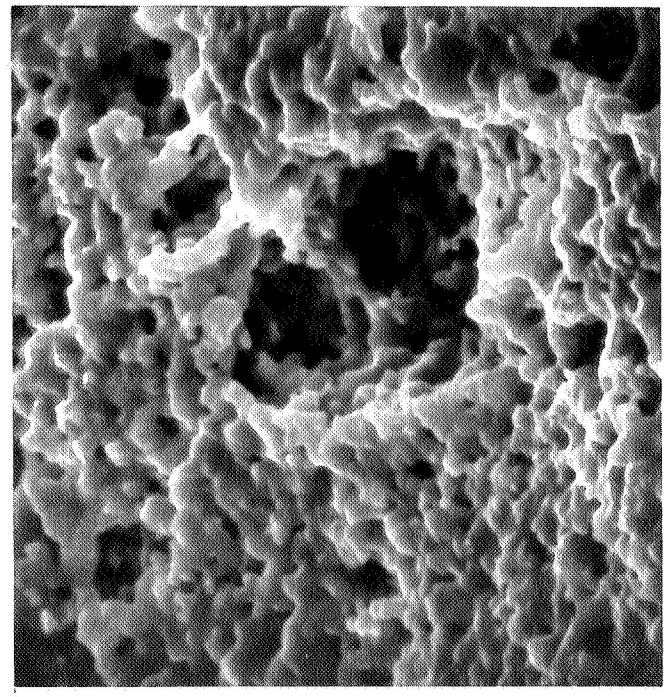
D. X-RAY DIFFRACTION

All samples described in Section IV. A, including a sample with CdS fired on top of a gold layer (DuPont No. 8115), were subjected to X-ray diffraction tests. This procedure probes the material near the surface within a few micrometers. None of the graphs obtained shows any correlation between mode of fabrication and diffraction pattern to conform with the evidence found in Section IV. C.



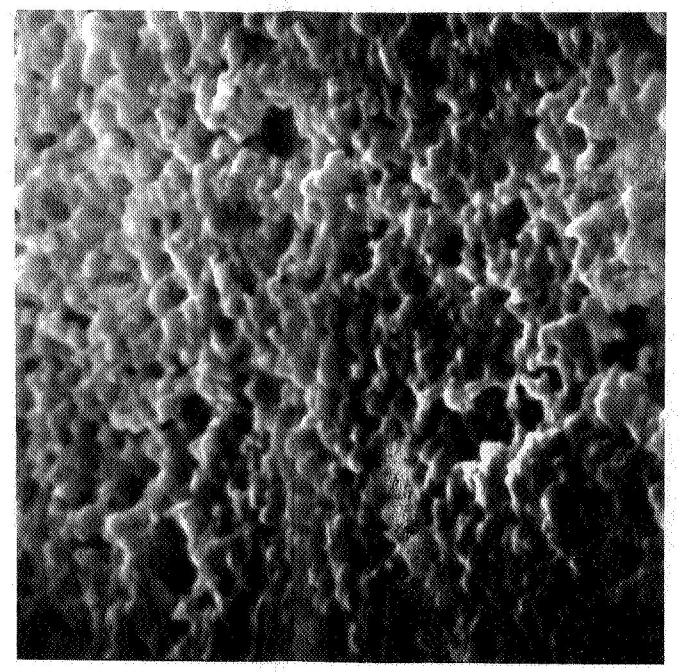
1 μm

a. Surface of printed CdS layer on top of ceramic substrate (5000X).



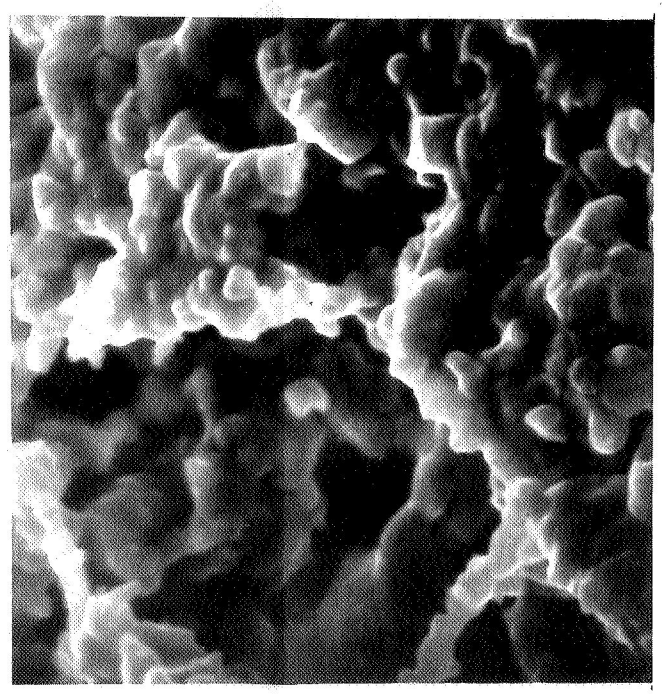
1 μm

c. Surface of printed CdS layer co-sintered with $BaTiO_3$ (5000X).



1 μm

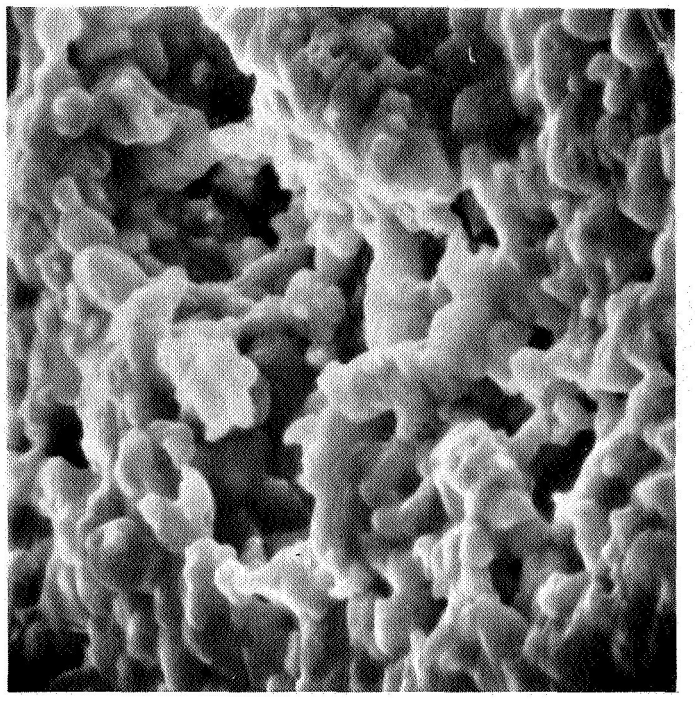
b. Surface of printed CdS layer on top of fired $BaTiO_3$ layer (5000X).



1 μm

d. Surface of printed CdS layer on top of a fired Au layer (5000X).

Fig. 19. Surfaces of TFT structures that were investigated.



e. Surface of printed CdS layer co-sintered with fired gold layers (5000X).

Fig. 19. Surfaces of TFT structures that were investigated.

E. MASS SPECTROSCOPIC ANALYSIS

The most accurate summary of ingredients and contaminants present in all the materials incorporated in the thick film transistor configuration was obtained by spark-emission spectroscopy. Five samples, as indicated in the table of Fig. 20, were investigated by utilizing a short pulse unidirectional discharge from high-purity-gold probes as a spark source. Of the five sample types listed, only the insulator on ceramic could not be sparked directly. A special method was used to obtain a qualitative identification of the constituents of this sample, but no numerical data can be supplied.

All values in the table shown in Fig. 20 are expressed in parts per million atomic (PPMA). It is estimated that the values reported are accurate to within a factor of three of the true value. Relative accuracy or precision is estimated to be ± 50% or better.

Element	Au on Ceramic		CdS on Ceramic		Au & Cds on Ceramic		CdS & Insulator on Ceramic		Insulator on Ceramic (Qualitative)
	PPMA*	Comments	PPMA	Comments	PPMA	Comments	PPMA	Comments	
As	95		10		30		3	NU	X
Br	7		7		ND		2		X
Sr	110		ND		15		ND		X
Pd	170		ND		15		ND		
Ag	275		5		30		6		
Cd	4300		Major		Major		Major		X
Sn	10		3		10		1		
Ba	2100		40		1300		450		X
Pt	3		ND		1		ND		
Au	Major		ND		Major		ND		
Pb	23,000		150		22,000		45		X
Bi	100		1		10		40		X
Sb									X
B	>2000		25		1700	NU	15		I
F	10		5		ND		5		
Na	1000		100		170		35		X
Mg	500		170		50		50		X
Al	2000		170		170	NU	55		X
Si	35,000		1100		1100		100		X
P	1500		15		15		55		X
S	90		Major		Major		Major		X
Cl	400		3300		4100		1300		X
K	500		25		90		5		X
Ca	1500		35		500		5		X
Ti	4500		45		450		150		X
V	35		ND		10		ND		
Cr	170		10		40		2		X
Mn	----	I	----	I	----	I	----	I	
Fe	2500	I-Partial	----	I	----	I	----	I	
Ni	ND		ND		120		ND		
Cu	120		110		160		35		X
Zn	130			I	----	I	----	I	
Ga	ND		10		40		ND		
Ge	260		ND		10		ND		

* PPMA = parts per million (atomic)

I - Cannot be determined due to spectral interference

NU - Non-uniform distribution of impurity

ND - Not detected. (In general, the detection limit for impurities in these samples was < 1 ppma.)

Fig. 20. Mass spectrographic analysis of thick film transistor samples.

It is obvious that the gold-ceramic combination contains considerably more impurities at higher concentrations than do the other samples. Some of the elements found are due, in whole or in part, to the ceramic substrate, but the gold deposit seems to be the major source of impurities. The most extensive additions there - lead and silicon - are due to a lead-glass frit as mentioned before. By comparing the data from samples (a) (plain CdS on the ceramic substrate) with data from samples with CdS plus insulator on ceramic, it can be seen that the insulating material (barium titanate) contributes relatively little to the impurities found. As would be expected, elemental concentration of the sample with the gold plus CdS on ceramic combination is in the majority intermediate between the samples where only Au or CdS is present.

F. CAPACITANCE-VOLTAGE MEASUREMENTS

All measurements so far dealt exclusively with material properties and characteristics throughout the thickness of the layers. They did not yield any specific information about the semiconductor-insulator interface. It is, however, this interface that determines to the largest extent the availability of mobile charges in the TFT channel. C-V measurements that are widely used in MOS technology (see Zaininger[5]) were therefore employed in an effort to determine why the TFTs fail to function.

Because it is known that a SiO film vacuum-deposited on top of the screen-printed CdS layer provides an interface which makes a semiconducting channel possible, a simple CdS-SiO structure with a vacuum-deposited aluminum contact on the CdS and a mercury probe on the SiO was investigated first. A typical C-V curve is shown in Fig. 21. The measurement was carried out under bright illumination in order to minimize the series resistance of the CdS layer. As can be seen, the curve represents the characteristics of a typical n-type semiconductor with a relatively sharp transition at the zero-bias axis. (It is assumed that the stoichiometrically excessive cadmium provides the donors in the form of interstitial impurities.) The sharpness of the capacitance change indicates the absence of a high density of trap levels at the interface; the fact that the step occurs at the zero-bias axis indicates that no positive ionic

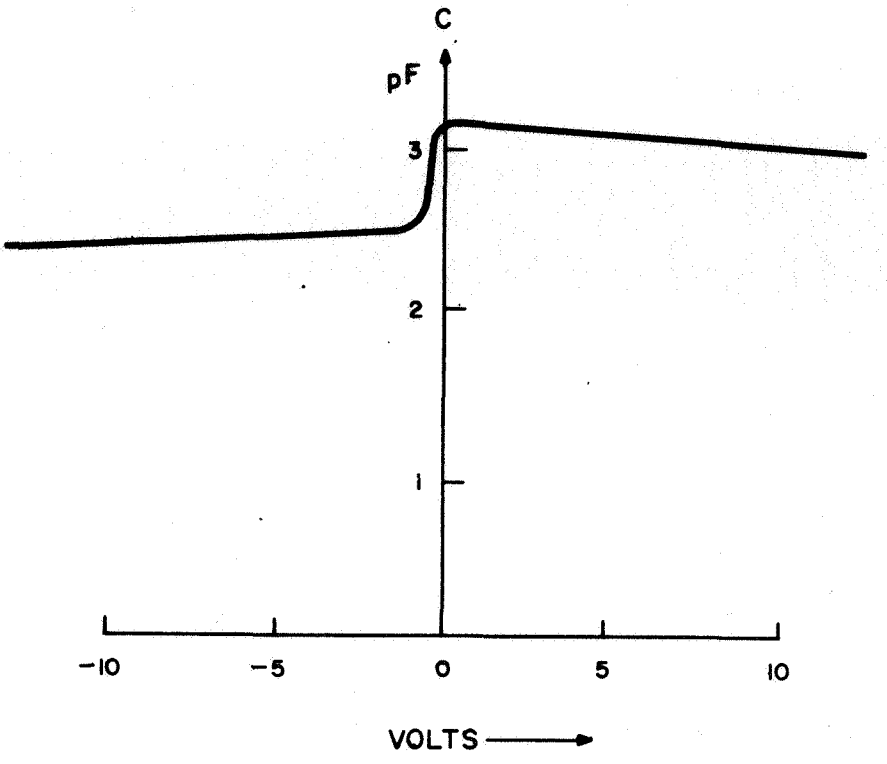


Fig. 21. C-V curve of a plain Cds-SiO interface showing n-type semiconductor characteristics.

charges are generated within the SiO film (Quantitative statements concerning dopant densities, etc. are difficult to derive because of the illumination-dependent series resistance of the CdS layer.)

Additional samples were tested, consisting, for example, of a Au-CdS-SiO configuration (see Fig. 22). This C-V curve shows a profound change, deviating completely from n-type characteristics. It is very difficult to interpret this type of curve which resembles a p-type materials characterization. The only conclusion that can be drawn is that the n-type semiconductor characteristics as observed with the CdS-SiO configuration have completely disappeared.

Further measurements of samples consisting of a barium-titanate layer, with or without an additional gold layer, do not show any capacitance change at all at bias

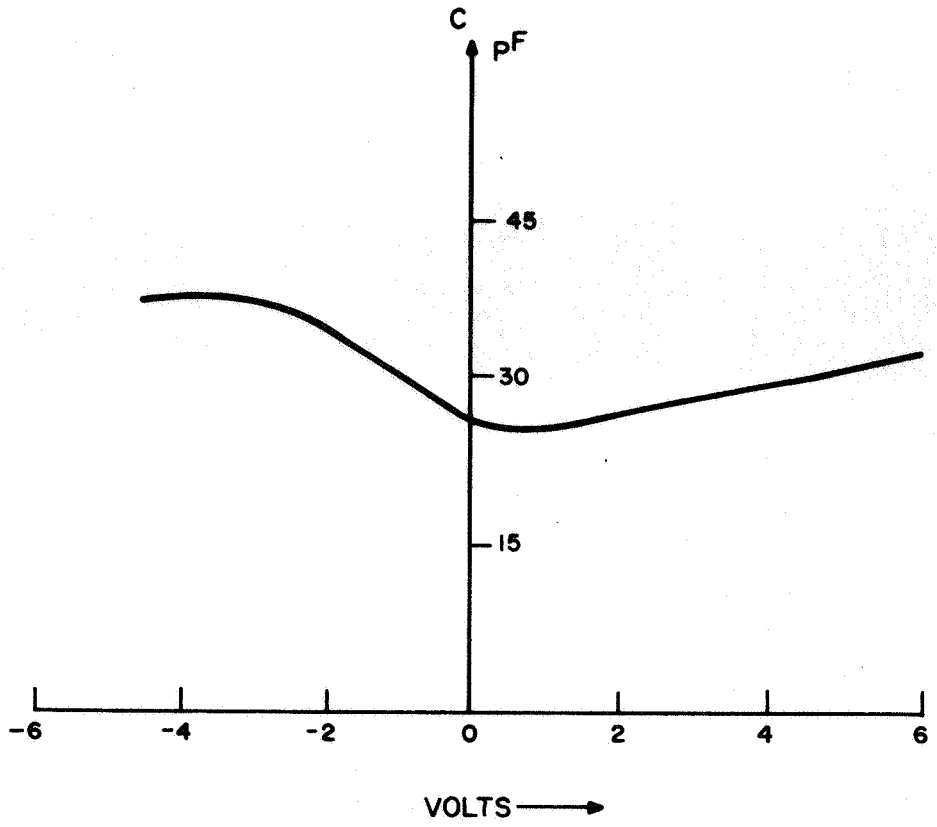


Fig. 22. C-V curve of a CdS-SiO interface on top of a printed Au layer.

voltages from +20 to -20 volts. Even the CdS-SiO interface with a titanate layer underneath the CdS layer does not show any sign of a mobile charge.

Efforts to improve the capacitance data by applying vacuum-deposited aluminum contacts, several square millimeters in size, on top of the insulators and semiconductors did not produce any better results because of large amounts of leakage current that were due to poor insulation characteristics of the SiO films. Structures of $BaTiO_3$ layers used as dielectric with aluminum contacts did not show any capacitance variation either.

In summary, no insulator-semiconductor combination gave any positive results regarding mobile charges other than the well-known CdS-SiO structure on top of a ceramic wafer without any other additional materials. This observation is believed to be a result of material contamination, surface roughness, and other material interface problems that are discussed in Section VI, Conclusions.

Section VI

CONCLUSIONS AND RECOMMENDATIONS

The potential of a randomly oriented screen-printed polycrystalline n-type cadmium-sulfide layer as a basis for insulated-gate field-effect devices has been established and has been realized by the fabrication of TFTs with vacuum-deposited source, drain, gate electrodes and gate insulator.

The attempt to fabricate analogous active devices consisting exclusively of screen-printed layers has not been successful to date. The reasons for the impossibility of generating a source-drain current at or near the semiconductor-insulator interface and subject to gate-field modulation can be summarized as follows:

1. The application of a fired barium-titanate layer as a gate insulator produces a semiconductor-insulator interface presumably with a high density of surface states as indicated by C-V curve tests. Since it is probable that the ferro-electric domains in the titanate with associated electric field intensities is equal to or higher than those produced by the gate voltage, it is unlikely that effective field modulation will be achieved even in the absence of other trap levels. In addition, the inherent surface roughness of both layers, CdS and $BaTiO_3$, which is higher by several orders of magnitude than the effective semiconducting channel depth, inhibits the formation of an adequate interface in a strictly topological sense.

2. As shown by the mass spectroscopic analysis, contamination from commercial inks used in this process is exceedingly high. Since a concentration of 1 ppma is equivalent to an impurity density of 4×10^{16} atoms per cm^3, one can easily see that only a very small part of these contaminants can generate enough trap levels to completely block the gate field with immobile charges. The application of high temperatures during the various firing and sintering steps aggravates this situation further, since diffusion constants increase considerably with temperature.

The precision printing technique developed during this program has proven quite successful. The printing apparatus constructed makes it possible to align and print miniature patterns with close to ± 1-mil accuracy. It is expected that even better accuracy can be achieved by utilizing thinner masks.

For further development work in the field of thick film active devices, it is therefore recommended that methods to eliminate the unfavorable conditions due to the roughness of the semiconductor-insulator interface be studied. These studies should include an evaluation of different materials and/or different modes of deposition. Further, an attempt should be made to minimize the contaminants by using only highly purified materials.

ACKNOWLEDGMENTS

The authors wish to thank all people whose cooperation made this work possible. We are particularly grateful to Mr. T. Koot, who carried out most of the laboratory work; to Messrs. E. Fisher and T. Howard and Miss F. Navitsky from the RCA Mountaintop, Pa., facility for their assistance with the semiconductor material; to Dr. G. Briggs, from RCA Lancaster, for valuable discussions; to Mr. F. Micheletti and Dr. A. Waxman, from the Laboratories, for assistance in mobility measurements; to Dr. R. Honig and Messrs. F. Shallcross, J. McCusker, and S. Perlman for important discussions; to Mr. M. Coutts for taking and interpreting electron microscope pictures; to Dr. W. Harrington for his mass spectroscopy analysis; to Dr. K. Zaininger for his interpretation of C-V curves; to Mr. A. Rapp for his cooperation with regard to the multivibrator circuit; to Messrs. R. Platt and J. Fabula, from the RCA Microelectronics group in Somerville, for their assistance in C-V measurements; and to Messrs. A. Danis and T. Matinho for their assistance with the screen printing equipment.

REFERENCES

1. "Applied Research in Thick Film Active Devices," Final Report No. 66266, Contract NAS 1-6285, December 1966.

2. H. Bube, Photoconductivity in Solids, J. Wiley & Sons, New York, 1960.

3. A. Waxman, Materials Analysis, April 1968.

4. F. Micheletti, "Ambient-Sensitive Photoelectronic Behavior of CdS Sintered Layers," RCA Internal Technical Report No. PTR-2421.

5. K. H. Zaininger, "Automatic Display of MIS Capacitance versus Bias Characteristics," RCA Review, September 1966.

APPENDIX

This Appendix contains the RCA Patent Disclosure Data Sheet for the Precision Thick-Film Printer.

PATENT DISCLOSURE DATA SHEET

To: Patent Operations
Radio Corporation of America
David Sarnoff Research Center
Princeton, New Jersey 08540

The herein described invention is submitted pursuant to my employment agreement.

(Date Received)	For Patent Operations Use Only (For Acknowledgment and Atty. Assignment)
	RCA Docket No.
	Date:
	Domestic Patents Mgr.
	Patent Attorney:
	Origin:

1. Date of this disclosure: January 2, 1968
2. DESCRIPTIVE TITLE: Precision Thick Film Printing Apparatus
3. PURPOSE, SUMMARY AND PROBABLE USES: This apparatus is a thick film printer equipped with a simple optical system in the form of a movable beam splitter for the precise alignment of mask and substrate. If used with a microscope, it is possible to print single and multiple thick film patterns with alignment tolerances less than .001 inches.

Answer All Questions – Use N/A when Not Applicable – **Submit Original — Keep Copy for Your Files**

4. Attached hereto is "Detailed Description" comprising Form Pat. 3010 (3) pages and the following papers, prints, samples, etc. _____
5. Invention described March 15, 1967, in Engineering Notebook No. N/A Pages N/A
6. Device constructed on November 24, 1967. 7. Shop Order # 944312
8. Tested on November 24, 1967. 9. Test Witnessed by T. Koot
   Bldg. Smvl. Flr. LL City and State Somerville, New Jersey RCA Tel. Ext. X2433
10. State any plans for use of the invention printing thick film transistors and precision thick film circuits
11. If this invention has been described in any publication or report, identify: N/A
12. Was invention *either* (a) conceived or (b) *first* actually reduced to practice in the course of or under Government Contract(s) or Subcontract(s)? (a) Yes x No ____ If "Yes," give date: January 15, 1967
    (b) Yes ____ No ____ If "Yes," give date: _____, 19____ (See explanation on reverse side)
13. If answer either to 12(a) or 12(b) is "Yes" list contract(s) or subcontract(s) numbers:
    (a) NAS1-7340 (b) _____
14. Is the invention embodied in any material either (a) furnished or (b) to be furnished under Government Contract(s) or Subcontract(s) ? (a) Yes ____ No x (b) Yes ____ No ____
15. If answer either to 14(a) or 14(b) is "Yes" list contract(s) or subcontract(s) numbers:
    (a) N/A (b) N/A
16. Security classification of the invention N/A
    (If any part of this disclosure is classified, the disclosure should be appropriately stamped and transmitted under security procedures.)
17. (1) Full Name Wilhelm (First) Hans (Middle) Laznovsky (Last) Citizen of USA
    Home Address 81 Bertrand Drive (Street) Princeton (City) Mercer (Zip Code / County) New Jersey (State)
    RCA Div. or Subsidiary ____ Bldg. No. ____ Flr. LL City & State Smvl., NJ RCA Tel. Ext. 3734
    Occupation No. 51973 Occupation Title Senior Project Member of Technical Staff
    (2) Full Name _____ (First / Middle / Last) Citizen of _____
    Home Address _____ (Street / City / Zip Code / County / State)
    RCA Div. or Subsidiary ____ Bldg. No. ____ Flr. ____ City & State ____ RCA Tel. Ext. ____
    Occupation No. ____ Occupation Title ____
    (TYPE or PRINT)
18. Sign full name(s) (1) Wilhelm Hans Laznovsky (2) _____

SPACE BELOW RESERVED FOR WITNESS

(An effort should be made to obtain the signature of the person to whom the inventor(s) first disclosed the invention)

19. The invention was first explained to me by the above identified inventor(s) on November 24, 1967, and is understood by me.
    Signature of Witness Tunis Koot Date of Signature Jan. 11, 1968, 19____
    Name of Witness (Type or print) Tunis Koot
    RCA Location: City & State _____ Bldg. ____ Flr. ____ Tel. Ext. ____

INVENTOR'S COPY DESTROY CARBON PAPER

PATENT DISCLOSURE DATA SHEET

RCA Docket No.

DESCRIPTIVE TITLE: Precision Thick Film Printing Apparatus

4. DETAILED DESCRIPTION: The trend of the thick film printing development towards the fabrication of more complex circuit patterns requiring a higher degree of mask-substrate alignment accuracy has generated the need for a precision thick film printing apparatus. Such a mechanism equipped with a simple optical system for mask-substrate alignment within ±.001" precision has been built and is being used for the fabrication of thick film structures.

This printer consists of four basic parts mounted on a rectangular base plate = the substrate carrier, the screen and squeegee carrier, the optical system and the drive mechanism.

1) Substrate Carrier

The principal part of this system is a two dimensional micropositioner MP (from Line Tool Co., Model I) with two micrometer drives for one inch travels in the x and y direction, respectively. The drums are divided in .001 and .0001 inch graduations. The micropositioner is mounted on an aluminum disk allowing angular adjustment with respect to the vertical axis. Attached to the top of the MP is a square aluminum plate carrying the ceramic substrate (usually in the range of .750 x .500 x .025 inches).

2) Screen and Squeegee Carrier

The screen mounted to a "True-plane screen frame" (Type #700 from IRI, nominal dimensions 5x5) is attached to a flip plate pivoting around the horizontal main shaft MS (see drawing). The screen is held and can be adjusted by eight fastening and spacing screws. The two basic flip plate positions - vertical for optical observation and horizontal for printing - are also defined by adjustment screws.

The squeegee assembly consists of two guide rods, a carriage with ball bushings, a spring loaded squeegee holder and a flip switch to lower the neoprene squeegee to the printing position. The carriage is linked to the drive wheel with two connector rods.

3) Optical System

The only optical element is the beam splitter held by a side arm which is attached to a vertical shaft on the left side of the printer. A handle at the bottom end of the shaft turns the shaft, arm and beam splitter into one of the two principal positions: 1) precisely in between the horizontal substrate plane and the vertical screen plane, so that these planes and the beam splitting plane intersect at equal angles (45°) at the axis of the horizontal main shaft MS. (Adjustment screws on the BS frame are provided to set the BS accurately.) With the screen in the vertical position and the BS correctly set one can observe the two respective images - substrate and mask - superimposed by looking into the BS from above with or without the aid of a microscope (B&L stereo zoom with the .5x lens attachment). This arrangement allows the precise

Wilhelm Hans Hannemann 1-11-68
Signature(s) of Inventor(s) Date

(For Patent Operations Use Only)

WITNESSED AND UNDERSTOOD BY

Louis Kost Jan. 11, 1968
Signature of Witness Date

INVENTOR'S COPY DESTROY CARBON PAPER

PATENT DISCLOSURE DATA SHEET

DESCRIPTIVE TITLE: Precision Thick Film Printing Apparatus

4. DETAILED DESCRIPTION: positioning of the substrate within ±.001" with respect to the mask prior to the printing process. After the BS is swung out of this alignment position to the side (position 2) than the screen plate can be flipped into the horizontal position ready for the printing step.

4) Drive Mechanism

In order to obtain reproducible squeegee speeds a motor drive was chosen consisting of a Boston Gear Ratio Motor (MW 109-25-AS 70 RRM), a pair of chain driven wheels coupled to the two connector rods pulling the squeegee carriage. The connector rods engage and disengage automatically with and from the driving wheels.

Signature(s) of Inventor(s) — Date: 1-11-68

WITNESSED AND UNDERSTOOD BY

Signature of Witness — Date: Jan. 11, 1968

INVENTOR'S COPY DESTROY CARBON PAPER

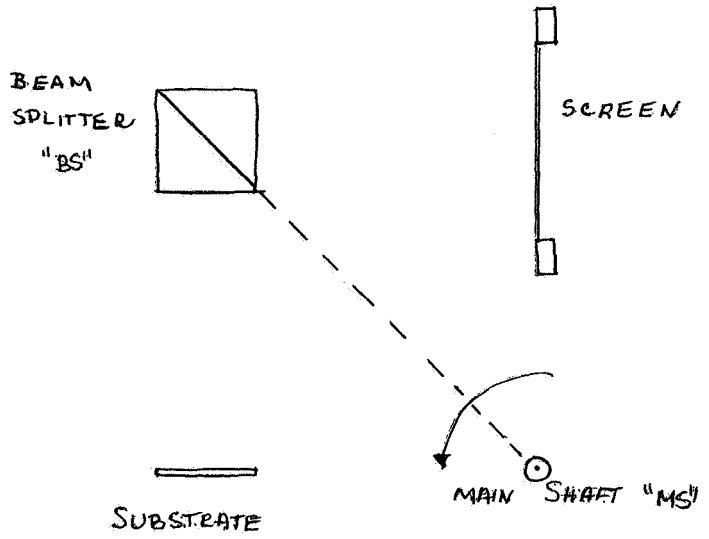
(For Patent Operations Use Only)

Form Pat. 3010 3-60

PATENT DISCLOSURE DATA SHEET

DESCRIPTIVE TITLE: Precision Thick Film Printing Apparatus

3. DETAILED DESCRIPTION: Side view of principal arrangement of screen, substrate, beam splitter and main shaft.



William Thos Hannaway
Inventor(s)

1-11-68
Date

(For Domestic Patents Use Only)

WITNESSED AND UNDERSTOOD BY

Janis Kost

Jan. 11, 1968
Date