A FLEXIBLE LSI SPACEBORNE DATA PROCESSING SYSTEM CONCEPT

R. J. Lesniewski

GODDARD SPACE FLIGHT CENTER
Greenbelt, Maryland

A FLEXIBLE LSI SPACEBORNE DATA PROCESSING SYSTEM CONCEPT

R. J. Lesniewski

INTRODUCTION

On-board computers are now successfully being flown for the first time in unmanned spacecraft, such as the Plasma Statistics[1] and the Autocorrelation computers aboard Explorer XXXIV. Although these machines are special purpose in nature, they herald the beginning of what might be termed the "spaceborne computer revolution."

At the outset of this revolution two schools of thought have emerged. One school favors the use of super redundant, "highly reliable," large central data processors to control and process an entire spacecraft. The opposing school favors the development of small yet flexible, low power, data processors where the ratio of processors to experiments in any given spacecraft is equal to or greater than 1. Large Scale Integration (LSI) utilizing complementary MOS technology is making the development of such small programmable processors possible.

There are two major advantages in using one or more small processors per experiment. One advantage is the ease of interfacing one experiment with its own processor, compared to the interfacing of many experiments with a central processor. Having his own processor permits the experimenter freedom to fly

on different missions without having to go through the difficulty of interfacing with each unique spacecraft processor, since only one experiment to processor interface need be done. While interfacing with telemetry cannot be avoided, nowhere does it compare with the problems of interfacing with a central processor.

Reliability is another advantage. With a collection of small processors, a failure does not jeopardize the entire mission of the spacecraft, since the processors are decentralized. Near and deep space missions of the past have survived failures of individual experiments, so too advanced missions of the future should survive failures of individual processors.

PARALLEL ULTRA LOW POWER PROCESSOR

PULPP (Parallel Ultra Low Power Processor) is a representative example of the school favoring small programmable decentralized processors. However, three factors set PULPP in a unique class from other data processing systems.

A. Four flexible, general purpose LSI arrays constitute the system's basic building blocks.

B. Each array is complete with its own encoded instruction set including all the required control.

C. Each array will be low power in nature with operating powers measured in the low milliwatts and standby powers measured below 5 microwatts.

The four LSI arrays can be described as:

A. a 288 bit scratch pad memory

B. a 16 stage parallel processor

C. a 288 bit read only memory

D. a 16 stage input-output memory buffer.

Highlights as to the nature of each of these arrays will be given, including an example of how they can be combined into a 6 chip PULPP system capable of programmed data formatting.

Scratch Pad Memory Array

Westinghouse Defense and Space Center has successfully developed a 288 bit complementary MOSFET scratch pad memory[2] for use in PULPP. This memory consists of 2600 active devices (98,000 devices per square inch). The scratch pad memory is a self contained system since the memory, address, and control circuits are integrated on the same 200 mil square array. Access time to or from the memory is 5 microseconds.

A block diagram (Figure 1) of the memory shows that only 20 leads are required. Access to and from the memory on the same 18 data lines makes possible the low lead count.

Parallel Processor Array

A program has been initiated to develop a 16 stage parallel processor (Figure 2). Development of this 1500 active device array will require the latest LSI technological advances in the areas of mask making and interconnection.

The parallel processor has an instruction repertoire of 26 unique operations, making it an extremely flexible device. Some of the major instructions include parallel load and output; right, left, and cyclic shift; and, substract, AND; OR;

EXCLUSIVE OR; clear to zero; set to one; count up; count down; and two's complement.

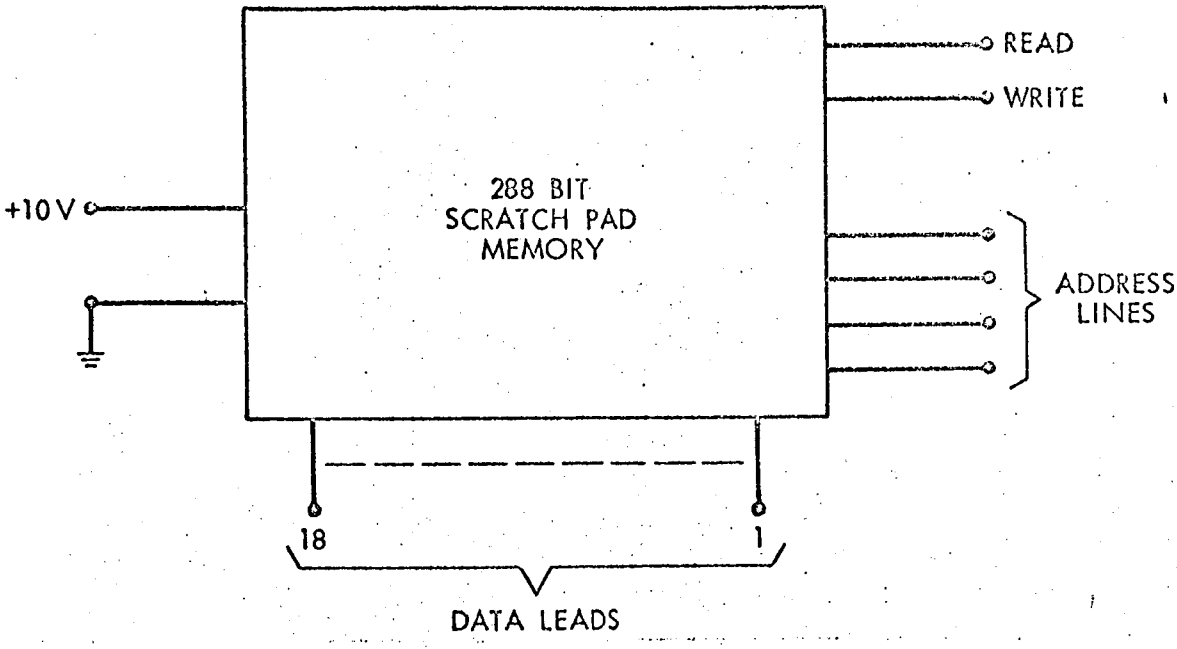

Figure 1.

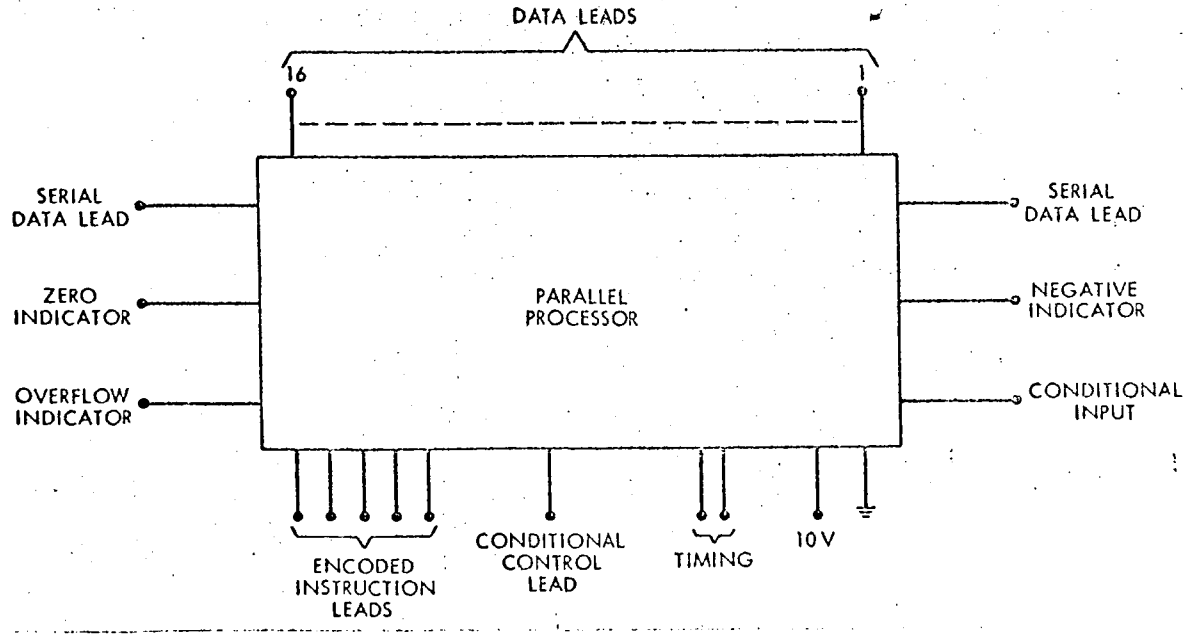

Figure 2.

An effort has been made to reduce the lead count both from an external interconnect and reliability point of view. For example, five leads are only required for the instruction set and sixteen leads for parallel access. The remaining leads are required for serial access, arithmetic indicators, timing, power and conditional operation.

Read Only Memory Array

A concurrent program has also been initiated to develop a monolithic 288 bit read only memory which can be programmed by the user after it has been packaged. Such memories are extremely useful for spacecraft applications since power is not required for memory retention. Again the memory will be self-contained with all the addressing and control circuitry integrated with the memory in the same array.

Buffer Array

The buffer register shown in Figure 3 is a 16 bit memory which has the following properties. Data may be loaded or unloaded from either side. Data may also be loaded from one side and outputed from the other with the option to store or not store the data. The 7 possible operations are controlled by 3 encoded instruction lines. The total lead count for this 16 stage buffer is 37 due to the accessibility from either side of the buffer. Since the buffer requires only 420 active elements, its development has been held up in preference to the parallel processor and read only memory, which are more powerful arrays.

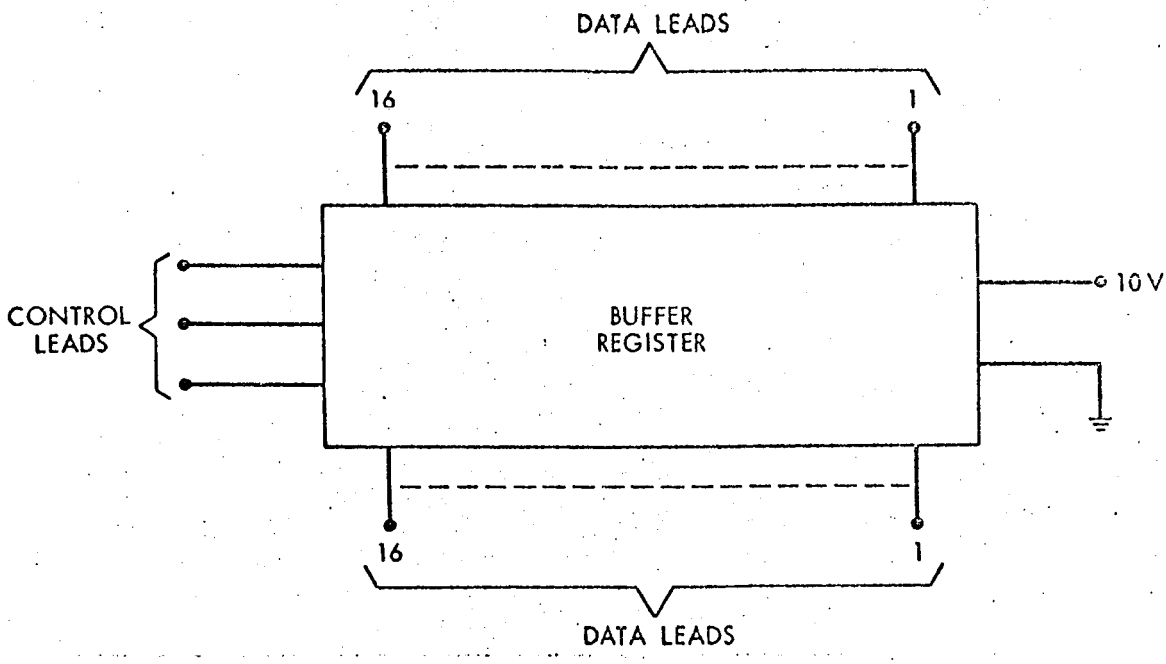

Figure 3.

6 CHIP PULPP SYSTEM

For purposes of illustration a minimum PULPP system will be described. The system (Figure 4) consists of only six LSI chips. Two memories are required. A read only memory is used for the program and a scratch pad memory is used for data storage. One buffer is required to establish programmed isolation between the PULPP system and the outside world. Three parallel processors are used as a program counter, a shift counter and a central processor unit.

This non-trivial configuration can, for example, be programmed to simultaneously sum and store 6 unsigned 12 bit numbers, logarithmic 'ly compress their sum into 4 bits of data and 4 bits of exponent, and output this result in the proper format to the telemetry link. The entire process requires 16 instructions

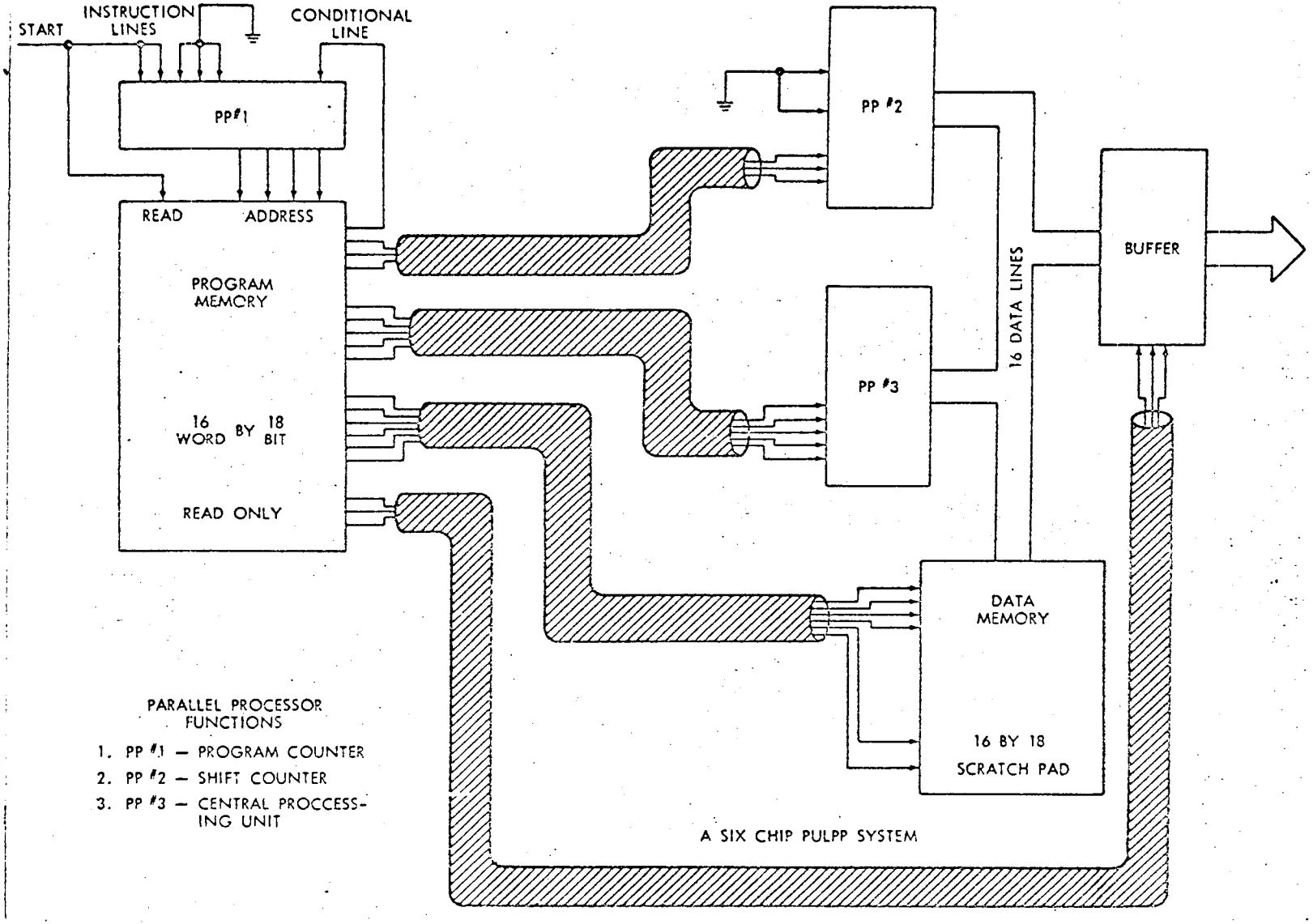
START
INSTRUCTION LINES
CONDITIONAL LINE
PP#1
READ
ADDRESS
PROGRAM MEMORY
16 WORD BY 18 BIT
READ ONLY
PP #2
PP #3
16 DATA LINES
BUFFER
DATA MEMORY
16 BY 18
SCRATCH PAD
PARALLEL PROCESSOR FUNCTIONS
1. PP #1 — PROGRAM COUNTER
2. PP #2 — SHIFT COUNTER
3. PP #3 — CENTRAL PROCCESSING UNIT
A SIX CHIP PULPP SYSTEM

Figure 4.

which are stored in the program memory. A new formatting sequence can be achieved by replacing the program memory with another containing a different program. Such a 6 chip system can be used as an interface between an experiment and telemetry. The standby power of this system is less than 20 microwatts. Operating with a 10 microsecond interpret-execute cycle a power dissipation of less than 30 milliwatts can be expected.

PULPP SYSTEM CONCEPT

PULPP can be thought of as a data processing system having the ability to both expand and reconfigure by using either hardwire or software. In less sophisticated applications where complex data reduction is not required, the PULPP system can be composed of only memory, parallel processing, and buffer arrays as previously described. In applications requiring priority interrupts and complex computations these same 3 arrays would be needed in larger numbers. In addition, four special purpose LSI arrays are needed to manage transfer and subroutine operations; monitor, acknowledge, and mask out interrupts; and test for arithmetic conditions. These four arrays constitute the nucleus of advanced PULPP system configurations around which memory and processing capability can expand as needed. This nucleus can manage random access memories expanded from 16 words of both program and data up to 4096 words of each. Up to 16 priority interrupt levels can be serviced.

Programs for theoretical PULPP systems have been written to do the tasks mentioned in reference 1 and 2 which include controlling the experiment,

extracting parameters from its raw data, and properly formatting these parameters for transmission over the telemetry link. Preliminary designs of such systems indicate that a PULPP system containing only 48 LSI arrays are required for those experiments. These 48 arrays consist of 33 read only memories, 5 parallel processors, 3 scratch pad memories, 3 buffers and 4 special purpose arrays. The standby power such a system would dissipate is less than 200 microwatts. Operating with a 10 microsecond interpret-execute cycle a power dissipation of around 250 milliwatts can be expected.

SUMMARY

Spaceborne data processing systems such as PULPP will have its initial impact upon the experimenter, since it will be possible for him to integrate a programmable, ultra-low power computer into his experiment package. Such a combination will enable him to easily meet the data format requirements of the spacecraft encoder, and the allotted bit output per experiment. Furthermore, should either the experiment or computer fail, the integrity of the spacecraft and its mission as a whole will not be jeopardized. These three functions will, therefore, offer the experimenter unprecedented opportunity to fly on many varied spacecraft without altering his computer except to change the program.

REFERENCES

1. Schaefer, D. H., and J. W. Snively, Jr., "The Plasma Statistics Computer Aboard Explorer XXXIV," Electronics and Aerospace Systems Technical Convention, October, 1967.

2. Cricchi, J. R., "Large Scale Complementary MOS Memory," Electronics and Aerospace Systems Technical Convention, October, 1967.

3. Lesniewski, R. J., "An L.S.I. Variable Function Register," Electronics and Aerospace Systems Technical Convention, October, 1967.

4. Beelitz, H. R., and H. S. Miller, "Partitioning for Large-Scale Integration," International Solid-State Circuits Conference, February, 1967.

5. Ahrons, R. W., and P. D. Gardner, "Complementary MOS Integrated Circuits," Proceedings of Integrated Circuits Seminar, Stevens Institute of Technology, Hoboken, New Jersey, February 1, 1967.