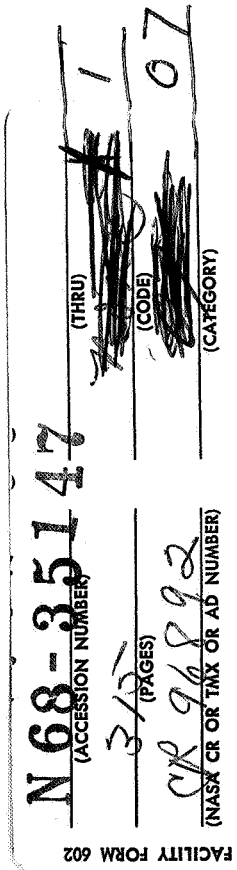
VOLUME 1 OF 2

SECTIONS I THROUGH VIII

FINAL REPORT

NIMBUS B PCM TELEMETRY SUBSYSTEM



15 AUGUST,1968
CONTRACT NO. 5—10139

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PREPARED BY

RADIATION INCORPORATED

SUBSIDIARY OF HARRIS-INTERTYPE CORPORATION

MELBOURNE, FLORIDA

FOR
GODDARD SPACE FLIGHT CENTER
GREENBELT, MARYLAND

2712

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ABSTRACT

This Final Report for Contract NAS 5-10139 describes the work done under this contract to supply PCM Telemetry Systems, Bench Test Equipment and Ground Stations for the Nimbus B Spacecraft.

The PCM Telemetry Subsystem, except for minor modifications and the ability to withstand environmental requirements, is identical in design to the electrical model system developed under Contract NAS 5-3787. The work under this contract (NAS 5-10139) included minor redesign, fabrication, assembly and environmental test of one prototype and two flight systems each consisting of:

1 Telemetry Electronics Unit (TME)
1 PCM Telemetry Unit (PCM)

The Bench Test Equipment developed under this contract utilized the Bench Test Equipment built under Contract NAS 5-902 which were completely modified except for commercial test equipment which was retained from the old systems. Three new Bench Test Equipments each housed in one rack, and two racks of test equipment resulted from modifying the greater number of racks used on NAS 5-902.

Four Ground Stations were modified extensively under this contract to include equipment to handle the substantially increased capability of the PCM Telemetry Subsystem. The fifth Ground Station was modified under Contract NAS 5-3787 along with construction of the electrical model PCM Telemetry Subsystem so that complete system performance could be checked. The Ground Stations modifications under this contract included added 5220 bit synchronizers, digital decom capability, time code display, modified simulator, and added event recorders plus the necessary cable and cabinet changes. These four stations were:

Station 1	Van Station Valley Forge New Station 8
Station 3	Classroom Valley Forge New Station 7
Station 4	Gelmore Creek Alaska New Station 4
Station 5	Goddard Space Center New Station 5

In addition to the above efforts instruction manuals were written covering all equipment.

Qualification Tests on the MOSFET device were run at General Instruments, the manufacturers, and at Radiation Incorporated to prove the reliability of the pyrolytic glass coated devices.

The prototype and two flight PCM Telemetry Subsystem, all Ground Stations and one Bench Test Equipment were delivered. Two Bench Test Equipments were retained at Radiation for integrator support. All delivered equipment went to General Electric, Valley Forge, Pennsylvania except for the Alaska and Goddard Space Center Ground Stations.

TABLE OF CONTENTS

Paragraph	Title	Page
	SECTION I. INTRODUCTION	
1.0	Introduction	1-1
1.1	Purpose	1-1
1.2	Scope	1-2
1.2.1	Spaceborne Equipment	1-2
1.2.2	Bench Test Equipment	1-2
1.2.3	Ground Stations	1-2
1.3	Nimbus B PCM Telemetry Subsystem General Description	1-4
1.3.1	General	1-4
1.3.2	Airborne Equipment	1-5
1.3.3	Bench Test Equipment	1-12
1.3.4	Ground Stations	1-12
	SECTION II. PCM TELEMETRY UNIT	
2.1	Introduction	2-1
2.2	Nimbus B Electrical Model General Description	2-1
2.2.1	Major Physical and Electrical Characteristics	2-4
2.2.2	Functional Block Diagram Discussion	2-29
2.3	Nimbus B Qualification and Flight Model Modifications and Component Differences	2-45
2.3.1	Electrical Design Considerations	2-45
2.3.2	Mechanical Packaging Design Considerations	2-64
2.3.3	Electrical Packaging	2-71
2.3.4	Component Difference Between the Qualification and Flight Model Systems	2-72
	SECTION III. TELEMETRY ELECTRONICS UNIT	
3.1	Introduction	3-1
3.2	Nimbus B Electrical Model General Description	3-1
3.2.1	Major Physical and Electrical Characteristics	3-5
3.2.2	Functional Block Diagram Discussion	3-11
3.3	Nimbus B Qualification and Flight Model Modifications	3-18
3.3.1	Electrical Design Considerations	3-18
3.3.2	Mechanical Packaging Design Considerations	3-22

TABLE OF CONTENTS (Continued)

Paragraph	Title	Page
	SECTION IV. BENCH TEST EQUIPMENT	
4.1	Introduction	4-1
4.2	BTE General Description	4-1
4.2.1	Major Characteristics	4-1
4.2.2	Summary of BTE Modifications	4-5
4.3	Functional Description	4-19
4.3.1	Modes of Operation	4-19
4.3.2	General Theory of Operation	4-21
4.3.3	Test Cables	4-26
	SECTION V. NIMBUS B PCM GROUND STATION MODIFICATIONS	
5.1	Introduction	5-1
5.2	PCM Ground Station Configurations and Equipment Allocations	5-1
5.2.1	Physical Descriptions	5-1
5.2.2	Functional Block Diagram Discussion	5-1
5.3	Nimbus B Ground Station Modifications	5-25
5.3.1	General	5-25
5.3.2	Physical Description of Modifications	5-26
5.3.3	Detailed Theory of Operation	5-28
	SECTION VI. RELIABILITY	
6.1	Introduction	6-1
6.2	Reliability	6-1
6.3	Subsystem Reliability Numerical Assessment	6-1
6.3.1	Reliability Mathematics	6-1
6.3.2	PCM Block Analysis	6-5
6.3.3	TME Block Analysis	6-8
6.3.4	Total System Reliability	6-12
6.3.5	Monitor Circuits	6-12
6.4	Failure Rate Considerations	6-13
6.5	Failure Rate Analysis	6-13
6.5.1	PCM Analysis	6-13
6.5.2	TME Analysis	6-13
6.6	Parts Selection and Vendor Evaluation	6-16
6.6.1	MOSFET, 5-Channel Multiplexer	6-16
6.6.2	Dual DTL NAND Gates	6-17
6.7	Malfunction History	6-18
6.7.1	Malfunction History Summary - Prototype System	6-18
6.7.2	Malfunction History Summary - Flight System 1	6-20
6.7.3	Malfunction History Summary - Flight System 2	6-23

TABLE OF CONTENTS (Continued)

Paragraph	Title	Page
	SECTION VII. PCM AND TME QUALIFICATION TESTING	
7.1	Introduction	7-1
7.1.1	Purpose	7-1
7.1.2	Philosophy of Environmental Test Program	7-1
7.1.3	Preparation for Test Program	7-1
7.1.4	Sequence of Testing	7-1
7.1.5	Test Condition Tolerances	7-2
7.1.6	Standard Conditions	7-2
7.1.7	History	7-2
7.2	Humidity	7-5
7.2.1	Purpose	7-5
7.2.2	Results	7-5
7.2.3	Test Equipment Required	7-5
7.2.4	Procedures	7-6
7.3	Vibration	7-6
7.3.1	Purpose	7-6
7.3.2	Results	7-6
7.3.3	Test Equipment Required	7-7
7.4	Acceleration	7-7
7.4.1	Purpose	7-7
7.4.2	Results	7-7
7.4.3	Test Equipment Required	7-7
7.4.4	Procedures	7-7
7.5	Thermal Cycling	7-7
7.5.1	Purpose	7-7
7.5.2	Results	7-8
7.5.3	Test Equipment Required	7-8
7.5.4	Procedures	7-8
7.6	Thermal Vacuum	7-8
7.6.1	Purpose	7-8
7.6.2	Results	7-9
7.6.3	Test Equipment Required	7-9
7.6.4	Procedures	7-9
	SECTION VIII. FLIGHT SYSTEMS 1 AND 2 PCM AND TME ACCEPTANCE TESTING	
8.1	Introduction	8-1
8.2	Flight System 2	8-1
8.2.1	PCM Unit	8-1
8.2.2	TME Unit	8-3
8.3	Flight System 1	8-5
8.3.1	PCM Unit Serial No. 0002	8-6

TABLE OF CONTENTS (Continued)

Paragraph	Title	Page
8.3.2	PCM Unit Phase I Test History 20-22 May 1967	8-6
8.3.3	PCM Unit Phase II History 26-27 May 1967	8-9
8.3.4	PCM Unit Phase III Test History 2-3 June 1967	8-10
8.3.5	PCM Unit Phase IV Test History 15 June 1967	8-12
8.3.6	PCM Unit (and TME Unit Serial No. 0003) Phase V Test History 28 January through 11 February 1968	8-13
8.3.7	TME Unit Serial No. 0003 Test History	8-13

VOLUME 2

Appendix I. Part Application Data Sheets

Appendix II. Failure Reports

Appendix III. Pyrolytic MOSFET Operational Life Test at Radiation

Appendix IV. Pyrolytic MOSFET Qualification Test at General Instruments

LIST OF ILLUSTRATIONS

Figure	Title	Page
1	Nimbus B PCM Telemetry Subsystem, Simplified Block Diagram	1-6
2	PCM Signal Flow, Simplified Block Diagram	1-7
3	Nimbus B PCM Telemetry Subsystem, Interface Wiring Diagram	1-9
4	PCM and TME Units	1-10
5	Bench Test Equipment	1-13
6	Nimbus B PCM Ground Station Cabinets	1-14
7	PCM Unit	2-2
8	PCM Unit, Functional Block Diagram	2-3
9	Housing Load Distribution	2-6
10	PCM Electronics, Housing, and Internal Structure	2-7
11	Maximum Response Within PCM Unit to Qualification Level Sine Vibration	2-9
12	Maximum Response Within PCM Unit to Qualification Level Random Vibration	2-10
13	Tool Card, Formed Foam Shim, and Card/Shim Assembly	2-11
14	Cordwood Welded Modules (Before and After Encapsulation)	2-13
15	PCM Unit Subassembly Reference Designators	2-14
16	Planar Mounted Multiplexer Card Assembly	2-16
17	Resistance Soldering of a Multiplexer Card Assembly	2-17
18	Bus Wire Interconnection Technique	2-20
19	Wired PCM Unit (Before Mechanical Assembly)	2-21
20	Nimbus PCM Telemetry Unit Functional/Packaging Block Diagram	2-23
21	Functional Assembly in Wiring Fixture and Location in PCM Unit	2-25
22	Prime Matrix Card Installed in System Test Fixture	2-26
23	System Test Fixtures	2-27
24	PCM Unit Detailed Block Diagram	2-30
25	PCM Output Word Diagrams	2-32
26	Programmer Interface Diagram	2-34
27	Programmer Simplified Logic Diagram	2-35
28	Multiplexer Simplified Block Diagram	2-37
29	Coder Simplified Block Diagram	2-40
30	Programmer Output Shift Register Split-Phase Converter, Simplified Block Diagram	2-42
31	Power Supply Simplified Block Diagram	2-44
32	RC Network Analysis	2-47
33	Coder Module No. 1 Schematic Diagram	2-49
34	Coder Module No. 2 Schematic Diagram	2-50
35	Coder Module No. 3 Schematic Diagram	2-53
36	Programmer Output Shift Register/Split-Phase Converter, Schematic Diagram	2-54
37	Programmer Module No. 1 Schematic Diagram	2-55
38	Shift Register and Programmer Problem Area Circuit	2-56
39	Equivalent Circuit	2-58
40	Coder 1 Filter Network	2-62

LIST OF ILLUSTRATIONS (Continued)

Figure	Title	Page
41	Telemetry Electronics Unit	3-2
42	TME Unit Simplified Block Diagram	3-3
43	TME Assembly - Spreadout Configuration	3-9
44	TME Unit Block Diagram	3-12
45	TME Unit Schematic Diagram	3-19
46	Bench Test Equipment Rear View	4-2
47	Bench Test Equipment, Subunit Designations and Locations	4-3
48	Countdown Time Code Simulator, 1A3G, Logic Diagram	4-7
49	Split-Phase Mark 0 Data Generator and Countdown Time Code Simulator, 1A3H, Logic Diagram	4-8
50	Countdown Time Code, Bit Synchronizer, and Data Error, 1A3B, Logic Diagram	4-9
51	Component Interface Board (Part of 1A6) Schematic Diagram	4-10
52	Time Code and Relays 1A6E, Logic Diagram	4-11
53	Bit Synchronizer, 1A6B, Logic Diagram	4-12
54	Sync Pattern Recognizer, Data Register, and Digital Comparator, 1A3E, Logic Diagram	4-13
55	Sync Pattern Recognizer, 1A3F, Logic Diagram	4-14
56	Word Counter Decode Gate, 1A3C, Logic Diagram	4-15
57	Frame Counters Buffers, Selected Word Decode and Bit Period Generator, 1A3D, Logic Diagram	4-16
58	Lamp Driver, 1A3A, Logic Diagram	4-17
59	Control Console, 1A5, Logic Diagram	4-18
60	Bench Test Equipment, Simplified Block Diagram	4-20
61	Bench Test Equipment, Signal Flow Diagram	4-22
62	Bench Test Equipment, Block Diagram	4-23
63	Time Code MO Format	4-24
64	Electrical Interconnect Box	4-27
65	Nimbus B Ground Station Configurations (Systems 4 and 5)	5-3
66	Nimbus B Ground Station Configurations (Systems 6 and 7)	5-4
67	Nimbus B Ground Station Configuration (System 8)	5-5
68	System Control Front Panel	5-6
69	Group Synchronizer Front Panel	5-7
70	Group Synchronizer Drawer Panel	5-8
71	Simulator Panels (Systems 4 and 5)	5-9
72	Simulator Panels (Systems 7 and 8)	5-10
73	Analog Decommutator Front Panel	5-11
74	Digital Decommutator Front Panel	5-12
75	Time Code Display Front Panel	5-13
76	Event Recorder (Front Panel)	5-14
77	Brush Recorder (Front Panel)	5-15
78	Computer Input Circuitry Front Panel	5-16

LIST OF ILLUSTRATIONS (Continued)

Figure	Title	Page
79	Bit Synchronizer (Signal Conditioner 5220-A) Front Panel	5-17
80	Power Supply (Mid-Eastern) Front Panel	5-18
81	Sola Power Supply Front Panel	5-19
82	Lambda Power Supplies Front Panels	5-20
83	DC and AC Circuit Breaker Panels	5-21
84	Telemetry Receiver Front Panel	5-22
85	Nimbus B Ground Station Functional Block Diagram	5-23
86	Group Synchronizer Block Diagram	5-30
87	Group Synchronizer Timing Diagram	5-31
88	Input Shift Register Logic Diagram	5-34
89	Frame Synchronizer Logic Diagram	5-35
90	Word Synchronizer Logic Diagram	5-37
91	Subframe ID Correlator Logic Diagram	5-38
92	Output Shift Register Logic Diagram	5-39
93	System Control Logic Diagram	5-41
94	Schematic and Assembly for Video Amplifier Card	5-43
95	Analog Decommutator (Systems 4, 6, 7, and 8) Logic Diagram	5-44
96	Analog Decommutator (System 5) Logic Diagram	5-45
97	Digital Decommutator (System 5) Logic Diagram	5-47
98	Digital Decommutator (System 4) Logic Diagram	5-51
99	Digital Decommutator (System 7 and 8) Logic Diagram	5-52
100	Time Code Display (Systems 4, 7 and 8) Logic Diagram	5-54
101	Time Code Display (System 5)	5-55
102	Simulator Functional Block Diagram	5-58
103	Simulator (System 4 and 5) Logic Diagram	5-59
104	Simulator (Systems 7 and 8) Logic Diagram	5-62
105	Time Code Generator Logic Diagram	5-65
106	Mission Time (Months)	6-2
107	Nimbus B Subsystem Reliability Diagram	6-6
108	TME Subsystem Reliability Diagram	6-9
109	TME Detailed Reliability Diagram	6-15

LIST OF TABLES

Table	Title	Page
1	PCM Mechanical and Packaging Characteristics	2-4
2	PCM Unit Card Assemblies and Reference Designators	2-12
3	PCM Unit Interconnection Scheme	2-22
4	PCM Electrical Characteristics	2-28
5	TME Physical Characteristics	3-6
6	TME Unit Card Assemblies and Reference Designations	3-8
7	TME Electrical Characteristics	3-10
8	Tape Recorders - Performance Characteristics	3-13
9	TME Input Power Lines	3-21
10	100 CPS Shielded Lines	3-22
11	BTE Signal Characteristics	4-4
12	BTE Commercial Power Supplies	4-5
13	PCM Ground Station Modifications	5-2
14	Subcommutation	5-48
15	TME Electronic Components and Relays	6-14
16	Failure Report Summary Nimbus B Prototype System	6-19
17	Failure Report Summary Nimbus B Flight System 1	6-21
18	Failure Report Summary Nimbus B Flight System 2 (Prior to Acceptance Level Tests)	6-24
19	Failure Report Summary Nimbus B Flight System 2 (After Start of Acceptance Level Tests)	6-24

SECTION I

INTRODUCTION

1.0 INTRODUCTION

This Final Report reports the effort accomplished during contract NAS 5-10139. Discussions and supporting data and illustrations are presented as follows:

a. Volume I Section I Introduction
Section II PCM Telemetry Unit
Section III Telemetry Electronic Unit
Section IV Bench Test Equipment
Section V Ground Stations
Section VI Reliability
Section VII Qualification Testing of the Space Equipment
Section VIII Acceptance Testing of Space Equipment

b. Volume II Appendix I Part Application Data Sheets
Appendix II Failure Reports
Appendix III Pyrolytic MOSFET Operational Life Test at Radiation
Appendix IV Pyrolytic MOSFET Qualification Test at General Instruments

Since the PCM Telemetry Units and Telemetry Electronics Units fabricated under this contract differ only slightly from the same units designed under contract NAS 5-3787, this report will be limited to discussions of differences rather than repeating data already available in the Addendum to the Final Report on contract NAS 5-3787.

In the case of the Bench Test Equipments, modifications were accomplished entirely under this contract and are discussed accordingly. Detailed operations and maintenance information can be found in the Bench Test Equipment Handbook prepared under this contract.

The Ground Station modifications were also accomplished entirely under this contract and therefore are covered entirely in this report. Detailed operation and maintenance can be found in the Ground Data Handbook prepared under this contract.

1.1 PURPOSE

This Final Report has been written in accordance with the requirements of contract NAS 5-10139 Statement of Work, Article III for the Goddard Space Flight Center, Greenbelt, Maryland.

The purpose of this report is to summarize and report on the work accomplished under this contract; to construct and deliver Spaceborn, Ground and Test Equipment for the PCM Telemetry Subsystem function in the Nimbus B Spacecraft.

1.2 SCOPE

The scope of work accomplished under Contract NAS 5-10139 was limited to the design, development, construction, test and delivery, along with instruction and maintenance manuals of flight qualified PCM Telemetry Subsystem, Bench Test Equipments, and Ground Station Modifications for the Nimbus B Satellite, and to work associated with the quality and reliability of these systems.

1.2.1 SPACEBORNE EQUIPMENT

A prototype and two flight model PCM Telemetry Subsystems were delievered under this contract each consisting of:

1 PCM Telemetry Unit
1 Telemetry Electronics Unit

These systems in addition to environmental qualification, differed from the electrical model system delivered under Contract NAS 5-3787 in the following respects.

a. Pyrolytic MOSFET devices were used in Flight Systems 1 and 2. The prototype used the non-pyrolytic devices.

b. The PCM Multiplexer MOSFET body bias circuit was changed to alleviate a noise problem.

c. Five minor changes were made in the PCM coder.

d. Several internal mechanical changes were made to the PCM unit involving wire potting, proper prototype and Flight model preloading and housing dimensions.

e. Significant wiring changes were made to the TME unit to improve overall reliability and to reduce noise and crosstalk that appeared on the TME output modulation signal to the transmitter.

The above items are discussed in detail in Sections II and III.

1.2.2 BENCH TEST EQUIPMENT

Some parts, racks and all commercial test equipment used in the Bench Test Equipment for Contract NAS 5-902 were used to construct three new Bench Test Equipment and two sets of test equipment to be used with the Nimbus B Telemetry Subsystem.

1.2.3 GROUND STATIONS

Four of the five Nimbus Ground Stations were modified under this contract to operate with the full capability of the Nimbus B PCM Telemetry Subsystem. To accomplish this these four stations were modified to include time code display, digital decommutation capability,

expanded simulator capability, event recorders, improved Bit Synchronization capability and other less significant specifications. The four stations modified were:

Station 1 Van Station
Station 3 Classroom - G.E.
Valley Forge, Pennsylvania
Station 4 Gelmore Creek, Alaska
Station 5 Goddard Space Center

1.3 NIMBUS B PCM TELEMETRY SUBSYSTEM GENERAL DESCRIPTION

1.3.1 GENERAL

The Nimbus B PCM Telemetry Subsystem is part of one of four satellites designed to gather meteorological data concerning the earth's atmosphere. The complete subsystem includes an airborne PCM telemetry subsystem, PCM ground stations, and Bench Test Equipment (BTE). The Nimbus B PCM Telemetry Subsystem was redesigned to include a digital measuring technique while retaining most of the original analog capabilities of its forerunners. As a result, the channel input capability of the PCM Telemetry Subsystem has been greatly increased. One time slot can now monitor up to seven digital inputs; whereas only one digital input was monitored per time slot in previous systems. In addition to adding the digital function, time code has been included as a telemetered parameter to provide an accurate time reference for every major data frame. Thus, when data is decommutated by the ground stations, accurate time references are provided for given measurements.

The airborne PCM unit accepts electrical inputs from various equipment in the Nimbus B spacecraft and formats these inputs into PCM code. Electrical inputs are both analog and digital. Analog inputs are converted to equivalent 10-bit digital words. Individual digital inputs are correlated into 7-bit words. The seven most significant bits of the converted analog words and digital words are time multiplexed, converted to split-phase, Mark 0 code, and routed to the TME unit.

The TME unit basically acts as a relay switching network and signal amplifier between the PCM unit and output transmitter and tape recorders. Upon command, the TME switches serial split-phase Mark 0 data from the PCM unit to the tape recorders for temporary storage, or to the transmitters for real-time data transmission, or both simultaneously.

The Nimbus B PCM Ground Stations receive and process telemetered data including time-code data from the Nimbus B Satellite System. Data is processed in real time or stored for later playback and processing. The maximum interrogation period for a single pass of the Nimbus B satellite is approximately 15 minutes. Stored-data playback time (one orbit) is approximately 3.6 minutes. Therefore, two-orbit recording is provided to collect data during those orbits when interrogation by the ground station is not possible. Unpon interrogation, the serial data input signal is processed in the system to obtain data synchronization and timing to drive system output devices. Channel output selection is made through the use of a decommutator program patch panel. Decommutator outputs are available to a peripheral computer for data processing according to the computer program. Two magnetic tape recorders, provided as part of the computer system, enable partially processed data to be stored for later processing. Other recording devices include oscillographs capable of plotting 32 channels of analog data, an event recorder capable of displaying 52 channels of digital on-off data, and magnetic tape recorders that accept and store the input video data for later processing. The digital decommutator and time code display processes the digital data recorded in certain words of the Nimbus B format and drives the system digital recorders and NIXIE time display.

Bench Test Equipment (BTE) is a special purpose test set that provides the necessary control signals, commands, and timing to the PCM Telemetry Subsystem. The BTE supplies the

signals to the PCM normally supplied by the Nimbus C clock in addition to other signals provided by other system components, when testing either a PCM or TME unit separately. The BTE generates split-phase mark 0 data that is applied to the PCM Telemetry Subsystem, and accepts the data from the PCM for comparison with preselected analog and digital channel data.

1.3.2 AIRBORNE EQUIPMENT

The airborne portion of Nimbus B PCM Telemetry Subsystem consists of five modules: a PCM Telemetry Unit (PCM), a Telemetry Electronics Unit (TME), two tape recorder modules, and one module containing two transmitters. The tape recorder and transmitter modules are government furnished equipment (GFE). Subsystem interface of these modules is shown as a simplified block diagram in figure 1.

Nine input circuits interface the PCM Unit with Nimbus "C" clock and Nimbus B digital and analog transducers. Of these nine inputs, four carry the Nimbus C clock frequencies of 500 cps, 100 cps, 10 cps, and 1 cps from the Nimbus clock. In addition, the Nimbus clock provides the time code (MO) input to the PCM Unit. All five inputs are routed through the TME to the PCM Unit to simplify interface wiring.

The four remaining inputs comprise the combined analog and digital channel gates from the source transducers to the PCM Unit. Analog inputs consist of 21 prime channels operating at the frequency of 1 sample per second, and 434 subcommutated channels that operate at a frequency of 1 sample per 16 seconds. Analog samples are then applied to an analog multiplexer and coder in the PCM Unit for coding into 7-bit data words.

Digital transducer inputs are routed through 63 prime digital channels that operate a a frequency of 1 sample per second and 280 subcommutated digital channels that operate at the frequency of 1 sample per 16 seconds.

All subsystem timing is controlled by a programmer contained in the PCM Unit which, in turn, receives timing from the Nimbus clock. The measurands, analog and digital, are applied through their respective multiplexers into sequence gates. PCM Unit signal flow is illustrated in the simplified block diagram shown in figure 2. As shown in the illustration, analog samples are converted to equivalent digital words before the final sequencer gates. After analog signals are coded, all digital and analog signals are handled in the same manner.

The final sequencer gates accept sync information, inject it into the word at the proper place, and output the word through an amplification stage to the output register. Here the word is converted to split-phase code and applied to the TME.

The 6-volt clamp circuit controls the operation of analog and digital channel gates. When one of the nonredundant PCM drivers is in use, a 6-volt output line from the driver in use energizes a clamping circuit in the other driver, thus clamping the outputs of the second PCM driver to ground. When the second driver is in use it, in turn, clamps the output of the first driver in a similar manner.

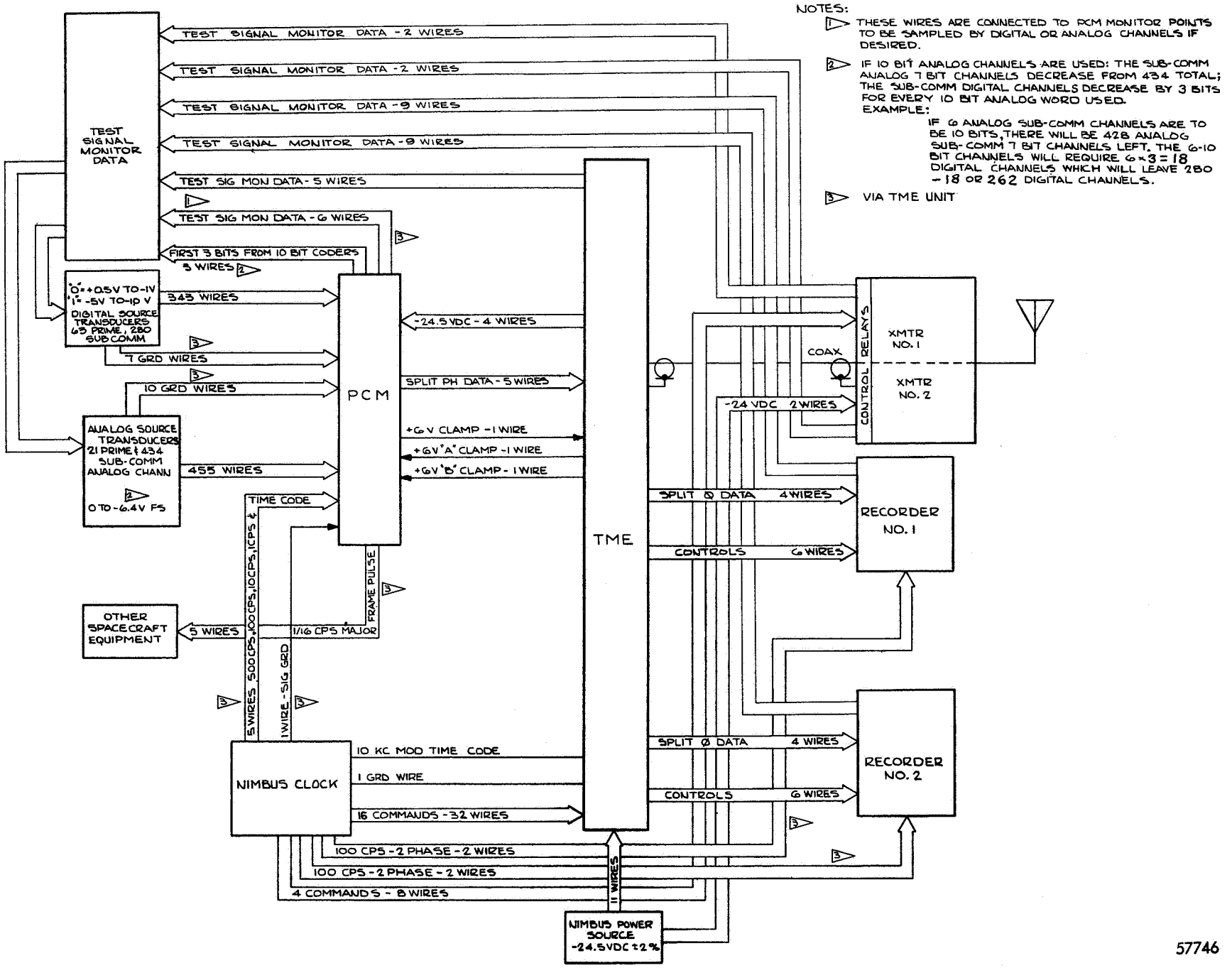


Figure 1. Nimbus B PCM Telemetry Subsystem, Simplified Block Diagram

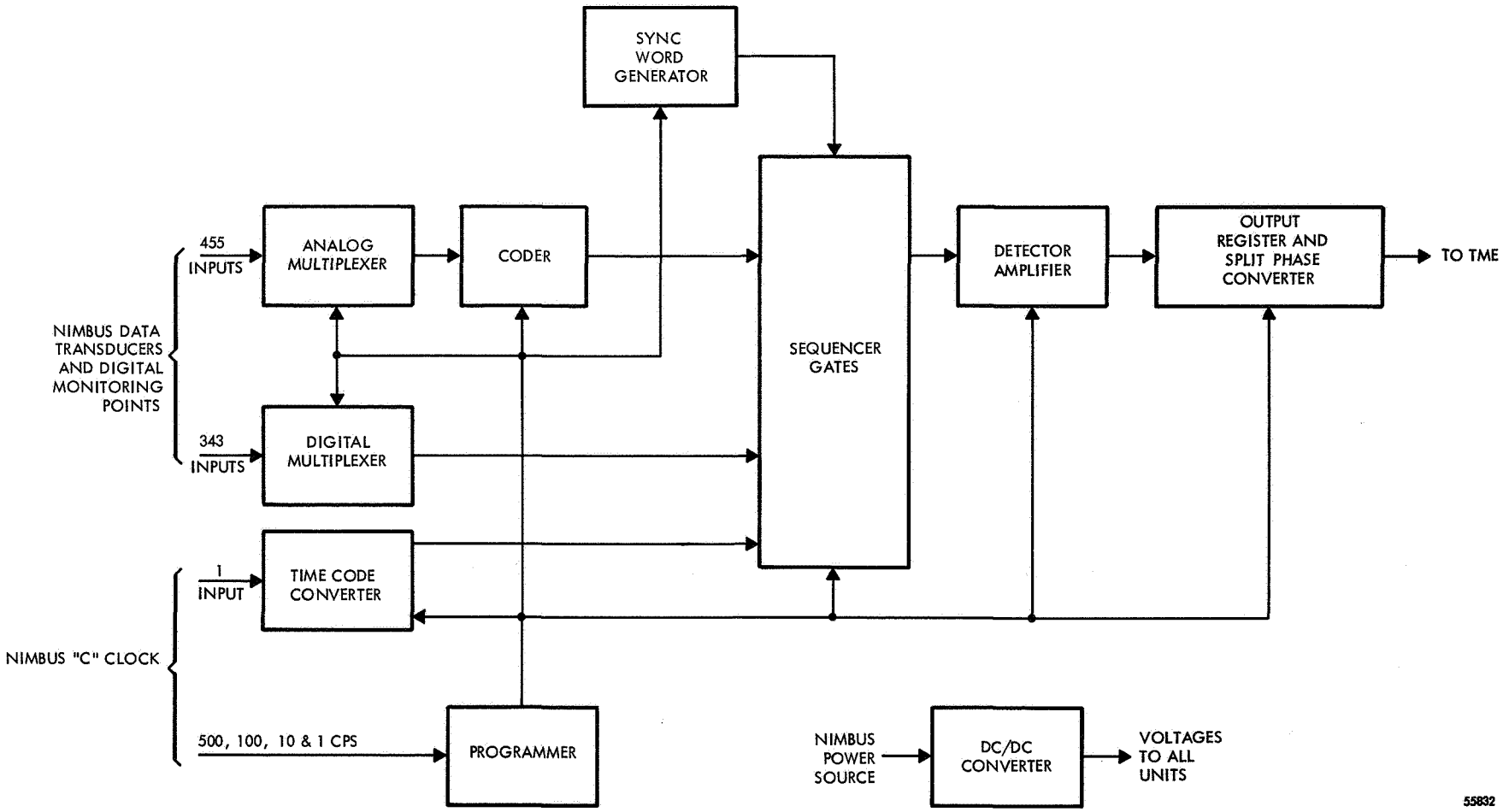


Figure 2. PCM Signal Flow, Simplified Block Diagram

The split-phase code is one of six inputs to the TME that interface with PCM Unit, Nimbus C clock, tape recorders, and power source.

A modulated 10 kc time code from the Nimbus C clock is applied to the TME for transmission of time code only, or for mixing with PCM real time data. The time code input is relay controlled within the TME. Two other inputs from Nimbus C clock are the nonlatching-relay and latching-relay commands. Nonlatching relays drive four parallel latching relay coils to reduce the total load on the Nimbus C clock command circuits. Command relays control the on-off states of the TME contained equipment, the tape recorder record/playback modes, and time code applications.

Split-phase data constitutes two more inputs to the TME. One is the PCM real time input and the other is the record data input. Real time PCM inputs are mixed with the 10-kc time code for transmission, and record data inputs are applied to two record amplifiers for routing to one or both of the tape recorders.

The TME controls all data routing through relay switching upon command from the ground. The data word is applied to the transmitter for real time data transmission or to either one or both of the tape recorders for temporary storage. Each tape recorder can store a maximum of 108 minutes of data. The normal Nimbus orbit is to be 96 minutes; thus, adequate storage capability exists. In addition, one tape recorder can be swtiched off while the other is recording and when full, the first one switched on and the second switched off to provide a maximum of 216 minutes of recording time. The tape recorders play back upon command from the ground.

Figure 3 illustrates the method of interface cabling to connect the complete airborne subsystem.

1.3.2.1 PCM UNIT - GENERAL DESCRIPTION. The PCM unit accepts electrical inputs from various equipment in the Nimbus B spacecraft through input gates designed fail-safe, thus protecting the inputs from damage in the event of transient power surges. In the event such an extreme condition does occur, no more than eight data channels will be lost as the result of one input gate failure. To increase reliability, the PCM Unit, except for input gates and prime data channel selectors, is block redundant; i.e., two of every assembly are contained within the PCM Unit. These complete, yet separate, assemblies are designated PCM No. 1 (A) and PCM No. 2 (B). Only one PCM assembly operates at any given time. Operational selection is made from the ground station which commands PCM 1 or PCM 2 through a relay in the TME unit.

The PCM unit, shown in figure 4, is encased in a machined magnesium housing six inches wide, eight inches high and 6-1/2 inches long. The complete unit, less cabling, weighs approximately 10.75 pounds, and contains both discrete and integrated circuit components. Block redundant assemblies are the following:

a. Programmer
b. Multiplexer Control Circuits
c. Analog-to-Digital Converter (Coder)

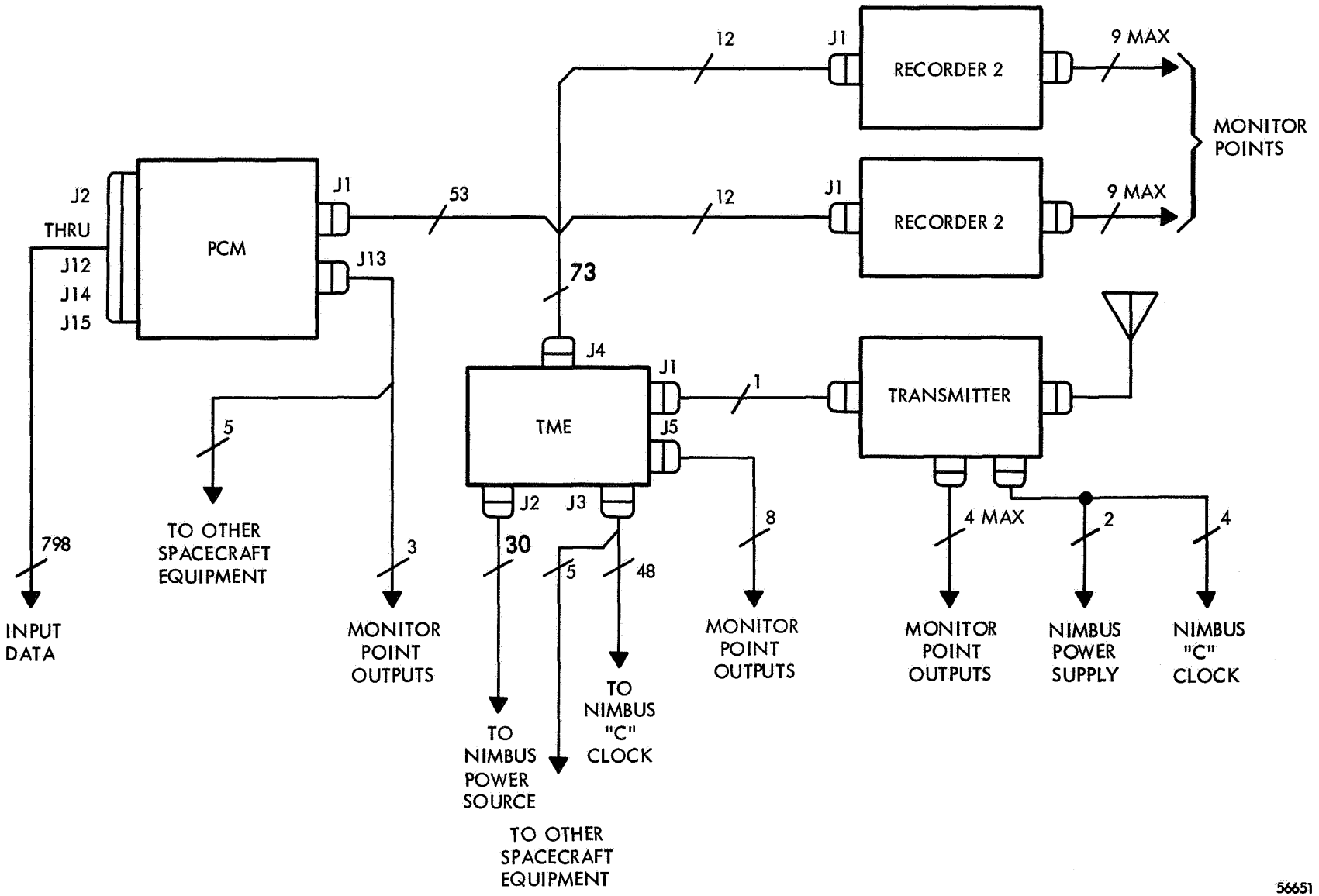
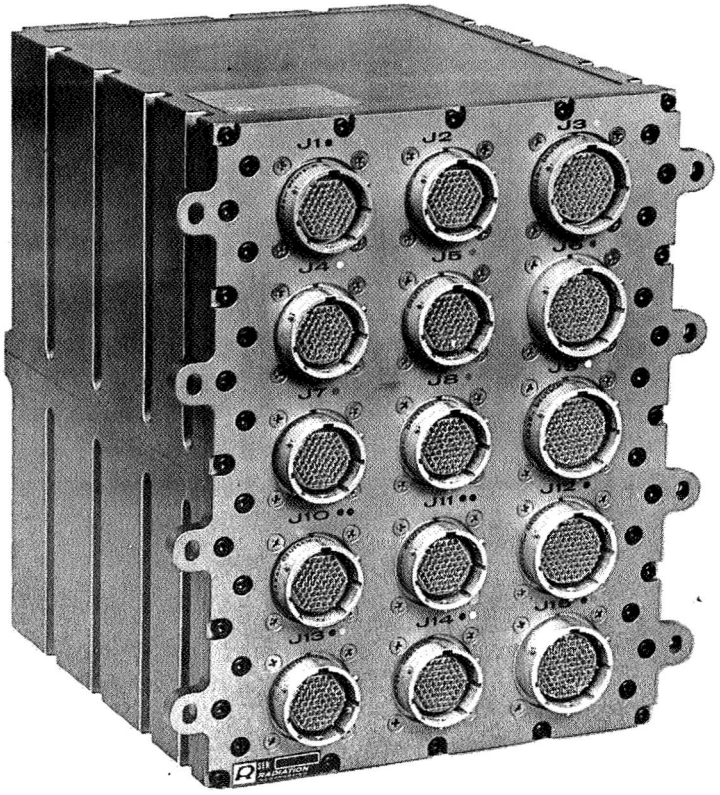
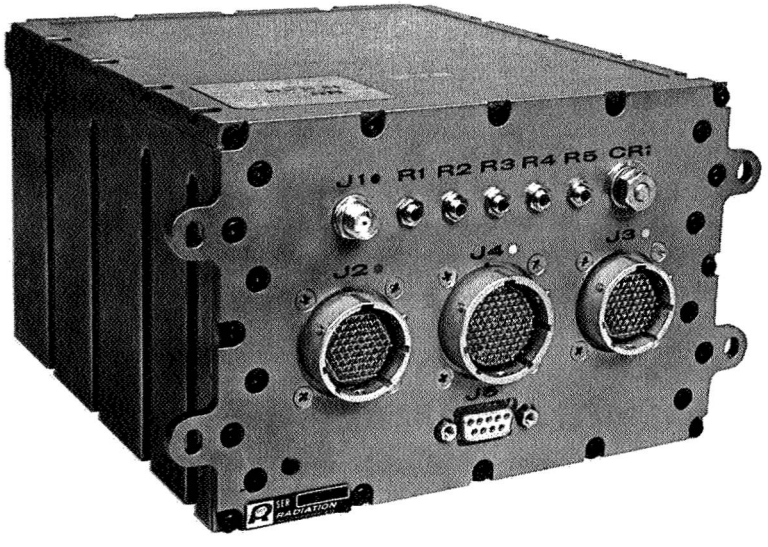


Figure 3. Nimbus B PCM Telemetry Subsystem, Interface Wiring Diagram



PCM



TME

57900

Figure 4. PCM and TME Units

d. Power supply
e. Output Register and Split-Phase Converter

Two construction techniques were employed in internal packaging of the electronic assemblies: (1) cordwood modules on 2-layer cards, and (2) planar assembly on 6-layer multilayer card assemblies.

Fifteen multi-pin connectors are mounted on one face of the unit and provide facility for all input/output interface cabling as shown in figure 3. Connectors J3, J6, J9, J12, and J15 are 85-pin connectors; the remaining are 65-pin connectors. Connectors J2 through J12, J14, and J15 provide inputs for all digital and analog measurement data. Connector J13 supplies outputs to other spacecraft equipment and three monitor points. Connector J1 provides the interface connection to the two tape recorder modules and the TME unit.

1.3.2.2 TME UNIT - GENERAL DESCRIPTION. The TME unit, shown in figure 4, acts as a relay switching network and signal amplifier between the PCM unit and output transmitter and tape recorders and between the Nimbus C clock and output transmitter. The TME performs four distinct functions: (1) switches serial split-phase Mark 0 data from the PCM unit to the tape recorders for temporary storage, or to the transmitters for real-time data transmission, or both simultaneously, on command; (2) switches to data playback from the tape recorders on command; (3) provides for time code transmission either superimposed on the real-time data or separately; and (4) provides externally adjustable controls for transmitter modulation.

Reliability of the TME unit is enhanced by complete circuit redundancy except for the passive summing network and relay armature coils which are nonredundant. The record amplifier, playback amplifier, and summing amplifier are block redundant.

The TME unit is contained in a machined magnesium housing four inches high, six inches wide and 6-1/2 inches in depth. The complete TME containing the electronics packaging on multilayer cards weighs approximately 4.25 pounds. Printed circuit cards include the two-layer discrete component type and the four-layer integrated circuit types. Modules, relays, and prior parts are mounted on the cards with hard wiring used for circuit connections. The TME contains the following modules and assemblies:

a. Two record amplifiers
b. Two playback amplifiers
c. Two summing amplifiers
d. Five signal monitor circuits
e. Seventeen control relays

All input/output interface connectors are located on one face of the TME unit. Connectors include TNC coaxial connector J1 for connection to the transmitter; an 85-pin connector J4 that provides the interface connections to the PCM unit and both tape recorders; two 61-pin connectors J2 and J3 that connect to the Nimbus power source, Nimbus C clock, and other spacecraft equipment; and a 9-pin connector for all signal-monitor outputs. Five gain control potentiometers R1 through R5 are also provided for adjustment of modulation levels into the transmitter. Zener diode CR1 is located on the TME front panel for convenience and is used for overvoltage protection to the PCM unit multiplexer.

1.3.3 BENCH TEST EQUIPMENT

The Bench Test Equipment (BTE) shown in figure 5 is a special purpose test set capable of testing a Nimbus B PCM Telemetry Subsystem that consists of a PCM unit, a TME unit, two tape recorders, and a telemetry transmitter. The BTE is also capable of testing individual PCM or TME units.

The BTE simulates and provides the necessary control, command, and timing signals to a PCM Telemetry Subsystem under test that would normally be supplied by the Nimbus C clock. When testing the operation of a PCM or TME unit separately, the BTE simulates signals other subsystem components would normally supply. The BTE also simulates analog and digital inputs from the transducers and test points within the Nimbus Satellite, and it generates split-phase Mark 0 data that is applied to the PCM Telemetry Subsystem. The data is then returned to the BTE for comparison with preselected analog and digital data. The BTE scans the type of data selected and upon command, compares it against either analog or digital tolerance switches to determine if the data is within tolerance. Error conditions exist when data is out of tolerance. Should an error be detected, the BTE displays the erroneous word, the word number, and subframe number and then stops. Through programming, the BTE can scan continuously and indicate data errors through GO/NO GO indicators without stopping, unless programmed to do so when an error is detected. The BTE has a self-check feature whereby split-phase Mark 0 data is applied directly to the BTE unit.

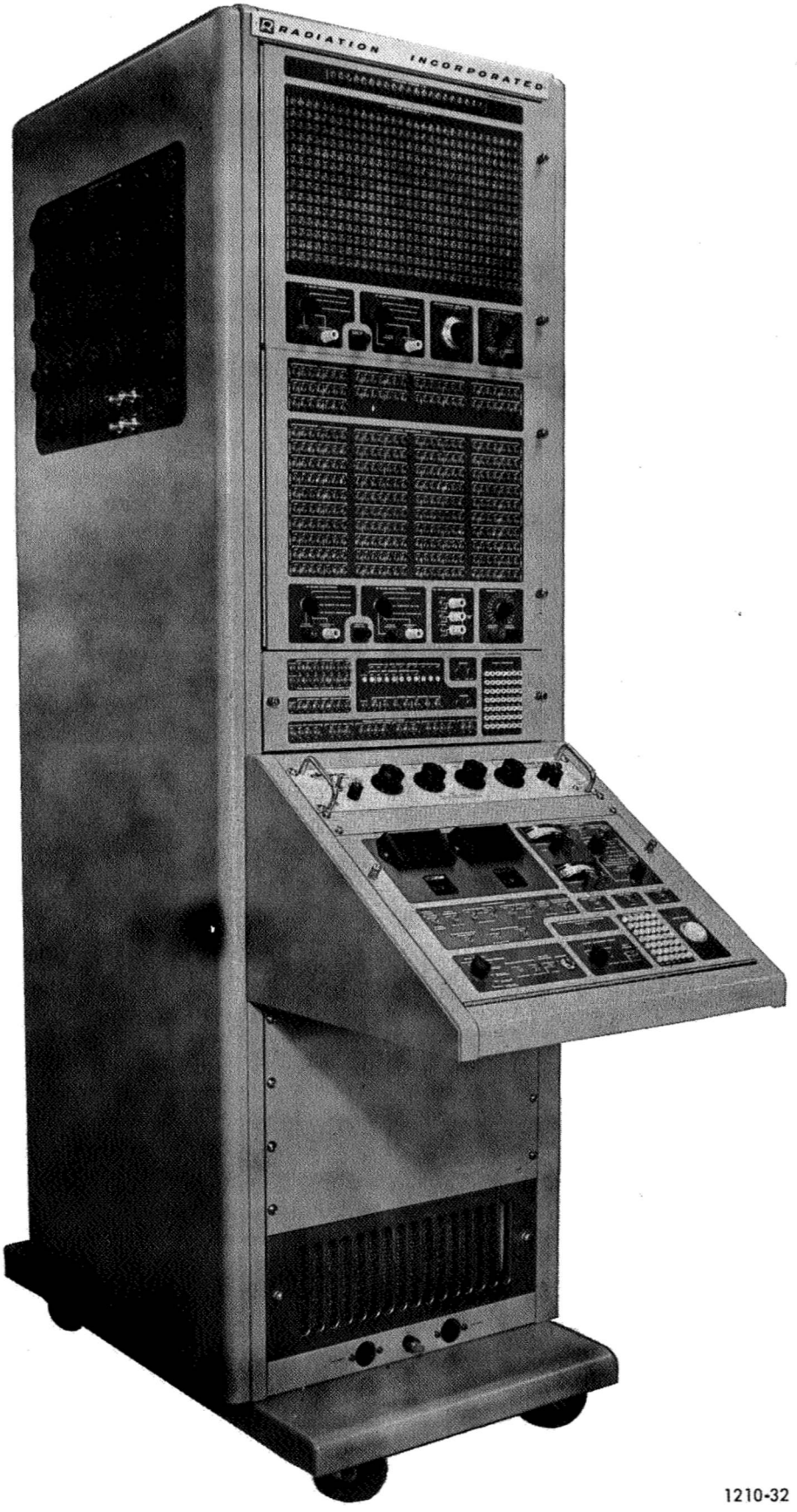
The complete BTE is composed of subunits contained in a single equipment cabinet mounted on casters for mobility. Access to the interior and subunits is gained through a full-length rear cabinet door, sectional front doors, and slide-mounted drawer assemblies. All operating controls and indicators are located on the front panels or on the console face. A connector panel is located on the side for test interface cable connections.

BTE unit power is self-contained, requiring only a single primary source. Internal power to all logic components is supplied through five system-contained commercial power supplies.

1.3.4 GROUND STATIONS

1.3.4.1 GENERAL. The ground portion of the Nimbus B PCM Telemetry Subsystem comprises five ground stations of varied configurations located at three sites. System configurations generally contain Radiation-built racks 3, 4, 5 and 6 with varying quantities of supplementary equipment racks. Equipment racks used in building up a system are shown in figure 6, and detailed descriptions of the various equipment configurations are discussed in Section V of this report. The primary function of all ground stations is identical regardless of configuration. Configuration differences occur generally in the method of data storage and display.

The Nimbus B PCM Ground Station receives and processes telemetered PCM data, including time code data, from the Nimbus B Satellite System. The data is processed in real-time at a 500 cps bit rate (split phase/single SP/S) or stored for later playback and processing at a 15 kc (SP/S) bit rate.



1210-32

Figure 5. Bench Test Equipment, Front View



Figure 6. Nimbus B PCM Ground Station Cabinets

The data format for both the 500 cps and 15 kc signals is constant and consists of sixteen 62.5-word frames. Each frame contains 16 bits (2 words) of frame sync information and four bits of coded subframe identification data (SFID). Each of the remaining 60 words in the frame contain eight bits of data.

Serial PCM input data is switch selected and applied to the system control logic at the real-time 500 cps bit rate or at the playback 15 kc bit rate. System-control conditions the data handling logic for operation at the respective bit rates. The serial PCM is routed through system control to the bit synchronizer for data reconstitution and conversion to NRZ. The regenerated serial data is applied to the group synchronizer with associated clock pulses where the data input is processed to obtain data synchronization and timing to drive system output devices. Digital processing includes the conversion of the input data from serial to parallel and then extracting the digitized data from selected words for application to the various storage and display devices connected to the system. Of these selected outputs, some drive the time code display, others are supplied to a digital-to-analog converter for conversion, and some parallel outputs are supplied to the computer interface circuitry. Group synchronizer also generates the frame and word gates used in the subsequent logic for data extraction.

Output devices are driven by the extracted parallel data. Of this data, 32 channels are available after conversion to drive analog plotting oscillographs, any of 52 preselected channels are available to drive the event recorder with digital on-off data, and all parallel outputs are supplied to the computer interface where it will be presented to the computer for processing according to a particular computer program. Two magnetic tape recorders are provided as part of the computer system, enabling partially processed data to be stored for later printout.

1.3.4.2 SYSTEM CONTROL. The PCM data from the receiver, Minicom recorder, or from the PCM-signal simulator is routed to the system control. Real-time data from the satellite may be routed through the system control to the Minicom recorder for later playback. PCM data to be processed is routed through to the bit synchronizer.

The system control conditions the bit synchronizer and computer input circuitry to handle the incoming data through the use of 15 kc and 500 cps frequency select squelch lines. Remote address strobing of the selected bit synchronizer data processing circuit is also provided by the system control using a word rate gated with the non-sync confidence signal from the group synchronizer. In a non-sync confidence condition, manual strobing of the bit synchronizer may be accomplished by a momentary switch on the system control panel until the system is in sync.

1.3.4.3 SIGNAL CONDITIONER 5220-A (BIT SYNCHRONZER). The bit synchronizer accepts serial PCM data in a varity of codes and over a wide range of bit rates. Data input sources include receiver, magnetic tape recorder, and simulator and are switch selected. The synchronizer is equipped with a means of remote selection by commands from a computer, or other device, to establish operating parameters such as bit rate and input code. Once programmed, either locally or remotely, the signal conditioner synchronizes a local clock to the incoming data and performs bit decisions on the incoming data. It, in turn, provides a regenerated serial data and phased clock pulses at preselected bit rates to the group synchronizer.

1.3.4.4 GROUP SYNCHRONIZER. The group synchronizer recognizes a frame synchronization code (programs units) each subframe and in turn generates synchronization and gate pulses at frame and word rates for application to the decommutator portion of the system. Once the system is synchronized to the incoming data, the group synchronizer converts the serial input data to parallel data. Parallel outputs are routed to a digital decommutator and time code display, computer input circuitry, and digital-to-analog converters. Sync pulse outputs command station logic in the extraction of data and time code for storage and display.

1.3.4.5 ANALOG DECOMMUTATION AND RECORDING. The analog decommutator accepts synchronization pulses from the group synchronizer including an SFID "locked" indication. It, in turn, generates the transfer pulses to the digital-to-analog converter for channel selection and decoding. The digital-to-analog converters receive parallel input data from the group synchronizer, and together with the transfer pulses from the decommutator, generate the analog equivalent of the input digital data for application to brush recorders. Thirty-two selectable channels of analog data are available to the recorder. The decommutator supplies word and minor frame gate signals to the digital decommutator and time code display.

1.3.4.6 DIGITAL DECOMMUTATOR AND TIME CODE DISPLAY. The digital decommutator and time code display extracts and processes digital data contained in certain words of the Nimbus B format, and then drives system digital event recorders and a NIXIE time display. Up to 56 digital on-off inputs can be recorded and are patch-panel selected from any parallel data inputs to the event recorder. Time-code data and marker traces are permanently wired to traces 1 and 59, and 2 and 60. Patch selectable channels are routed to traces 3 through 58.

1.3.4.7 COMPUTER INPUT CIRCUITRY AND COMPUTER SYSTEM. The computer input circuitry interfaces the computer system to the PCM ground station decommutator. The computer input circuitry accepts incoming parallel data from the group synchronizer and prepares it for application to the computers system. The computer evaluates selected PCM telemetered data according to the computer's program and provides a printout of all telemetered data.

1.3.4.8 GROUND STATION CHECKOUT. A ground station checkout capability is provided by the PCM signal simulator incorporated in the system configuration. The simulator generates the various input signals required for system operation and evaluation. The outputs provided by the PCM signal simulator include a simulated PCM video data (SP/S) signal to the system input, NRZ and bit rate to the group synchronizer, parallel data and frame/word rates to the decommutator, synchronization signals to the computer input circuitry, and a simulated computer input to the computer.

Aside from system evaluation and checkout, the PCM signal simulator used in conjunction with the system-contained dual-trace oscilloscope, RF signal generator, and frequency counter can be used for fault isolation and troubleshooting.

SECTION II

PCM TELEMETRY UNIT

SECTION II

PCM TELEMETRY UNIT

2.1. INTRODUCTION

This section of the Nimbus B final report describes the PCM Telemetry Unit. This section includes a general description of the electrical model (designed and built under contract NAS 5-3787) and a block diagram level description of its operational and functional characteristics. Following this is a discussion of certain design modifications incorporated into the electrical model in the development of the prototype and flight models under this contract.

2.2. NIMBUS B ELECTRICAL MODEL GENERAL DESCRIPTION

The Nimbus B PCM Unit shown in figure 7 accepts electrical inputs from various equipment in the Nimbus B spacecraft, formats these inputs into PCM code, and routes them through the TME unit to the tape recorders for temporary storage or to transmitters for transmission to ground stations. The electrical inputs are both analog and digital. Analog inputs are converted to an equivalent 10-bit digital word. Individual digital inputs are correlated into a 7-bit word. The seven most significant bits of the converted analog words and digital words are combined with a word sync bit to form a standard 8-bit word. These 8-bit words are time multiplexed, converted to a split-phase, Mark 0 code, and routed to the TME unit. The three least significant bits of the analog code can be used for improved resolution of selected words. A simplified block diagram of the PCM unit is presented in figure 8.

The PCM unit format contains a total of 1000 time slots per data frame. A data frame consists of 16 subframes, each of which contains 62.5 8-bit words. A data frame is accumulated in 16 seconds. Of the 1000 8-bit time slots available per data frame, 40 are sync, 6 are time code, 336 are utilized for 21 prime analog channels, 434 are subcommutated analog channels, 144 are utilized for 63 prime digital channels and 40 are utilized for 280 subcommutated digital channels. Prime channels are sampled once per second and subcommutated channels are sampled once every 16 seconds. Seven digital channels comprise one time slot.

Analog inputs are obtained from transducers supplying a voltage to a ramp-type analog-to-digital converter (coder) which converts the transducer voltage to an equivalent 10-bit digital word. Normally, the seven most significant bits (MSB) of the converted word are retained as the data and the three least significant bits (LSB) are either discarded or reinserted after the respective digital sample for increased resolution. One or more of the three least significant bits already coded can be inserted into a digital channel immediately following the analog channel for which increased resolution is desired.

A word sync bit is added as the MSB of the 7-bit data word, thus making every analog and digital data word an eight-bit word. The difference between an analog and digital word is that the seven data bits of the analog word always present a digitized voltage while the seven data bits of the digital word can be seven different on/off functions.

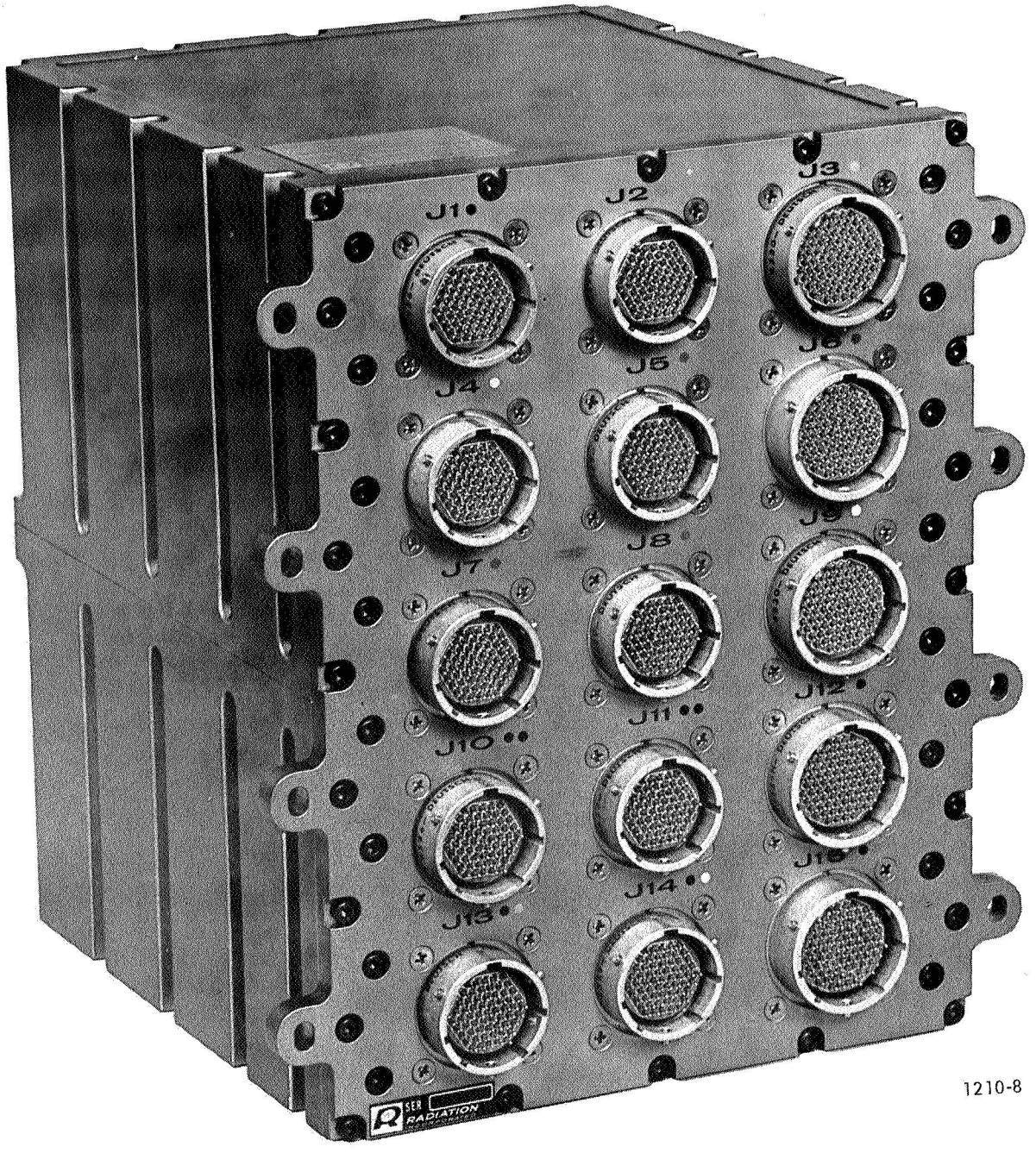


Figure 7. PCM Unit

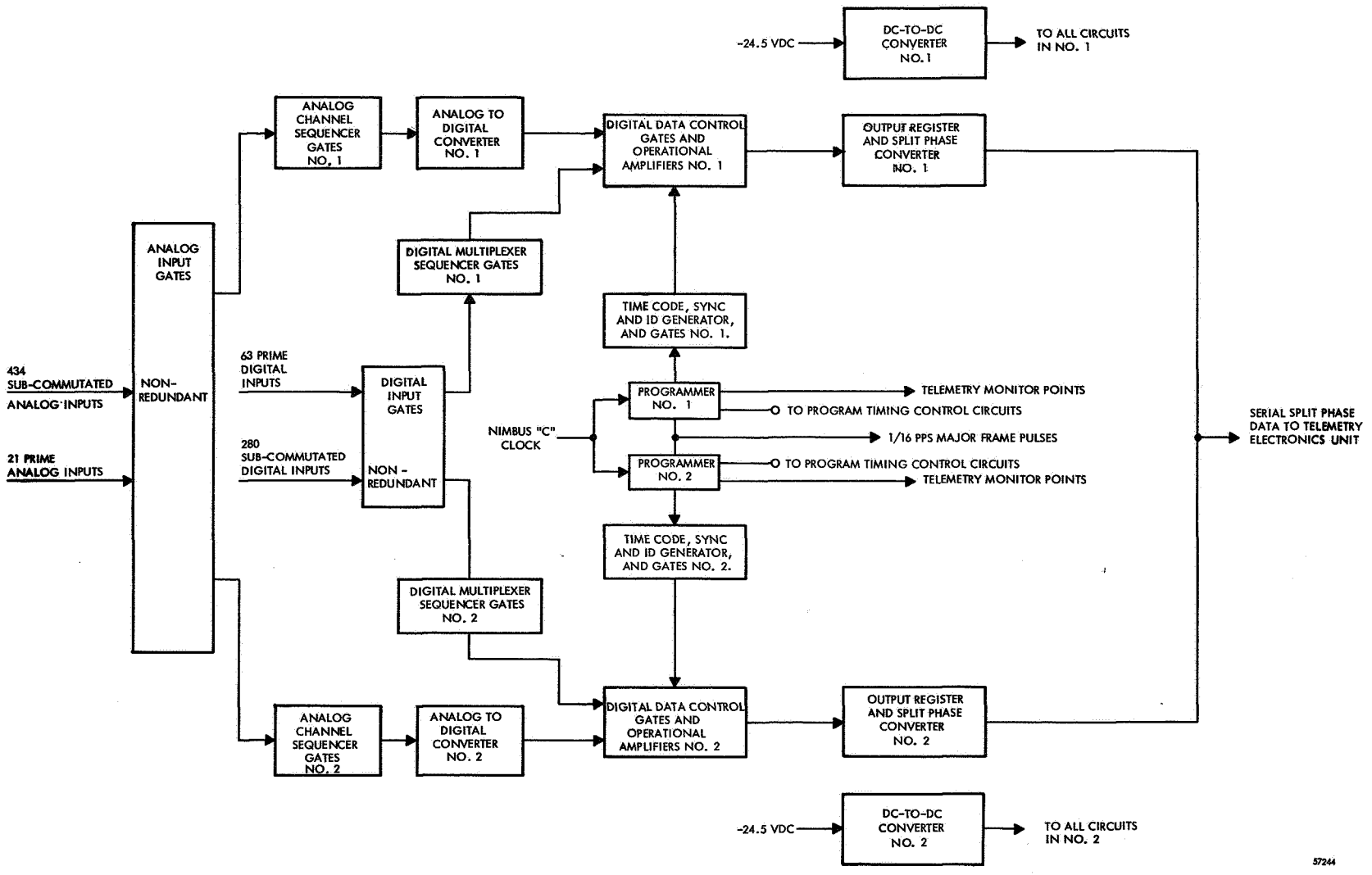


Figure 8. PCM Unit Functional Block Diagram

The PCM unit follows a pre-established program that is hardwired into the unit. Thus, external interface determines which experiments are sampled as prime channels and which are subcommutated channels, as well as which experiments are analog and which are digital.

All input gates are designed fail-safe, meaning that their inputs are protected such that power surges cannot damage the gate except under extreme over-voltage conditions. In the event such an extreme condition does occur, the PCM unit is wired so that no more than eight data channels will be lost as the result of the failure of one input gate.

The PCM unit, except for the input gates and the prime data channel selectors, is block redundant; i.e., there are two of every assembly in the unit. These complete, yet separate, assemblies are designated PCM No. 1 (or A) and PCM No. 2 (or B). Only one PCM assembly operates at any given time; the operational selection is made from the ground station which commands PCM 1 or PCM 2 through a relay in the TME unit.

2.2.1. MAJOR PHYSICAL AND ELECTRICAL CHARACTERISTICS

This paragraph outlines major physical and electrical characteristics of the current improved Nimbus B PCM Unit. Descriptions cover physical dimensions of the unit and the mechanical and electrical packaging concepts employed in its manufacture. Printed-circuit card packaging, interconnecting, and reference designations are also described. In addition, electrical characteristics are tabulated describing functions and operating parameters of PCM signals.

2.2.1.1. PHYSICAL CHARACTERISTICS. The mechanical packaging of the Nimbus B PCM utilizes a compression-packaged technique first proven on the Nimbus A and Telstar PCM telemetry systems. In utilizing this technique, the electronics are integrated into what is effectively one mass, allowing a thin-walled lightweight housing design to be utilized. This housing design is possible because the walls of the unit are in tension only, while the bending moment is applied to the rigid ends of the housing. Weights of these end panels are minimized, while rigidity is maintained by drilling holes in the panel, which are then filled with foam. The rigidity is enhanced in the Nimbus B unit by adding a bonded-on panel, thus creating a "sandwich" structure. Characteristics of the Nimbus B system are shown in table 1.

Table 1. PCM Mechanical and Packaging Characteristics

Characteristic	Nimbus B PCM
Size	8" x 6" x 6-1/2"
Weight	10-3/4 lbs.
Housing	
Design	Closed Box
Finish	Electroless Nickel

Table 1. PCM Mechanical and Packaging Characteristics (Continued)

Characteristic	Nimbus B PCM
Connectors	
Manufacturer	Deutsch
Type	Standard Cylindrical
Environment Protection	Yes
Locking Device	Bayonet-lock
Packaging Concept	
Printed Circuit Card Type	2-sided/6 layer M/L
Internal Connections	Feed-through Bus Wires and Hard-wiring
Components	Discrete and Integrated Circuit
Internal Packaging Structure	Yes
Internal Vibration Isolation	Yes
Compression-Loaded	Yes
Component Packaging	Modular and Planar

2.2.1.1.1. MECHANICAL PACKAGING. The mechanical integrity of the system relies upon a preloaded electronics assembly (figure 9). Utilizing this preloading technique, the electronics are integrated into what is effectively one mass, allowing a thin-walled, lightweight housing design to be utilized. This is possible since the walls of the housing are in tension only, while the bending moment is applied to the rigidized ends of the unit.

This concept was implemented through the use of an internal electronics support structure, along with a separate system housing (figure 10). The electronics support structure consists of two aluminum pressure plates connected by six columns. The electronics assembly is placed into the support structure, and a hydraulic press is used to apply the required compressive load. Fiberglass and foam loading shims ensure that the desired loads and correct displacement are achieved simultaneously.

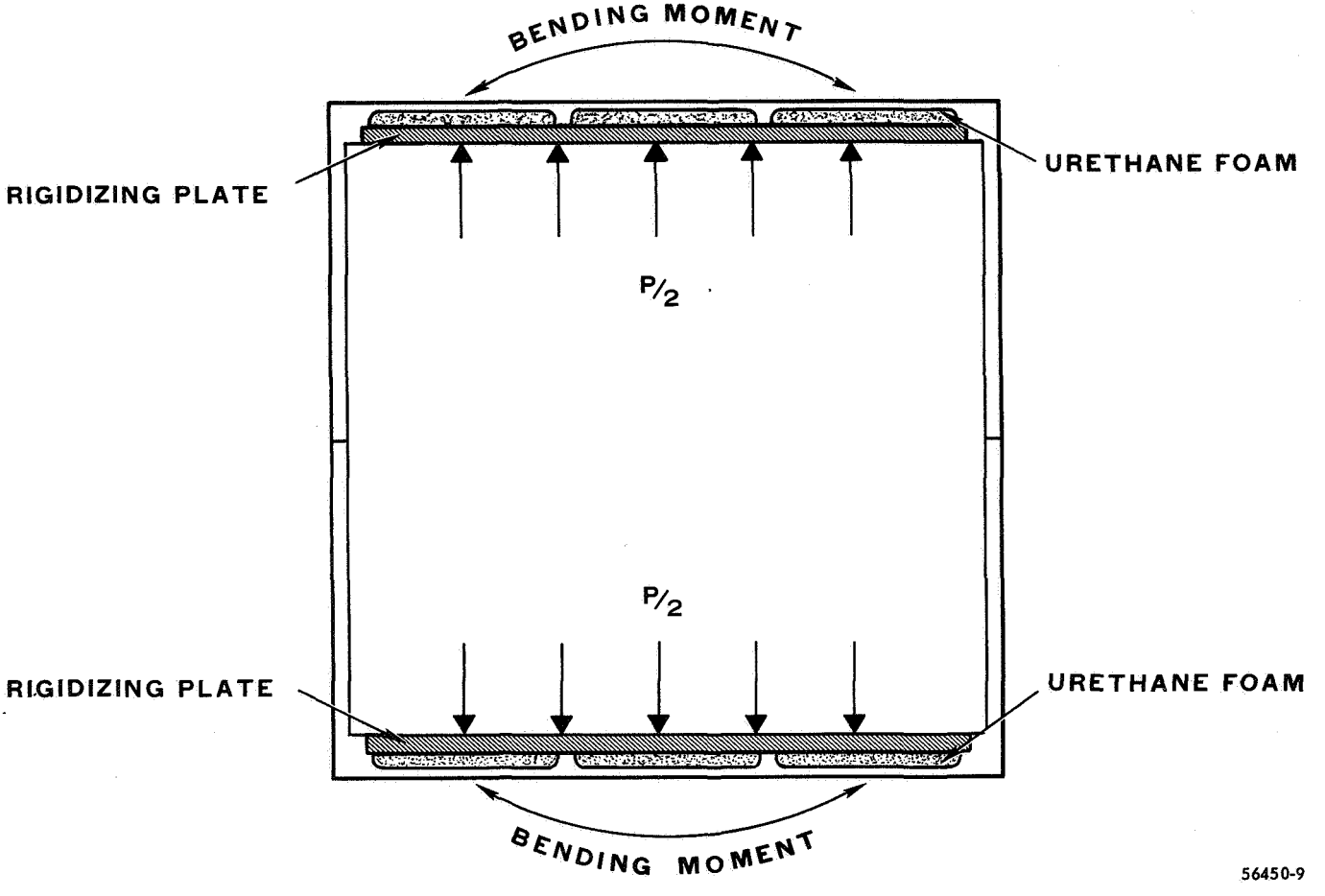


Figure 9. Housing Load Distribution

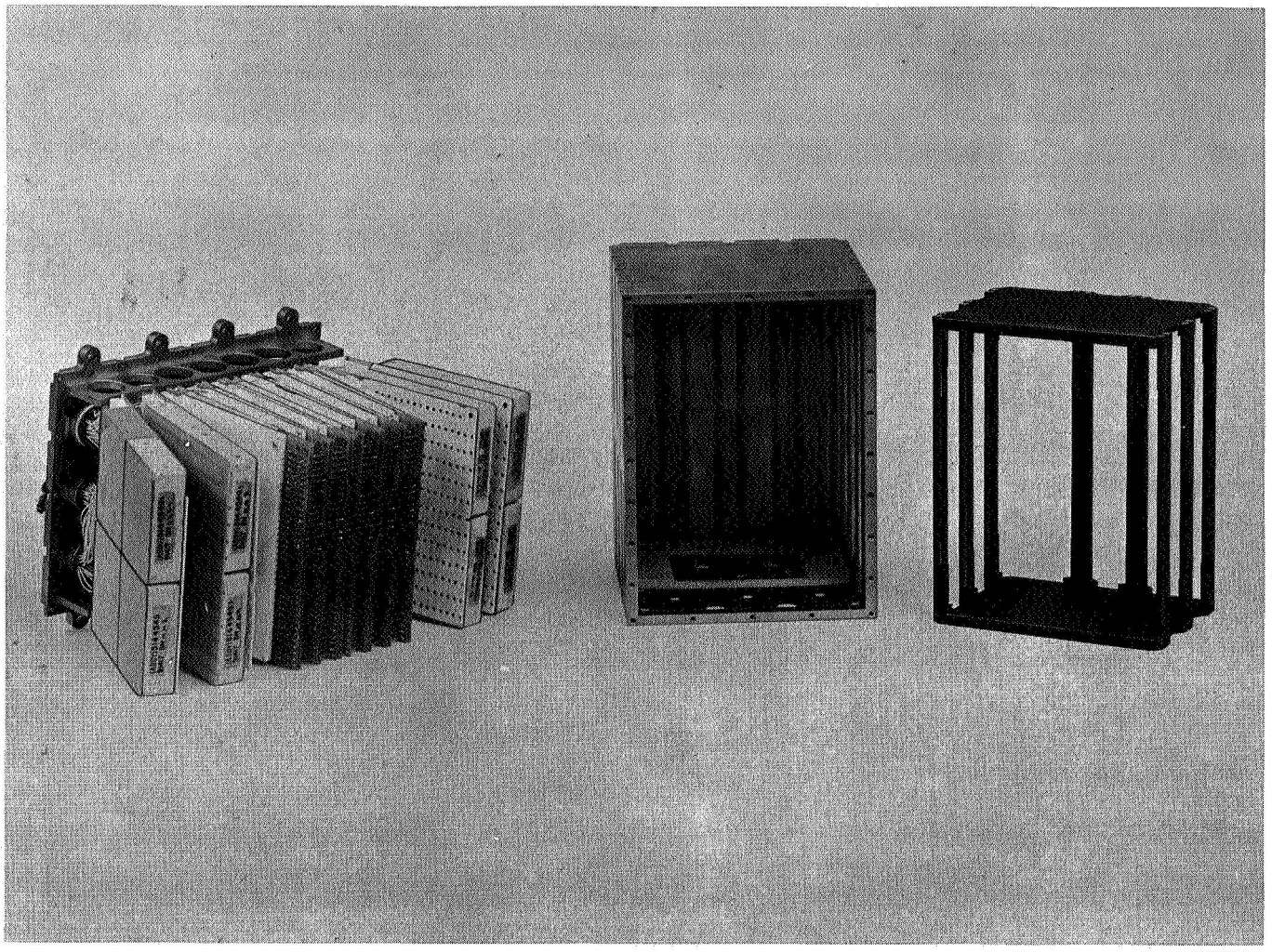


Figure 10. PCM Electronics, Housing, and Internal Structure

The electronics support structure provides for proper alignment of the card assemblies and also maintains the preload on the electronics. This allows the electronics to be completely assembled before insertion into the housing. It also permits complete system test and operation prior to assembly in the housing.

The housing consists of two machined monolithic magnesium structures. These structures, when secured together in a "clamshell" manner and with the front panel in place, provide support and protection for the electronics. The housing weight is minimized by using 0.040-inch walls wherever possible and through use of a rigid foam sandwich construction of the compression panels (ends of the housing).

When the system is assembled, the internal loading structure is separated from the housing by strips of foam silicon rubber bonded to the inside of the housing compression panels. These strips are designed primarily to provide high frequency vibration isolation, but also provide resonance control by being located around the perimeter of the compression panels. By locating the rubber strips in this manner, each of the two structures is exposed only to those areas of minimum displacement of one another when at their respective resonances. This technique has resulted in a maximum amplification factor (Q) of approximately 3.0 when vibration tested to qualification levels (sine - 10 g 0-peak maximum, 20 to 2,000 cps; random - 20 grms, 20 to 2,000 cps, 0.2 g^2/cps spectral density) in all three planes (figures 11 and 12). Part of this can be attributed to the excellent damping characteristics of the rubber strips, which, being compressed to 35% of their free thickness, are in a high stress condition and perform with a high degree of efficiency. The success of this packaging technique is illustrated by the fact that there were only negligible differences between simultaneous readings taken at various locations in the electronic stack during the testing.

To effectively compression-load the electronics, in which conventional and integrated circuit packages are mounted on the same cards, a common height denominator required for all of the assemblies was accomplished through the use of formed foam shims that conform to the shape of the components on the cards. This also provided a flat surface against which the next card assembly was placed (figure 13). The shims were made using tool cards for each type of planar packaged card in the system. The tool cards utilized dummy components slightly larger than those in the system to prevent loading on the actual system components. A sheet of thin latex rubber was stretched over the tool card and the card was placed in a mold. Foam was poured into the mold and cured. During the curing cycle, the foam expanded and conformed to the inside dimensions of the mold and, by stretching the rubber, assumed the contour of the tool card and its components.

Since the rubber sheet is not affected by either the foam or the curing bake, the mold was easily separated from the tool card.

The foam shim is molded to the exact form factor and component layout of the particular tool card utilized and is, therefore, keyed as to card and placement in the system.

2.2.1.1.2. ELECTRONIC PACKAGING. A thorough evaluation of several approaches to packaging the PCM for minimum size and weight was performed early in the program. This study indicated that both planar and modular packaging techniques had to be employed to

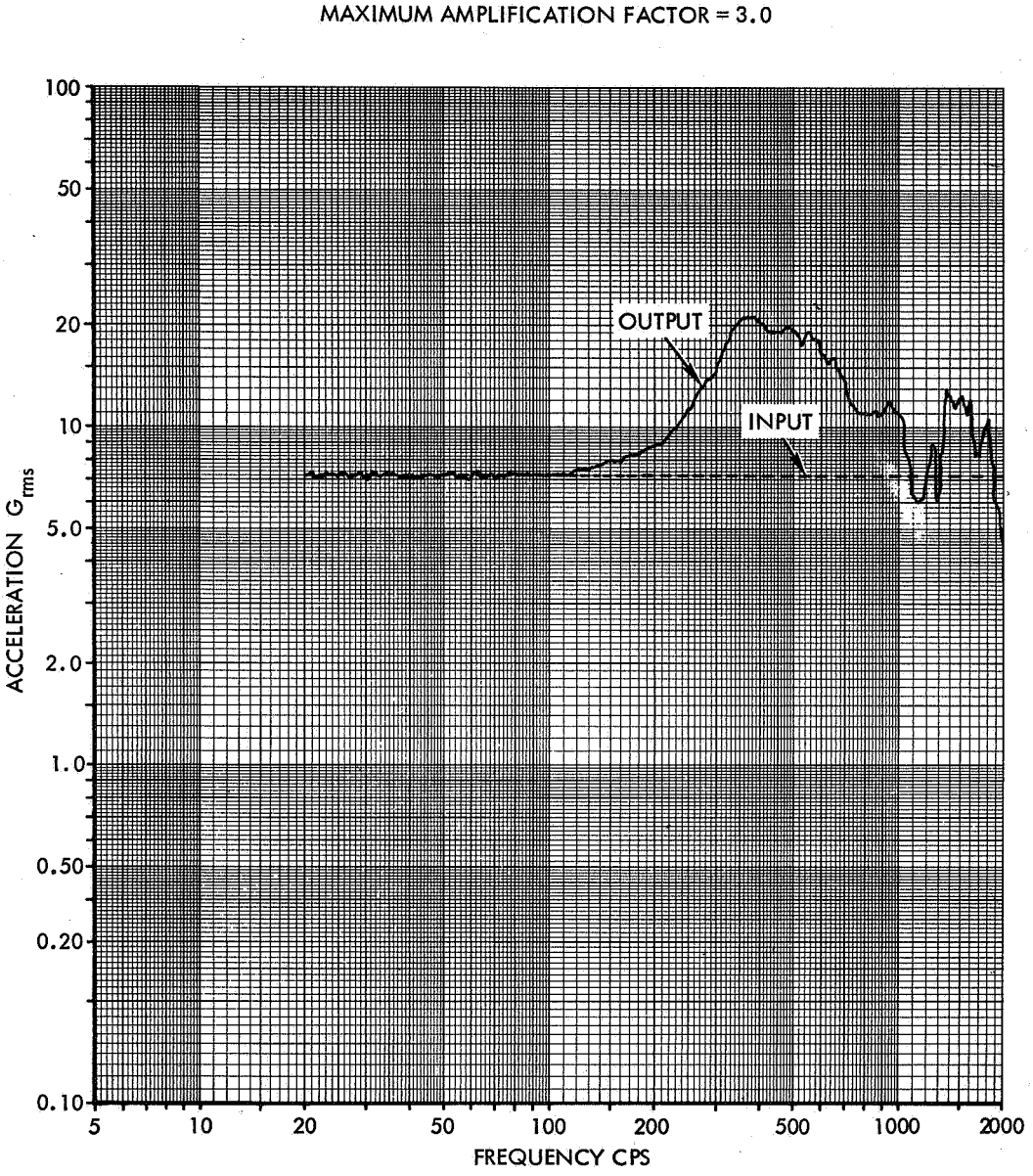
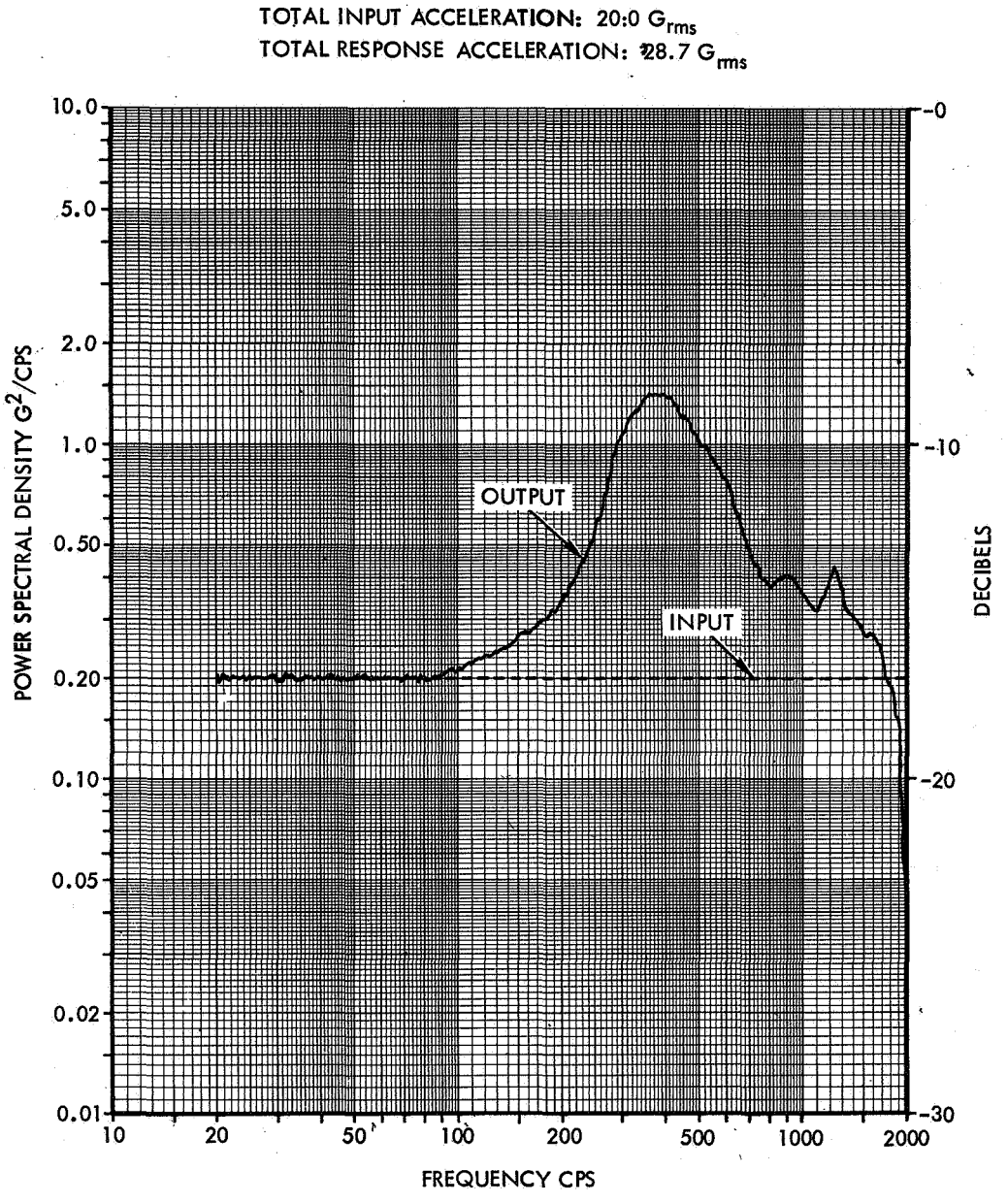


Figure 11. Maximum Response Within PCM Unit to Qualification Level Random Vibration



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Figure 12. Maximum Response Within PCM Unit to Qualification Level Random Vibration

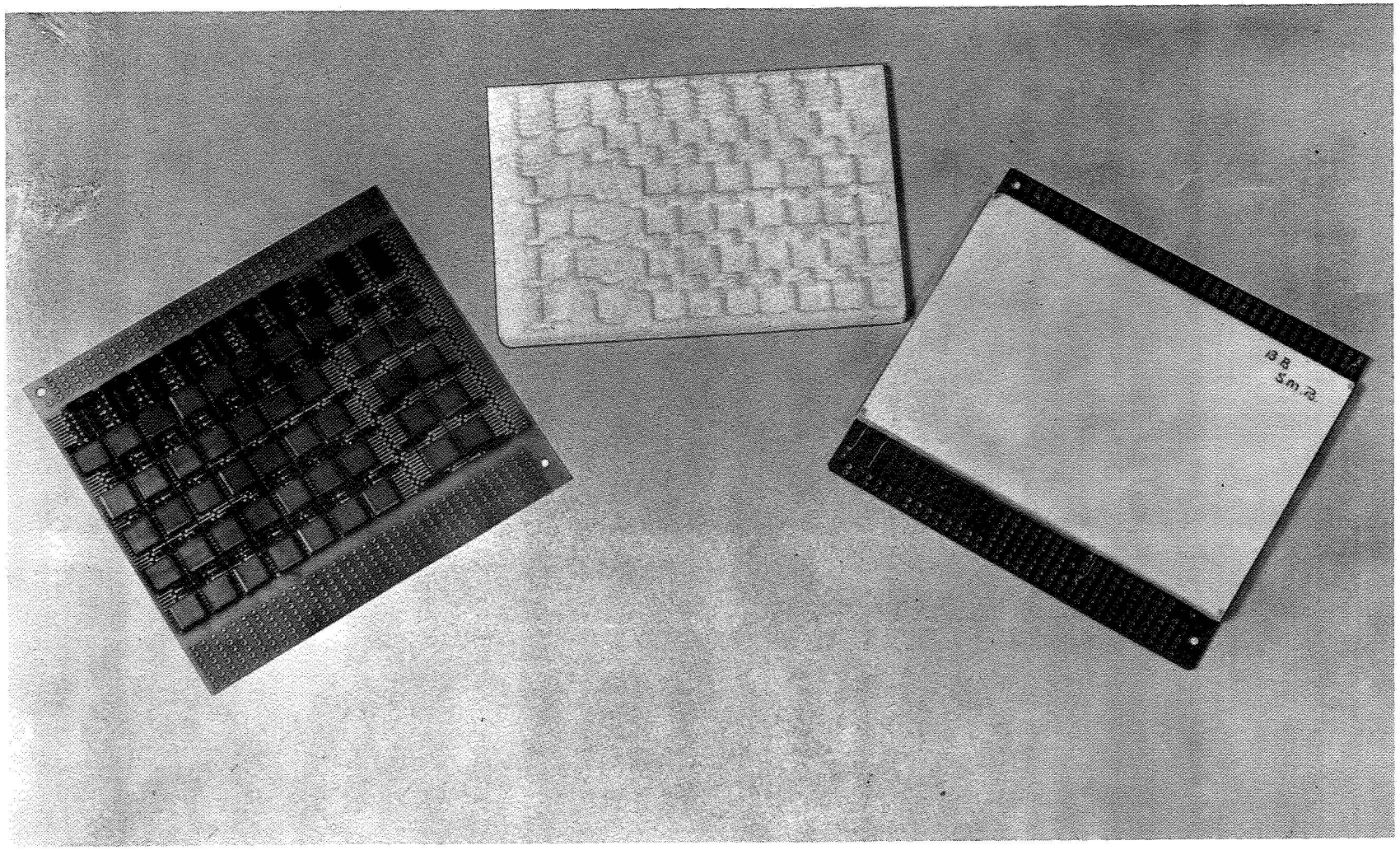


Figure 13. Tool Card, Formed Foam Shim, and Card/Shim Assembly

meet the system size requirements. A breakup of the electronics by circuit function showed that the power supply, programmer, A/D converter, and output register/split-phase converter circuitry all utilized conventional discrete components, while the multiplexer, timing and sequencer circuits utilized a combination of integrated circuits, microdiodes, and miniature resistors.

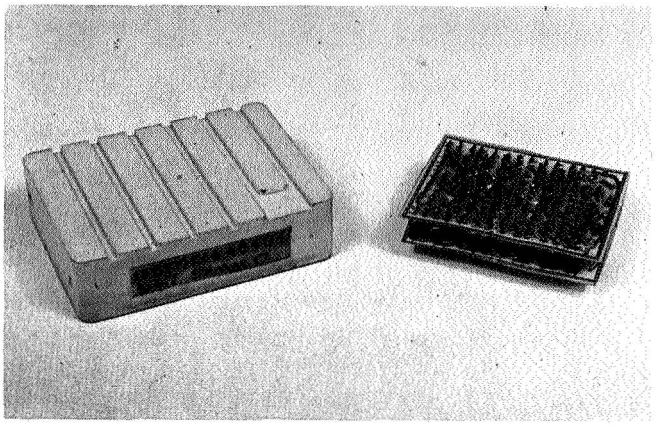
2.2.1.1.2.1. Modular Packaging Technique. A study of the parts/unit count showed that the A/D converter, programmer, power supply, and output register circuits could be packaged in eight 2 x 2.68-inch welded cordwood modules. This is accomplished by positioning the components parallel to each other between, and normal to, two mylar sheets. The components are interconnected by resistance welding nickel ribbon to the leads (figure 14.) Following electrical test, the welded field is coated with a conformal layer of epoxy to prevent stress during the foam-in-place molding operation. This molding is performed in cavities of accurate dimensions to provide modules of consistent size for the compressive loading operation.

The foamed modules are then mounted onto doublesided printed-circuit cards, having plated-through holes. The modules are secured to the card by soldering the module pins to the printed wiring pads on the opposite side of the card, thereby effecting the electrical interconnections.

These card assemblies, part of the redundant portion of the multiplexer, are located in two groups; one at each end of the card stack. Their reference designations, nomenclature, and packaging technique are referenced in table 2 and illustrated in figure 15.

Table 2. PCM Unit Card Assemblies and Reference Designators

Reference Designation	Card Nomenclature	Packaging Technique
1A1	Power Supply, A/D Converter Assembly	Cordwood Module
1A2	Programmer Output Register/Split-Phase Converter	Cordwood Module
1A3	Output Board 1A	Planar
1A4	Output Board 11A	Planar
1A5	Submatrix Board A1	Planar
1A6	Submatrix Board B1	Planar
1A7	Submatrix Board A2	Planar
1A8	Submatrix Board B2	Planar
1A9	Prime Matrix Board	Planar



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Figure 14. Cordwood Welded Modules (Before and After Encapsulation)

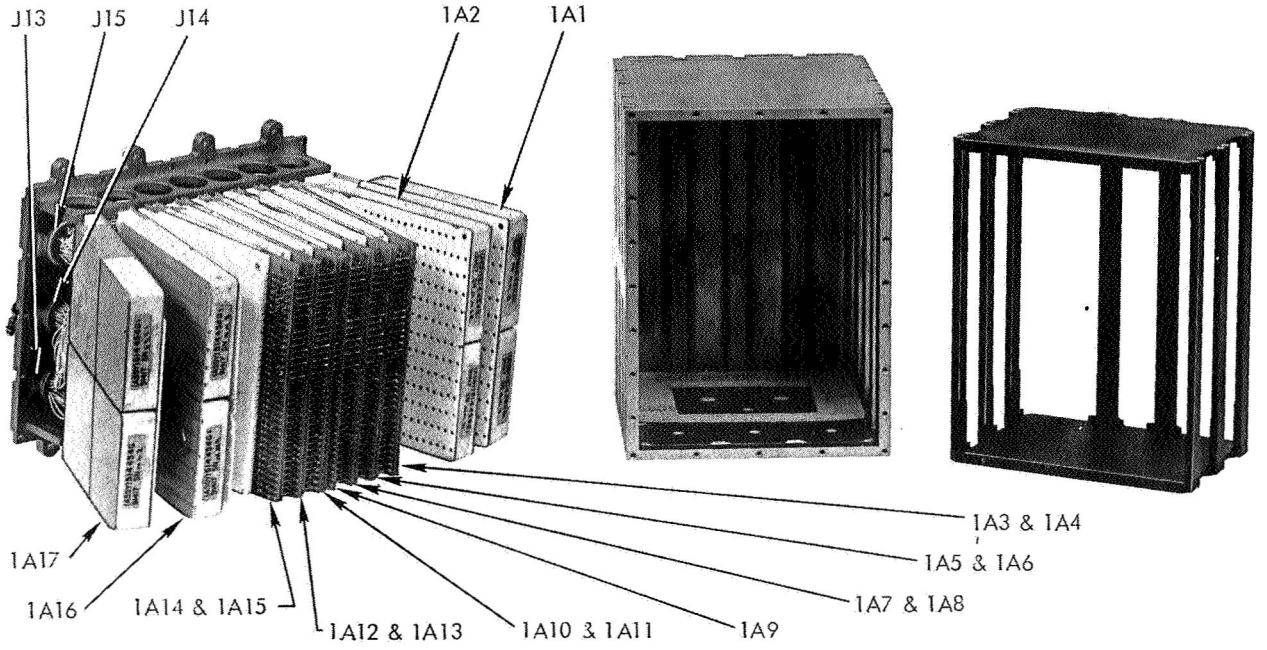


Figure 15. PCM Unit Subassembly Reference Designators

Table 2. PCM Unit Card Assemblies and Reference Designators (Continued)

Reference Designation	Card Nomenclature	Packaging Technique
1A10	Submatrix Board A3	Planar
1A11	Submatrix Board B3	Planar
1A12	Submatrix Board A4	Planar
1A13	Submatrix Board B4	Planar
1A14	Output Board 1B	Planar
1A15	Output Board 11B	Planar
1A16	Programmer, Output Register/Split-Phase Converter	Cordwood Module
1A17	Power Supply, A/O Converter Assemblies	Cordwood Module

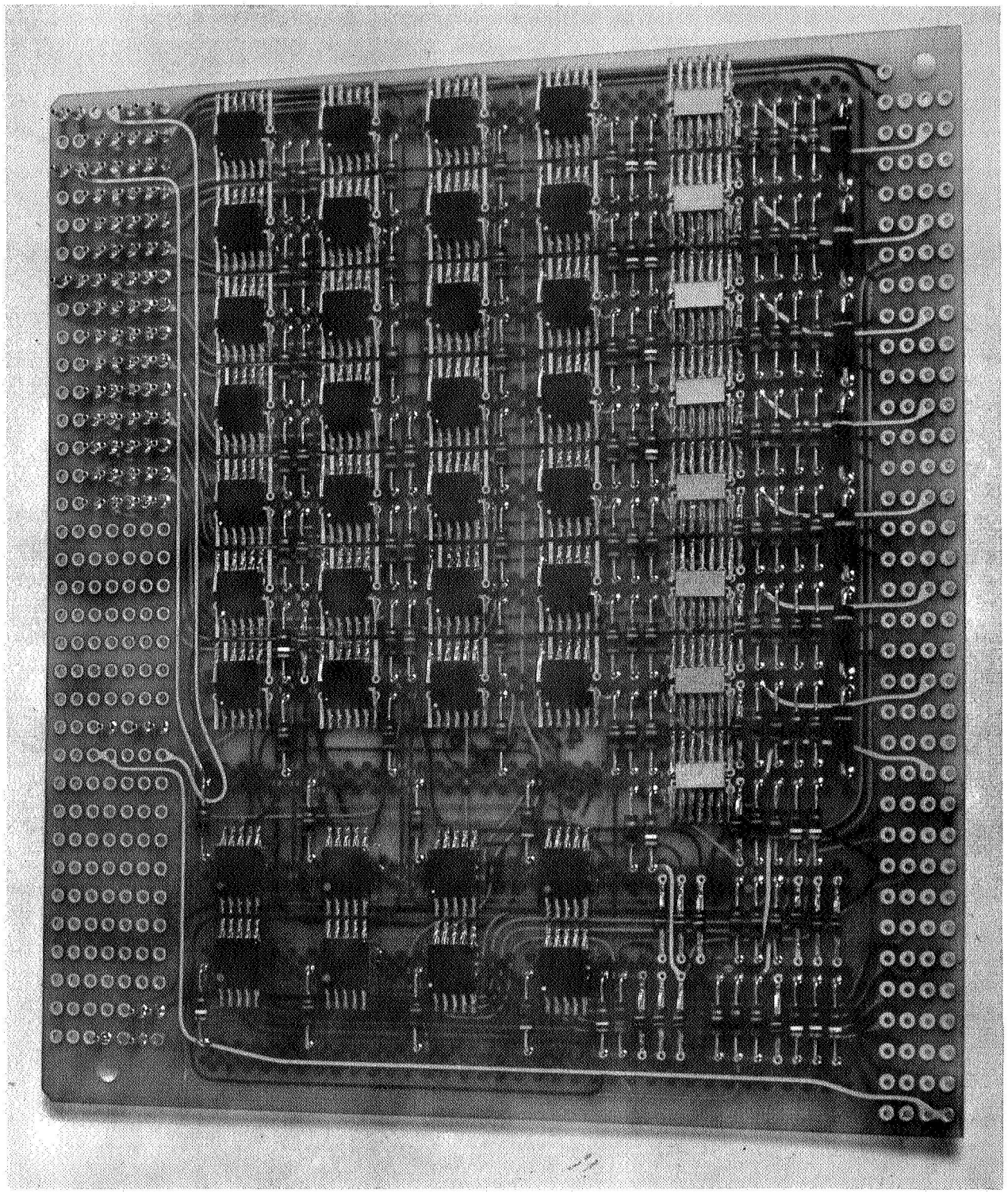
2.2.1.1.2.2. Planar Packaging Technique. The multiplexer, sequencers, and timing circuits are composed of 708 flat-pack integrated circuit devices, 276 microzener and switching diodes, and 1,059 resistors and capacitors. The use of these various components is necessitated by the requirements that any single failure shall cause the loss of no more than eight channels of data. The majority of the resistors and diodes are utilized exclusively for the fault protection function.

The large quantity of components, along with the variety of form factors, required that a low-volume, high-density packaging technique be utilized. It was found that this requirement could be met through the use of a planar packaging technique. The circuits are packaged on 6-layer multilayered, plated-through hole, printed-circuit cards, with integrated circuit, discrete, and microcomponents all mounted on the same cards (figure 16). The capacitors and resistors are mounted parallel to the card, with leads bent at a 90-degree angle and inserted through the plated-through holes for soldering. The microdiodes and integrated circuit packages are mounted flat against the multilayered card. These devices are procured with pretinned flat ribbon leads, which are fluxed and placed on top of their interconnecting circuit lands on the card. Interconnection is then made through the use of a temperature/time cycle controlled resistance soldering technique (figure 17).

A functional breakup of these circuits showed that if analog and digital channels were packaged on the same printed-circuit cards, a minimum number of different card types would be required.

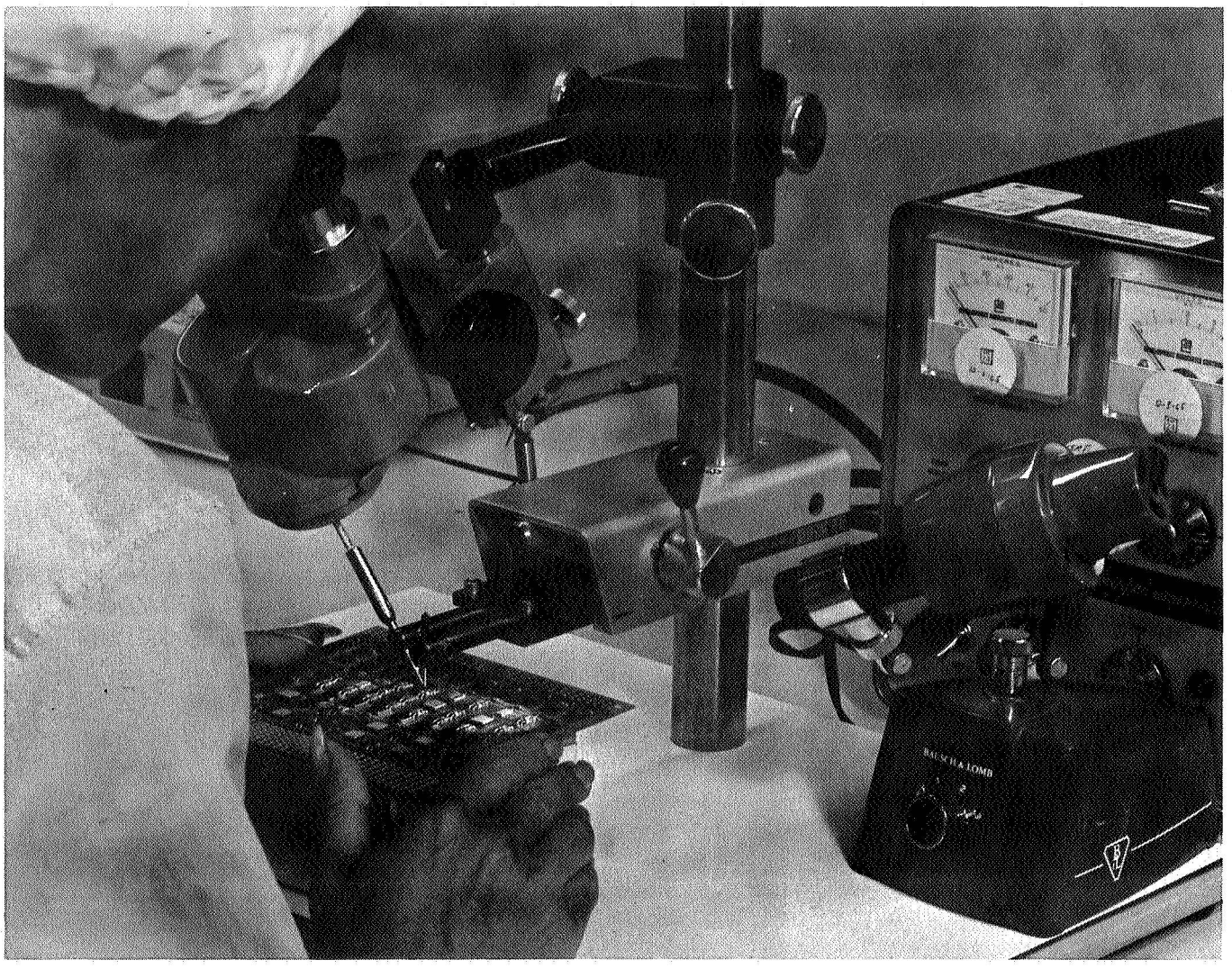
This breakup resulted in the following four types of card assemblies:

a. Prime channel multiplexer card assembly



1210-13

Figure 16. Planar Mounted Multiplexer Card Assembly



56450-6

Figure 17. Resistance Soldering of a Multiplexer Card Assembly

b. Subcommutated channel multiplexer card assemblies

c. Multiplexer timing circuits card assemblies

d. Multiplexer output circuits card assemblies

The prime channel multiplexer card assembly (hereafter referred to as the prime matrix card) contains all of the channel gates for the 21-prime analog and the 63-prime digital channels. The functions on this card are nonredundant, but utilize fail-safe circuit design. Thus, only one prime matrix card per PCM unit is required.

The subcommutated channel multiplexer card assemblies (hereafter referred to as submatrix cards) contain all of the subcommutated analog and digital gates on eight cards. All of these cards are identical except that the top layer is reversed on four of the cards to simplify system assembly and wiring. The circuits on these cards are nonredundant, but utilize fail-safe circuit design to minimize the propagation of any failures that might occur.

The multiplexer timing circuits card assemblies (hereafter referred to as output cards 1A and 1B) contain the timing generator for the row, column and sequencer commands to operate the analog and digital multiplexer, along with circuits to generate timing commands for the sync, ID, and time code words, and the multiplexer readout commands. These cards are identical, with one card required for each PCM unit to provide block redundancy for these functions.

The multiplexer output circuits card assemblies (hereafter referred to as output cards 2A and 2B) contain the multiplexer output circuits and sync word generators, along with the ID, time code, and analog and digital gates. These cards are identical except for differences in two resistors and differences in zener diode values necessitated by the multiplexer timing.

The locations, reference designations, and construction are listed in table 2, and illustrated in figure 15.

2.2.1.1.2.3. Printed-Circuit Cards. Two types of printed-circuit cards are utilized in the system. The cordwood modules have two-sided cards with plated-through holes for mounting and interconnection, while the planar-packaged electronics have six-layer multilayered cards.

To minimize checking and rework time of the multilayered card masters, and to provide a high confidence level for card correctness prior to fabrication, a digital computer was used for checking these cards. Two sets of input sheets were independently originated from the card detail drawings, one by engineering and one by drafting. These were then entered into the computer, and the readouts checked independently against the card wiring diagram. Following this, they were crosschecked against each other. In this manner, total errors (engineering and drafting) were held to 3 out of a total of 10,031 circuit lines, with no mistakes being attributed to errors in pad identity.

All of the printed-circuit cards in the system utilized plated-through holes for interconnection between circuit layers. To comply with NASA specification NPC 200-4, redundant pads and jumper wires are also utilized for layer interconnection on the two-sided cards. Where this was not practical, such as with the multilayered cards, extensive quality

control tests (which exceed the requirements of the NPC standards) are performed on test coupons attached to each card. In addition, photomicrographs are taken of etched cross-sectioned plated-through holes on the coupon and are examined as a part of the inspection process prior to release of the cards to system assembly.

2.2.1.1.2.4. Interconnections. The extreme density of the package (due to its high channel capability and redundancy/fail-safe provisions) required that a minimum volume, high capacity system be utilized for card interconnections.

In reviewing this requirement, it was determined that sufficient wiring pads were available to hard-wire the module cards together, since only 32 wires interconnected them, with an additional 23 wires from these two cards going to the external connectors. Since these two cards (which contained the power supply, programmer, A/D converter, and output register/split-phase converter modules) were connected directly to output cards 1 and 2 (which required a total of only 31 additional pads on both boards), it was decided that these would also be hard-wired together. This utilized 116 of the total 210 pads available on each of the module cards. Since the output type 1 and 2 cards had no wires going to an external connector, only 46 wires interconnected what thus became a four card group to the external connectors.

The wiring of the multiplexer was a different situation altogether. Due to the functional circuit breakup, number of channels per card assembly, quantity of timing signals required, and similarity of card layouts, over 460 pads would be required for most of the cards to provide the necessary intraconnections within the multiplexer, notwithstanding the 798 pads required for the input signals. To alleviate this situation, a unique interconnection technique was utilized (figure 18).

Interconnections among the multiplexer cards are effected through the use of miniature spring sockets, manufactured by AMP, Incorporated. These sockets are placed into the holes in the printed-circuit cards and soldered onto their pads. The pads are oriented so that any interconnection from a pad on one card is directly in line with pads on other cards which must also be connected to this line. Solid bus wires are inserted through these sockets effecting electrical contact to all cards where required. On cards where connection is not required, a nylon insulator is bonded in that hole, and the wire passes through this insulator without making contact with that card.

This technique has many advantages. It eliminates the need for bused pads to connect wires which provide several boards with the same signal. (It reduced the requirement for 460 intraconnection pads per card to a maximum of 210.) It allows 0.085-inch diameter pads to be spaced on 0.100 by 0.150-inch centers. It allows closer spacing of card assemblies, since no additional space is required for any wiring harness. It provides the capability of minimizing crosstalk and noise problems on sensitive signal lines by separating them from power and other noise generating wires (sometimes difficult to do with hard-wiring). Other advantages include savings in card layout time, simplified interconnection wire lists, elimination of potential damage to the printed-circuit cards from soldering and unsoldering of wires, and ease of system assembly and disassembly. The utilization of this interconnect method can be seen in figure 19, which shows the PCM unit prior to mechanical assembly.

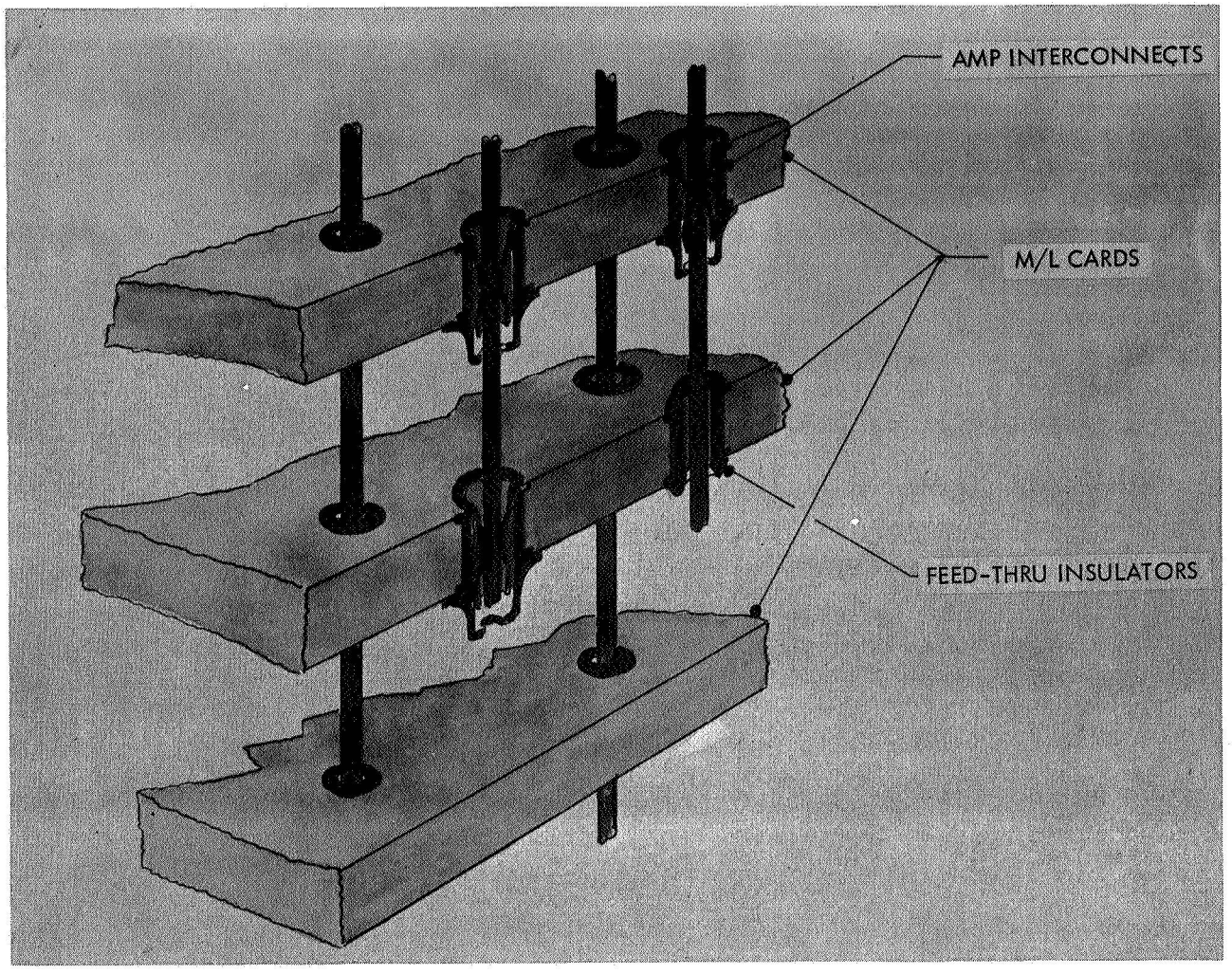
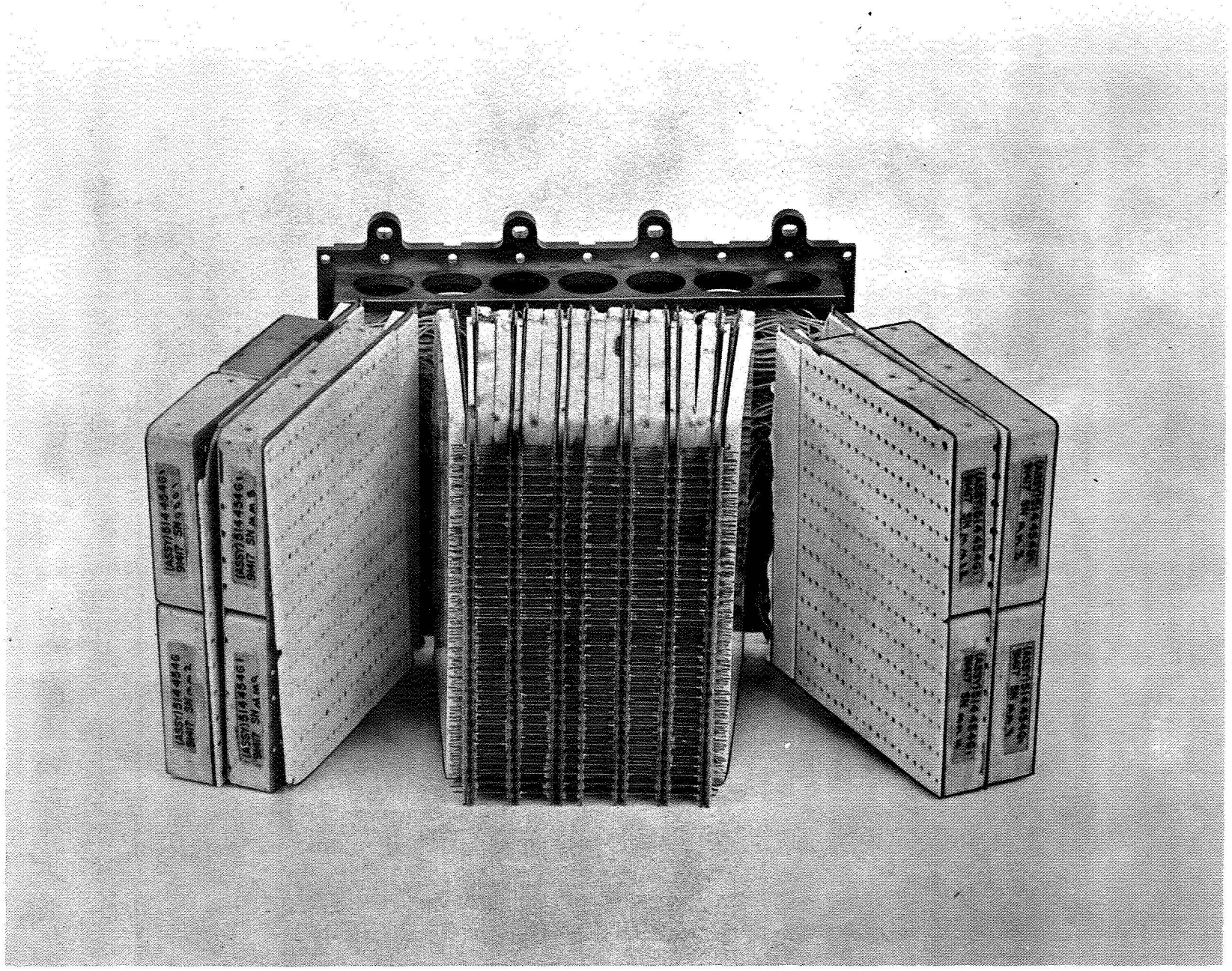


Figure 18. Bus Wire Interconnection Technique



1858-15

Figure 19. Wired PCM Unit (Before Mechanical Assembly)

2.2.1.1.2.5. System Assembly and Test. The card assemblies are wired as functional groups with each group having independent connectors. This type of wiring is possible because of bus wire interconnections in the multiplexer and because the prime and submatrix card assemblies require direct connections only to their transducer inputs (figure 20). All other inputs and outputs must pass through the modular-packaged discrete component portion of the system. Thus, except for the transducer inputs, all inputs are brought into the system through the module card assemblies, from which they are transferred to the output type 1 and 2 cards via point-to-point hard-wiring. From these cards, the signals are routed to the multiplexer card assemblies via the rigid wire interconnect system. The data is multiplexed and routed through rigid wires to the output circuit and module card assemblies where it is converted, properly sequenced, and applied to the output register/split-phase converter before transmission to the ground. Power is routed from the power supply module in a similar manner.

This interconnection scheme allows the card assemblies to be wired as shown in table 3.

Table 3. PCM Unit Interconnection Scheme

Reference Design	Card Assembly Group No.	No. of Connectors/ Card Assembly Group	Cards in Group
1A1	SA-1	1	Power Supply, A/D Converter
1A2	SA-1	1	Programmer, Output Register/ Split-Phase Converter
1A3	SA-1	1	Output Board 1A
1A4	SA-2	3	Submatrix Board A1
1A5	SA-2	3	Submatrix Board B1
1A7	SA-3	3	Submatrix Board A2
1A8	SA-3	3	Submatrix Board B2
1A9	SA-4	1	Prime Matrix Board
1A10	SA-5	3	Submatrix Board A3
1A11	SA-5	3	Submatrix Board B3
1A12	SA-6	3	Submatrix Board A4
1A13	SA-6	3	Submatrix Board B4
1A14	SA-7	1	Output Board 11A

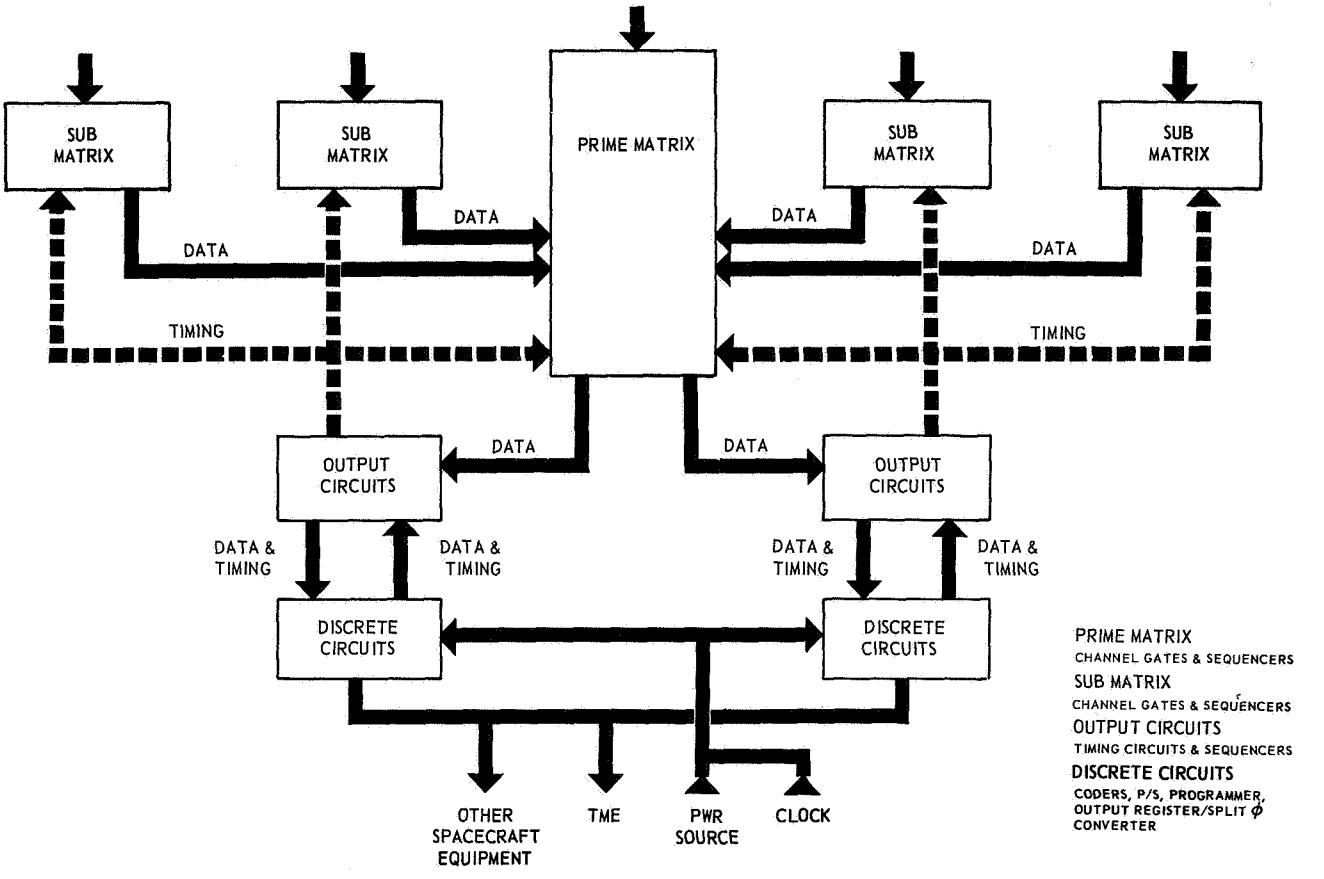


Figure 20. Nimbus PCM Telemetry Unit Functional/Packaging Block Diagram

Table 3. PCM Unit Interconnection Scheme (Continued)

Reference Design	Card Assembly Group No.	No. of Connectors/ Card Assembly Group	Cards in Group
1A15	SA-7	1	Output Board 11B
1A16	SA-7	1	Programmer, Output Register/Split-Phase Converter
1A17	SA-7	1	Power Supply, A/D Converter

Each group of card assemblies is wired to their appropriate connectors in special fixtures (figure 21). The fixtures are designed so that card assemblies and connectors are located relative to each other in the unit, thereby eliminating excessive wire loops and unnecessary strain on the wires and solder joints.

The system is then assembled in its electrical test fixture for preliminary checkout. The card groups, with their respective connector panels, are removed and secured in the system test fixture (figure 22). Electrical contacts connected to jumper wires are then inserted into the AMP sockets to effect electrical interconnection to the cards of the multiplexer. The front panel connectors are mated to cables from the test set, which simulates the spacecraft electrical interfaces.

The complete PCM unit consists of one prime matrix card assembly (nonredundant), four submatrix A and B card assemblies (identical but nonredundant), two output type 1 card assemblies (redundant), two output type 2 card assemblies (essentially identical), two programmer-power supply card assemblies (redundant), and two A/D converter-output register/split-phase converter card assemblies. (Refer to table 3.)

The system is tested by stringing the card assemblies in a holding fixture in a spread-out configuration (figure 23). Following successful completion of testing in this configuration, the system is compressed down to its ultimate operating configuration, placed in the internal support structure, and tested again. Upon successful completion of this testing, the proper preload is applied to the electronics, which is then loaded in the housing and forwarded to formal Acceptance Testing.

2.2.1.1.2.6. Maintainability and Repairability. The system is repairable to the individual component or integrated circuit. Two levels of maintenance have been considered for the system; maintenance at field and at depot repair levels. Troubleshooting may not be practical under certain conditions; therefore, the housing is designed to be easily removed and replaced in the spacecraft without special tools or equipment.

At the repair depot, the electronics can easily be removed from the housing through use of a hydraulic press. Standard repair procedures are used for removal and replacement of the foamed modules from their card assemblies, and removal of the potting foam and components from the defective module. Component replacement on the planar packaged card

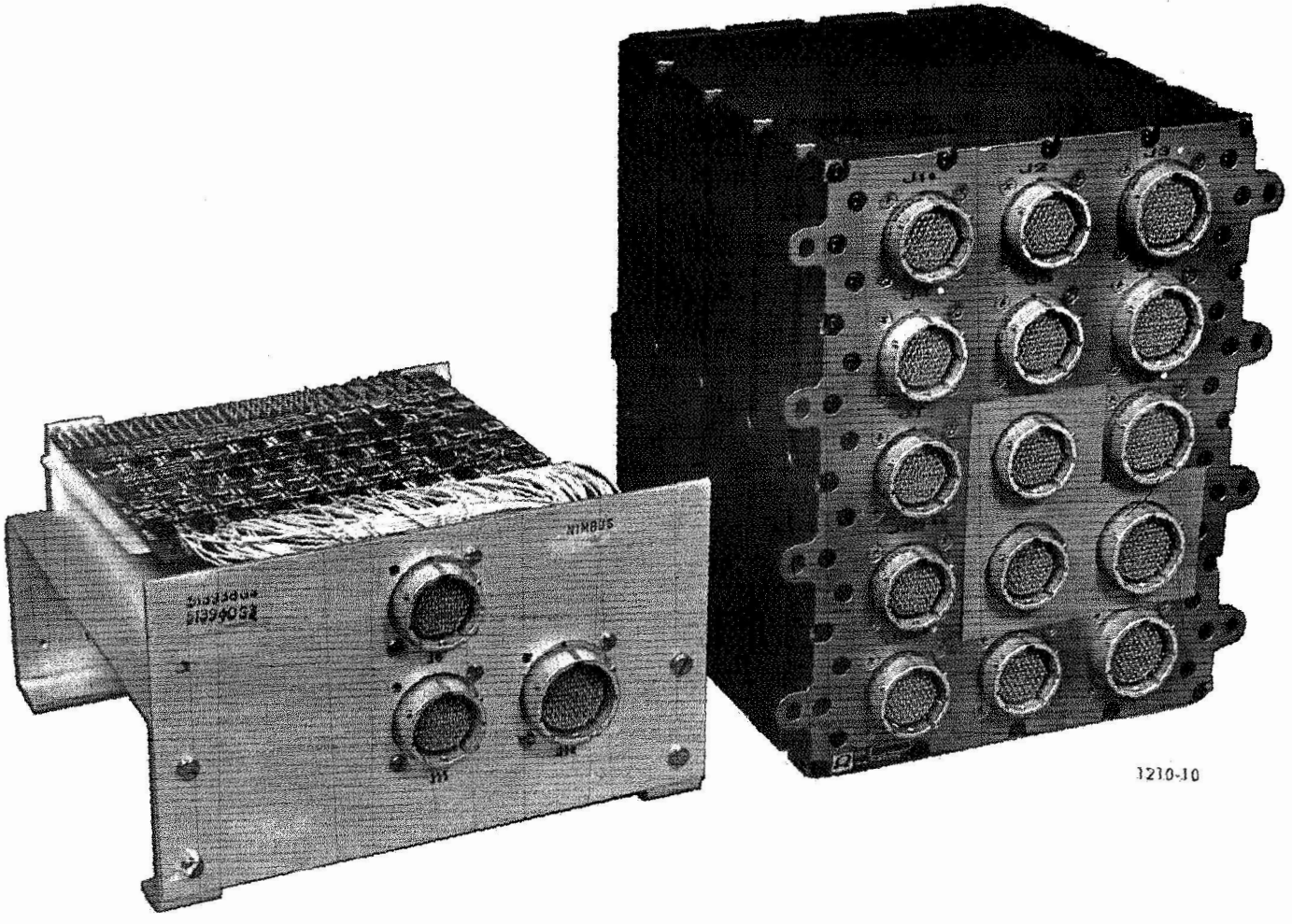


Figure 21. Functional Assembly in Wiring Fixture and Location in PCM Unit

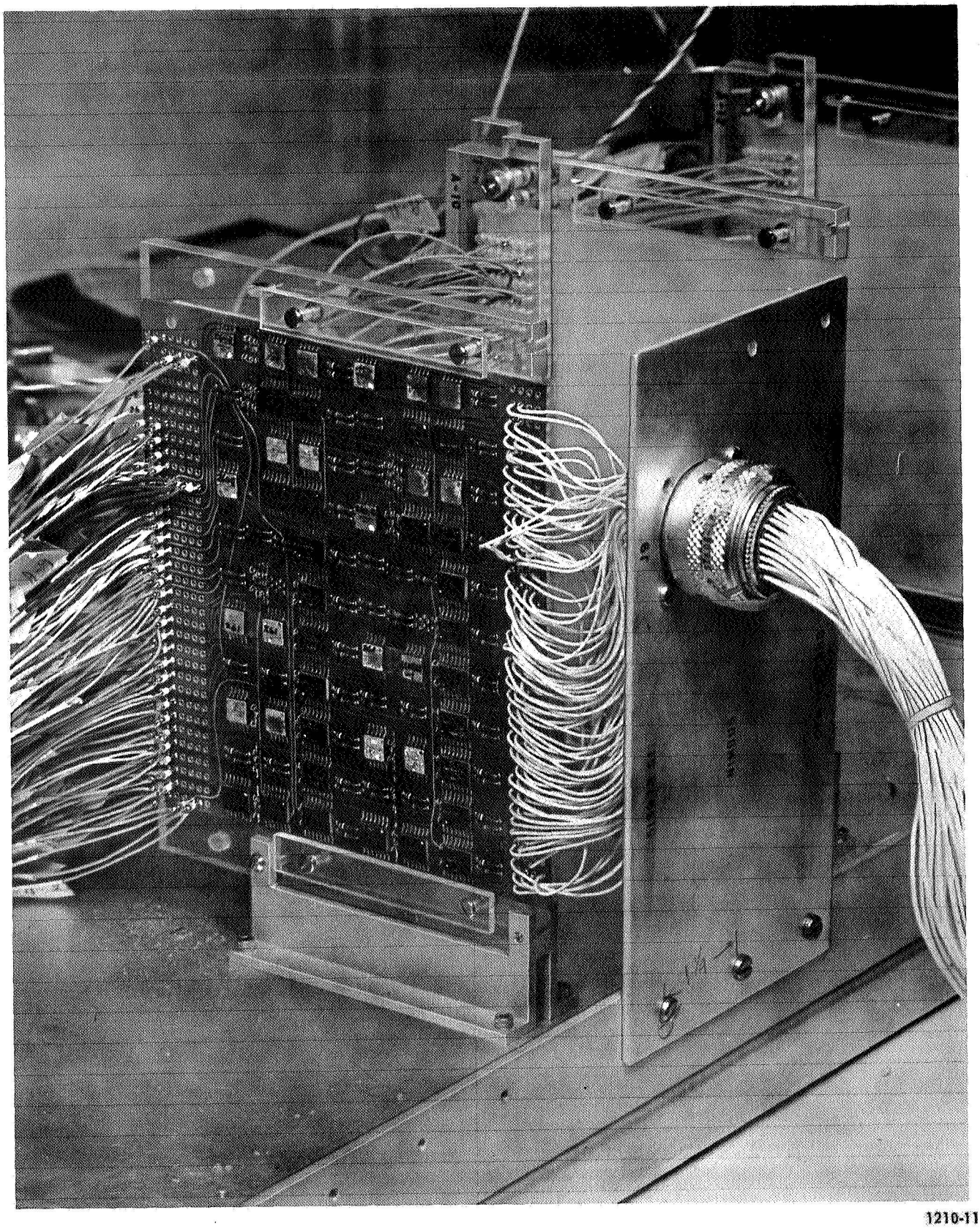
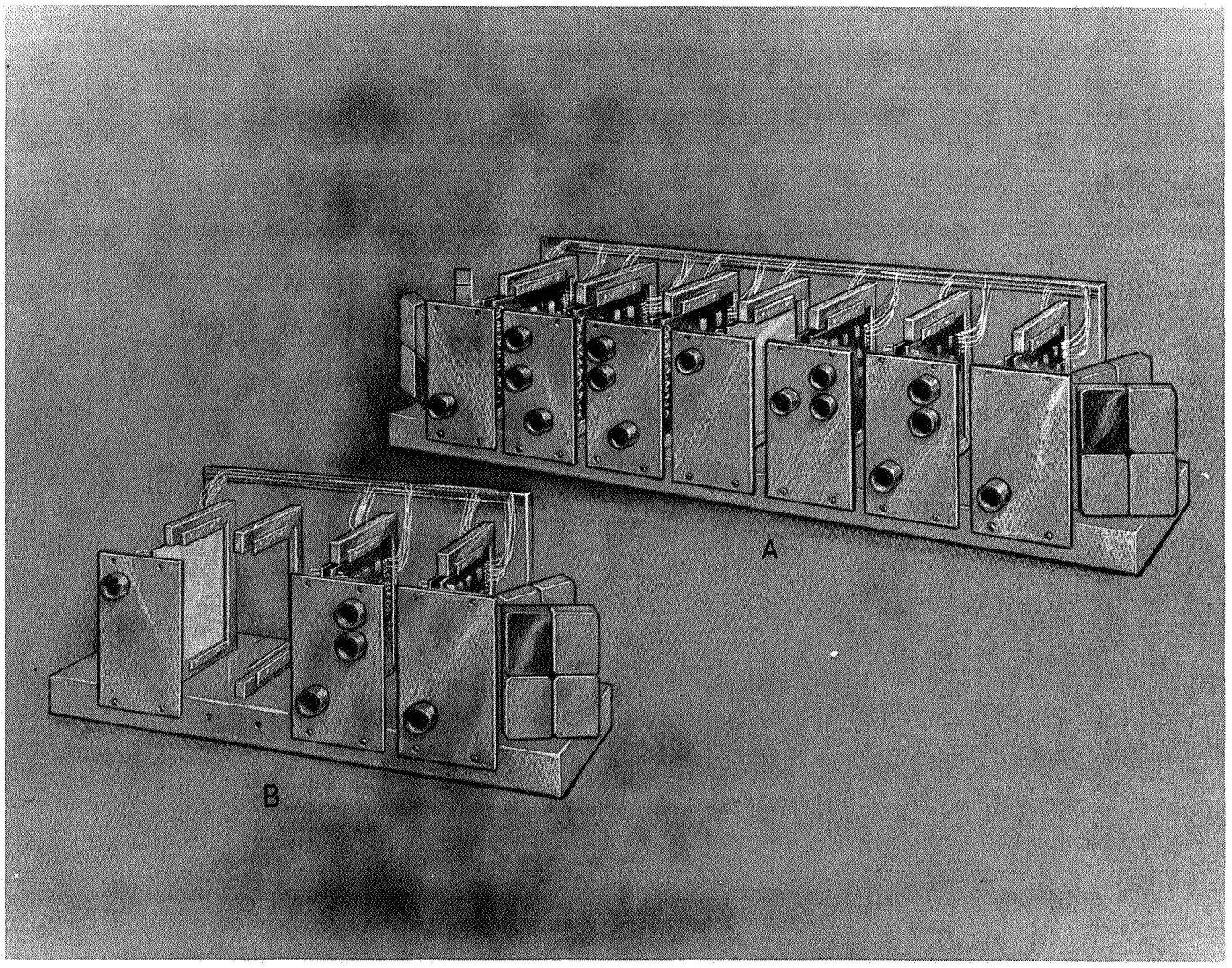


Figure 22. Prime Matrix Card Installed in Systems Test Fixture



56450-17

Figure 23. System Test Fixtures

assemblies can be effected by removing the malfunctioning card group from the system. This is accomplished by removing the bus wires from the multiplexer card stack and by removing the associated connector(s) from the front panel. Repair at the card level is accomplished by removing the foam shim from the card, unsoldering the defective component, and soldering the replacement component onto the card.

2.2.1.2. ELECTRICAL CHARACTERISTICS. Table 4 contains a listing and summation of the primary electrical characteristics of the PCM unit.

Table 4. PCM Electrical Characteristics

Function	Characteristics/Parameter
Power Consumption	1.6 watts nominal
Digital Input ZERO	0 volt to -1 volt
Digital Input ONE	-5 volts to -10 volts
Analog Transducer Input Voltage Range	0 to -6.4 volts dc full scale
Bit Rate	500 cps
Sync Words	Words one, two and 62.5 in every subframe
DC Voltage Input	-24.5 volts ±2% (Survive to -35V one orbit)
Overload Range (Analog and Digital)	Survive +0.5 volt dc to -24.5 volts dc
Output Modulation Type	Split-phase, mark 0
Analog Source Impedance	3.3K ohms for ±0.4% accuracy
Analog Input Impedance	
Operating	One megohm during sample, >10 megohms with channel off
Nonoperating	>10 megohms
Prime Sample Rate	1 sample per second
Subcommutated Sample Rate	Once every 16 seconds

Table 4. PCM Electrical Characteristics (Continued)

Function	Characteristics/Parameter
Digital Input Impedance	
Operating	500K ohms during sample, >10 megohms with channel off
Nonoperating	>10 megohms
Analog Sample Aperture Time	170 ±30 microseconds
Channel Allotment	
21 Prime Analog 63 Prime Digital 434 Subcom Analog 280 Subcom Digital 1 Time Code	

2.2.2. FUNCTIONAL BLOCK DIAGRAM DISCUSSION

2.2.2.1. GENERAL. The functional description of the PCM unit is initially discussed on a system level and then followed by general subsystem descriptions. The overall system discussion describes PCM unit operating principles with reference to the detailed block diagram illustrated in figure 24. Subsystem descriptions are oriented to the following subsystems contained in the PCM unit:

a. Programmer

b. Multiplexer

c. Analog-to-digital converter (coder)

d. Output shift register and split-phase converter

e. Power supply

2.2.2.2. OVERALL PCM UNIT OPERATING PRINCIPLES. The PCM unit, illustrated in block diagram, figure 24, performs four distinct functions:

a. Accepts all data inputs

b. Formats all digital inputs into 7-bit data words, where each bit represents a different item of information

c. Converts all analog transducer inputs to an equivalent binary code and formats the converted analog inputs into 7-bit data words

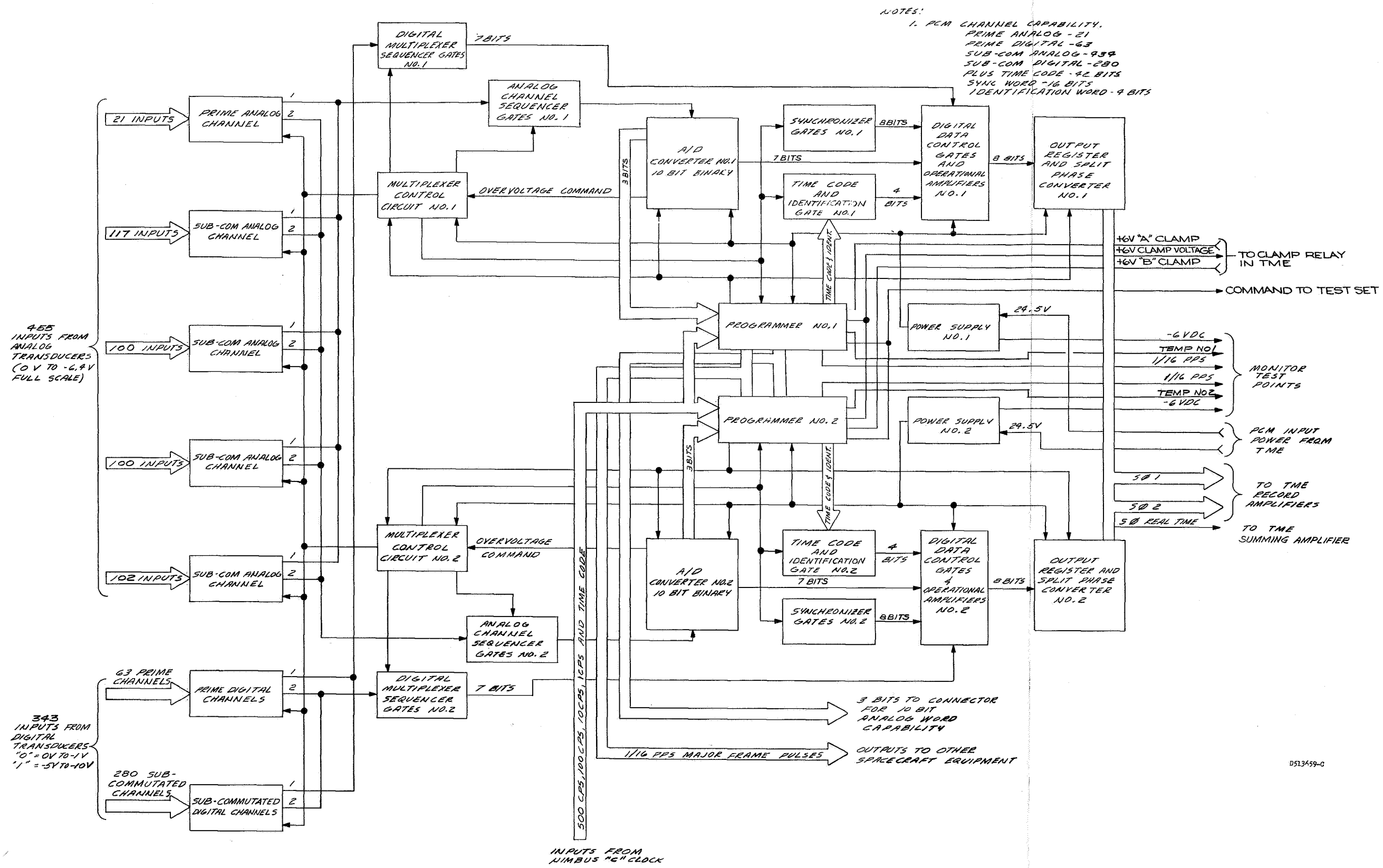


Figure 24. PCM Unit Detailed Block Diagram

d. Formats data words, time code, and sync words into split-phase, Mark 0, serial outputs to the TME

Data inputs to the PCM unit constitute 455 analog, and 343 digital signals sampled in the Nimbus B spacecraft. The measurands, analog and digital, are applied through their respective nonredundant multiplexers into dual-redundant analog or digital sequencer gates. Analog sequence outputs are applied to their respective analog-to-digital converters where all analog data words are coded to an accuracy of 10-binary bits. After conversion, three LSB's of every word are discarded, resulting in the 7-bit data word. One sync bit is added to every output word to aid ground stations in the decommutating process; thus, every output word contains eight binary digits. Under certain conditions it is possible to retain up to 10 bits of the coded analog word, however, up to three data bits of the following digital word will be lost. All digital and analog inputs are handled in the same manner after the analog inputs are coded. After coding, the digital sequencers are applied to the digital data control gates for final formatting. Format timing and time-code and sync information insertion is controlled by two programmers. The data control gates accept the digital inputs, Nimbus C time codes, and sync information and inject it into preassigned words at the proper place. (Detailed descriptions of the complete format and relative time and sync code positions within the 16 subframes are provided in the PCM Unit Instruction Manual.)

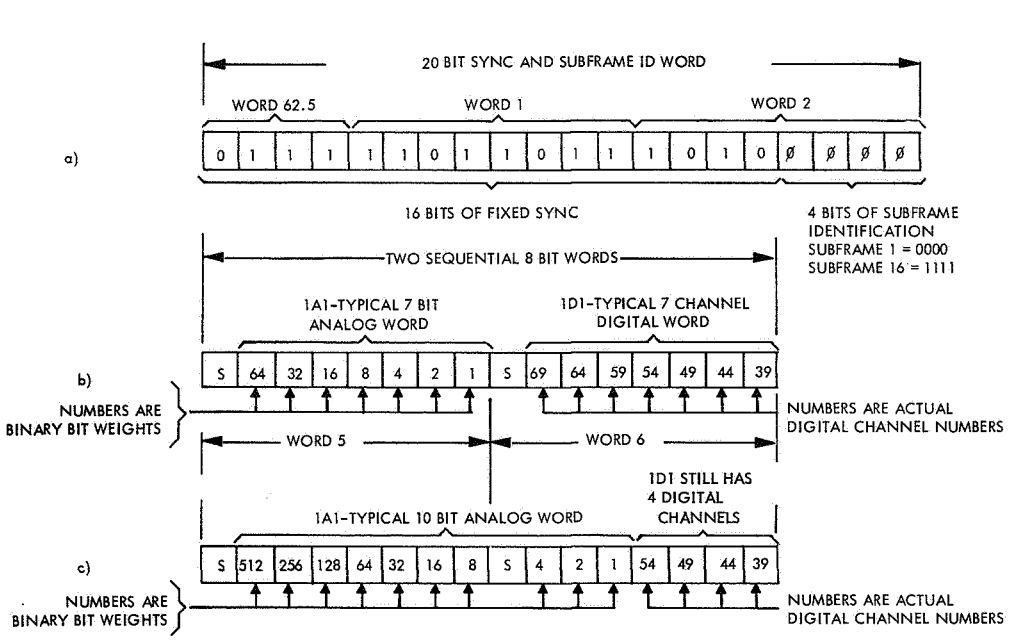
Sync information is an internally generated 16-bit subframe sync code and 4-bit subframe identification (SFID) code. This sync information together with Nimbus clock time code information is inserted into unique locations within the data format. Data format is contained in a major frame of 16-second duration. Each major frame is composed of 16 subframes (1 subframe per second) containing 62.5 eight-bit words (7 data bits and 1 sync bit) each. Figure 25 depicts the arrangement of sync and subframe ID words and the bit arrangement of analog, digital, and time-code words.

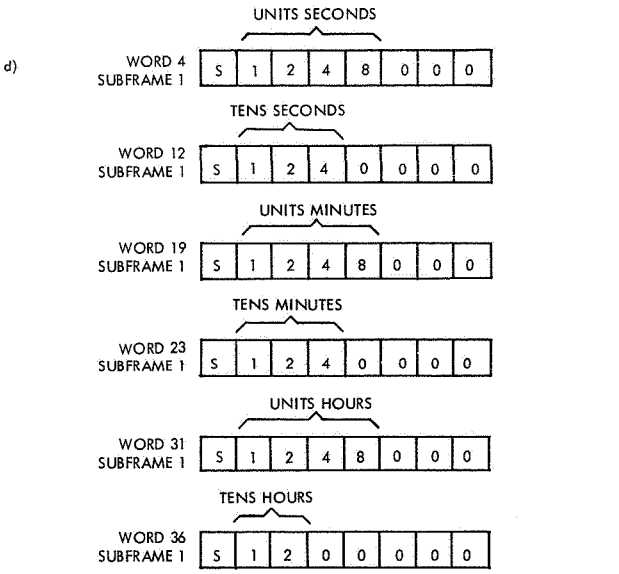
Part "a" of figure 25 shows the 20-bit combined sync and subframe ID word contained in words 62.5, 1, and 2 of two consecutive subframes. The 16 bits of fixed sync are preprogrammed and remain constant to obtain data synchronization through pattern recognition 16 times each major frame. The four-bit SFID pattern is a continuously changing binary code that ensures synchronization and provides identification through a unique pattern generated for each of the 16 subframes contained in a major frame.

Part "b" shows the bit arrangement of typical 8-bit analog and digital words. Analog words are converted to binarily-weighted 7-bit words containing 1 sync bit as shown in the figure. Digital words contain seven bits of digital data plus the 1 sync bit.

Part "c" depicts the bit arrangement of a typical 10-bit analog word. Analog signals are coded to 10-bit words, but three bits are dropped after coding. However, the three bits dropped can be reinserted into the data for higher resolution under certain circumstances. Time codes are shown in part "d" of the illustration with their relative position in subframe No. 1.

The formatted data output of the digital data control gates is amplified and applied to dual redundant output registers and split-phase converters. The output register is a parallel-to-serial converter that accepts 8-parallel read-in data bits from the data control circuits and





NOTES:
1) ALL 6 TIME CODE WORDS OCCUR IN SUB-FRAME NO. 1
2) UNITS OF SECONDS, MINUTES AND HOURS REQUIRE 4 BITS, TENS OF SECONDS AND MINUTES REQUIRE 3 BITS AND TENS OF HOURS REQUIRE 2 BITS.
3) LAST 3 BITS IN ALL 6 WORDS ARE ZEROES
4) ACTUAL TYPE OF CODE IS BCD
5) MAXIMUM TIME CODE COUNT IS 24 HOURS WITH THE READOUT OCCURRING ONCE EVERY 16 SECONDS.

55882A

Figure 25. PCM Output Word Diagrams

serially shifts the data out as an NRZ code at a 500 cps bit rate to the split-phase converter. The NRZ is then converted to split-phase Mark 0 code and applied to the TME unit for real-time transmission, or to two RME tape recorders for storage and later transmission.

2.2.2.3 PROGRAMMER GENERAL DESCRIPTION. The PCM unit contains two block-redundant programmers and only one programmer operates at a time. Each programmer comprises three functional modules designated No. 1, 2, and 3. The electrical interfaces shown in figure 26 and described in the following paragraphs are applicable to either programmer, although some functions performed are normally not considered to be a part of the programmer. A simplified logic diagram of the programmer is shown in figure 27. The major circuits in module No. 1 are:

a. 8:1 Bit counter

b. Multiplexer timing circuits

c. 15-microsecond strobe command generator

d. Coder command circuits

The major circuits in module No. 2 are:

a. Time-code gating and storage circuits

b. 1/16-pps pulse generator

c. 1-cps reset circuit

Module Nos. 2 and 3 contain monitoring circuits. In addition, module No. 3 contains the circuits listed below:

a. Multiplexer clamp circuit

b. Bench test equipment command circuit

c. Subframe ID buffers

d. Coder 3-bit buffer storage

The programmer does not contain an internal clock, but relies on the Nimbus C clock for proper operation. The 500-cps bit rate from the Nimbus C clock is applied to the 8:1 bit, 62.5:1 word, and 16:1 subframe counters that generate all PCM system timing commands. The 1-cps clock input synchronizes the programmer with the Nimbus C clock so time codes can be placed properly in subframe 1 of the output format. The programmer also generates five major frame pulses that are 250 microseconds wide and occur once every 16 seconds in phase with bit 1, word 1, and subframe 1, referred to the input.

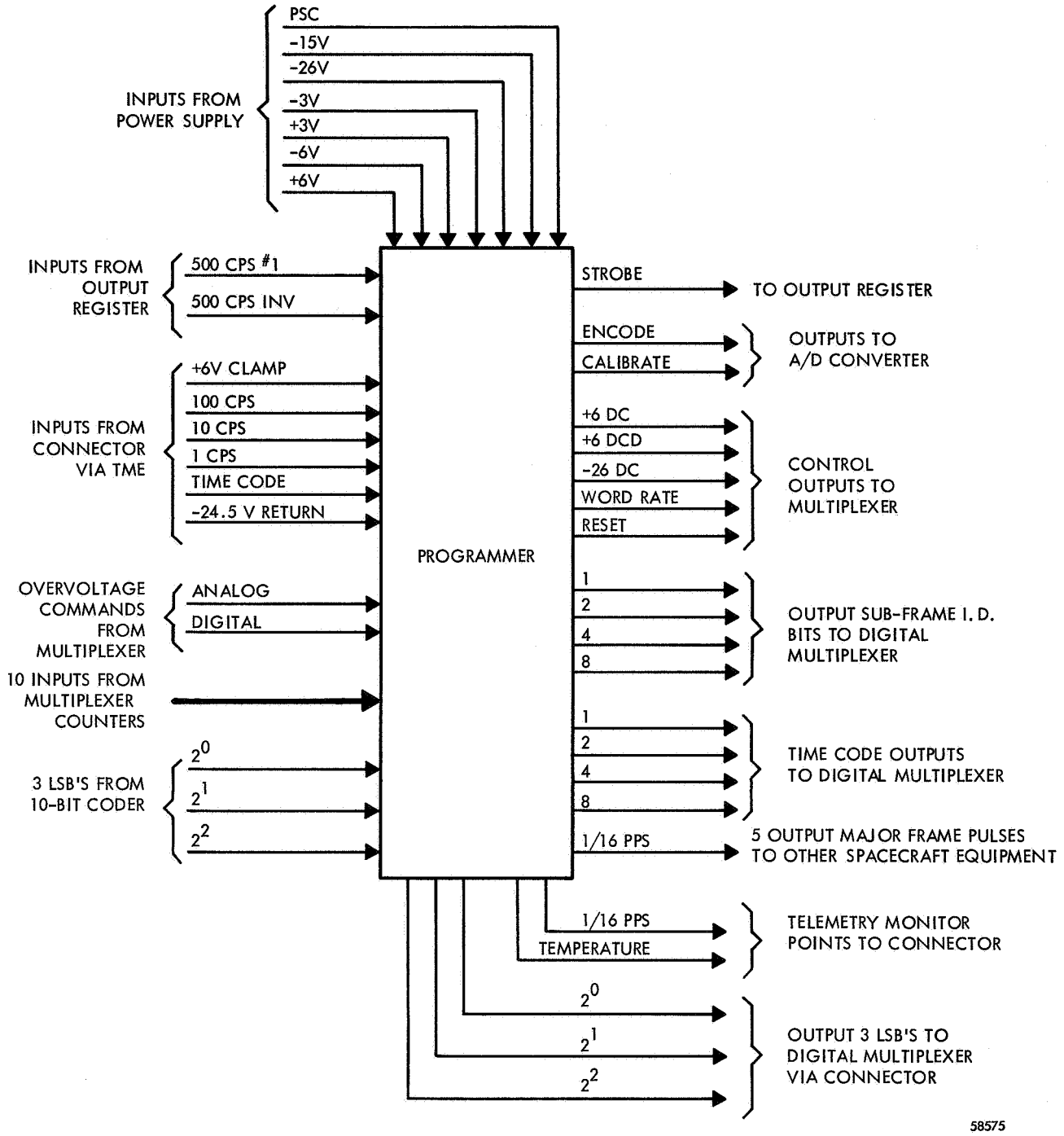


Figure 26. Programmer Interface Diagram

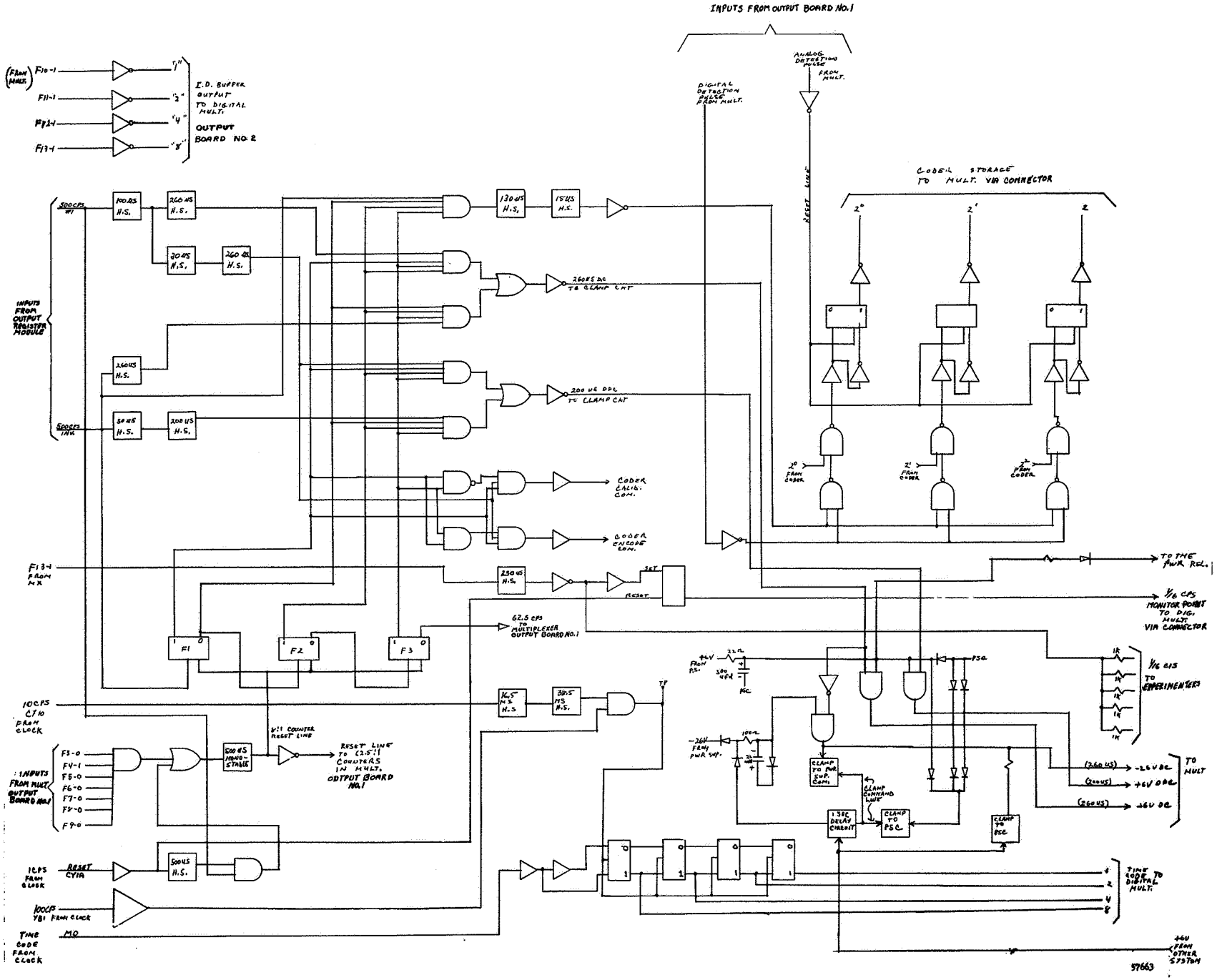


Figure 27. Programmer Simplified Logic Diagram

2.2.2.4 MULTIPLEXER GENERAL DESCRIPTION. The multiplexer accepts analog and digital inputs from other satellite equipment, and using two coders, processes the inputs into 8-bit parallel words that are supplied to the output shift registers. The multiplexer handles 21 prime analog inputs, 434 subcommutated analog inputs, 63 prime digital inputs, 280 subcommutated digital inputs, a time code, a sync word and an ID count. Analog inputs have a voltage from 0 to -6.4 volts. Digital inputs are: binary zero = 0 to -1 volt, binary one = -5 to -10 volts. Unlike other components of the PCM system, the multiplexer input gates are not block redundant; however, the sequencers, timing, and output circuits are.

Functionally, the multiplexer consists of a prime matrix, a prime analog multiplexer, a prime digital multiplexer, a subcommutation (subcom) matrix, a subcom analog multiplexer, a subcom digital multiplexer, two output circuits and two timing circuits as shown in figure 28. Since the prime analog, prime digital, subcom analog and subcom digital multiplexers are nonredundant, these elements are active regardless whether PCM 1 or 2 is being used. However, timing circuits and output circuits are block redundant and active only when a corresponding PCM is selected. If PCM 1 is selected, the multiplexer receives timing from the "A" timing circuits. The analog portion of the multiplexer supplies outputs to coder No. 1 and this unit, in turn, supplies digital outputs to the A output circuits. Similarly, if PCM 2 is selected, the "B" timing circuits, coder No. 2, and the B output circuits are used with the multiplexer.

For an example of multiplexer operation, assume that PCM 1 is being used. Further, assume that a prime analog input is to be sampled. For these conditions, the A timing circuits supply the prime matrix with row and column commands that activate a prime analog multiplexer gate for 200 microseconds. In coincidence, a series multiplexer gate is activated by a sequencer command and coder No. 1 is activated by an encode command. As a result, the prime analog input is passed by the prime analog multiplexer and is stored in coder No. 1. During the interval that follows coder No. 1 converts the prime analog into its equivalent binary value and supplies the resulting binary word to the A output circuits. If prime analog input was not an overvoltage (-6.4 volts or greater), coder No. 1 enables the A timing circuits to provide an analog detection pulse (ADP). This pulse causes the A output circuits to gate the binary word from coder No. 1 to output shift register No. 1. If, however, the prime analog input was -6.4 volts or greater, coder No. 1 supplies the A timing circuits with an overvoltage signal. This signal causes the timing circuits to generate a digital detection pulse (DDP) that is supplied to the A output circuits. As a result of this input, the output circuits ignore the coder input, and strobe the prime digital multiplexer output. Since the digital multiplexer was not active for the prime analog input this condition results in the gating of all ones (full-scale indication) to the output shift register No. 1.

Similar operations are performed on subcommutated analog inputs. However, a subcom matrix is used and three multiplexer gates are used in series between the analog input and the coder instead of the two used for prime analog inputs. Digital inputs are processed somewhat differently since the inputs do not have to be encoded. Processing of digital inputs is similar to that for analog overvoltage. For every digital input word (7 bits) there is an analog input gate connected to -15 volts (overvoltage). The analog gates and the digital multiplexer gates have a common matrix. Thus, when a digital or analog input is multiplexed, both the analog and digital gates are strobed. As a result an analog multiplexer gate supplies the overvoltage input to a coder. The coder, in turn, converts the overvoltage to its binary

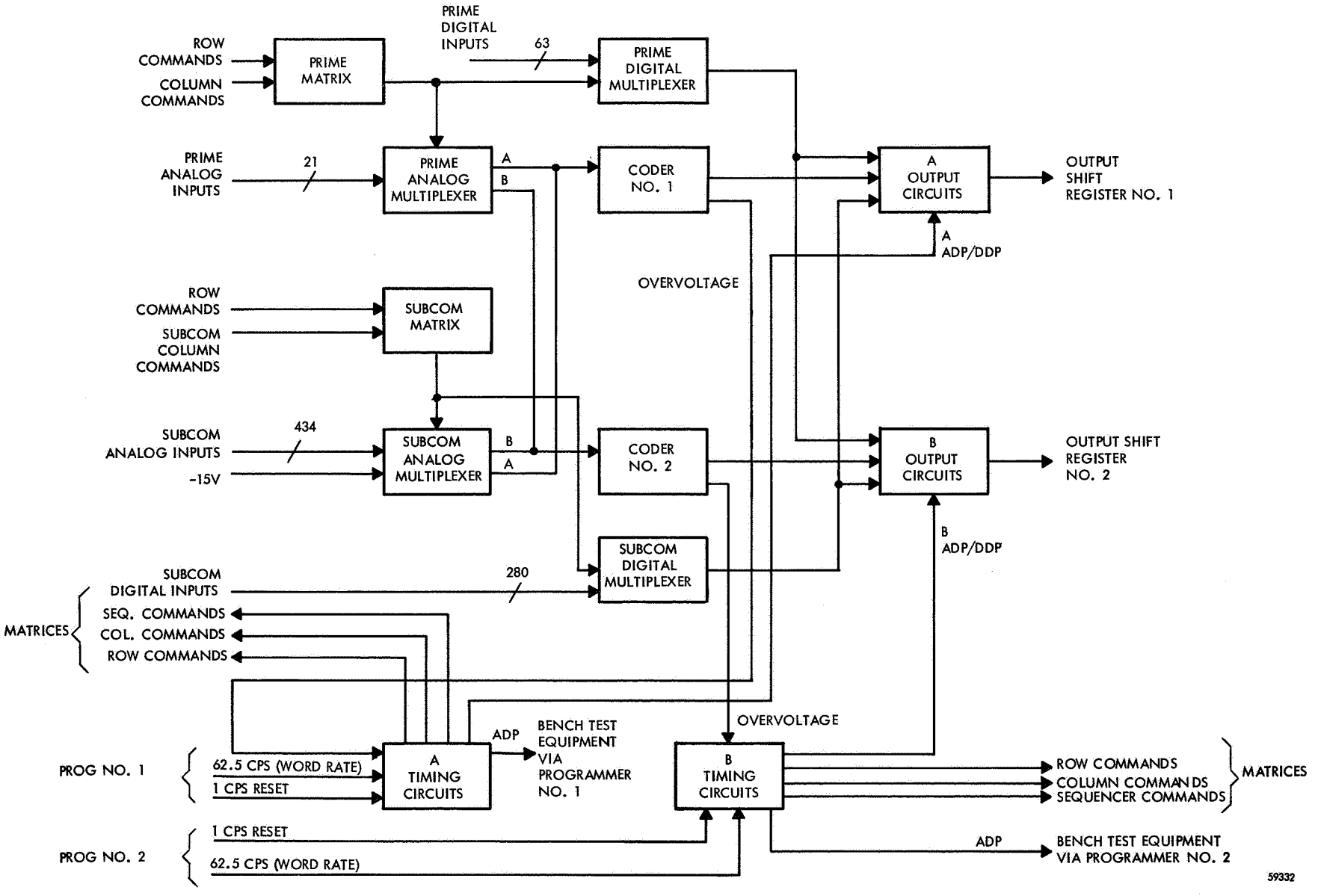


Figure 28. Multiplexer Simplified Block Diagram

equivalent (full count of 1023) and supplies an overvoltage signal to the active timing circuits. This signal causes the timing circuits to provide a DDP output to the active output circuits. As a result of this input, the active output circuits strobe the digital multiplexer output. Since a digital multiplexer gate was activated by the common matrix, the digital input is gated to the output shift register. This method of processing digital inputs permits maximum flexibility for interchanging digital and analog inputs. For example, digital inputs can be changed to analog inputs by removing the interconnection between the digital multiplexer gates and the common matrix and connecting the analog multiplexer gate input to the analog source instead of -15 volts. Similarly, analog sampling for a given channel can be changed to digital sampling by connecting the analog multiplexer gate to -15 volts and interconnecting a digital multiplexer gate to the common matrix.

2.2.2.5. ANALOG-TO-DIGITAL CONVERTER (CODER) GENERAL DESCRIPTION. The coder is a precision, ramp-type coder that converts analog inputs, having a range from 0 to -6.4 volts full scale, into 10-bit binary words. The coder provides a resolution of 1 part in 1024, however only seven bits (1 part in 128) are hardwired to the digital multiplexer. The other three bits can be individually selected to provide 8-bit resolution (1 part in 256) 9-bit resolution (1 part in 512) or 10-bit resolution (1 part in 1024). However, digital channel usage is reduced whenever a resolution of greater than seven bits is selected because the additional bits must occupy bit positions of words normally used for digital channels. Thus, with this requirement, increased resolution for analog channels is possible only when the analog channel word immediately precedes a digital channel word.

The coder, upon command by the programmer, accepts an analog input from the Pulse Amplitude Modulation (PAM) bus and stores the analog input in a capacitor store circuit. The operation is commonly called a sample and hold operation. The capacitor is then discharged at a controlled linear rate. A level detector, connected to the capacitor circuit, monitors the charge remaining on the capacitor, and until this charge decreases to zero volts, a 500-kc oscillator steps a 10-stage binary counter. Thus, the count recorded in the counter is representative of the analog input within the limits of resolution. However, there is one exception to this basic operation. Since a full-scale analog voltage (-6.4 volts) is the equivalent of a full count (1023), a voltage greater than full scale would cause the counter to recycle and provide an erroneous count. To prevent this from occuring for overvoltage inputs, counter stepping is inhibited and the charge remaining on the storage capacitor is ignored whenever a full count is reached. The coding of analog inputs from the PAM bus is termed an encode cycle. The coder performs an encode cycle for each analog sample in the PCM format. To compensate for temperature changes and circuit aging, the coder also performs calibrate cycles. In these cycles, a precision voltage, representing a full-scale input, is encoded. If the resulting count is less than or greater than that of a full scale voltage, a compensating circuit adjusts the encoding circuits accordingly. Three calibrate cycles are performed for each encode cycle to ensure precision operation under various operating conditions.

When digital inputs are sampled, the PAM bus is switched to -15 volts i.e., for every digital word there is a multiplexer gate whose input is connected to -15 volts. Thus, the coder is forced to code an overvoltage. As a result, the coder records a full count and supplies an overvoltage command to the final sequencers that causes readout from the digital multiplexer rather than from the coder. The overvoltage command not only controls multiplexer

readout, but is also supplied to output boards Nos. 1A and B to generate an output that controls the BTE for the automatic, all-channel test mode. This output also controls the coder 3 LSB storage register located in programmer module 1 and 2.

A simplified block diagram of the analog coder is presented in figure 29. For an example of coder operation, assume that an encode cycle is to be performed. For the encode cycle, the programmer supplies the coder with an encode command. This command initiates three operations for sampling an analog input, (1) sets the code/calibrate control flip-flop, (2) it closes the MOS gate for connecting the PAM input to the buffer amplifier and, (3) triggers the 170-microsecond monostable multivibrator via the sample initiate gate. The coder/calibrate control flip-flop, in turn, disables the calibration (+) and calibration (-) gates to prevent calibration correction during the encode cycle. In addition, the flip-flop causes the code/calibrate gate to supply an enable level to the bit counter gate.

When triggered by the encode command, the 40-microsecond half shot resets the 10-stage binary counter that stores the binary equivalent of the analog input, and the 170-microsecond monostable initiates the final control function for the sample and hold operation. For this control function, the 170-microsecond output is applied (in normal and inverted form) to the start/stop flip-flop where it is phase-locked with 500-kc from the 500-kc astable oscillator circuit (1-megacycle oscillator and 2:1 reduction counter). This synchronization operation is necessary to ensure that the same time interval is allotted for storing the analog voltage each encode time and that stepping of the 10-stage counter starts on the correct phase when the encoding process is begun. As a result of coincident edges of these inputs, the start/stop control flip-flop sets and provides a disable level to the bit counter gate. This prevents triggering of the 10-stage counter during storing of the analog voltage. The start/stop control flip-flop also closes switches (gating diodes) in the buffer amplifier circuit to enable storing of the analog voltage.

During the interval that follows, the MOS gate and buffer amplifier enable charging of the ramp capacitor to the analog voltage on the PAM bus. This process continues until the 170-microsecond pulse is terminated. With the next correct phase of the 500-kc input to the start/stop control flip-flop after the 170-microsecond pulse is terminated, the start/stop flip-flop changes states. This action opens the buffer amplifier switches and isolates the PAM bus input from the ramp capacitor. Concurrently, the start/stop control flip-flop supplies an enable level to the bit counter gate.

In coincidence with enabling of the bit counter gate, the ramp capacitor begins discharging through the constant current source at a precise linear rate; this rate is approximately 3.128 millivolts per microsecond. Thus, for each cycle of the 500-kc squarewave (2 microseconds) the ramp capacitor discharges the equivalent of one bit. As long as the ramp capacitor voltage is greater than zero, the zero level detector causes the code/calibrate gate to condition the bit counter gate for passing the 500 kc. When ramp capacitor voltage decreases to zero, the zero level detector disables the bit counter gate by disabling the code/calibrate gate. If an overvoltage (greater than 6.4 volts) was not encoded, the seven MSB's of the count are transferred to the output shift register via the digital multiplexer. The three LSB's of the count are supplied to the programmer. These bits, if used, are patched at connector J1 or J13 from a 3-stage register located in programmer module 3 and inserted in the

FOLDOUT FRAME 1

FOLDOUT FRAME 2

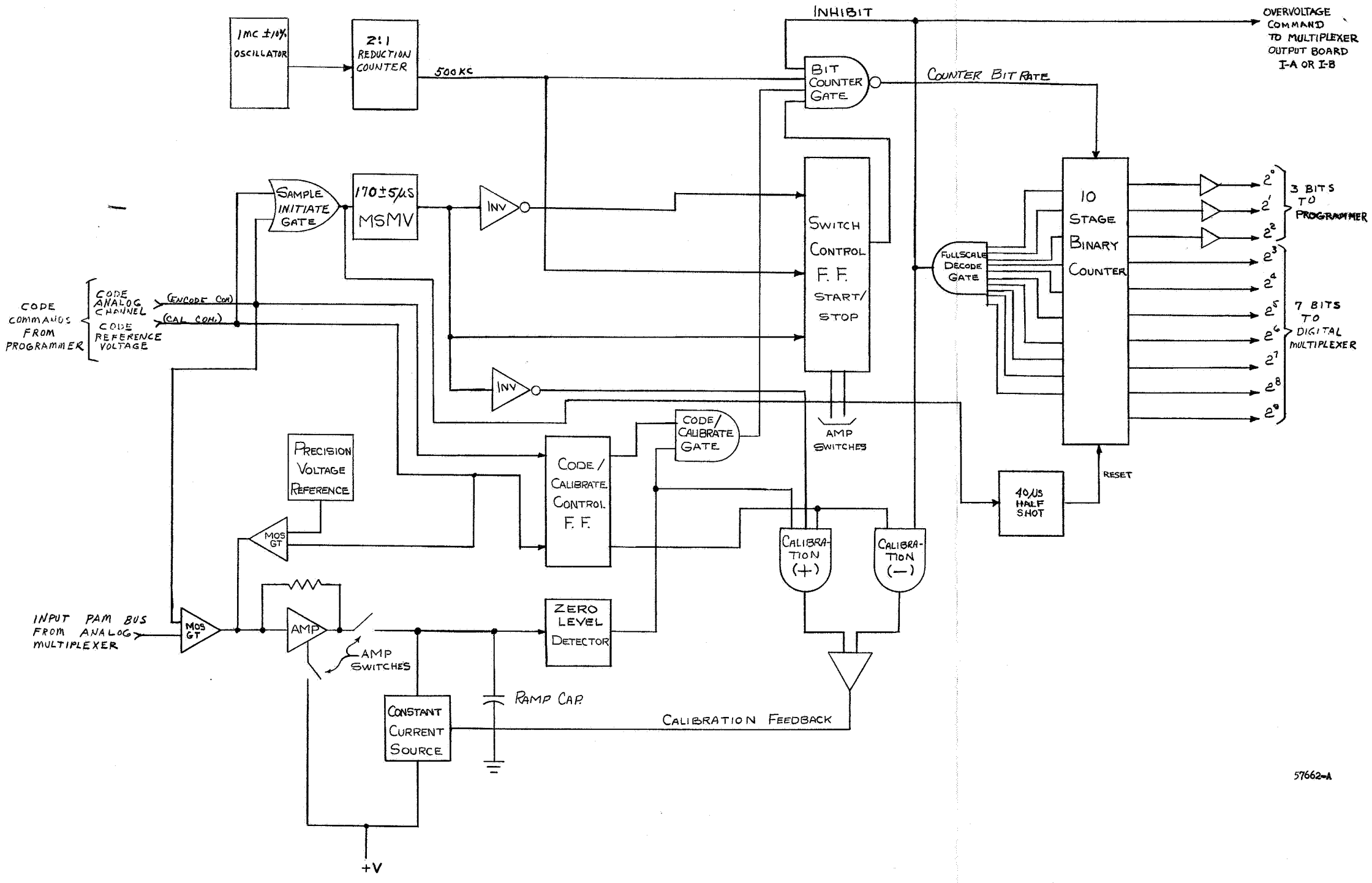


Figure 29. Coder Simplied Block Diagram

first three bit slots of the next word. If an overvoltage is encoded, the 10-stage counter reaches its full count (1023) before the zero level detector disables the bit counter gate. To prevent counter recycling, the full count is decoded and inhibits the 500-kc squarewave at the bit counter gate. The decoded full count (overvoltage command) is also routed to output board 1; (A or B) where it causes digital inputs to be used instead of using the count in the 10-stage counter.

For a calibrate cycle, the programmer supplies the coder with a calibrate command. Like the encode command, the calibrate command activates the code/calibrate control flip-flop. However, for a calibrate operation, the flip-flop enables the calibration (+) and calibration (-) gates. The calibrate command also enables a MOS gate that provides the precision reference voltage (full scale voltage of -6.4 volts) to the buffer amplifier input. In coincidence with this action, the calibrate command triggers the 170-microsecond monostable multivibrator. The action that follows is the same as that for an encode cycle. That is, the 170-microsecond pulse and 500-kc squarewave trigger the start/stop flip-flop which, in turn, closes the buffer amplifier switches to store the precision voltage on the ramp capacitor. When the sample and hold operation is completed, the ramp capacitor discharges the precision voltage through the constant-current source. Again, the bit counter gate passes the 500-kc squarewave as long as the ramp capacitor voltage is greater than zero or a full count is not recorded. If the 10-stage counter reaches a full count before the zero level detector reaches a zero level (indicative of a slow discharge rate), the calibrate (-) gate provides a correction signal to the constant-current source until a full count is reached. Similarly, if the zero level detector detects a zero level before a full count is reached (indicative of a fast discharge rate), the calibration (+) gate provides a correction signal to the constant-current source until a full count is reached. Thus, the constant-current source receives a correction signal that is proportional to difference between zero level detection and full count detection. These correction signals adjust the rate of ramp capacitor discharge to compensate for circuit aging and temperature variations. Except during power turn-on, the coder calibrate cycle supplies the full correction current in only one cycle. During power turn-on, several cycles are required to charge the ramp capacitor. Since normal operation provides three calibrate cycles per encode cycle, the desired accuracy is achieved for all conditions.

The coder consists of three modules designated coder module 1, 2, and 3. Coder module 1 containing the analog circuits is termed the analog module. Coder modules 2 and 3 are both digital modules.

2.2.2.6. OUTPUT REGISTER AND SPLIT-PHASE CONVERTER GENERAL DESCRIPTION. The output register and NRZ-to-split-phase converter are located in one module. Because block redundancy is employed (two modules in each PCM unit), only one module is described. This module is illustrated in the simplified logic diagram, figure 30.

The shift register receives eight parallel read-in data bits from the digital multiplexer and a 15-microsecond load strobe from the programmer. After the data has been loaded by the 15-microsecond strobe, the shift line serially shifts the data out as NRZ code at a 500-cps bit rate. The NRZ code is then converted to split-phase Mark 0 such that a continuous series of binary ONE's appears as a squarewave at bit rate, and a continuous series of binary ZERO's appears as a squarewave at one half the bit rate. The binary ZERO bits in the output

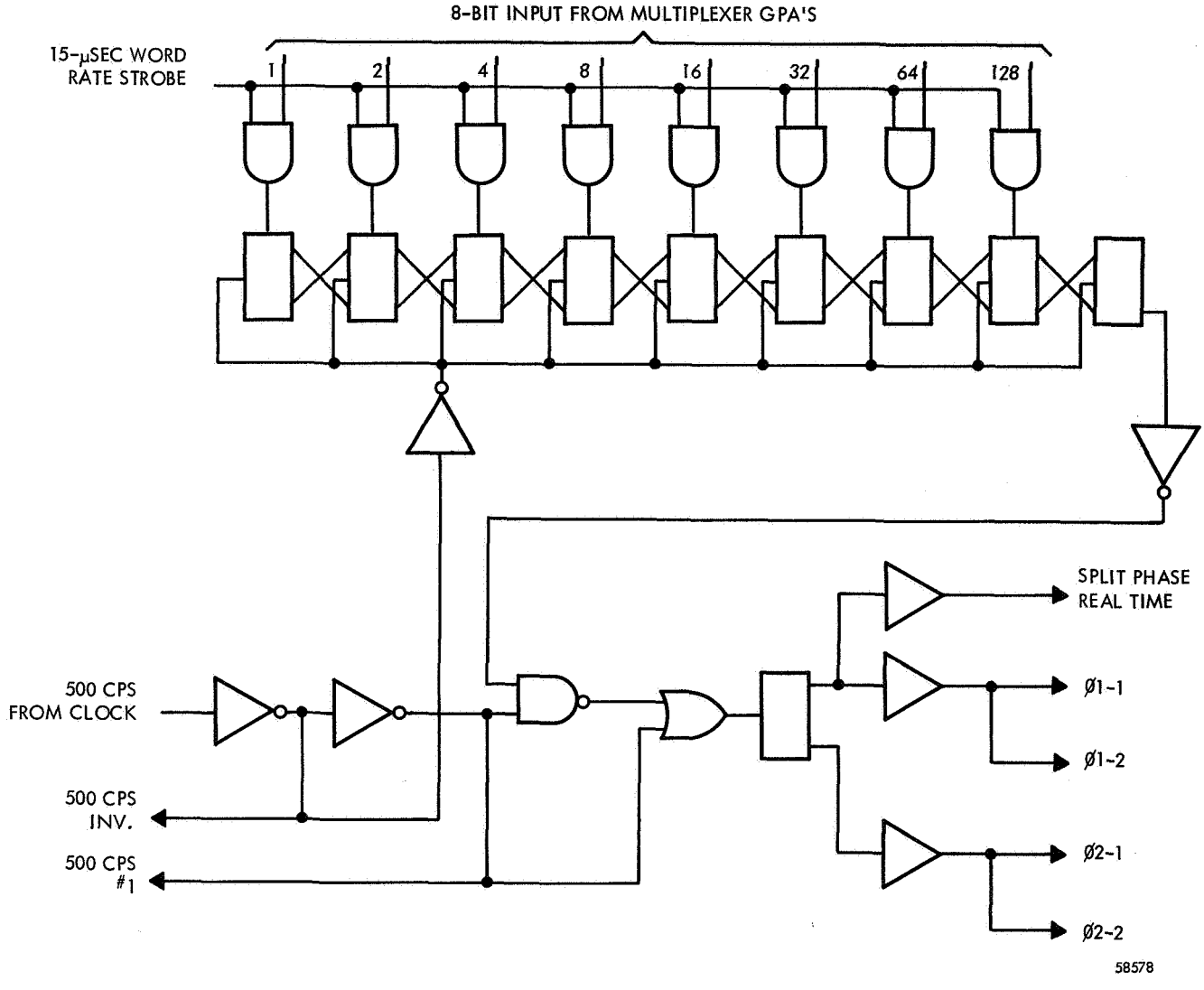


Figure 30. Programmer Output Shift Register/Split - Phase Converter, Simplified Block Diagram

are phase shifted while the binary ONE bits are not. A transition occurs in the middle of all bits (binary ONE's or ZERO's) and a transition occurs at the beginning of all binary ONE's.

The split-phase converter output is applied to three output drivers. One driver routes the real-time PCM data to the TME unit; the other drivers each supply two outputs that provide two phases of the output data to the two record amplifiers in the TME unit. The two record amplifiers are driven in parallel through separate isolation resistors so that shorting of one output line does not affect the data to the second recorder. In addition, the five output lines are connected to the five output lines of the other output register module to achieve block redundancy while using one set of output wires. To provide fail-safe operation in the event of a single failure, resistors are used as protection for the record amplifier signals, while a diode protects the PCM unit real-time driver.

The output register and split-phase converter module also contains the 500-cps buffer amplifier for CY500 from the Nimbus C clock. This buffer amplifier produces both phases of the 500-cps signal, with one phase operating the countdown flip-flops and shift register. Both phases are used for logic gating commands to the programmer and to generate the split-phase code.

2.2.2.7. POWER SUPPLY GENERAL DESCRIPTION

The power supply consists of an input voltage regulator, a dc chopper and saturable transformer, and diode rectifiers with output filtering for the various output dc voltages. The dc chopper and saturable transformer perform a function comparable to a conventional vibrator and power transformer. There are two block redundant power supplies in the PCM unit. These supplies are contained in one brass-covered module designated 1A17. Figure 31 illustrates a simplified block diagram of one power Supply unit.

Negative voltage operating power from the Nimbus B power supply of -24.5 vdc ±2% is applied through CR2 to the voltage regulator and chopper networks. (Diode CR2 provides reverse polarity circuit protection.) The input voltage into the chopper is converted to ac voltages that are conventionally rectified and filtered to produce isolated dc outputs.

The input voltage provides a reference voltage through CR3 to one side of differential amplifier Q3. The voltage input into the other side of the amplifier represents a sampling of the output across the high side of the series regulator. This sampling voltage is compared against the reference voltage by Q3 and an error voltage is generated if the input voltage is other than -24.5 vdc. The error voltage is amplified by Q1 and applied to the series regulator as a correcting voltage. This action results in a substantially constant voltage between the chopper input and the high side of the series regulator. The RFI filter shown in the diagram is used to suppress transient voltages.

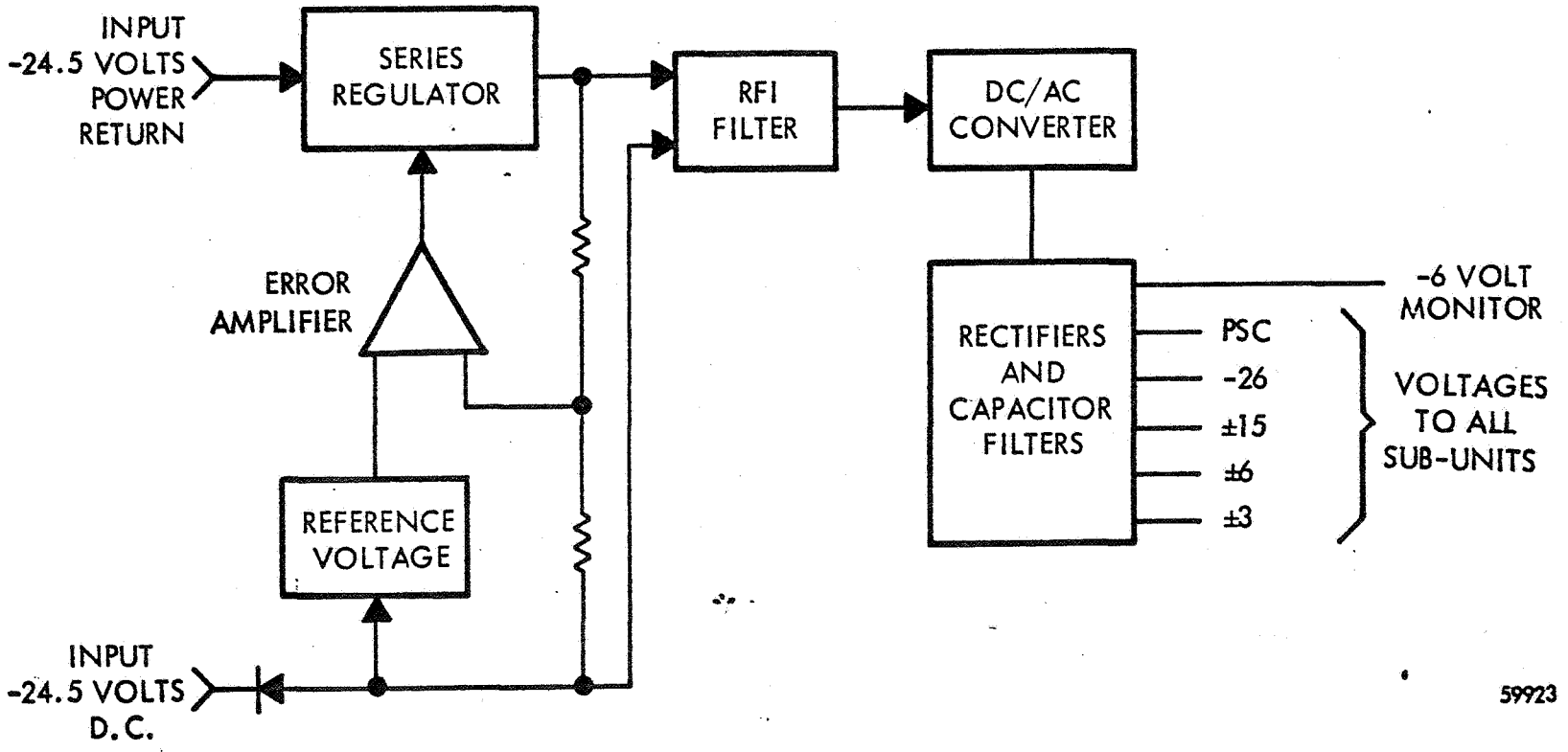


Figure 31. Power Supply Simplified Block Diagram

2.3. NIMBUS B QUALIFICATION AND FLIGHT MODEL MODIFICATIONS AND COMPONENT DIFFERENCES

This section describes the specific modifications and product improvements to the Nimbus B Study PCM Unit accomplished under this contract. Several modifications and product improvements were inherent in the Nimbus B Study PCM Unit and certain modifications were required as a result of problem areas that were discovered during testing of the Qualification and Flight Models. Modifications were accomplished in the areas of electrical design, electrical and mechanical packaging, and in the area of component differences between the Qualification and Flight Models with specific reference to the problem of the MOSFET device failures encountered during testing. Discussions of the details of these modifications and product improvements, including their background, are given in the following subparagraphs.

2.3.1. ELECTRICAL DESIGN CONSIDERATIONS

The Nimbus Study PCM Unit was fabricated "as is" for the Nimbus B program. However, several product-improvement changes have been incorporated: one in the multiplexer, four in the coder, and one in the shift register and split-phase converter. These changes are as follows:

a. MOSFET multiplexer switch body bias circuit was changed from the Zener diode in the Study PCM to an RC network in the Nimbus B PCM.

b. The PAM line into the coder from the multiplexer is direct in the Study PCM; an additional MOSFET switch has been added into the PAM line in the Nimbus B PCM.

c. The coder ramp 10-stage counter in the Nimbus B PCM is reset by a slow, high voltage transistor to alleviate a voltage-over-stress condition encountered in the Study PCM counter-reset transistor. Reset timing has also been modified in Nimbus B to compensate for the slower transistor used.

d. Outputs from the coder seven-stage counter to the digital multiplexer were fed through diode-resistor isolation circuits in the Study PCM. These circuits were thought to be unnecessary for Nimbus B and were not included in the original hardware. However, the isolation circuits still proved necessary and were added to Nimbus B.

e. During thermal cycling, random bit dropout occurred in the output shift register and split-phase converter due to improper loading and out-of-tolerance supply voltages. Many circuit design changes have been incorporated to alleviate this condition.

2.3.1.1. MULTIPLEXER MOSFET BODY BIAS CHANGE. The multiplexer MOSFET-body bias circuitry presented a noise problem that was discovered early in the Nimbus Program. Feedback noise pulses were encountered at the input transducers when MOSFET gates were turned "ON". This condition was caused by a negative pulse being capacitively coupled from gate to body when the gate was strobed ON (from +5 volts to -26 volts). The pulse caused the source-to-body junction to be forward-biased and the MOSFET gate functioned as a capacitor multiplier. A negative pulse, from 1 to 2 volts in amplitude and about 1/2 microsecond in duration, appeared

at the source terminal. In this case, the pulse at the source terminal is smaller in amplitude because the gate-to-body capacitance is small (2 to 3 picofarads).

By returning the MOSFET body directly to ground, the feedback capacity would be minimum (approximately 2 picofarads), and the feedback noise caused by the switching time transitions would be minimized. However, this solution for the problem of feedback noise to the transducer could not be effected due to the input +0.5-volt fault requirement as well as the fail-safe design criteria. A 100-K ohm resistor to +6 volts was installed in the body leads of all MOSFET gate flat packs, but this allowed the MOSFET to operate as a capacity amplifier when the gate lead was suddenly switched to the negative supply that enabled the gate. This capacity allowed a negative voltage noise spike of 4 to 8 volts to appear at the input transducer. The ultimate solution to the feedback problem would be to place a capacitor across the resistor in the body leak, thus creating an RC network. However, since the Study PCM had been completely fabricated at the time, the desired fix (an RC network) would not physically fit on the multilayer cards; in addition, the capacitors were not available to meet delivery requirements. As an alternate solution the resistors to the +6 volts were replaced with 6-volt Zener diodes connected to PSC in the Study PCM because they would fit physically and were readily available.

Nimbus B multilayer cards were modified to permit use of the desired RC network. The net result is less noise feedback into the Nimbus B PCM transducer circuits than in the Nimbus Study PCM. The use of an RC network between the body terminal of the MOSFET gate and +6 volts provides the required positive overvoltage protection and also provides a low impedance reference point for the body. The RC network was chosen as the best solution to the problem, with the addition of several capacitors being the only drawback. An analysis of the RC network is contained in the following paragraphs.

The RC network should contain a resistance large enough so that, if the body terminal shorts to another element in the gate, the increased load on the +6-volt power supply would be negligible. This value of resistance was determined to be 100K ohms. As shown in figure 32, the minimum time between MOSFET gate duty cycle pulses is 2.8 milliseconds. The value of C_1 must be chosen such that T = 5RC is less than 2.8 milliseconds, and such that the body terminal of the MOSFET gate never goes below ground. The MOSFET gate specification states that the maximum capacitance between the drain terminal and all other elements of the gate is 2 picofarads. The maximum capacitance between the gate terminal and all other elements of the gate is 3 picofarads. Since each flatpack contains five gates, the total capacitance is 10 and 15 picofarads for these two cases. Using the worst-case capacitance of 15 picofarads for C_2 (figure 32), C_1 should be no less than 65 picofarads to keep the body terminal of the MOSFET gate above ground. To ensure that the body terminal stays above ground (over temperature range, etc.), a value of 470 picofarads was chosen for C_1. With T = 5RC using a 470-picofarad capacitor and a 100 K ohm resistor, a time of 235 microseconds is obtained, which is well within the 2.8 milliseconds allotted for recovery time of C_2.

The final solution to feedback noise problems provides for connection of the selected RC network in all body connections of all MOSFET flatpacks for both the analog and digital channel gates, first sequencers, and final sequencers. With this problem solved (the only multiplexer problem), the Nimbus B multiplexer provides significant improvement over the old Nimbus system multiplexer.

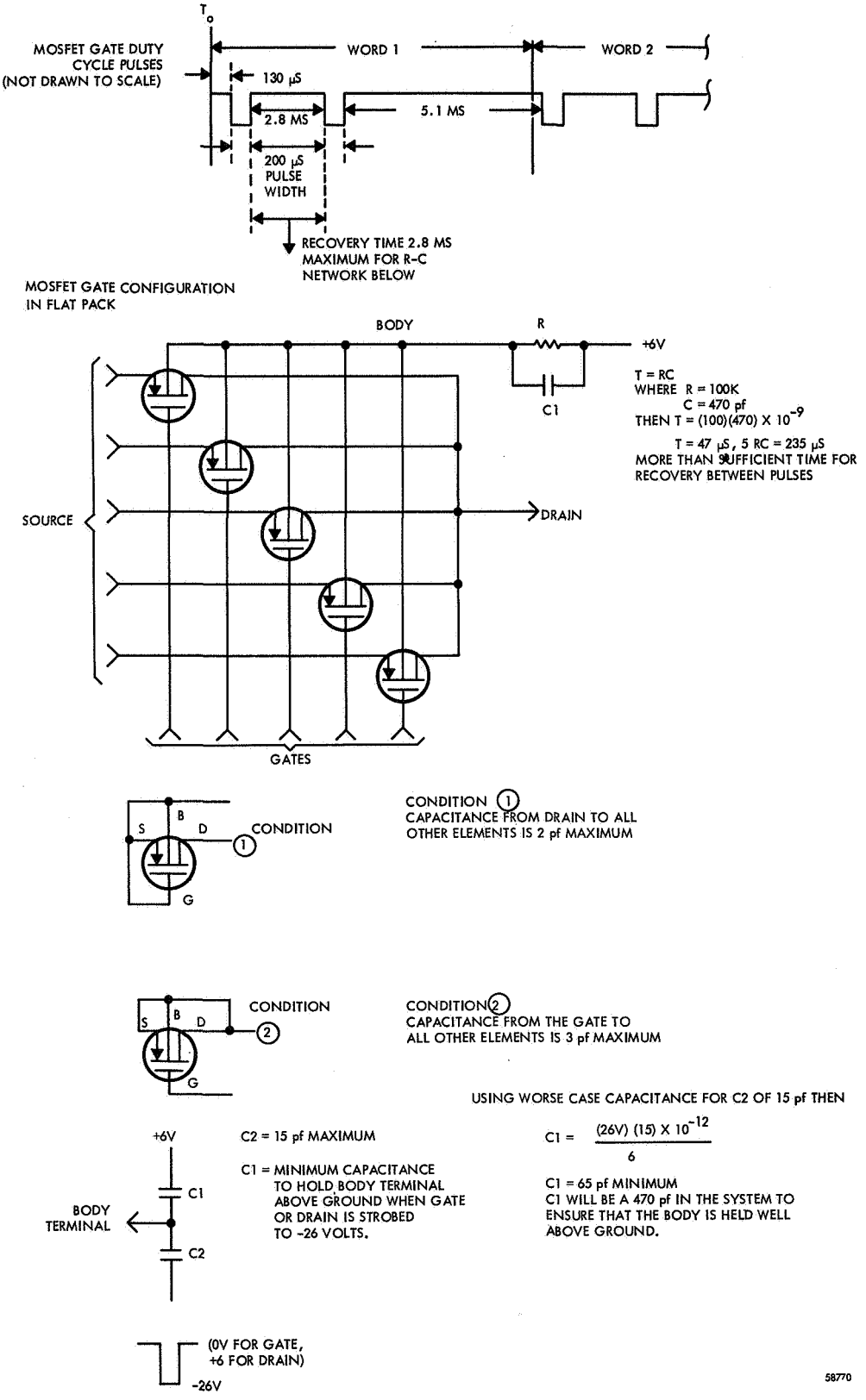


Figure 32. RC Network Analysis

2.3.1.2. CODER CHANGES. There are five minor changes in the Nimbus B Coder, with one change having been made in each of the three Coder modules. Each of the changes improve the Coder's immunity to noise and therefore provide for more reliable data conversion.

2.3.1.2.1. PAM INPUT FROM MULTIPLEXER. The Nimbus Study PCM Coder operated properly until the final package compression step in the fabrication process. When the cards were compressed into their final configuration, both coders had a sudden increase in full-scale voltage from approximately -6.401 volts to -6.413 volts for PCM No. 1, and -6.415 volts for PCM No. 2. It was determined that the only possible cause for full-scale voltage increase would be that the voltage calibrate reference increased. Since both coders increased and remained within ±3 millivolts of the average straight line from minimum scale (0 volts) to the new full scale (-6.415 volts), the problem affected both coders. The only difference in the newly-compressed PCM unit was that the general-purpose amplifiers were duty cycled. The duty cycling involved a -26 volt power switch which could produce noise on adjacent circuits; this noise would increase as the circuits were compressed. The PAM lines into both coders are routed through the multiplexer amplifier interconnect area close to the -26 volt power switching circuit. Since both coders (PCM No. 1 and PCM No. 2) were affected, and since the coding conversion was still linear, it became obvious that the calibrate voltages were increasing due to noise or crosstalk from the -26 volt multiplexer power switches.

The solution to this problem was to isolate the calibrate voltage from the multiplexer PAM bus, so the multiplexer switching noise could not be picked up or added to the calibrate precision voltage. This change was made by adding a MOSFET gate in the input to coder module No. 1 that is turned ON only during the encode or sample cycle. When this MOSFET is OFF and the calibrate MOSFET is ON, the multiplexer noise is isolated and cannot enter the coder.

The added MOSFET gate and driver in coder module No. 1 are Q16 and Q23 (figure 33) with the input-driver transistor being Q44 in coder module no. 2 (figure 34). These circuits are activated by the encode command from the programmer.

The input analog gate, MOS gate Q16, isolates the buffer amplifier input from the multiplexer during a calibrate cycle. This isolation prevents multiplexer noise from creating inaccuracies in the calibration voltage. During an encode cycle, the input analog gate connects the multiplexer analog voltage to the input of the buffer amplifier. Transistor Q23 controls the switching of Q16. During the encode cycle, the FF2 input from the code/calibrate bistable goes positive and turns on Q23. As a result of the negative transition on its gate, Q16 connects the PAM input to the base of Q13A. During the calibration cycle, the FF2 is a negative level and holds Q23 off. Thus, Q16 isolates the multiplexer from the buffer amplifier input.

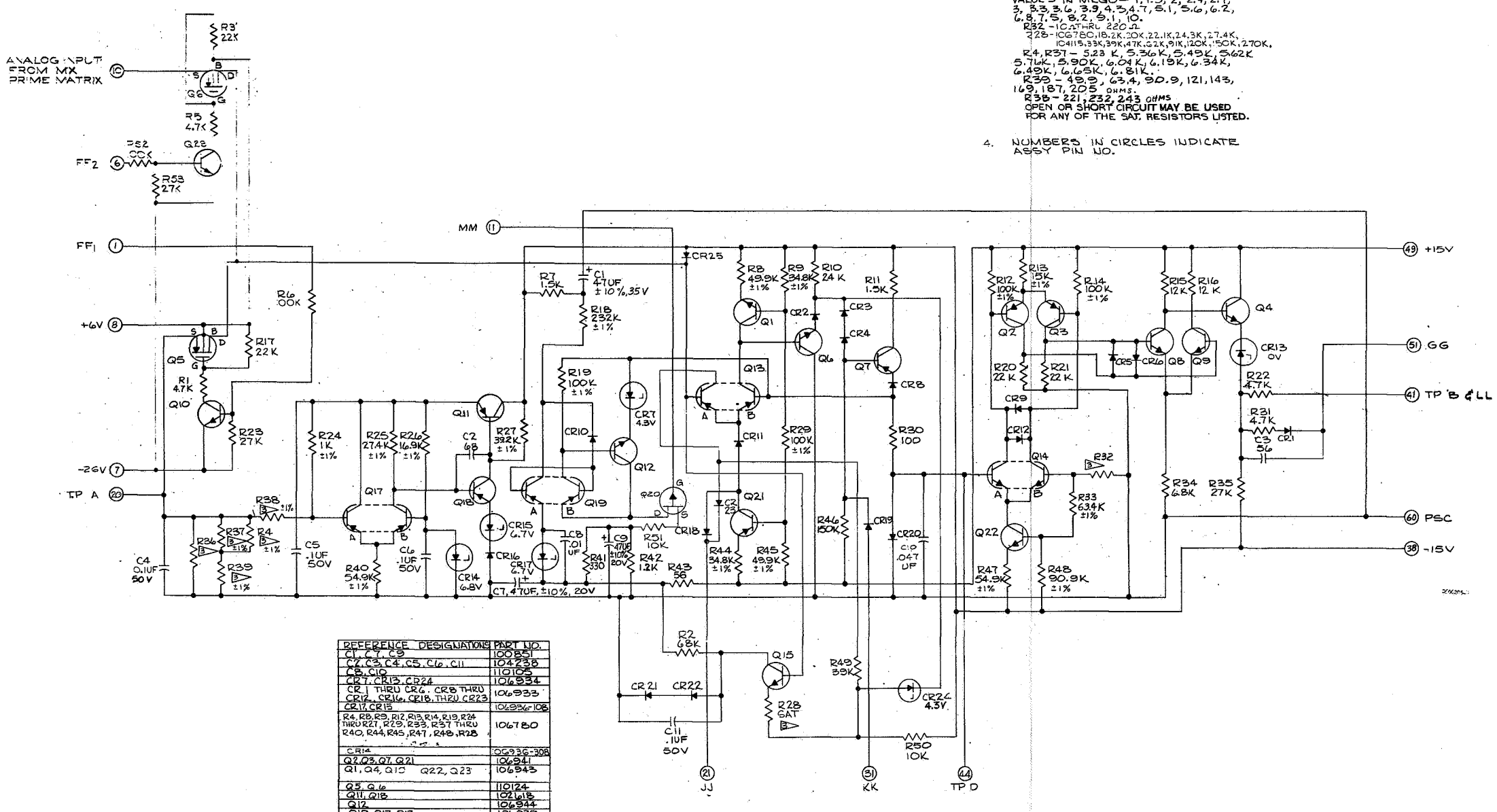
Activation of the code/calibrate gate circuits in coder module No. 1 are controlled by the MOS command circuit in coder module No. 2 (figure 34). The MOS command circuit consists of transistors Q17 and Q44. Both are operated as common-base switches in which the output follows the input. Positive encode commands (nominal +6 volts) to the emitter of Q44 cause the stage to saturate and result in positive commands (FF2) that activate the input analog gate circuit in coder module No. 1. Similarly, the positive calibrate commands to the emitter of Q17 saturate this stage and result in activation of the calibrate gate circuits in coder module No. 1.

FOLDOUT FRAME 1

FOLDOUT FRAME 2

NOTES:

1. PARTIAL REF DES ARE SHOWN; FOR COMPLETE DES, PREFIX WITH UNIT NO. OR SUB-ASSY. DES.
2. UNLESS OTHERWISE SPECIFIED, RESISTANCE VALUES ARE IN OHMS, ¼W ±5% TOL.; CAPACITANCE VALUES ARE IN PICOFARDS ±10% TOL. 200V
3. SELECT AT TEST COMPONENTS
   RANGE OF VALUES: R36
   VALUES IN MEGO – 1, 1.5, 2, 2.4, 2.7, 3, 3.3, 3.6, 3.9, 4.3, 4.7, 5.1, 5.6, 6.2, 6.8, 7.5, 8.2, 9.1, 10.
   R32 – 10, 47, 82, 220 Ω.
   R28 – 10, 68, 180, 2K, 20K, 22.1K, 24.3K, 27.4K, 10, 115, 33K, 39K, 47K, 62K, 91K, 120K, 150K, 270K.
   R4, R37 – 5.23 K, 5.36K, 5.49K, 5.62K 5.74K, 5.90K, 6.04K, 6.19K, 6.34K, 6.49K, 6.65K, 6.81K.
   R39 – 48.9, 63.4, 90.9, 121, 143, 169, 187, 205 OHMS.
   R38 – 221, 232, 243 OHMS
   OPEN OR SHORT CIRCUIT MAY BE USED FOR ANY OF THE SAT. RESISTORS LISTED.
4. NUMBERS IN CIRCLES INDICATE ASSY PIN NO.



REFERENCE DESIGNATIONS	PART NO.
C1, C7, C8	100851
C2, C3, C4, C5, C6, C11	104238
C9, C10	110105
CR7, CR13, CR24	106934
CR1 THRU CR6, CR8 THRU CR12, CR14, CR16, THRU CR23	106933
CR17, CR15	106936-108
R4, R8, R9, R17, R13, R14, R19, R24 THRU R27, R29, R33, R37 THRU R40, R44, R45, R47, R48, R28	106780
CR14	06936-308
Q2, Q3, Q7, Q21	106341
Q1, Q4, Q13 Q22, Q23	106343
Q5, Q16	110124
Q11, Q18	106418
Q12	106344
Q15, Q17, Q13	106339
Q14,	106340
Q20	110088
Q6, Q8, Q9,	110092
R2, R6, R7, R10, R11, R15, R16, R17, R20 THRU R23, R26, R50, R31, R32, R34, R35, R36, R41, R42 R43, R46, R49, R50, R1, R51, R3, R5 R52, R53	104115
Q15	106942
CR25	100828
R18	04608

Figure 33. Coder Module No. 1, Schematic Diagram

FOLDOUT FRAME 1

REF. DESIGNATION	PART NO.
CR1 THRU CR16, CR23, CR33, CR36, CR38, CR39 THRU CR45, CR49	106833
R67, R76, R88, R3, R4	106780
C3, C20	100851
C4 THRU C14, C19	104238
Q31, Q32	106942
Q11	102618
Q3, Q4, Q5, Q8, Q9, Q10, Q12	101936
Q6, Q7	106943
Q34, Q17, Q37, Q44	106941
Q13, Q16, Q18 THRU Q30, Q33, Q43	110092
R2, 5-40, 44-65, 70-75, 77, 78, 84-101	104115
Q35, Q36, Q38 THRU Q42	110095
CR17, CR18	106836
Q14 + Q15	110121
C1, C2	104202
C21	106299

FOLDOUT FRAME 2

NOTES:

1. UNLESS OTHERWISE SPECIFIED, RESISTANCE VALUES ARE IN OHMS, ±5% TOL, ⅛ WATT, CAPACITANCE VALUES ARE IN PICOFARADS, ± 10%, 200 VOLTS, DIODES ARE IN916.
2. PARTIAL REF. DESIGNATIONS ARE SHOWN; FOR COMPLETE DESIGNATION PREFIX WITH UNIT NO. OR SUBASSY DESIGNATION (S).
3. NUMBERS IN CIRCLES INDICATES ASSY PIN NUMBERS.

▷ SELECT AT TEST COMPONENTS RANGE OF VALUES, R3, R4, 10.5K, 11.3K, 12.1K, 13.7K.

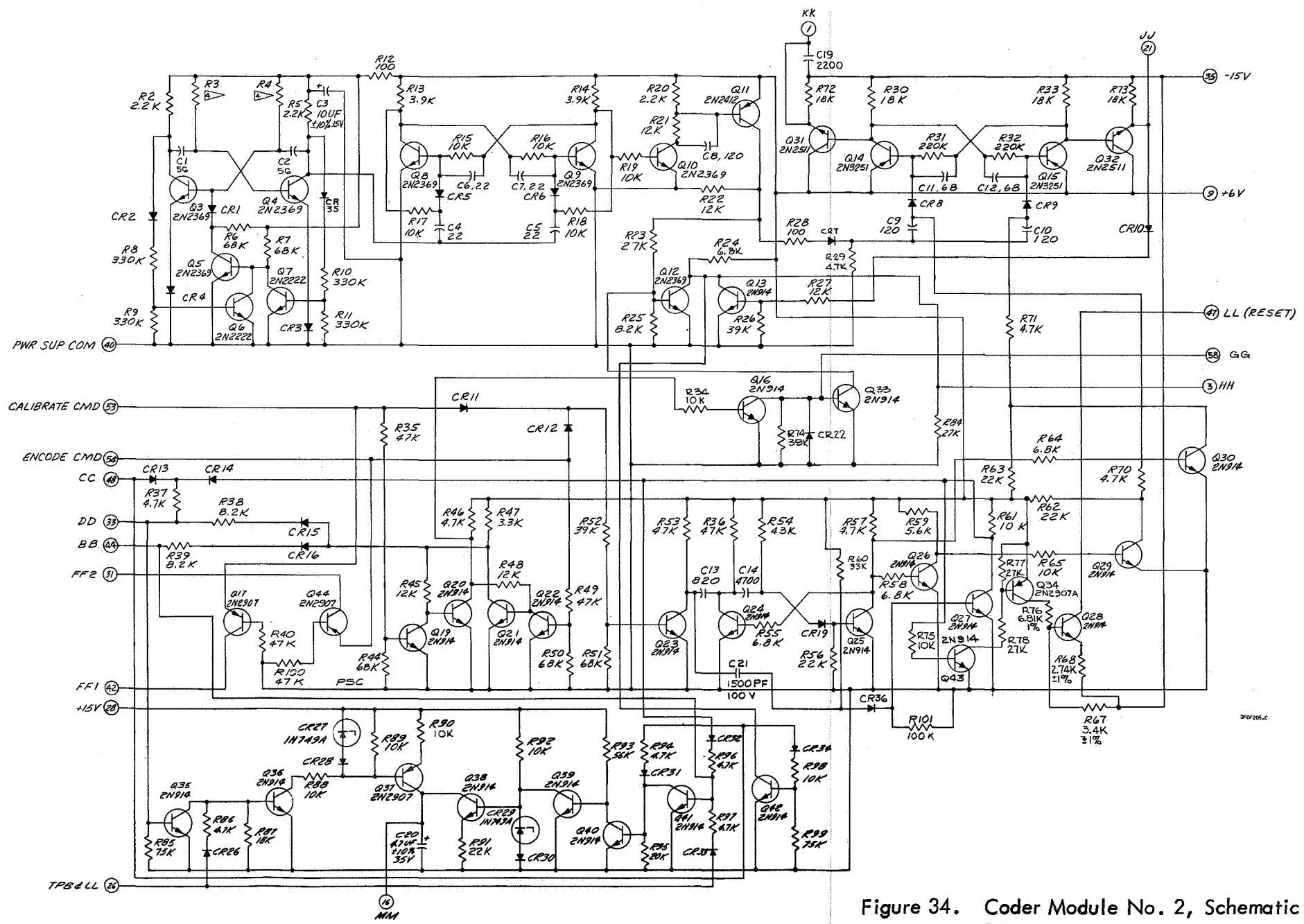


Figure 34. Coder Module No. 2, Schematic Diagram

2.3.1.2.2. 10-BIT COUNTER RESET CIRCUIT. The Nimbus Study PCM Coder 10-Bit counter operates properly, but transistor Q34 (a 2N2412) in coder module No. 2 (figure 34) is voltage overstressed. This overstress is less than that allowed by the transistor manufacturer but is greater than that allowed by the reliability derating philosophy. Good engineering practice dictated a change to a higher voltage device, which turned out to be a larger geometry device with subsequently greater delay and storage times for "turn ON" and "turn OFF". The Q34 transistor used was changed to a 2N2907A which had more storage time than the circuit allows, and as a result, the Nimbus B 10-stage counter was still being held in the reset state during the time the first two or three counts were being fed into the counters. Consequently, these two or three counts were lost and the coder output was 12 to 18 millivolts less than the coder input.

To solve this problem the reset pulse was retimed by reconnecting transistor Q27, to operate as a half-shot whose "OFF" time is determined by capacitor C21, diode CR36, and resistors R60 and R101. Thus the reset pulse occurs for approximately 40 microseconds, beginning at the leading edge of the 170 microsecond monostable command, so the reset pulse to the counters (transistor Q28) is removed approximately 130 microseconds before the first count enters the counters. This change also provides a greater safety margin than the circuit in the study PCM. This reset pulse occurs four times per word, first when the encode analog sample command is given, and then when the three calibrate commands are given.

2.3.1.2.3. 10-BIT COUNTER LOAD ISOLATION. The coder 10-stage counter contains three isolation buffers for the first three counter stages that are connected to storage registers in the programmer. The seven stages used to produce the 7-bit analog words were directly coupled through MOSFET gates into the GPA circuits. Switching circuit noise transients were generated in the Nimbus Study PCM whenever the GPA's and Final Sequencer MOSFETs were power strobed to the "ON" condition, as explained in detail in the New Technology Section III of the Nimbus Study Final Report.

The noise problems were solved one at a time with several fixes installed in the Study PCM. One of these fixes entailed diode-resistor isolation for the seven data bits from the coder to the final sequencers by installing components on the printed circuit card in the pad area where hard wires are fed from the module card to Output Board No. II. This fix solved the problem, but not the source of the problem. The source of the problem was eliminated when the GPA "turn ON" time was increased by an RC filter, and when the MOSFET final sequencer body bias circuit was changed from a resistor to a zener diode in the Study PCM and to an RC circuit for the Nimbus B PCM. At this time, it was decided to retain the diode-resistor fix to avoid damaging the printed circuit cards as replacing the cards could have caused as much as two months slippage in delivery of the Nimbus Study PCM to the GE Integration Facility. A later change was made when the GPA and digital multiplexer circuits would not produce a reliable all-ONES code when an analog channel had an input voltage greater than 6.4 volts. The all-ONES code was not produced because when the GPA power strobe "turn ON" time was increased to solve the noise problem, the input capacitor into the GPA was no longer effective. This capacitor was replaced by a resistor which solved the all-ONES problem and at this time the Nimbus Study PCM was 100 percent operative. This resistor, however, created another problem that had been overlooked because of the diode-resistor fix previously mentioned.

When the Nimbus B PCM was fabricated, these diode-resistor fixes were left out because they were thought to be unnecessary. When the PCM Qualification model module cards were wired to the multiplexer output boards, it was again observed that random noise generated by the charge-transfer method would reset some of the coder counters to the ONE condition. Thus the diode-resistor fix was added to coder module No. 3 (figure 35) such that the outputs for 2^3 through 2^9 contain the series diodes CR46 through CR62 with PSC reference 22K resistors R71 through R77. The diode-resistor isolation circuit was added between each of the coder's seven counter outputs and the final sequencer MOSFET. The actual problem is that in the quiescent state just prior to gating an analog word into the GPA the input line on the GPA is at a voltage level between -6 volts and -26 volts owing to the 2.2 megohm resistor and the input leakage and capacitance of the GPA. When the MOSFET is turned ON, this capacitance high voltage is discharged back through the MOSFET and the counter circuit. If a ONE is stored in the counter circuit, there is no problem. However, if a ZERO is stored in the counter circuit, the GPA input negative voltage discharge resets this counter by base triggering the opposite side of the counter through the base speed-up capacitor. The diode-resistor fix prevents this negative noise spike of about two microseconds from reaching the counter output transistor, and therefore prevents the resetting of the counter to a ONE output.

2.3.1.2.4. REPORT ON SHIFT REGISTER AND SPLIT-PHASE CONVERTER PROBLEM

During the +55°C portion of thermal cycling on the Flight 1 Nimbus B Telemetry Subsystem, the PCM 2 unit began to drop several randomly bits of data from the data train. Investigation uncovered a circuit in the shift register and split-phase converter module (figure 36) that was causing the trouble. The components involved in the shift register module are R61, R62, Q14, Q20 and Q21. Some additional loading is placed on the circuit by programmer module 1 (figure 37) with the most important load involving R43, R44 and Q18. The Shift Register and Split-Phase Converter and Programmer circuit in question is shown in figure 38.

The problem area of this circuit as it is shown on figure 38 exists when Q19 is off. The collector voltage of Q19 rises to a value determined by the resistor divider network R61, R62 and R43 plus the energy gaps of Q20 and Q18. This value must be enough to keep the base-emitter junction of Q21 reverse biased thus keeping Q21 off. In other words the voltage at the collector of Q19 must not drop more than .4V below the emitter voltage of Q21. This was not the case at high temperature, however, and Q21 began to turn on intermittently. After examining the circuit, it became apparent that two factors contributed to the failure of this circuit at high temperature. They were:

1) Power supply deviations in excess of the circuit design philosophy used at the time of design.

2) The circuit in question did not have enough overall margin of safety built in.

The first item is not a problem in any other circuit except this particular one; therefore, no action will be taken to correct the power supply voltage deviations. At the time this circuit was designed, it was thought that all voltages would be within ±5% under all conditions. Since only one voltage from the power supply can be SAT'd to an exact value, the -6 volt output was chosen. Due to transformer winding tolerances the other voltages may

FOLDOUT FRAME 1

REF DESIGNATION	PART NO.
Q1 THRU Q9	101936
CR1 THRU 44, 46-52	106933
CR 45	106934
R1 THRU R77	104115
C1 THRU C40	104238
Q10 THRU Q25	106943

FOLDOUT FRAME 2

NOTES:

1. UNLESS OTHERWISE SPECIFIED, RESISTANCE VALUES ARE IN OHMS, ±5% TOLERANCE, ¼ WATT; CAPACITANCE VALUES ARE IN PICOFARADS, ±10% TOLERANCE, 200 VOLTS.
2. PARTIAL REF DESIGNATIONS ARE SHOWN; FOR COMPLETE DESIGNATION PREFIX WITH UNIT NO. OR SUBASSY DESIGNATION(S).
3. NUMBERS IN CIRCLES INDICATES ASSY PIN NUMBERS.

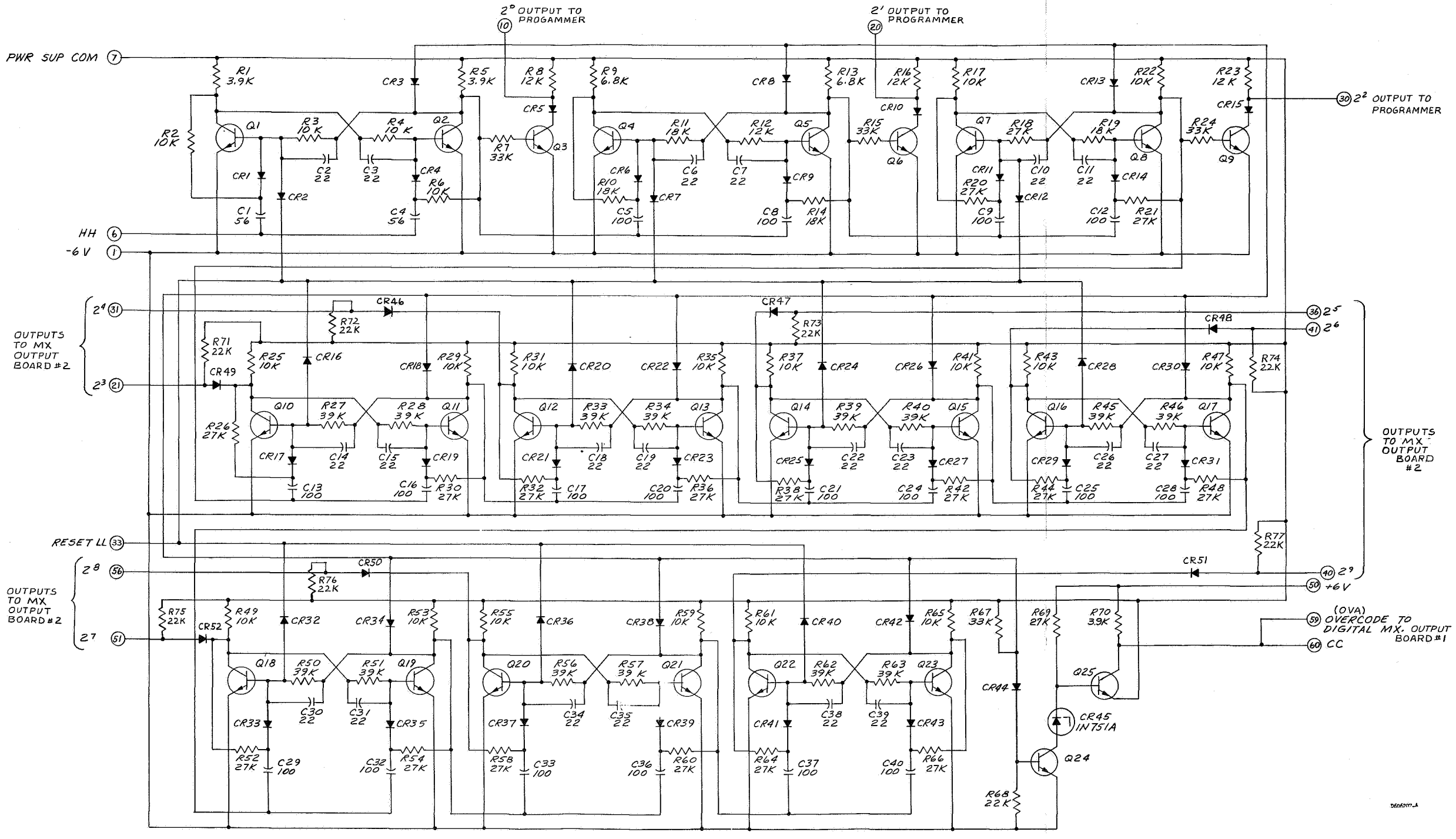


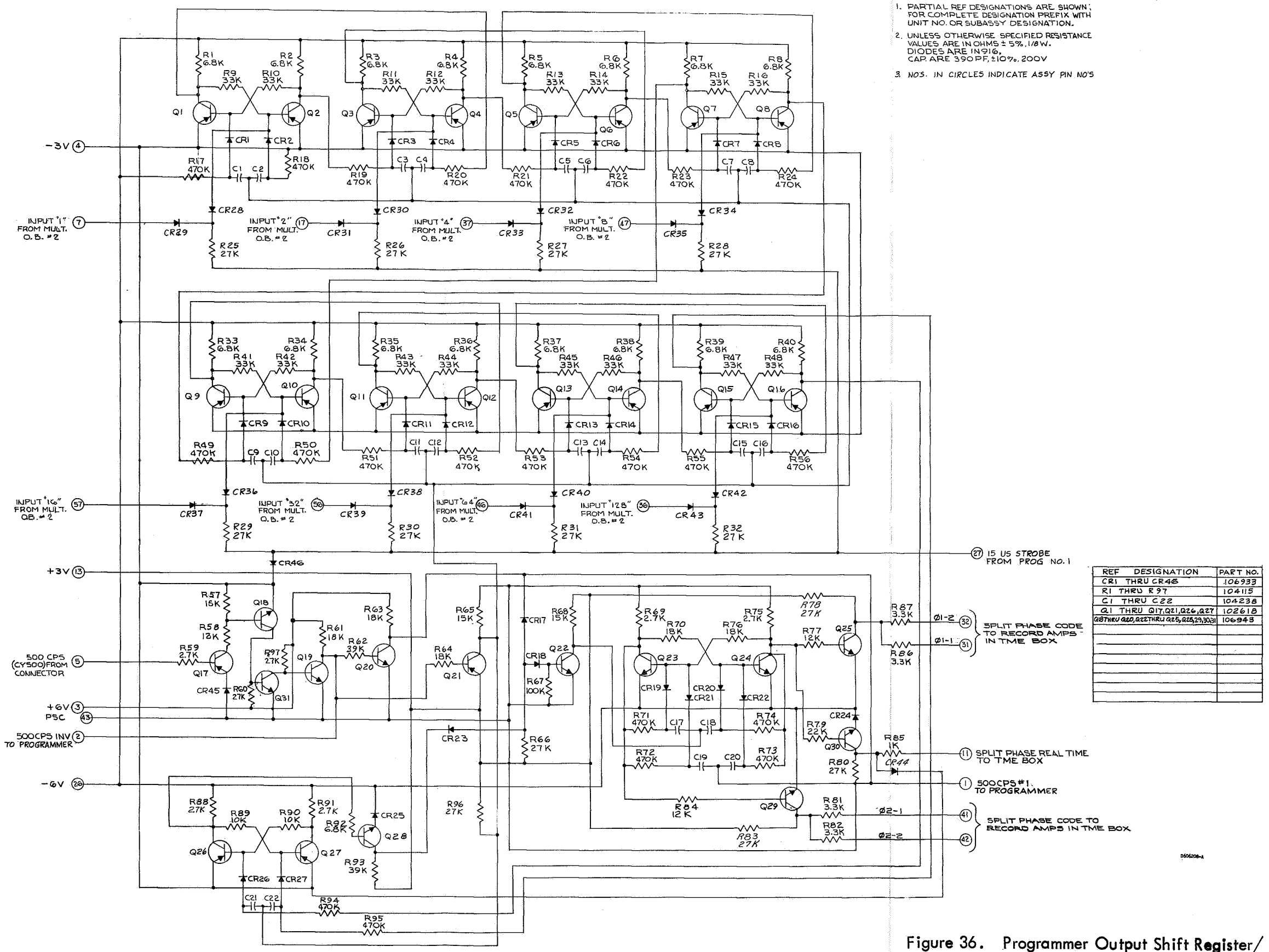
Figure 35. Coder Module No. 3, Schematic Diagram

FOLDOUT FRAME 1

FOLDOUT FRAME 2

NOTES:

1. PARTIAL REF DESIGNATIONS ARE SHOWN; FOR COMPLETE DESIGNATION PREFIX WITH UNIT NO. OR SUBASSY DESIGNATION.
2. UNLESS OTHERWISE SPECIFIED RESISTANCE VALUES ARE IN OHMS ± 5%, 1/8W. DIODES ARE 1N916, CAP. ARE 390 PF, ±10%, 200V
3. NOS. IN CIRCLES INDICATE ASSY PIN NO'S



REF DESIGNATION	PART NO.
CR1 THRU CR48	106933
R1 THRU R97	104115
C1 THRU C22	104238
Q1 THRU Q17, Q21, Q26, Q27	102618
Q18 THRU Q20, Q22 THRU Q25, Q28, Q29, Q30, Q31	106943

Figure 36. Programmer Output Shift Register/ Split - Phase Converter Schematic Diagram

FOLDOUT FRAME 1

FOLDOUT FRAME 2

REF DESIGNATION	PART NO.
CR1 – CR58	106933
Q1-Q22, Q25 – Q32	106943
Q23 & Q24	102618
C1 & C4	100851
C2, C5, C10, C7	104202
R1, R2, R4, R6, R7 – R13, R17 – R23, R25, R27 – R52, R54, R56 – R89	104115
R3, R5, R14, R15, R16, R24, R26, R40, R53, R55	106780
C8 – C17, C6, C3	104238

NOTES:
1. PARTIAL REF DESIGNATIONS ARE SHOWN; FOR COMPLETE DESIGNATIONS PREFIX WITH UNIT NO. OR SUBASSY DESIGNATION.
2. NUMBER IN CIRCLE INDICATES ASSY PIN NO.
3. UNLESS OTHERWISE SPECIFIED: RESISTANCE VALUES IN OHMS, ± 5%, 1/8 WATT. CAPACITANCE VALUES IN PICOFARADS ± 10%, 200 V. DIODES ARE IN916. TRANSISTORS ARE 2N2222.

4 SELECT AT TEST COMPONENT RANGE OF VALUES 820 K TO 56.8K ± 1%.

5 SELECT AT TEST COMPONENT RANGE OF VALUES R84, R86, R864 R87; 220K TO 1.5 MEGO ± 5% IN 10% STEPS.

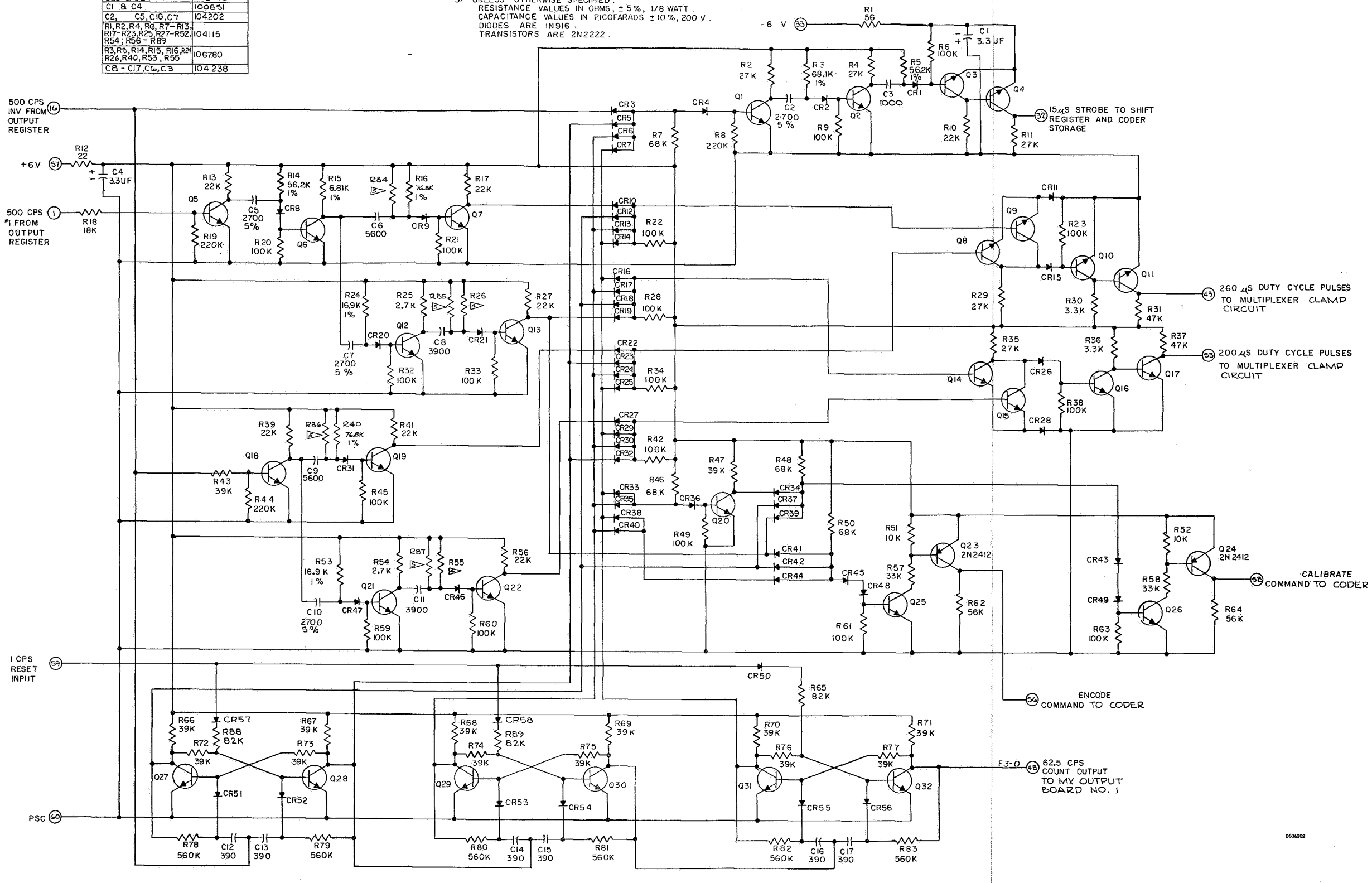


Figure 37. Programmer Module No. 1, Schematic Diagram

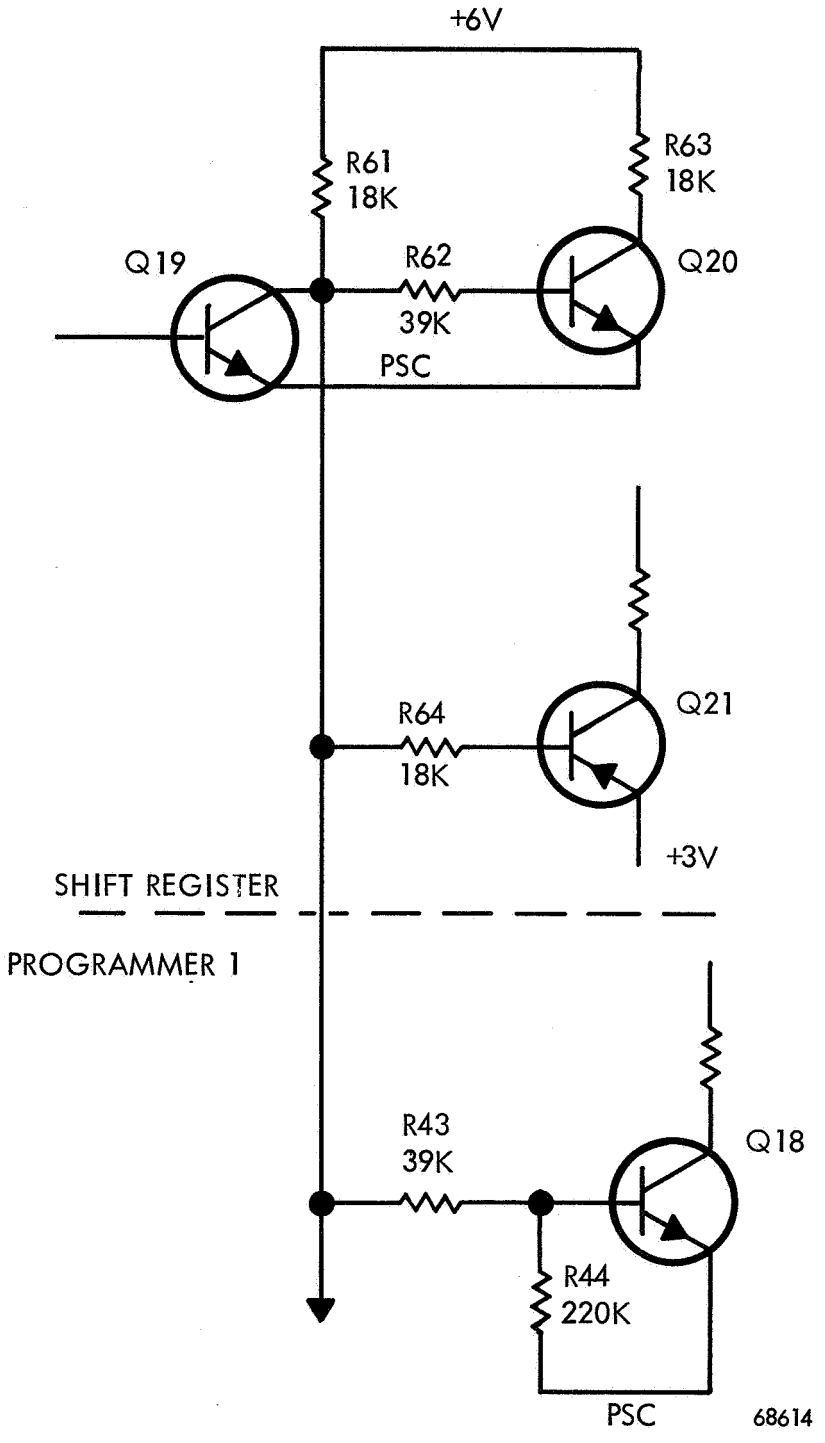


Figure 38. Shift Register and Programmer Problem Area Circuit

be out of the ±5% range at room ambient. The voltages that are out of the 5% range at room ambient may then deviate as much as 7% from nominal at high temperature. The 7% from nominal would not effect the circuit in question if all voltages changed in the same direction; however, this is not the case. At high temperature the +6 volt supply tends to drop in voltage (due to external load increases) and the +3 volts tends to rise. Since the base-emitter junction of Q21 actually works between these two voltages, if the difference between the two voltages decreases, the circuit could become marginal. The problem in the Shift Register Module was not identified in the Qualification Model or in Flight 1, PCM 1 because the power supplies were within the 5 percent limit on all voltages over temperature. The +3 and +6 volt supplies on Flight 1, PCM 2 were slightly out of the 5 percent range at room ambient and, beyond that temperature, the deviation increased to 7 percent. A 10 percent deviation will not affect any of the other circuits in the systems due to the tremendous safety factors used during the design phase.

The second problem area in the circuit in question is the lack of a safety margin. After the original design phase on Nimbus B had been completed and during the module fabrication phase, it was found that an additional stage of inversion was needed to obtain proper timing with respect to the Nimbus Clock. Q19 was added as this additional stage, and in the haste of making the necessary changes to a module in the fabrication stage, it is obvious that not enough design effort went into the change. Since this was the only change made at that time and since this circuit is the only circuit that uses a resistor divider to back bias a transistor to keep it off, no additional problems are anticipated. The voltage divider network was used because this stage must also perform level shifting functions and to save space and parts in the module that would otherwise have to be used to perform the same task. This circuit (figure 39) with proper design can be as reliable as the rest of the circuits in the system; as a matter of fact, only one resistor value need be changed to accomplish this. The modification simply consists of changing the value of resistor R61 such that the voltage at the collector of Q19 (when off) is closer to +6 volts. The value of R61 must be chosen to provide ample back bias voltage for Q21 under worse case conditions. Before examining the modified circuit, a look at the original circuit (paragraph 2.3.1.2.4.1) will yield information concerning the problem involved and will show how the modified circuit corrects this problem. The modified circuit analysis is discussed in paragraph 2.3.1.2.4.2.

2.3.1.2.4.1. Original Circuit Analysis. Worst case conditions that existed in the original circuit analysis are as follows:

a) 5%, then 7% voltage variations

b) VBE range .4 - .9 volts

c) Resistor variations 10%

d) 19.8K = (R61 + 10%)
17.55K = (R62 and R43 in parallel -10%)

e) Nominal voltages and the resistor values cited result in 2.66 + (VBE min of Q18 and Q20) = 3.06V at the base of Q21.

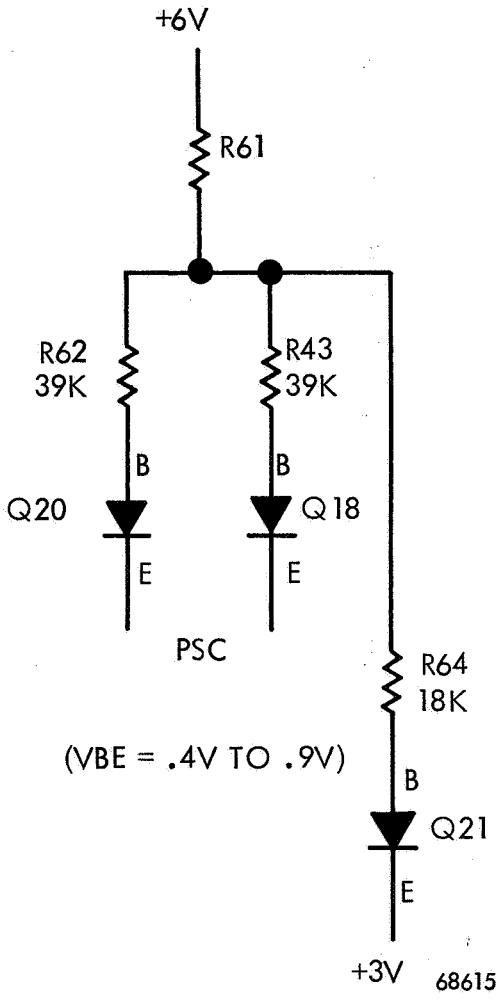


Figure 39. Equivalent Circuit

f) Taking 5% voltage variations yields:

3V + 5% = 3.15 (ΔV = .15V)

6V - 5% = 5.7V (ΔV = .30V)

g) Using the 5% voltages, the new figure for the base voltage of Q21 is:

3.06 nominal
- .30 10% ΔV
+ 2.76

h) The difference between the base and emitter voltages is:

3.15 emitter voltage
- 2.76 base voltage
.39V difference in the forward bias direction

i) Taking 7% voltage variations yields:

3V + 7% = 3.21 (ΔV = .21V)
6V - 7% = 5.58 (ΔV = .42V)

j) Using 7% voltages, the base voltage for Q21 becomes:

3.06
- .42
+ 2.64

k) The difference between the base and emitter voltages is:

3.21 emitter voltage
- 2.64 base voltage
.57V difference in the forward bias direction

As can be seen in step K the transistor (Q21) will not turn on.

2.3.1.2.4.2. MODIFIED CIRCUIT ANALYSIS. Worst case conditions in the modified circuit analysis are as follows:

a) 10% voltage variations

b) VBE range .4 - .9 volts

c) Resistor variations 15%

d) 7.82K = (R61 + 15%)
16.5K = (R62 and R43 in parallel -15%)

e) Using nominal voltages and the resistor values cited, the base voltage of Q21 equals 3.8V + (VBE min of Q18 and Q20) = 4.2V.

f) 10% voltage variations yields:

6V - 10% = 5.4V (Δ V = .6V)
3V + 10% = 3.3V (Δ V = .3V)

g) Using the above voltages, the new figure for the voltage at the base of Q21 is:

4.2V nominal
-.6V 15% ΔV
3.6V

h) The difference between the base and emitter voltages is:

3.6V base voltage
- 3.3V emitter voltage
.3V difference in the reverse bias direction

i) Voltage needed on the base to forward bias the base-emitter junction of Q21:

3.3V
- .4
+2.9V on base

A back bias of approximately .3V + .4V or .7V is present on the base of Q21 under worst case conditions. Under normal conditions back bias of one or more volts will be present at the base of Q21.

The modified circuit has approximately 1 volt of noise immunity using 10 percent voltage variations and 15 percent resistor deviations. This is ample protection against Q21 turning on under worst case conditions. The system was run at temperatures up to +60°C with these modified shift register modules, and all circuits functioned well.

2.3.1.2.5. Coder 1 Filter Network and Voltage Ripple Problem

Just before going into Phase I thermal vacuum on the Flight II System, a problem occurred in PCM 1 which required the opening of the PCM unit for troubleshooting. It was not necessary to disassemble the stack. Word 3, in almost all subframes, appeared randomly in error by approximately 20 mv. Further investigation showed that other words in the subframes were also randomly in error but by a smaller amount, and thus word 3 was the first to show up as an error on the BTE. The problem was diagnosed to be one of random offset between

words. At first, the problem was believed to be isolated to PCM 1, but careful investigation uncovered the fact that PCM 2 also had this characteristic though to a much lesser degree. The coder modules in PCM 1 were investigated thoroughly. Several parts were replaced in the calibration loop (Q37, Q38, and Q20). Coder modules were interchanged with those on Flight 1, but no major improvement was noticed. The coder modules were then completely removed from the system and placed in the coder test fixture. Since the coder test fixture contained its own DC/DC converter to run the coder, all that was needed from the system was encode-calibrate commands and the PAM line. The outputs from the coder were fed back into the System and read out on the BTE in the normal fashion. In the coder test fixture (running from the separate power supply) all worked well. One at a time the voltages running the coder were changed back to system power. When +15V system power was changed back to the coder, the random offset between words appeared. Looking at the +15V P.S., it was noted that the ripple was twice as high on PCM 1 as PCM 2. At first the power supply was suspected and another power supply was installed in PCM 1. The other power supply decreased the offset between words but did not cure the problem altogether. A power supply from Flight 1 was installed and the offset between words was at least as good as PCM 2. An investigation of the coder 1 modules showed that a filter network installed in the correction circuit of the constant current source, used to discharge the ramp capacitor, was arranged in such a way as to feed any ripple directly onto the correction circuit of the constant current source (see figure 40). Furthermore, the constant load on the +15V power supply was only about 1 ma with a 5 ma duty cycled load. This caused the RC network in the 15V power supply to have a peak detecting action, thus increasing the ripple seen by the coder 1 module. Several methods of correction were discussed but the simplest approach was to increase the current through the resistor divider network and change the reference of the filter capacitor (see figure 40). The modification (Reference ECO 0320219 dated 16 November 1967) was installed in both PCM 1 and 2 coders and although some offset between words still exists (approximately 4 - 5 mv), it is not considered a problem. The ripple on the +15V line of the original power supply was not out of spec. even though it was twice as much as that on some of the other power supplies. The differences between the power supplies can be caused by slightly different transformer, rectifier, or preregulator characteristics which affect the impedance of the power supply. This would normally not be a problem but because the power supply had a very light load, these differences became more apparent in the form of ripple. This coupled with the filter capacitor being referenced to +15V, caused the slope of the ramp to change slightly during the subframe. (Word 3 follows the sync and ID words in each subframe). Power supply loading and noise are no doubt worse in this area, causing word 3 to have a little greater offset than other words in the subframe.

Why this problem was not isolated sooner can only be surmised. It had been noticed that the coder in PCM 1 took a negative offset after vibration but since the shift did not put the coder out of specification limits, no action was taken. This negative offset coupled with some power supply aging may have brought the problem to light. Since all channels are not individually checked for offset and since the problem was of a random nature, it could have been present to a lesser degree before going into environmental testing but it was not detected. The power supply is about the only element in the system that could cause offset from one word to the next; however, in this case the power supply is not totally to blame.

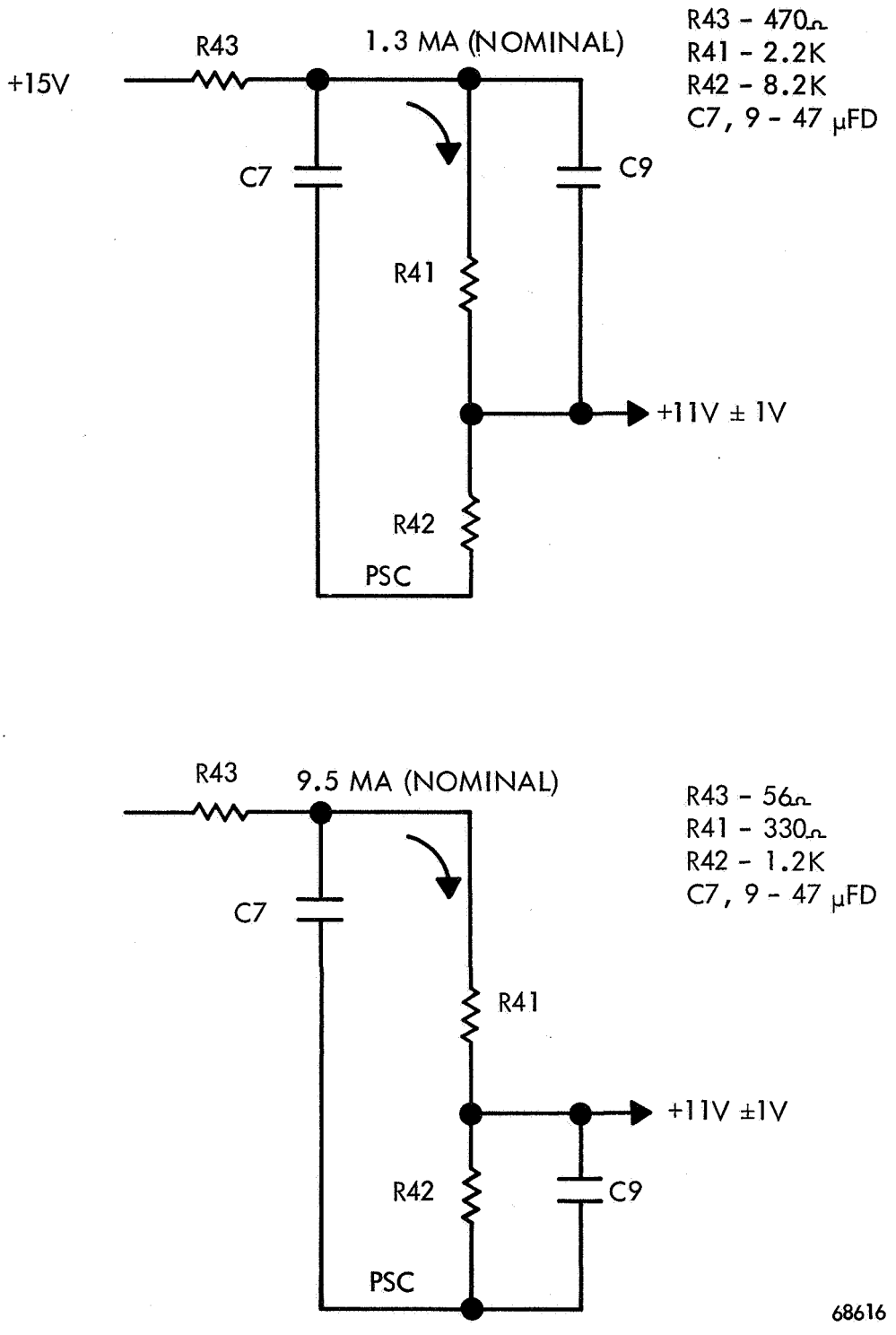


Figure 40. Coder 1, Filter Network

2.3.1.2.6. CODER NO. 2 DESIGN IDIOSYNCRASY. A design idiosyncrasy was discovered during system testing at G.E. concerning the coding of full scale analog words by the ramp coder. The anomaly was discovered when a voltage, near the exact full scale voltage (± 6 mv), was applied to several analog channels. Instead of reading a stable code of all ONES these words would randomly drop to an all ZERO code. Further investigation revealed that all analog channels, given enough time, would exhibit this problem if the input voltage were adjusted to the critical point.

At first it was believed that the zero detector was at fault. Since the anomaly was voltage dependent it was theorized that perhaps the zero detector was going into its linear region due to a critical ramp voltage and internal noise on the ramp. It was evident that there existed a condition whereby noise on the ramp could cause a sweep action of the zero detector allowing it to bounce off and on. Any oscillatory action by the zero detector would introduce additional transitions into the counters. It was realized that only one such transition appeared to be present since the words with the full scale voltage would drop to zero; however, since the linear region of the zero detector is very narrow, this could have been possible. Additional tests were requested at G.E. These tests involved introducing noise into the system and measuring the range of the input signal that would cause the output to drop to an all zero code. The results of the test were negative and the zero detect theory was discarded.

More investigation into the coder, plus added information from NASA uncovered a design idiosyncrasy in the counter gating circuit. This circuit is made up of Q12, Q13, Q33 and Q42 in coder module II (Figure 34) and controls the 500 KC clock to the counters. When the analog input voltage is approximately equal to the full scale voltage there exists the possibility of the zero detect pulse arriving first before the full scale pulse from the coder counters. If this happens the sequence of events is as follows:

a. The zero detect pulse arrives at (GG) and causes Q33 to turn on. When Q33 turns on it clamps the base of Q12 to ground and allows the collector of Q12 to go high.

b. The full scale pulse arrives at (CC) and causes Q42 to turn on. When Q42 turns on it clamps the collector of Q12 to ground.

c. The counters switch on negative transition from the gating circuit. Thus when the collector of Q42 pulls to ground an extra transition is sent to the counter. This extra transition causes the counter to change from an all "ones" code to an all "zero" code since the "carry" is not recorded.

d. Since the system depends on a full scale pulse to change from analog to digital operation and since the coder counters which furnish this pulse are now reading all zeros, the system remains in the analog state. The counters are read directly when the system is in the analog state and the all zero code is transferred directly into the data stream.

The exact analog input voltage where this condition occurs may vary slightly from word to word. This is because it is dependent on the last set of calibration cycles. The calibrate cycles determine the amount of time difference between the zero detect pulse and the

full scale pulse. If there were no errors in the coder loop the zero detect pulse and the full scale pulse would be coincident. This will never be the case, however, as a small amount of error is always present. It is evident that the zero detect pulse always leads the full scale pulse by this small amount. When the analog voltage is greater than the full scale voltage of the coder (by about 50 mv) it does not drop the all "one" code. This is because the ramp capacitor is charged to a voltage greater than full scale. This guarantees that the full scale pulse arrives before the zero detect pulse. Q42 still clamps the collector of Q12 to ground. However, the collector of Q12 was already at ground due to the 500 KC clock input to the base of Q12. The time delay between the negative going transition, which changed the counter to an all "ones" code, and the full scale pulse, created by the all "ones" code in the counter, is less than 1/2 the period for 500 KC and no extra transitions are fed to the counters.

The anomaly was not observed earlier because an automated test set was not available to run a continued check on the system during all modes of operation. Since the anomaly was random and the input analog voltage is critical it was never observed during any of the system tests at Radiation. Actual interface with the ground station and the aid of computer print out available at G.E. and not at Radiation helped to uncover this anomaly.

The coder anomaly could easily be corrected by modification to coder module II. Since all units have been through environmental testing, and since no system degradation in life or performance except at this one point will occur, it was recommended and decided upon that no action be taken to correct the problem.

2.3.2. MECHANICAL PACKAGING DESIGN CONSIDERATIONS

There were no changes in the external mechanical characteristics of the PCM Unit between the Engineering Model and the subsequent Prototype and Flight Models. The only differences have been internal, and they were the following:

a. Wire potting

b. Preload

c. Housing dimension changes

d. MOSFET

2.3.2.1. WIRE POTTING. For ease of troubleshooting, the soldered interconnect hard wiring was not encapsulated nor restrained. To insure the protection needed during exposure of the Prototype and Flight Models to the dynamic environments, these areas were potted with RTV 521 silicone compound.

2.3.2.2. PRELOAD. Since the Engineering Model incorporated some last-minute changes which meant using some oversized components and multiple-use jumper wires, the preload applied to that unit was such as to preclude movement of the electronic components during normal handling and usage, but insufficient to provide protection against the dynamic environment. The Prototype and Flight Model systems have had the changes properly incorporated into the systems, and are preloaded to the proper value necessary for environmental protection.

2.3.2.3. HOUSING DIMENSION CHANGES. One unanticipated mechanical problem did manifest itself, however, in the magnesium housing. These units were procured from an outside vendor. Upon shipment from the vendor, and again upon arrival at Radiation Incorporated, the physical measurements of the housings were taken. All the measurements showed that the housings were of the correct dimensions and within the tolerances allowed. However, upon packaging the units, the final dimensions were found to be out of the allowable specification limits. The unit was disassembled, and the housing remeasured. It was found that the housing dimensions were no longer within tolerance. Upon examination of the housings for subsequent units, it was found that they were also out of tolerance.

It was found that the machining process had caused internal stresses in the housing which had relaxed while sitting on the shelf, resulting in the out-of-tolerance conditions.

By consulting with metallurgists familiar with magnesium, it was found that the stresses could have been relieved by a thermal stress relieving plan implemented during and just subsequent to the machining of the housings. In addition, there was a fairly high probability that the present housings could be brought back within acceptable tolerances by precision fixturing and heat treating. However, there were several drawbacks to this approach:

a. The sandwiched foam will be burned and lost due to the high temperatures required (500°F).

b. The high temperature would degrade the housing finish (electroless nickel), requiring a stripping and replating process.

c. In order to heat treat the housings, the stainless-steel inserts must be removed. Once removed, a very high probability exists that one or more holes may be stripped, thereby precluding the possiblity of inserting and seating new stainless-steel inserts.

d. The minimum turn-around cycle to completion would be six weeks.

Due to these new developments, it was felt to be in the best interests of the program to determine if the units could successfully fit into the spacecraft and, if so, to forward those units for delivery with NASA concurrence. The course to follow on those units which could not fit into the spacecraft would be determined on an individual basis.

2.3.2.4. MOSFET DEVICE PROBLEM AND SOLUTION. This paragraph discusses the two major problem areas concerning the metal-oxide-semiconductor field-effect transistor (MOSFET), 5-channel Multiplexer used in the Nimbus B PCM Telemetry Systems.

One of these areas concerned difficulties in handling procedures and the other concerned failures of the MOSFET devices during environmental testing as a result of particle contamination. The failures of the MOSFET devices resulted in a delay of almost six months in the program.

2.3.2.4.1. SELECTION OF GENERAL INSTRUMENT MOSFETS FOR THE FLIGHT SYSTEMS. MOSFETs are extremely susceptible to damage caused by static charge. Static charge generated by friction in handling is sufficient to destroy a unit so to prevent this type of damage a handling procedure was generated (Radiation Drawing 110174, Handling and Shipping Flatpack and MOSFET devices) that outlined all special requirements for both the vendor and Radiation Incorporated personnel.

The major supplier, Fairchild Semiconductor, was unable to protect the units adequately during handling and they therefore had a high destruction rate. The excessive fallout seriously threatened the production schedule, thus necessitating a search for a second source. It was determined that FSC flatpacks have a potentially dangerous internal design. The mounting of the chip to the header and the subsequent wire bonding and routing creates a potential problem of inadvertent shorting, particularly when exposed to vibration.

In fabricating this part, gold whiskers are bonded to the chip, then to the bonding pad (see figure 110). After making the chip bond, the gold lead must be drawn upward, across, then down below the chip surface to the printed circuit pad. The printed circuit pad is on the same level with the molytab, thus proper fabrication relies heavily on operator dexterity to keep the gold lead from being able to short to an adjacent lead or the molytab.

The problems with Fairchild P/N 106510 MOS flatpacks were complicated by the difficulty of determining those which are poorly made, after the part is complete. Normal radiographs will not clearly show how close the gold leads are to the molytab. Therefore, with only the potential lead to lead shorts being found a part cannot be considered reliable.

This, in addition to the above, and extremely poor deliveries led to the discontinuation of FSC as a supplier for MOSFET flatpacks for the Nimbus B PCM telemetry.

General Instrument Corporation (G.I.) of Hicksville, L.I., indicated promise as a potential supplier because of development work on a 5-channel MOSFET. Negotiations were inaugurated to develop a circuit that would be interchangeable with the Fairchild circuit. General Instrument's plant, production procedures, and quality control procedures were surveyed and found to be inadequate for production of aerospace components. Radiation and G.I. personnel met on several occasions to revamp production and quality control procedures so that fabrication of the circuits could begin. General Instrument Corporation (G.I.) was ultimately selected as the source of supply for this item, as was discussed in the "Addendum to Final Report for Nimbus Design Study".

Only G.I. devices were used in the Flight Systems. It was not considered necessary to replace the Fairchild devices in the prototype model, and as a result this model contains a mixed quantity of Fairchild and G.I. devices.

The G.I. device, manufactured by the General Instrument Corporation, in Hicksville, New York, incorporated five P-channel MOSFETs in a single, fourteen-lead, 1/4 in. x 3/8 in. Kovar-and-glass package. The 110245-2 part number assigned to these units designates a Radiation specification to which the devices are purchased; this specification requires various electrical and environmental testing and screening.

The active element of the 110245-2 is a 0.040 x 0.030 in. silicon chip in which the five MOSFETs have been constructed by essentially conventional planar technology. The chip is attached by eutectic bond to the gold-flashed bottom of the Kovar package. Interconnections between the aluminum contact metallization on the chip and the internal stubs of the package leads are effected with small (approximately 1-mil dia.) gold wires, attached at the chip with thermocompression ball bonds and at the lead stubs with thermocompression wedge bonds. (Only twelve of the fourteen package leads are used for the 110245-2.)

In some devices, a six-MOSFET chip is used, and, in these, the extra MOSFET is short-circuited to the package bottom with gold wires.

Although G.I. obtains the device packages from three different package manufacturers, it was reported that all units supplied to Radiation Incorporated had been fabricated with packages manufactured by Seal-a-metic, Incorporated, in Haledon, New Jersey. Details of the package construction are as follows:

a. The Kovar package bottom is placed in a recess of a carbon block.

b. A slurry of 7052 glass is placed over the package bottom, and a lead frame (containing all fourteen leads) is positioned in this slurry. A Kovar ring is placed over the top edge of the slurry, and a monel-metal weight is used to hold the package bottom, slurry, lead-frame, and ring in this configuration.

c. The package constituents, held in the carbon block as described above, are fired at +1700°F. During this operation, the 7052 glass tends to withdraw from the center of the package bottom.

d. After firing, extraneous (hardened) glass is removed from the package leads and, if necessary, from the package bottom, using an aluminum oxide abrasive. The Kovar parts of the package are subsequently gold-flashed.

This package is supplied with a gold-flashed Kovar lid, as well as with a gold/tin preform which is used to solder the Kovar lid to the Kovar ring of the package. G.I., after installing the semiconductor chip and internal interconnection wires, solders the lid in place at a preform temperature reported to be +281°C.

2.3.2.4.2. MOSFET FAILURE DURING FLIGHT I ACCEPTANCE TESTING AND SUBSEQUENT ANALYSES. Serious problems with the G. I. MOSFET devices started during the vibration acceptance testing of Flight System I, the first system using only the G. I. MOSFETs.

The failures became evident during the vibration test of a subassembly containing 298 of the devices. During the vibration test, 10 devices out of approximately 20 that were monitored exhibited failures due to shorts. These shorts occurred only when the packages were vibrated in the Y_1 direction (a direction normal to the plane of the lid with the package either right side up or upside down). No failures were observed when the subassembly was vibrated in other planes.

Highlights of the exhaustive analyses and investigations conducted separately and concurrently at Radiation Incorporated, General Instrument, at Cape Kennedy, and at GSFC (detailed in Radiation's document entitled "Sixteenth Monthly Progress Report - NAS5-10139, No. 1210-4180-132, dated 21 July 1967 and in NASA Failure Analysis Section Report, Serial No. 779, dated 31 August 1967, entitled "Investigation of Particles in General Instrument Type 110245-2 Semiconductor Device Sets") are summarized in the following subparagraphs.

During the investigation carried out by Radiation Incorporated 45 devices which had previously failed a burn-in test were studied. Of the 45, 13 were rejected during X-ray inspection for suspected contamination; of these, six were submitted to the GSFC Failure Analysis Section. It was requested that these six units be examined for particle contamination.

Preliminary failure analyses conducted by Radiation and G.I. revealed the presence of extraneous particles in the packages of the failed semiconductor device sets. It was found that these particles were in some instances conductive, large enough to short circuit the contact metallization on the semiconductor chip, and free to move within the package. It was concluded that the particles were the cause of the subsystem failures.

A sample analysis conducted on the MOSFET device A16, which failed in third vibration and subsequently cured itself after the system was temperature cycled, was presented to GSFC and demonstrated the following:

a. Electrical test revealed gate-to-drain and gate-to-source short.

b. The device was X-rayed seven times and a particle was noted on only one X-ray.

c. Autopsy was performed and a particle was visually detected and measured (3.9 x 2.8 mils), confirmed to be conductive and was loose within the package.

d. A short was induced in the good device gates by placing the particle on the chip metallization. The failure disappeared when the particle was removed.

A second failure analysis was presented of a device, selected at random, from the latest units received from General Instruments. The purpose here was to determine the extent of the problem. (The problem is evident with all devices in house as witnessed by particle contamination being found in devices date coded 6645 through 6718.)

a. X-ray of this device did not reveal particles.

b. Autopsy revealed a conductive particle 5 mils in length.

A third analysis was presented of a device which contained a loose gold particle and what was more interesting was the fact that disappearing aluminum and "purple plague" was evident on the device chip. As a result, Radiation felt that some gross leak hermeticity tests were necessary. These hermeticity tests were performed on several gross leakers found.

A fourth item was presented showning the results of the particle analysis conducted by the NASA laboratory at Cape Kennedy.

The following materials were found within the G.I. MOSFET units. (The materials were identified from particles extracted from the units.)

a. Iron alloy with a small amount of manganese
b. Sodium
c. Silicon and iron
d. (1) Aluminum
   (2) Chlorine
   (3) Titanium
   (4) Potassium
   (5) Copper
   (6) Nickle
*e. Gold

One of the materials listed under Items a, b, c, and e was contained in the particles and comprised the major constituent. The items listed under Item d were also found in lesser quantities and comprised 1 to 10 percent of the particle.

Subsequent to the presentations discusssed in the preceding paragraphs, an investigation, finally and conclusively, proved that the most significant particles were causing the devices to short circuit. A flatpack under inspection was found to have a particle across the leads, causing a short circuit in the device. Subsequent investigation also revealed that the most probable source of contamination was at the source of manufacture of the flatpack, Seal-a-Metic and was introduced into the package during the abrasive cleaning process. This investigation also revealed that the G.I. receiving inspection process was inadequate to discover the particles, e.g., Microscopic examination of 30X is not adequate to reveal the particles and also, X-ray was proved not to be an effective screen.

During the GSFC Failure Analyses Section investigation, techniques were developed which minimized or eliminated the introduction of contamination during package opening. Five of the six submitted units were successfully opened by these techniques. Of the five units, two were found to contain no foreign material visible at magnifications up to 400X. The three remaining units were found to contain numerous particles having maximum dimensions which ranged from a fraction of a mil (typical) to approximately 5 mils (one particle). A detailed description of the techniques developed and used and the findings are contained in the GSFC Failure Analysis Section Report referenced above.

A discussion of the conclusions and recommendations resulting from these investigations is presented in the following subparagraphs.

* Identified at Radiation, not at the NASA facility.

2.3.2.4.3. CONCLUSIONS AND RECOMMENDED SOLUTIONS. A summary of the conclusions reached by the team of investigators including Radiation Incorporated, General Instrument and NASA (although the Failure Analysis Section Investigation was not made specifically to prove that the G.I. MOSFET had caused the PCM Telemetry Subsystem failures) are as follows:

a. The G.I. 110245-2 package can be opened for visual inspection -- using special techniques -- without the introduction of foreign particles as proved by the investigation carried out by the GSFC Failure Analysis Section.

b. Appearance-wise, the particles observed by the investigating teams were similar in description (by Radiation Incorporated after exhaustive failure analyses of many units and subsequently by NASA personnel after a NASA survey of the G.I. manufacutring facility). The particles also appeared similar to those found in unsealed packages obtained directly from Seal-a-metic by the GSFC Failure Mechanisms Group.

c. The particles, including those which were either partially or totally imbedded within the glass lead frame, appeared to be distributed randomly. However, the "clean" package-opening technique precluded tests which might have determined whether the particles in the open areas of the package had been mobile.

d. The particles were in many instances large enough (in some cases 3 to 5 mils in length) to span the space between gate and drain (or source) metallization stripes (0.3 to 0.5 mil). In several instances, the particles were also large enough to contact simultaneously the drain and source metallization stripes (across the gate stripe). A Radiation test did discover a particle crossing the leads in one flatpack under analysis.

e. Of the four particles analyzed, by the NASA Failure Analysis Section, three were probably metallic and therefore conductive (it is concluded that the fourth particle, which evaporated during electron probe analysis, was made up of organic materials). It should be emphasized that the electron probe microanalyzer is useful for identification of constituent atoms, but would not disclose the presence of -- as an example -- iron oxides. The evidence obtained during visual examination, however, indicated that the cores of three of the particles were metallic. The outer shells of these particles appeared nonmetallic; this may have been due to a) rough surface textures and/or b) overlying metal oxides; either of these conditions could have arisen from high temperatures incurred by the particles during package manufacture (at Seal-a-metic) or device fabrication (at G.I.). Radiation Incorporated analyses revealed that many of the particles found were indeed magnetic.

f. The origin(s) of the particles has been determined. It was found that they probably originate from the carbon blocks or monel-metal weights used during package fabrication at Seal-a-metic, from both abrasive and solvent materials used for processing and cleaning the packages at Seal-a-metic, and possibly from various sources at G.I.

The recommendations to alleviate the problems caused by the contaminated MOSFETs fell into two basic categories:

a. Elimination of the failure modes in the Flight Systems to continue with the test program.

b. Preclusion of failures by particle contamination by an effective 100 percent source inspection procedure.

A fix to the Flight System failure problems was recommended by General Instrument. The suggestion was made to utilize a new pyrolytic MOSFET device to replace the non-pyrolytic device which was causing the failures. Even though the new devices are constructed with flatpacks from the same source, the glass technique aids in the elimination of metallization scatches and, as a by-product, the glass prevents shorts due to foreign particles less than 3 mils in largest dimension. The pyrolytic process uses silicon over the entire area except bonding pads. The bonding pads are etched with a controlled etch that will not attach aluminum. It was decided to adopt this solution and reassemble the flight systems with pyrolytic devices. However, in addition, the new pyrolytic devices would have to undergo qualification testing (the results of which are included as Appendix III to this report) and GI would have to institute an adequate receiving inspection and handling process to screen out contaminated flatpacks, pyrolytic and nonpyrolytic. The procedures instituded include:

a. 100X microscopic examination

b. Establish of clean room maintenance program and personnel indoctrination

c. 100% monitored vibration screening on nonglassivated devices

d. Cleaning incoming flatpacks if necessary

e. Ultrasonic cleaning of all flatpacks three times followed by 100% visual inspection until flatpacks from suppliers can be cleaned up.

2.3.3 ELECTRICAL PACKAGING

Two items in the electronics packaging area were changed in the Prototype and Flight Models from those used in the Engineering Model. These areas are discussed in the following paragraphs:

2.3.3.1. Z NETWORKS. The Nimbus Engineering Model PCM utilized Zener diodes in the body lead of the MOSFET gates to provide protection against positive overvoltage; however, when operating near ground potential, the problem of the pulse feeding back was still present. (Refer to paragraph 2.3.1 of this report for a detailed discussion of this problem.)

To preclude this situation occurring, a Z (RC) network was located between the MOSFET body terminal (in place of the Zener diodes) and the +6-volt terminal. This network provides the required overvoltage protection, as well as a low impedance reference point for the body through the use of a Z network assembly which replaced the Zener diode. The assembly was made by placing a 100 K ohm, 1/8-watt resistor "piggyback" on a 470 pf, 100-volt capacitor and welding their leads to the common riser wires. This assembly was then

inserted into a mold for encapsulation in an epoxy resin. Following part marking and testing, the Z network was assembled into the system.

2.3.3.2. SINGLE PIN CONNECTORS. During checkout of the PCM, the cards in the system are spread apart for ease of access to the planar-mounted components on the cards. Since portions of the PCM are cross-strapped, it was necessary to have the 35 wires which interconnected the two ends of the system a minimum of 36 inches long to enable full system operation during checkout. Since the assembly sequence requires the interconnecting hard wires to be potted prior to system checkout, and since it is impossible to remove and replace the long wires when the system is compressed down to its normal size, a problem existed on the excessive interconnect wires. The bulk of the wire did not allow it to be coiled up and positioned between the cards and the front panel, and the cutting and splicing of these wires (as was done on the Engineering Model) was not allowed by the NPC-200-4 specification.

To solve this problem, a single-pin connector, almost identical to one that had been previously qualified on missile harness wiring at the Goddard Space Flight Center (NASA), was investigated. This connector incorporates a spaceflight-proven positive contact retention system, withstands the dynamic environment it would be exposed to, and utilizes spaceflight-approved materials. Its size is ideal for incorporation into the wire harness area, and the fact that the contacts are crimp insertable and removable made it easier to assemble, disassemble, and troubleshoot the assembled PCM at various stages between checkout and insertion of the electronics unit into the housing.

2.3.4 COMPONENT DIFFERENCE BETWEEN THE QUALIFICATION AND FLIGHT MODEL SYSTEMS

Flight Systems 1 and 2 utilize the new pyrolytic MOSFET devices and use the MOSFETs supplied exclusively by General Instruments. The Qualification Model uses both Fairchild Semiconductor and General Instrument MOSFET devices and is constructed using the original nonpyrolytic MOSFET design.

SECTION III

TELEMETRY ELECTRONICS UNIT

SECTION III

TELEMETRY ELECTRONICS UNIT

3.1 INTRODUCTION

This section of the Nimbus B report describes the Telemetry Electronics Unit (TME) and provides a general description of the TME electrical model. The description includes a summary of the major physical and electrical characteristics of the TME. This section also discusses the modifications that were required, and the electrical and mechanical design considerations involved in the incorporation of the modifications into the TME.

3.2 NIMBUS B ELECTRICAL MODEL GENERAL DESCRIPTION

The Nimbus B TME Unit shown in figure 41 accepts Mark 0 split-phase data from the Nimbus B PCM Unit and Nimbus C clock time codes and then basically acts as a relay switching network and singal amplifier between the PCM unit and output transmitter and tape recorders, and between the Nimbus C clock and output transmitter. In regard to this overall purpose, the TME unit performs four distinct functions: (1) upon command, switches serial split-phase Mark 0 data routing from the PCM unit to the tape recorders for temporary storage or to the transmitters for real-time data transmission or to both simultaneously; (2) upon command, switches data playback from the tape recorders; (3) provides for MM10A time code transmission either superimposed on the real-time data or separately; and (4) provides externally adjustable controls for transmitter modulation.

The TME unit provides almost complete circuit redundancy. The record amplifier, playback amplifier, and summing amplifier are block redundant. The passive summing network and relay armature coils are nonredundant. A simplified block diagram of the TME unit (figure 42) illustrates the redundancy technique used. As shown, the summing network and relay switching circuits are nonredundant while the summing amplifiers, record amplifiers, and playback amplifiers are block redundant. The GFE supplied tape recorders and transmitters that interface with the TME unit are also redundant. The two tape recorders are independently controlled so that neither, either, or both can be used at one time. Monitor circuits are provided within the TME unit to monitor temperature and operating modes.

The TME unit can modulate the transmitter with time code from the clock, or can mix the time code with real-time output data from the PCM unit, and at the same time can record this PCM data on two tape recorders. The transmitter real-time information provides a beacon signal, while the tape recorders store data when the satellite is out of range of a ground receiving station. Each tape recorder is capable of storing the data accumulated during one orbit, and a 30:1 playback speed to record speed ratio enables rapid transmission of recorded information while the satellite is within range of the receiving station. The record time for each recorder is approximately 108 minutes; the playback time is approximately 3.6 minutes. The two tape recorders provide 2-orbit storage capability by turning off one recorder (by ground command) at the end of the first orbit, and letting the second recorder store second orbit information. Then the two tape recorders are dumped (by ground command) sequentially during a 7.2 minute interval over a receiving station.

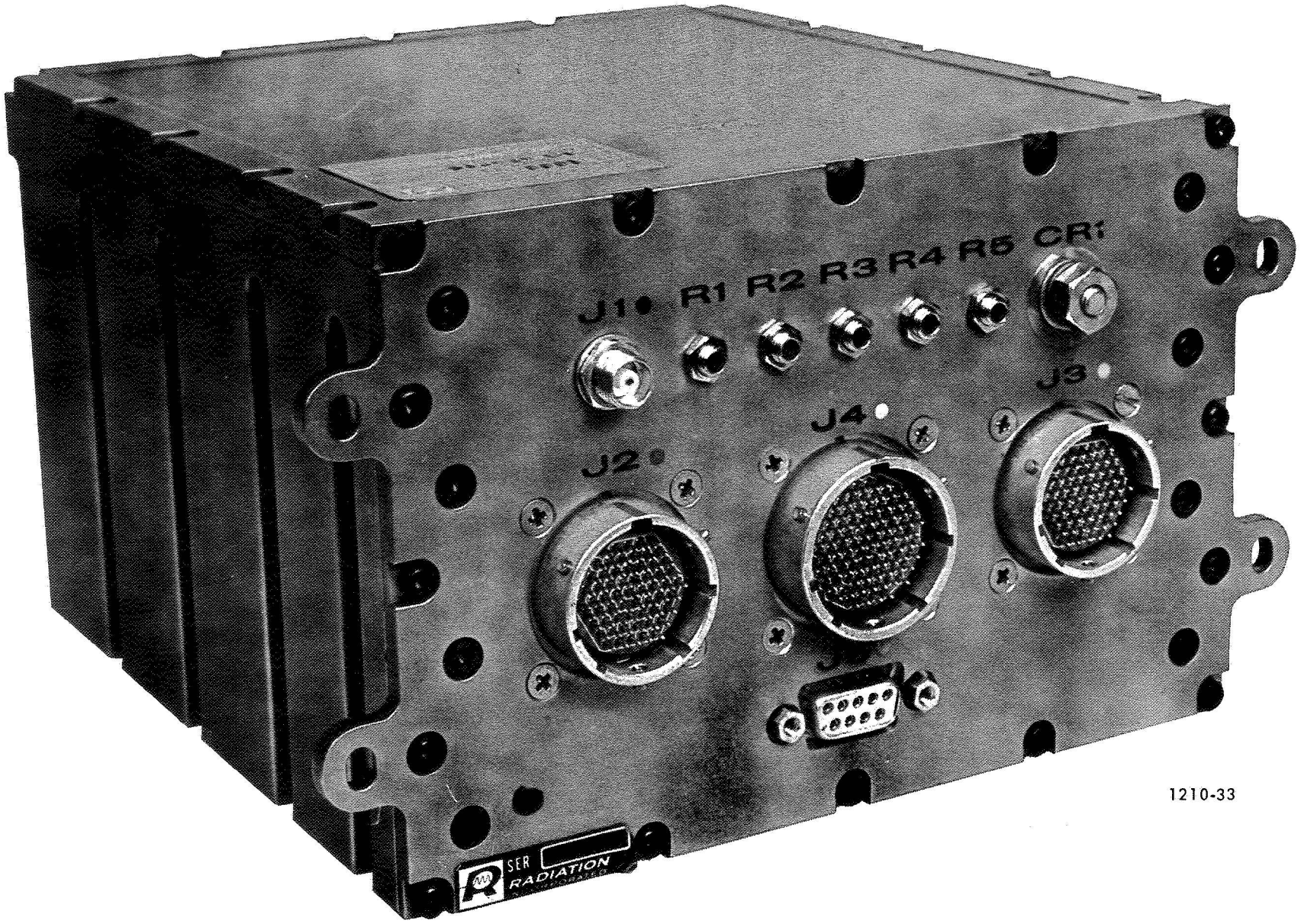


Figure 41. Telemetry Electronics Unit

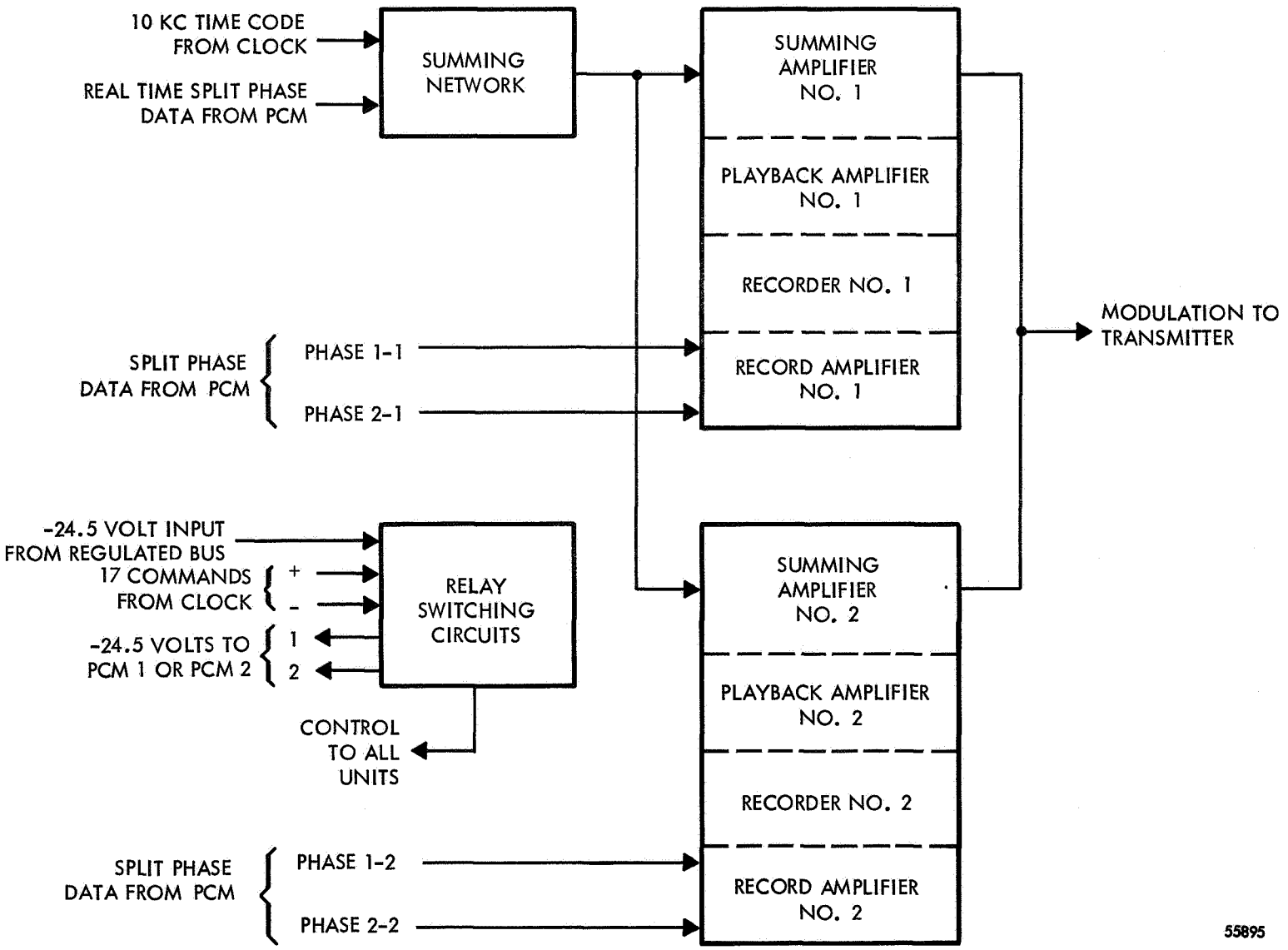


Figure 42. TME Unit Simplified Block Diagram

The TME unit command switching relays present a single coil interface to the Nimbus C clock. Both ends of all coils are floating with respect to each other, and with respect to -24.5 volt power and return. Additional relays isolate clock commands from the circuits they control in the two tape recorders. For example, the tape recorder automatically generates a pulse to switch the TME unit relays back into the record mode at the end of the play-back function initiated by ground command. This automatic pulse directly operates a TME unit relay; therefore, an isolation relay is provided to achieve maximum isolation between the clock commands and all subsystem power and power-return lines.

There are two record amplifiers, one connected to each of two tape recorders, to saturate the tape with the split-phase Mark 0 data. Each record amplifier is connected to only one record head and tape recorder. The single record/playback head in the recorder is switched between the record amplifier output and the playback amplifier input. Since the record amplifier is of the saturated type, current is always flowing in the head winding and the magnetic tape particles are always being aligned in one of the two possible directions. The inputs to the two record amplifiers are isolated in the PCM unit by separate output resistors so that each record amplifier effectively has its own driving source.

Two playback amplifiers are provided, each one being connected to a separate record head through the record/playback switching relay described above. The input data frequency from the recorder is 7.5 kc for all data ZERO's and 15 kc for all data ONE's because of the 1:30 increase in tape speed from record to playback. The input voltage is approximately 40 millivolts, peak-to-peak.

The summing network and summing amplifier combine the different signals programmed to modulate the beacon transmitter. The summing network is passive and nonredundant. There are two input/output block-redundant summing amplifiers operated as class A amplifiers that provide maximum signal isolation in the event of a failure.

The relay switchable operating commands are use summing amplifier 1 or use summing amplifier 2. One summing amplifier must be on at all times since the 10-kc modulated time code is used as a beacon and is transmitted during the major portion of the orbit time (except during recorder playback) through one or the other of these summing amplifiers.

Only the input and output signals are relay switched and the power line is returned to the -24.5 volts regulated bus so that both summing amplifiers have power whenever power is applied to the TME unit. The outputs applied to the summing network are:

a. Ten kc time code from clock (MM10A).

b. Time code plus PCM real-time data.

c. Playback data from recorder 1.

d. Playback data from recorder 2.

e. Time code emergency bypass.

There are five telemetry monitor points in the TME unit. One is TME unit internal temperature and must be applied to an analog channel gate in the PCM unit. This circuit is identical to the two PCM unit circuits. The remaining monitor points are applied to digital channels within the PCM unit and verify, in real-time, that the relays have received the following commands from the clock and have switched to the new position.

a. Recorder channel 1 - power on (power on produces a data ONE and power off produces a data ZERO).

b. Recorder channel 2 - power on (power on produces a data ONE and power off produces a data ZERO).

c. Recorder 1 - record mode (record mode produces a data ONE and playback mode produces a data ZERO).

d. Recorder 2 - record mode (record mode produces a data ONE and playback mode produces a data ZERO).

3.2.1 MAJOR PHYSICAL AND ELECTRICAL CHARACTERISTICS.

This paragraph outlines major physical and electrical characteristics of the current improved Nimbus B TME Unit. Descriptions cover physical dimensions of the unit and the mechanical and electrical packaging concepts employed in its manufacture. Printed circuit card packaging, interconnecting, reference designations, and their relative locations within the assembly are discussed. In addition, signal characteristics of the TME are tabulated describing their functions and operating parameters.

3.2.1.1 PHYSICAL CHARACTERISTICS. Table 5 contains a listing of the primary TME physical characteristics. The TME unit consists of a cabinet enclosure that contains three multilayer printer-circuit cards. These cards are hard-wired to connectors for interface cabling. Modules, relays, and piece parts are mounted on the cards with hard-wiring used for circuit connections. The TME unit contains the following modules and assemblies:

b. Two playback amplifiers.

c. Two summing amplifiers.

d. Five signal monitor circuits.

e. Seventeen control relays.

f. Five gain controls and zener diode.

g. One coaxial, two 61-pin male, one 85-pin male, and one 9-socket female connector on the front panel.

Table 5. TME Physical Characteristics

Characteristic	Nimbus B
Size	4 in. x 6 in. x 6.5 in.
Weight	4.25 lb.
Housing	
Design	Closed Box
Finish	Electroless Nickel
Connectors	
Manufacturer	Deutsch, Cannon (Multipin) GRFF (Coaxial)
Type	Standard Types
Environmental Protection	Yes
Locking Device	Bayonet-lock Screw-lock Screw-on
Packaging Concepts	
Printed-Circuit Card Type	2-sided and 4-layer M/L
Internal Connections	Hard-wiring
Internal Vibration Isolation	Yes
Compression-loaded	Yes
Component Packaging	Modular and Planar

The record/playback amplifiers, two summing amplifiers, and monitor circuits are located on one cordwood-type modular assembly in the center of the TME unit.

The relays are mounted on two printed-circuit cards with eight relays on card No. 1 and nine relays on card No. 2. All relays provide DPDT contacts. Thirteen relays are the magentic latching type, and the remaining four relays are standard nonlatching type.

The five gain control potentiometers are accessible at the front panel for adjustment of modulation levels into the transmitter.

The zener diode is located on the front panel of the TME unit for convenience only and is used to provide overvoltage protection for the PCM unit multiplexer.

Connector J1 is a TNC coaxial connector for the TME unit output signal to the transmitter. Connector J2 provides connections for -24.5 vdc PCM unit emergency power, -24.5 vdc temperature sensors, chassis grounds, six (-24.5 vdc) lines from the Nimbus regulated voltage bus, and analog and digital signal grounds. Connector J3 provides connection for 17 relay commands, clock, and timing signals. Connector J4 provides connections to the PCM unit and to each tape recorder. Connector J5 provides PCM and TME monitor points.

As with the PCM, the packaging concept for the TME unit utilizes a compression-loading technique that places the electronic under a load using light-weight polyurethane foam potting and spacer material. The resultant package provides protection to the electronics from the exposed dynamic environments.

3.2.1.1.1 MECHANICAL PACKAGING. As with the PCM, the TME unit consists of a preloaded electronics assembly. This technique effectively integrates the electronics into one mass, allowing use of a thin-walled light-weight housing design.

The housing assembly consists of three separate parts; the housing bottom, cover, and front panel. The housing bottom is fabricated by machining of a monolithic magnesium block. The cover is a hollow magnesium panel which, when filled with foam and rigidized by a bonded-on plate, forms a rigid light-weight structure capable of withstanding the bending moments caused by preloading. The front panel is a machined magnesium plate that provides support of the TME in the spacecraft and provides mounting for the external connectors, fault protection diode, and variable resistors.

Internally, the relay card assemblies, the shield cards, and the module card assembly are separated by both foam and fiberglas loading shims. This grouping is isolated from the housing bottom and housing top cover by foam silicone rubber strips which provide vibration isolation. The strips also provide resonance control by contacting the perimeters of both the box and the electronic assembly, thereby minimizing vibration displacement of the electronics.

Except for the lack of an internal support structure and the differences outlined above, the mechanical packaging of the TME is nearly identical to that of the PCM.

3.2.1.1.2 ELECTRONICS PACKAGING. The circuits within the TME can be grouped into five basic functional groups. These groups are the relay and noise suppression circuits, the record amplifier, the playback amplifier, the summing circuits, and the temperature monitoring circuit. A review of this grouping, together with a study of the electrical requirements, indicated that optimum design would result from packaging the record amplifier, playback amplifier, temperature monitor circuit, and the fixed value components of the summing circuits into welded cordwood modules. These circuits are packaged into four modules as follows:

Circuit	No. of Module Types	No. of Modules Per TME
Record Amplifier		
Playback Amplifier	1	2
Monitor Circuit	1	1
Summing Circuitry	1	1
Total	3	4

Since there are two separate recorders, two sets of record/playback amplifiers are needed. For electrical reasons, record amplifier No. 1 is located in the module with playback amplifier No. 2 and record amplifier No. 2 is packaged with playback amplifier No. 1. The modules are electrically interconnected by soldering the modules to printed-circuit cards. The variable resistors employed in the summing circuits are located on the front panel so that the adjustments are accessible externally.

The relays and their associated noise suppression components are mounted directly onto printed-circuit cards in a planar manner. Interconnection is effected through solder connections to the cards.

The module card is a single-sided card with plated-through holes. One such module card assembly is required in the TME.

The relay cards are four-layered M/L cards, with circuitry located on all but the top layer (the layer on which all of the components are located). One each of two types of relay card assemblies are required in the TME.

Two ground plane shield cards are used in each TME. These cards are placed between each relay card assembly and the module card assembly to block stray signals that might be emitted by the relays. The shield cards prevent such signals from adversely affecting the circuits in the module card assembly.

The location of these card assemblies and their reference designations are listed in table 6 and illustrated in figure 43.

Table 6. TME Unit Card Assemblies and Reference Designations

Reference Designation	Card Nomenclature	Packaging Technique
A1	Relay Card Assembly (Ty 1)	Planar
A2	Ground Card	---

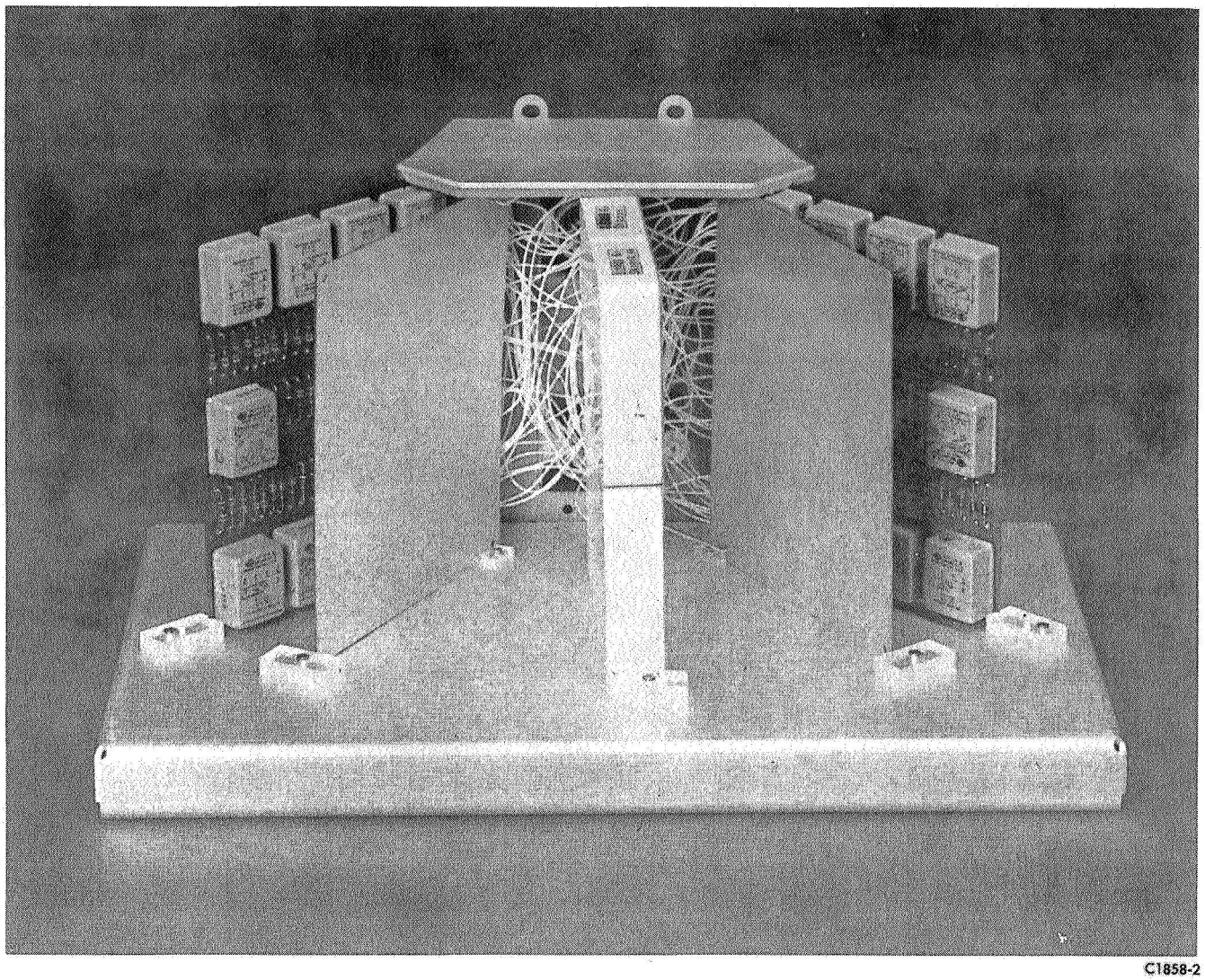


Figure 43. TME Assembly - Spreadout Configuration

Table 6. TME Unit Card Assemblies and Reference Designations (Continued)

Reference Designation	Card Nomenclature	Packaging Technique
A3	Record/Playback, Summing Amplifier, and Monitor Assemblies	Cordwood Module
A4	Ground Card	-
A5	Relay Card Assembly (Ty II)	Planar

3.2.1.1.3 SYSTEM ASSEMBLY AND TEST. The initial step in the assembly of the TME is preparation for unit test. The relative simplicity of this unit is such that except for the usual module tests, no subunit tests are required. To prepare the TME for unit test, the card assemblies and their associated connectors are hard-wired together, the ground plane cards are installed in the proper locations, and the assembly is mounted to the front panel. The unit is then secured to a holding fixture in which initial unit checkout is performed. Following checkout, the assembly is removed from the fixture and the appropriate compression shims are installed. The assembly is then installed in the housing, the top panel is positioned, and a hydraulic press is used to apply a predetermined load to the stack. While the load is maintained, the top and front panels are secured. The TME unit is removed from the hydraulic press and is then ready for final test.

3.2.1.1.4 MAINTAINABILITY AND REPAIRABILITY. As with the PCM, two levels of maintenance (field and depot) are feasible to provide repairability of the TME to the component level. Since troubleshooting on the field may not be considered expedient, the unit is designed to be easily removed and replaced in the spacecraft without the use of special tools.

At depot level, the electronics are easily removed from the housing through the use of a hydraulic press. Standard repair procedures are used to remove and replace the foamed modules from their card assemblies, and to remove the potting foam and components from the defective module. Component replacement on the planar-packaged cards (relay/component cards) is effected by fanning the card stack apart (figure 43), unsoldering the defective component, and soldering the replacement onto the card.

3.2.1.2 ELECTRICAL CHARACTERISTICS. Table 7 contains a listing and summation of the primary electrical characteristics of the Nimbus B TME Unit.

Table 7. TME Electrical Characteristics

Input power:	0.5 watt maximum
Current	20 ma dc nominal
Voltage	24.5 vdc reg buss
Input signals:	
Split-phase, real-time serial data	2.8 v p-p nominal
Split-phase, for recording, serial data	6.0 v p-p nominal
Time code (MM10A)	1.0 v p-p nominal

Table 7. TME Electrical Characteristics (Continued)

Input signal frequency:	
Split-phase data	250 cps (All ZERO's) 500 cps (All ONE's)
Time code (MM10A)	10 kc
Output signals:	
Time code	630 ±40 mv p-p
Time code and real-time data	630 ±40 mv p-p
Playback data	630 ±40 mv p-p
Output signal frequency:	
Time code	Same as input
Time code and real-time data	Same as input
Playback data	7.5 and 15 kc (30 x split-phase input record frequency)
Record time:	
Each recorder	108 minutes approximately
Playback time:	
Each recorder	3 minutes approximately

3.2.2 FUNCTIONAL BLOCK DIAGRAM DISCUSSION

The functional description of the Nimbus B TME Unit is discussed on a general level covering each functional subassembly and its operating characteristics. The discussion is briefly extended to include the tape recorders and transmitters for clarity and a better understanding of overall system operation.

3.2.2.1 GENERAL DISCUSSION. The TME is primarily a command and control relay switching system and signal amplifier that functions as an interface between the Nimbus B PCM Unit and the GFE (Government Furnished Equipment) tape recorders and transmitters. Signal switching performed in the TME is either ground controlled or self-driven depending on the operational mode the Nimbus satellite is in at the moment.

As shown in the block diagram, figure 44, the control switching network acts as an interface between all TME-contained subassemblies and control their operation. Through command switching the TME can modulate the transmitter with the 10-kc time code from the clock, or mix the time code with real-time output data from the PCM, and at the same time record this PCM data on two tape recorders. The transmitted real-time information provides a beacon signal, while the tape recorders store data when the satellite is out of range of a ground receiving station. Each tape recorder is capable of storing the data accumulated during one orbit, and the 30:1 playback speed ratio enables rapid transmission of recorded

FOLDOUT FRAME 1

FOLDOUT FRAME 2

NOTES:

1. THIS MONITOR POINT MUST BE CONNECTED INTO AN ANALOG CHANNEL IF USED.
2. THESE MONITOR POINTS MUST BE CONNECTED INTO A DIGITAL CHANNEL IF USED

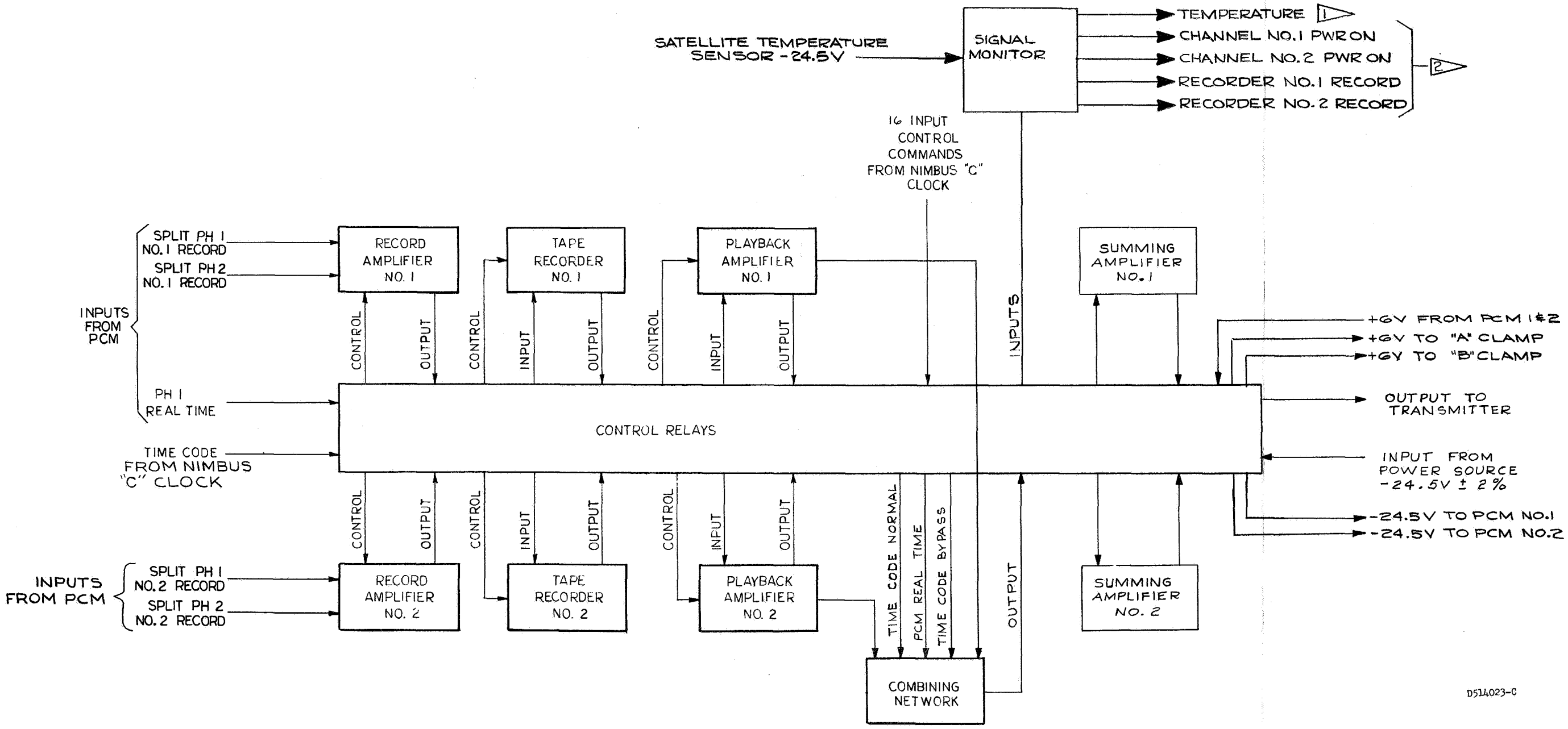


Figure 44. TME Unit Block Diagram

The tape recorders are housed in pressure-sealed containers utilizing "O" ring seals that maintain a pressure differential of 15 psi. A pressure transducer and two temperature thermistors are contained within each housing and are provided to measure internal pressure and temperature. These measurements are provided as part of the PCM telemetry data.

Each tape recorder contains a record motor and a playback motor. The record motor is a 2-phase, 100-cps, hysteresis synchronous motor having an input power no greater than 1-1/4 watts during the record mode. The input to the motor power supply is from the Nimbus -24.5-volts, ±2-percent, regulated power supply. In turn, the tape recorder power supply produces a 100-cps, 18-volts, ±20 percent, peak-to-peak 2-phase square wave. Input transients no greater than 0.25 volts, peak-to-peak, are generated.

The playback motor is a 100-cps, 2-phase, hysteresis synchronous motor with power input requirements no greater than 4 watts during the playback mode. The motor is capable of attaining a playback speed of 12-inches per second in less than 6 seconds. A compensating motor provides momentum compensation to reduce impulse and gyroscope effects on the spacecraft during the playback mode. Total residual angular momentum never exceeds 75×10^{-4} inch-pounds-per second. The compensation motor does not consume more than 2 watts of power. Telemetry monitoring of each phase of each motor is provided.

Performance characteristics of the tape recorders are listed in table 8.

Table 8. Tape Recorders - Performance Characteristics

Function/Item	Characteristic/Parameter
Amplitude modulation	Does not exceed 10% at a 16,500-cps playback frequency over a temperature range from -5°C to +55°C.
Playback pulse	0.015-second duration (minimum)
Tape speed	
Record	0.4-inch per second
Playback	12-inches per second
Record/Playback ratio	1:30 ±1%
Channels	1
Signal-to-noise ratio	40 dB
Record frequency	100 - 500 cps
Playback frequency	3,000 - 16,500 cps
Input sensitivity	12.6 millivolts (peak-to-peak)

Table 8. Tape Recorders - Performance Characteristics (Continued)

Function/Item	Characteristic/Parameter
Recording time	108 minutes (nominal)
Playback time	Timer time minus 3 ±1 second
Timer time	219 ±1 seconds
Overlap time	3 ±1 seconds
Starting time	6 seconds (maximum)
Power consumption	
Record mode	Less than 2 watts
Playback mode	Less than 12 watts
Record motor current	Less than 70 ma dc
Playback motor current	Less than 250 ma dc
Momentum motor current	Less than 250 ma dc
Harmonic distortion	Less than 5%
Record/Playback head	
Record current	1.0 ma ±0.1 ma
Record bias current	2.3 ma ±0.5 ma at 8,000 cps
Input Impedance	Inductance = 84 mh ±5% DC resistance = 11.4 ohms at 1 kc with 1 volt
Playback output voltage	50 ±15 mv
Telemetry voltage output range	0 to -6.4 volts dc
Record, playback, and momentum motor output impedance, phase A and B	100K ohms across 40 μfd capacitor

information while the satellite is within range of the receiving station. The record time is approximately 96 minutes; the playback time is approximately 3 minutes. The two tape recorders provide 2-orbit storage capability by turning off one recorder (by ground command) at the end of the first orbit, and letting the second recorder store second orbit information. Then the two tape recorders are dumped (by ground command) sequentially during a 6-minute interval over a receiving station.

3.2.2.1.1 COMMAND SWITCHING. The Nimbus B TME command switching network comprises 17 control relays mounted on two printed-circuit cards containing nine relays per card. All relay coils (or parallel relay coils) contain 2 parallel diodes in series with the input command voltage and another 2 diodes connected in series across the coil. The diodes provide isolation and reduce noise generation. All 18 relays have DPDT contacts with 14 relays having magnetic latching with two separate command coils (relay operates like a set-reset flip-flop). The remaining four relays are nonlatching (standard) relays with one command coil. The nonlatching relays are used to drive four parallel latching relay coils. The relays are connected in this manner to reduce the total load on the Nimbus C clock command circuits.

The 14 latching relays have a dc coil resistance of 230 ohms, and the four nonlatching relays have a dc coil resistance of 210 ohms. All relays operate with a nominal 12 volts and the DPDT contacts are rated at 3 amperes, dc. Two parallel resistors are connected in series with the command voltage to reduce the drive to the relays that are energized directly from the -24.5 volt power line. Since the tape recorder automatically switches the relays back to the record mode after three minutes in the playback mode, the two nonlatching record command relays provide signal isolation between the Nimbus C clock record command and the tape recorder record command. The isolation is necessary for proper operation of the clock output circuits.

The following command signals control the relays and perform all TME and PCM switching functions:

Channel No. 1 - Power ON

Channel No. 1 - Power OFF

Channel No. 2 - Power ON

Channel No. 2 - Power OFF

Recorder No. 1 - Record

Recorder No. 1 - Playback

Recorder No. 2 - Record

Recorder No. 2 - Playback

Summing Amplifier No. 1 ON - No. 2 OFF

Summing Amplifier No. 1 OFF - No. 2 ON

PCM Power No. 1 ON - No. 2 OFF

PCM Power No. 1 OFF - No. 2 ON

Time Code Normal

Time Code Bypass

Time Code ON - PCM Real Time OFF

Time Code ON - PCM Real Time ON

3.2.2.1.2 RECORD AMPLIFIERS. There are two record amplifiers, one connected to each of two tape records through the command switching network, to saturate the tape with split-phase Mark 0 data. Each record amplifier is driven from a separate, isolated source in the PCM unit to achieve maximum isolation and redundancy. The PCM output circuit contains buffer amplifiers or drivers that isolate the NRZ-to-split-phase code source from the load. The second amplifier receives both phases of the split-phase signal. A single record/playback head in the recorder is switched between the record amplifier output and the playback amplifier input. Since the record amplifier is of the saturated type, current is always flowing in the head winding and the magnetic tape particles are always being aligned in one of the two possible directions. The normal record data frequency varies from 250-cps for all data 0's to 500-cps for all data 1's.

3.2.2.1.3 PLAYBACK AMPLIFIERS. There are two playback amplifiers with each one connected to a separate record head through the record/playback switching relay described previously. Both the record and playback amplifiers use the same tape recorder head winding. The winding is relay-switched to the desired amplifier. As the winding is switched to desired amplifier, a second relay, operating in parallel, applies -24.5 volts to the desired amplifier. Thus, the unused amplifier is not connected to -24.5 volts nor to the record/playback winding and only one amplifier is in operation at any given time. The playback amplifier data input frequency is 30 times that of the record frequency (the playback motor operates the tape 30 times faster than the record motor). Therefore, the maximum playback frequency (all ONE's) is 15 kc and the minimum frequency (all ZERO's) is 7.5 kc. In normal operation, the record amplifier records data on the tape recorder for approximately 90 minutes and the playback amplifier then plays back this data for approximately 3 minutes. After playback, the recorder automatically switches all circuits back to the record mode.

3.2.2.1.4 SUMMING NETWORK. The summing network and a summing amplifier combine the different signals programmed to modulate the beacon transmitter. The summing network is passive and nonredundant. There are two input/output block redundant summing amplifiers that provide maximum signal isolation in the event of a failure.

The two summing amplifiers are conventional operational amplifiers and are contained in one module. The -24.5-volt power line is connected to both amplifiers in parallel, and complete signal or redundancy isolation is achieved by relay switching both the inputs and the outputs. Thus, only one amplifier at a time can be connected between the summing junction and the coaxial cable to the transmitter. The summing junction functions under relay control to present any one of the following signals to the amplifier: (1) 10-kc modulated time code, (2) 10-kc modulated time code mixed with real time PCM split-phase data, (3) playback of recorded data from channel 1 recorder, (4) playback of recorded data from channel 2 recorder, and (5) emergency by pass 10-kc modulated time code plus playback data from either recorder

if the playback mode is commanded. Each of the circuits that develop these signals includes an adjustment potentiometer to control the output signal amplitude to the transmitter.

When mixing time code and PCM real-time data in the summing network, the time-code amplitude to the summing network is halved through relay contacts and a precision voltage divider. Thus, the time code and PCM real-time data each contribute one-half the total signal amplitude to the summing junction.

The summing amplifier module contains two identical operational amplifiers. Either of these amplifiers can be selected as the output summing amplifier for the TME unit. Amplifier selection is accomplished by relay switching the input of the amplifier to the combining resistor network, and simultaneously switching the output of the amplifier to the transmitter input cable. The amplifiers, when connected to the input combining network, perform the summing function for the various input signals. The amplifiers also provide gain adjustment for each signal without affecting the gain settings of the other inputs. The gain is controlled by adjusting the resistance of the input resistor in the combining network.

Relay switchable operating commands are use summing amplifier 1 or use summing amplifier 2. One summing amplifier must be on at all times since the 10-kc modulated time code is used as a beacon and is transmitted during the major portion of the orbit time (except during recorder playback) through one or the other of these summing amplifiers.

Only the input and output signals are relay switched. The power line is returned to the -24.5 volts regulated bus so that both summing amplifiers have power whenever power is applied to the TME.

3.2.2.1.5 TELEMETRY MONITORS. There are five telemetry monitor points in the TME. One is TME temperature and must be applied to an analog channel gate in the PCM. This circuit is identical to the two PCM circuits. The remaining monitor points are applied to digital channels and verify, in real-time, that the relays have received the following commands from the clock and have switched to the new position.

a. Recorder channel 1 - power on (power on produces a data "1" and power off produces a data "0").

b. Recorder channel 2 - power on (power on produces a data "1" and power off produces a data "0").

c. Recorder 1 - record mode (record mode produces a data "1" and playback mode produces a data "0").

d. Recorder 2 - record mode (record mode produces a data "1" and playback mode produces a data "0").

3.2.2.1.6 TAPE RECORDERS. Two recorders are used in the PCM telemetry subsystem. These are government-furnished single-channel magnetic tape recorders manufactured by Raymond Engineering Laboratories.

3.2.2.1.7 TRANSMITTERS. The RF link for the PCM telemetry subsystem is a model SST-100-05 solid-state, amplitude-modulated transmitter, manufactured by Hughes Aircraft Company and GFE to Radiation. For increased reliability, two transmitters are used in a redundant configuration and are housed in one 6 x 2 x 6-1/2-inch Nimbus module.

The transmitters are block-redundant and are switched by three latching relays within the housing. The first relay turns the -24.5-volt, ±2-percent, power supply on and off; the second relay switches the -24.5-volt, ±2-percent, and modulation signals to the selected transmitter; and the third relay operates in parallel with the second relay and connects the antenna to the appropriate transmitter.

Each transmitter produces a power output of 0.25 watts (minimum).

3.3 NIMBUS B QUALIFICATION AND FLIGHT MODEL MODIFICATIONS.

No major problems appeared imminent that required structural modifications. Certain design changes became desirable in the Nimbus Study TME and were accomplished in the Nimbus B. Changes in the electrical design occasioned some minor changes in TME packaging. Significant changes occurred in the relay control circuits and their fuse sources. These changes are discussed in the following paragraphs.

3.3.1 ELECTRICAL DESIGN CONSIDERATION

The Nimbus Study TME electronic circuits have been fabricated "as is" for the Nimbus B program. However, there have been significant changes in the relay wiring which affects both the relay functions and the input -24.5 volt fuse circuits that provide power to the tape recorders, record and playback amplifiers, summing amplifiers, and PCMs 1 and 2. These changes have been made to improve the overall reliability so that a single fuse failure in the playback mode will prevent a catastrophic failure resulting in total PCM real-time data loss. In addition to modifying the relay control circuits, some internal TME wiring has been modified to reduce crosstalk and noise that appear on the TME output modulation signal to the transmitter.

These changes are as follows:

a. The playback command interlock relays have been removed.

b. An emergency power relay has been added to allow the PCM and Time Code to modulate the transmitter with both tape recorders turned OFF.

c. The fuse sources supplying power to the tape recorders and tape recorder control relays have been changed to improve channel power line isolation in the event of a blown fuse.

d. Input -24.5 volt dc lines 1 through 4 are unchanged, but lines 5 and 6 have been made block (or parallel) redundant from the Nimbus Regulated Bus.

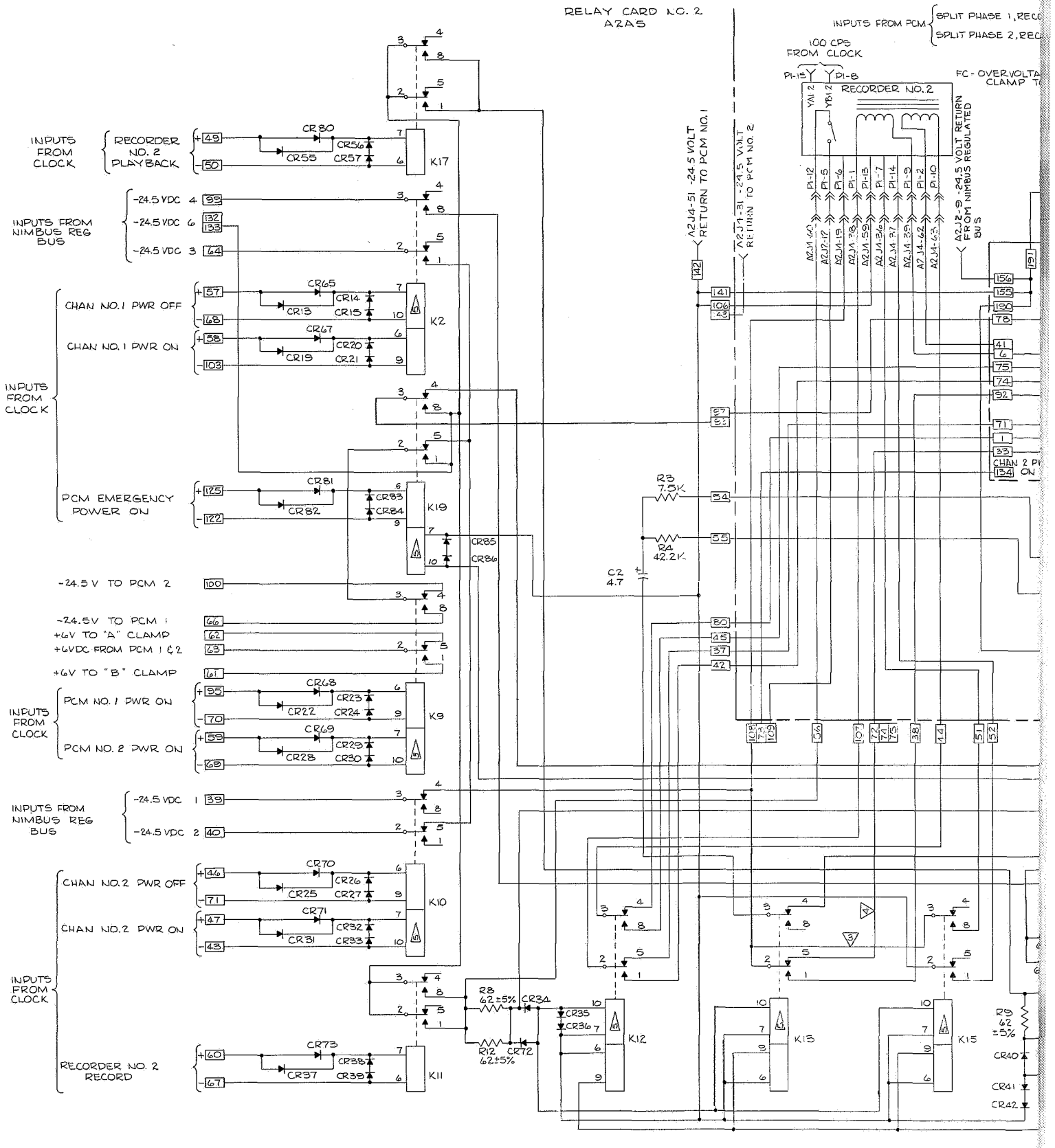
e. The 100-cps signal lines from the Nimbus clock to the two tape recorders going through the TME unit, have been replaced with shielded lines and rerouted to reduce cross-talk and noise appearing on the TME output modulation signal to the transmitter.

3.3.1.1 PLAYBACK COMMAND INTERLOCKS. It is undesirable to give a wrong command that would allow both recorders to playback at the same time, so the two interlock relays K6 and K14 were originally provided. Thus, if tape recorder No. 1 were playing back data, tape recorder No. 2 could not be commanded to the playback mode until after tape recorder No. 1 automatically went back into the record mode. These two relays (K6 and K14) are present in the Nimbus Study TME. However, because of certain failure modes, they have been removed from the Nimbus B TME (figure 45). Thus, if both Nimbus B recorders are commanded to the playback mode at the same time, the output data will be scrambled because both recorders can playback simultaneously. The interlock relays were removed because if one channel's relay failed in the playback mode, it would not allow the other channel to be commanded to playback, which would allow one relay failure to fail both channels in the playback mode, while at the same time it would fail the PCM real-time data train. Thus, one interlock relay failure could remove all data to the transmitter except for time code bypass data, which would effectively fail both PCMs.

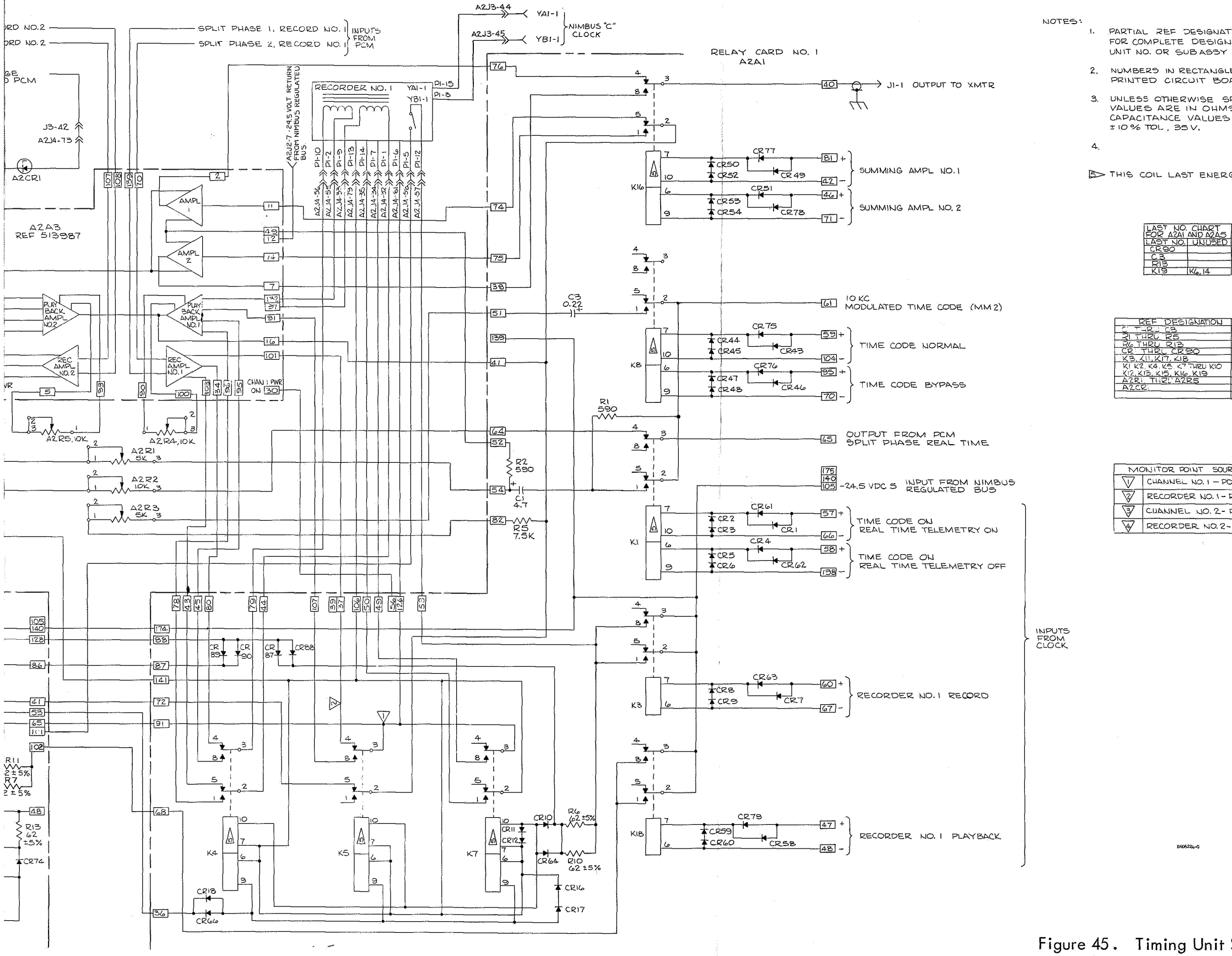
3.3.1.2 EMERGENCY POWER OPERATION. The Nimbus Study TME summing amplifier power can be turned OFF if both recorder channels are commanded OFF. In this case, the beacon transmitter would also be useless since it would not receive a modulation signal. The recorder channel power relays also control power to the PCM unit. These features are undesirable from a systems engineering point of view; therefore, the circuits are modified in the Nimbus B program.

In the Nimbus B TME the summing amplifiers are powered full-time as long as power is applied to the TME unit from the Nimbus Regulated Bus. Thus, the 10 kc modulated time code signal from the Nimbus clock can always modulate the beacon transmitter regardless of other TME commands. The power is applied to the summing amplifiers through fuse No. 5 during normal operation (channels 1 and/or 2 operating) and is supplied by fuse No. 6 during emergency operation.

Past experience has shown that mechanical devices with moving parts are the weakest parts of any spacecraft. Thus, on the Nimbus B program, the PCM real-time data function must be made independent of the two recorders, so power to the PCM is supplied through fuse No. 2 (channel No. 2 on) and fuse No. 3 (channel No. 1 on) in the normal modes, but in an emergency, this power is supplied through fuse No. 6 (vdc 6 line). Fuse No. 6 is thus termed the PCM Emergency Power input and is controlled by a new relay (K19) shown in figure 45. When the PCM Emergency Power on command is given, power is supplied through vdc 6 to either PCM No. 1 or No. 2 and to both summing amplifiers with both recorder channels in the power off condition. If either recorder is commanded on and to the record mode, the emergency power relay (K19) is reset to normal. In the normal operating condition, fuse No. 6 is used only to supply relay power to channel No. 2's playback and record command relays (K12, K13 and K15).



Foldout FRAME 1



NOTES:

1. PARTIAL REF DESIGNATIONS ARE SHOWN; FOR COMPLETE DESIGNATION, PREFIX WITH UNIT NO. OR SUBASSY DESIGNATION.
2. NUMBERS IN RECTANGLES REPRESENT PRINTED CIRCUIT BOARD TERMINATIONS.
3. UNLESS OTHERWISE SPECIFIED, RESISTANCE VALUES ARE IN OHMS ±1% TOL, ¼ WATT; CAPACITANCE VALUES ARE IN MICROFARADS ±10% TOL, 35 V.
4. ▷ THIS COIL LAST ENERGIZED.

LAST NO. CHART FOR A2A1 AND A2A5	
LAST NO.	UNUSED
CR80	
C3	
R13	
K19	K6, 14

REF DESIGNATION	PART NO.
C1, C2	00851
R1 THRU R5	106780
R6 THRU R13	04115
CR THRU CR80	06355
K3, K11, K17, K18	110429
K1 K2 K4 K5 K7 THRU K10 K12 K13, K15, K16, K19	110439
A2R1 THRU A2R5	110285
A2CR1	110650

MONITOR POINT	SOURCE VOLTAGE
▽	CHANNEL NO. 1 – POWER ON
▽	RECORDER NO. 1 – RECORD MODE
▽	CHANNEL NO. 2 – POWER ON
▽	RECORDER NO. 2 – RECORD MODE

Figure 45. Timing Unit Schematic Diagram

Foldout FRAME 2

Foldout FRAME 3

3.3.1.3 RECORDER POWER LINE REWIRING. As it has been previously explained, the playback interlock relays (K6 and K14) could cause a catastrophic system failure in the event one recorder failed in the playback mode. This explanation also holds true if fuse No. 5 (vdc 5 line) is blown in the Nimbus Study TME since vdc 5 line supplies relay command power to both recorder-control relays for both clock commands and the automatic record command at the end of 3 minutes of playback data. Therefore, if this fuse is blown in the Nimbus Study TME by the playback function, then all PCM data is lost and only the time code bypass function is available. The Nimbus B power lines have been rewired to prevent such an occurrence.

In the Nimbus B TME, the power supply lines between the two recorder channels have been isolated, and are also isolated between the clock command power and the recorder automatic command power. Thus, if an automatic command blows a fuse a clock command can be given to place that channel back to the record mode and then the channel power can be turned off. At this time, the redundant tape recorder must be used by PCM real time data is back in normal operation. If the clock-command relay power fuse blows during playback, then the automatic command from the recorder will reset the relays to the record mode at the end of 3 minutes of playback data, and again the PCM real time data is available.

Table 9 shows the loads applied to the six TME input fuses. Observe that fuses 1 and 4 have identical functions, fuses 2 and 3 have identical functions, and fuses 5 and 6 have identical functions. Also observe that fuses 2, 3 and 6 supply power to the PCM, and fuses 5 and 6 supply power to the summing amplifiers with different fuses supplying power in different modes of operations.

Table 9. TME Input Power Lines

-24.5 vdc Number (Fuse No.)	Fuse Applies Power To:	
1	Recorder No. 2 including R/P Amps	Identical
4	Recorder No. 1 including R/P Amps	Functions
2	PCM when Channel 2 is ON	Identical Functions
3	PCM when Channel 1 is ON	
5	Relay Power (K4, K5, K7) for Recorder No. 1	Identical*
6	Relay Power (K12, K13, K15) for Recorder No. 2	Functions

*In addition to Relay Power Fuse No. 5 Supplies Normal Operating Power to the Summing Amps and Fuse No. 6 Supplies Emergency Power to both Summing Amps and the PCM.

3.3.1.4 REDUNDANT POWER LINES. The Nimbus B TME input power lines 5 and 6 are redundant from the connector pins to the TME card pads. Input -24.5 vdc No. 5 can be fed into the TME on connector pins J2-12 and/or J2-61 while input -24.5 vdc No. 6 can be fed into the TME on connector pins J2-1 and/or J2-59. This redundancy provision will allow two external fuses to supply power to each of the two power lines.

3.3.1.5 100 CPS SHIELDING. The 100-cps power lines used to supply driving power to both recorder motor amplifiers are fed through both the Nimbus study and Nimbus B TME Units but are not directly used by the TME circuits. The 100-cps signal is an approximate 24 volt square wave which creates an undesirable crosstalk problem with the crosstalk noise appearing on the modulation signal to the transmitter. To minimize this crosstalk, all four 100 cps lines between connectors J3 and J4 have been shielded in the Nimbus B TME and in addition the junction point for YB1-1 to the PCM has been removed from TME card A2A1. These shielded wires are routed as shown in table 10.

Table 10. 100 CPS Shielded Lines

TME Connector			
100 CPS Function	Input Pin Number	Output Pin Number	Destination
YA1-1	J3-44	J4-82	Recorder No. 1
YB1-1	J3-45	J4-83	Recorder No. 1
YB1-1	J3-45	J4-77	PCM 1 and 2
YA1-2	J3-46	J4-84	Recorder No. 2
YB1-2	J3-47	J4-85	Recorder No. 2

3.3.2 MECHANICAL PACKAGING DESIGN CONSIDERATIONS.

There were no changes in the mechanical characteristics of the Nimbus B TME from the Nimbus Study TME, but there were some changes in the electrical packaging area. The only changes were the replacement of some internal hookup signal wires, including the 100-cps line, with twisted shielded-pair wire, along with a different relay card.

The twisted shielded wire was necessary to reduce the 100-cps line noise, and the new relay card was needed for the addition of a new relay (K19) and some changes in the printed-circuitry. The additional relay now incorporates the capability for switching into the emergency power on mode.

SECTION IV

BENCH TEST EQUIPMENT

SECTION IV

BENCH TEST EQUIPMENT

4.1. INTRODUCTION

The Bench Test Equipment (BTE) shown in figure 46 is a special purpose test set designed to test the Nimbus B PCM Telemetry Subsystem. The BTE performs functional tests on Nimbus B airborne telemetry packages consisting of a PCM unit, a TME unit, two tape recorders, and a telemetry transmitter. The BTE also tests individual PCM and TME units. This section of the Nimbus B report discusses the effort performed on this contract to develop and fabricate the BTE. This section also briefly describes the present BTE configuration with emphasis on all changes incurred in its design to date. Descriptions covering functional, physical, and operational characteristics are presented in their entirety to include all changes and their impact on overall unit operation. The descriptions entail functional block diagram descriptions according to updated logic diagrams. There were 3 BTE's built on this contract.

4.2. BTE GENERAL DESCRIPTION

4.2.1. MAJOR CHARACTERISTICS

The BTE is composed of subunits contained in a cabinet 70 inches high, 18.5 inches wide, and 23 inches deep. The cabinet is mounted on four casters bolted to a broad based platform which provides balance and stability to the system. The locations, functions, and reference designations of the BTE subunit panels are shown in figure 47. The full length cabinet rear door, front sectional doors, and slide-mounted drawer assemblies permit easy access to system subassemblies. Subunits 1A3 and 1A6 are slide assemblies that are held in place by captive screws, while sectional hinged doors provide access to subunits 1A1, 1A2, 1A5, 1A6, and 1A8. Subunits 1A4, 1A7, and 1A9 are mounted directly to the cabinet and are accessible through the cabinet rear door. To gain access to subunit 1A6, it is necessary to open the 1A2 hinged panel. Control panels are mounted on the face of logic drawer 1A3 and the inclined control console 1A5. Control panels contain mode selection switches, test monitor devices, and internal circuit test points. Digital and analog data are programmed at the digital panel 1A2, and analog panel 1A1, respectively. Circuit breakers and power supply adjustments are located on the power chassis panel 1A8.

Wiring to and from the horizontal drawer assemblies is accomplished through cables that interconnect between the drawers and a frame of connectors at the rear of the cabinet. In the drawer, the cable connectors mate with connectors mounted on the 50-module contact boards.

Fourteen test cables are included with the test set to permit test interconnections in any of the configurations described in the Bench Test Equipment Instruction Manual. Test connections are made through a connector panel mounted on the side of the BTE.

Table 11 lists the BTE primary power requirements, environmental requirements, signal inputs, and signal outputs. Five commercial dc power supplies are used in the BTE. Four

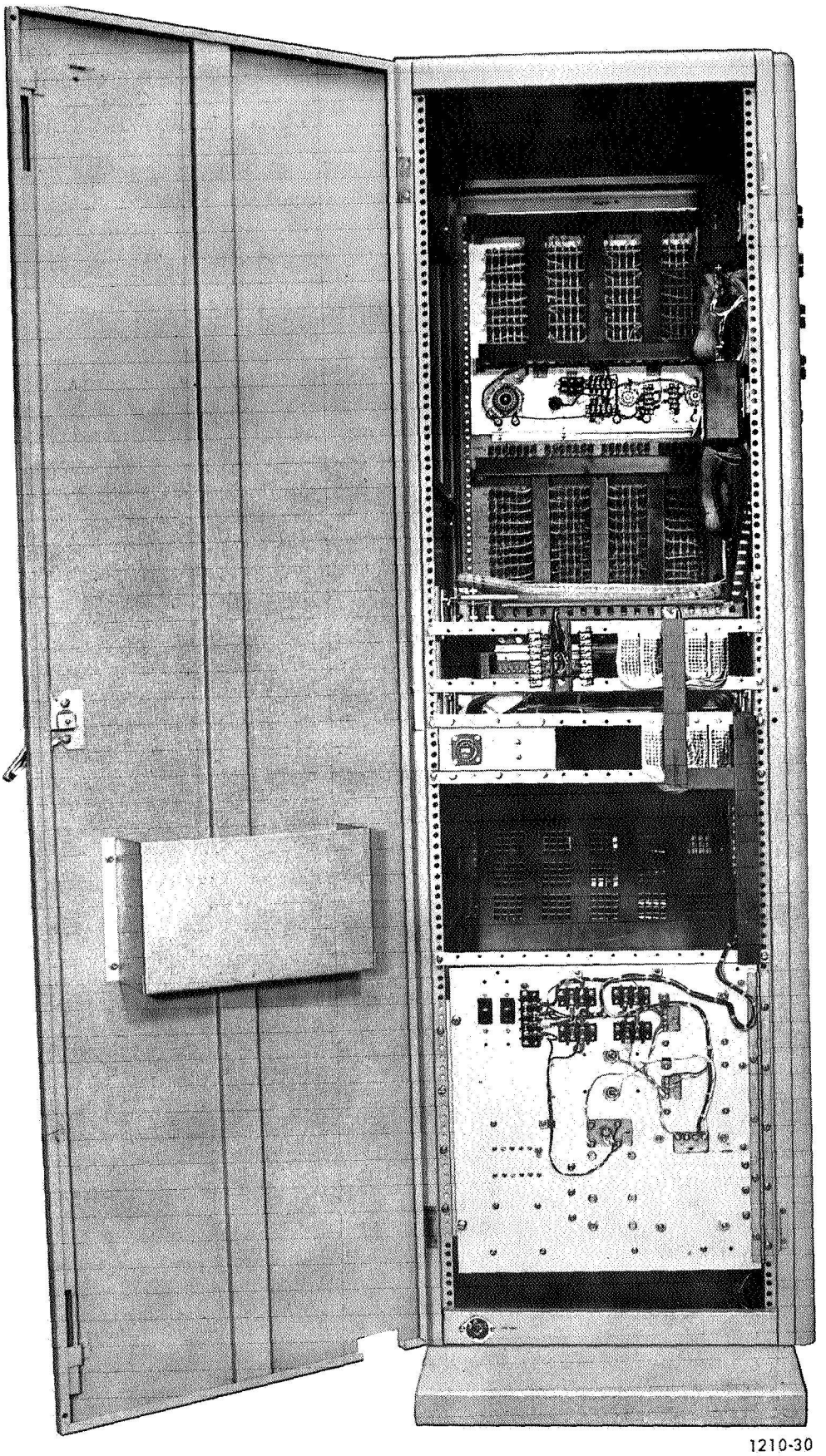


Figure 46. Bench Test Equipment Rear View

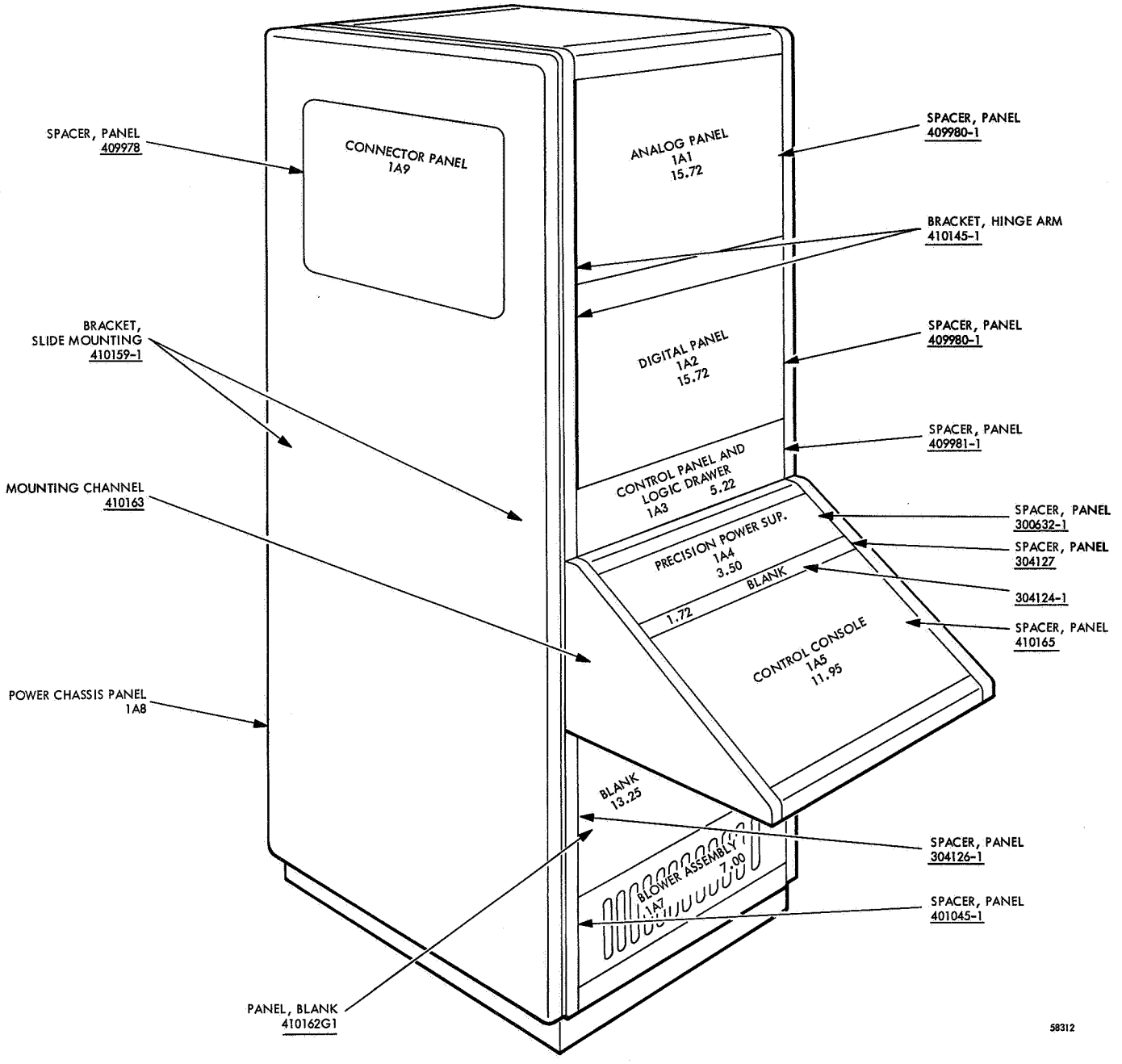


Figure 47. Bench Test Equipment, Subunit Designations and Locations

of these supplies are contained in power supply chassis 1A8. The fifth supply is in unit 1A4. Table 12 lists the power rating and purpose of each supply. Primary power is routed to all power supplies and the blower motors through a single primary power cable. The system is protected against overload hazards by a 10-ampere circuit breaker. Two utility outlets, located at the bottom front of the cabinet, are also protected by a 10-ampere circuit breaker.

Table 11. BTE Signal Characteristics

Input Power Requirements	
Voltage Current	115 ±10 vac, 60 cps ±5 cps single phase 20 amperes
Environmental Requirements	
Barometric Pressure	27 to 31 inches
Humidity	5% to 90%
Temperature	70° ±20°F
Signal Input	
No Load:	
Command To Test Set	+6 volt pulse
External Input	+1 to -11 vdc
Split-Phase Real-Time Data From TME	630 ±50 mv symmetrical about a -12V dc level
Split-Phase Real-Time Data From PCM	-2.5 to -5.3 volts, peak-to-peak
Signal Output	
No Load:	
Time Code MO	0 to -5.4 ±0.5 vdc
Time Code MM10A	Minimum 0.3 ±0.1 volts peak maximum 1 ±0.2 volts peak
Split-Phase Real Time (Phase 1 and 2 to Recorders)	+3 to -6 ±0.2 vdc
Split-Phase Real Time (Phase 1 to TMX)	-2.5 ±0.2 vdc to -5.3 ±0.5 vdc
Commands	-24.5 vdc nominal
100 cps YA1 YB1	0 to 23.0 ±1.5 vdc
500 cps	0 to 5.8 ±0.5 vdc
10 cps	0 to 5.4 ±0.5 vdc
1 cps	0 to 5.8 ±0.5 vdc

Table 12. BTE Commercial Power Supplies

Nomenclature	Manufacturer	Location	Function
Power Supply	Kepco	1A4	Provides precision voltages from 0 to -11.11 vdc for voltage coding.
Power Supply, SWR 0-40.0 vdc 3.0 amperes	Technipower Inc.	1A8	Provides power to spacecraft subsystems.
Power Supply, M 184.0 vdc 0.050 amperes	Technipower Inc.	1A8	Supplies +190 vdc to unitary decimal indicator.
Power Supply, M 9.8 vdc, 6.0 amperes	Technipower Inc.	1A8	Provides -10 vdc ±1% for logic supply.
Power Supply, M 9.8 vdc, 1.5 amperes	Technipower Inc.	1A8	Provides +10 vdc ±1% for logic supply.

4.2.2. SUMMARY OF BTE MODIFICATIONS

This section contains a summary of BTE modifications made since publication of the BTE manual.

4.2.2.1. DETAILED DESCRIPTION OF CHANGES

a. The BTE previously recognized the sync pattern and ID once each major frame and used the signal to reset the bit, word and subframe counters. This was not desirable, since the BTE bit synchronizer drops bits when playing back from tape. To obtain a more stable operation the BTE was modified to recognize sync independently of the ID. Thus, the bit counter and word counter are now reset each subframe. The subframe counter is not reset when subframe one ID is detected concurrent with sync. The subframe counter is now driven by a combination of word rate and decoding of word 62.5 from the data register. This ensures that the subframe counter toggles at the correct bit time. Originally the detection of word 63 and bit 4 from the counter was used.

b. Considerable jitter was experienced during tape playback. This caused the transfer of data into the display register to be incorrect by one or two bits occasionally, especially those words occurring just prior to the counters being reset. The two words immediately preceding the resetting of the counters are word 1 and word 62.5, both sync words. It

is desirable to have these words displayed reliably, therefore, the method of generating a transfer strobe from the counters for transferring these words was changed. The actual sync words are now decoded from the data register and used to generate the transfer strobes.

c. The input data register was dropping bits due to the overloading of the clock driver. This was corrected, as well as several other areas where excessive loading of the drivers was a problem, by replacing all buffer amplifiers (BA) used to drive the trigger inputs of CSR's with complementary drivers (CD).

d. The analog comparator was modified to provide a more reliable comparison by ANDing bit rate with the lower limit comparator output.

e. The YA1 and YB1 clocks were modified to reduce the rise and fall times to 3 microseconds and 6 microseconds, still within specifications. This reduced cross-talk in the cables, BTE, and PCM subsystem. Twisted shielded pair wire was also added for routing these clocks to the connector.

f. The MM10A output driver was modified to reduce the output impedance. (See drawing 605429, figure 69).

g. A capacitor was added to module 1A3B6B to eliminate the effects of noise from the command to test set line.

h. 10K resistors were added from TP3, TP4, TP5, TP6 and TP7 to ground to provide correct loading of the PCM outputs.

i. The value of capacitor C4 on the bit sync was changed from 0.0018 microfarad to 0.0033 microfarad.

j. The reset line on the time code counter was changed to give correct timing.

k. Resistors were added to the base inputs of the YA1 and YB1 clock drivers to prevent overdriving the base.

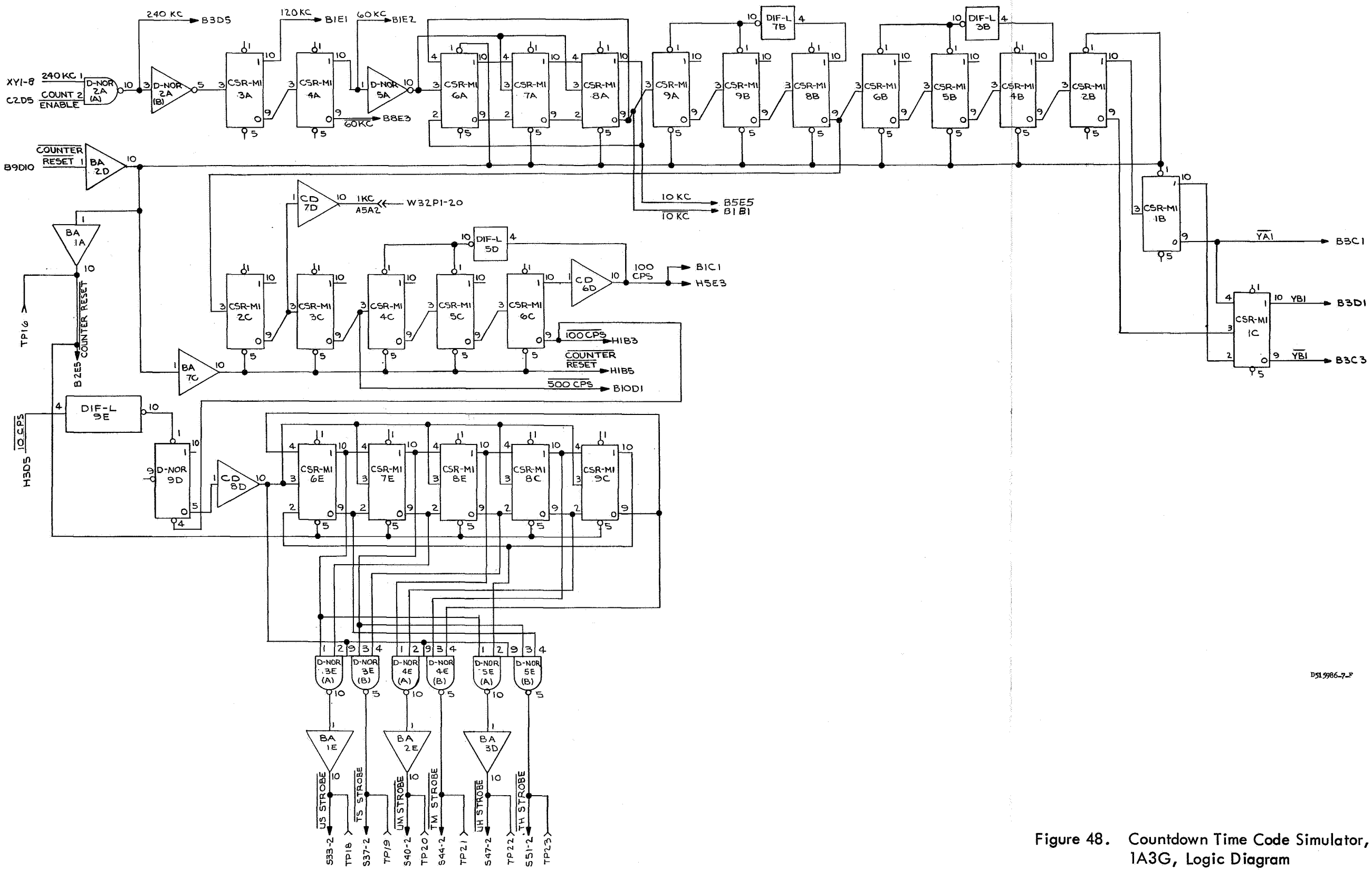
l. Twisted shielded pair wire was installed in the cables where noise immunity is required. Two 0.22 microfarad capacitors were added to cable W-9 to reduce noise spikes caused by the switching of YA1 and YB1. The AWG 24 wire used to supply -24.5 volts to the PCM was replaced with AWG 18 wire. Radiation cable assembly wire listings Numbers 112851 through 112864 contain all of the specific changes in the test cables.

4.2.2.2. CHANGES IN OPERATION. Operation of the test set was unaffected except in self-test. When operating in self-test mode, word 62.5 (binary 0111) must be the first four bits of the simulated data word for the subframe counter and data display to work correctly. The subframe counters will operate if a 0111 pattern is contained anywhere within the simulated data word, but word 62.5 will not be displayed in the correct bit positions when selected.

4.2.2.3. LOGIC DRAWING CHANGES. Logic drawings that reflect equipment changes since the last issue of the BTE manual are given in figures 48 through 59.

FOLDOUT FRAME 1

FOLDOUT FRAME 2



D51 5986-7-F

Figure 48. Countdown Time Code Simulator, 1A3G, Logic Diagram

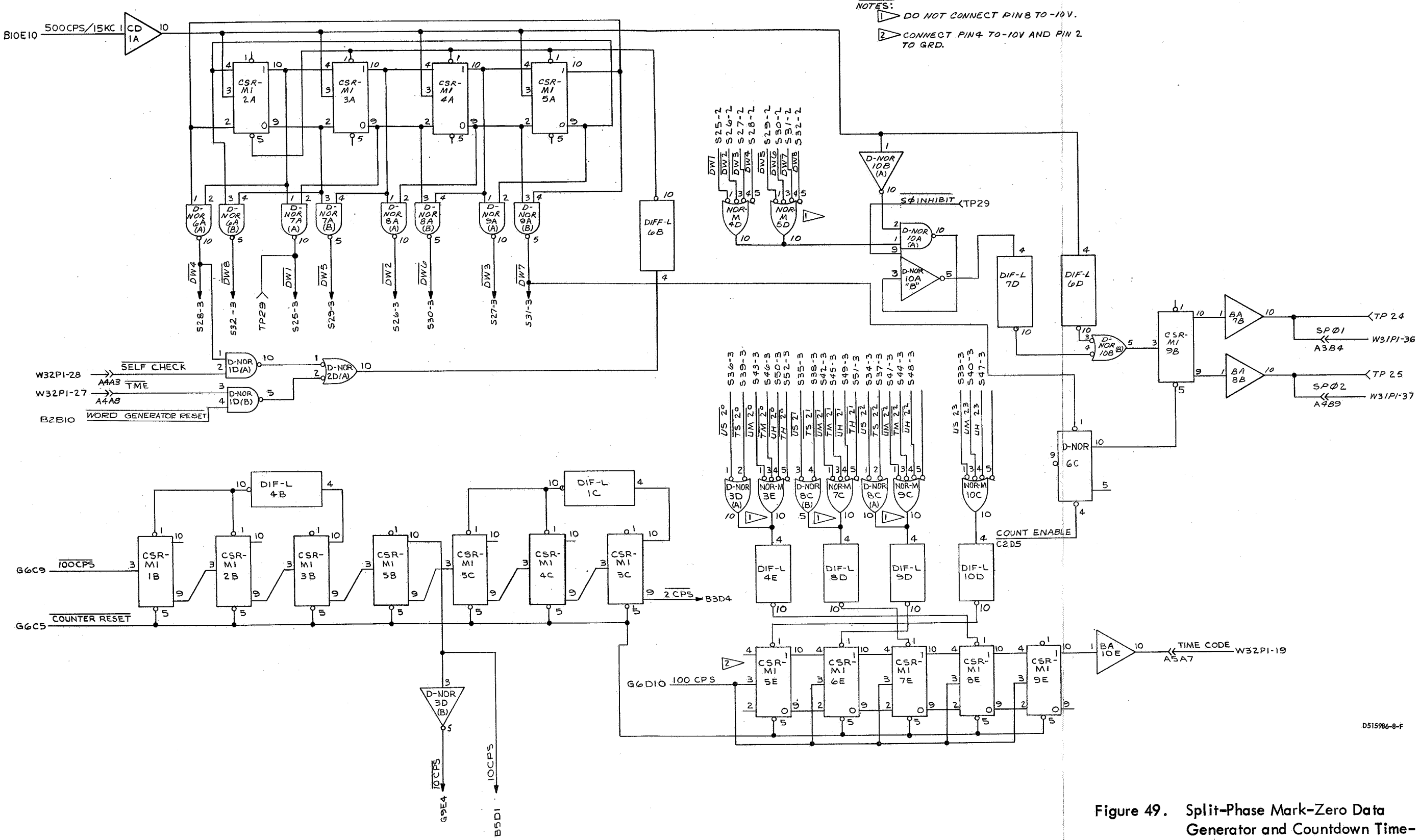


Figure 49. Split-Phase Mark-Zero Data Generator and Countdown Time-Code Simulator, 1A3H, Logic Diagram

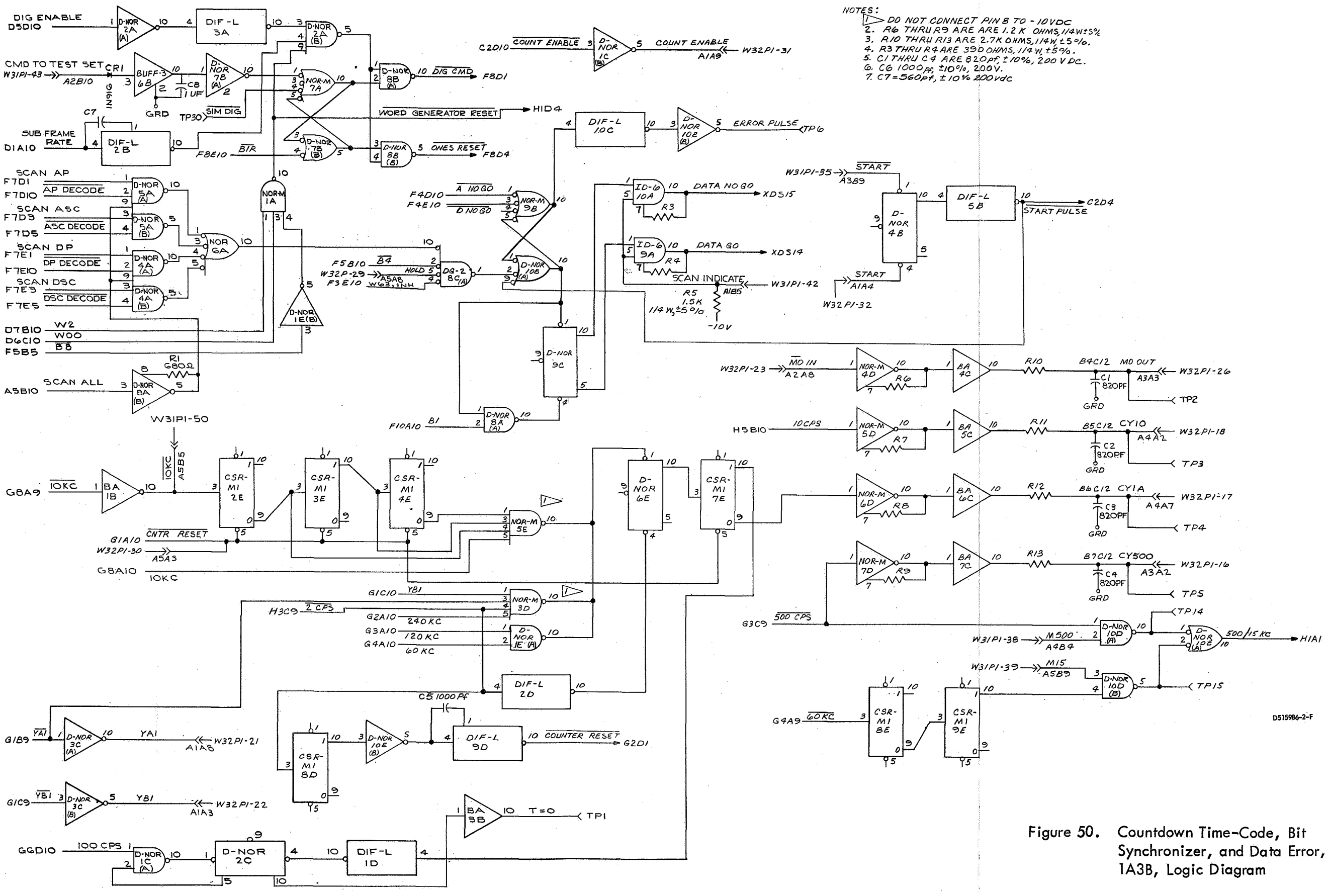


Figure 50. Countdown Time-Code, Bit Synchronizer, and Data Error, 1A3B, Logic Diagram

FOLDOUT FRAME 1

FOLDOUT FRAME 2

NOTES:
1. PARTIAL REF DESIGNATIONS ARE SHOWN. FOR COMPLETE DESIGNATION, PREFIX WITH UNIT NO. OR SUBASSY. DESIGNATION.
2. UNLESS OTHERWISE SPECIFIED, RES. VALUES ARE IN OHMS ±5%, 1/4 WATT. CAP VALUES ARE IN MICROFARADS ±10%, 50 V.

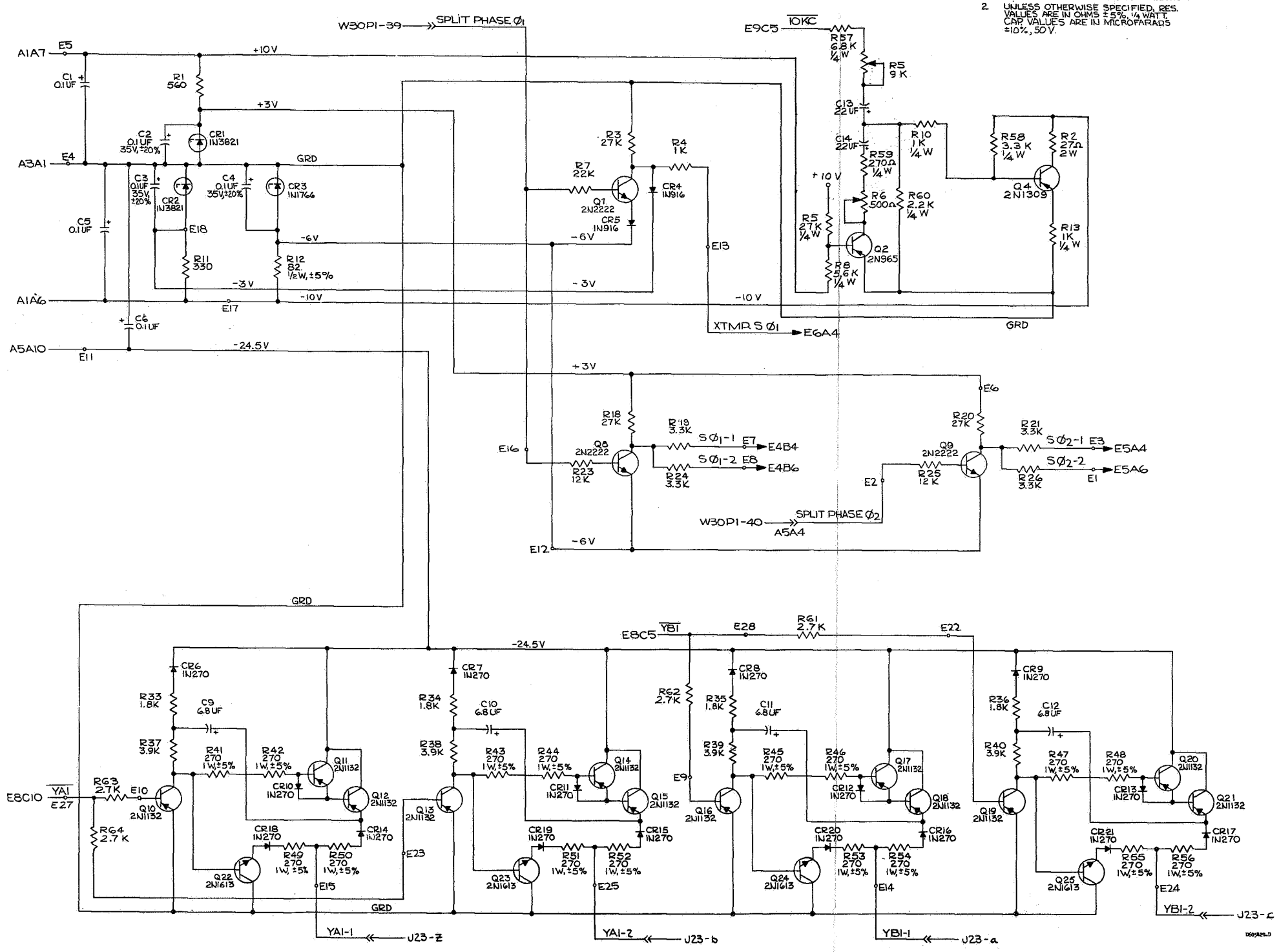


Figure 51. Component Interface Board (Part of 1A6), Schematic Diagram

FOLDOUT FRAME 1

FOLDOUT FRAME 2

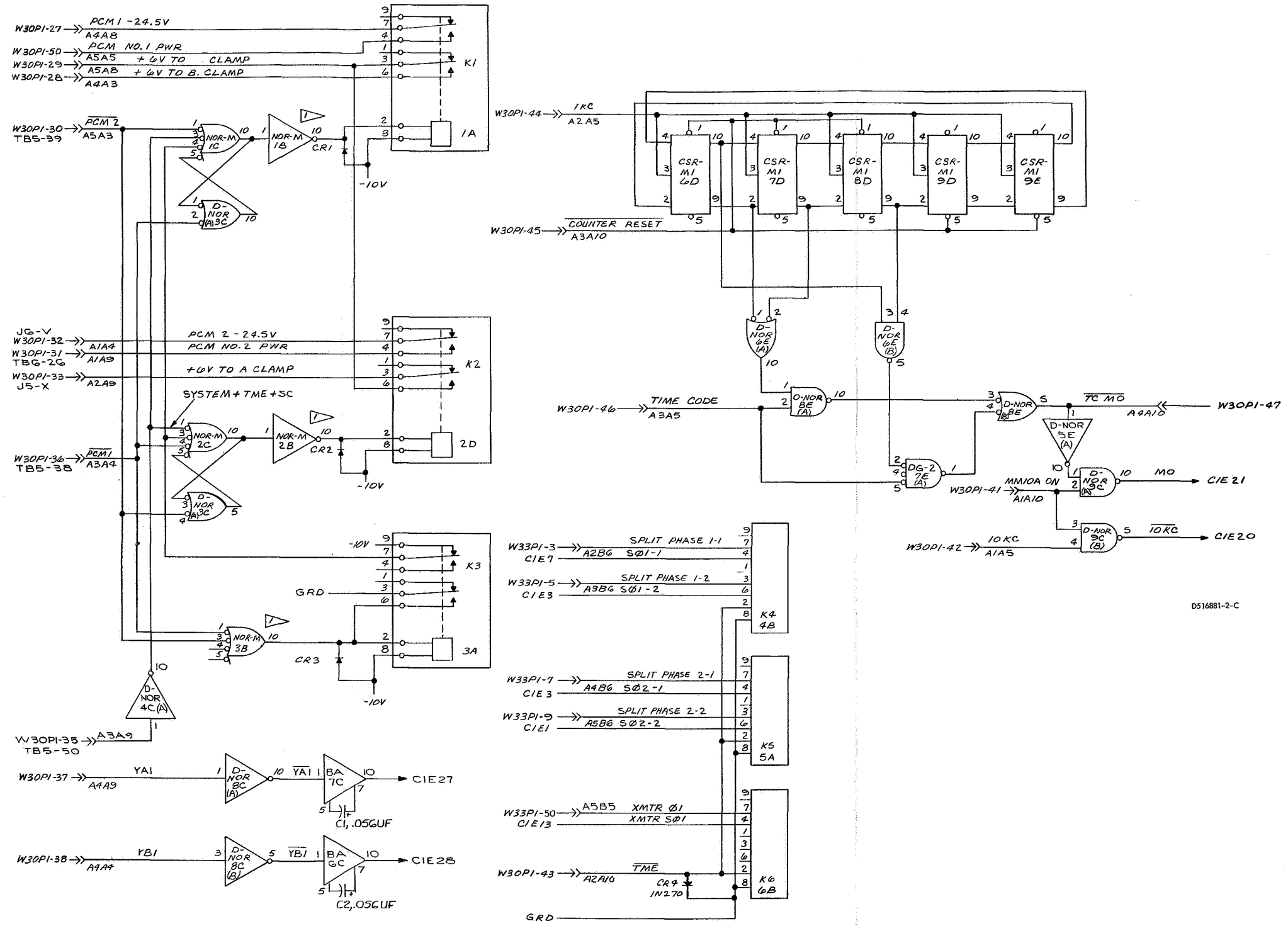


Figure 52. Time Code and Relays, 1A6E, Logic Diagram

NOTES:
1. DO NOT CONNECT PIN 8 TO -10V
2. R1, R2 ARE 10K, 1/4W, ± 5%

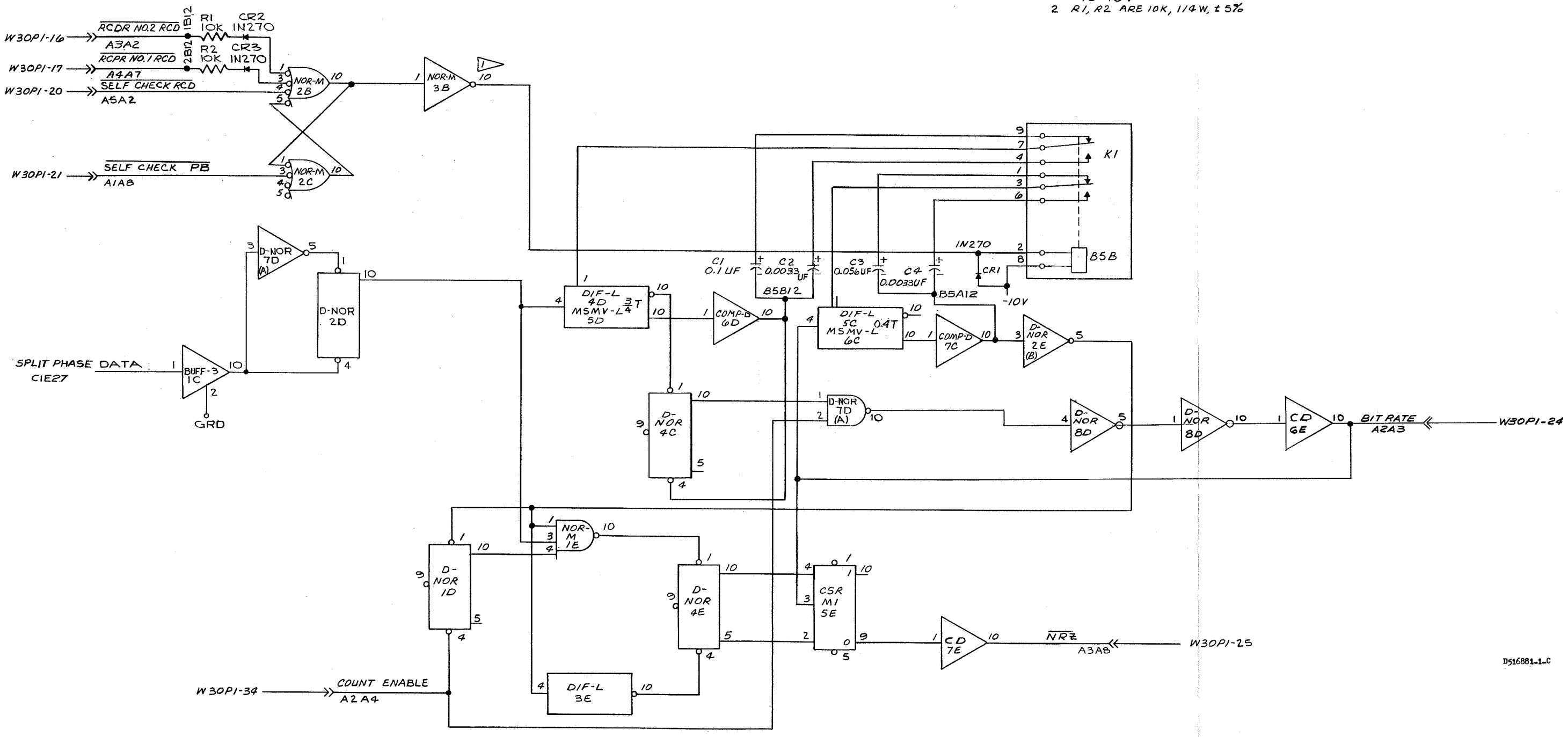


Figure 53. Bit Synchronizer, 1A6B, Logic Diagram

FOLDOUT FRAME 1

FOLDOUT FRAME 2

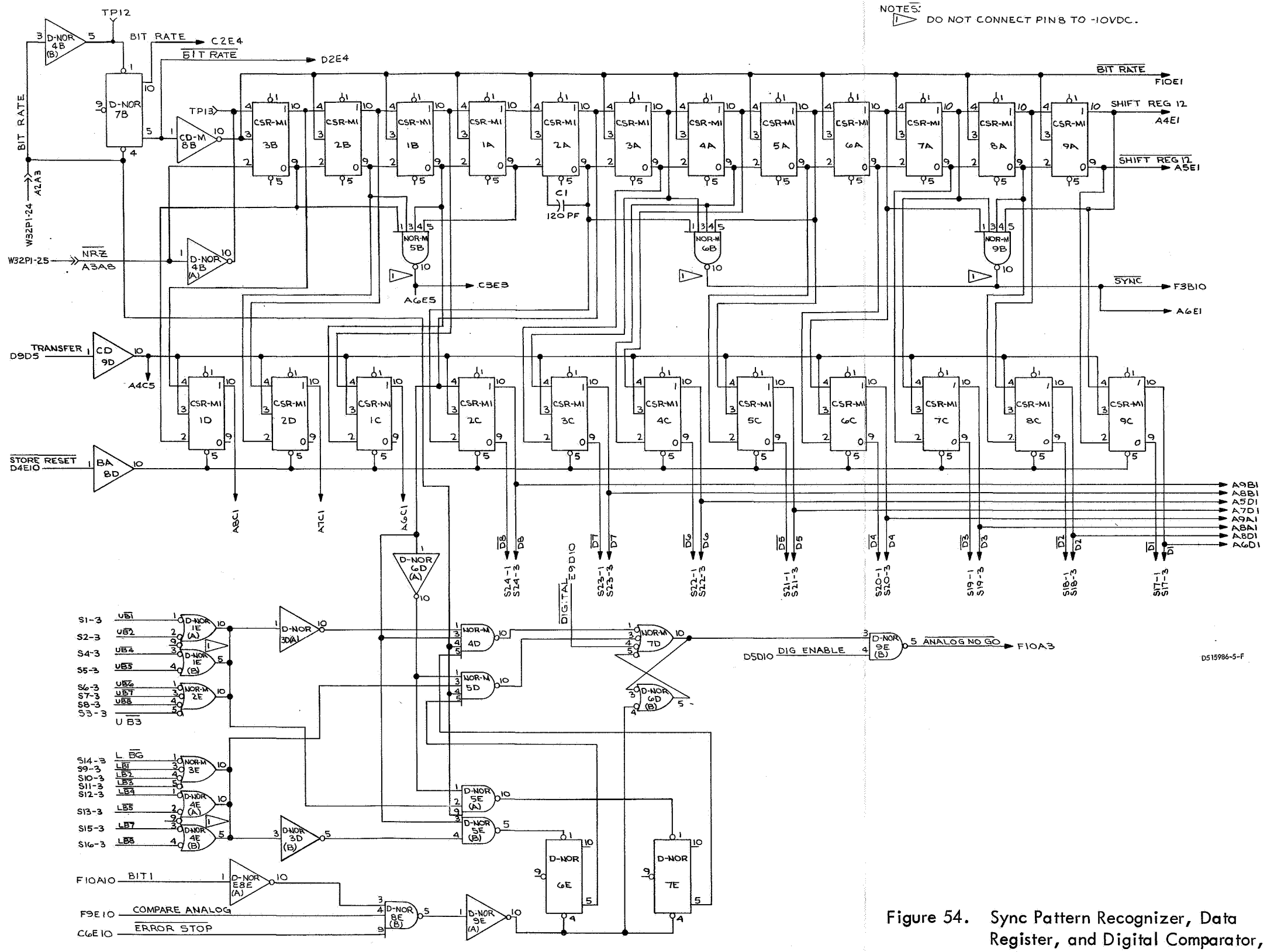


Figure 54. Sync Pattern Recognizer, Data Register, and Digital Comparator, 1A3E, Logic Diagram

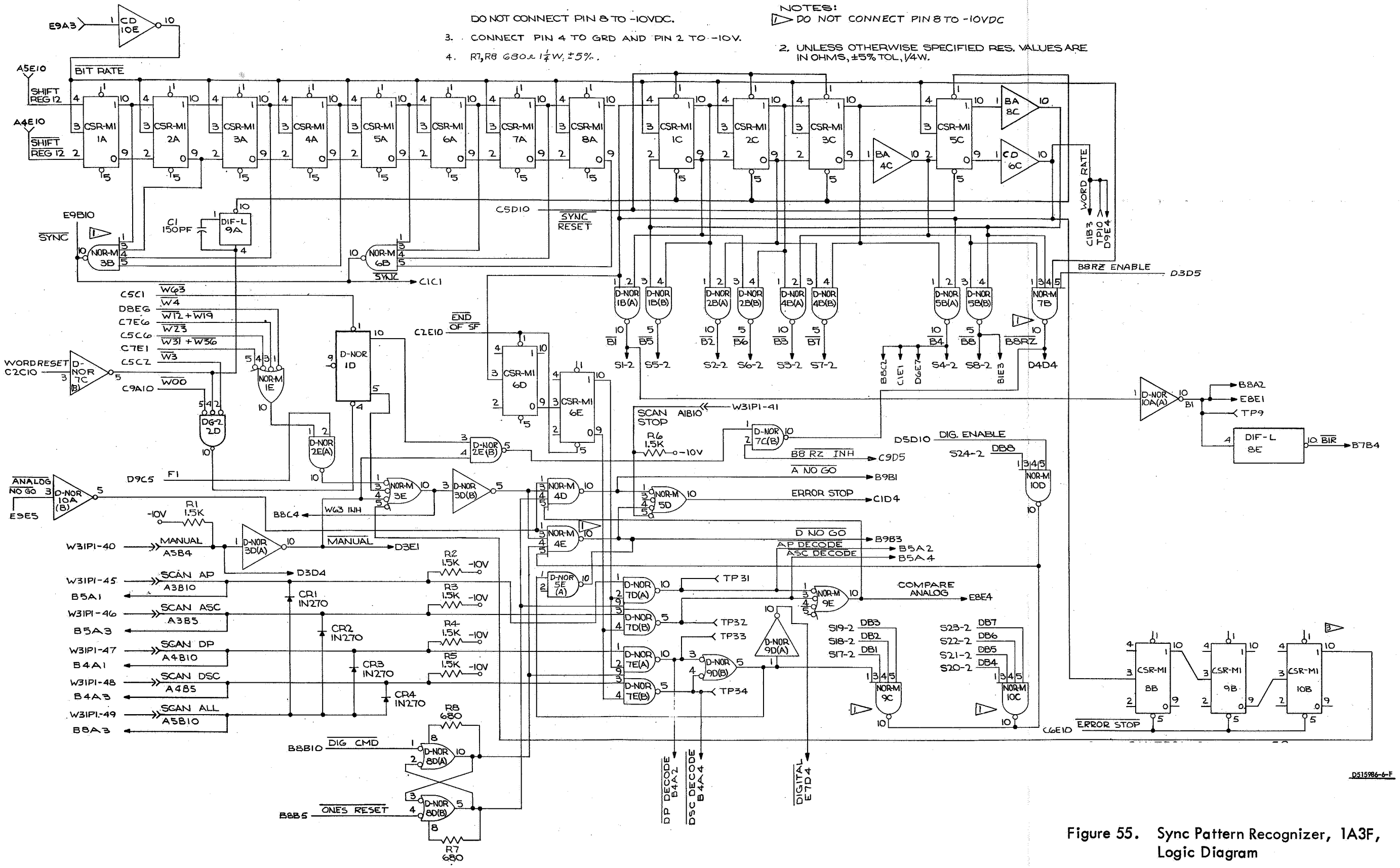


Figure 55. Sync Pattern Recognizer, 1A3F, Logic Diagram

NOTE:
1. PARTIAL REF. DESIGNATIONS ARE SHOWN. FOR COMPLETE DESIGNATION, PREFIX WITH UNIT NO. OR SUBASSEMBLY DESIGNATION.

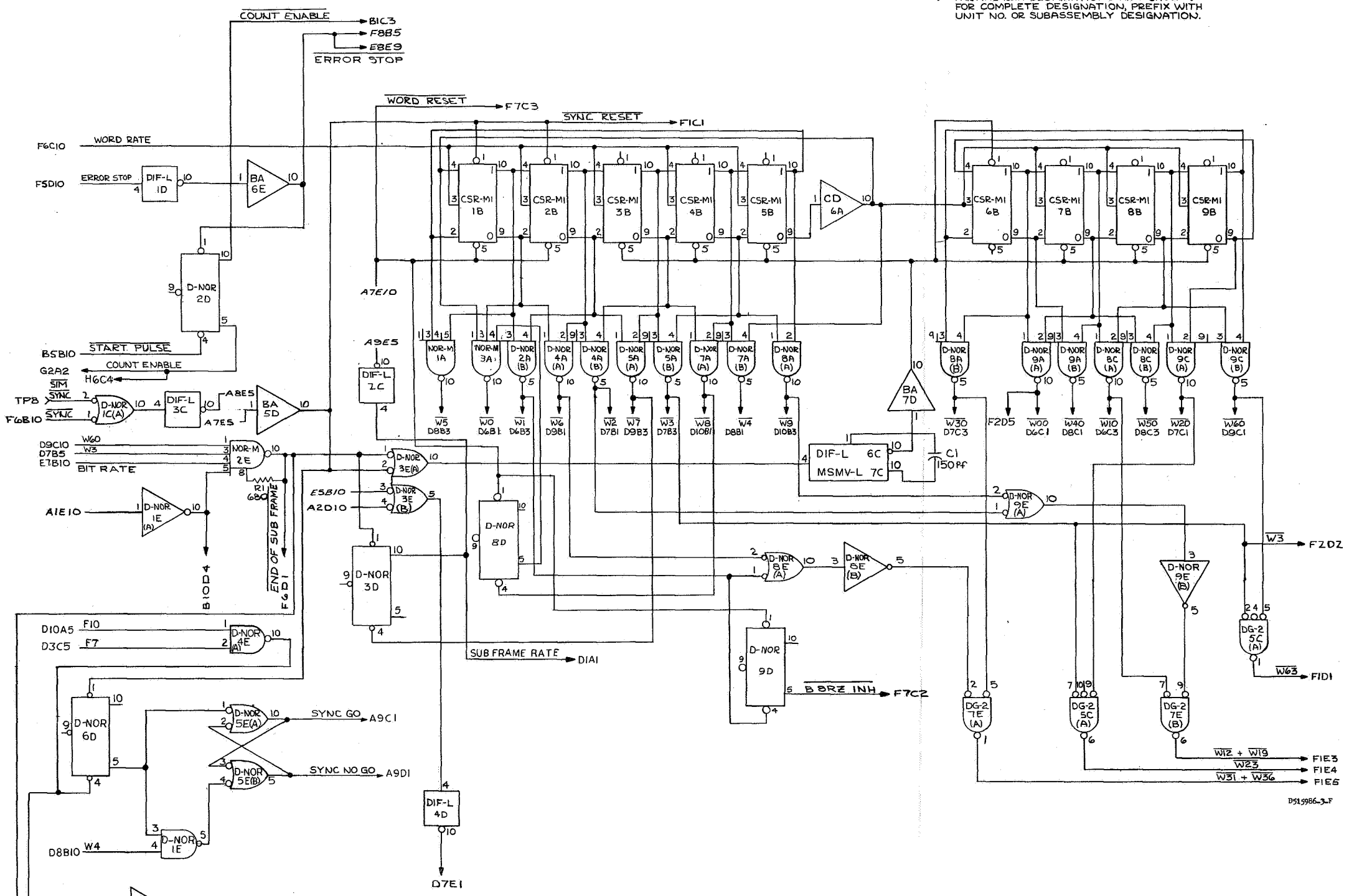


Figure 56. Word Counter Decode Gate, 1A3C, Logic Diagram

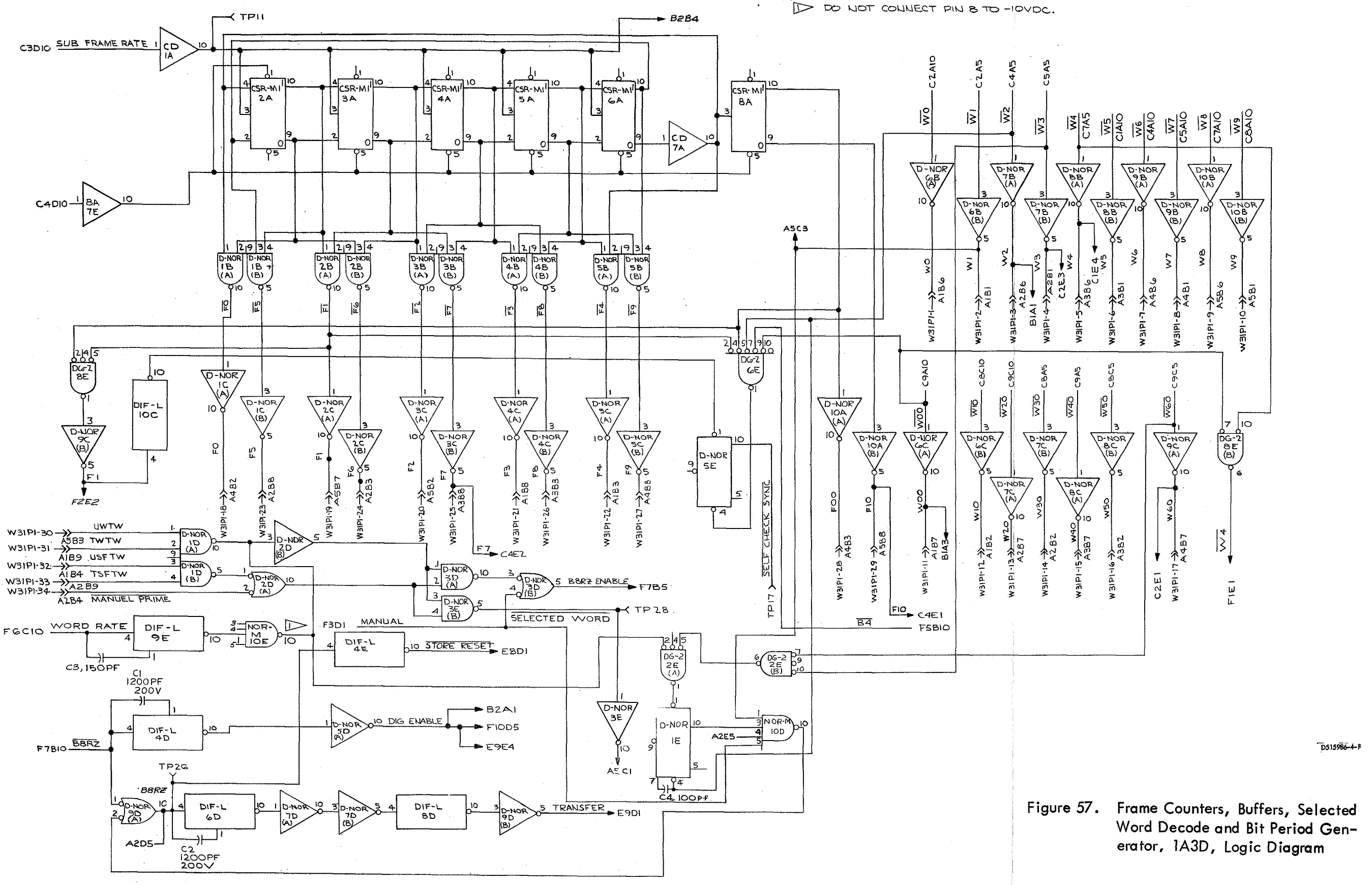
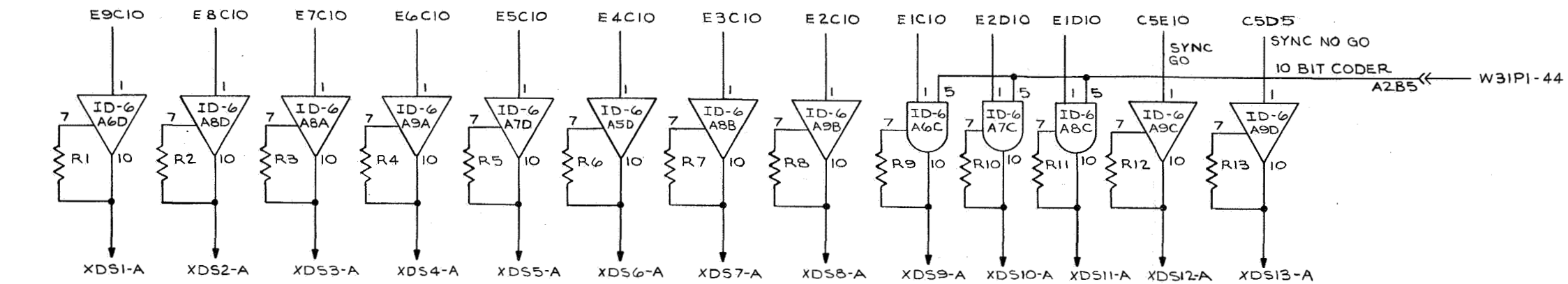
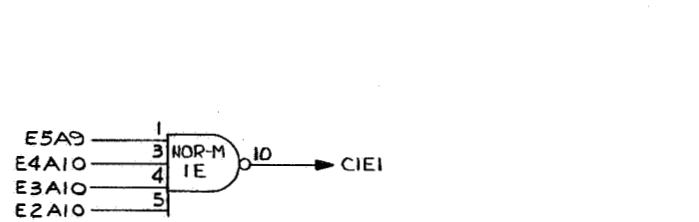


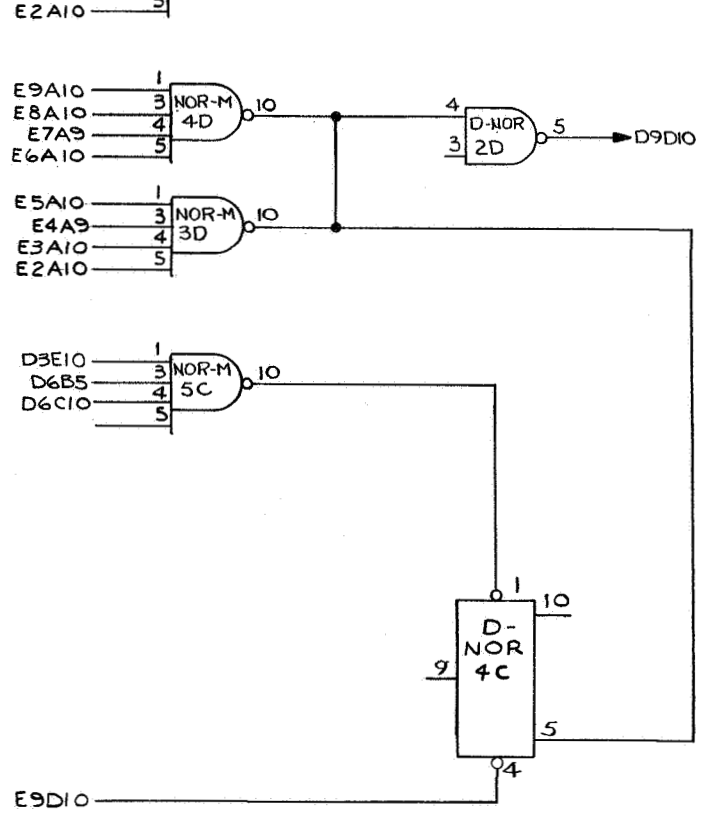
Figure 57. Frame Counters, Buffers, Selected Word Decode and Bit Period Generator, 1A3D, Logic Diagram

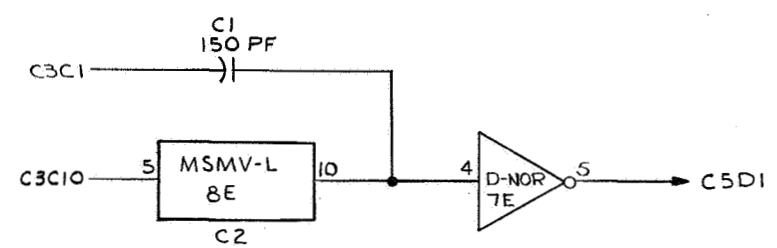
NOTES:

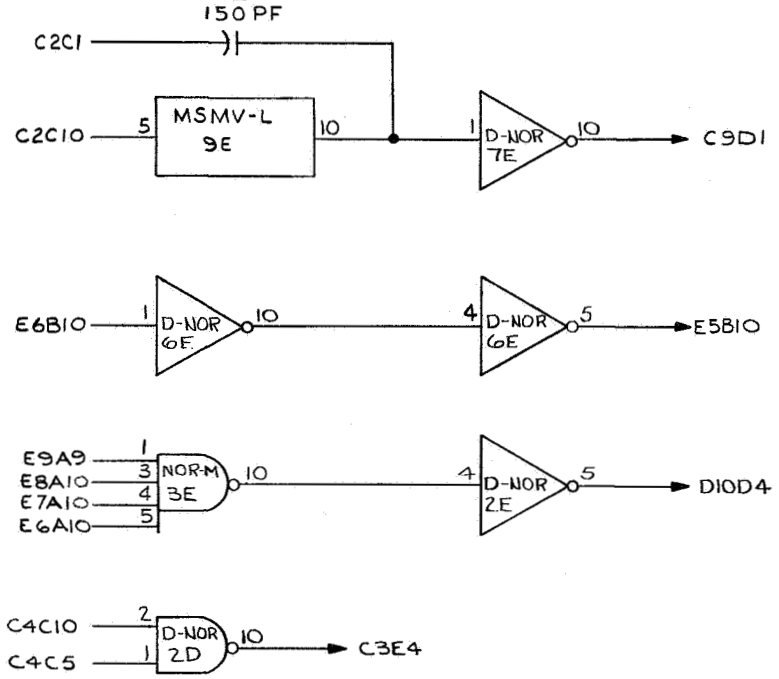
1. R1 THRU R13 ARE 390Ω, 1/4W, ±5%.
2. PARTIAL REF DES ARE SHOWN; FOR COMPLETE DES, PREFIX WITH UNIT NO. OR SUBASSEMBLY DES.

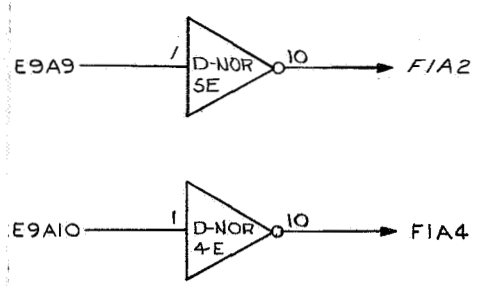












D515986-1-F

Figure 58. Lamp Driver, 1A3A, Logic Diagram

FOLDOUT FRAME 1

FOLDOUT FRAME 2

NOTES:

1. PARTIAL REF DESIGNATIONS ARE SHOWN. FOR COMPLETE DESIGNATION, PREFIX WITH UNIT NO. OR SUBASSEMBLY DESIGNATION.
2. UNLESS OTHERWISE SPECIFIED, RES VALUES ARE EXPRESSED IN OHMS ±5% TOL AND 1/4 WATT.

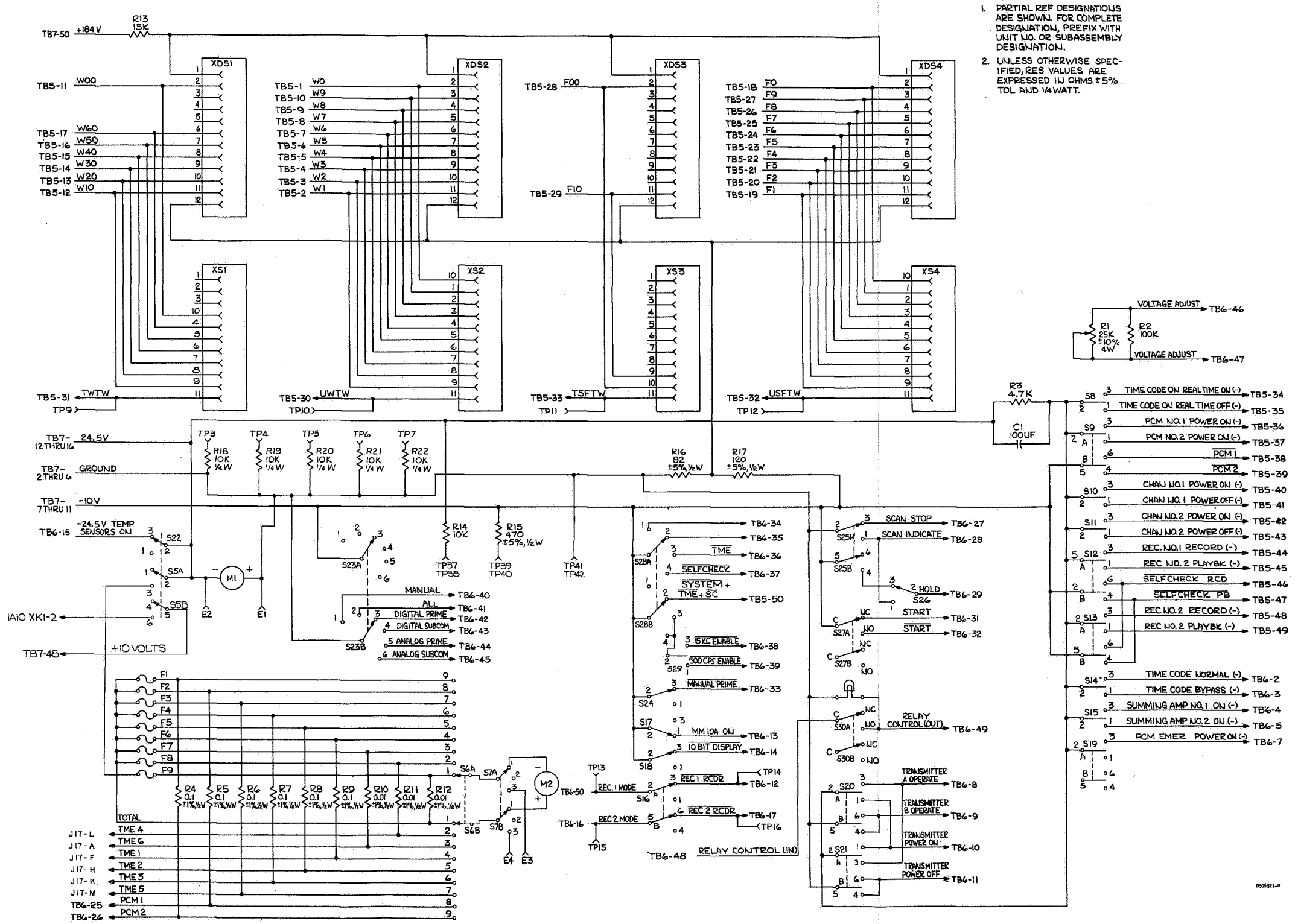


Figure 59. Control Console, 1A5, Logic Diagram

4.3 FUNCTIONAL DESCRIPTION

This paragraph contains the functional description of the BTE. The discussion is limited to a functional block diagram level. The detailed theory of operation can be found in the BTE Instruction Manual delivered under this contract.

Operating in two major modes, manual and scan, the BTE generates and provides simulated signals and commands to the PCM Telemetry Subsystem under test. Primary signal sources are shown in figure 60. The control signals, commands, and timing provided by the BTE are those normally provided by the satellite-borne Nimbus clock. Analog and digital data representing signals obtained from transducers and test points within the Nimbus satellite are simulated by operation of toggle switches and applied to the PCM Telemetry Subsystem. When testing the operation of PCM and TME units separately, the BTE supplies signals that other subsystem components would normally supply. Split-phase Mark-0 data is generated within the BTE to simulate PCM unit outputs when testing individual TME units. During self-check operation, the Mark-0 data can be applied directly to the BTE data reduction and evaluation circuits. The data reduction and evaluation circuits accept the data from the PCM Telemetry Subsystem or the split-phase generator and then comparing this incoming data with preselected analog and digital channel data against established criteria. The results of the data comparison are then displayed on GO/NO GO indicators and supplied to test points for monitoring.

4.3.1. MODES OF OPERATION

4.3.1.1. MANUAL MODE. The manual mode is divided into prime and subcom submodes. When operating in manual mode, a particular word and subframe within the format can be selected from the control console by thumbwheel switches. The BTE continuously scans the data, and when the selected word and subframe time slot occurs within the format, the data word in that time slot is displayed on the data display section of the control panel. When the MANUAL switch is in SUBCOM position, both the word and subframe decode gates are enabled, and only the selected word in the selected subframe is displayed on the control panel. When the MANUAL switch is in PRIME mode position, the subcom decode gates are disabled and the selected word from every subframe is displayed, thereby enabling the operator to examine each prime word in each subframe.

4.3.1.2. SCAN MODE. The scan mode is divided into five submode scan operations: (1) scan all words, (2) scan digital prime words, (3) scan digital subcom words, (4) scan analog prime words, and (5) scan analog subcom words. The BTE scans the type of data selected and upon command, compares it against either the analog or digital tolerance switches to determine if the data is within tolerance. If the data is not within tolerance, an error condition exists. In the scan mode, the BTE can be programmed to either stop on an error or to indicate the error by visual display. When the BTE is programmed for error stopping and an error is detected, the BTE stops and displays the erroneous data word, the word number, and subframe number. To resume operation, the START switch is depressed to enable the BTE to again start scanning data. The SCAN switch is set to the INDICATE position when it is not desired to stop the BTE. In this mode, the BTE does not stop, but produces a pulse for each error detected. The data

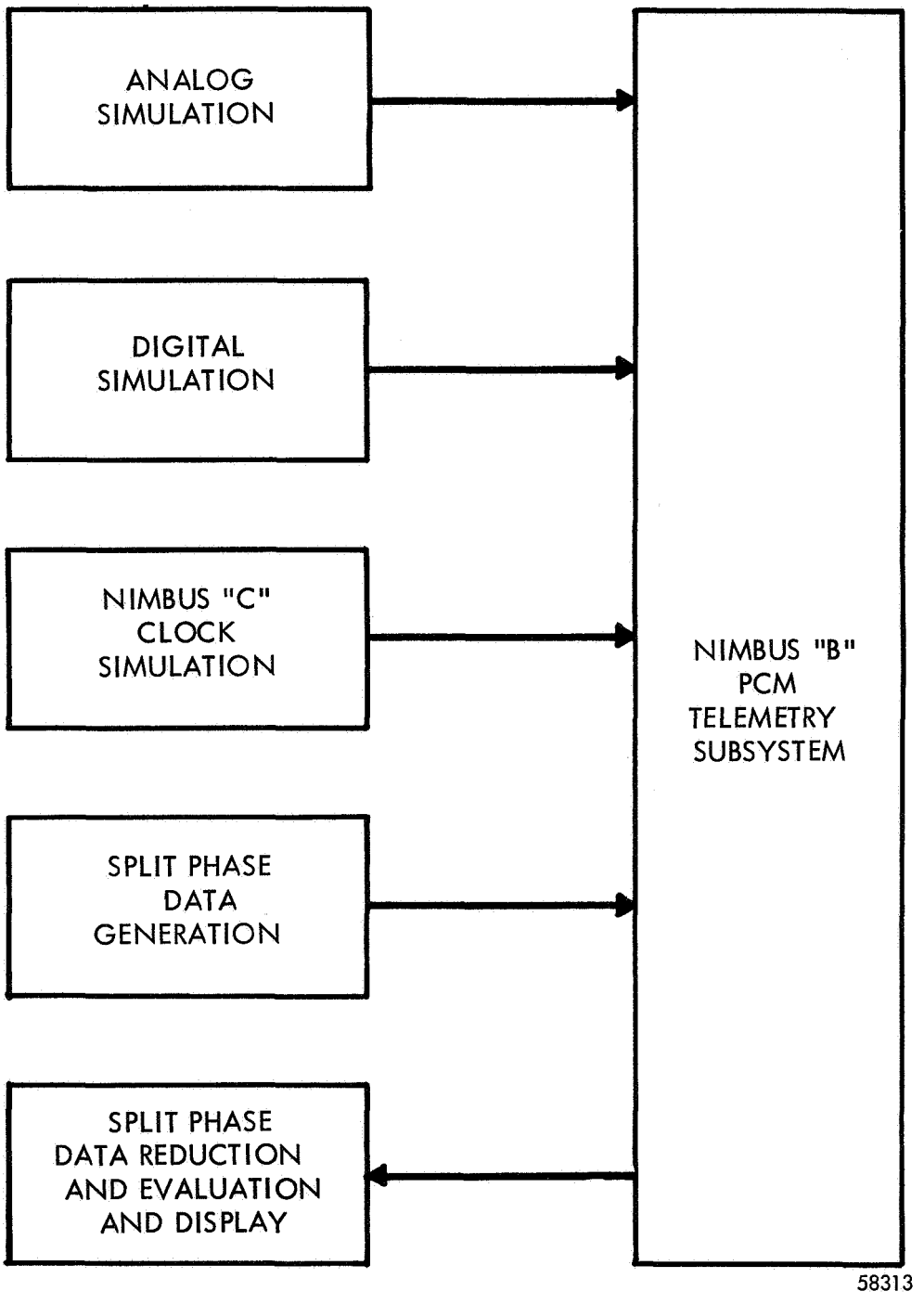


Figure 60. Bench Test Equipment, Simplified Block Diagram

GO/NO GO indicator lights on the control panel indicate whether the data is within tolerance. When the data is out of tolerance, the NO GO indicator is energized until the data returns to the prescribed tolerances set by the analog and digital switches. The DATA ERROR switch is set to the HOLD position when the system is in the indicate mode and when it is desired to have only one error indicated. When the DATA ERROR switch is in the HOLD position, the first error detected by the BTE energizes the data NO GO light. The NO GO light remains energized until the START switch is depressed to reset the BTE error detection circuits.

4.3.2. GENERAL THEORY OF OPERATION

Figures 61 and 62 illustrate BTE signal flow and detailed block diagrams, respectively. The BTE supplies several simulated outputs to the PCM Telemetry Subsystem including the Nimbus C clock; whereupon, the telemetry subsystem using these inputs returns the data to the BTE in split-phase Mark-0 form for comparison against preselected channel data. A more detailed theory of operation can be found in the BTE manual delivered under this contract.

System timing generated in the Nimbus clock simulator and the time-code generator timing are derived from a 240 KC crystal controlled oscillator. The oscillator output is counted down to provide phase 1 and 2 100 cps, 500 cps, 10 cps, and 1 cps clock pulses for transmission to the PCM Telemetry Subsystem. Two time code formats are generated: MO and MM10A. These are derived from the 100 KC and 10 KC Nimbus clock simulator outputs.

Simulated time codes are selected through BTE control panel switch settings. The switches can be set to either the ONE or ZERO position with a resulting bit in the associated time slot set to either a ONE or ZERO. Time code MO is a serial data train of negative pulses that are either six milliseconds (ONE bit) or two milliseconds (ZERO bit) wide. (Time code format is shown in figure 63). A 10-millisecond time slot is allotted for each time code bit. Units of seconds data appears in the first 100 milliseconds of the time code format, and tens of seconds, units of minutes, tens of minutes, units of hours, and tens of hours data occupy successive 100-millisecond time slots. The unused portions of the time code format contains ZERO's. The time code generator comprises a strobe generator, a 5-stage shift register and decode gates, and a PDM (pulse duration modulation) encoder. The generator driven by the 10 KC and 100 KC Nimbus clock outputs, produces a switch selected code which is converted to PDM for transmission to the PCM Telemetry Subsystem and time code MM10A modulator. The MM10A signal is a 10 KC clock modulated by the MO time code output. All time codes require switch selection.

When the BTE is checking the TME unit separately, the BTE supplies split-phase data to the TME unit in place of the data normally supplied by the PCM unit. The split-phase data is also selected through BTE control panel switch settings, and generated by the split-phase Mark-0 data generator. The generator comprises a 4-stage counter and decode gates, a group of data word switches, and a split-phase converter, or data generator. The 4-stage counter functions as a word generator and is driven by the bit rate clock train. The word generator is decoded to produce eight sequential bits during each word period. The eight word bits are routed through the data switches where selected logic levels are inserted into each bit before application to the split-phase converter. Each data bit is sampled during the first half of its duration. The sample determines the output state of the split-phase Mark-0 output.

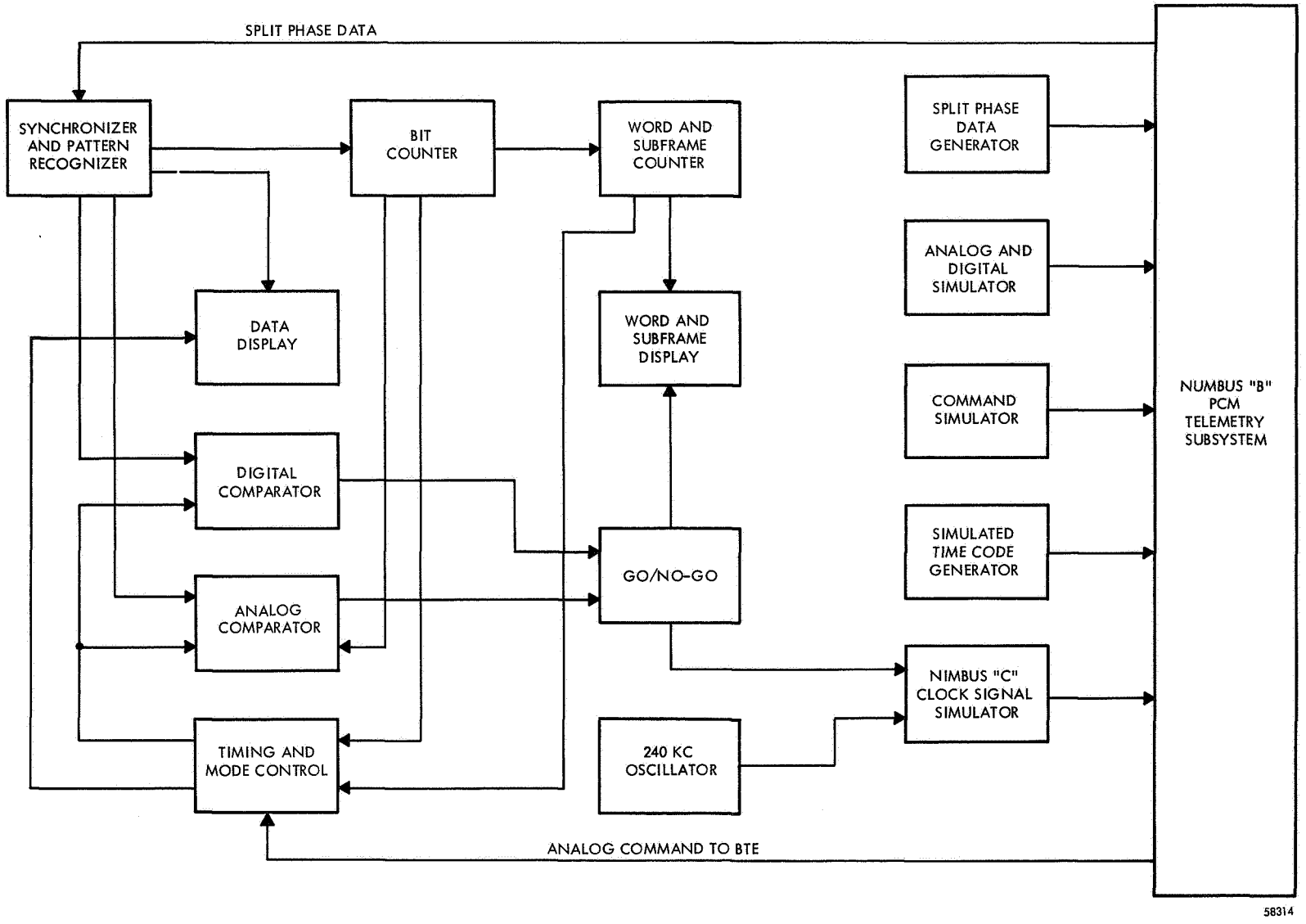


Figure 61. Bench Test Equipment, Signal Flow Diagram

FOLDOUT FRAME 1

FOLDOUT FRAME 2

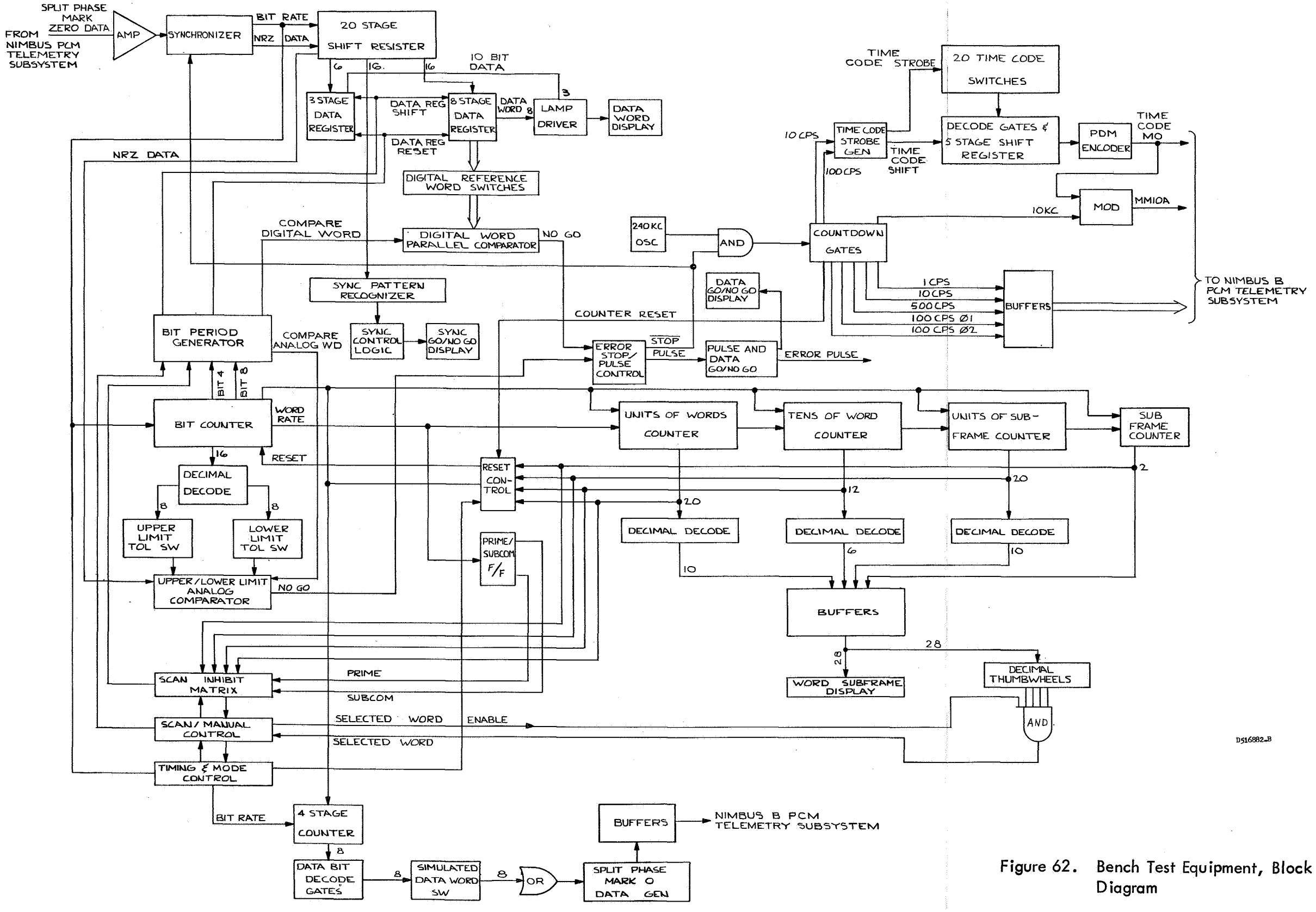


Figure 62. Bench Test Equipment, Block Diagram

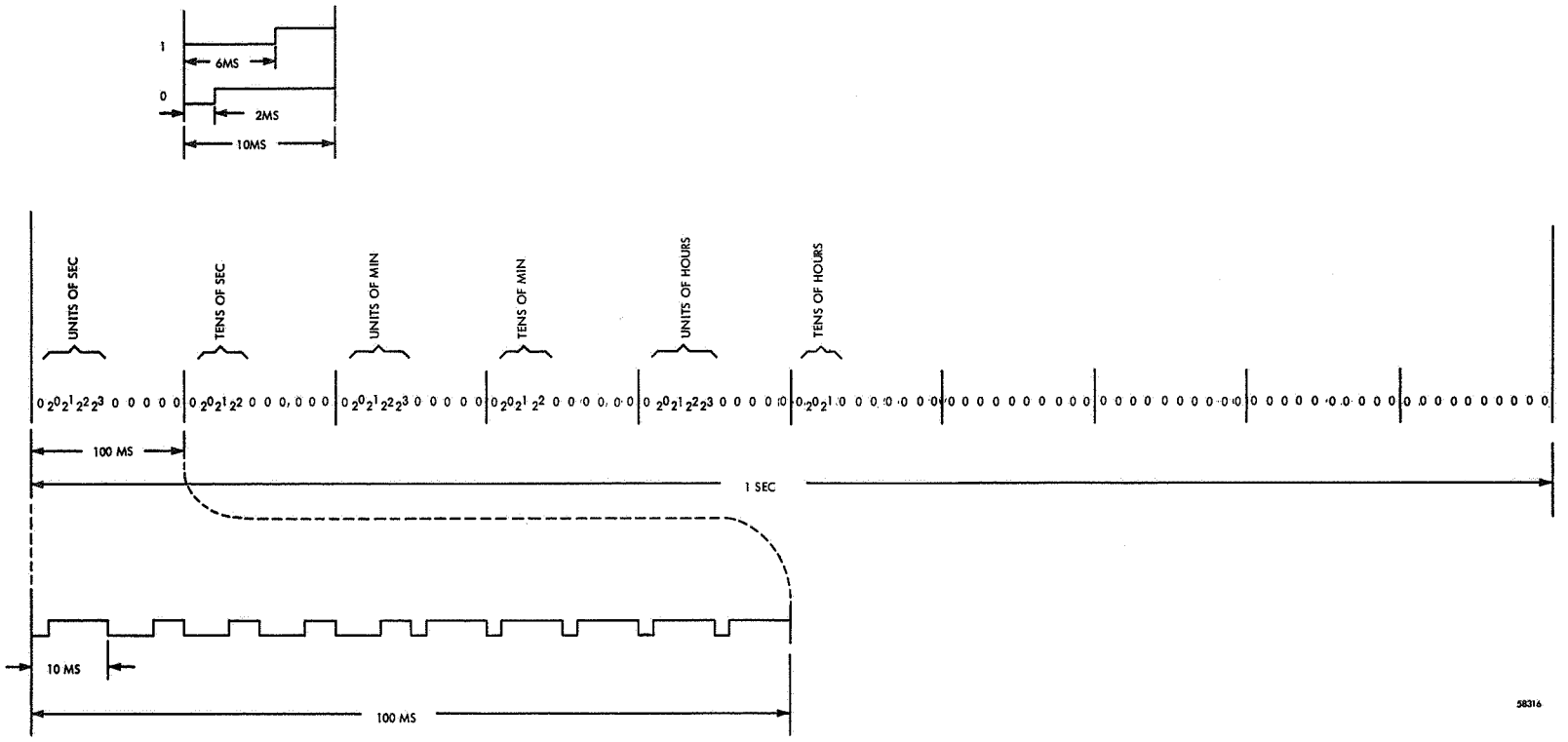


Figure 63. Time Code MO Format

Analog and digital simulators provide the data normally received by a PCM unit from the Nimbus satellite. Twenty-one simulated analog prime channels, nine digital prime words, and 40 digital subcom words are switch selected at the control console.

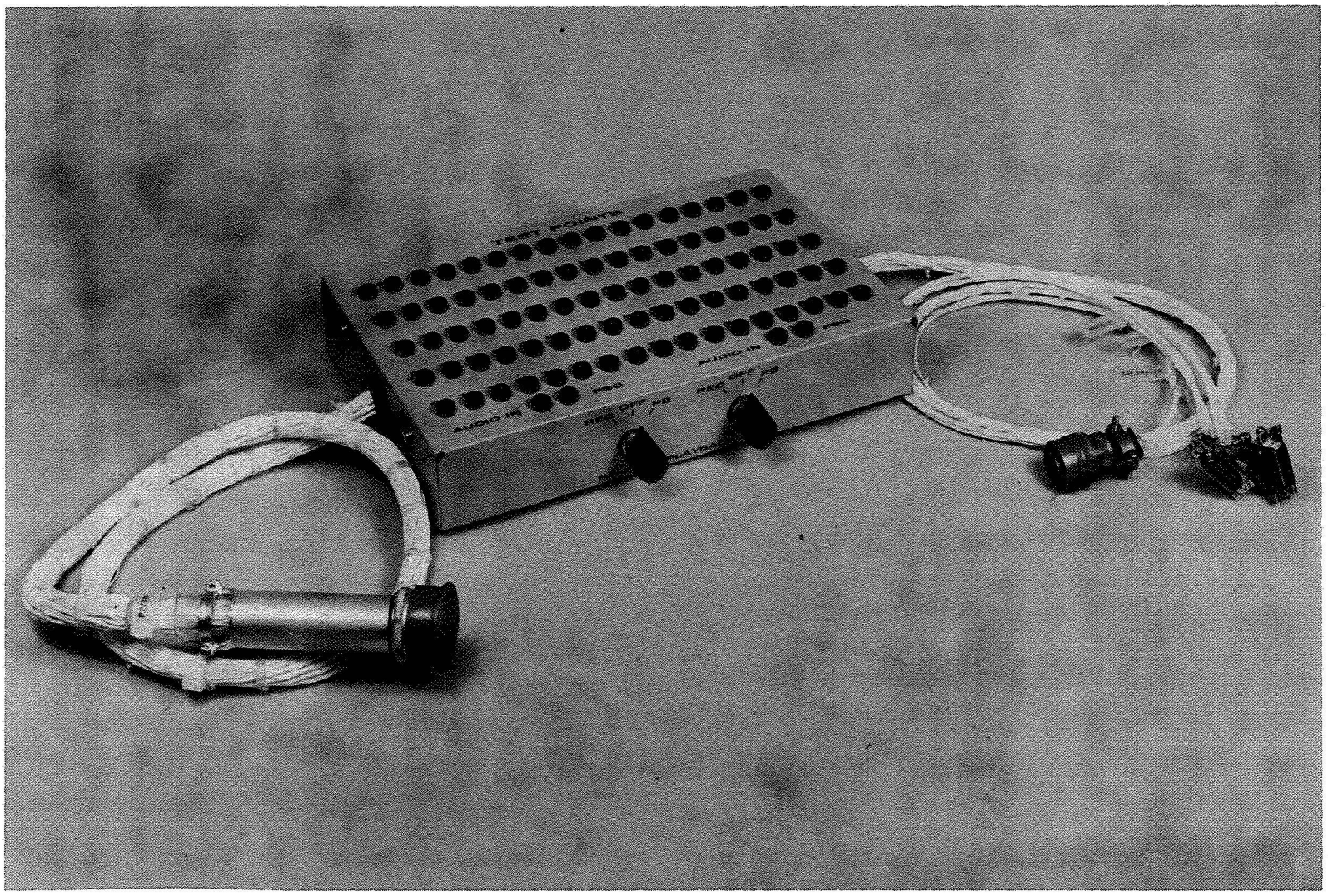
With the BTE operating in the Scan-All-Words Mode, the split-phase data from the PCM Telemetry Subsystem is accepted by the bit synchronizer where it is conditioned for conversion to NRZ data. The conversion process also generates a bit rate which is applied, with the NRZ data, to a 20-stage shift register. The NRZ data from the synchronizer is then shifted into the shift register. Bit rate is also routed to a bit counter which develops a word-rate output for every eight bit-rate pulse inputs. The word-rate output of the bit counter is routed to word and subframe counters which count the words and subframes within a major frame. The contents of the word and subframe counters are decoded by decimal decoders which provide buffered outputs to drive word and subframe displays on the control console. The sync pattern recognizer receives parallel outputs from the shift register. The sync pattern circuitry then decodes each valid pattern as it is placed in the register. Two types of sync are received. The sync decoder continuously looks for the 16-bit sync pattern which is contained in word 62.5, word No. 1, and the first half of word No. 2. When this 16-bit pattern occurs, a sync pulse is generated to set the bit counter and word counter. The unit also searches for ID sync which is contained in the last half of word No. 2. When ID sync (0000) occurs and normal sync is also present, an ID sync pulse is generated to set the subframe counter. When the subframe counter has been reset, the BTE is in synchronization.

The PCM subsystem generates a 260-microsecond pulse 1 millisecond prior to every digital word coming into the test set. This pulse is used to enable the digital comparator. The analog comparator is enabled only when the pulse is not present. NRZ data from the 20-stage shift register is parallel-loaded into an eight-stage holding register which is part of the digital comparator. At the same time, data is serially routed through the analog comparator for comparison with the analog upper and lower limit tolerance switch settings on the control panel. Should the data value be greater than the upper limit tolerance setting, or less than the lower limit tolerance setting, an error condition results. If the word is digital, the digital comparator is enabled and compares the data in the holding register with the settings of the DIGITAL REF WORD switches on the control panel. If an exact comparison is not obtained, an error condition results. If the BTE is in the scan stop mode when either of the error conditions occurs, the BTE stops and displays the word and subframe along with the data word in error.

Data displays are controlled by a series of word counters and thumbwheel switches on the control console. The bit counter word rate output drives a word units counter which in turn drives a word tens counter. The output of this counter drives the two subframe counters. Parallel outputs of three of the four counters are decoded through decimal decoding gates. Selected subcommutated channels are displayed on the control console when the selected number is reached by the counters. Since these word counters are driven by the input data bit rate, a particular word can be extracted for display when the counters reach a predetermined decimal count. The selected count is determined through thumbwheel switch settings, and when the correct number is reached, logic levels are applied to the select switches and their outputs are ANDed when enabled by the Scan/Manual Control.

4.3.3. TEST CABLES. Wire lists for each of the test interconnection cables are contained in Radiation cable assembly wire listings Numbers 112851 through 112864. An electrical interconnect box (figure 64) is included in cable W13 to permit easy accessibility to frequently used test points. Switches on the front of the interconnect box permit checkout of the record/playback amplifiers when performing separate tests on the TME unit.

Two 0.1 microfarad capacitors are included in cable W6 and two 0.22 microfarad capacitors are included in the W9 cable to shunt to ground noise spikes that are generated under certain switching conditions. The capacitors are connected in the BTE recorder plugs (W6-P3 and W6-P4) between PI-14 and PI-7 and ground. The capacitors shunt spikes on the 100 cps that are developed due to crosstalk when either channel 1 or 2 are switched to the record mode.



1210-45

Figure 64. Electrical Interconnect Box

SECTION V

NIMBUS B PCM GROUND STATION MODIFICATIONS

5.1. INTRODUCTION

This section discusses the modifications made to the Nimbus B PCM Ground Stations (Systems 1, 3, 4, and 5) under this contract and briefly describes the Ground Stations in the latest configurations. After modification stations 1 and 3 became stations 8 and 7, respectively, stations 4 and 5 retained the same numbers. The modifications to the Ground Stations to accommodate the Nimbus B formatted data were accomplished on a minimum change and individual station approach. Uniformity of system configuration and compatibility with the modifications to the airborne equipment dictated the changes and additions to the PCM Ground Station equipment.

5.2. PCM GROUND STATION CONFIGURATIONS AND EQUIPMENT ALLOCATIONS

Table 13 shows the old and new serial numbers for the Ground Stations (including System 6 previously modified to accommodate the new Nimbus B format) and their respective geographic location. A more detailed description of the equipment configuration for each location is shown in figures 65 through 67.

5.2.1. PHYSICAL DESCRIPTION

The Ground Station equipment is housed in the cabinets shown in figure 6. The equipment contained in each cabinet at each individual site is depicted in figures 65 through 67. Individual illustrations of the principal control panels are shown in figures 68 through 84.

All Ground Stations have identical cabinet 3/4 configurations (housing the Radiation Model 5220A signal conditioner, system control assembly, group synchronizer and power supplies), analog recorder (Brush equipment) cabinets, Mincom recorder cabinet, and digital event recorder cabinets. Each system is equipped with time code display units. Time code data is presented on a Nixie panel and on event recording traces. Simulation and test equipment including a PCM signal simulator, oscilloscope, frequency counter, and RF signal generator is contained in cabinet 5 for all systems except in the van configuration of System 8. The simulator for System 8 is contained in Cabinet 6, which also contains the time code display and digital decommutator. In the Systems 4, 5, 7, and 8 configurations, Cabinet 6 contains the time code display and digital decommutator.

5.2.2 FUNCTIONAL BLOCK DIAGRAM DISCUSSION (Figure 85)

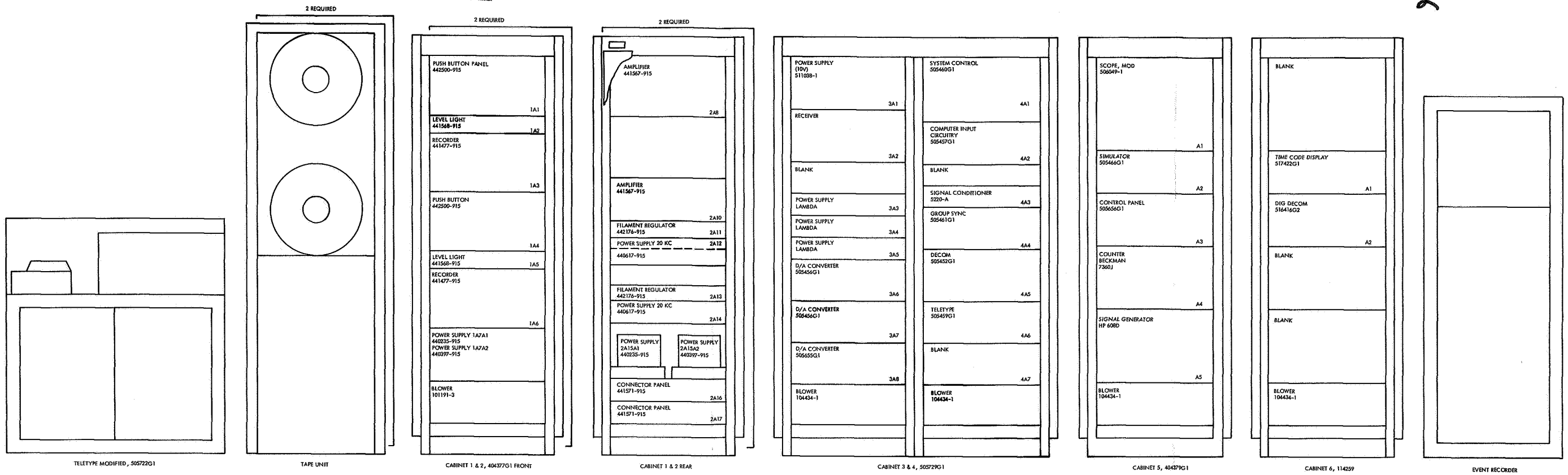
The Nimbus B PCM Ground Station receives and processes telemetered PCM data including time code data from the Nimbus B Satellite System. The data is processed real time at a 500 cps (split phase/single SP/S) bit rate or stored for later playback and processed at a 15 kc (SP/S) bit rate.

Table 13. PCM Ground Station Modifications

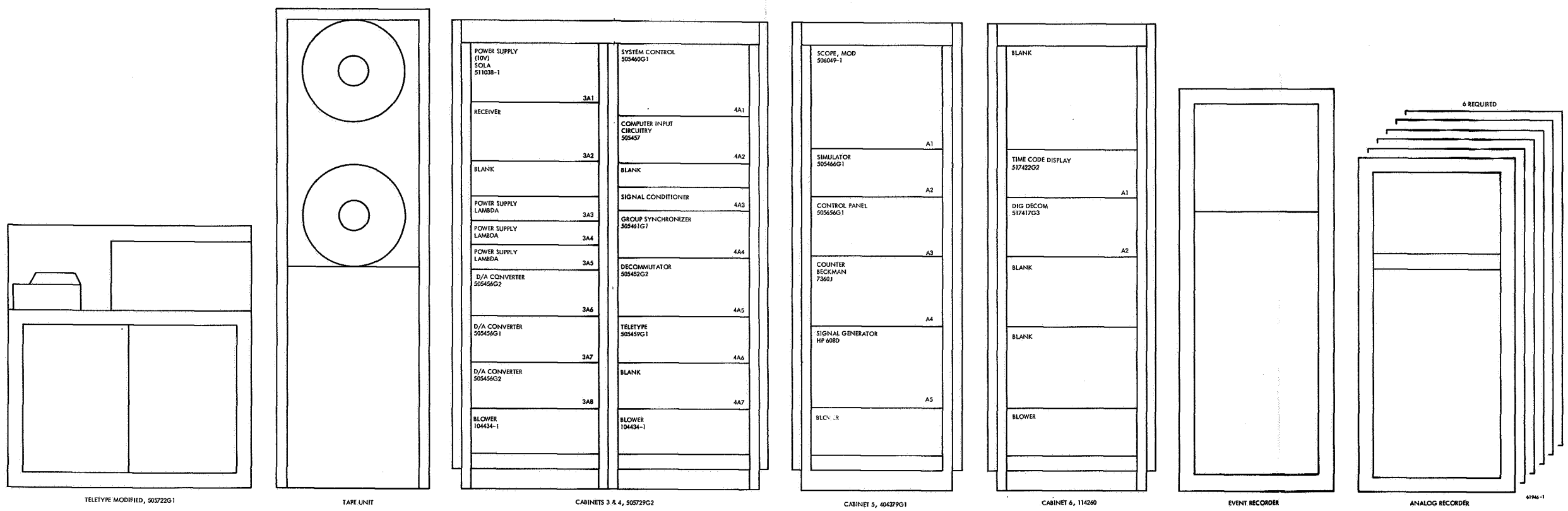
Old Station No.	Location	New Station No.	Summary Nimbus B - Modification
1	Valley Forge, Pa. (Van Station)	8	a. Modify existing 3/4 cabinet assemblies for Nimbus B. 1. Replace Bit Sync with 5220A unit. 2. Modify System Control, Group Sync, Anal. Decom. and Computer Input Circuitry. 3. Cabinet wiring and cabling. b. Added Digital Decom and TC Display Assemblies as Cabinet 6. c. Simulator updated and modified for Nimbus B and relocated in Cabinet 6. d. Added Event Recorder Cabinet Assembly.
2	Valley Forge, Pa. (Control Room)	6	a. Previously modified for Nimbus B (Feb. 1966). b. Field Service liaison to incorporate latest changes to maintain system-to-system uniformity.
3	Valley Forge, Pa. (Classroom)	7	Same as for System 1/8 a. - d.
4	Alaska (Gilmore Creek)	4	Fabricated field kits to: a. Modify existing 3/4 cabinet assemblies for Nimbus B. 1. Replace Bit Sync with 5220A unit. 2. Modify System Control, Group Sync, Anal. Decom. and Computer Input Circuitry. 3. Cabinet wiring and cabling. b. Modify simulator for Nimbus B. c. Add Cabinet 6 with Digital Decom and TC Display. d. Add Event Recorder Cabinet Assembly.
5	Washington, D. C. (Goddard)	5	Same as for System 4.

FOLDOUT FRAME

FOLDOUT FRAME 2



NIMBUS B GROUND STATION SYSTEM 4 (506813 G1) ALASKA (FAIRBANKS, ALASKA)



NIMBUS B GROUND STATION SYSTEM 5 (506813 G2) GODDARD, (GODDARD SPACE FLIGHT CENTER, GREENBELT, MARYLAND)

Figure 65. Nimbus B Ground Station Configurations (Systems 4 and 5)

FOLDOUT FRAME 1

FOLDOUT FRAME 2

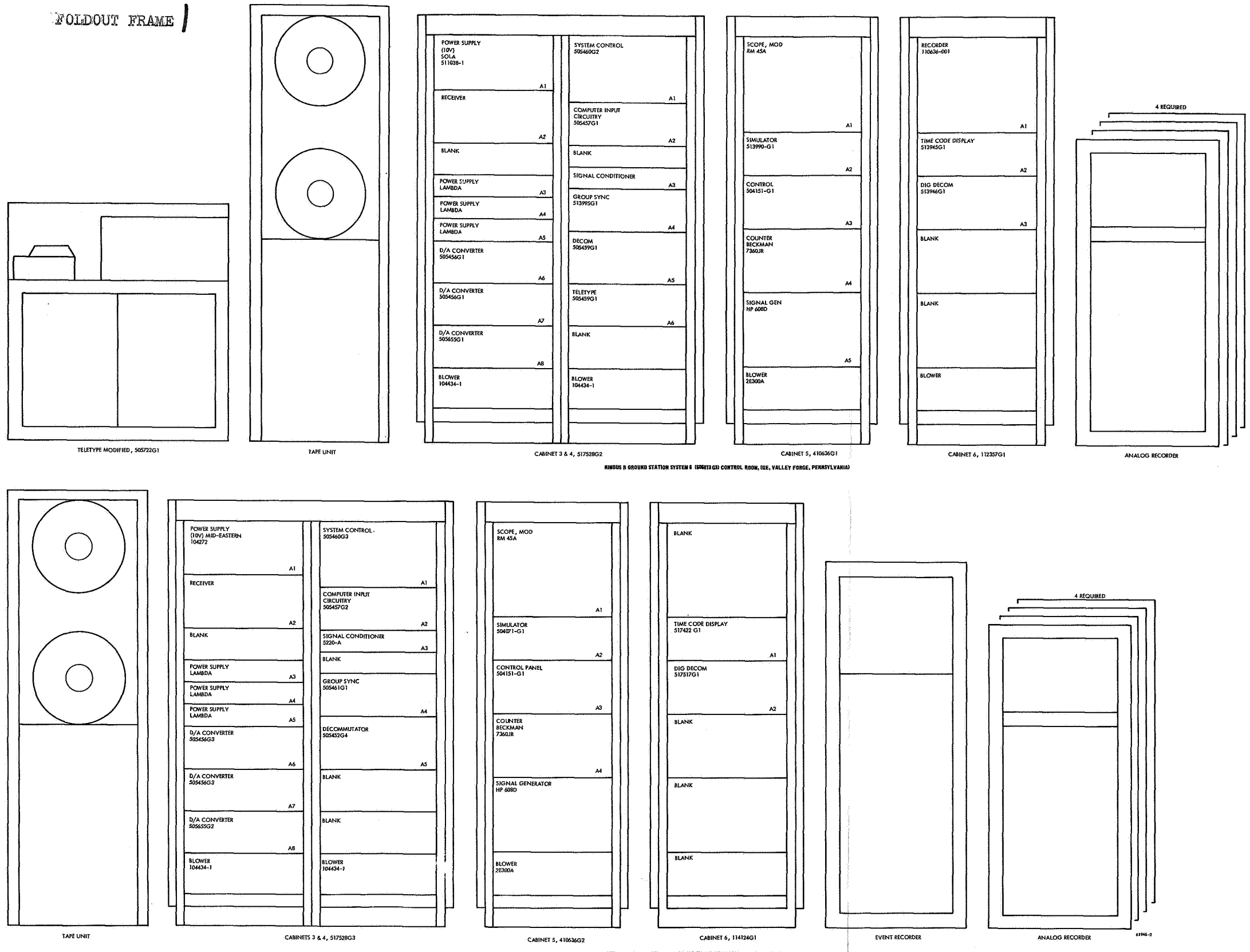


Figure 66. Nimbus B Ground Station Configurations (Systems 6 and 7)

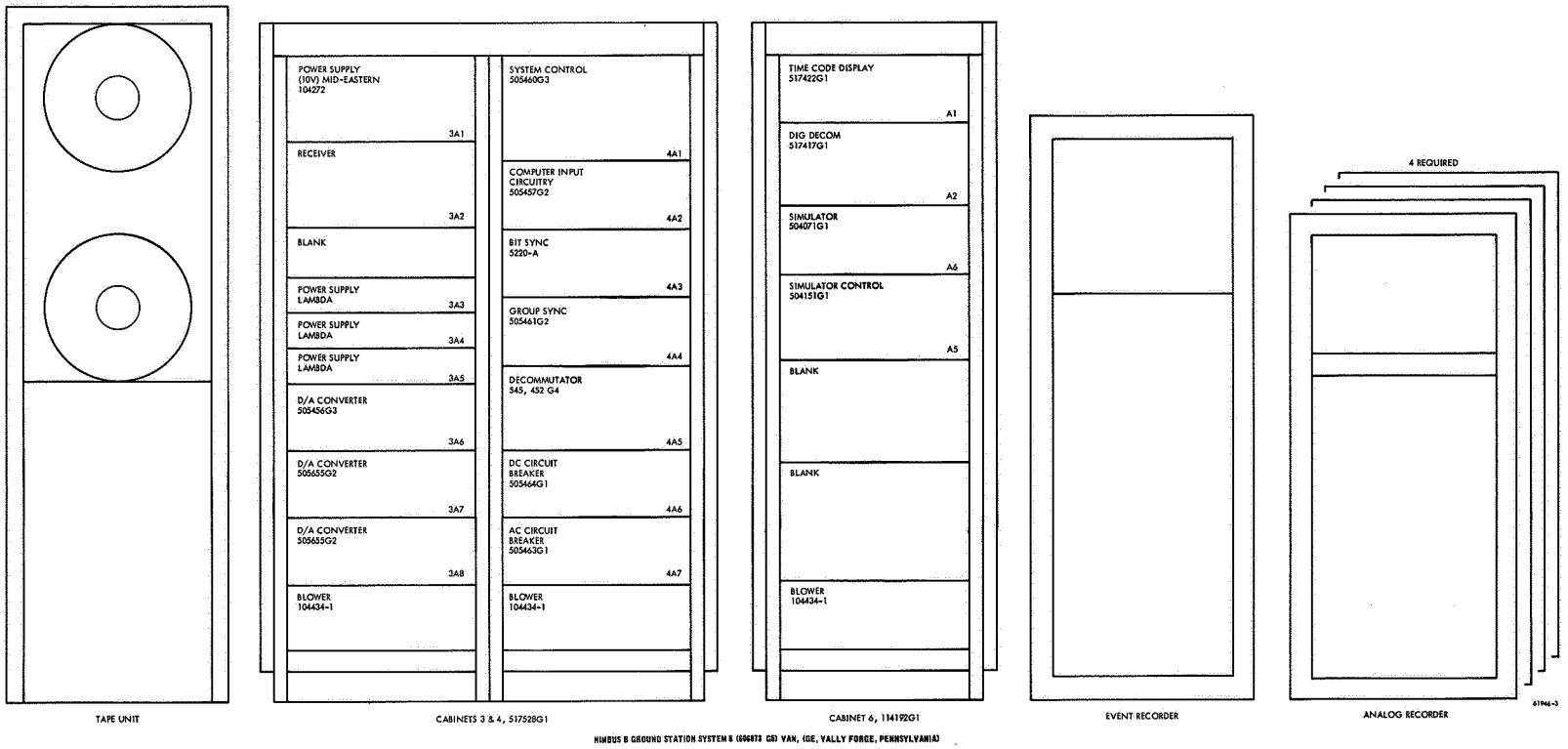


Figure 67. Nimbus B Ground Station Configurations (System 8)

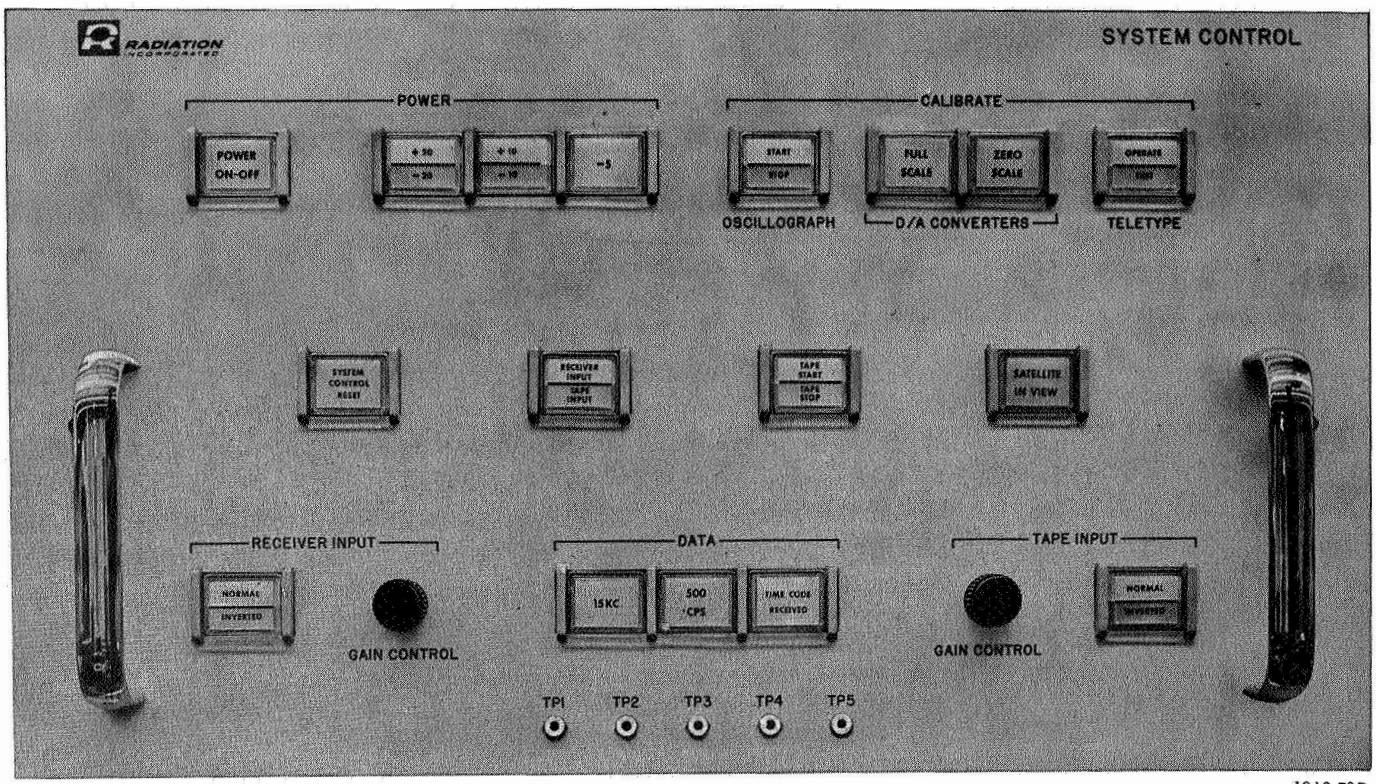


Figure 68. System Control Front Panel

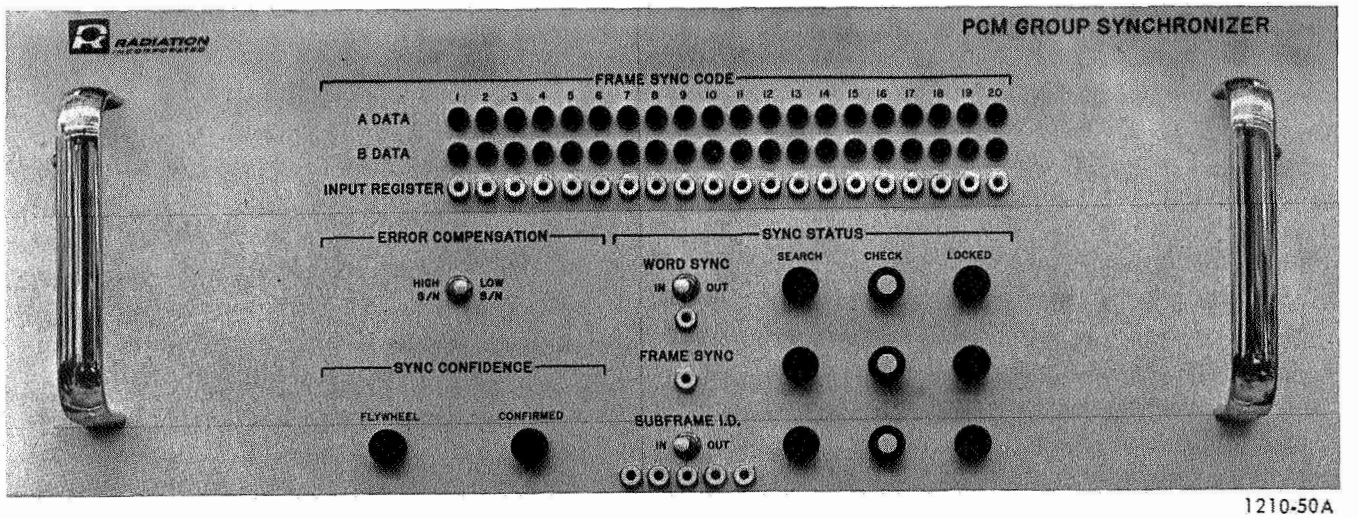
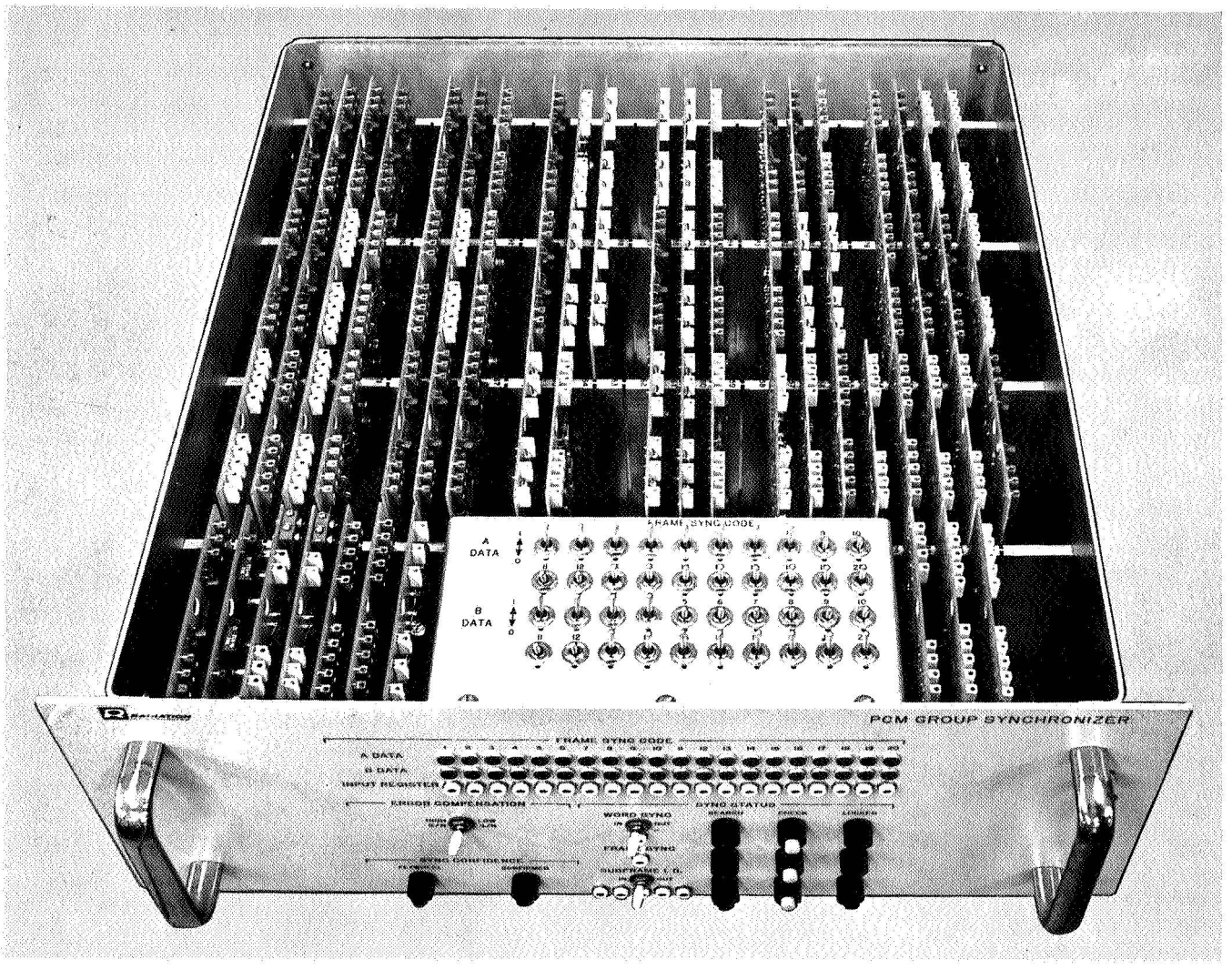
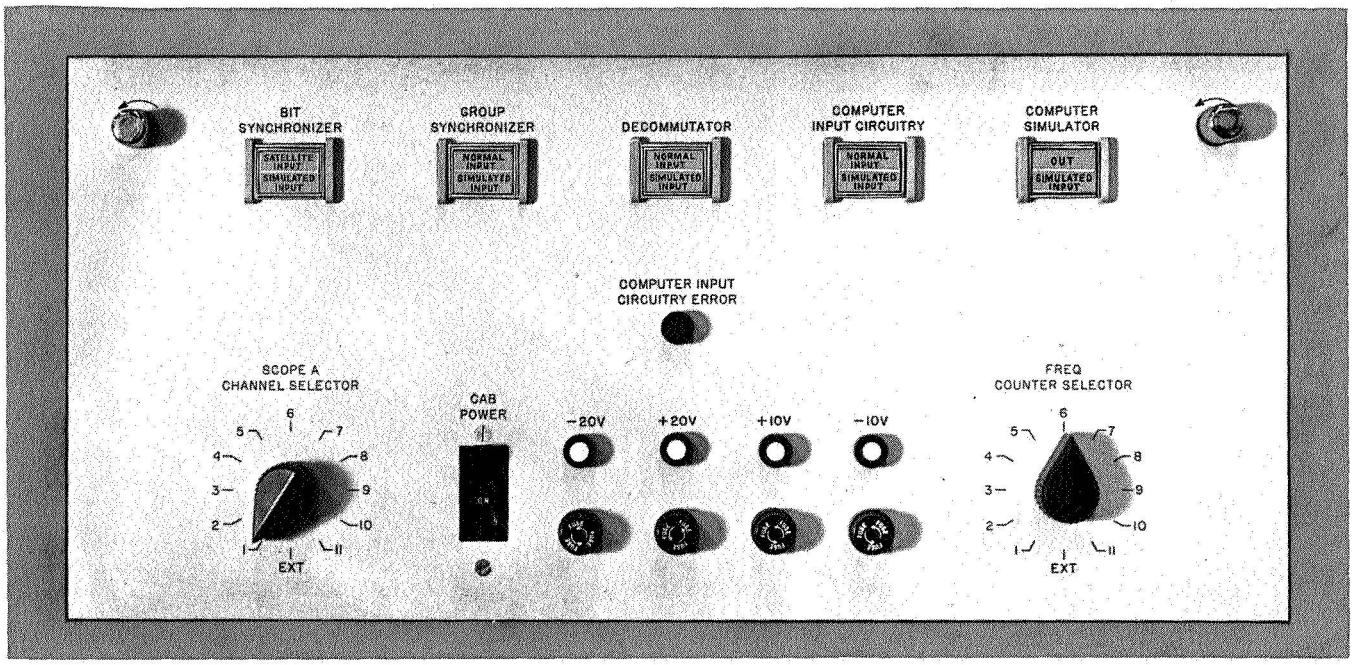


Figure 69. Group Synchronizer Front Panel



1416-212

Figure 70. Group Synchronizer Drawer Panel



1416-231B

Figure 71. Simulator Panels (Systems 4 and 5)

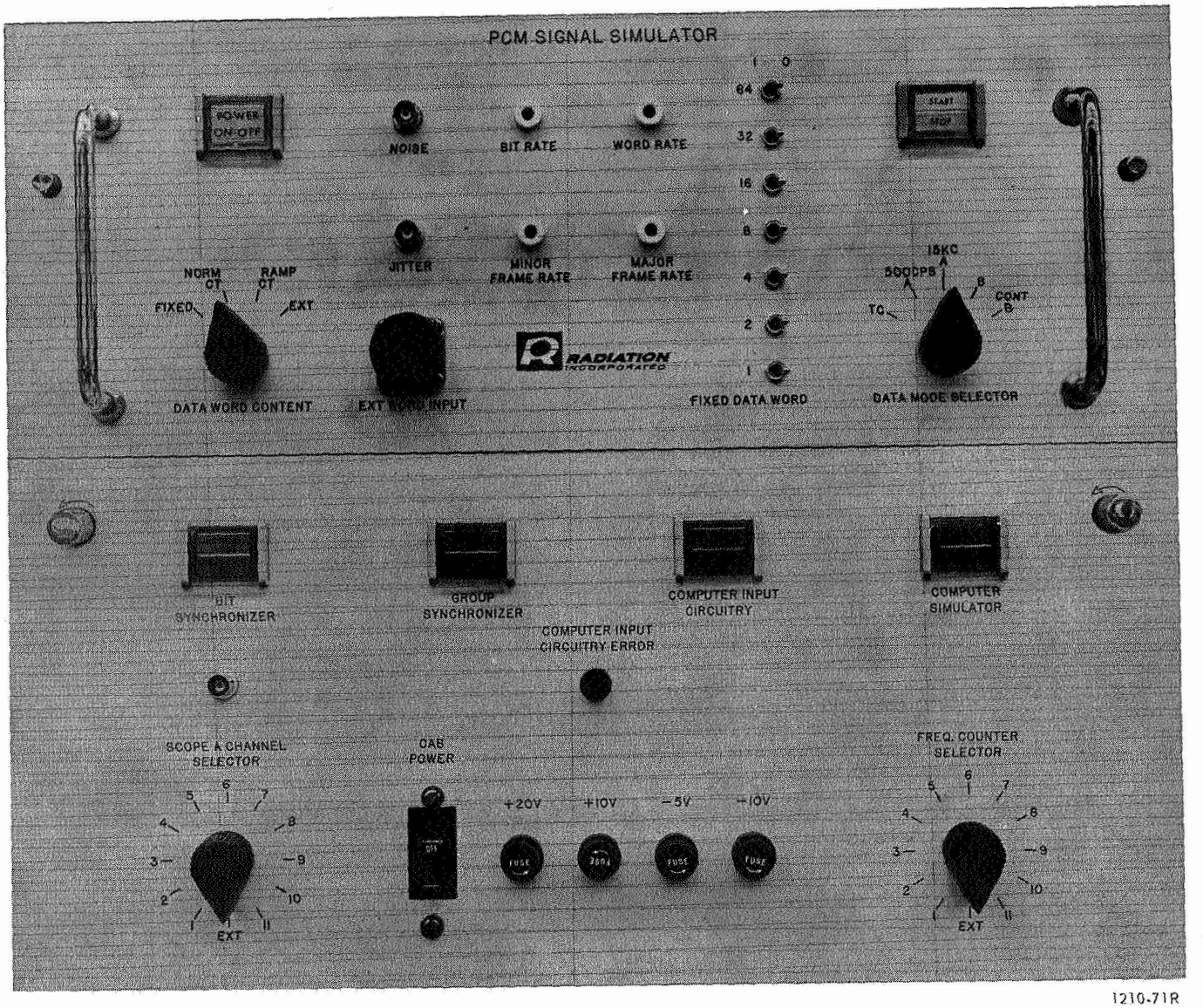


Figure 72. Simulator Panels (Systems 7 and 8)

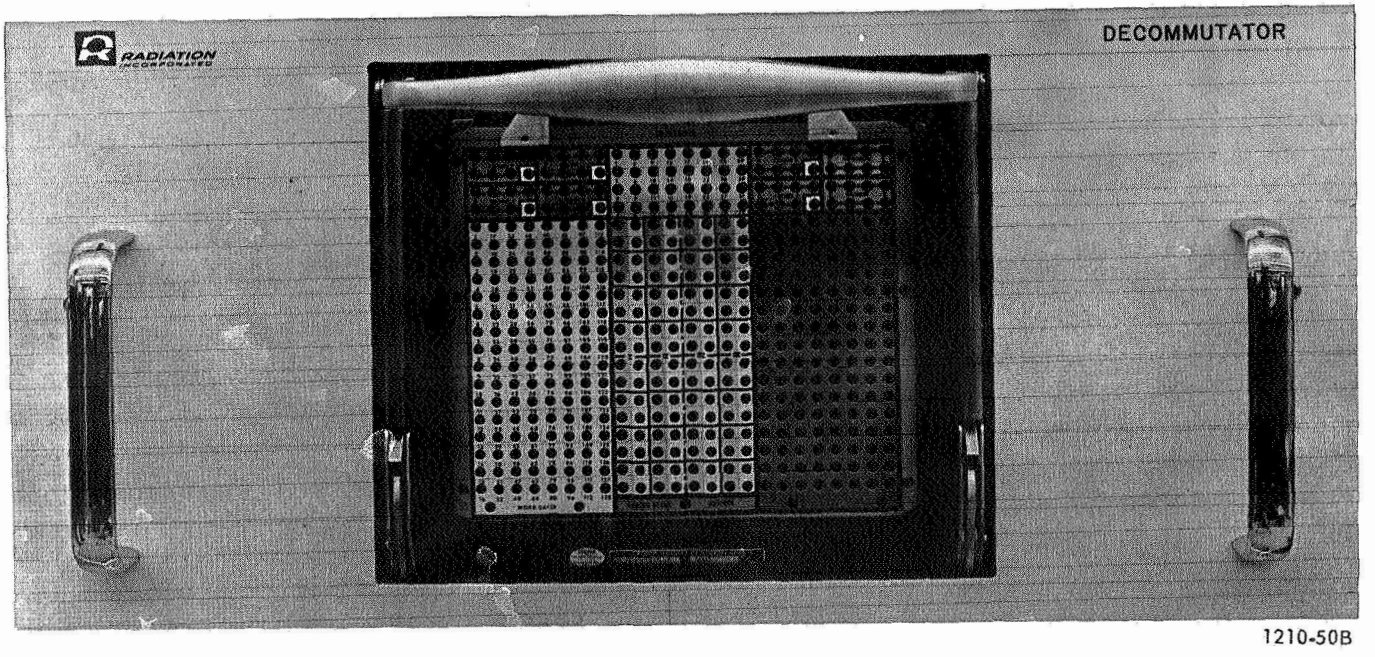


Figure 73. Analog Decommutator Front Panel

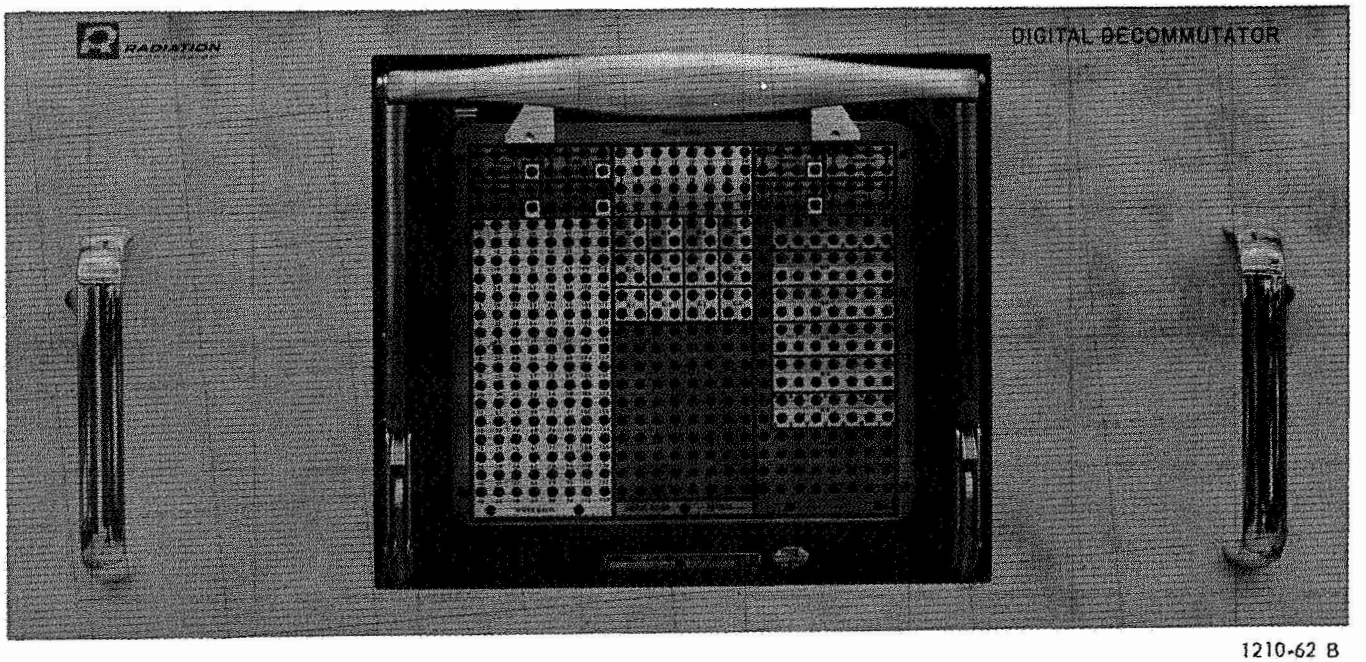


Figure 74. Digital Decommutator Front Panel

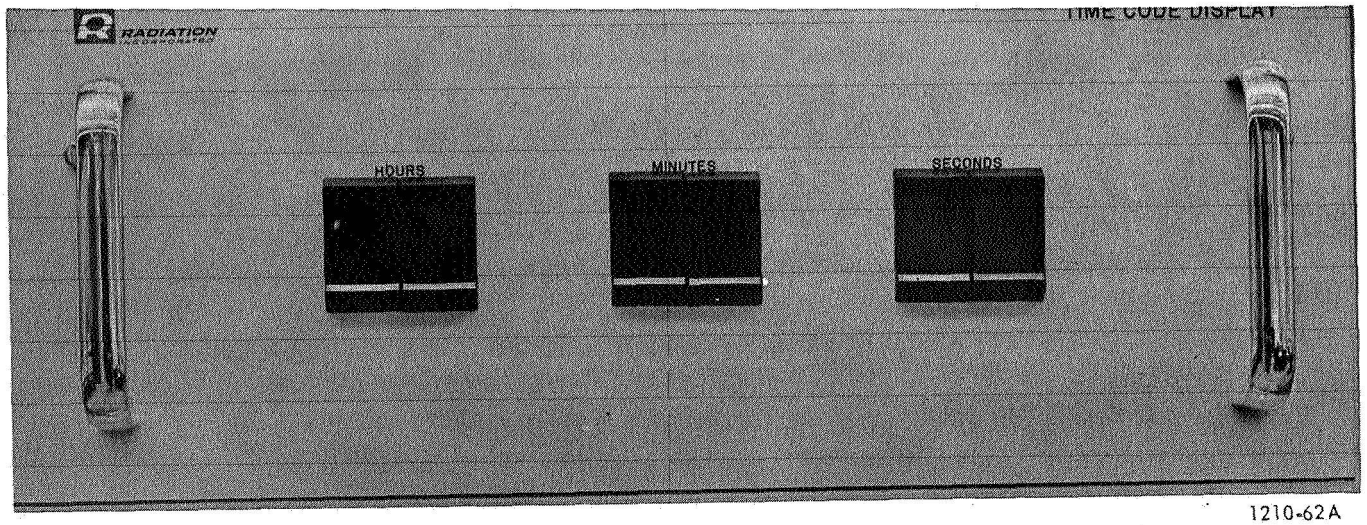


Figure 75. Time Code Display Front Panel

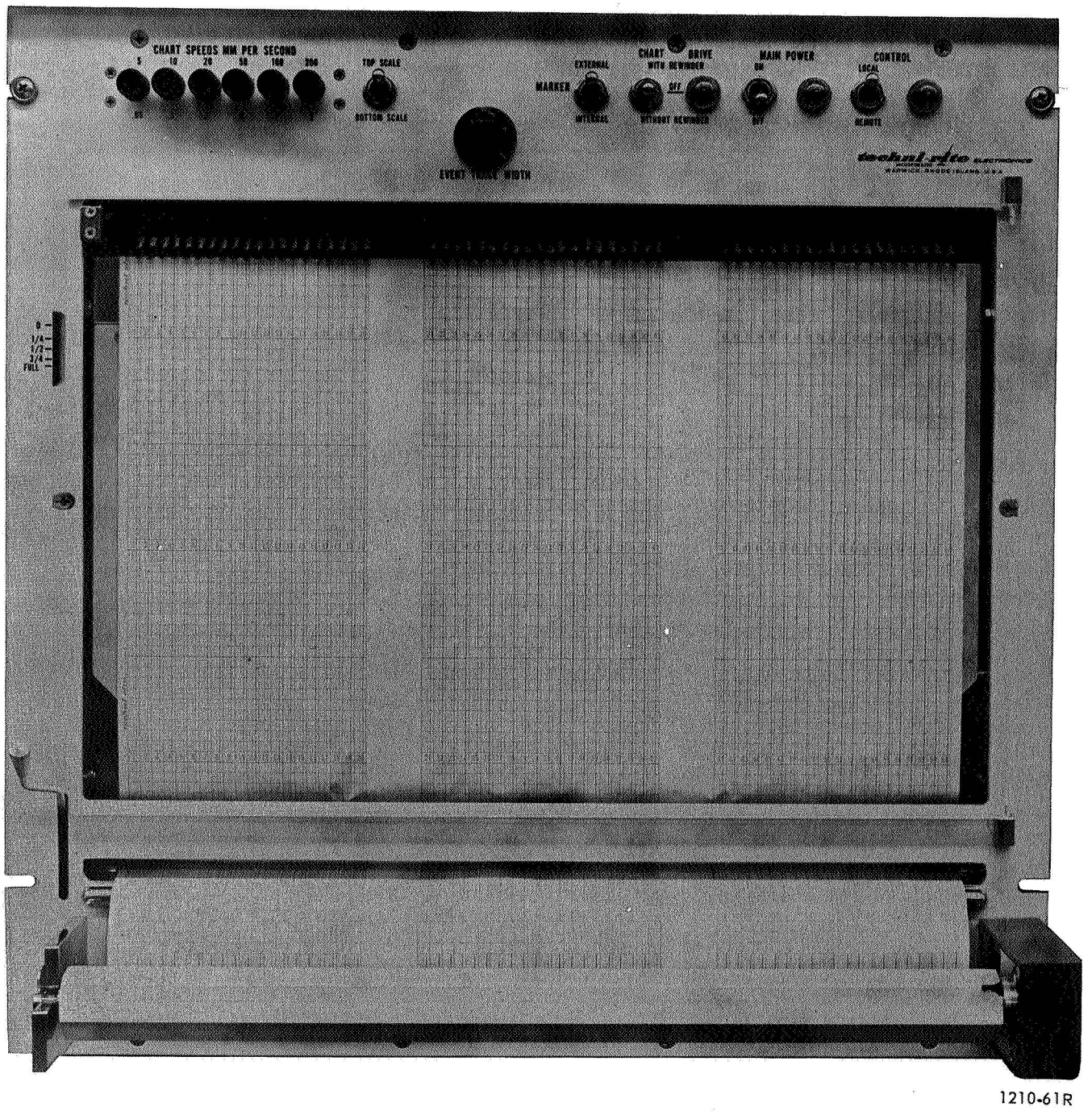
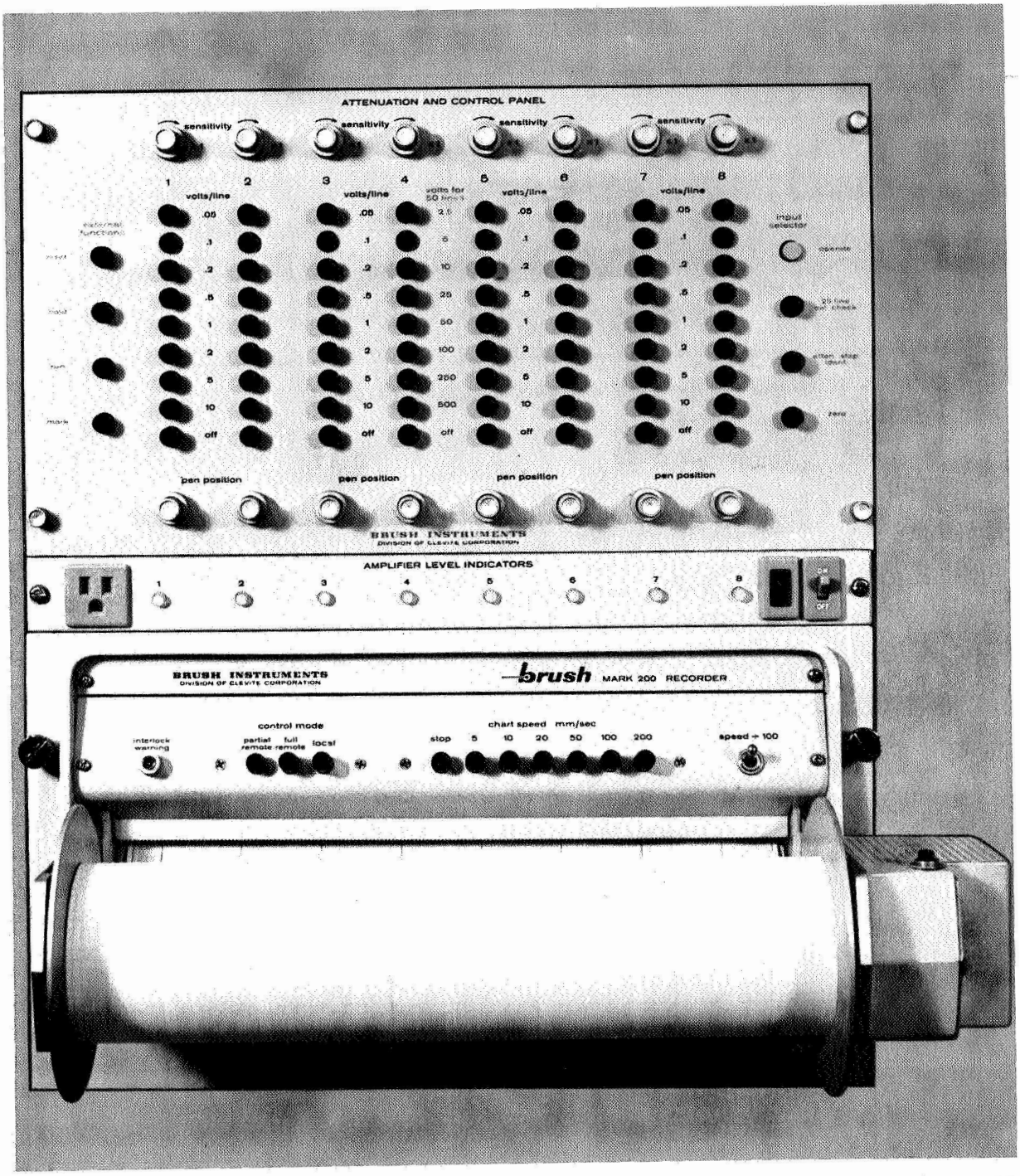
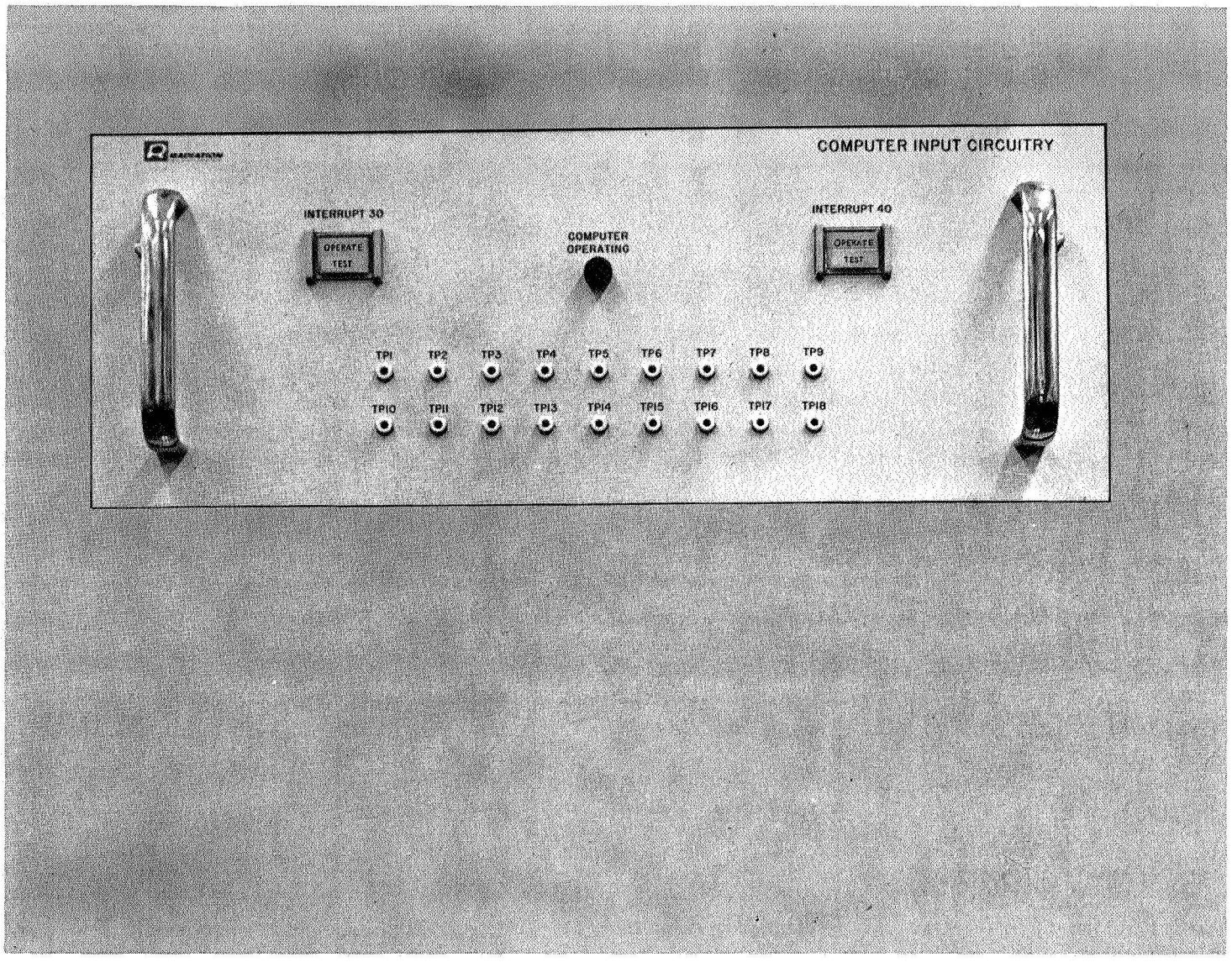


Figure 76. Event Recorder Front Panel



1416-230

Figure 77. Brush Recorder Front Panel



1416-236E

Figure 78. Computer Input Circuitry Front Panel

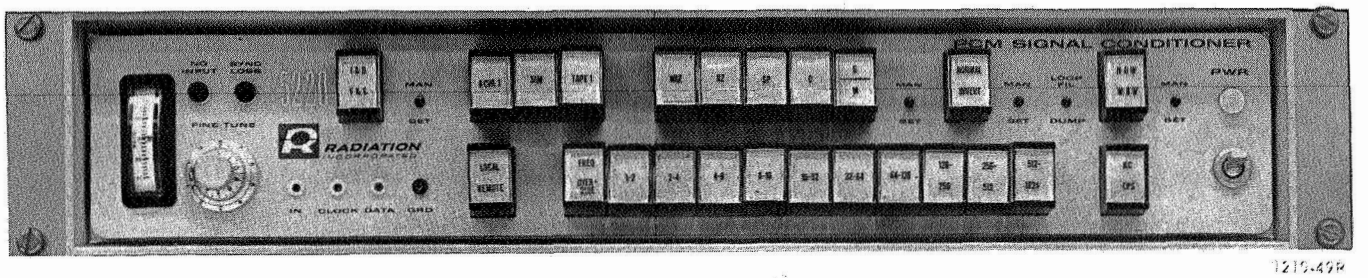
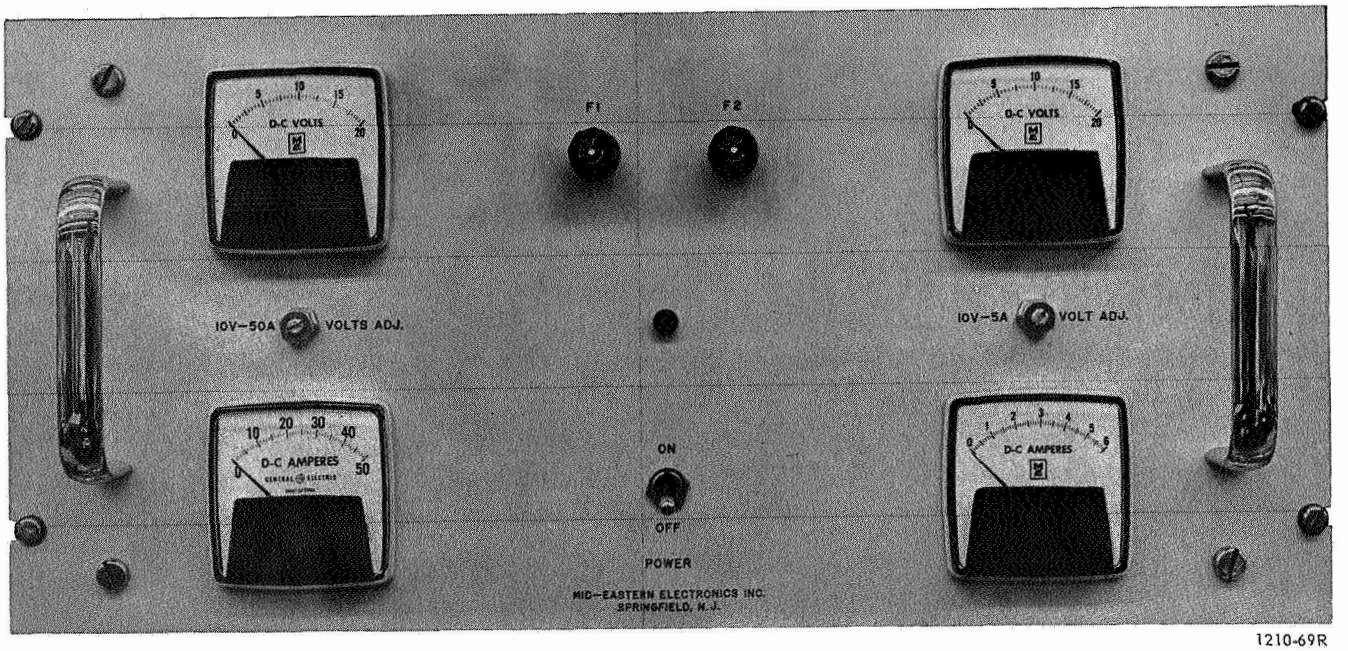
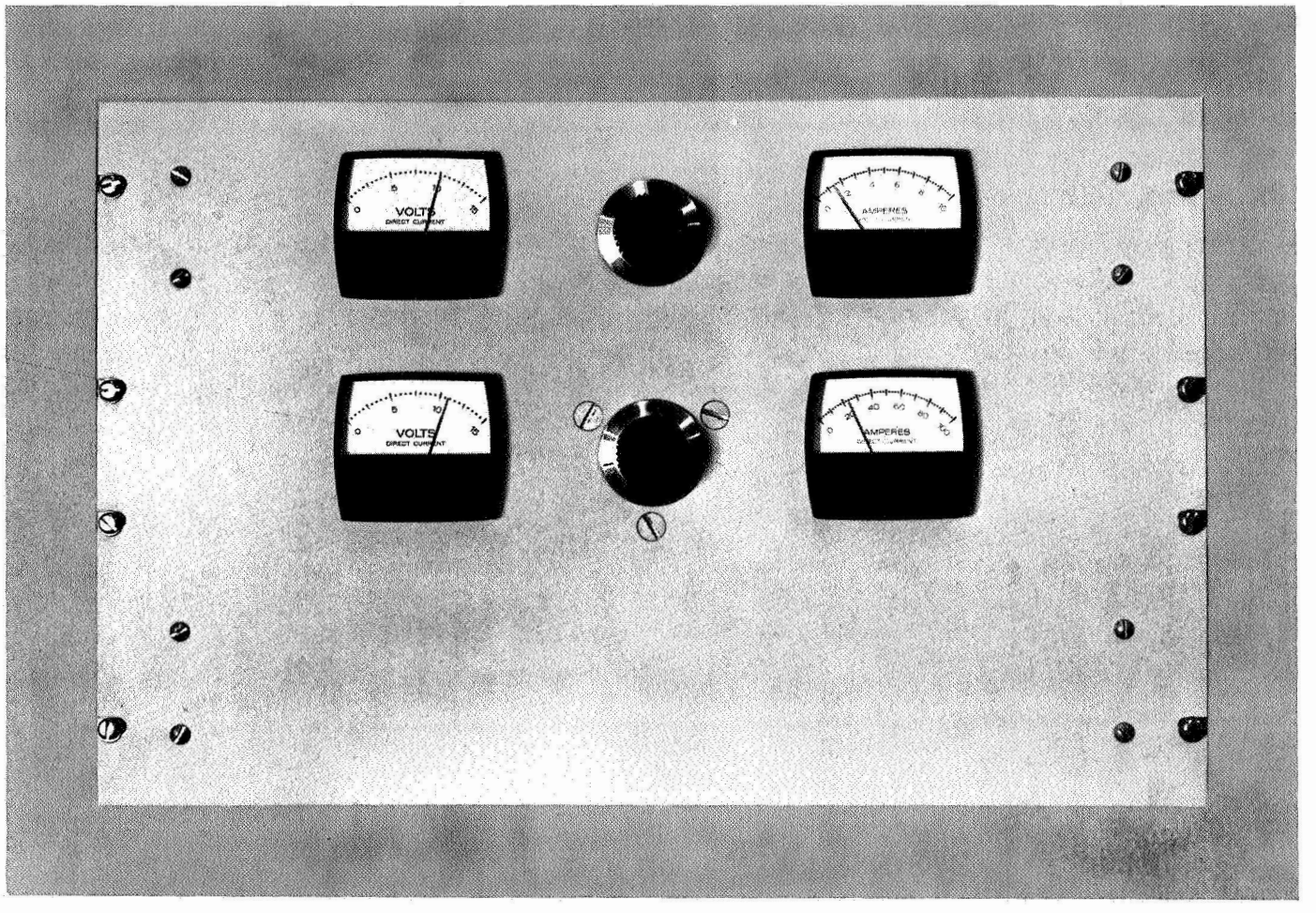


Figure 79. Bit Synchronizer (Signal Conditioner 5220A) Front Panel



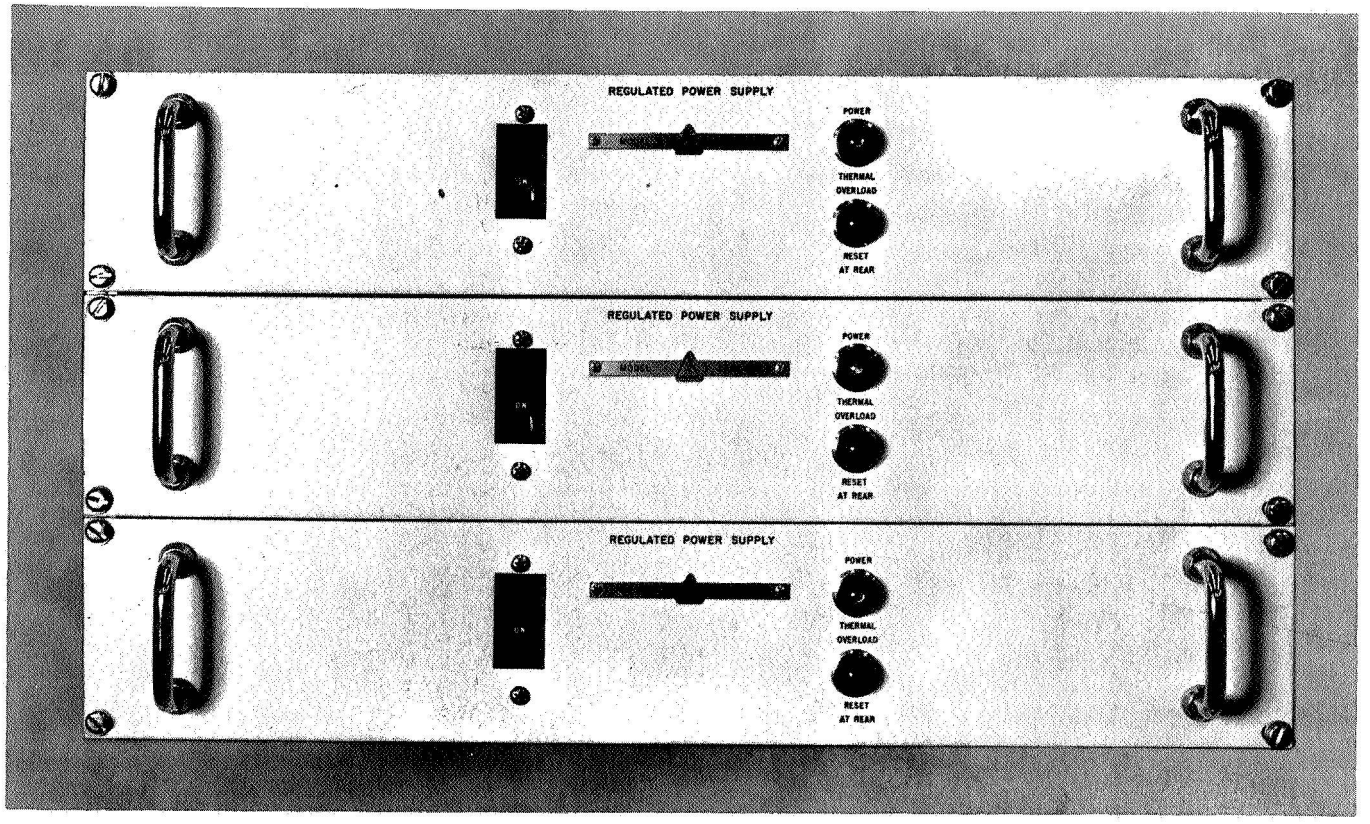
1210-69R

Figure 80. Power Supply (Mid-Eastern) Front Panel



1416-229

Figure 81. Solar Power Supply Front Panel



1416-228B

Figure 82. Lambda Power Supplies Front Panels

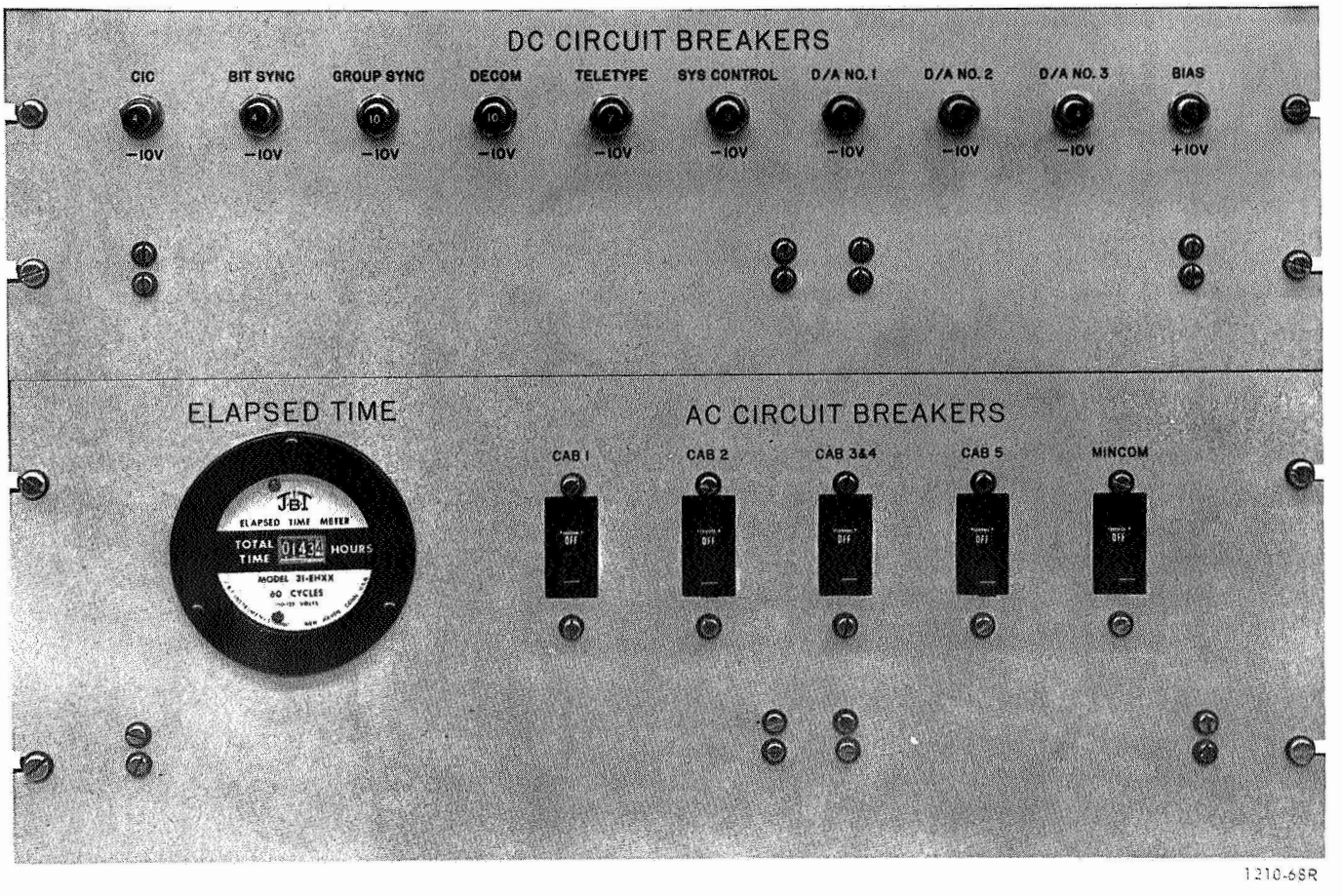
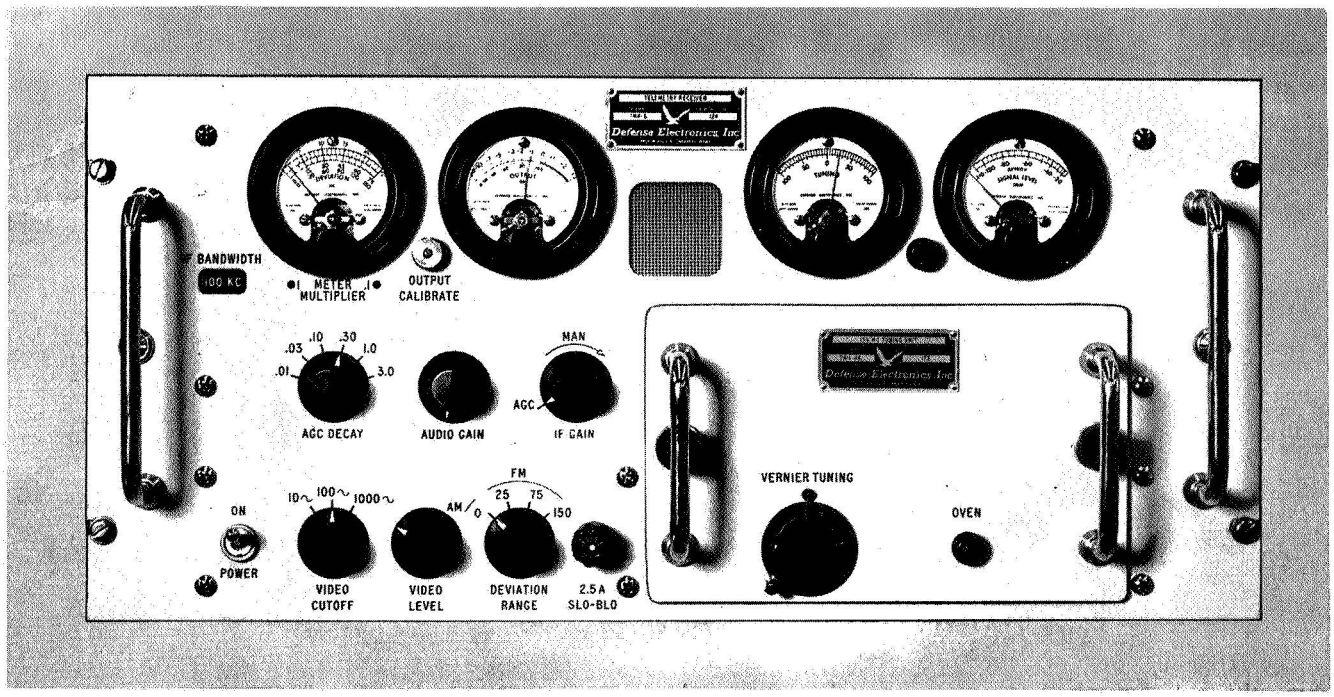


Figure 83. DC and AC Circuit Breaker Panels



1416-228A

Figure 84. Telemetry Receiver Front Panel

FOLDOUT FRAME 1

FOLDOUT FRAME 2

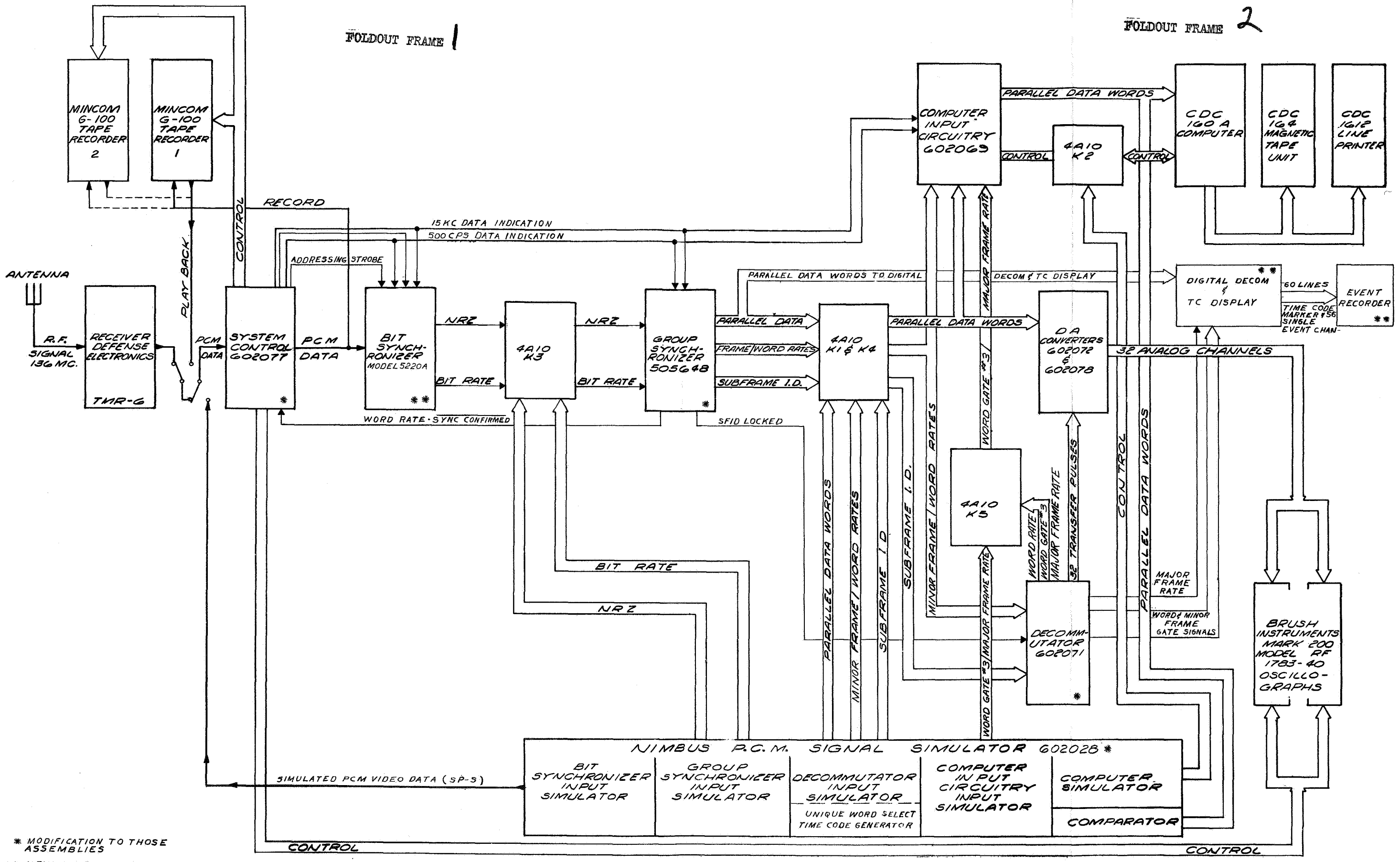


Figure 85. Nimbus B Ground Station Functional Block Diagram

The data format for both the 500 cps and 15 kc signals is constant and consists of sixteen 63-word frames. The first 16 bits of each frame contains frame sync data, the next 4 bits contain subframe identification (SFID) data, and the remaining bits contain information data including the time code. The first word of each frame contains 4 bits with each succeeding word containing 8 bits. Thus, word number 1 contains 4 bits of frame sync, word number 2 contains 8 bits of frame sync, word number 3 contains 4 bits of frame sync and 4 bits of SFID data, and each succeeding word 8 bits of data.

The maximum interrogation period for a single pass of the Nimbus B satellite is approximately 15 minutes. Stored data playback time (one orbit) is approximately 3.6 minutes. Two orbit recording is provided to collect data during those orbits when interrogation by the Ground Station is not possible.

The serial data input signal is processed in the system to obtain data synchronization and timing to drive system output devices. The computer will process data according to the computer program. Analog plotting of 32 channels is available with brush recorders. Analog channel selection is made by means of a decommutator assembly patch panel. Input video data may be recorded on magnetic tape for later processing. Two magnetic tape recorders are provided as part of the computer system, enabling partially processed data to be stored for later printout. Digital on-off data in any of fifty-six selected channels is available from an event recorder. Serial time code is decommutated from the format by the digital decommutator and time code display and displayed.

The data flow through the system (figure 85) is described in the following paragraphs.

5.2.2.1. SYSTEM CONTROL. The PCM Data from the receiver, the Minicom recorder, or from the simulator is routed to the system control. Real-time data from the satellite may be routed through the system control to the Minicom recorder for later playback. The PCM data to be processed is routed to the bit synchronizer.

The system control conditions the bit synchronizer and computer input circuitry to handle the incoming data through the use of the 15 kc and 500 cps frequency select squelch lines. Remote address strobing of the selected bit synchronizer data processing circuit is also provided by the system control utilizing word rate gated with the nonsync confidence signal from the group synchronizer. Manual strobing of the bit synchronizer may be accomplished at any time by depressing the SYSTEM RESET switch on the system control panel.

5.2.2.2. SIGNAL CONDITIONER 5220-A (BIT SYNCHRONIZER). The bit synchronizer is a universal type bit synchronizer designed to accept all forms of serial PCM data. In the Nimbus system, the bit synchronizer operating parameters are set up by remote programming to accept and process the Nimbus split phase/single (SP/S) data.

5.2.2.3. GROUP SYNCHRONIZER. The group synchronizer is programmed and recognizes the different synchronization codes and outputs synchronization pulses and synchronization status levels to the analog decommutator and system control and parallel data to the computer input circuitry for routing to the computer system, to the D/A converters, and to the digital decommutator and time code display.

5.2.2.4. ANALOG DECOMMUTATION AND RECORDING. The analog decommutator accepts synchronization pulses from the group synchronizer including the subframe identification (SFID) locked indication and outputs transfer pulses to the digital-to-analog converters for channel selection. The digital-to-analog converters supply analog voltages to the brush recorders which have the capability of making an analog recording of any thirty-two channels (either prime or subcommutated), of the real-time or playback A data. The decommutator also outputs word and minor frame gate signals to the digital decommutator and time code display.

5.2.2.5. DIGITAL DECOMMUTATION AND TIME CODE DISPLAY. The digital decommutator and time code display processes the digital data recorded in certain words of the Nimbus B format and drives the system digital recorders and NIXIE time display. The decommutator patch panel permits placing any digital word in the format on any desired group of digital event recorder channels. There are sixty signal lines to the recorder. Time code data and marker traces are fixed wired to traces 1 and 59 and 2 and 60. Patch selectable channels are routed to traces 3 through 58.

5.2.2.6. COMPUTER INPUT CIRCUITRY AND COMPUTER SYSTEM. The computer input circuitry accepts incoming data from the group synchronizer and prepares it for entry into a computer system. The function of the computer is to evaluate selected PCM telemetered data in accordance with the program selected and to provide a printout of all telemetered data.

5.2.2.7. GROUND STATION CHECKOUT. Ground Station checkout capability is provided by the signal simulator which supplies the signal inputs necessary to independently check out any of the subsystems.

In addition to the independent check-out of the subsystems through the use of the signal simulator, the analog recording subsystem can be independently checked out by test circuitry which is incorporated.

So that equipment necessary to troubleshoot the system will be available in the field, a dual-trace oscilloscope, RF signal generator and a frequency counter are also integrated into the cabinet containing the simulator.

5.3. NIMBUS B GROUND STATION MODIFICATIONS

5.3.1. GENERAL

Figure 85 is a functional block diagram of the Ground Station. The modified and new portions are flagged for identification. It can be seen that the functional signal flow has changed very little. The Teletype Translator and associated signal lines have been removed, a new bit synchronizer has been denoted and the Digital Decom and Time Code Display is shown driving an event recorder. The WR sync confirmed signals from the Ground Sync are shown routed to System Control resulting in address strobe output to Bit Synchronizer. The SFID Locked Status signal is shown routed from the Group Synchronizer to the Analog Decommutator for initial SFID addressing strobe to major frame counter.

The digital decommutator time code display block is shown with a parallel data input (originating from the group synchronizer) and word and minor frame gate signals from the analog decommutator. There are 60 signal lines to the event recorder. Time code data and the marker trace are fixed wired to traces 1,59 and 2,60, respectively. Patch selectable single event (digital) channels are routed to traces 3-58.

The addition of unique word select capability and time code data generation is shown in simulator block.

The following paragraphs describe the modifications to the PCM Ground Station equipment. Equipment not modified is not described in this report.

5.3.2. PHYSICAL DESCRIPTION OF MODIFICATIONS

5.3.2.1. GENERAL

The modifications to the Ground Stations Systems 1, 3, 4, and 5 are described in the following subparagraphs.

5.3.2.1.1. SYSTEMS 4 AND 5. Modifications to the PCM Ground Stations, Systems 4 and 5, include:

a. Addition of a Radiation 5220A Bit Synchronizer to provide improved signal-to-noise performance.

b. Modification of the Group Synchronizer to permit synchronization with a longer and more uniquely coded sync pattern and to permit operation at the revised words/frame format.

c. Modification of the Decommutator and incorporation of a new Digital Decommutator to provide on/off and time code decommutation capability.

d. Addition of a Time Code Display unit to provide visual readout of time code data.

e. Addition of an event recorder to record up to 60 channels of unitary on/off data or time code data.

f. Modification of the Simulator to provide simulation of Nimbus B format, including time code, digital channels, split-phase data, revised words/frame format, and revised synchronization code format.

These modifications were accomplished through addition of Cabinet 6 that contains the digital decommutator and the time code display; the addition of a single card file that contains the time code generator to the simulator cabinet (Cabinet 5); and rework of the group synchronizer, system control, decommutator, and simulator.

5.3.2.1.2 SYSTEMS 1 AND 3. The modifications to the PCM Ground Stations 1 and 3 (updated to 8 and 7 respectively) consisted of adding a complete new Cabinet 3/4 group modified to the above Nimbus B configuration plus the new Cabinet 6 as described above. Cabinet 3/4 includes three power supplies, three D/A converters, a system control drawer, a group synchronizer drawer, an analog decommutator drawer, a computer input circuitry assembly and a new bit synchronizer. The modification also included the relocation of the simulator and simulator control units into the new Cabinet 6.

5.3.2.2. MECHANICAL CHARACTERISTICS. Changes in the mechanical layout of the PCM Ground Stations were not extensive. The major change was the addition of a new single-unit cabinet to house the digital decommutator, and time code display units. The cabinet is equipped with a blower and convenience outlets. Ac and dc power were brought in from Cabinet 3/4 to a connector panel mounted in the top rear of the new cabinet. The event recorder was mounted in its own separate cabinet.

The addition of the new cabinet required adding a connector panel in the top rear of Cabinet 3 and three external cables to interconnect the two panels. Ac power, dc power and signal leads were routed through these cables.

A single card file of twenty-five cards was mounted directly below the simulator and behind the simulator control panel in Cabinet 6 to house the time code generator circuitry. Inputs, outputs, and power leads interface directly with the simulator.

The relocation of the simulator and simulator control required various brackets and mechanical modification of Cabinet 6.

The mechanical configuration of the new cabinets 3/4 in System 8 and 7 was basically the same as in the present System 4 and 5.

5.3.2.3. ELECTRICAL CHARACTERISTICS. Changes in the electrical characteristics of the PCM Ground Station equipment are discussed briefly in the following paragraphs. Details of the circuit modifications are discussed in paragraph 5.3.3.

The original bit synchronizer was replaced by a Radiation Model 5220A Bit Synchronizer because the original unit was not capable of accepting split-phase/single (SP/S) input signals. The combination of SP/S signals and the new units provides better signal-to-noise ratio. The 5220A unit is completely programmable and is controlled by the squelch circuits.

Squelch circuits in the system control unit were changed to accommodate the SP/S signals. In addition, programming signals were added to remotely control the bit synchronizer when switching from real-time to playback signals.

The group synchronizer was modified to permit operation with a 62-1/2-word format instead of the 64-word format. Parallel data outputs were added to the output shift register and routed to Cabinet 6.

The decommutator was changed by adding parallel outputs for various word and frame pulses needed in the time code display unit. In this way, no extra loads were added to patch panel outputs.

Since the new Nimbus B format has digital time code inserted in given words in the first minor frame, a time code display unit was added to the system. This unit decommutates and displays the digital time code on NIXIE tubes. The time code display unit also generates and distributes a serial time code to certain event recorder channels and to the analog recorder event markers. A relay, mounted in the analog recorder and controlled by the time code display unit, activates the analog recorder event markers.

The new Nimbus B format also has digital data recorded in certain words. A digital decommutator, a digital patch panel and a 60-channel event recorder were added to handle this data. The patch panel permits placing any decimal word in the format on any desired group of event recorder channels.

The most extensive modification was made to the simulator. The simulator was changed to generate 62-1/2-word formats instead of 64-word formats, and the video output was changed from nonreturn-to-zero (NRZ) to split-phase/single (SP/S). A selectable sync word capability was added to replace the previous fixed sync word. In addition, a single word select feature was incorporated as a troubleshooting aid. This permits the operator to insert any bit combination into any single word slot in the format. A time code generator was added to simulate the time code words in the new Nimbus B format. Since there was not enough space in the simulator to house the additional circuitry, a card file was mounted at the rear of the cabinet to house the time code generator. This unit inserts a digital time code into the format at the proper time and updates the time code at a simulated time rate.

5.3.3. DETAILED THEORY OF OPERATION

The following paragraphs contain the detailed theory of operation and latest logic diagrams of the Ground Station circuits modified. Only the analysis of the positions of the circuits modification is included herein. The theory of operation of the complete system is described in detail in the Nimbus B PCM Ground Station Instruction Manual.

5.3.3.1. BIT SYNCHRONIZER. The original bit synchronizer from all the Ground Stations was removed and replaced by a Radiation 5220A bit synchronizer that was modified to handle split-phase mark zero input data. Addition of this unit provides a better signal-to-noise ratio than the original unit. The 5220A bit synchronizer is completely programmable as to data type and bit rate. Complete information on the 5220A bit synchronizer is contained in the 5220A instruction manuals supplied with the equipment.

Remote programming was performed by routing separate 15 kc and 500 cps squelch status (negative true) lines to the remote inputs. Selected parameters that remained the same for both types of data were wired to a -10 vdc line. Inputs to nonselected parameters were left open. Thus, when a data type is received causing a squelch circuit to indicate its status, a negative level is applied with a fixed negative line to all remote inputs required to program the bit synchronizer.

When the data type changes, inactive squelch lines go to ground (no select level) and the active squelch goes to a negative level effecting a select signal level. The address strobes occur until Sync Confidence status is obtained, guaranteeing read-in of remote addressing.

The video signal is inputted to the bit synchronizer through J4 and is controlled manually by a front panel pushbutton labeled RECEIVER INPUT. Output NRZ data is taken from J1 on the rear of the bit synchronizer for routing to the group synchronizer assembly. Phase 1 (P1) of the bit synchronizer clock was routed out (E8A7) to the group synchronizer where the negative transition is used to transfer data into the input shift register.

5.3.3.2. GROUP SYNCHRONIZER. A block diagram description of the operation of the group synchronizer is given in subparagraphs a through i below. The overall block diagram of group synchronizer is shown in figure 86. The group synchronizer timing diagram is shown in figure 87. A discussion of the modifications to the group synchronizer for Systems 4, 5, 7, and 8 is given in paragraphs 5.3.3.2.1 through 5.3.3.2.5 by a functional circuit basis. Included as aid are the latest logic diagrams of the functional circuits including the changes and additions.

a. The reconstructed NRZ data and its complement are shifted serially into the input storage register using the delayed bit rate F_o. The capacity of the input storage register is twenty bits, and in this description, register 1 is designated as the last stage (or the position) containing the first bit shifted in the register at the time the register is initially filled. Various blocks are tied to the outputs of the input storage register such that, with appropriate timing, all outputs and further handling of data is done in parallel bit form.

b. The frame sync correlator block receives its inputs through separate sets of twenty FRAME CODE SELECT switches; one set for A data and one set for B data. Since B data is no longer used the second correlator and associated switches are used as spares. These switches are DPDT with center-off, and route either the negative-true side of the shift register for a code bit ONE or the complement side for a ZERO bit and is positioned to center-off for bits not used. Thus, for the present Nimbus B Data Format, a Barker type code word of 16 bits is stored in the A data switches identical to airborne generated frame sync code. The input shift register is 20 bits long and is thus capable of storage for broadside comparison. Thus, when the selected frame sync code pattern is in the input shift register, all inputs to the correlator will be at a negative level. Any bit error will be routed through at zero level.

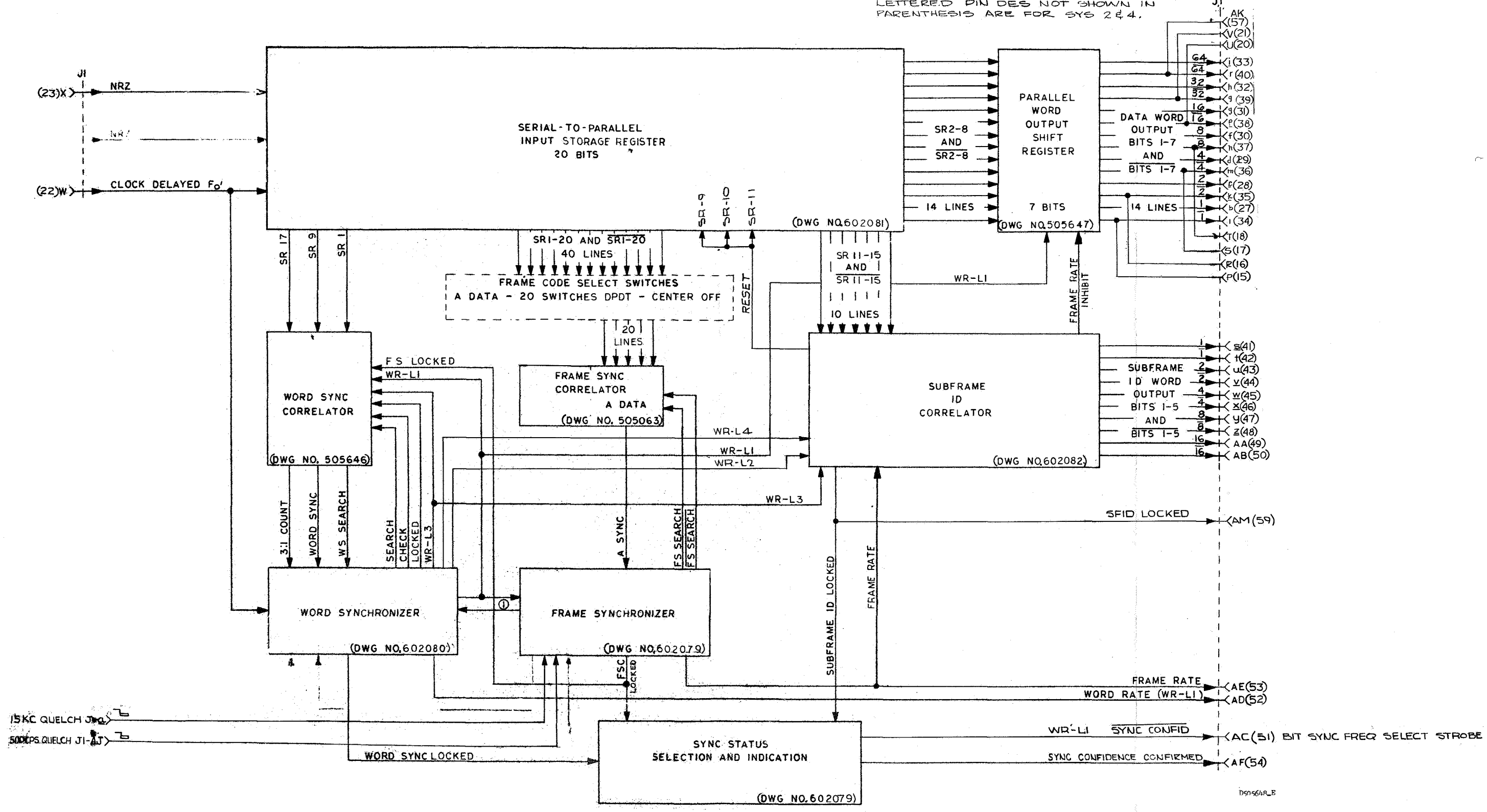
c. These inputs are summed in the correlator, and a voltage comparator circuit determines the detection of the frame sync code pattern and generates a frame sync pulse. Allowance for bit errors (parameter r) is set in the voltage comparator of the frame sync correlator circuit.

d. The frame sync pulse is routed to the frame synchronizer block. Essentially, the frame synchronizer logic generates a frame rate pulse which is synchronized with the detected frame sync pattern during the Search mode and then the occurrence of the pattern is

FOLDOUT FRAME 1

FOLDOUT FRAME 2

NOTES:
1. NUMBERED PIN DESIGNATIONS SHOWN IN PARENTHESIS (XX) ARE FOR SYS 7 & 8 LETTERED PIN DES NOT SHOWN IN PARENTHESIS ARE FOR SYS 2 & 4.



① F S RESET
② WR GATE 'B' INHIBIT

Figure 86. Group Synchronizer Block Diagram

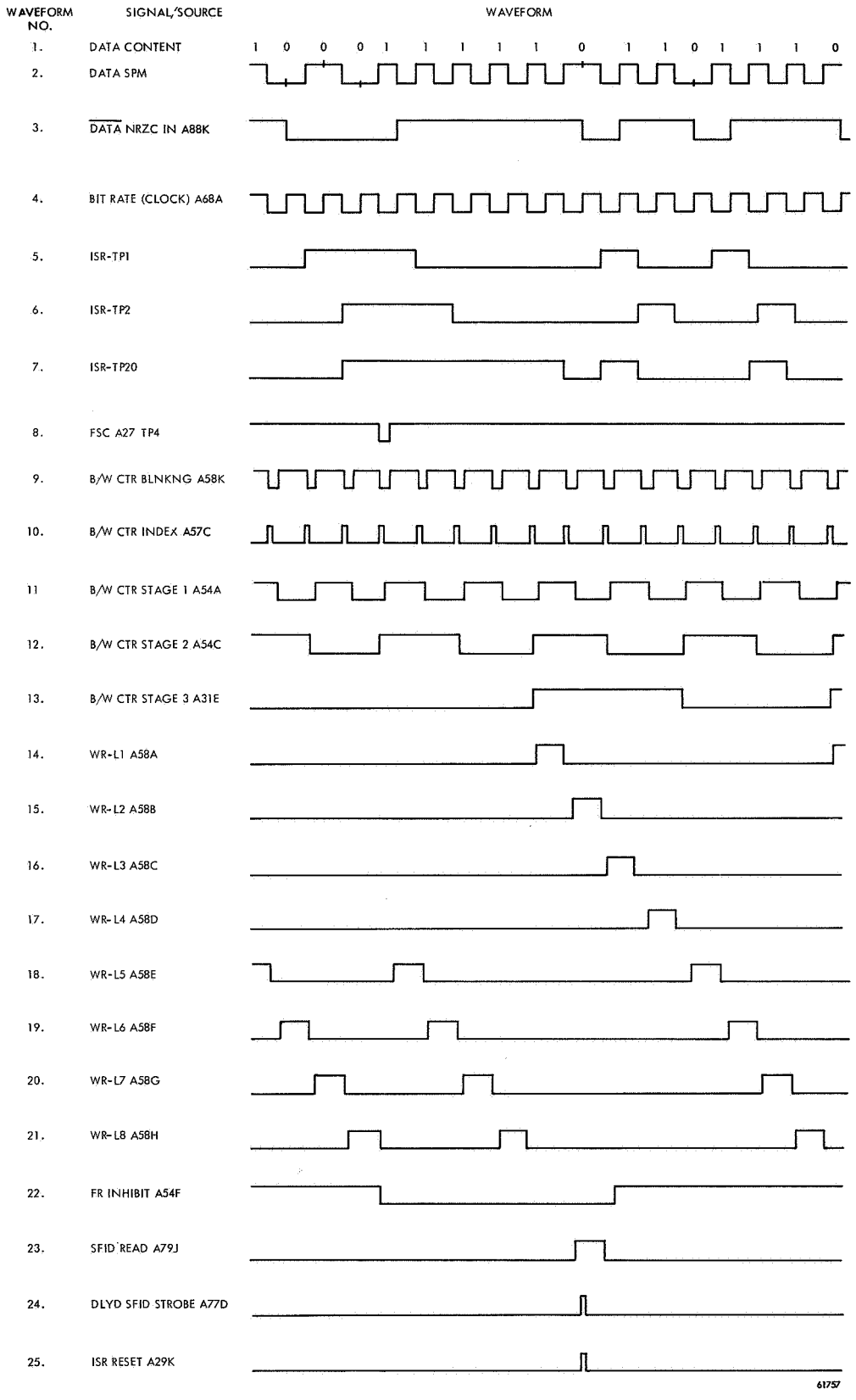


Figure 87. Group Synchronizer Timing Diagram

compared with the fly-wheeling frame rate during Check and Locked modes. The frame synchronization status is indicated on the front panel with a red light for SEARCH, yellow for CHECK and green for LOCKED. When frame synchronization goes from Search to Check, the correlator switches operate to allow one bit error in the frame sync pattern during the Check mode. If two consecutive coincidences of frame sync and frame rate occur, the frame synchronization mode will switch to Locked. At any time a frame rate pulse occurs without a frame sync detection, an error-pulse is generated and used as a reset to return operational mode to Search, whereupon, the frame sync pattern is looked for, allowing no-bit error (r=0) and when detected, once again synchronizes the fly-wheeling frame rate, goes to Check mode and seeks further frame sync and frame rate coincidences.

e. The word sync correlator block has the same function as the frame sync correlator, but since the word sync code in the Nimbus format is only one bit (ZERO code) per word, simple gating logic is employed to detect this pattern. No bit errors are allowed during word sync Search mode, but upon detecting the word sync pattern the operation is switched to a Check mode and one (r=1) error is permitted. Since the word sync code is fixed, the inputs to the word sync correlator from the input storage register are fixed, looking at stages 1, 9 and 17. Thus, three words are looked at to detect three word-sync zero bits at the proper word interval. To avoid the word sync discontinuity caused by the frame sync code and subframe identification address each minor frame, a 3:1 word counter gates the output of the word sync correlator so that groups of three words are searched every third word interval. The true occurrence of the word sync pattern generates a word sync pulse.

f. The output of the word sync correlator is routed to the word synchronizer whose function is the same as the frame synchronizer. A fly-wheeling word rate pulse is synchronized with the detected word sync pattern and then the coincidence of the word sync and word rate are checked. Occurrence of a word rate without word sync constitutes an error. This check is made every third word rate, the same as the word sync Check mode. The word rate error analysis is set: r=1, u=5, and K=15. Thus, during the Check mode, if five or less errors occur during a 15-word group (three words per group) Check, the operation is switched to the Locked mode and the same error check is continued. If more than five errors occur during Check or in Locked mode, this is detected and used to reset the operational mode to Search. Then the next word sync pattern detected resets (synchronizes) the fly-wheeling word rate, switches operation to the Check mode and word synchronization error analysis is started.

g. The subframe identification (SFID) correlator block contains logic to pick out the subframe address (binary 1 through 16) occurring immediately following the frame sync code. This occurs and is processed for both 500 cps and 15 kc data. At the time the frame sync code is detected, the SFID data is in the input storage register stages 17 through 25. For 5 bit SFID the bit in shift register stage 16 would be used. The next word rate will be one half word (4 bits) after frame rate; and to avoid a timing problem WR-L2 (delayed one bit) is used to shift the SFID address into the SFID correlator. The SFID data is now in input shift register stages 11 through 15 and these are wired to SFID accumulator, where a read-in and/or a comparison is made with an expected SFID address. A continual error analysis is made in SFID Check and Locked modes, requiring a minimum of three successive correct addresses to define the Locked mode. An error subtracts one count from successive checks, requiring a minimum of three successive errors to switch from Locked down through Check and into Search. In the

Search mode the address is read in from the input storage registers, and during Check and Locked it fly-wheels by adding one count to the read-in stored address just before the next comparison check. The output of the SFID correlator routes a 5-bit (bit 1 always zero) binary word to the decommutator assembly where it is matrixed to unitary 1 through 16 (frame gate signals) for decommutating data.

h. The block labeled sync status selection and indication is logic contained in other blocks. It is separated as a functional block to describe the attainment of over-all data synchronization status. The data synchronization status is defined as fly-wheeling when its front panel indicator red lamp is on and LOCKED when the green lamp is on. The over-all sync status is an AND condition of frame synchronization always, and word synchronization if the WORD SYNC switch is IN, and SFID synchronization if SFID SYNC switch is IN. Normally both switches are IN; however, some test conditions may contain fixed data words creating additional word sync patterns causing an unreasonable high probability of errors, and system confidence may be improved by inhibiting word sync status. Word sync quality can still be monitored by its status indicator lamps. A switch is provided to use or inhibit SFID sync status so that during high-noise or low-signal conditions, where many errors are expected, the operator can inhibit the influence of SFID sync status and maintain system data synchronization with normal error-analyzed frame and word synchronization.

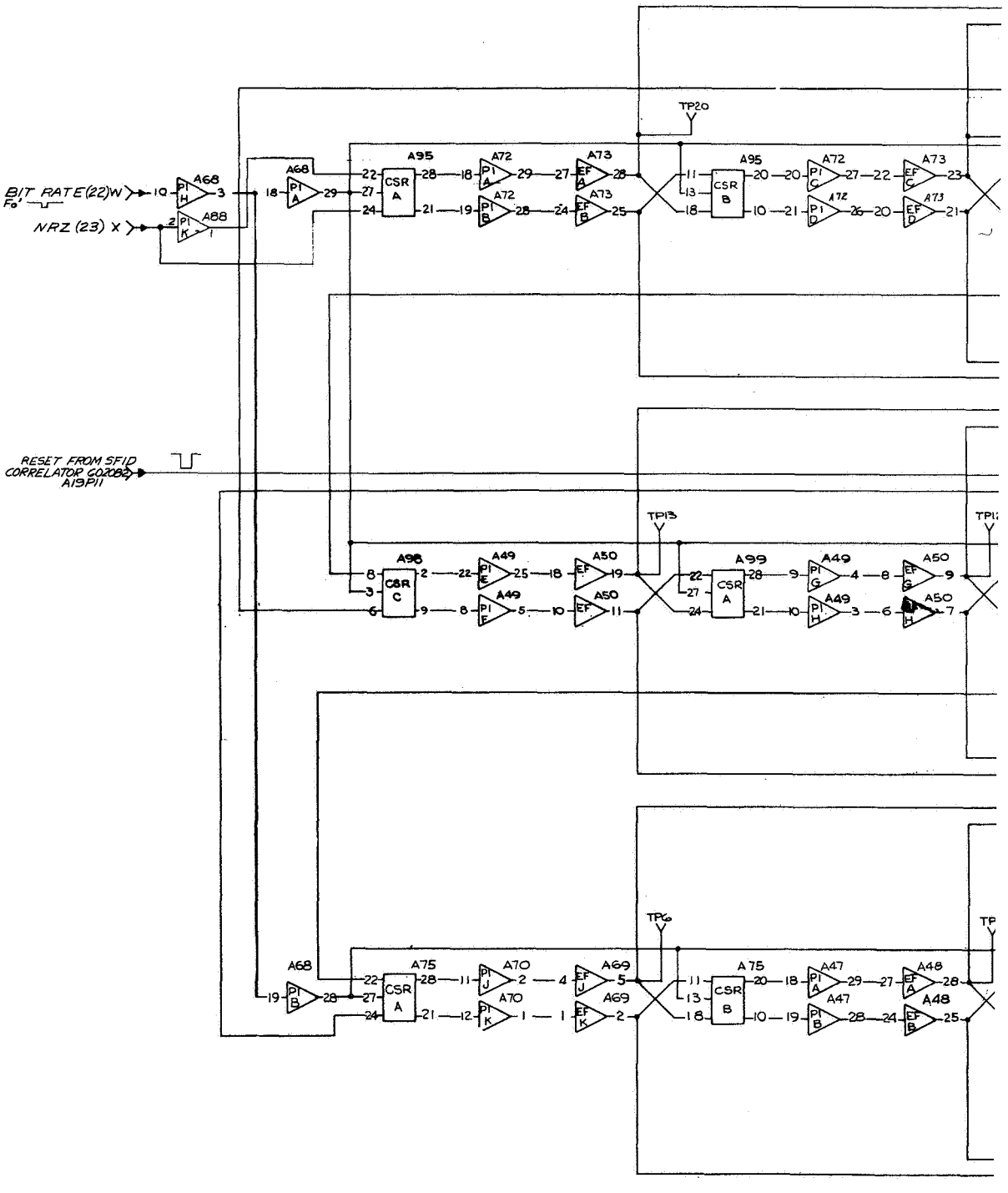
i. The output shift register block provides 7-bit parallel output storage for the data words. Input storage register stages 2 through 8 are shifted broadside to the output shift register by word rate timing. There are fourteen output lines routing; the true and complement 7-bit data words to the computer input circuitry, the digital-to-analog converters, and to the binary-to-teletype converter (no longer used). At frame rate time, the output shift register is reset to all zeros for a 6-bit interval (covers word 1 time) so that the computer input circuitry can OR in the major frame count.

5.3.3.2.1. INPUT SHIFT REGISTER LOGIC (FIGURE 88). A dc reset signal was added to input shift register stages 11 (CSR A99B), 10 (CSR A99C) and 9 (CSR A100A) to clear the portion (3 most significant bits) of the subframe identification (SFID) word actually used as part of the frame sync code word. The reset signal is derived in the SFID Correlator logic using a delayed SFID read pulse gated with frame sync locked status. Thus, after a sync locked status, the reset signal clears the unwanted frame sync code bits leaving only the 4 least significant (1-16 count) bits to be transferred to the output (broadside data word) shift register as the SFID word.

A power inverter stage, A68K, was added as an input buffer and inverter for the bit rate (clock) signal from the new Bit Synchronizer assembly.

5.3.3.2.2. FRAME SYNCHRONIZER LOGIC (FIGURE 89). The Frame Synchronizer logic was modified to make the words per frame counter a 63:1 count instead of the 64:1 count for the old format. Differentiator stage A33F was added to reset the first stage of this counter, thereby adding one count such that 63 word pulses now cause the 64 count. Also, the recognition of the frame sync code word during search status is OR'ed with the zero count of the words per frame counter and routed out as frame rate. This frame rate is then used as the zero reset line to both the words per frame and bits per word counters.

FOLDOUT FRAME 1



FOLDOUT FRAME 2

FOLDOUT FRAME 3

NOTES:
1. LETTERED OUTPUTS USED ON SYS 4-5; NUMBERED ON 1-3.

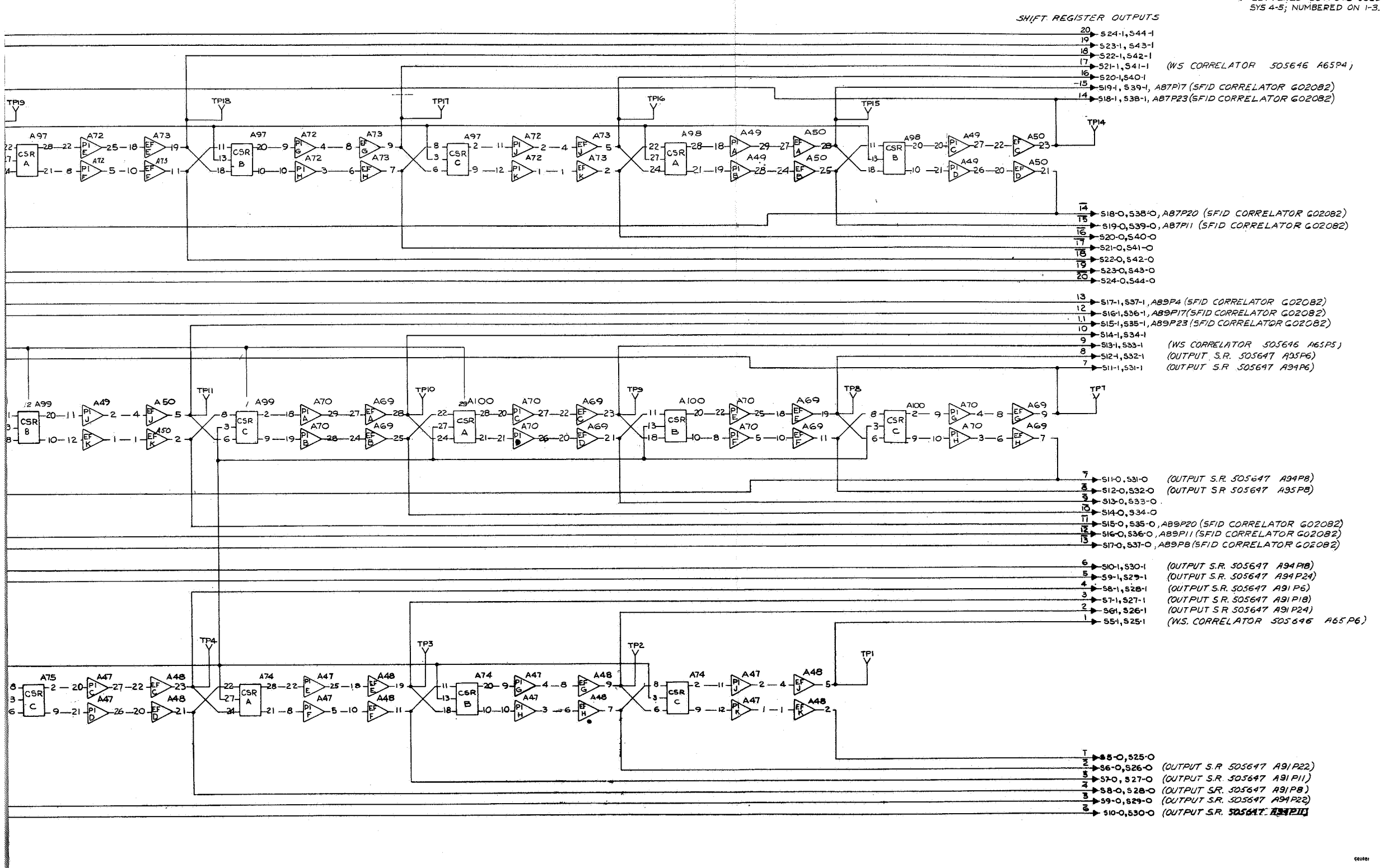
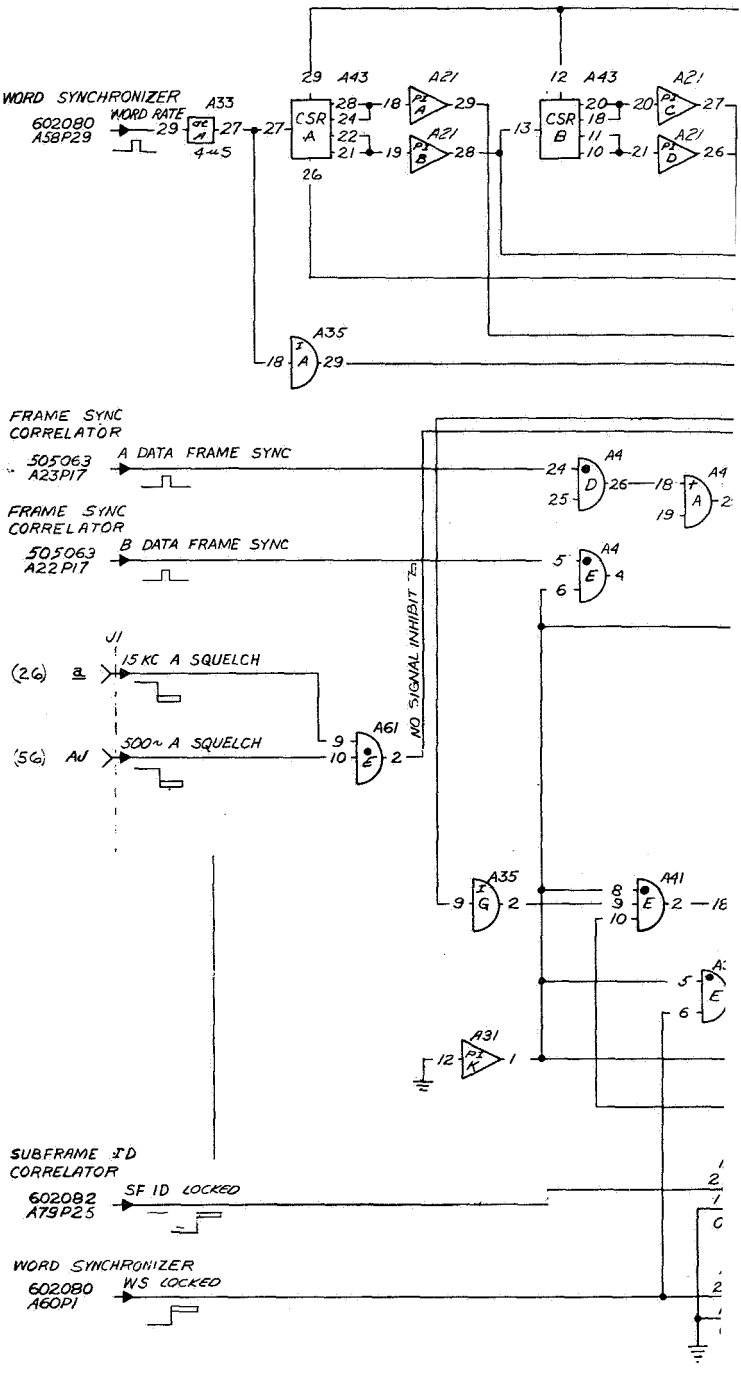


Figure 88. Input Shift Register Logic Diagram

FOLDOUT FRAME 1



FOLDOUT FRAME 2

FOLDOUT FRAME

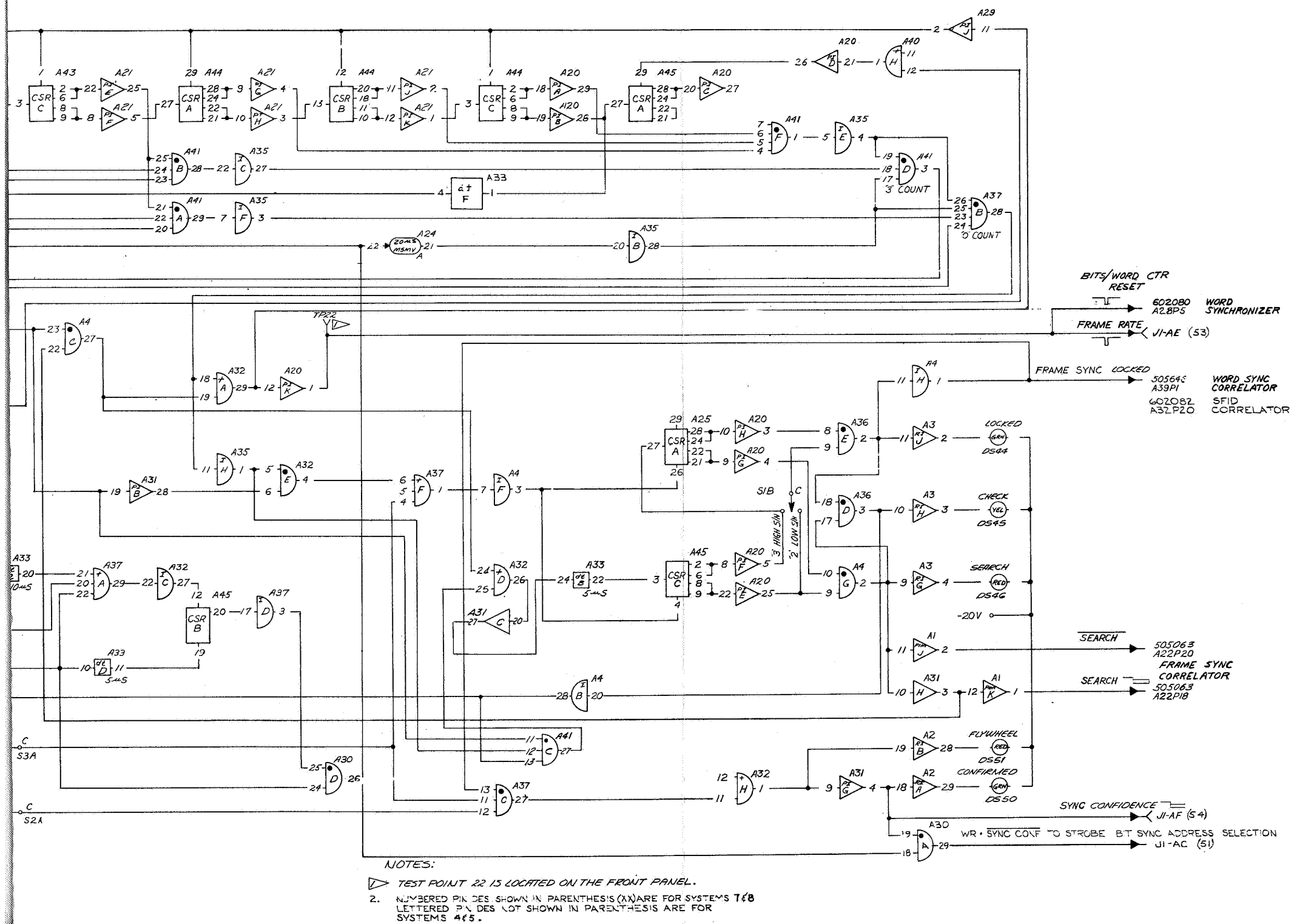


Figure 89. Frame Synchronizer Logic Diagram

The bit synchronizer addressing strobe originates in the Frame Synchronizer logic using the sync confidence status AND'ed (A30A) with a word rate pulse from the words per frame counter logic. Thus, in a Not-Sync Confirmed (flywheeling) status, pulses are outputted to the system control assembly to a power inverter to strobe the bit synchronizer. In a Sync Confirmed status, the strobes are inhibited. If the sync condition ever drops for any reason, the bit synchronizer is once again strobed until a sync condition is regained.

Other logic changes in the frame synchronizer logic involved removing portions of the B data circuitry where malfunctions of this circuitry could impair new A data operation.

5.3.3.2.3. WORD SYNCHRONIZER LOGIC (FIGURE 90). The word synchronizer logic was modified to handle the 1/2 word portion of the 62-1/2 words per frame format. The bits per word counter (CSR's A52A, B and C) are reset to a 5-count (1 through 8 count cycle) by the frame rate so that the first word of each minor frame is only 4 bits; then each succeeding word is the full 8 bits.

Other changes in this drawer involved removal of some of the B data logic.

5.3.3.2.4. SUBFRAME ID (SFID) CORRELATOR (FIGURE 91). The SFID correlator logic was modified to use a SFID read strobe delayed from frame rate time to be compatible with the timing change required to accommodate the initial 1/2 word. Word rate line 2 (WR-L2) was used in place of WR-L1. Thus, when frame rate occurs at WR-L1 time, the word rate count is immediately set to WR-L5. Use of WR-L1 would have been marginal without special shaping and delay. The first 1/2 word is then routed normally and as WR-L2 time pulse first occurs during next word interval. This is gated through as SFID read strobe. However, the SFID data has moved one bit interval later through the input shift register and it was thus necessary to change SFID data lines from the input shift register stages 12-16 to stages 11-15.

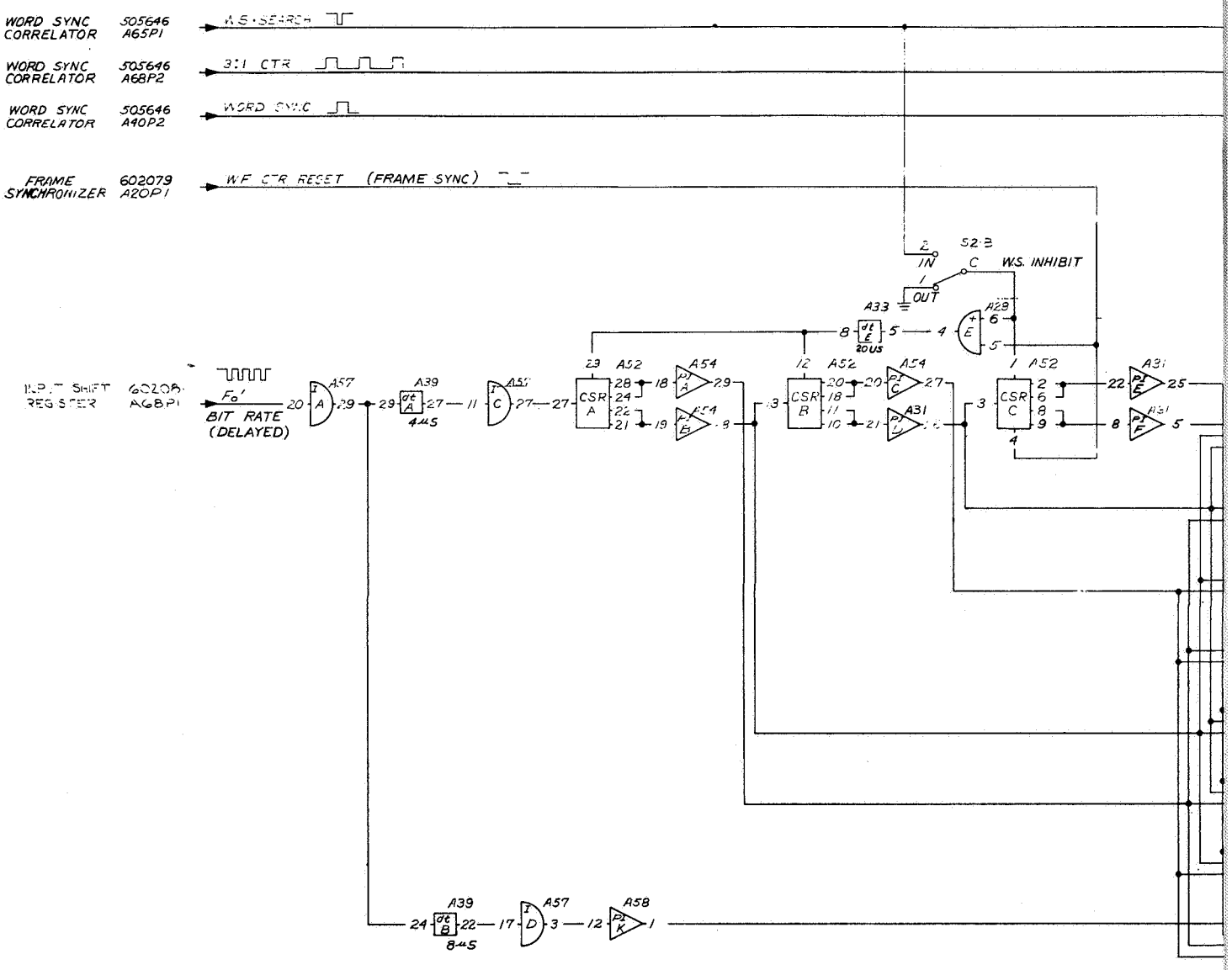
As the SFID data is shifted on down the input shift register for transfer to form the 7-bit broadside word to the output shift register, the 3 most significant bits are those of the end of the frame sync code word. A delayed SFID read signal was added from the SFID correlator to reset the input shift register stages containing these bits (stages 9, 10 and 11). Since the outputted data word is flagged as good by sync confidence Confirmed, this status signal was used to gate the resetting signal enabling it only after sync confidence is Confirmed, thereby avoiding any possibility of disturbing the frame sync correlation pattern during the no-error Search interval.

A power inverter stage A54D was added to provide increased drive on the frame rate inhibit signal to the output shift register logic.

5.3.3.2.5. OUTPUT SHIFT REGISTER (FIGURE 92).

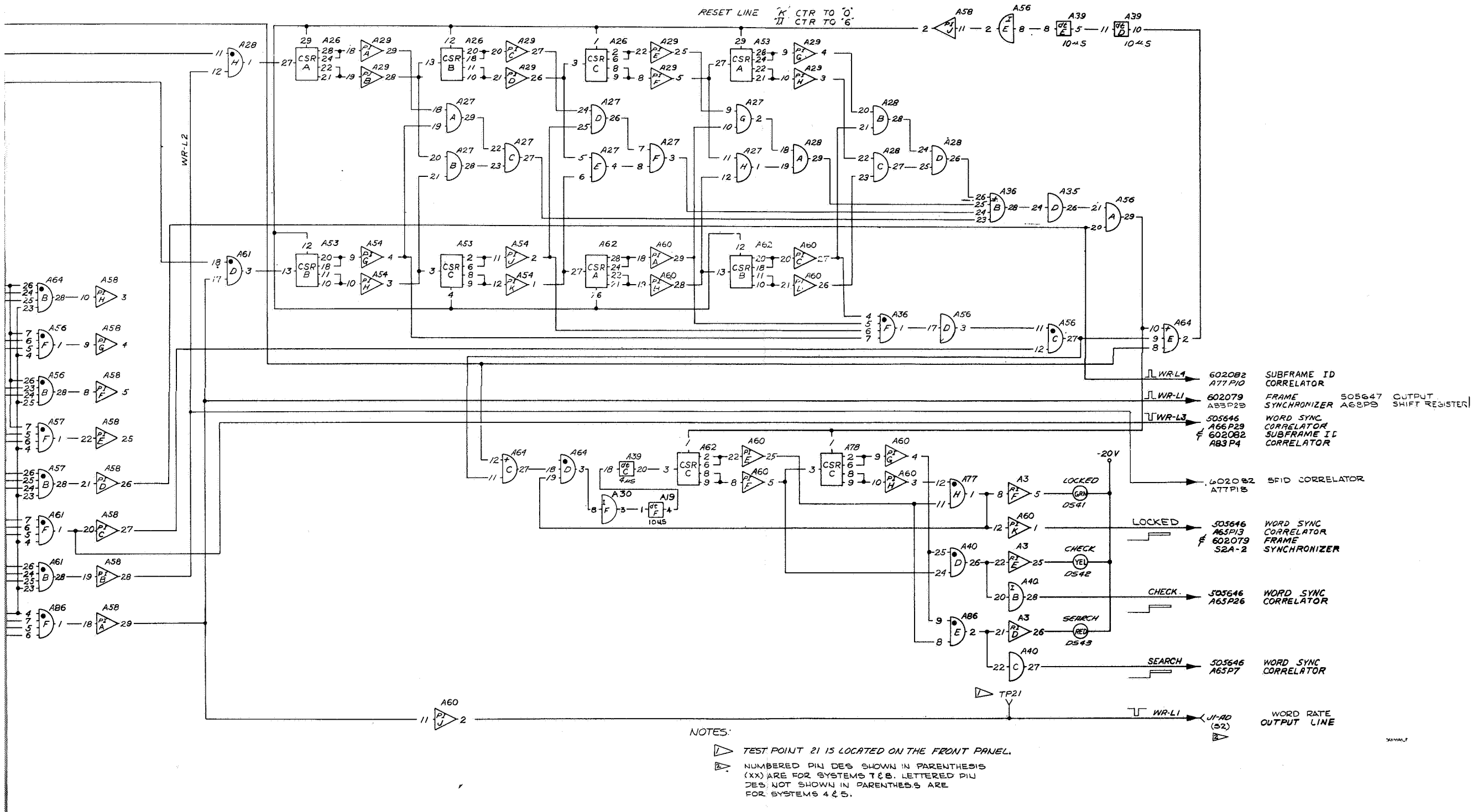
The output shift register was modified to provide the additional drive capability required for outputs to the digital decommutator and the time code display. The additional drive is furnished by power inverters A88A through A88G that are connected in parallel with power inverters A93A, A93C, A93E, A93G, A93J, A68C and A68E.

FOLDOUT FRAME 1



FOLDOUT FRAME 2

FOLDOUT FRAME 3



NOTES:

1. TEST POINT 21 IS LOCATED ON THE FRONT PANEL.
2. NUMBERED PIN DES SHOWN IN PARENTHESIS (XX) ARE FOR SYSTEMS 7 & 8. LETTERED PIN DES NOT SHOWN IN PARENTHESIS ARE FOR SYSTEMS 4 & 5.

Figure 90. Word Synchronizer Logic Diagram

FOLDOUT FRAME 1

FOLDOUT FRAME 2

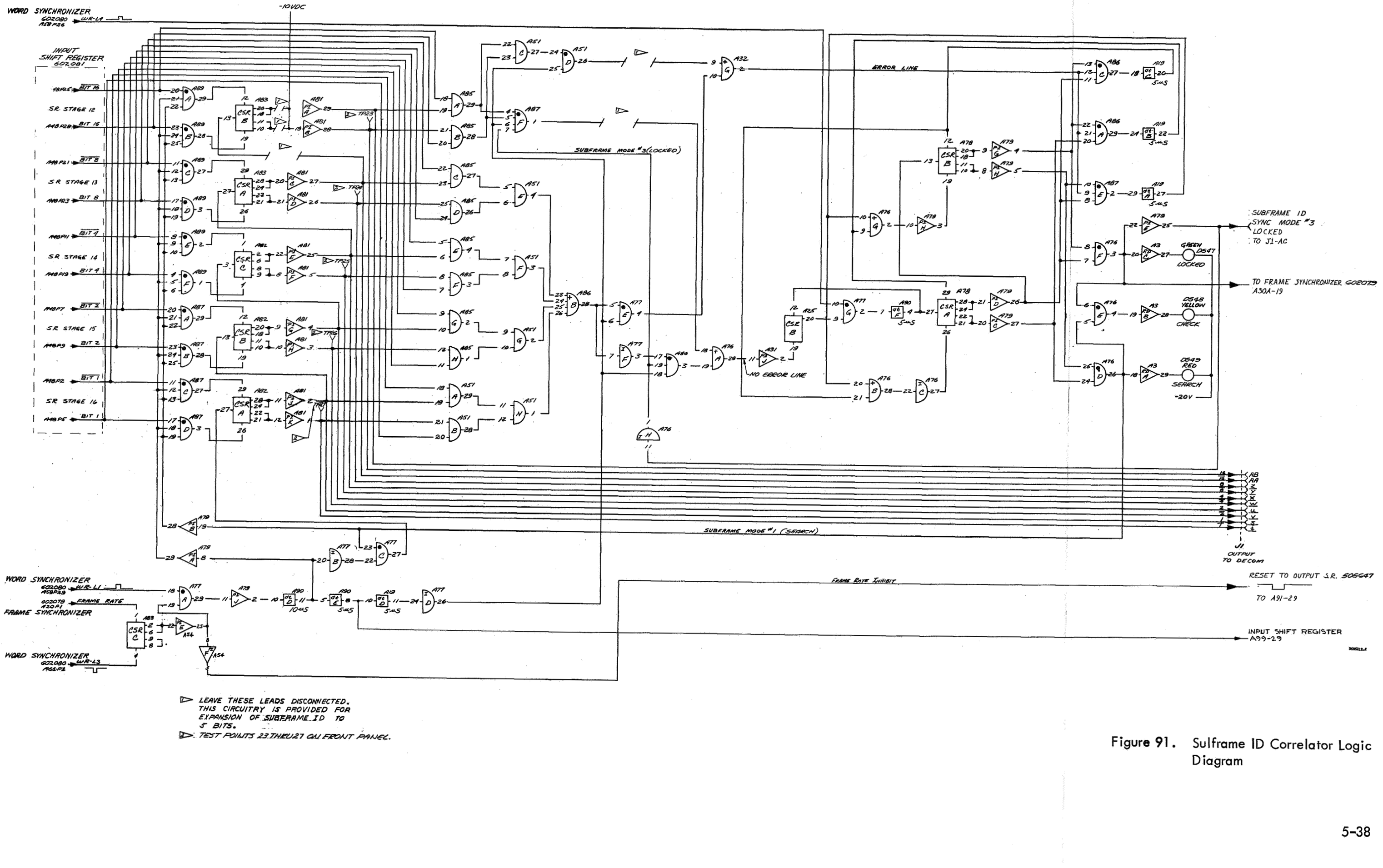
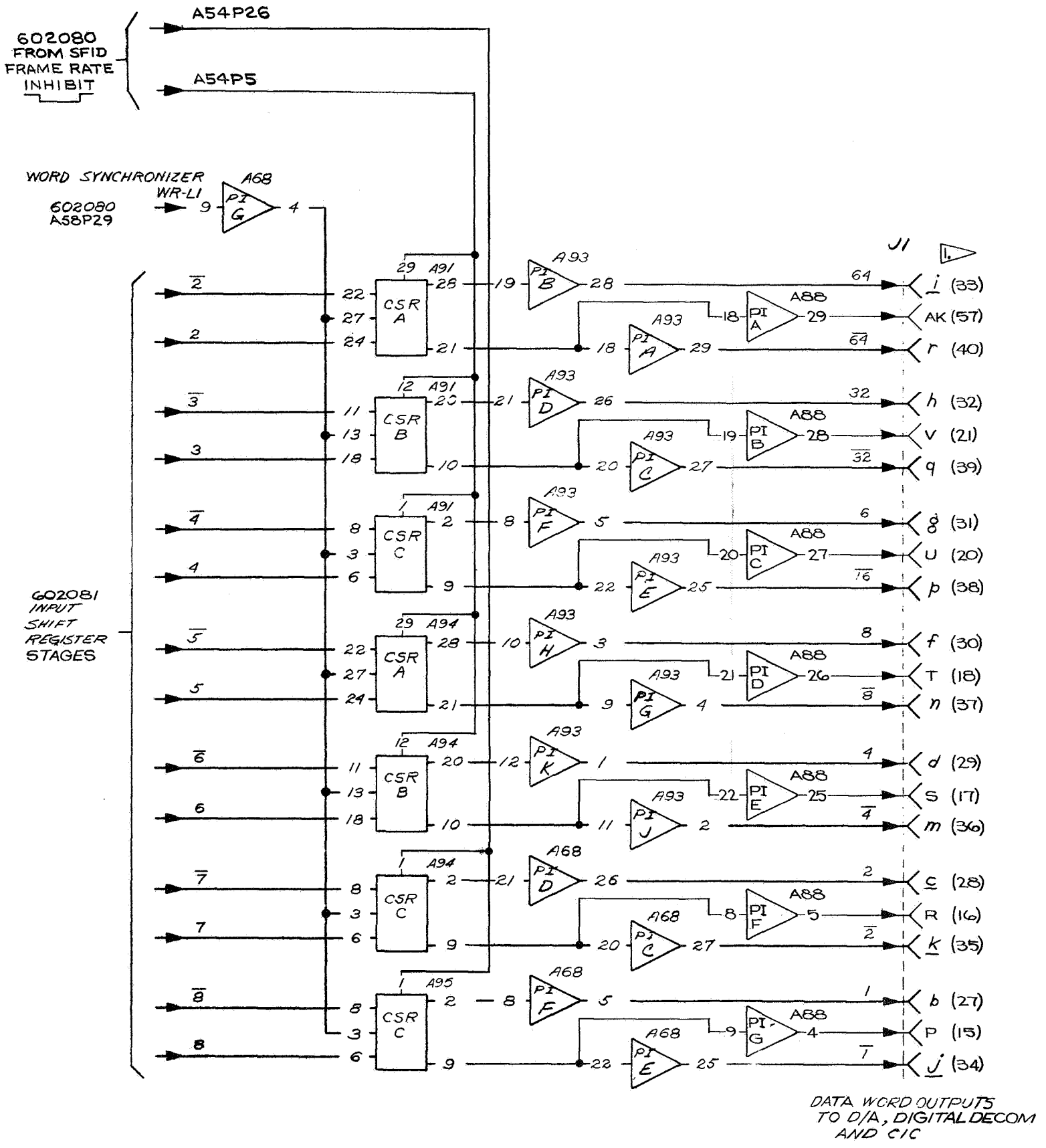


Figure 91. Sulframe ID Correlator Logic Diagram

FOLDOUT FRAME 1



FOLDOUT FRAME 2

NOTES:

1. NUMBERED PIN DES SHOWN IN PARENTHESIS (XX) ARE FOR SYSTEMS 7 AND 8. LETTERED PIN DES NOT SHOWN IN PARENTHESIS ARE FOR SYSTEMS 4 AND 5.

D505647-D

Figure 92. Output Shift Register Logic Diagram

The reset line to the word storage CSR stages was divided for load distribution of the additional drive capability.

5.3.3.3. SYSTEM CONTROL (FIGURE 93). Modifications to the system control assembly include the addition of two squelch circuits for complete code pattern recognition of split-phase data, a new video amplifier with AGC and the capability of remote control of the bit synchronizer programming. Switching was added to provide continuous or inhibited squelch signals time code. Also an indication was provided for time code received status. The B data squelch circuit and associated logic was removed.

5.3.3.3.1. REAL-TIME SQUELCH CIRCUIT. With a split-phase data input, squelch circuits are required for the half-frequency, as well as the basic frequency, because a series of ZERO's in a split-phase input appears as a signal that is one-half the frequency of a series of ONE's. Since B-type data is no longer required, the B-data squelch card was removed and a 250-cps squelch card was installed in location A98. The 250-cps and 500-cps squelch cards are adjusted for overlapping operation, i.e., a squelch output is developed by A97 or A98 for any code pattern in the input signal ranging from all ONE's to all ZERO's. The outputs from A97 and A98 are inverted by A93B and A93F, respectively, and are OR'ed by A77E. The resultant output from the OR gate is inverted by power inverter A93G to provide a real-time squelch signal to system control logic.

5.3.3.3.2. TIME CODE SQUELCH. Time Code Squelch recognition logic was modified with the addition of a switch section to the old B data panel indicator assembly to enable it to perform a momentary contact simulated time code squelch signal. Further, the existing indicator was rewired to indicate the status of the time code storage register (CSR A79A). The simulated 10 kc switch S18A and DS21A were removed from the SATELLITE-IN-VIEW indicator. Switch S4 on A85 was wired to provide a continuous time code stored (Received) signal when in the ON position. The time code inhibit function remains the same as before on Switch S5 of A85.

5.3.3.3.3. PLAYBACK (15 KC) SQUELCH LOGIC. This circuitry was modified same as the 500 cps squelch logic adding another squelch circuit for 7.5 kc frequency in card slot A27. Spare logic from B data removal, A28A and B and A77D were used for inverters and OR'ing of 15 kc and 7.5 kc squelches.

5.3.3.3.4. B DATA LOGIC. Most of the B data logic and the B data squelch were removed and used where added circuitry was required. The B data indicator was used for time code (see 5.3.3.3.2). The B data start logic (MSMV A27, gating A28A, B, C, and D) and outputs (A77C and E, and A93B) were removed.

5.3.3.3.5. BIT SYNCHRONIZER PROGRAMMING. Extra drivers (A28E, C, and D) were added to the 15 kc and 500 cps squelch indication outputs and routed to the remote select inputs to the bit synchronizer. Word rate gated (enabled) with the Sync Confidence status from the group synchronizer assembly is routed through an added driver A28F as the remote addressing strobe to the bit synchronizer. One section of the system RESET switch S3B was wired to generate an address strobe on this line when a system Reset is generated. TP5 was changed from monitoring B data to provide test point on this strobe line.

FOLDOUT FRAME 1

FOLDOUT FRAME 2

K1 - TIME DELAY RELAY
S2 - RECEIVER/TAPE INPUT
S3 - RESET
S4 - START/STOP TAPE
K5 - START/STOP OSCILLOGRAPHS
S6 - START/STOP OSCILLOGRAPHS
S7 - TEST/OPERATE TELETYPE

S8 - 2 SEC DIR CONVERTERS
S9 - FULL SCALE DIR CONVERTERS
S10 - NORMAL/INVERT RECEIVER
S11 - NORMAL/INVERT TAPE
K12 - RECEIVER/TAPE INPUT
K13 - MINCOM CONTROL
K14 - MODE INDICATOR
S15 - ON/OFF POWER
K16 - NORMAL/SIMULATE RELAY
S17 - RECORD INHIBIT
S18 - MANUAL TIME CODE SQUELCH

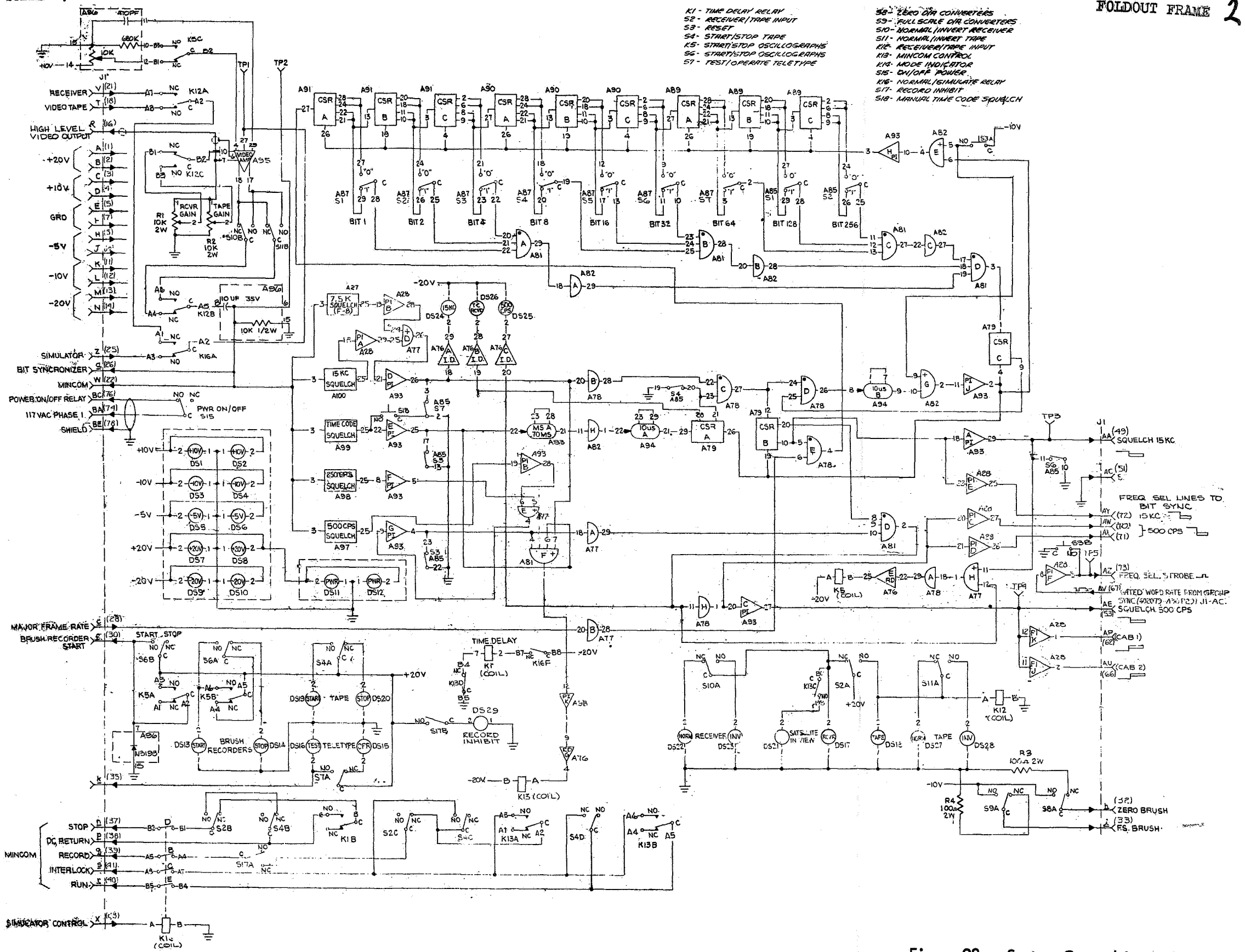


Figure 93. System Control Logic Diagram

5.3.3.3.6. VIDEO AMPLIFIER (FIGURE 94). A new video amplifier circuit was developed to replace the existing video amplifier. The new circuit features automatic gain control (AGC), a high level (30 vptp) external output capable of driving a 600-ohm load, normal and inverted system ac coupled outputs and the existing panel gain controls on the receiver and tape inputs. An extra card was added in slot A96 to provide an initial gain adjustment and AGC time constant so that, with no signal, the AGC is disabled, improving noise immunity. When a signal is received causing squelch indication, spare contacts on relay K5 switch the video amplifier to AGC, thereby offering a constant level output over a wide range of input signal levels. A high frequency noise input by-pass capacitor was added to card A96 and connected to the video amplifier. The components for ac coupling the video amplifier output were also placed on card A96. A diode to ground was placed on the Brush Recorder Start line to suppress relay coil switching spikes. This diode was also placed on card A96.

5.3.3.4. ANALOG DECOMMUTATOR (FIGURES 95 AND 96). Addition of the time code display and digital decommutator in Cabinet 6 required routing all of the word gate pulses (1 - 64) and the first 16 minor frame gates out of the Analog Decommutator to Cabinet 6. Parallel routing was used to prevent excessive loading on the present patch panel outputs.

This was done by the addition of 8 complementary emitter follower cards. In Systems 8, 4 and 7 (figure 95), the circuits used were A27A through A27K, A30A through A30K, A46A through A46K, A55A through A55K, A61A through A61K, A71A through A71K, A80A through A80K and A96A through A96K. These circuits correspond to word gates 1-64 and minor frame gates 1-16, respectively. The outputs of these circuits were brought out to the rear drawer connector J2, pins 1-5, 7, 8, 10-18, 20-60, 62-67, 70-80, 82 and connector J1, pins 42-46. Again, these correspond to word gates 1-64 and minor frames gates 1-16.

In System 5 (figure 96), the circuits used are A38A through A38K, A42A through A42K, A46A through A46K, A55A through A55K, A63A through A63K, A71A through A71K, A80A through A80K, and A96A through A96K. The correspondence with the word gates, frame gates and output pin numbers is the same as in Systems 4, 8, and 7. It should be noted that the complementary emitter followers provide the capability of driving the long length of cable plus the circuit load on the terminating end.

The wire between A64-11 and A99-20 was removed to prevent the state of the last unused SFID CSR from affecting the output major frame strobe. It was also noted that power inverter A81H was marginal in operation because of the driving of A77A through A77H, A74F and A74G. Another power inverter A47J was added in parallel with A81H to drive half of the load. The circuitry was rewired so that A81H now drives A77G, A77D, A77H, A74F and A74G. In turn, A47J now drives A77A, A77C, A77E and A77F.

Another gate, A64E was added to gate word rate, minor frame rate, and minor frame 1 together to generate a noise free major frame rate pulse during (at the end of) minor frame 1. The output of A64E is inverted by A64F and routed to the output connector J1-P(38). This provides a major frame rate pulse for routing to the time code display drawer in cabinet 6.

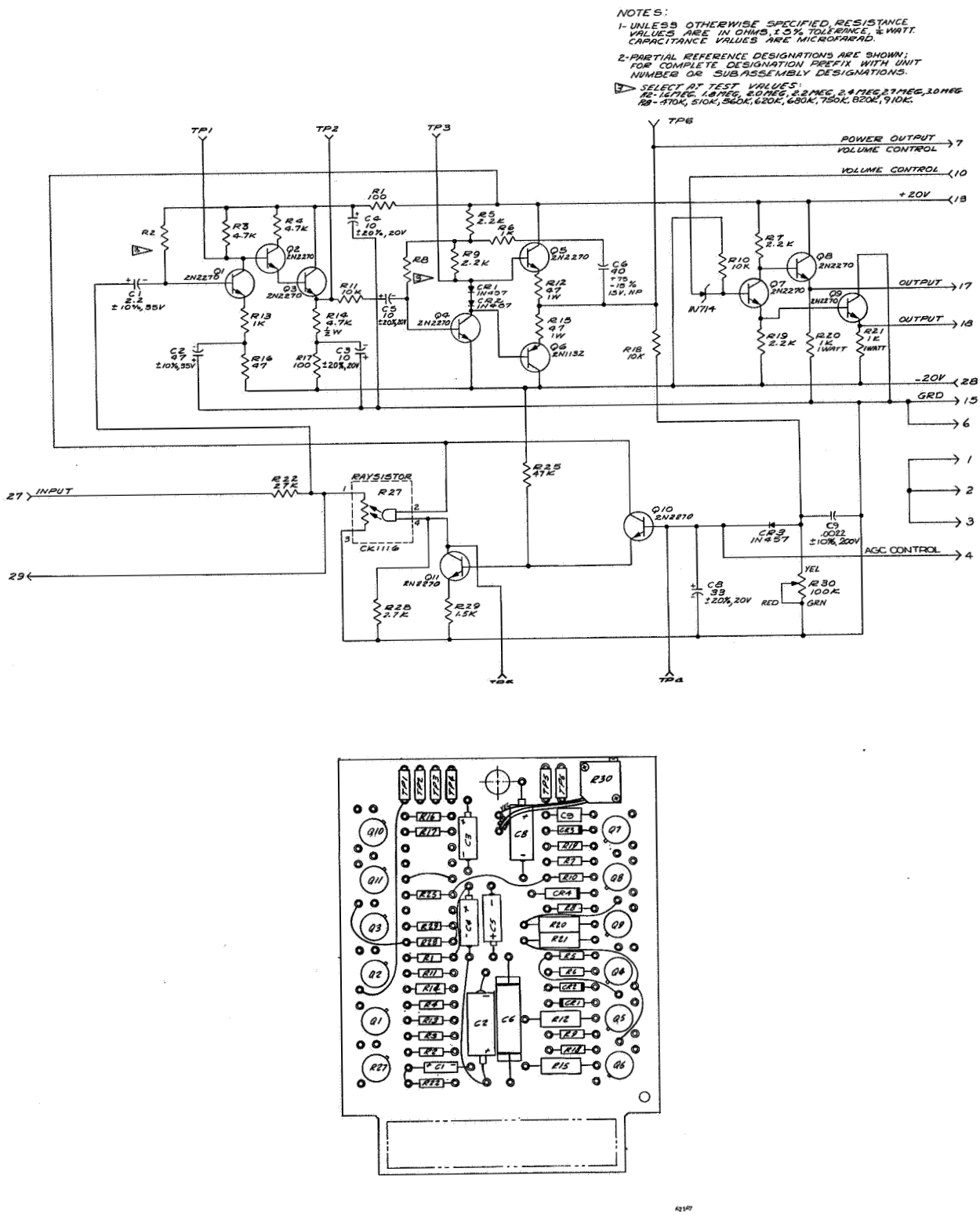
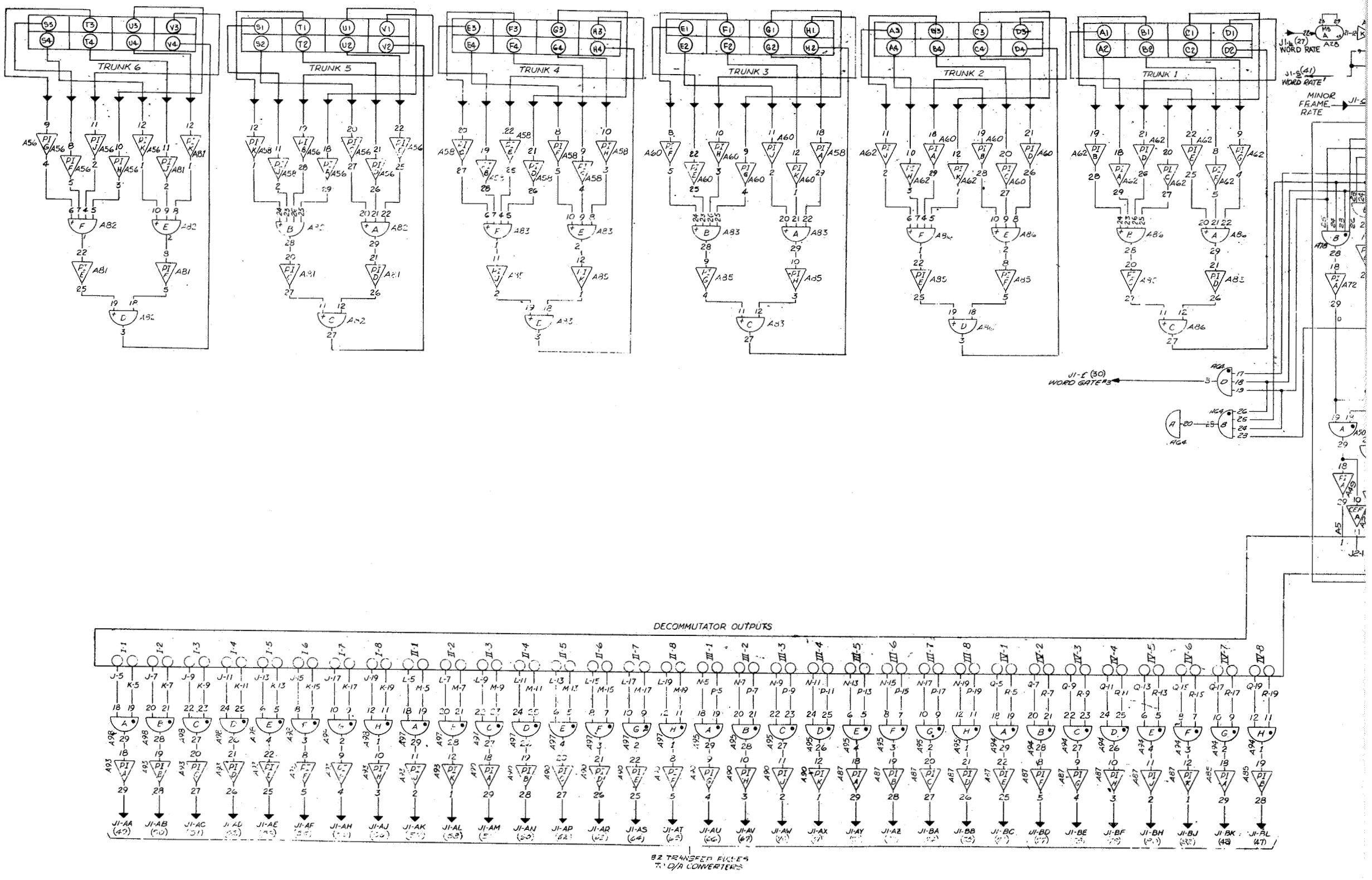
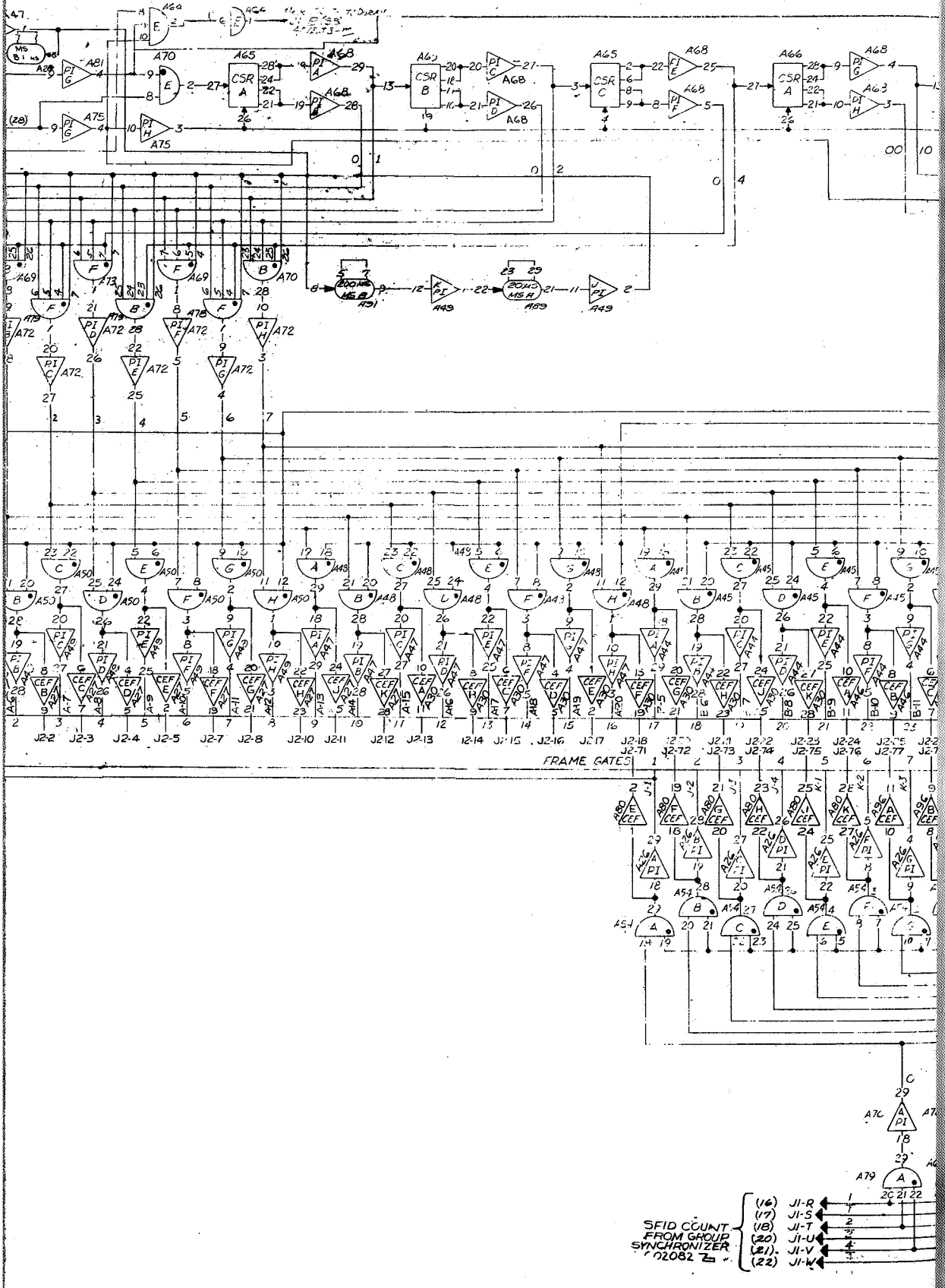


Figure 94. Schematic and Assembly for Video Amplifier Card

FOLDOUT FRAME 1

FOLDOUT FRAME 2




FRAME GATES
SFID COUNT FROM GROUP SYNCHRONIZER
(16) J1-R
(17) J1-S
(18) J1-T
(20) J1-U
(21) J1-V
(22) J1-W

NOTES:
1. NUMBERED PIN DES SHOWN IN PARENTHESES (..) ARE FOR SYSTEMS 1, 2, 5, 6. LETTERED PIN DES NOT SHOWN IN PARENTHESES ARE FOR SYSTEM 4.

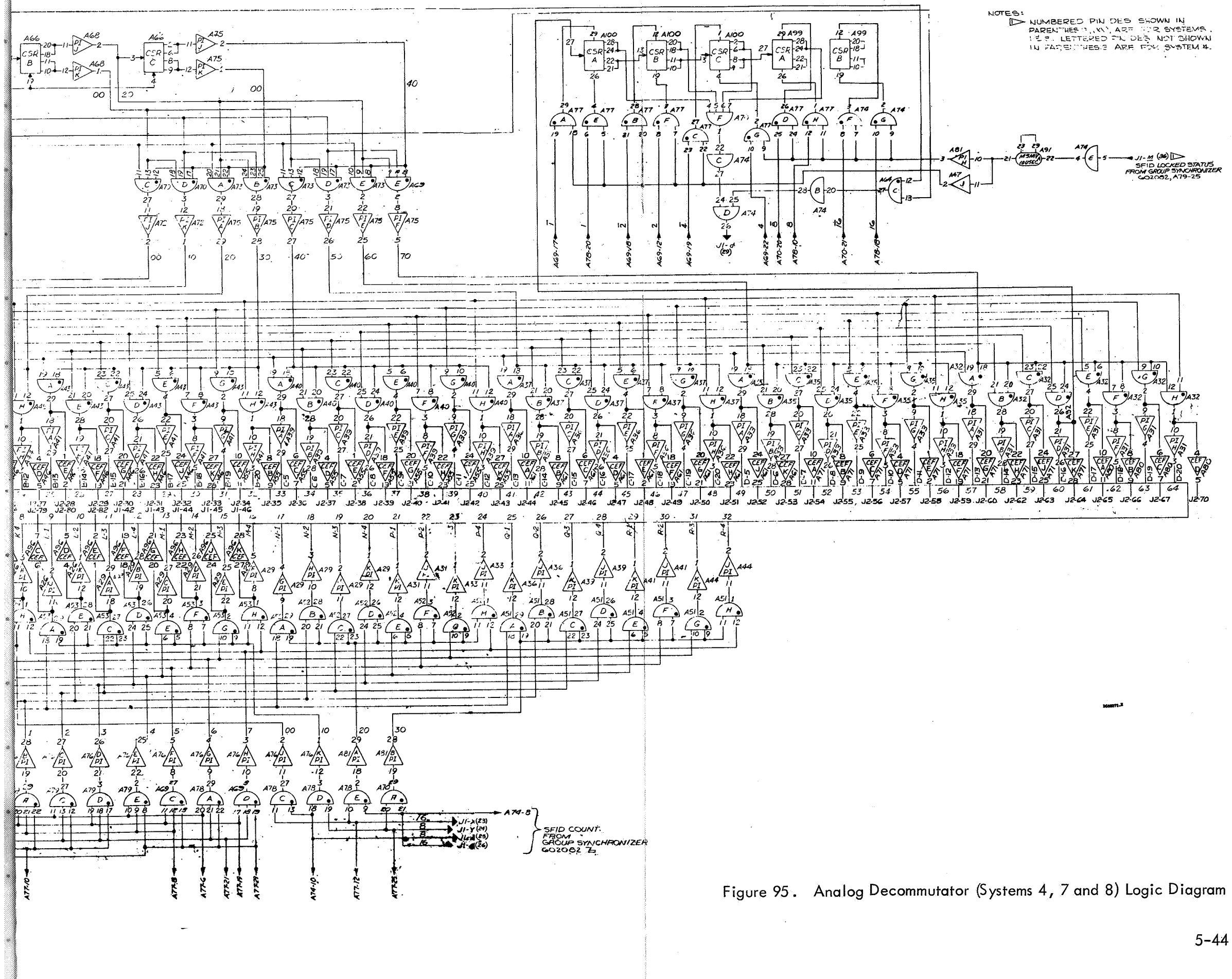
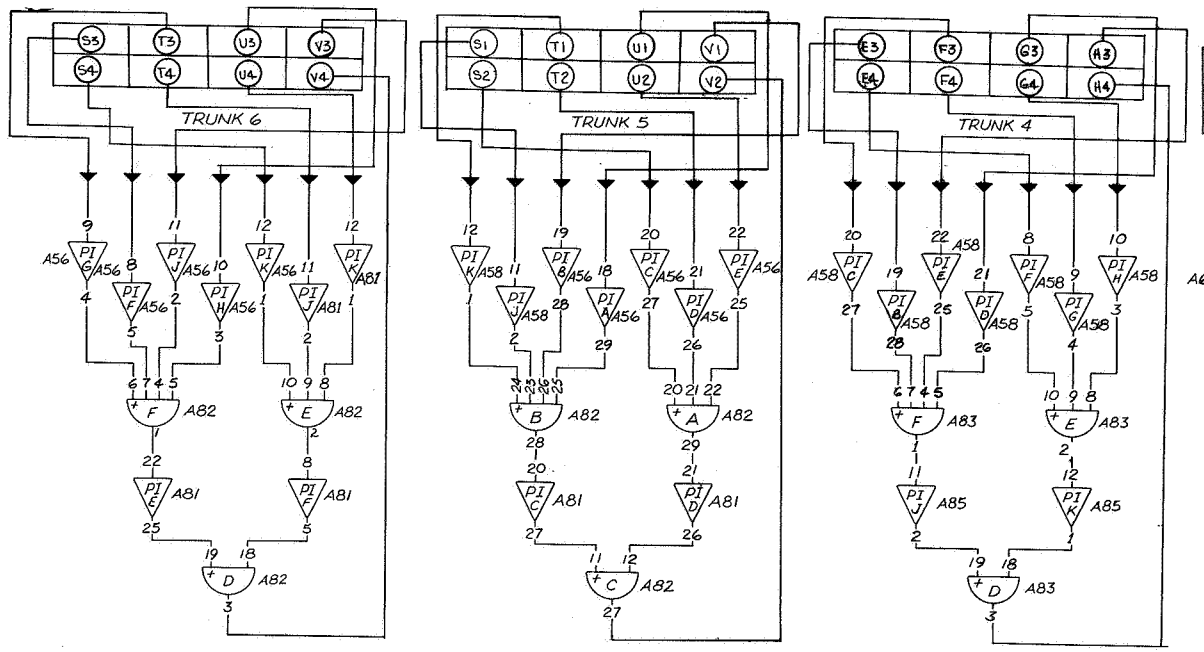
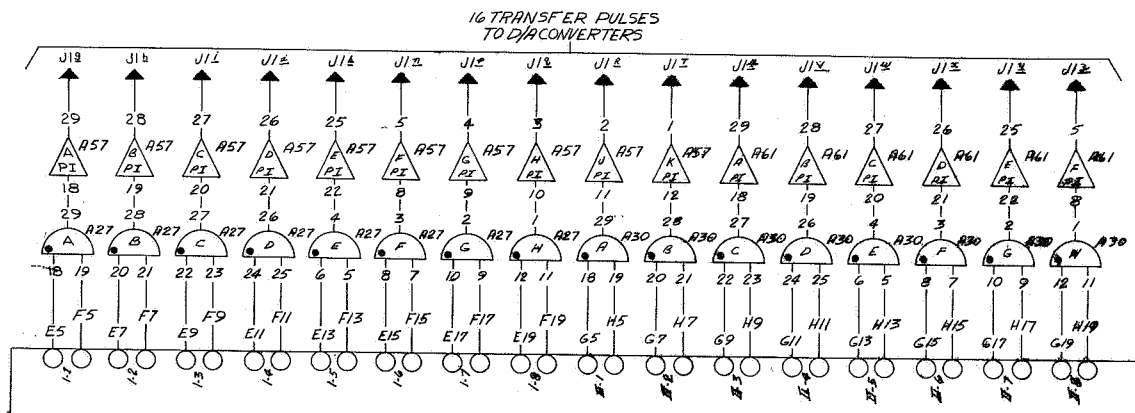


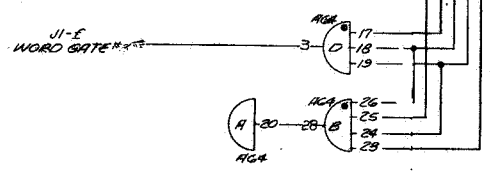
Figure 95. Analog Decommutator (Systems 4, 7 and 8) Logic Diagram

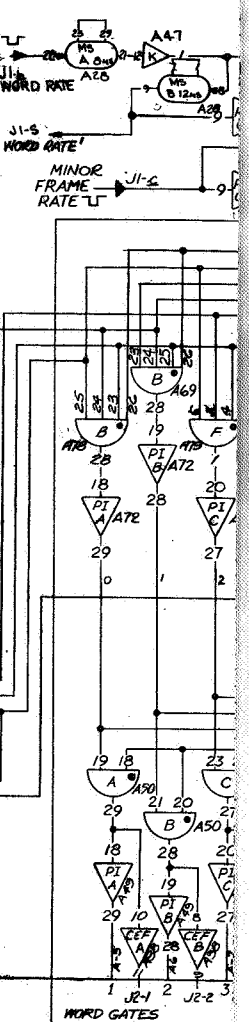
FOLDOUT FRAME 1

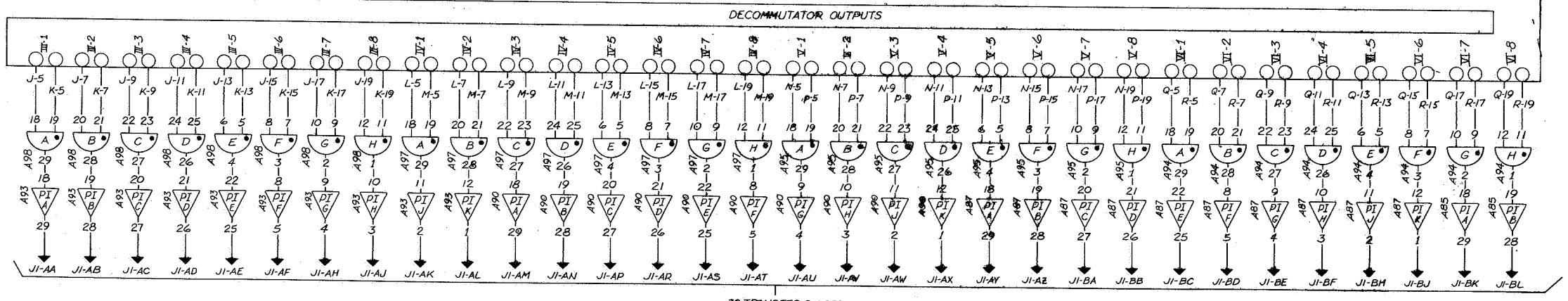
FOLDOUT FRAME 2











FOLDOUT FRAME 3

FOLDOUT FRAME

FRAME GATES

SFID COUNT FROM GROUP SYNCHRONIZER G02082

SFID COUNT FROM GROUP SYNCHRONIZER G02082

FOLDOUT FRAME 4

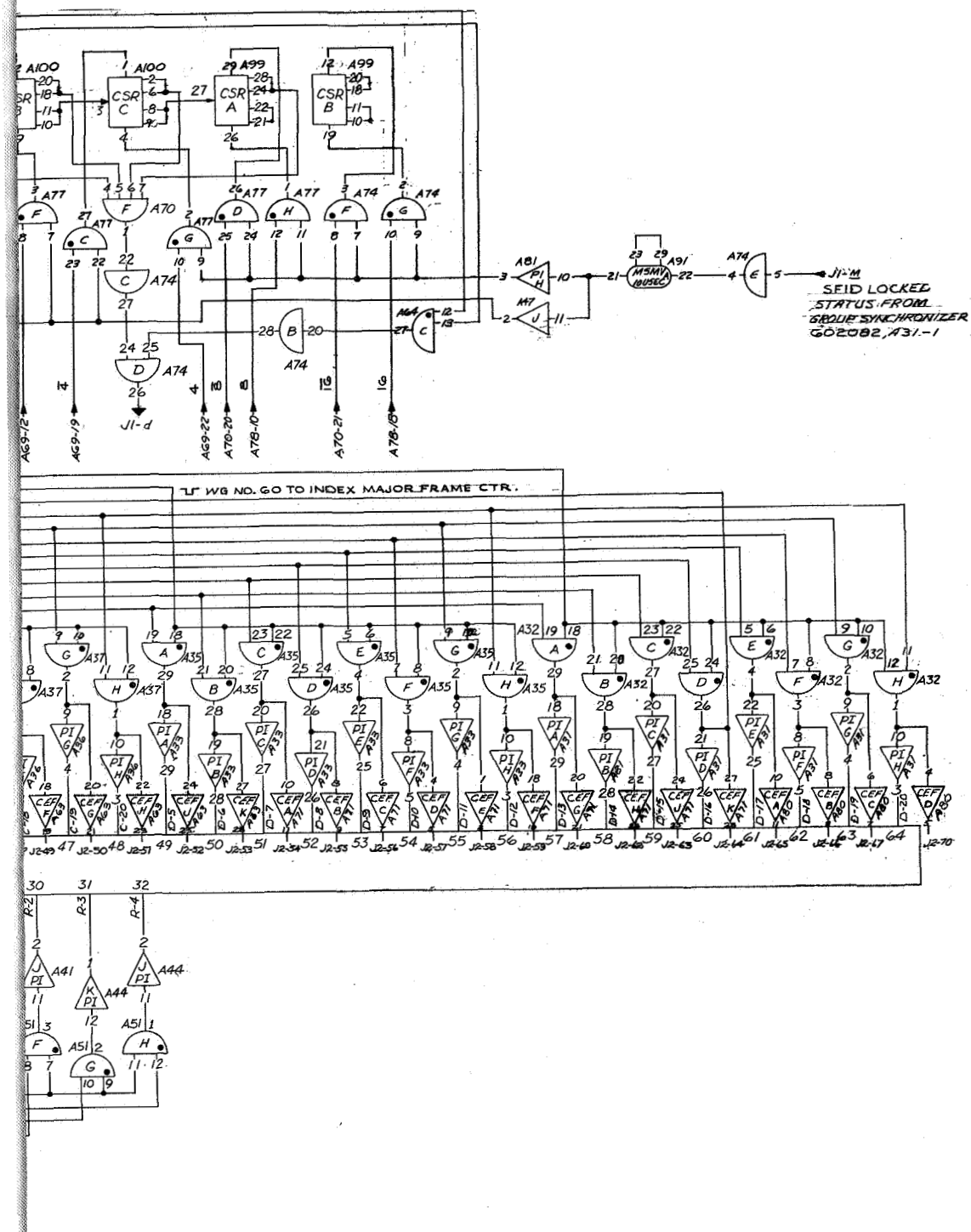


Figure 96. Analog Decommutator (System 5) Logic Diagram

5.3.3.5. DIGITAL DECOMMUTATOR. The configuration of the digital decommutators in Systems 7 and 8 and Systems 4 and 5 vary both in type of decommutation and channel capability. Systems 4 and 5 have a single bit decommutation capability. This permits the placing of any single bit onto any given output channel.

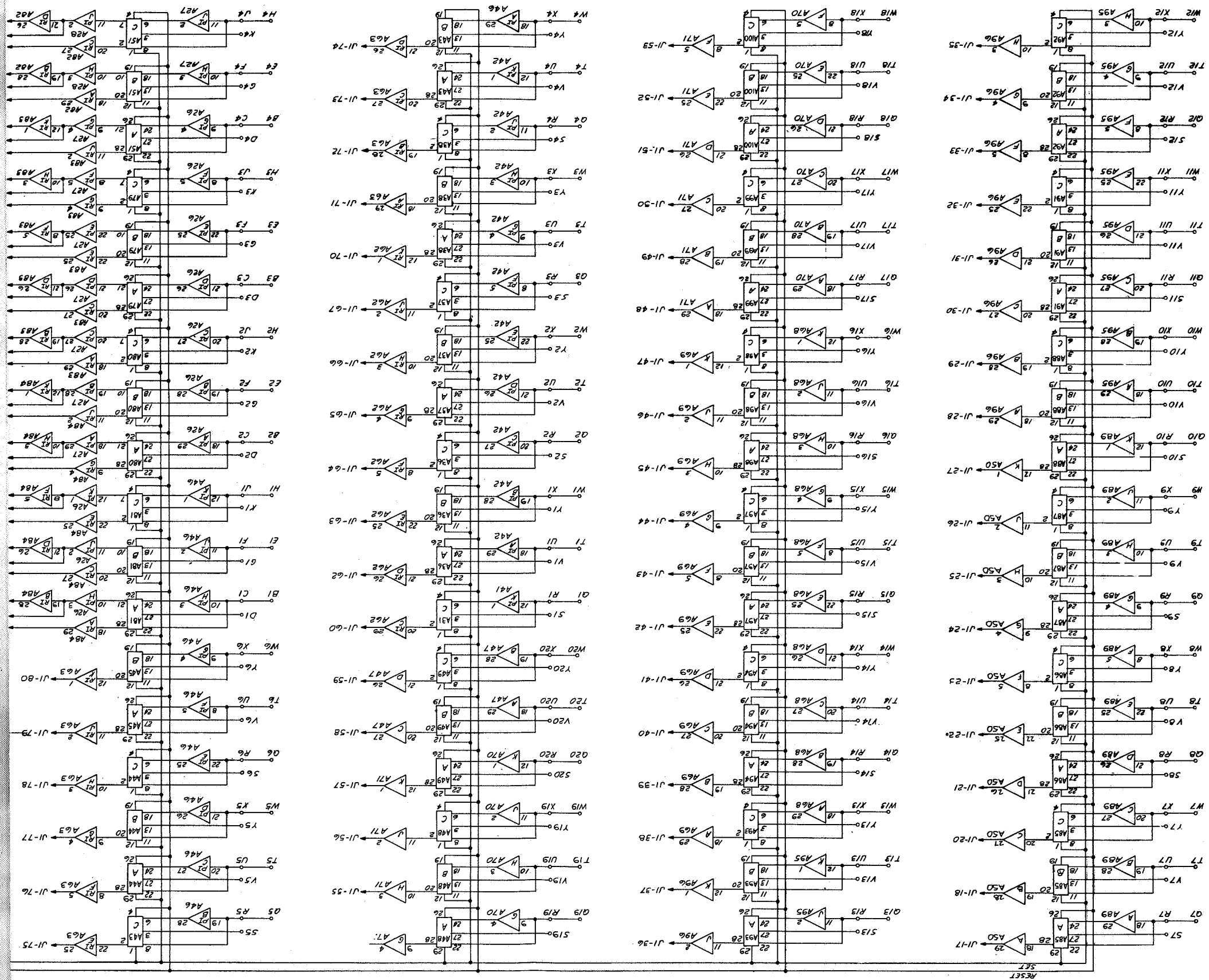
Systems 7 and 8 only have the capability to decommutate out a single word, consisting of the seven data bits in that word. This limits the flexibility but not the output channel capability of these digital decommutators.

5.3.3.5.1. DIGITAL DECOMMUTATOR (SYSTEM 5). The digital decommutator for System 5 (figure 97) consists of seventy-five cards located in the digital decommutator drawer, a front panel-mounted patch panel and fifteen cards located in the time code display drawer. The layout of the digital patch panel was changed from that of the panel in Systems 7 and 8 because of the different type of decommutation. The new layout for the System 4 and 5 digital patch board is shown in figure 74.

Each of the seven broadside data bits from the group synchronizer drawer is routed into the time code display drawer through a single inverter and then into two complementary emitter followers. The inverters are A80A through A80G and the complementary emitter followers are A67B through A67K and A63A through A63E. The output of each emitter follower is routed out of the time code display drawer, into the digital decommutator drawer and finally to two patch panel holes. This leaves a capability of having four patch cards from each data bit.

Each subcommutated digital channel in the format is located in a given frame and given word in that frame. Each prime commutated digital channel is located in a given word in every minor frame. The necessary minor frame and word strobes were brought in to generate the forty subcommutated data strobes and nine prime-commutated data strobes. A Sync Confirmed signal was brought in through A80H, A71K and A67A to provide an enable signal on each of the forty-nine strobe gates only when the system is in sync. Each of the word and minor frame strobes were first routed through an inverter before being gated with the Sync Confirmed signal.

The output of each data strobe gate was routed through a complementary emitter follower, out of the time code display drawer, into the digital decommutator drawer and to the respective holes in the patch panels. Table 14 lists which signals are used to generate each of the forty-nine strobes.


RESET
SET
BOLDOUT FRAME 1

FOLDOUT FRAME 2

FOLDOUT FRAME 3

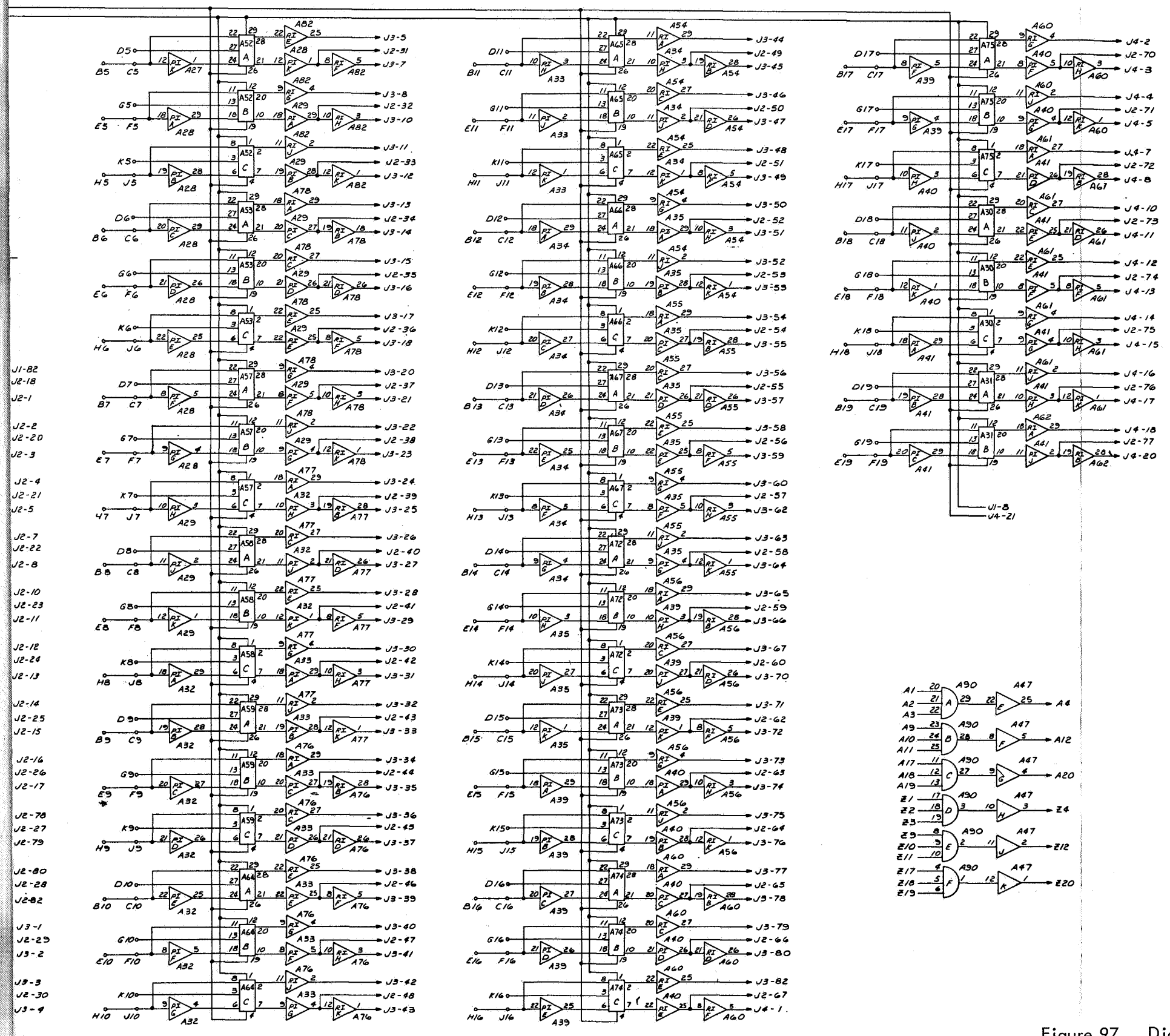


Figure 97. Digital Decommutator (System 5) Logic Diagram

Table 14.

Subcommutation

Subcom. Channel No.	Minor Frame	Word
1	1	12
2	1	16
3	2	21
4	2	25
5	3	29
6	3	33
7	4	36
8	4	37
9	4	40
10	4	41
11	5	44
12	5	48
13	6	52
14	6	53
15	6	56
16	6	57
17	8	4
18	8	5
19	8	8
20	8	9
21	9	60
22	10	5
23	11	12
24	11	13
25	11	16
26	11	17
27	12	20
28	12	24
29	13	28
30	13	29
31	13	32
32	13	33
33	14	37
34	14	40
35	14	41
36	15	45
37	15	49
38	16	52
39	16	56
40	16	57

Table 14 (Continued)

Prime

Prime Com. Channel No.	Word
1	7
2	10
3	14
4	27
5	31
6	42
7	46
8	59
9	63

Each of the digital decommutator channels consists of a Counter Shift Register (CSR) with the strobe line brought out to a single patch hold. The set-steer is brought out to two holes bussed together and the input to an inverter whose output drives the reset-steer line. The output of each CSR is buffered with a power inverter, a relay driver or both.

Decommutation is performed in the following manner. A given digital word, subcommutated or prime-commutated, is selected by patching one of the forty-nine data strobes into the strobe lead of any desired channel. The output of the channel will be hard wired to a given event recorder channel, event pen channel or lamp channel. Then the desired bit in the word selected is patched into one of the data input lines of the CSR. This routes a broad-side data bit to one steer input and an inverted data bit to the other steer bit. At the proper time, the data strobe inputs the state of the selected bit into the CSR. The state of the CSR will not be changed until the next data strobe.

System 5 has a total capability of 116 single bit channels. The first 56 of these have three outputs per channel. The first output is routed through a relay driver. This output will be used to drive a single indicator lamp (A-lamps). The second output is off a power inverter and is used to drive a single event channel on the digital recorder. The third output is routed through another relay driver to drive a different indicator lamp (B-lamps).

The next 42 channels have a single power inverter off of the true side of the CSR. Each power inverter drives a single event pen mounted in one of the analog recorders.

The last 18 channels have a single relay driver off the true side of the CSR. Each relay driver is used to drive a single indicator lamp (C-lamps). It should be noted that the A-lamps, B-lamps, C-lamps, event pens for the analog recorders and interconnecting cables for the above, were not supplied as part of this modification. Also, to provide even more flexibility, six-three input OR gates were provided to permit a super-commutation capability. Also six four-input busses were provided for easier patching.

A master set-reset switch is routed to every CSR to set or reset all channels in the digital decommutator. A digital decommutator inhibit line is also brought in and tied to the master reset line. This line is controlled from the system control front panel by a two-position switch. In the active position, a negative 10 volts is put on the master reset line, disabling all registers in the digital decommutator.

5.3.3.5.2. DIGITAL DECOMMUTATOR (SYSTEM 4). The digital decommutator for System 4 (figure 98) consists of approximately 63 cards, all located in the digital decommutator drawer, and a front panel-mounted patch panel.

The type of decommutation, strobe generation, data bit generation and channel strobing is done exactly as in System 5. The only variation is in the number of channels provided and output drive capability.

System 4 has capability for decommutation of 84 digital channels. The first 56 channels have a single power inverter off of the false side of the CSR which is routed to a single event channel on the event recorder.

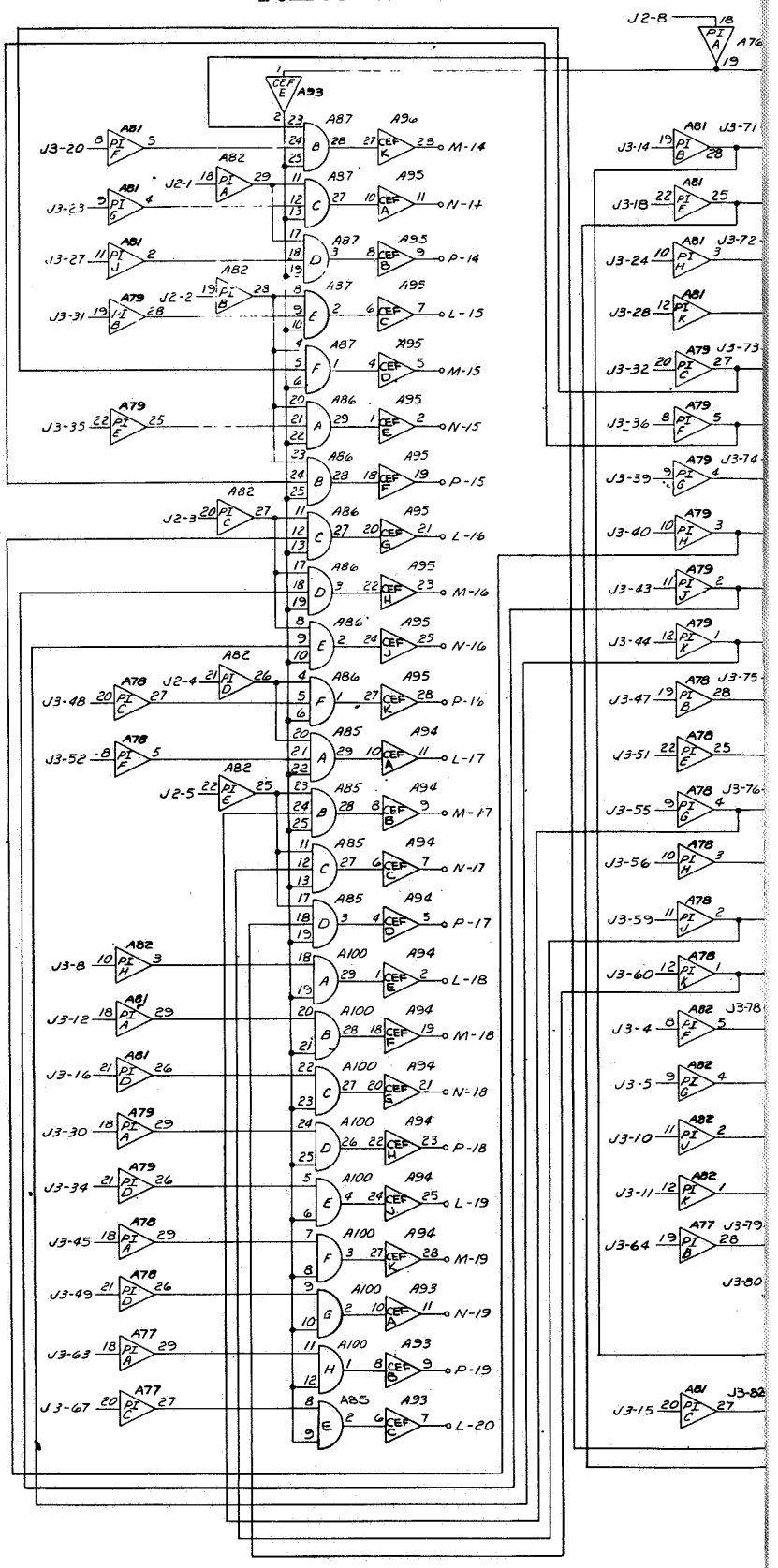
The last twenty-eight channels have a single power inverter off of the true side of the CSR. This power inverter drives a single event pen on an analog recorder. As stated above, the event pens were not provided as part of the modification.

As in System 5, six, three-input OR gates and six, four-input busses are also provided. A master set-reset switch allows setting or resetting all 84 channels at once. As in System 5, a digital decommutator disable line is brought in and tied to the master reset line to disable the all digital decommutator registers.

5.3.3.5.3. DIGITAL DECOMMUTATOR (SYSTEMS 7 AND 8). The digital decommutator added to Systems 3 and 1 (Systems 7 and 8) (figure 99) during the modification consists of twelve 7-bit storage registers and a front panel-mounted patch panel. The unit receives the parallel 7-bit data word output from the group synchronizer output register and, dependent on patch panel programming, loads data words from the program-selected time slots into selected registers for application to the event recorder or the event pens on the analog recorders.

The 7-bit data word output from the group synchronizer output register is received through digital decommutator power inverters on A59A-A59K and A74A-A74D. True and inverted data outputs from the power inverters are routed through complementary emitter followers A73A-A73H and A72A-A72F and applied to as steering inputs of the twelve 7-bit storage register flip-flops. Word and frame gate signals, patch-selected on the front patch panel are routed to 2-NOR AND gates on A66A-A66H and A67A-A67D. Upon coincidence of the selected frame and word time slot, the AND gate associated with selected event recorder channels is enabled to develop a trigger pulse to load the data word into the 7-bit register for these channels. When recording of supercommutated data (data sampled every frame) is required, the frame gate patch connection is left open and the AND gate is enabled every selected word time to load the supercommutated data into the selected storage register. Outputs from the storage register flip-flops are routed through power inverters to event recorder inputs.

FOLDOUT FRAME 1



FOLDOUT FRAME 2

FOLDOUT FRAME 3

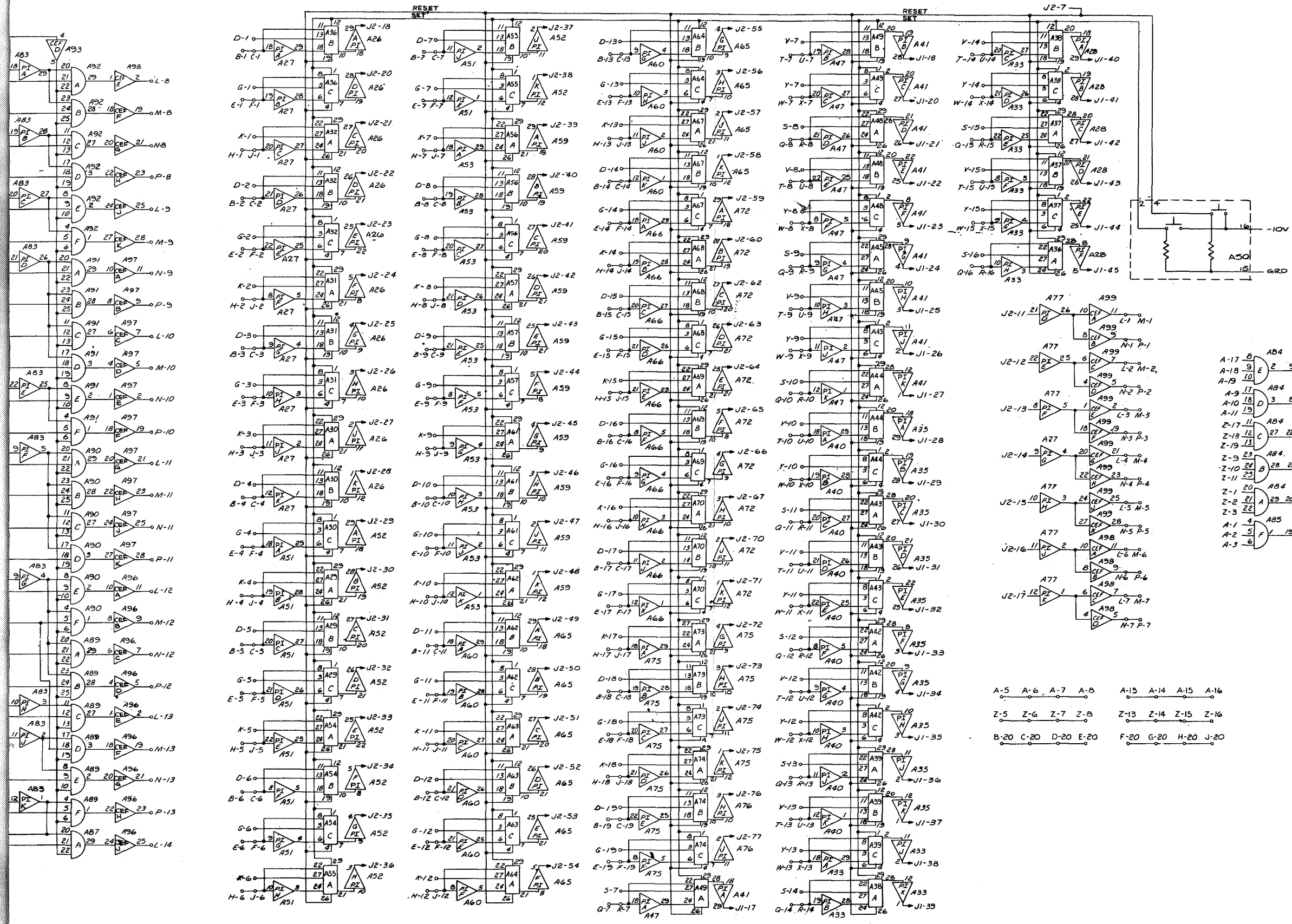
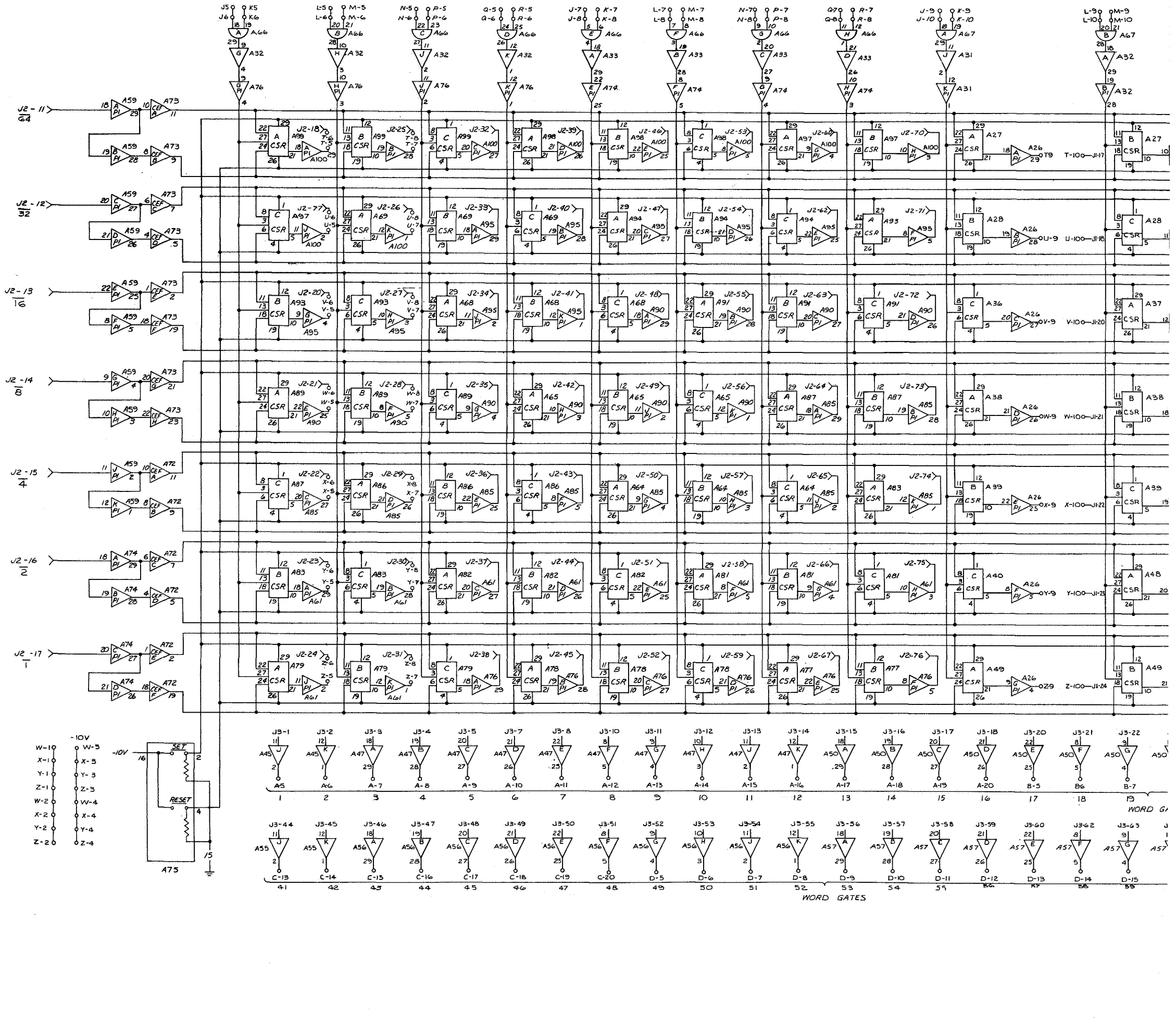
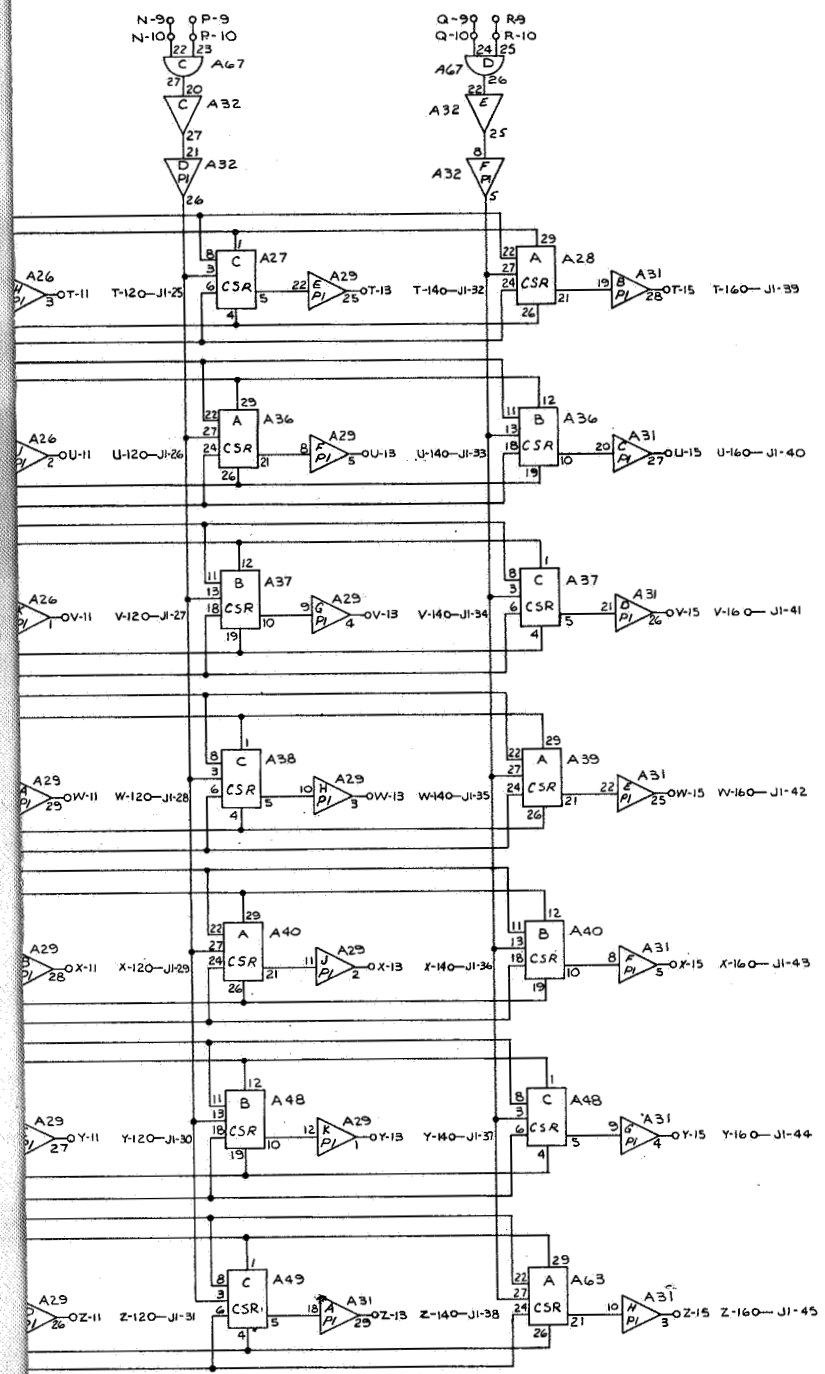


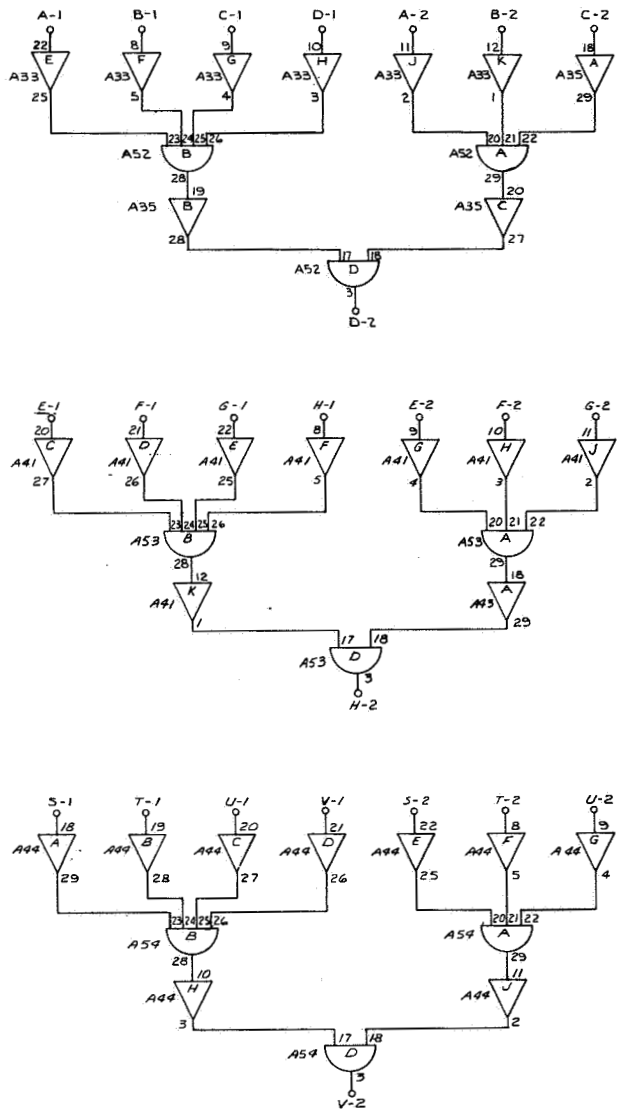
Figure 98. Digital Decommutator (System 4) Logic Diagram

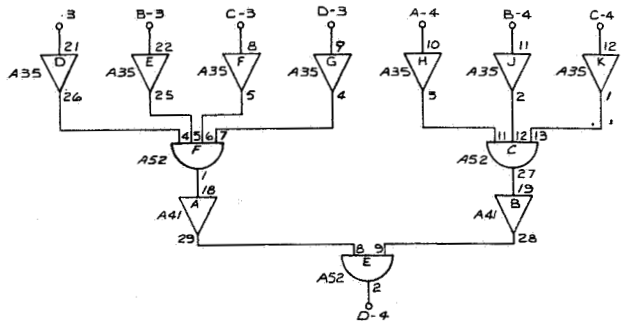
FOLDOUT FRAME 1

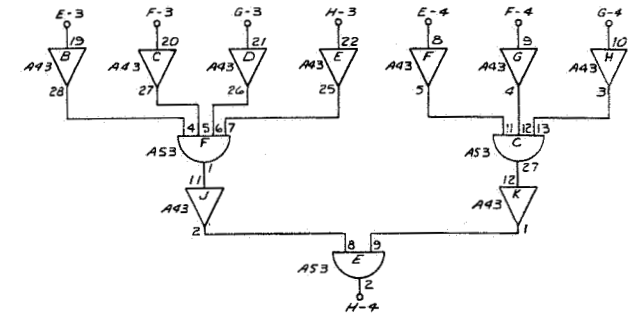


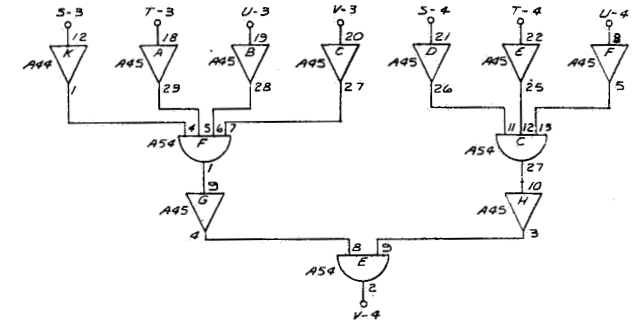
FOLDOUT FRAME 2











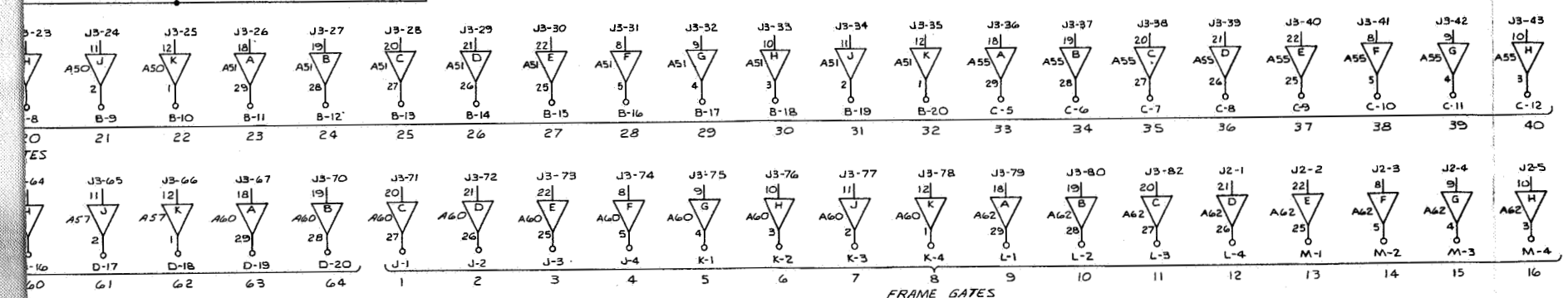


Figure 99. Digital Decommutator (Systems 7 and 8) Logic Diagram

The outputs of the last four registers are routed to 28 output holes on the patch panel. Another 28 input holes go directly to the external connector for routing to the event pens of the analog recorders. This permits shifting of given bits in four words to any of the 28 event pen channels. A master set-reset switch is provided to strobe all ONE's or all ZERO's into every register.

To provide word gate 1-64 strobes and frame gate 1-16 strobes, these signals were routed from the Analog Decommutator into a power inverter and then to the patch panel. These inverters were, respectively, A45J, A45K, A47A-A47K, A50A-A50K, A51A-A51K, A55A-A55K, A56A-A56K, A57A-A57K, A60A-A60K, and A62A-A62H.

A single common trunk which ties 8 patch holes together was provided. Also, an inhibit trunk which ties 8 holes to -10 volts is provided. Six, seven-input AND gates are used as part of the patching arrangements. These also have the inputs and outputs located on the patch panel. The circuits used to implement these circuits are power inverters. A33E through A33K, A35A through A35K, A41A through A41K, A43A through A43K, A44A through A44K and A45A through A45H.

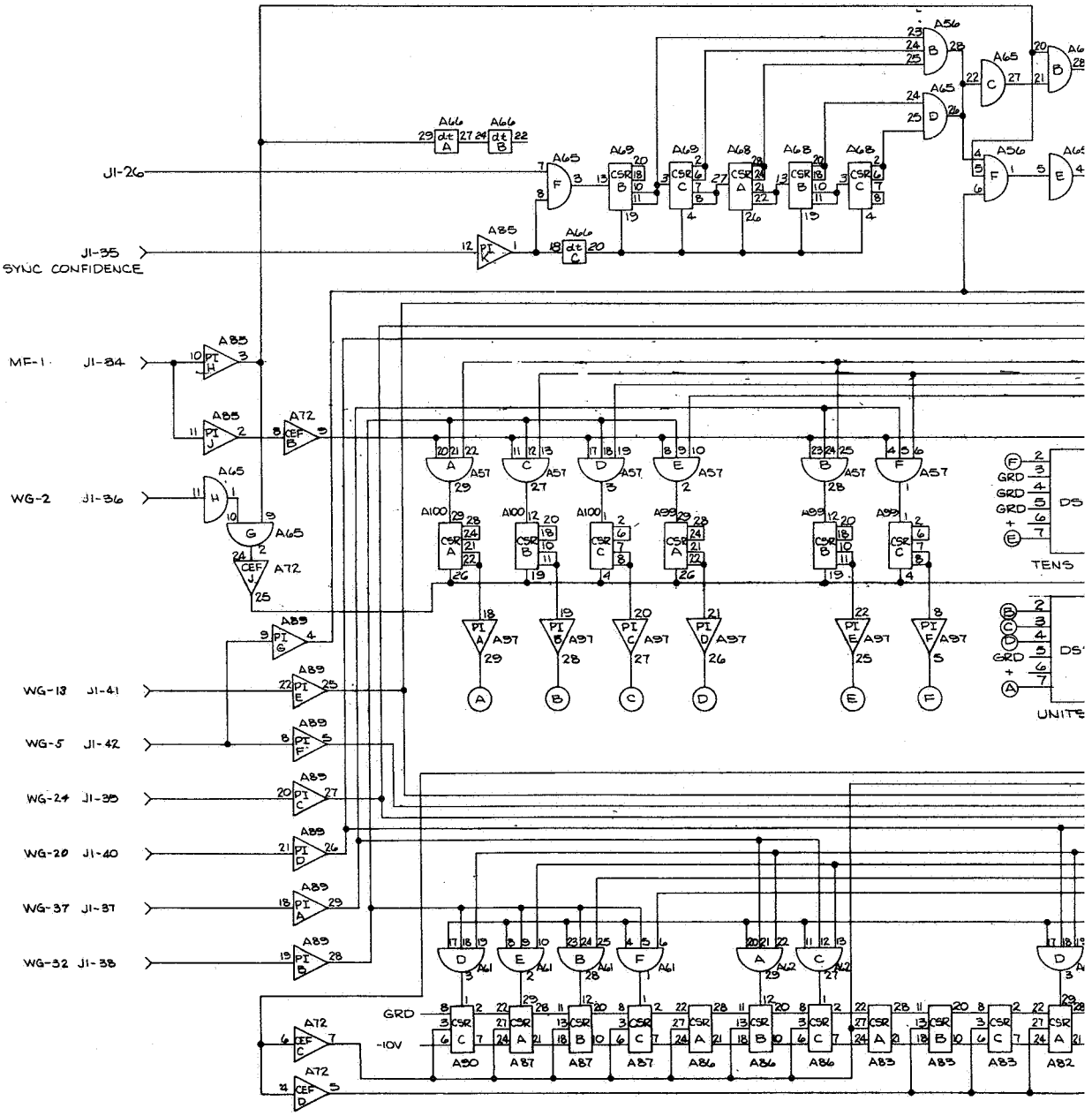
The layout of the digital decommutator patch panel, shown in figure 74 is basically the same arrangement as in the analog decommutator patch panel. Inputs and outputs to and from the patch panel are designated on the digital decommutator logic diagram (figure 99).

5.3.3.6. TIME CODE DISPLAY

The time code display unit (figures 100 and 101) included in the system modification provides logic circuits for decimal display of hours, minutes and seconds of time code data and for generation of time code plots on analog and digital recorders.

The four data bits containing time code are routed from the group synchronizer output register, through the digital decommutator, to input CEF's in the time code display. From the outputs of the CEF's, the data is routed to the input AND gates, A57A through A57F, A58A through A58F, A60A through A60F, A61A and A61C. During each first minor frame period, the FRAME GATE 1 signal from the decommutator is received through power inverter A85J and complementary emitter follower A72B to enable all register input gates. During word time 5 of the first frame, units of seconds time code data is received and WORD GATE 4 signal from the Decommutator is routed through power inverter A89E to strobe AND gates A60B through A60E. The strobe pulse loads CSR's A94B, A94C, A91A and A91B with units of seconds time code data. During word time 13 of the first frame, tens of seconds time code data is received. The WORD GATE 12 signal received through power inverter A89E strobes AND gates A60F, A61A and A61C to load tens of seconds data into CSR's A91C, A90A

FOLDOUT FRAME 1



FOLDOUT FRAME 2

FOLDOUT FRAME 3

NOTES:

PARTIAL REF DESIGNATIONS ARE SHOWN, FOR COMPLETE DESIGNATION PREFIX WITH UNIT NO. OR SUBASSY DES.

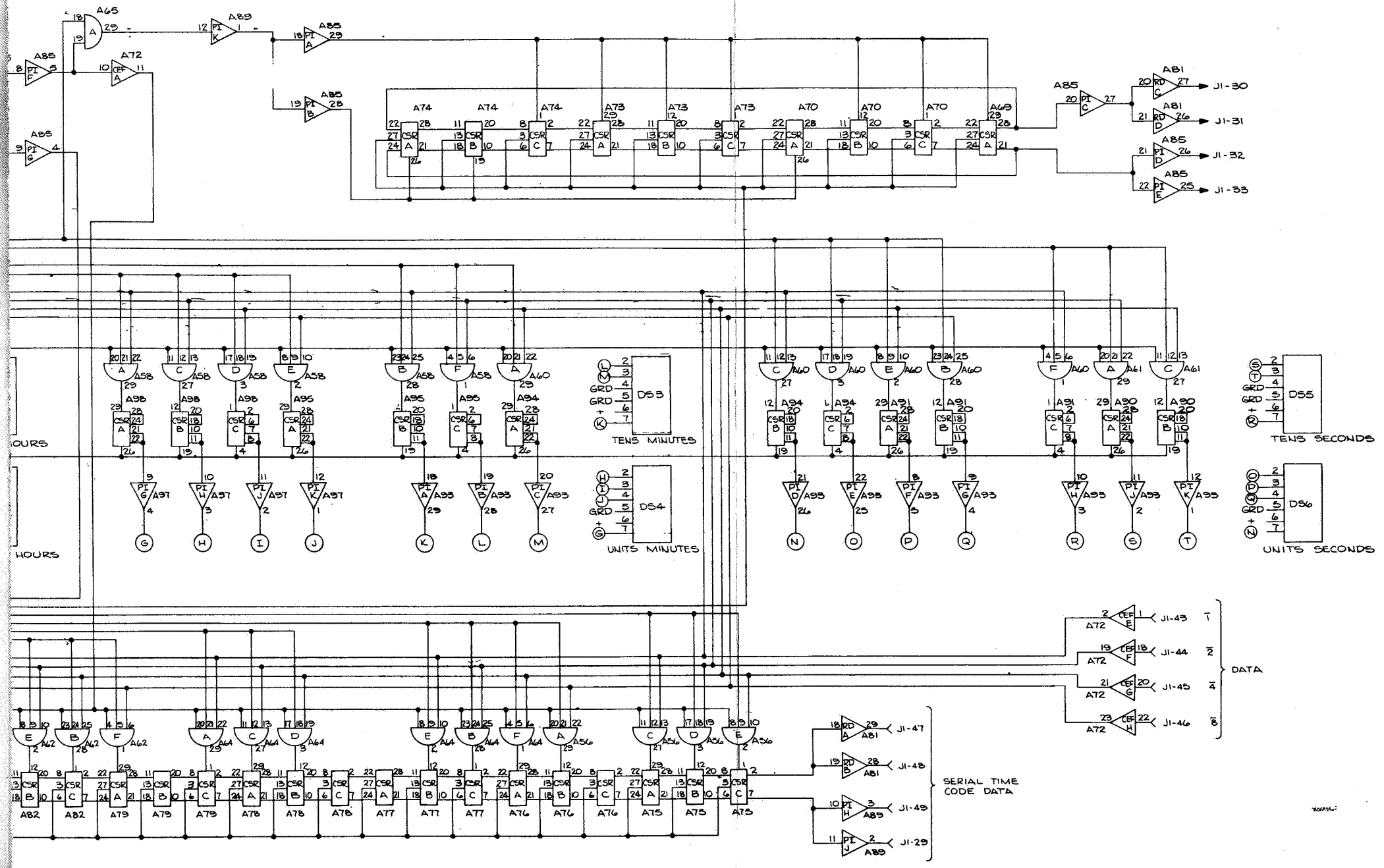


Figure 100. Time Code Display (Systems 4, 7 and 8) Logic Diagram

SUBCOM STROBES 1-20
TO DIGITAL DECOM 8/07/200
J4-22 THRU J4-62

FOLDOUT FRAME 1

FOLDOUT FRAME 2

J3-59
J3-60
J3-62
J3-63
J3-64
J3-65
J3-66
J3-67
J3-70
J3-71
J3-72
J3-73
J3-74
J3-75

J1-26
J1-35 SYNC CONFIDENCE
MF-1 J1-34
WG-2 J1-36
WG-18 J1-41
WG-5 J1-42
WG-24 J1-35
WG-20 J1-40
WG-37 J1-37
WG-32 J1-38

DS1 TENS HOURS
DS2 UNITS HOURS
TENS
UNITS

GRD
-10V

A54
J4-75 SET
J4-73 RESET
-10

FOLDOUT FRAME 4

NOTES:

PARTIAL REF DESIGNATIONS ARE SHOWN; FOR COMPLETE DESIGNATION, PREFIX WITH UNIT NO. OR SUBASSY DES.

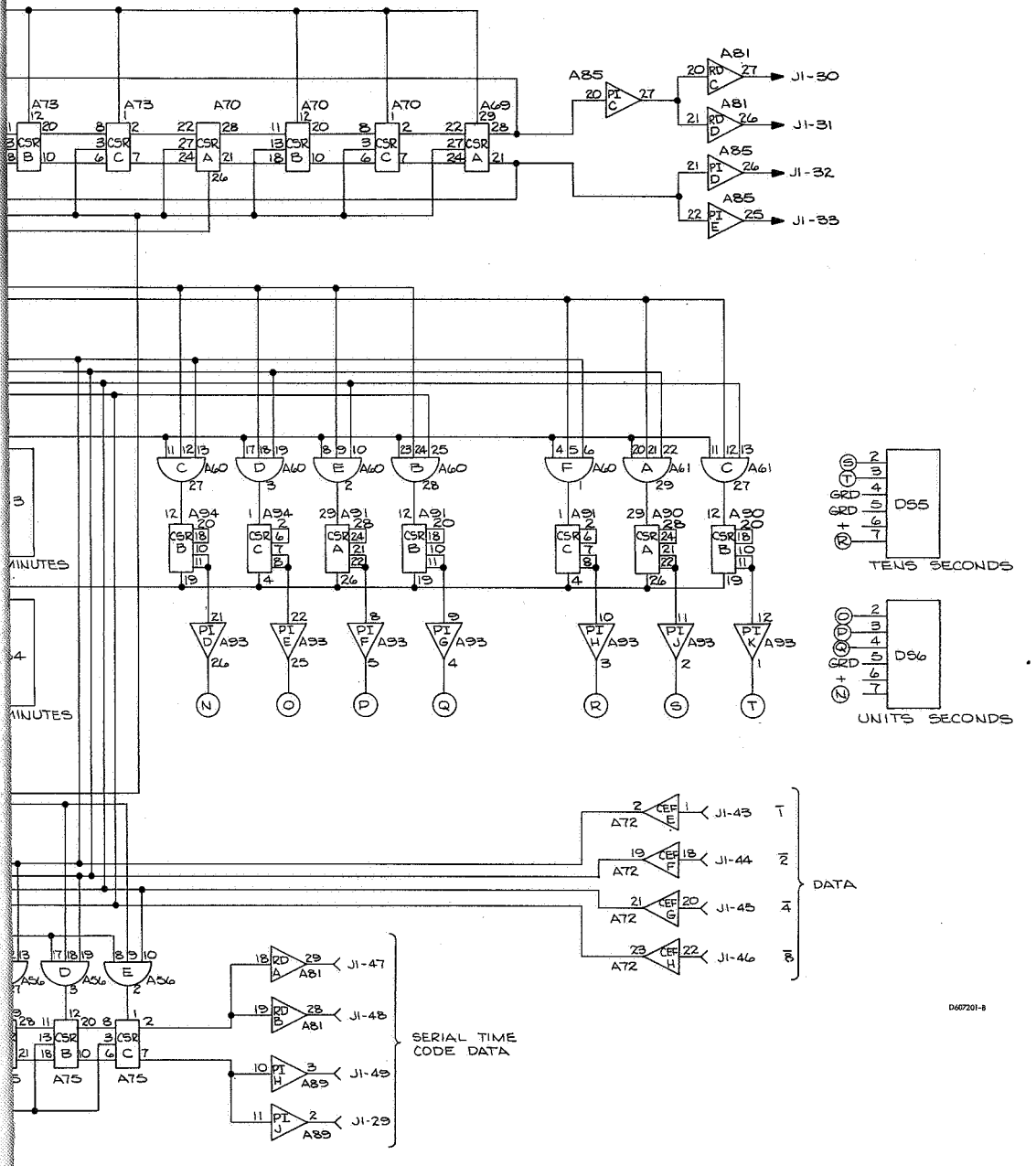


Figure 101. Time Code Display (System 5) Logic Diagram

and A90B. Similarly, WORD GATE 20 signal through power inverter A89D loads units of minutes data into CSR's A98A, A98B, A98C and A95A WORD GATE 24 signal through power inverter A89C, loads tens of minutes data into CSR's A95B, A95C and A94A; WORD GATE 32 signal, through power inverter A89B, loads units of hours data into CSR's A100A through A100C, and A99A and WORD GATE 37 signal, through power inverter A89A, loads tens of hours data into CSR's A99B and A99C.

The display register is reset just before new data is strobed into the register. This is done by ANDing the minor frame No. 1 signal and word No. 3 signal at A65G, then routing the reset pulse through complementary emitter follower A72J to the reset side of all of the CSR's. Display register CSR outputs are routed through power inverters on A97 and A93 to drive unitary readout indicators DS1 through DS6 that provide a decimal readout of time code data in hours, minutes, and seconds. The decimal readout is updated during each first minor frame.

A second 28-bit shift register is used to store and shift out a serial time code. The shift register consists of the following circuits: A90C, A87A through A87C, A86A through A86C, A83A through A83C, A82A through A82C, A79A through A79C, A78A through A78C, A77A through A77C, A76A through A76C and A75A through A75C. The loading and gating is done exactly as described above only a different set of AND gates is used. The units of hours data is gated in by A61B, A61D, A61E and A61F. Tens of hours is gated in by A62A and A62C. Units of minutes is gated in by A62B, A62D, A62E and A62F. The tens of minutes data is gated in by A64A, A64C and A64D. Units of seconds is gated in by A64B, A64E, A64F and A56A. Finally tens of seconds data is gated in by A56C, A56D and A56E. The output of the register is through two relay drivers, A81A and A81B to the event pens on the analog recorders. The inverted output is routed through two power inverters, A89H and A89J to the event recorder.

The time code display drawer also contains a third register, the marker shift register. It consists of a ten bit shift register with feedback from the last to the first stage. The circuits used are A74A through A74C, A73A through A73C, A70A through A70C, and A69A. This register is loaded broadside with a 0011110111 pattern from power inverters A85A and A85B. The code pattern recirculates in sync with the serial time code register and provides a logic ONE mark on another channel where the time code bits are located. The output of the marker register are routed through A85C and relay drivers A81C and A81D to event pens on the analog recorders. The inverted side is routed through A85D and A85E to the event recorder.

The data bit strobes and shift pulses for the two serial registers are derived from the minor frame counter circuitry in the time code display drawer. A major frame rate pulse is brought in to AND gate A65F and gated with a sync confidence signal. This assures the system is in sync before the counter updates. The sync confidence signal also provides a counter reset signal. AND gate A56B and A65D provide an enable every 32nd major frame, routed through A65C to the AND gate A65B. This signal is gated with a minor frame 1 to enable (via CEF A72A) the data gates to the serial shift register. The same signal is gated (in A65A) with word gate 5 for delay and strobes the marker register with the fixed pattern (given above) through power inverters A89K, A85A, and A85B. At this same time, AND

gates A56B and A65D are inhibiting gate A56F, which generates the shift pulses for both registers. This signal is routed through A65E and A85G to the complementary emitter followers A72C and A72D, to the shift inputs.

Therefore, during the first minor frame after the sync confidence level, the data and pattern is strobed into the registers. Then, during the next 31 major frames, the load gates are inhibited and the shift gates are enabled, permitting the serial time code and marker to be shifted out serially to the recorders.

5.3.3.7. SIMULATOR (FIGURE102 BLOCK DIAGRAM)

Modifications to the simulator include: (a) incorporation of a split-phase code generator to simulate Nimbus-B data signals; (b) modification of bit and word counters to comply with the 62-1/2-word frame format; (c) addition of single word insertion and selectable frame capabilities; and (d) modification to data register input circuits to permit simulator loading of time code. In addition, a time code generator was assembled into a single card file and was mounted in Cabinet 5 to provide simulated time code data.

5.3.3.7.1. SYSTEM 4 AND 5 SIMULATOR MODIFICATIONS

5.3.3.7.1.1. SPLIT-PHASE CODE GENERATION. Split-phase code is generated by toggling a counter shift register (CSR) at the leading edge of each ZERO data bit, ANDing bit rate with the ONE output of the CSR, ANDing bit rate with the ZERO output of the CSR, and OR-gating the resultant signals.

The NRZ output of the simulator data shift register is routed through power inverter A68F to AND gate A59F that is enabled by every ZERO bit in the data signal. The bit rate signal from A32-G is inverted through 2-NOR A46H and provides bit rate sample pulses to AND gates A59F and A59A. The applied NRZ ZERO bit enable and the BIT RATE sample signals to AND gate A59F result in a negative-going output that is coincident with the leading edge of each NRZ data bit. Each negative-going signal from AND gate A59F toggles CSR A92A that alternately enables AND gates A59A and A59C. AND gate A59A is sampled by the bit rate output of A46H and AND gate A59C is sampled by the BIT RATE output of 2 NOR A32G. The outputs of the AND gates are OR'ed by A59D and are routed to filter card A76. Since the CSR changes state with each ZERO bit to alternately enable gating of opposite phases of bit rate, the resultant OR'ed signal changes phase with each ZERO data bit to fulfill split-phase code requirements.

5.3.3.7.1.2. BIT AND WORD COUNTER. Simulator bit and word counters were modified such that the first word of each minor frame is limited to four bits and the remainder of the frame is limited to sixty-two 8-bit words. This results in a minor frame length of 62-1/2 words, as required by the Nimbus B format.

FOLDOUT FRAME 1

FOLDOUT FRAME 2

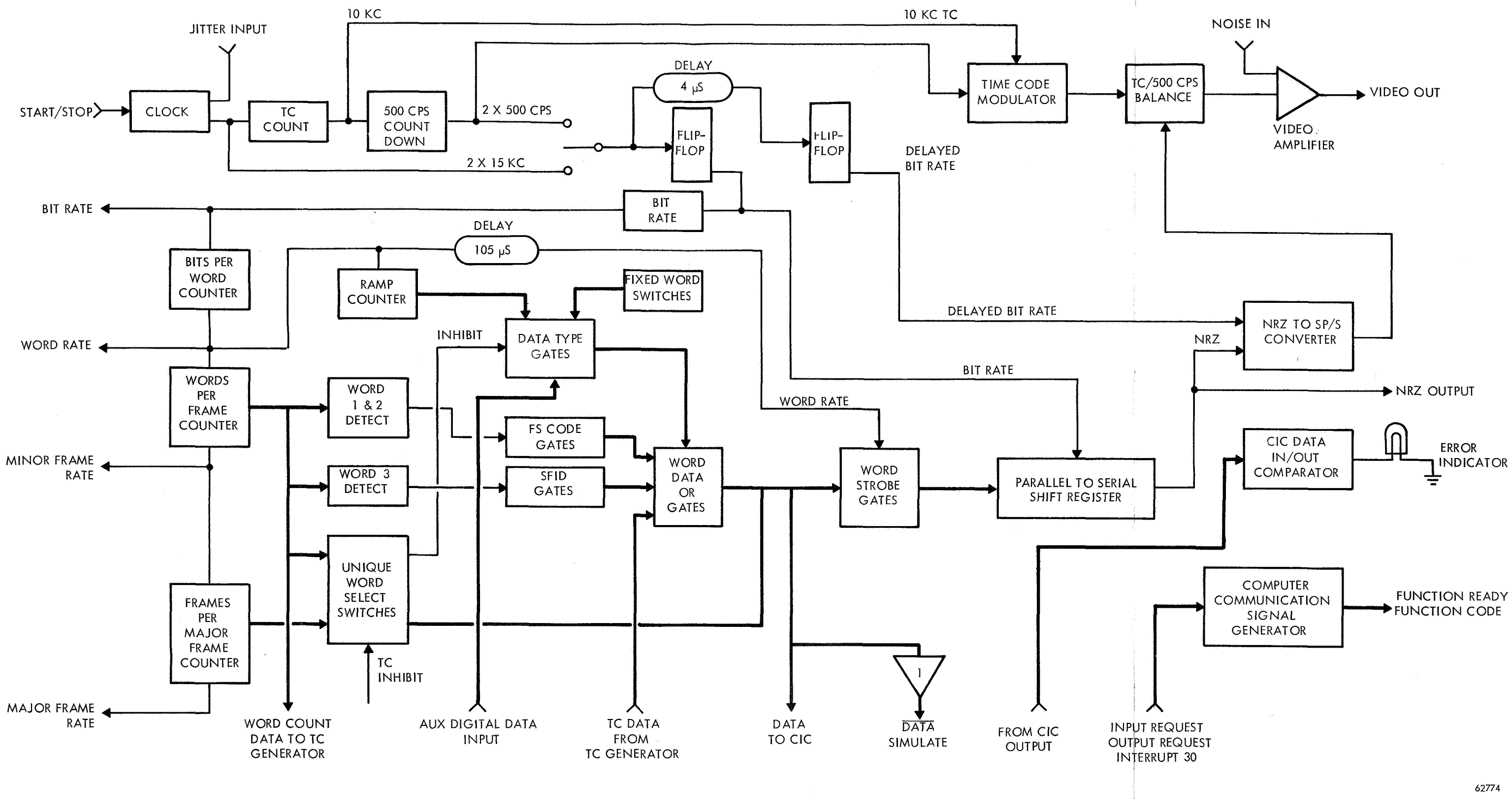
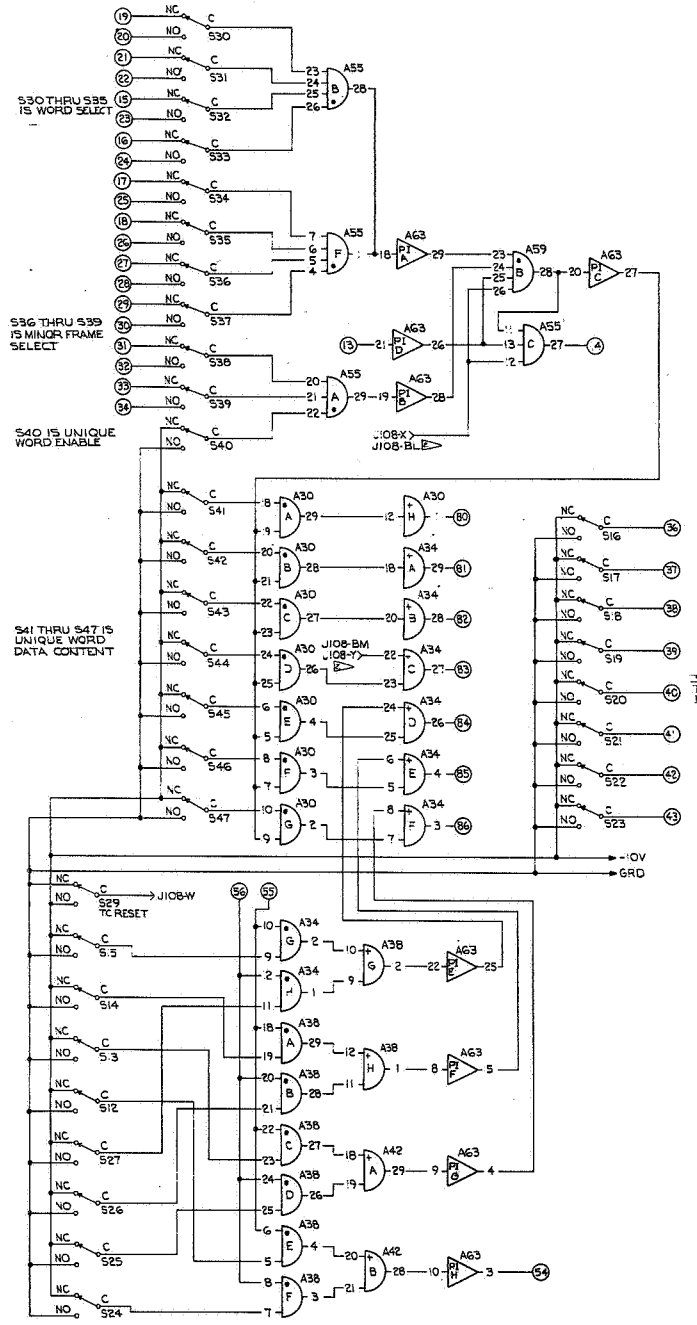
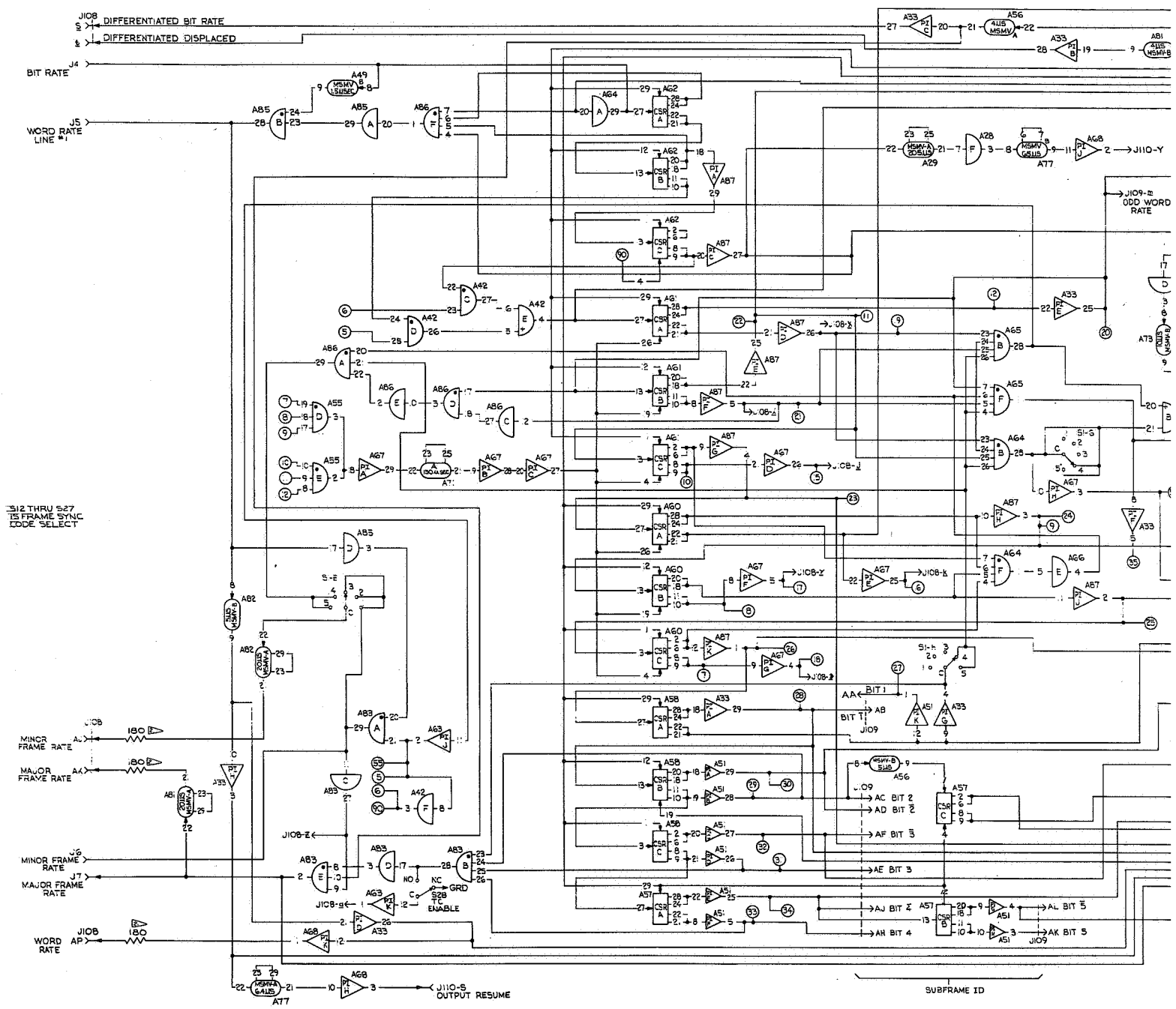


Figure 102. Simulator Functional Block Diagram

FOLDOUT FRAME 1

FOLDOUT FRAME 2



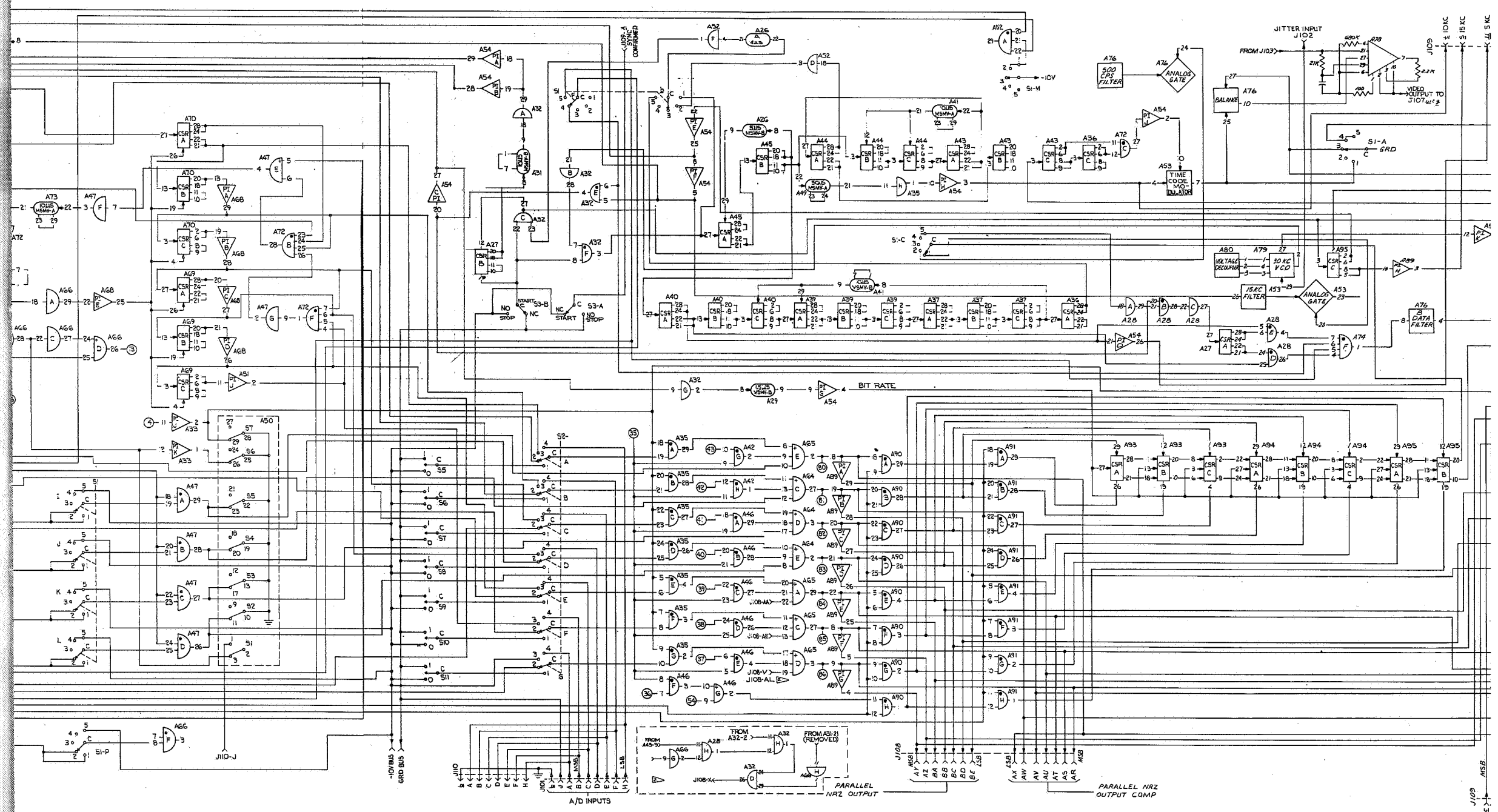


FOLDOUT FRAME

FOLDOUT FRAME

3

FOLDOUT FRAME



FOLDOUT FRAME 4

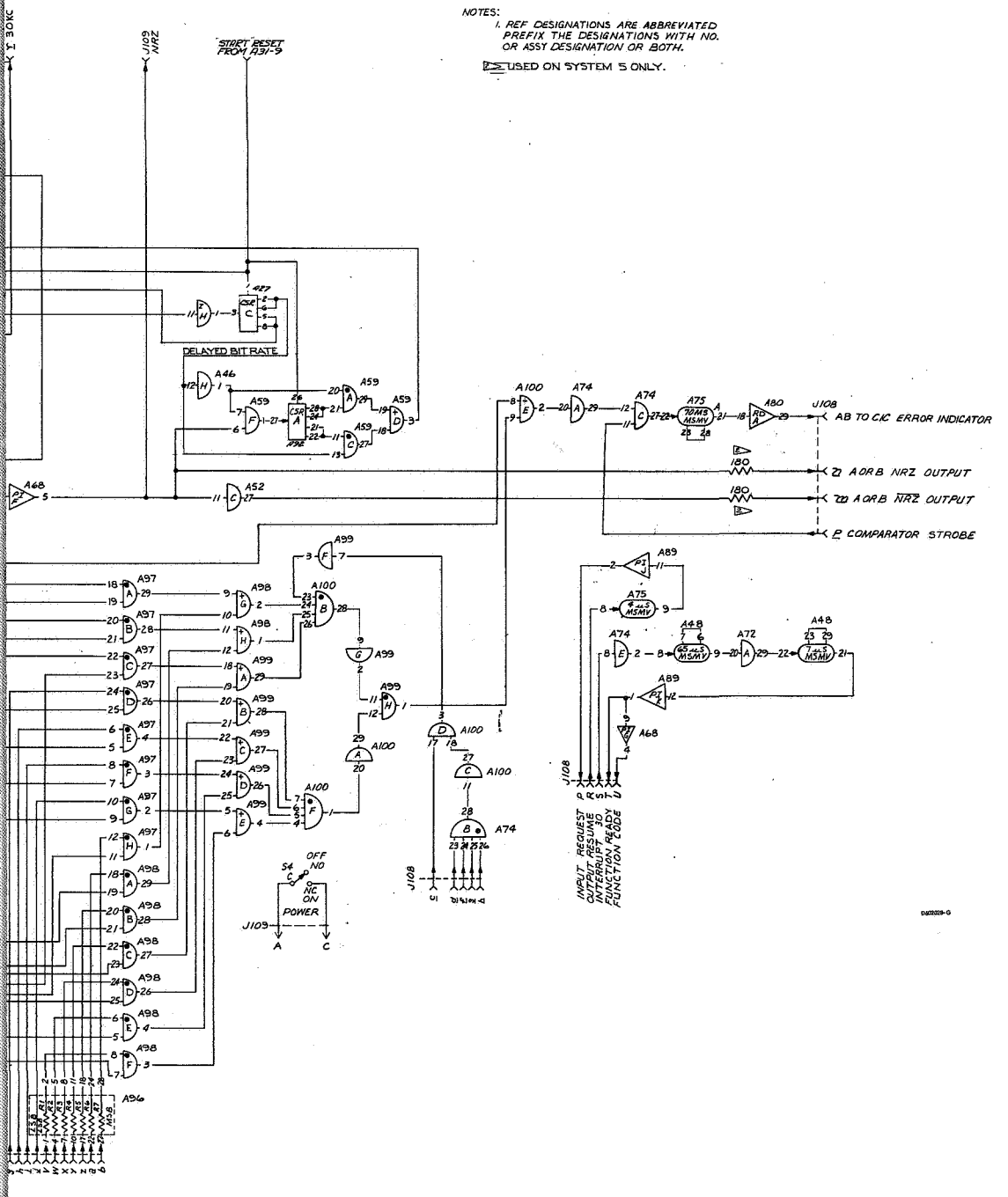


Figure 103. Simulator (Systems 4 and 5) Logic Diagram

Occurrence of the first word of each minor frame is detected by AND gate A65B and routed through power inverter A63J and gate A42F. The output of A42F is routed to the reset lead on A62C. A62C is the last CSR in the bits per word portion of the counter. Therefore, during word No. 1, A62C is held in a reset condition and the bits per word counter only toggles to a count of four. During all of the other words, the counter toggles normally, giving a count of eight bits per word.

Count 62 of the frame counter is detected by AND gates A55D and A55E that produce a negative output through A67A to monostable multivibrator A71A, and the resultant 2-microsecond output is routed through power inverters A67B and A67C to reset the frame counter.

5.3.3.7.1.3. Single Word Insert Capability

The single word insert capability was accomplished by adding circuits for selection of word time slot and word content. Switches S30 through S39 are positioned to select the word and frame time slot and are connected to true and inverted outputs of word and frame counter CSR's. Switch S40 provides enable/disable control of the single word insertion logic. Outputs from the Word/Frame select switches and the enable/disable switch are applied to a 13-input AND gate consisting of A55B, A55F, A55A, A63A, A63B and A59B. AND gate A59B also receives inhibit inputs from power inverter A63D during sync time slots and from the time code gating time slots. If the enable/disable switch is in the enable position and a valid time slot is selected, the 13-input AND gate is enabled during the selected time slot with a resultant output through power inverter A63C that strobes word content AND gates A30A through A30G. The word content AND gates are enabled or inhibited as selected by word content switches S41 and S47. The word thus constructed is strobed through the word content AND gates to the OR gates at the simulator data register input. The negative output of the 13-input AND gate also inhibits AND gate A55C to prevent loading other data during the single word insertion time slot.

5.3.3.7.1.4. Selectable Sync Word Capability

The selectable sync word capability was accomplished by adding circuits for selection of sync word. Switches S12 through S27 and associated gating logic provide this capability. Switches S12 through S15 are positioned to select the pattern for the first four bits of the frame sync word. Outputs from these switches enable or inhibit AND gates A38E, A38A, A38C and A34G that are strobed during word time 1 by the output from power inverter A63J. The resultant gated output bits are OR'ed by A38G, A38H, A42A and A42B and are routed through power inverters A63E, A63F, A63G and A63H to the OR gates at the simulator data register input.

Frame sync pattern bits 5 through 12 are constructed by switches S16 through S23. Outputs of these switches control AND gates A42G, A46A through A46F that are strobed during word time 2 by the output of power inverter A33F. The second portion of the frame sync word is routed from the AND gates to the OR gates of the Simulator data register input.

Bits 13 through 16 of the frame sync pattern are constructed by switches S24 through S27. These switches control AND gates A38F, A38D, A38B and A34H that are strobed during word time 3 by the output from AND gate A64B through power inverter A67H. The AND gate outputs are then OR'ed, inverted, and applied to the simulator data register input OR gates as described for frame sync pattern bits 1 through 4. Power inverter A93A output also strobes AND gates A47A through A47D to gate the four ID sync bits to the simulator data register input.

5.3.3.7.1.5. Time Code Inputs

The simulator data register input OR gates were further modified to accept four bits of time code data from the time code generator. These time code bits are received through pins AA, AE and Y of connector J108. The OR gates were expanded to four and five input gates by addition of 2 input NOR circuits A30H, A34A through A34F. The OR function was performed by connecting the outputs of the above circuits to the outputs of A65E, A64C through A64E, A65A, A65C and A65D.

The video amplifier card originally used (slot A78) was removed and a new, improved video amplifier card put in its place. The new card provides a better response time and waveshape appearance for the new split-phase type of signal. Also, a time code generator enable/inhibit switch was added to control the externally mounted time code generator from the simulator drawer. Switch S28 provides the signal through power inverter A63K. The output of A63K is routed to J108-a.

5.3.3.7.2. SYSTEMS 7 AND 8 SIMULATOR MODIFICATIONS (FIGURE 104)

5.3.3.7.2.1. Split-Phase Code Generation

Split-phase code signals are generated the same as in Systems 4 and 5.

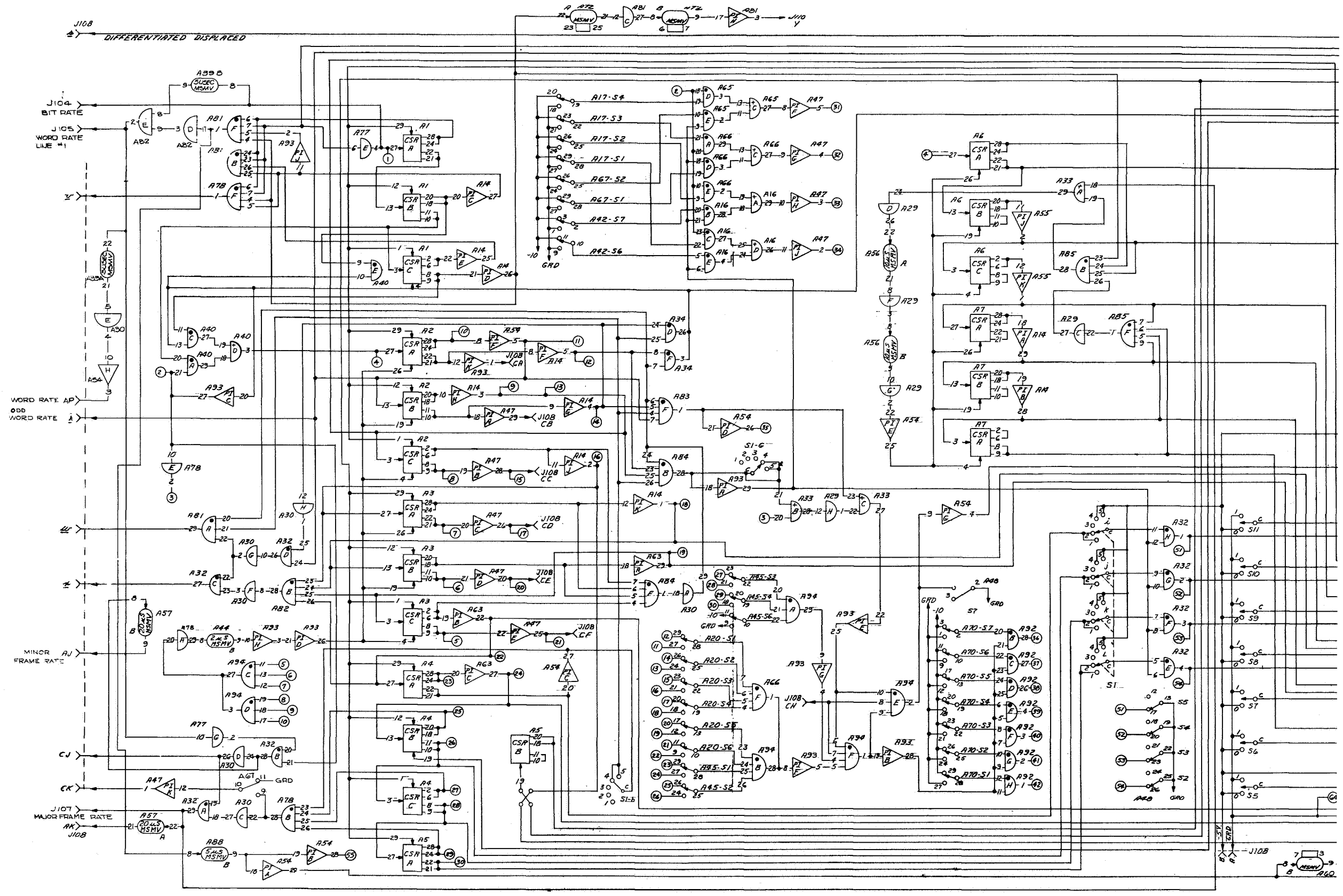
The NRZ output of the Simulator data shift register is routed through power inverter A55B to AND gate A69A that is enabled by every ZERO bit in the data signal. The BIT RATE signal from A77E is inverted through 2-NOR A34E and provides $\overline{\text{BIT RATE}}$ sample pulses to AND gate A69B. A69A receives $\overline{\text{BIT RATE}}$ from A64G. The applied NRZ ZERO bit enable and the $\overline{\text{BIT RATE}}$ sample signals to AND gate A69A result in a negative-going output that is coincident with the leading edge of each NRZ data bit. Each negative-going signal from AND gate A69A toggles CSR A19A that alternately enables AND gates A69B and A69C. AND gate A69B is sampled by the BIT RATE output of A34E and AND gate A69C is sampled by the BIT RATE output of gate A29F. The outputs of the AND gates are OR'ed by A69D and are routed to filter card A87. Since the CSR changes state with each ZERO bit to alternately enable gating of opposite phases of bit rate, the resultant OR'ed signal changes phase with each ZERO data bit to fulfill split-phase code requirements.

5.3.3.7.2.2. Bit and Word Counter

Simulator bit and word counters were modified such that the first word of each minor frame is limited to four bits and the remainder of the frame is limited to sixty-two 8-bit words. This results in a minor frame length of 62-1/2 words, as required by the Nimbus B format.

FOLDOUT FRAME

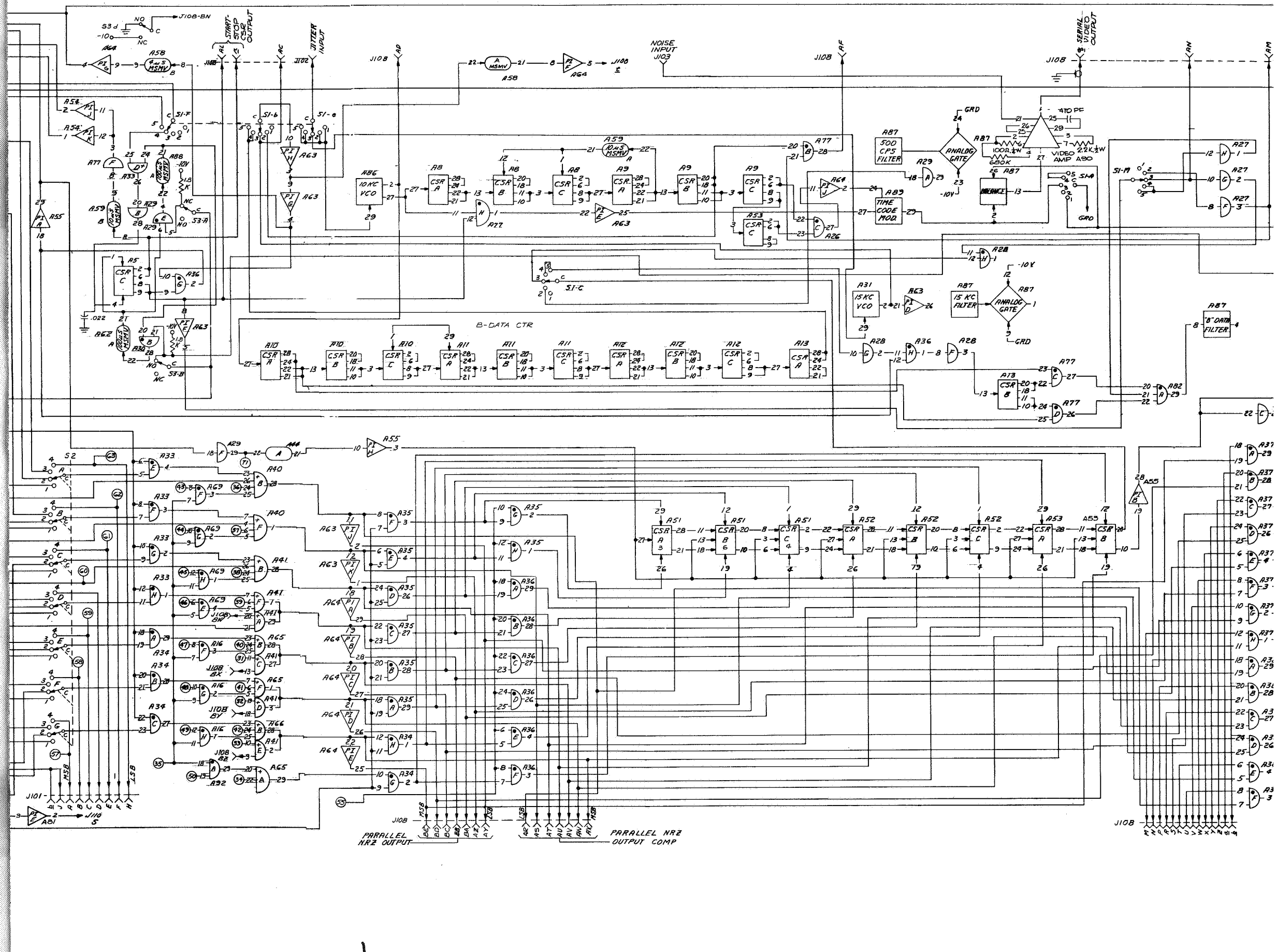
FOLDOUT FRAME



FOLDOUT FRAME 2

FOLDOUT FRAME 3

FOLDOUT FRAME



FOLDOUT FRAME 4

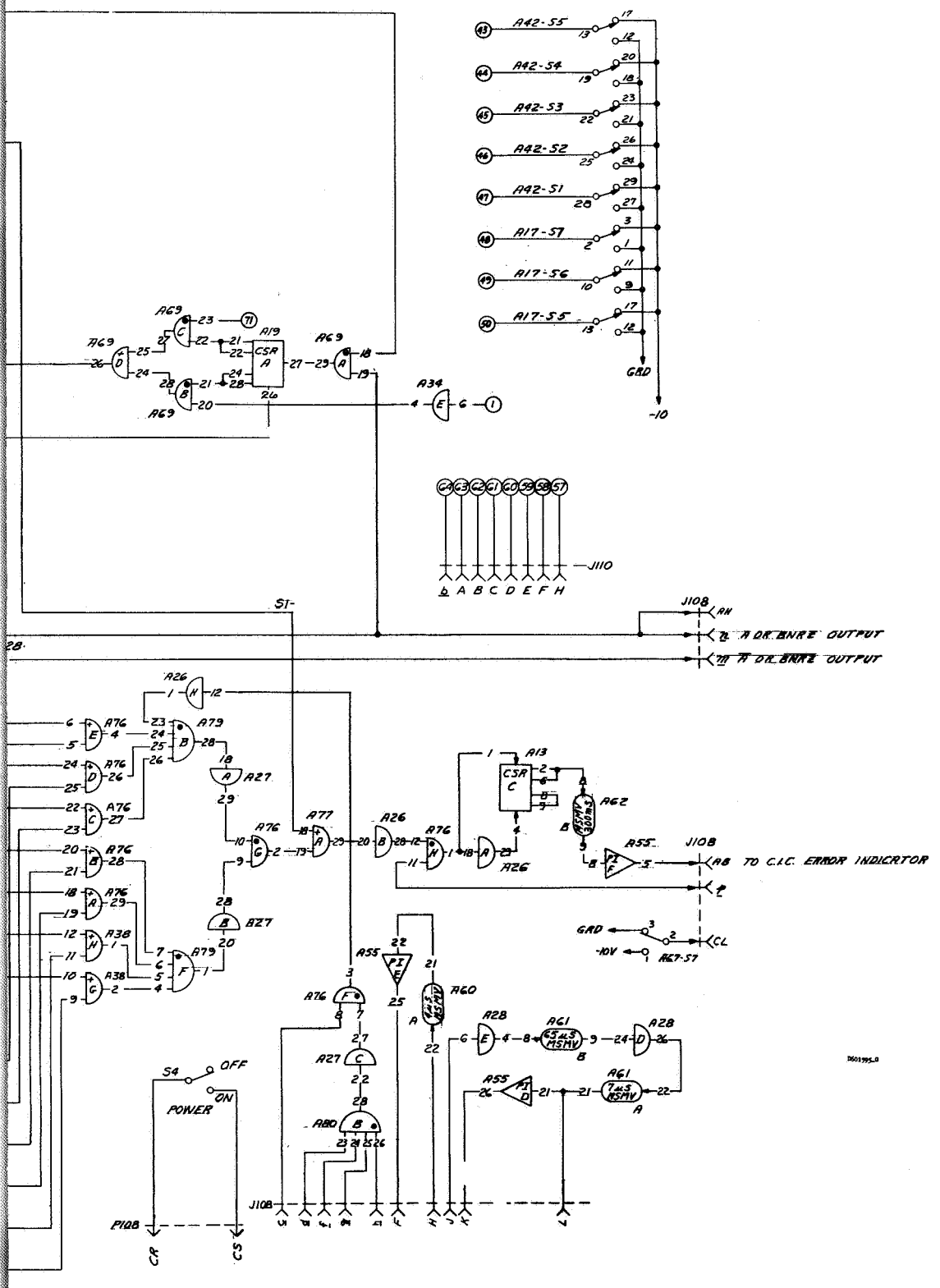


Figure 104. Simulator (Systems 7 and 8) Logic Diagram

Occurrence of the first word of each minor frame is detected by AND gates A34D and A34F and then routed to the reset side of A1(c). The operation of the bits per word counter is the same as in Systems 4 and 5.

Count 62 of the frame counter is detected by AND gates A94C and A94D that produce a negative output through A78A to monostable multivibrator A44B. At count 63, the trailing edge of the count 62 signal triggers monostable multivibrator A44B, and the resultant 2-microsecond output is routed through power inverters A93H and A93D to reset the frame counter.

5.3.3.7.2.3. Single Word Insert Capability

The single word insert capability was accomplished by adding circuits for selection of word time slot and word content. Switches A20-S1 through A20-S6 and A45-S1 through A45-S4 are positioned to select the word and frame time slot and are connected to true and inverted outputs of word and frame counter CSR's. Switch A45-S6 provides enable/disable control of the single word insertion logic. Outputs from the time code select switches and the enable/disable switch are applied to a 13-input AND gate consisting of A66F, A94B, A94A, A93F, A93G, and A94F. AND gate A94F also receives inhibit inputs from power inverter A93E during sync time slots and from the time code gating time slots. If the enable/disable switch is in the enable position and a valid time slot is selected, the 13-input AND gate is enabled during the selected time slot with a resultant output through power inverter A93B that strobes word content AND gates A92B through A92H. The word content AND gates are enabled or inhibited as selected by word content switches A70-S1 through A70-S7. The word thus constructed is strobed through the word content AND gates to the OR gates at the simulator data register input. The negative output of the 13-input AND gate also inhibits AND gate A94E to prevent loading other data during the single word insertion time slot.

5.3.3.7.2.4. Selectable Sync Word Capability

The selectable sync word capability was accomplished by adding circuits for selection of sync word. Switches on circuit cards A17, A42 and A67 and associated gating logic provide this capability. Switches A17-S1 through A17-S4 are positioned to select the pattern for the first four bits of the frame sync word. Outputs from these switches enable or inhibit AND gates A16C, A66E*, A66A, and A65D that are strobed during word time 1 by the output from AND gates A34D and A34F through power inverter A93C. The resultant gated output bits are OR'ed by A65C, A66C, A16A and A16D and are routed through power inverters A47F, A47G, A47H, and A47J to the OR gates at the simulator data register input.

Frame sync pattern bits 5 through 12 are constructed by switches A17-S5, A17-S7 and A42-S1 through A42-S6. Outputs of these switches control AND gates A92A, A16F through A16H and A69E through A69H that are strobed during word time 2 by the output from AND gate A83F through power inverter A54D. The second portion of the frame sync word is routed from the AND gates to the OR gates at the simulator data register input.

Bits 13 through 16 of the frame sync pattern are constructed by switches A42-S6, A42-S7, A67-S1 and A67-S2. These switches control AND gates A16E, A16B, A66D and A65E that are strobed during word time 3 by the output from AND gate A84B through power inverter A93A. The AND gate outputs are then OR'ed, inverted, and applied to the Simulator data register input OR gates as described for frame sync pattern bits 1 through 4. Power inverter A93A output also strobes AND gates A32E through A32H to gate the four ID sync bits to the simulator data register input.

5.3.3.7.5. TIME CODE INPUTS. The simulator data register input OR gates were further modified to accept four bits of time code data from the time code generator. These time code bits are received through pins BZ, BY, BX and BW of connector J108.

The OR gates were expanded to four- and five-input gates by addition of gates A41F, A41C through A41E. The OR function was performed the same way as in Systems 4 and 5.

The video amplifier card originally used (Slot A90), was removed and a new, improved video amplifier card put its place. The new card provides a better response time and waveshape appearance for the new split-phase type of signal.

Also, a time code generator enable/inhibit switch was added to control the externally mounted time code generator from the simulator drawer. Switch A67-S6 provides the signal through power inverter A47K. The output of A47K is routed to J108-CK.

There were other minor changes made in the simulator drawer for System 7 and 8 that were not because of the B-modification but only to bring the function configuration up to the state of the simulators in Systems 4 and 5. These changes are mentioned here but will not be described in detail. The modifications included the addition of a simulated sync confidence signal, the addition of a drawer connector J11C for external computer control of the data content of the simulated output signal, and the modification of timing signals generating word rate and minor frame rate pulses.

5.3.3.8. TIME CODE GENERATOR

The time code generator (figure 105) contains six binary-coded-decimal (BCD) up-counters that are advanced at a 1-pps rate to generate time code data comprised of units and tens of seconds, minutes, and hours.

The units of seconds up-counter is formed by CSR's A7A through A7C and A8A and is advanced at a 1-pps rate by the minor frame rate signal received through power inverter A16A. When the counter is advanced to count 10, AND gate A21D is enabled by the $\bar{8}$ output of the CSR A8A, the 2 output of CSR A7B (inverted through A15D), and the frame rate signal (inverted through A16B). The resultant negative output of AND gate A21D advances the tens of seconds counter and is applied through OR gate A6A and power inverter A16C to trigger differentiator A19A. The output of differentiator A19A resets the units of seconds counter to 0.

FOLDOUT FRAME 1

FOLDOUT FRAME 2

FOLDOUT FRAME

CONNECTOR DESIGNATIONS 5A2-TBI SHOWN IN PHANTOM OR PARENTHESIS ARE FOR SYSTEMS 4 AND 5. CONNECTOR DESIGNATIONS P108 NOT SHOWN IN PHANTOM OR PARENTHESIS ARE FOR SYSTEMS 8, 6, AND 7.

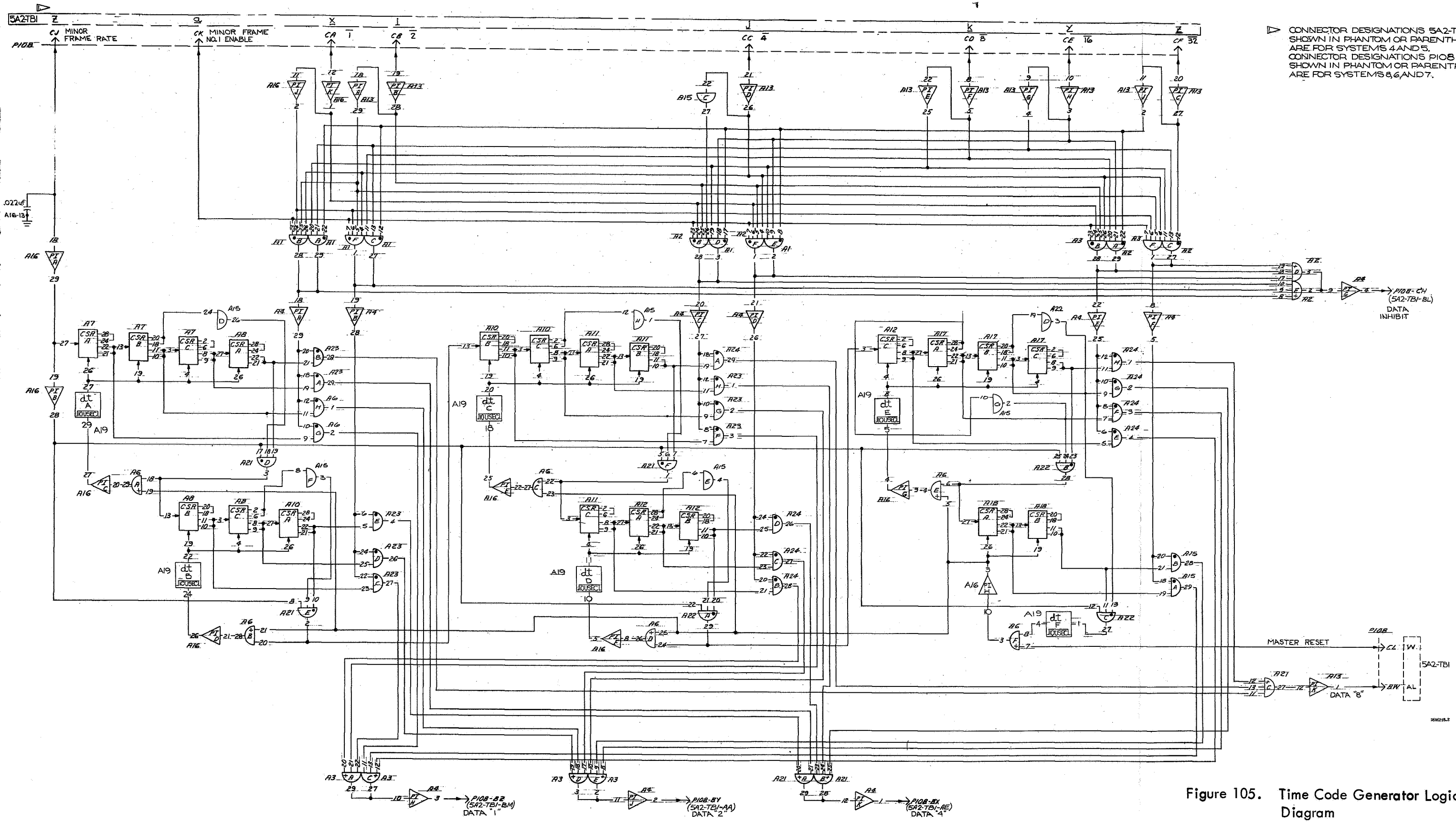


Figure 105. Time Code Generator Logic Diagram

Each count 10 output from the units of seconds up-counter causes the tens of seconds up-counter to advance as discussed above. The tens of seconds counter is a 6:1 counter and is comprised of CSR's A8B, A8C, and A10A. When the tens of seconds up-counter is advanced to count 6, AND gate A21E is advanced by the 4 output of CSR A10A, the 2 output of CSR A8C (inverted through A15F) and the inverted frame rate signal. The resultant negative output of AND gate A21E advances the units of minutes up-counter and is applied through OR gate A6B and power inverter A16D to trigger differentiator A19B. The output of differentiator A19B resets the tens of seconds up-counter to 0.

Operation of the units of minutes up-counter (CSR's A10B, A10C, A11A and A11B) and the tens of minutes up-counter (CSR's A11C, A12A, and A12B) is identical to the seconds up-counters described in the preceding paragraphs.

The units of hours up-counter (CSR's A12C and A17A through A17C) and the tens of hours up-counter (CSR's A18A and A18B) operate similarly to the counters described in the preceding paragraphs except that the hours count is reset at count 24. When the counter is advanced to count 24, AND gate A22C is enabled by the $\overline{2}$ output of CSR A18B, the 4 output of CSR A17B (inverted through A22D), and the inverted frame rate signal. The resultant negative output from AND gate A22C is applied through OR gate A6F and power inverter A16H to reset the tens of hours up-counter. The output of power inverter A16H is also applied through OR gate A16E and power inverter A16G to trigger differentiator A19E to reset the units of hours up-counter and through OR gates A6A through A6D to reset the seconds and minutes up-counters.

The FRAME GATE $\overline{1}$ signal from the Decommutator provides one enable input to each of the AND gates in the word gate matrix consisting of NOR circuits on A1, A2 and A3. These circuits also receive true and inverted WORD GATE 1, 2, 4, 8, 16, and 32 signals through power inverters A13A through A13K, A16J, and A16K and A26C. During word time 4 of each first frame, AND gates A1A and A1B are enabled by applied FRAME GATE $\overline{1}$ and WORD GATE 1, 2, 4, 8, 16 and 32 signals to develop an output through power inverter A4-A to strobe AND gates A23A, A23B, A6G and A6H. These gates receive the ZERO outputs of CSR's A7A through A7C and A8A and, when strobed, gate units of seconds data through OR gates A3A, A3C through A3E, and A21A through A21C and power inverters A4H, A4J, A4K, and A13K to the simulator data register.

During word time 13 of the first frame, AND gates A1C and A1F are enabled to develop an output through power inverter A4-B to strobe AND gates A23C through A23E to gate tens of seconds data to the simulator. During word time 22, the output of AND gates A2B and A1D strobes AND gates A23F through A23H and A24A through power inverter A4C to gate units of minutes data; during word time 24, the output of AND gates A2F and A1E strobes AND gates A24B, A24C and A24D through power inverter A4D to gate tens of minutes data; during word time 32, the output of AND gates A3B and A2A strobes AND gates A24E, A24F, A24G and A24H through power inverter A4E to gate units of hours data; and during word time 37, the output of AND gates A3F and A2C strobes AND gates A15A and A15B through power inverter A4F to gate tens of hours data.

Each word gate matrix output is OR'ed by A2D and A2E and is routed through power inverter A4G to inhibit normal simulator data loading during the word time slots. Provision is also made for a switch-controlled input through connector P108-CL to OR gate A6F to reset all Time Code Generator counters.

5.3.3.9. POWER SUPPLY. In Systems 7 and 8, the ±10V power supply used was a Mid-Eastern RDH-10-50. This provides the logic +10 volts and -10 volts with the following ratings:

+10 volts at 5 amperes
-10 volts at 50 amperes

Since the overall front panel height of the Mid-Eastern supply was smaller than the Sola supply, a 5.5-inch blank panel was added to Cabinet 3. More information on the power supply may be found in the Power Supply Instruction Manual.

5.3.3.10. EVENT RECORDER. Each system was provided with a single 60 channel event recorder. This unit was a Techni-rite TR-6360-357, deflection type, heat stylus, event recorder. The recorder is mounted on slides, completely self-contained, in its own 60-inch roll-around cabinet for accessibility.

In an inactive state (defined as a logic ZERO), the pens mark on the uncalibrated portion of the paper. In an active state (defined as a logic ONE), the pen deflects to the left and marks in the calibrated portion of the paper.

Channels No. 1 and 59 are serial time code traces. Channels 2 and 60 are time code marker traces. Channels 3-58 are the digital information channels.

5.3.3.11. ANALOG RECORDERS. The analog recorders (Brush - Mark 200) previously contained in the system were modified with the addition of a relay bracket assembly mounted in the rear of each recorder cabinet.

The time code and marker signals are routed from the time code display drawer, using relay drivers, into the relay bracket assembly. The contacts of each relay were used to activate the two event pens on the analog recorder. Each relay bracket contained two relays plus necessary input/output connectors.

SECTION VI

RELIABILITY

6.1. INTRODUCTION

The following paragraphs describe changes to the reliability assessment, failure effects analysis, and parts selection necessary to update the Nimbus Design Study report (Contract No. NAS-5-3787) to reflect the present Nimbus B configuration. Included in paragraph 6.6 is a complete failure history of the prototype and the flight models during qualification and acceptance tests.

Part application data sheets for every part within each subassembly are contained in Appendix I along with reliability calculation forms summarizing the failure rates for each subassembly GSFC malfunction.

6.2. RELIABILITY

A summary of the probability of success for each mode of operation for the Nimbus Design Study configuration and the Nimbus B configuration, including Government-Furnished Equipment (GFE) recorders and transmitters, is as follows:

Mode of Operation	Probability of Success	
	Design Study	Nimbus B
Record/Playback	0.8949	0.8200
Time Code Plus Real Time	0.8807	0.8069
Time Code Less Real Time	0.8885	0.8147
Time Code Bypass	0.8922	0.8174

All reliability calculations are based on a 6-month (4380-hour) mission time. The probability of success as a function of mission time is shown in figure 106 for the record/playback and time code plus real time modes. The remaining modes, time code less real time and time code bypass, are not shown because the graphical presentation would become overly complicated due to closeness of the curves.

6.3. SUBSYSTEM RELIABILITY NUMERICAL ASSESSMENT

6.3.1. RELIABILITY MATHEMATICS

The following paragraphs present mathematical techniques which, when used to form the mathematical model of the subsystem, best reflect the electrical configuration of the equipment. The diagrams graphically and numerically display the probability of success for each function performed by the equipment and are not intended to show signal flow.

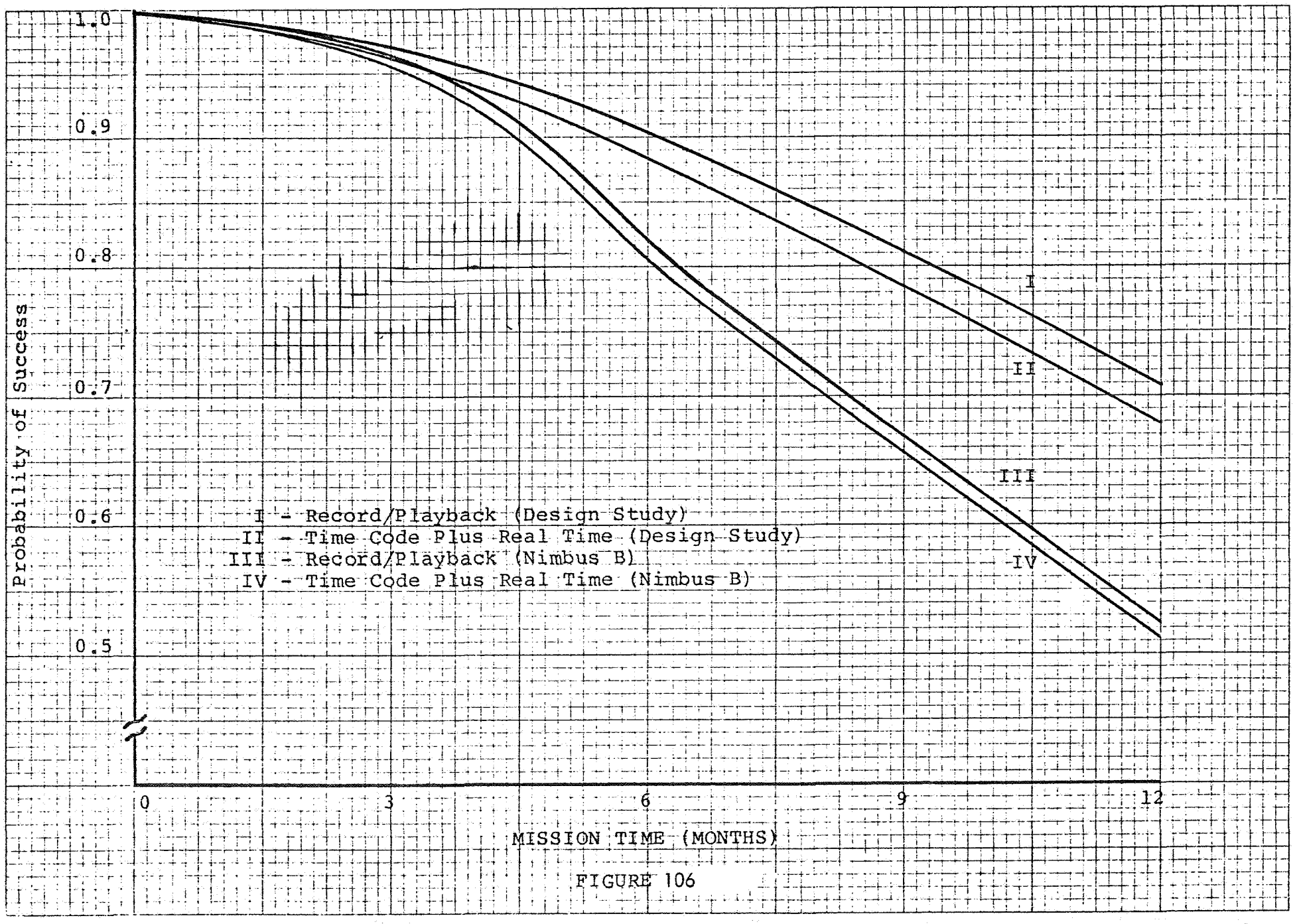

1.0
0.9
0.8
0.7
0.6
0.5
Probability of Success
I
II
III
IV
I - Record/Playback (Design Study)
II - Time Code Plus Real Time (Design Study)
III - Record/Playback (Nimbus B)
IV - Time Code Plus Real Time (Nimbus B)
0
3
6
9
12
MISSION TIME (MONTHS)

FIGURE 106

6.3.1.1. NONREDUNDANT COMPONENTS

The mechanism underlying the exponential reliability function of nonredundant components is that of random or chance failures that are independent of accumulated life and are individually unpredictable. This type of "failure law" for complex systems is used because different part failure rates, varying deterioration mechanisms, varying environmental conditions, etc., result in stress-strength combinations that produce failures randomly in time.

Exponential and Poisson distributions are equivalent except for the choice of the random variable. For the exponential, the random variable is the time-to-failure; for the Poisson, the random variable is the number of failures per given time period when failure times are exponentially distributed.

The exponential reliability expression is derived from the Poisson distribution as the probability of zero failures in the interval [0,t].

$$R = e^{-\lambda t}$$

where R = reliability or probability of success

λ = failure rate

t = mission time

6.3.1.2. REDUNDANT COMPONENTS

The expression used to represent the probability of successful operation for redundant components, whereby the active component fails at some time (t_1) and the standby component is switched into operation for the remaining mission time, is derived as follows:

Success can be achieved in the following ways:

a. Components A and B succeed to time t (mission duration).

b. Component A fails at time t_1, less than t, and component B must operate to time t. (The switch must work at time t_1.)

c. Component A succeeds to time t and the standby component B fails.

Translating the preceding three conditions of success into time independent probabilities:

$$R_{(t)} = \epsilon^{-\lambda_A t} + \lambda_A \epsilon^{-\lambda_B t} \int_0^t \epsilon^{-(\lambda_A + \lambda_S)t_1} dt_1$$

where λ_A = failure rate of the initially active component

λ_B = failure rate of the standby component

λ_S = failure rate of the switch

Solution of the above equation yields:

$$R_{(t)} = \epsilon^{-\lambda_A t} + \frac{\lambda_A}{\lambda_A + \lambda_S} \epsilon^{-\lambda_B t} \left[1 - \epsilon^{-(\lambda_A + \lambda_S) t}\right]$$

When redundant components A and B have the same failure rate, this equation reduces to:

$$R_{(t)} = \epsilon^{-\lambda_A t} \left[1 + \frac{\lambda_A}{\lambda_A + \lambda_S} \left(1 - \epsilon^{-(\lambda_A + \lambda_S)t}\right)\right]$$

6.3.1.3. ALLOWABLE CHANNEL LOSS

The allowable loss of eight analog and seven digital inputs has been introduced to define mission success. With this definition of success, the binomial distribution is applicable. However, when the number of channels is large and single channel failure probability is small, the Poisson distribution is a close approximation to the binomial. The reliability expression becomes:

$$R = \sum_{r=0}^{X} \frac{a^r \epsilon^{-a}}{r!}$$

where R = reliability

$a = \lambda t$

λ = total failure rate

t = mission time

X = number of allowable failures

Where circuit configuration is such that a single failure will cause maximum allowable data loss for mission success, the expression above reduces to:

$$R = \epsilon^{-\lambda t} (1 + \lambda t)$$

6.3.2. PCM BLOCK ANALYSIS

The reliability of the PCM subsystem has decreased as a result of noise immunity modifications incorporated in the coder and multiplexer circuits. Figure 107 is a reliability diagram that shows the Nimbus B PCM subsystem divided into nonredundant input circuits and redundant blocks. The following paragraphs discuss differences in reliability of the Nimbus B PCM circuitry compared with the Design Study PCM circuitry.

6.3.2.1. NONREDUNDANT INPUT CIRCUITS

The PCM subsystem is a block-redundant configuration except for the multiplexer submatrix input gates. The reliability has decreased for both analog and digital input circuitry as shown by the following comparison:

	Reliability	
	Design Study	Nimbus B
Digital Data (R_{DD})	0.9951	0.9872
Analog Data (R_{AD})	0.9654	0.9328
Total ($P_1 = R_{DD}R_{AD}$)	0.9607	0.9209

where:

R_{DD} = reliability of digital input gates with one allowable failure.

R_{AD} = reliability of analog input gates with one allowable failure.

A major cause of the decrease in reliability of multiplexer input circuits is the addition of metal film resistors required to remove MOSFET switching transients.

6.3.2.2. REDUNDANT BLOCK

The reliability has decreased for PCM redundant circuits. These circuits are divided into subsections as shown below with a comparison of the Design Study and Nimbus B reliability estimates.

	Reliability	
	Design Study	Nimbus B
Multiplexer (R_M)	0.8772	0.7997
Programmer (R_P)	0.9429	0.9439
A/D Converter (R_C)	0.9413	0.9310

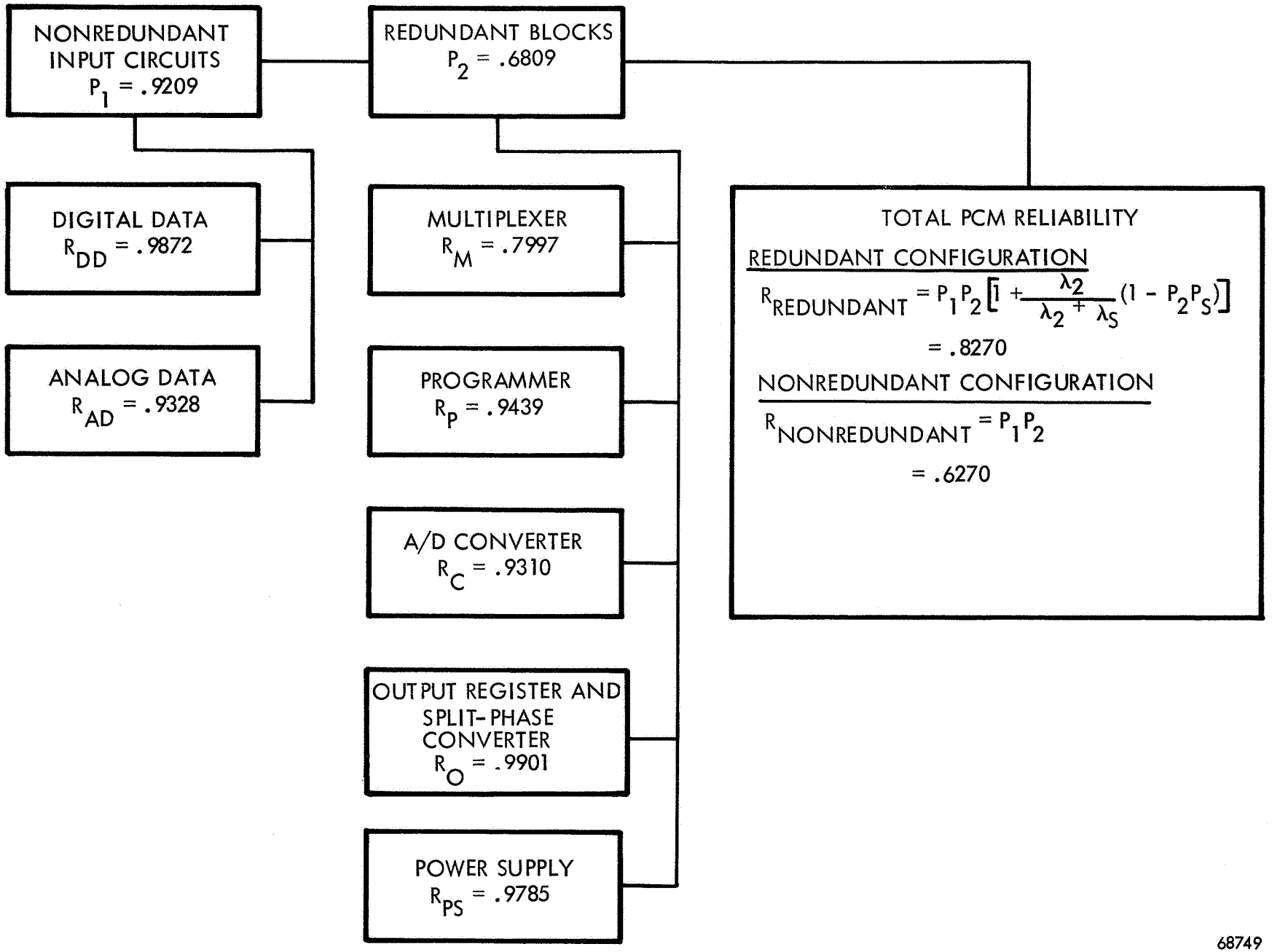


Figure 107. Nimbus B Subsystem Reliability Diagram

	Reliability	
	Design Study	Nimbus B
Output Register & Split Phase Converter (R_O)	0.9901	0.9901
Power Supply (R_{PS})	0.9760	0.9785
Total ($P_2 = R_M R_P R_C R_O R_{PS}$)	0.7523	0.6809

where:

R_M = reliability of redundant multiplexer circuits

R_P = reliability of programmer

R_C = reliability of A/D Converter

R_O = reliability of output register and split phase converter

R_{PS} = reliability of power supply

Additional circuitry in the coder and multiplexer to increase noise immunity have resulted in decreased reliability of the PCM redundant block.

6.3.2.3. TOTAL PCM RELIABILITY

The reliability of the PCM subsystem has decreased from 0.9026 to 0.8270 as a result of design changes.

The mathematical model for the complete PCM subsystem is as follows:

$$R = \epsilon^{-\lambda_1 t}\left\{\epsilon^{-\lambda_2 t}\left[1+\frac{\lambda_2}{\lambda_2+\lambda_S}\left(1-\epsilon^{-(\lambda_2+\lambda_S)t}\right)\right]\right\}$$

$$= P_1 P_2\left[1+\frac{\lambda_2}{\lambda_2+\lambda_S}(1-P_2P_S)\right]$$

where $P_1 = \epsilon^{-\lambda_1 t}$ = probability of success of multiplexer input circuits with allowable losses

$P_2 = \epsilon^{-\lambda_2 t}$ = probability of success of redundant circuitry

$P_S = \epsilon^{-\lambda_S t}$ = probability of success of switching circuitry

PCM subsystem reliability, in a nonredundant configuration, is shown in the following mathematical model for comparative purposes.

	Reliability	
	Design Study	Nimbus B
$R = P_1 P_2$	0.7235	0.6270

6.3.3. TME BLOCK ANALYSIS

For analysis purposes, the TME subsystem is divided into four modes of operation, the redundant record/playback blocks and the nonredundant real time and time code circuitry (figure 108). The GFE tape recorders and transmitters that interface with the TME are included in the analysis. There has been no significant changes in the TME reliability estimates resulting from minor design changes as described in paragraph 6.5.2.

6.3.3.1. COMMON EQUIPMENT ($P_{CE} = .9977$). The following equipment is common to all modes of operation:

a. Summing Amplifier ($P_{SA} = .9953$)

b. Transmitter ($P_T = .9527$)

The mathematical model for these redundant blocks is as follows:

$$P_{CE} = \{P_{SA}\ [1 + \frac{\lambda_{SA}}{\lambda_{SA} + \lambda_{S2}}\ (1 - P_{SA}P_{S2})]\}\ \{P_T\ [1 + \frac{\lambda_T}{\lambda_T + \lambda_{S3}}\ (1 - P_T P_{S3})]\}$$

where P_{SA} = probability of success of summing amplifier

P_T = probability of success of transmitter

P_{S2} = probability of success of switching circuitry for the summing amplifier

P_{S3} = probability of success of switching circuitry for the transmitter

6.3.3.2. RECORD/PLAYBACK ($R_{R/P} = .9915$). The mathematical model for the record/playback mode of operation is as follows:

$$R_{R/P} = P_{CE}\ \{P_{R/P}\ [1 + \frac{\lambda_{R/P}}{\lambda_{R/P} + \lambda_{S1}}\ (1 - P_{R/P}P_{S1})]\}$$

where P_{CE} = probability of success of common equipment (summing amplifiers, transmitters, and associated switching circuits)

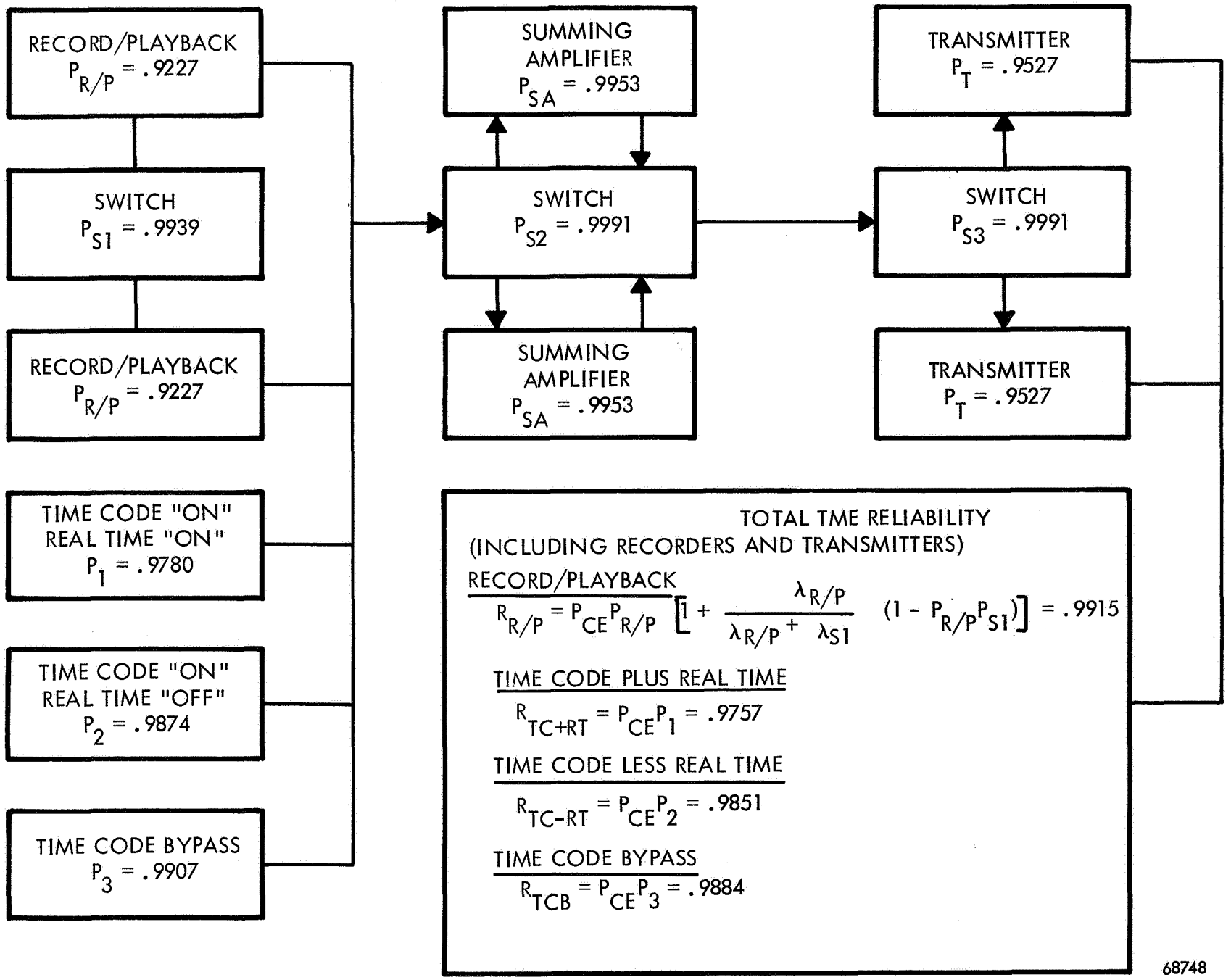


Figure 108. Time Subsystem Reliability Diagram

$P_{R/P}$ = probability of success of recorder, record amplifier, and playback amplifier

P_{S1} = probability of success of record/playback switching circuits

6.3.3.3. TIME CODE "ON", REAL-TIME "ON"

(R_{TC+RT} = .9757)

Nonredundant, internal TME components required for this mode of operation are:

Component	N	$N\lambda \times 10^{-5}$
Relay	4	0.080
Resistor, Variable WW	2	0.266
Resistor, Metal Film	4	0.088
Capacitor, Tantalum	2	0.074
Total Failure Rate		0.508

$P_1 = e^{-N\lambda t} = .9780$

The mathematical model for time code plus real-time mode of operation is as follows:

$R_{TC+RT} = P_1 P_{CE}$

where P_1 = probability of success of TME nonredundant circuitry

P_{CE} = probability of success of common equipment

6.3.3.4. TIME CODE "ON", REAL-TIME "OFF"

(R_{TC-RT} = .9851)

Nonredundant, internal TME components required for this mode of operation are:

Component	N	$N\lambda \times 10^{-5}$
Relay	3	0.060
Resistor, Variable WW	1	0.133

Component	N	$N\lambda \times 10^{-5}$
Resistor, Metal Film	1	0.022
Capacitor, Tantalum	2	0.074
Total Failure Rate		0.289

$P_2 = e^{-N\lambda t} = .9874$

The mathematical model for time code less real-time mode of operation is as follows:

$$R_{TC-RT} = P_2 P_{CE}$$

where P_2 = probability of success of TME nonredundant circuitry

P_{CE} = probability of success of common equipment

6.3.3.5. TIME CODE BYPASS

($R_{TCB} = .9884$)

Nonredundant, internal TME components required for this mode of operation are:

Component	N	$N\lambda \times 11^{-5}$
Relay	1	0.020
Resistor, Variable WW	1	0.133
Resistor, Metal Film	1	0.022
Capacitor, Tantalum	1	0.037
Total Failure Rate		0.212

$P_3 = e^{-N\lambda t} = .9907$

The mathematical model for time code bypass mode of operation is as follows:

$$R_{TCB} = P_3 P_{CE}$$

where P_3 = probability of success of TME nonredundant circuitry

P_{CE} = probability of success of common equipment

6.3.4. TOTAL SYSTEM RELIABILITY

A summary of the reliability calculations discussed in the preceding paragraphs is as follows:

$R_{PCM} = .8270$

$R_{R/P} = .9915$

$R_{TC+RT} = .9757$

$R_{TC-RT} = .9851$

$R_{TCB} = .9884$

Total system reliability is calculated for each mode of operation as follows:

$R_{EQUIPMENT} = R_{R/P}R_{PCM} = .8200$ Record/Playback

$= R_{TC+RT}R_{PCM} = .8069$ Time Code Plus Real-Time

$= R_{TC-RT}R_{PCM} = .8147$ Time Code Less Real-Time

$= R_{TCB}R_{PCM} = .8174$ Time Code Bypass

Monitor circuits are considered nonessential to mission success and are not included in the above equipment reliability calculations.

6.3.5. MONITOR CIRCUITS

Reliability of the components used to monitor environmental conditions within the equipment is listed below:

Component	N	$N\lambda \times 10^{-5}$
Monitor Module	1	0.082
Thermistors	2	0.060
Diode	2	0.002
Resistor, MF	2	0.044
Resistor, Carbon Comp.	3	0.003
Total Failure Rate		0.191

$R_{MONITOR} = e^{N\lambda t} = 0.9916$

6.4. FAILURE RATE CONSIDERATIONS

Failure rates for discrete components were selected at appropriate stress levels from MIL-HDBK-217. Failure rates for semiconductor devices were improved by a factor of 10:1 to reflect improvements realized from power ageing. This improvement factor is based on data obtained from GSFC Document X-650-65-105, "A Comparison of Burn-In and Bake as Semiconductor Screening Techniques For the Nimbus Spacecraft Program," dated March, 1965.

Failure rates for multiplexer components were obtained from the latest manufacturer-supplied testing information, as follows:

a. MOSFET 0.03%/1000 hours

b. Integrated Devices 0.016%/1000 hours

c. Custom Device (GPA) 0.04%/1000 hours

Failure rates for record/playback and erase heads were not included in MIL-HDBK-217 and were obtained from "Failure Rate Data Handbook (FARADA)," dated 1 March 1965, that was supplied by the Bureau of Naval Weapons.

6.5. FAILURE EFFECTS ANALYSIS

The addendum to Final Report for Contract No. NAS-5-3787 contained a complete failure effects analysis for the Nimbus Study PCM subsystem, presented on a circuit function level for the PCM and by mode of operation for the TME. Subsequent design modifications for the Nimbus B configuration require changes to this analysis as presented in the following paragraphs.

6.5.1. PCM ANALYSIS

Modifications have been incorporated in the PCM to improve noise immunity in the coder and multiplexer circuits. The failure effects analysis requires no change as a result of these product improvement modifications.

6.5.2. TME ANALYSIS

The TME Relay Switching Diagram has been revised to reflect a few minor changes made to the design study configuration. Figure 108 shows the electronic components and relays required, as well as the state of the relay contacts, for each mode of operation of the Nimbus "B" TME configuration. Table 15 lists the circuitry in figure 109 under subsystem No. 1 and the associated complementary circuitry for the redundant path under subsystem No. 2. The following paragraphs describe part changes within the TME and the associated failure mode and effects analysis.

Table 15. TME Electronic Components and Relays

	Subsystem No. 1	Subsystem No. 2
Relays	K1 K2 K3 K4 K5 K7 K8 K9 K16 K17 K19	K1 K10 K11 K12 K13 K15 K8 K9 K16 K18 K19
Resistors	R1 through R5 R6, R10 R7, R11 A2R1 through A2R3 A2R4	R1 through R5 R8, R12 R9, R13 A2R1 through A2R3 A2R5
Amplifiers	Record No. 1 Playback No. 1 Summing No. 1	Record No. 2 Playback No. 2 Summing No. 2
Recorders	Recorder No. 1	Recorder No. 2
Transmitters	Transmitter No. 1	Transmitter No. 2

Addition of the "PCM Emergency Power On" command required one relay (K19) and ten protective diodes (CR81-CR90). The diodes are redundant so that open or short mode failures will not effect operation of relay K19. A failure in relay K19 (coil or contacts) will result in loss of ability to provide emergency power to the PCM should Nimbus prime power be lost.

The gain adjust potentiometers (A2R4 and A2R5), added to the playback amplifiers, will cause an increased gain for short mode failures and a decreased gain for open mode failures.

Interlocking relays K6 and K14 have been removed. These relays prevented simultaneous operation of the two recorders in playback mode. It is now possible for the ground station to command both recorders to playback at the same time, which will result in scrambled data.

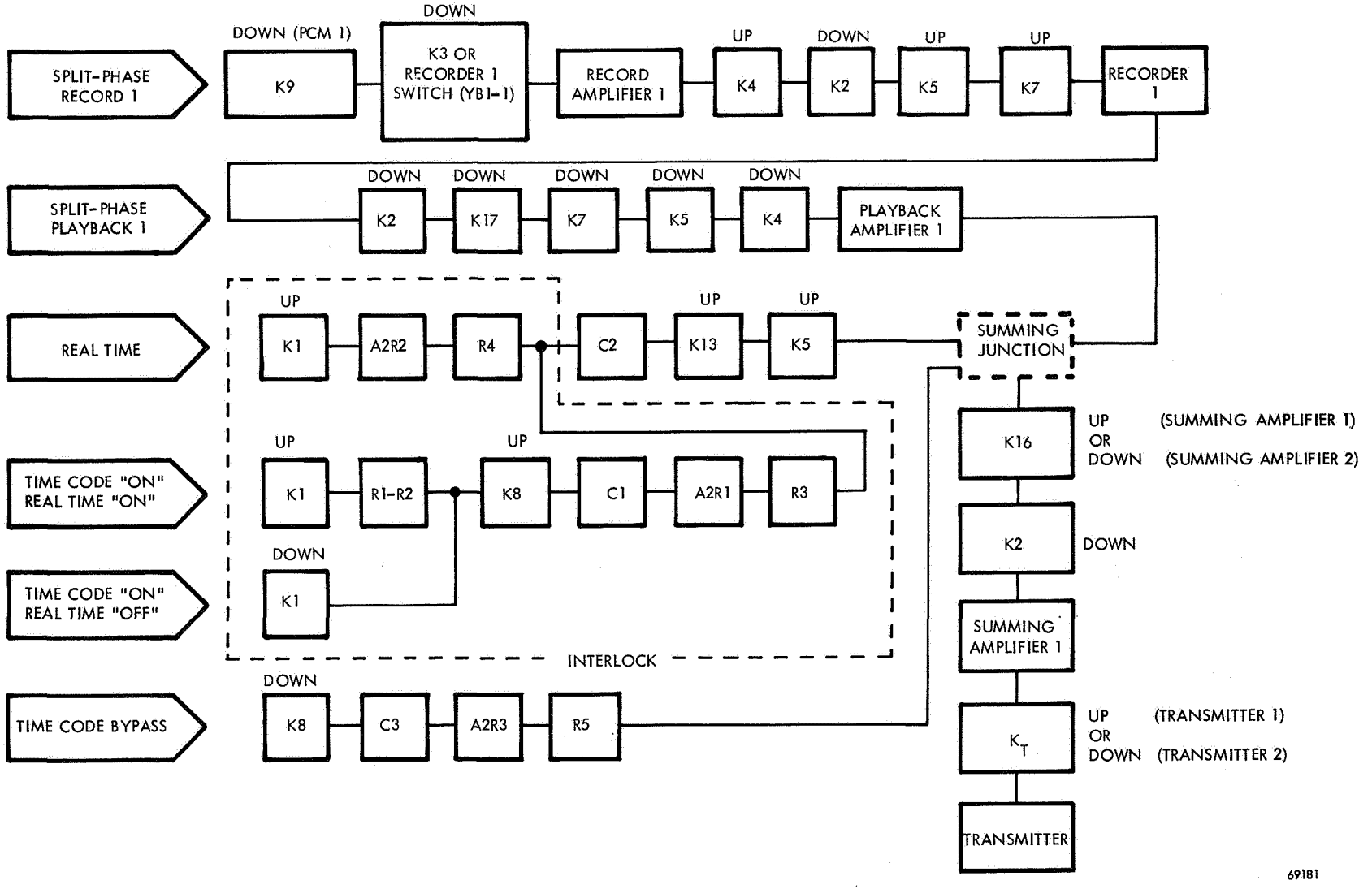


Figure 109. TME Detailed Reliability Diagram

6.6. PARTS SELECTION AND VENDOR EVALUATION

6.6.1. MOSFET, 5 CHANNEL MULTIPLEXER

MOSFET's presented two major problem areas. These areas can be considered as handling procedures and supply source.

MOSFET's are extremely susceptible to damage caused by static charge. Static charge generated by friction in handling is sufficient to destroy a unit. To prevent this type of damage, a handling procedure was generated (Radiation Drawing 110174, Handling and Shipping Flatpack and MOSFET devices) that outlined all special requirements for the vendor and for Radiation personnel.

The major supplier, Fairchild Semiconductor, was unable to adequately protect the units during handling and therefore had a high destruction rate. The excessive fall-out seriously threatened the production schedule, thus necessitating a search for a second source. It has been further determined that FSC flatpacks have a poor internal design. The mounting of the chip to the header and the subsequent wire bonding and routing creates a potential problem of inadvertent shorting.

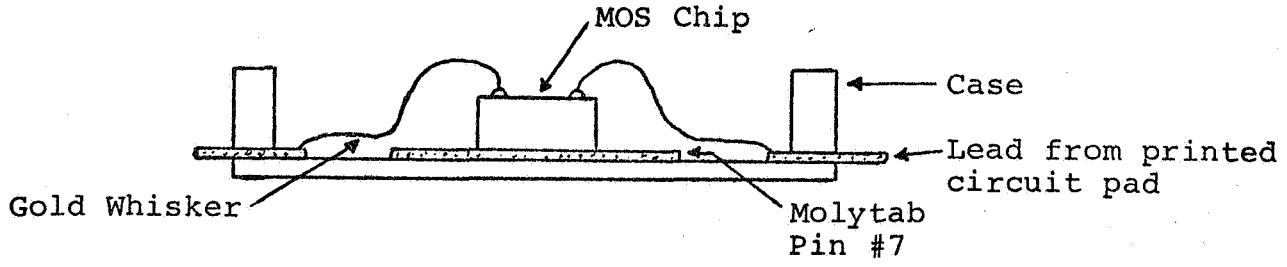


figure 110

In fabricating this part, gold whiskers are bonded to the chip, then to the bonding pad (see figure 110). After making the chip bond, the gold lead must be drawn upward, across, then down below the chip surface to the printed circuit pad. The printed circuit pad is on the same level with the molytab, thus proper fabrication relies heavily on operator dexterity to keep the gold lead from being able to short to an adjacent lead or the molytab.

The problems with Fairchild P/N 106510 MOS flatpacks are complicated by the difficulty of determining those which are poorly made, after the part is complete. Normal radiographs will not clearly show how close the gold leads are to the molytab. Therefore, with only the potential lead to lead shorts being found a part cannot be considered reliable.

This, in addition to the above, led to the discontinuation of FSC as a supplied for MOSFET flatpacks.

General Instrument Corporation (G.I.) of Hicksville, L.I., indicated promise as a potential supplier because of development work on a 5-channel MOSFET. Negotiations were inaugurated to develop a circuit that would be interchangeable with the Fairchild circuit. General Instrument's plant, production procedures, and quality control procedures were surveyed and found to be inadequate for production of aerospace components. Radiation and G.I. personnel met on several occasions to revamp production and quality control procedures so that fabrication of the circuits could begin. General Instrument Corporation (G.I.) is now the source of supply for this item, as was discussed in the "Addendum to final report for Nimbus Design Study".

The Fairchild MOSFET's on the flight models were replaced with General Instrument MOSFET's. It was not considered necessary to replace the Fairchild devices in the prototype model, however, and as a result this model contains approximately equal quantities of Fairchild and G.I. devices.

Problems with General Instrument MOSFET devices started during acceptance testing of the Flight 1 system. Analysis by both Radiation and General Instrument revealed three possible problems:

a. Contamination by foreign particles

b. Pin holes in the oxide

c. Seal problem

During a briefing at NASA/GSFC it was pointed out that particle contamination was the most probable cause of the system failures since the failures occurred only during system vibration. The participants at the briefing were informed that x-ray was not an effective screen for particle contamination and that a possible problem existed in the sealing of the G.I. MOSFET devices since an excessive number of gross leakers had been detected during random sampling.

The particle contamination and seal problems were investigated at General Instrument. Evidence gathered during the investigation indicated a process, process control, procedure, quality control or inspection inadequacy at General Instrument. Corrective action was undertaken and more stringent process controls and inspections were instituted. In addition to the corrective action, G.I. recommended that the MOSFET's presently used in the Nimbus program be replaced with a pyrolytic oxide construction (glass overlay) device which would protect against all particles except those large enough to short between bonding pads or wires (3 mils). Radiation concurred with this recommendation and, with NASA approval, all of the nonpyrolytic MOSFET's in flight systems 1 and 2 were replaced with the pyrolytic devices. Qualification tests of the pyrolytic devices are in process and the results will be contained in a subsequent report.

Further investigations revealed that some of the particles were present in the materials used to manufacture the packages or were introduced during the manufacturing process. That corrective action taken at General Instrument (pyrolytic oxide and package inspection and cleaning) has been successful is shown by the device qualification and system test results. It is, therefore, deduced that the particle contamination was the cause of system failure.

6.6.2 DUAL DTL NAND GATE

Problems with the Westinghouse WM261G device started during qualification tests of the prototype system. The problem was a Westinghouse manufacturing defect which shorts the base to ground and clamps V_{ce} to V_{cc}. Westinghouse confirmed the problem with their own analysis which concluded that the diode wire was diffused too deeply and resulted in a temperature sensitive leakage path to substrate. A method of screening was developed by Westinghouse. One volt is applied to pin 7 with pin 14 grounded and all other pins open. Current should read 10 microamperes or less. This method proved to be effective and all WM261G devices from both flight systems were removed from the cards and screened.

6.7 MALFUNCTION HISTORY

The following paragraphs describe the malfunction history for the prototype, flight 1 and flight 2 systems. GSFC malfunction reports are contained in Appendix II.

6.7.1 MALFUNCTION HISTORY SUMMARY - PROTOTYPE SYSTEM

A total of seventeen system level failures were reported during qualification testing of the prototype model. These failures involved seven Fairchild MOSFET's, five General Instrument MOSFET's, three Westinghouse dual-NAND gate flatpacks, one Texas Instruments 2N2412 transistor, and one failure due to workmanship. Table 16 lists the failures which occurred during Qualification Tests.

6.7.1.1 SYSTEM FAILURES DURING QUALIFICATION TESTING

6.7.1.1.1 ITEMS 1 AND 2

These devices (Failchild MOSFET's) failed during random longitudinal vibration. Since the Fairchild MOSFET's were no longer being qualified for flight systems, no analyses were performed on the failed devices and General Instrument MOSFET's were used as replacements.

6.7.1.1.2 ITEMS 3, 4 AND 5. Prime digital channels (words 64-6, 62-13, 65-30, 61-45, and 52-63) were intermittent during longitudinal random vibration then became stable after vibration and remained stable throughout the remaining tests. An analysis of the circuits associated with the intermittent channels revealed three MOSFET's which could have been responsible for the intermittent operation.

Analysis performed on item 3 by the Diagnostic Lab gave no failure indications and the MOSFET was considered to be a good device.

Electrical tests revealed that item 4 was shorted. However, since the system failure was intermittent and could not be explained by a shorted condition, it can be assumed that the device was damaged after system test.

Table 16. Failure Report Summary Nimbus B Prototype System

Item	GSFC F.R.	Rad. F.R.	Date	Module/Card	P/N	S/N	Ckt. #	P/N	Manufacturer
1	11004	01786	3/27/67	Prime Matrix	516492	0001	A15	106510	Fairchild
2	11016	01901	4/5/67	Submatrix A4	516530G4	0001	A1	106510	Fairchild
3	11005	01902	4/5/67	Output Bd. 2A	516465G1	0001	A13	110245	G.I.
4	11017	01903	4/5/67	Output Bd. 2B	516465G2	0001	A13	110245	G.I.
5	11018	01904	4/5/67	Prime Matrix	516492	0001	A38	106510	Fairchild
6	11006	01783	3/27/67	Submatrix B3	516531G3	0001	A50	106510	Fairchild
7	11003	01790	3/27/67	Submatrix B2	516531G2	0001	A48	106510	Fairchild
8	11007	01784	3/27/67	Prime Matrix	516492	0001	A19	110245	G.I.
9	11008	01785	3/27/67	Prime Matrix	516492	0001	A20	110245	G.I.
10	11009	01787	3/27/67	Output Bd. 1A	516467G1	0001	A57	110426	Westinghouse
11	11012	01792	3/27/67	Output Bd. 1A	516467G1	0001	A31	110426	Westinghouse
12	11013	01791	3/27/67	Output Bd. 1A	516467G1	0001	A63	110426	Westinghouse
13	11010	01788	3/27/67	Prime Matrix	516492	0001	A17	106510	Fairchild
14	11011	01789	3/27/67	Prime Matrix	516492	0001	A18	106510	Fairchild
15	11014	01793	3/27/67	Prime Matrix	516492	0001	A10	110245	G.I.
16	11015	01794	3/27/67	Programmer 3	515604	0002	A41	102618	T.I.
17	11019	01905	4/21/67	Output Bd. 1A	516467G1	0001	N/A	N/A	N/A

Source 5 was found to be open in item 5. Decasing and visually examining the device revealed the gold bond (aluminum metallization interface) was black. The bond at pin 5 was probed and found open, but intermittent contact was indicated. An Au-Al formation around the bonds of pins 9 and 10 apparently caused the device to operate intermittently. A G. I. MOSFET was used as a replacement for item 5 (Fairchild MOSFET).

6.7.1.1.3 ITEM 6. Subcommutated channels of subframe 12, words 1/16A-301, 305, 311, 315, 319, and 323 were lost during longitudinal vibration. The problem was corrected by replacing item 6 (Fairchild MOSFET) with a G. I. MOSFET.

6.7.1.1.4 ITEM 7. Subcommutated analog channel subframe 14, word 14 read high during temperature tests. Item 7 (Fairchild MOSFET) was replaced with a G. I. MOSFET.

6.7.1.1.5 ITEMS 8 AND 9. Prime analog channels 1A3, 1A7, 1A13, 1A15, and 1A19 were lost during electrical test at room ambient. Analysis of item 8 revealed surface contamination, external to the device. The failure was considered to be of a random nature. Item 9 was electrically tested and the reported failure mode could not be verified. There was no evidence that the device was defective.

6.7.1.1.6 ITEMS 10, 11 AND 12. These items (dual DTL NAND gates) failed during temperature testing. Analysis conducted by the Diagnostic Lab indicated a manufacturing defect which resulted in heat sensitivity and excessive leakage current through the reversed bias diode of the substrate. Westinghouse confirmed the problem and proposed a method of screening the devices. One volt is applied to pin 7 with pin 14 grounded and all other pins open. The current should be 10ua or less. This method proved to be effective and was used to screen all the Westinghouse flatpacks on the flight systems.

6.7.1.1.7 ITEMS 13, 14 AND 15. Leads on these items were weakened during electrical testing and troubleshooting of the system. The damaged parts were replaced with new devices.

6.7.1.1.8 ITEM 16. The Texas Instrument 2N2412 transistor was suspected of having a collector to emitter short that caused the loss of BTE Command on PCM 2. The defective part was lost during module rework and therefore no analysis of the part could be obtained. However, no other failures of this device occurred on the Nimbus B program and it is felt that no significant information was lost.

6.7.1.1.9 ITEM 17. PCM data was lost during the thermal vacuum test. A solder short was found in Output Board 1A between pins 3 and 4 of A44. The failure was attributed to a fabrication error.

6.7.2 MALFUNCTION HISTORY SUMMARY - FLIGHT SYSTEM 1

Fifteen system level failures were reported during qualification testing of flight system 1. These failures are listed in table 17 and include nine General Instrument MOSFET's, four Westinghouse dual NAND gates, one Sprague NPN driver, and one failure due to workmanship.

Table 17. Failure Report Summary Nimbus B Flight System 1

Item	GSFC F.R.	Rad. F.R.	Date	Module/Card	P/N	S/N	Ckt. #	P/N	Manufacturer
1	11020	01906	5/23/67	Output Bd. 2A	516465G1	0002	A12	110245	G.I.
2	11021	01908	5/24/67	Submatrix B3	516531G3	0002	A51	110245	G.I.
3	11022	01907	5/23/67	Submatrix A1	516530G1	0002	A39	110245	G.I.
4	11024	01909	5/24/67	Submatrix B3	516531G3	0002	A17	110245	G.I.
5	11025	01911	5/24/67	Output Bd. 2A	516465G1	0002	A55	110426	West.
6	11026	01914	5/31/67	Prime Matrix	516492	0002	A38	110245	G.I.
7	11027	01913	5/31/67	Output Bd. 2A	516465G1	0002	A14	110245	G.I.
8	11028	01912	5/31/67	Submatrix A2	516530G2	0002	A11	110245	G.I.
9	11029	01916	6/9/67	Submatrix A3	516530G3	0002	A16	110245	G.I.
10	11031	01915	6/9/67	Output Bd. 1A	516467G1	0002	A11	110426	West.
11	11032	01917	6/16/67	Submatrix A3	516530G3	0002	A11	110245	G.I.
12	11033	01918	6/14/67	Output Bd. 1A	516467G1	0002	A31	110426	West.
13	11034	01919	6/15/67	Output Bd. 1A	516467G1	0002	A31	110426	West.
14	11023	01910	5/23/67	Submatrix A3	516530G3	0002	A29	110260	Sprague
15	11035	01920	6/16/67	Output Bd. 1A	516467G1	0002	A51	N/A	N/A

All of the above failures occurred during the initial environmental tests performed on the system. Testing was suspended after vibration tests and three days of thermal cycling had been completed so that the MOSFET failure problem could be resolved. No failures were reported during the rerun on the environmental tests.

Flight System 1 was subjected to vibration seven times during the initial environmental tests (three times consecutively without rework) and failed due to MOSFET device problems four times. All of the failures occurred during random vibration in the longitudinal axis.

Electrical tests performed in the Reliability Diagnostic Lab indicated that five of the MOSFET devices tested good, two were shorted, and two had intermittent shorts. Seven of the devices were autopsied at General Instrument and one or more particles were found in each device. Probing of the particles revealed that some were conductive and of sufficient size to create a short. The other two devices were autopsied in the Reliability Diagnostic Lab and particles were found which were large enough to cause shorts.

6.7.2.1. SYSTEM FAILURES DURING ACCEPTANCE TESTING

6.7.2.1.1. ITEMS 1, 2, 3, 7 AND 8. These devices (G.I. MOSFET's) were reported to have failed during longitudinal random vibration. Electrical tests performed in the Reliability Diagnostic Lab indicated that the devices were good. Autopsy of the MOSFET's at General Instrument revealed that particles were present in each device. The particle found in item 2 was approximately 10 mils. Holes were found in the metallization of item 7, probably due to static charge damage after removal from the system.

6.7.2.1.2. ITEMS 4 AND 11. Items 4 and 11 were reported to be shorted during longitudinal random vibration. Electrical tests indicated that each device had an intermittent short and x-rays revealed foreign particles. Particles were discovered during autopsy at G.I. which were conductive and large enough to cause a short.

6.7.2.1.3. ITEMS 5, 10, 12 AND 13. Item 5 was reported to be temperature sensitive at $-5^{\circ}C$ and items 10, 12 and 13 at $+55^{\circ}C$. The failed devices (dual DTL NAND gates) were returned to Westinghouse for analysis. Results of the analysis indicate that the devices failed due to high leakage from the stopper diodes to the substrate. The diode wire was diffused too deeply and resulted in a temperature sensitive leakage path to the substrate. This results in the base current being shorted which in turn causes V_{SAT} to increase.

Westinghouse proposed a method of screening the devices which proved to be effective. One volt is applied to pin 7 with pin 14 grounded and all other pins open. If the current is greater than ten (10) microamps the device should be rejected. All the Westinghouse devices on Flight System 1 were removed and subjected to the above test.

6.7.2.1.4. ITEMS 6 AND 9. These failures (MOSFET's) were reported during longitudinal vibration. Gate 4 of item 6 was found to be shorted during electrical tests performed in the Diagnostic Lab. Autopsy at G.I. revealed foreign particles, however, the material was firmly attached and could not be moved. A fixed gate to drain short was found in item 9. Autopsy revealed a particle which was found to be conductive and of sufficient size (3.8 X 2.9 mils) to cause a short. The metallization pattern was removed and pin holes in the oxide underneath the metallization were detected in the shorted gate. The pin holes probably resulted from a static charge after removal of the devices from the card.

6.7.2.1.5. ITEM 14. This device (NPN driver) was damaged during disassembly and repair of the system and had to be replaced.

6.7.2.1.6. ITEM 15. This failure was a cold solder joint at pin 8 of A51.

6.7.3. MALFUNCTION HISTORY SUMMARY - FLIGHT SYSTEM 2

A total of eleven failures were reported during system level testing of Nimbus B Flight System 2. All failures which occurred after the system was assembled, in a spread out configuration, are included. Table 18 lists the failures which occurred prior to acceptance level testing and table 19 lists those failures which occurred after the start of acceptance level testing.

6.7.3.1. FAILURES PRIOR TO ACCEPTANCE LEVEL TESTS

6.7.3.1.1. ITEM 1. This part (dual DTL NAND gate) was reported to be intermittent during temperature cycling at +60°C. Analysis performed by the Reliability Diagnostic Lab revealed no defects. Discussion with project personnel revealed the reported failure was most likely due to a cold solder joint. (NOTE: A cold solder joint was suspected at the time the device was replaced.)

6.7.3.1.2. ITEMS 2 AND 3. The output of submatrix A (516530G2) was intermittent during temperature cycling at +66°C. Replacement of item 2 did not correct the malfunction and, therefore, no analysis of the part was performed. Analysis of item 3 (pyrolytic MOSFET) revealed three shorted gates. Two of the shorted gates were the ones which had presented problems in the system. Autopsy of the device did not reveal the cause or location of the failure in the chip.

6.7.3.1.4. ITEM 4. This part (DTL dual-gate) failed during temperature cycling at 66°C. Preliminary analysis performed by the Reliability Diagnostic Lab indicates that the device tests are good at ambient temperature.

6.7.3.1.5. ITEM 5. Item 5 (GPA) was temperature sensitive at -20°C. The device was accidentally damaged during analysis and, therefore, no information is available. However, no other failures of this device have occurred on the Nimbus B program and it is felt that no significant information has been lost.

6.7.3.2. FAILURES AFTER START OF ACCEPTANCE LEVEL TESTS

6.7.3.2.1. ITEMS 6 THROUGH 11. Word three in most subframes was reading high during the functional test performed prior to the thermal vacuum acceptance test. Replacement of parts (items 6, 7 and 8) improved the performance of the system, but did not totally correct the malfunction. Items 9, 10 and 11 were damaged while troubleshooting the system. Further troubleshooting revealed that Coder Module 1 was unstable due to voltage ripple. A design change was performed which improved the coder stability and corrected the system malfunction. (Reference ECO #0320279 dated 11/16/67.)

Table 18. Failure Report Summary Nimbus B Flight System 2 (Prior to Acceptance Level Tests)

Item	Rad. F.R.	Date	Module	P/N	S/N	Part	P/N	Description
1	12722	10/18/67	Output Bd. 1A	516467G1	0003	A65	110426	See discussion
2	12723	10/19/67	Submatrix A	516530G2	0003	A23	110260	See discussion
3	12724	10/19/67	Submatrix A	516530G2	0003	A12	110245	See discussion
4	12725	10/19/67	Output Bd. 1B	516467G2	0003	A48	110430	See discussion
5	12747	10/20/67	Output Bd. 2B	516465G2	0003	A38	108984	See discussion

Table 19 . Failure Report Summary Nimbus B Flight System 2 (After Start of Acceptance Level Tests)

Item	Rad. F.R.	Date	Module	P/N	S/N	Part	P/N	Description
6	02927	11/2/67	Coder 2	515606G1	0005	Q37	106941	See discussion
7	02928	11/3/67	Coder 2	515606G1	0005	Q38	110092	See discussion
8	02929	11/3/67	Coder 1	515605G1	0004	Q20	110088	See discussion
9	02930	11/6/67	Coder 1	515605G1	0004	Q16	110124	See discussion
10	15137	11/9/67	Power Supply	515600G1	0005	Q5	106941	See discussion
11	15138	11/9/67	Power Supply	515600G1	0005	Q4	106941	See discussion

SECTION VII

PCM AND TME QUALIFICATION TESTING

7.1 INTRODUCTION

7.1.1 PURPOSE

To define the Environmental exposures and tests that were performed on the PCM Telemetry Subsystem for the NIMBUS Series of satellites.

7.1.2 PHILOSOPHY OF ENVIRONMENTAL TEST PROGRAM

The environmental test program delineated in the following pages is intended to provide the technical officer with a high level of confidence in the reliability of the Subsystem and the success of the Nimbus mission. The prototype tests were performed to demonstrate a sufficiently conservative margin of design safety in the telemetry subsystem. The flight acceptance test program was performed to demonstrate the successful reproduction of the subsystem.

7.1.3 PREPARATION FOR TEST PROGRAM

The PCM Telemetry subsystem submitted for prototype testing had all the protective covering, potting, etc. Any appendage or other attachment that rendered the subsystem more vulnerable were included or simulated. Flight models submitted for acceptance testing were exact replicas of the qualified prototype. The subsystem undergoing environmental exposure in either a prototype or flight acceptance test program were in the operating condition expected of it during that portion of its flight history being simulated by the environmental exposure.

7.1.4 SEQUENCE OF TESTING

In the prototype qualification and flight model acceptance test programs, exposure to the various environments were in the following order:

QUALIFICATION Prototype Test Program	FLIGHT MODEL Acceptance Test Program
1. Humidity	1. Vibration
2. Vibration	2. Thermal-Vacuum
3. Acceleration	
4. Thermal-Vacuum	

A chronological log was kept throughout the prototype and flight acceptance test programs and contained all test program data, identification, procedure descriptions, and a record of all pertinent events during the test program.

7.1.5 TEST CONDITION TOLERANCES

The following are the parameters and test condition tolerances maintained during the prototype and flight acceptance test program.

Control Tolerance - The maximum allowable tolerances on environmental test levels during testing were as follows:

a.	Temperature	$\pm 2^{\circ}C$
b.	Sine Vibration Amplitude	±10%
c.	Vibration Frequency	±2% or 1 cps, whichever is greater.
d.	Acceleration spectral density	$^{+3}_{-1}$ dB
e.	Random Total RMS Acceleration	+15% -10%
f.	Pressure	Less than 1×10^{-5} Torr

7.1.6 STANDARD CONDITIONS

Unless otherwise specified, the following were considered standard conditions:

a.	Temperature	$25^{\circ} \pm 5^{\circ}C$
b.	Relative Humidity	90% or less
c.	Barometric Pressure	Local Ambient

7.1.7 HISTORY

The Qualification Model environmental testing program can be divided into four phases. The sequence of tests performed in each phase is shown below. After each phase of testing the PCM unit was opened for repairs. The next phase of testing then took place when repairs were completed. The Qualification Model completed the room ambient acceptance test without any discrepancies before going into environmental testing; however, five prime analog channels failed.

Phase I

1. Humidity
2. Vibration
   a) Vertical axis (sine)
   b) Lateral axis (sine)

c) Longitudinal axis (sine)

d) Longitudinal axis (Random)

e) Lateral axis (Random)

f) Vertical axis (Random)

3. Acceleration

4. Thermal Cycling

a) +55°C (first)

b) -5°C (second)

c) R/A (last)

5. Stop of first phase testing

Phase II

1. Thermal Cycling

a) +55°C (first)

b) -5°C (second)

c) R/A (last)

2. Vibration

a) Longitudinal axis (Random)

3. Thermal Cycling

a) +55°C (first)

b) -5°C (second)

c) R/A (last)

4. Vibration

a) Lateral axis (Random)

b) Vertical axis (Random)

5. Stop of second phase testing

Phase III

1. Thermal Cycling
   a) +55°C (first)
   b) -5°C (second)
   c) R/A (last)
2. Vibration
   a) Longitudinal axis (Random)
   b) Longitudinal axis (sine)
   c) Lateral axis (Random)
   d) Lateral axis (sine)
   e) Vertical axis (Random)
   f) Vertical axis (sine)
3. Thermal Cycling
   a) +55°C (first)
   b) -5°C (second)
   c) R/A (last)
4. Thermal Vacuum
   a) +55°C for 24 hours
   b) -5°C for 24 hours
   c) 0°C for 48 hours
   d) +50°C for 12 hours
5. Stop of third phase testing

Phase IV

1. Thermal Vacuum

   a) +50°C for 36 hours

   b) 0°C for 48 hours

   c) +50°C for 48 hours

   d) -5°C for 24 hours

   e) +55°C for 24 hours

   f) R/A last test

2. Stop of fourth and final testing phase of the Qualification Model.

At the time of shipment Word 3 Subframe 2 was the only channel out of tolerance. Word 28 in subframe 16 failed at +55°C in thermal vacuum but returned to normal operation at room ambient. In subframe 13, words 7, 15, 23, 31, 39, 47 and 55 failed during the repair sequence in phase 3 but were normal throughout the following thermal vacuum tests.

7.2 HUMIDITY

7.2.1 PURPOSE

The purpose of the Humidity testing program was to demonstrate a conservative margin of design safety in equipment operation when exposed to operational environmental operating conditions.

7.2.2 RESULTS

The Humidity test was carried out in Phase I testing and since no electrical problems were encountered it was not repeated in any other phase.

7.2.3 TEST EQUIPMENT REQUIRED

a) Tektronix 545A scope

b) Type CA or 1A1 pre-amp

c) Type D pre-amp

d) HP 3460 A DVM

e) Simpson 260 or equivalent V.O.M.

f) HP Wide Range Oscillator Model CDR 200

g) HP Frequency Counter Model 524C

h) HP Frequency Converter Model 525C

i) HP Power Meter Model 434A

7.2.4 PROCEDURES

Refer to the Nimbus B PCM Telemetry Subsystem Acceptance Test Procedure RAD 342 and 343 for all test procedures. The room ambient acceptance test serves as the Pre-test for humidity.

7.3 VIBRATION

7.3.1 PURPOSE

The purpose of the Vibration testing program was to demonstrate a conservative margin of design safety in equipment operation when exposed to environmental operating conditions.

7.3.2 RESULTS

7.3.2.1 PHASE I. Five prime analog channels were out of tolerance before going into the vertical sine axis of vibration. These five prime analog channels corrected themselves during this test so that all channels were normal after the test. The next plane of vibration was the Lateral sine axis. The BTE command for PCM 2 was lost in this test and channel verification had to be accomplished manually, all channels were normal after this test. During the Longitudinal sine axis six analog subcom channels were lost; all other circuits, except for the BTE command for PCM 2, were functioning normally. Vibration in the Longitudinal Random axis caused the loss of two additional prime analog channels but corrected the BTE Command for PCM 2. Lateral Random and Vertical Random axis caused no further channel failures. Vertical Random axis caused the BTE command for PCM 2 to fail again. The total number of failures experienced at one time or another during vibration are as follows; two prime analog channels, six subcom analog channels and the BTE command for PCM 2. The five prime analog channels that were out of tolerance going into vibration and that corrected themselves after the vertical sine axis are still good. The channels and current monitored during the vibration tests were stable and all circuits other than those mentioned functioned well. The TME had no failures through vibration.

7.3.2.2 PHASE II. The first plane of vibration in phase II testing was the longitudinal random axis. All channels were good going into the test. During longitudinal random vibration, six subcom analog channels plus five prime digital channels were lost on both PCM's. The PCM 2 data also became intermittent. After completion of a second thermal cycle vibration of the system was continued. The first plane to be run after the second thermal cycle was lateral random. No additional channel failures were experienced in this plane and the prime digital channels corrected themselves during this test. The vertical random axis contributed no additional channel failures. PCM data was intermittent throughout vibration testing. The TME had no failures throughout vibration.

7.3.2.3 PHASE III. In the third phase of testing only the PCM unit was vibrated as the TME had already successfully completed two phases of vibration testing. All channels were good going into third phase testing and no channel failures were experienced in any of the six planes of vibration. The channels and current monitored during the vibration tests were stable and all circuits functioned well.

7.3.3 TEST EQUIPMENT REQUIRED

Test equipment required is listed in paragraph 7.2.3.

7.3.4 PROCEDURES

Refer to the Nimbus B PCM Telemetry Subsystem Acceptance Test Procedure RAD 342 and 343 for all test procedures

7.4 ACCELERATION

7.4.1 PURPOSE

The purpose of the Acceleration testing program was to demonstrate a conservative measure of design safety when the operational equipment was exposed to environmental operating conditions.

7.4.2 RESULTS

The acceleration test was carried out in phase I testing and since no electrical problems were encountered it was not repeated in any other phase. All channels and current monitored during the tests were stable and all circuits functioned well.

7.4.3 TEST EQUIPMENT REQUIRED

The test equipment required is listed in paragraph 7.2.3.

7.4.4 PROCEDURES

Refer to the Nimbus B PCM Telemetry Subsystem Acceptance Test Procedure RAD 342 and 343 for all test procedures.

7.5 THERMAL CYCLING

7.5.1 PURPOSE

The purpose of the Thermal Cycling testing was to demonstrate a conservative measure of design safety when the operational equipment was exposed to environmental operating conditions.

7.5.2 RESULTS

7.5.2.1 PHASE I. Going into phase 1 thermal cycling the following channel failures were present; five intermittent prime analog failures (before thermal cycling these channels read normal), six analog subcom channels, the BTE command for PCM 2 and two prime analog channels lost in the longitudinal random axis of vibration. At +55°C in the thermal cycle test the five intermittent prime analog channels again went out of tolerance, the other failure remained unchanged. A new subcom analog channel on both PCM's plus all subcom digital channels on submatrix boards A2 and B2 of PCM 1 failed. The last two words of time code (units and tens of hours) in PCM 1 also failed at -5°C. The new analog subcom channel failure gained at +55°C, read normal as did the subcom digital channels on submatrix cards A2 and B2. The last two words of time code in PCM 1 also returned to a normal condition. The BTE command for PCM 2 did not recover at the low temperature end; all circuits other than those mentioned functioned well. The TME unit had no failures throughout the thermal cycling.

7.5.2.2 PHASE II. Two thermal cycles were run in phase 2 testing; one before and one after longitudinal random vibration. No electrical problems were encountered during the first thermal cycle before vibration. Going into the second thermal cycle however, several failures were present. These failures, consisting of six analog channels and five prime digital channels, occurred in longitudinal random vibration. During the second thermal cycle at +55°C the five digital channels corrected themselves and appeared normal for the rest of the thermal cycle. No new electrical failures were encountered in this test. The TME unit had no failures throughout the second phase of thermal cycling.

7.5.2.3 PHASE III. In phase 3, only the PCM unit was subjected to thermal cycling as the TME had successfully completed two previous phases of thermal testing. Two thermal cycles were conducted in phase 3 testing one before and one after the six planes of vibration. No electrical problems were experienced in either test. All circuits functioned well during thermal cycling.

7.5.3 TEST EQUIPMENT REQUIRED

The test equipment required is listed in paragraph 7.2.3.

7.5.4 PROCEDURES

Refer to Nimbus B PCM Telemetry Subsystem Acceptance Test Procedure RAD 342 and 343 for all test procedures.

7.6 THERMAL VACUUM

7.6.1 PURPOSE

The purpose of the Thermal Vacuum testing was to demonstrate a conservative measure of design safety when the operational equipment was exposed to environmental operating conditions.

7.6.2 RESULTS

7.6.2.1 PHASE III. Phase 3 thermal vacuum tests on the Nimbus B Telemetry Subsystem were curtailed after 108 hours due to a major system failure in PCM 1. Earlier in the thermal vacuum test two analog subcom channel failures were experienced. These channel failures occurred in the +55°C portion of the test. When the thermal vacuum chamber was returned to room temperature and pressure only, one subcom analog failure remained. The TME unit had no electrical failures during this phase, all other circuits other than those mentioned functioned well.

7.6.2.2 PHASE IV. The PCM unit was opened and the major system failure was repaired. The channel failures were traced to Fairchild MOS gates, therefore, it was decided those channels would not be repaired. During the repair sequence seven additional subcom analog channels went out of tolerance, however, they were reading normal when the PCM unit was repackaged and did not fail in fourth phase thermal vacuum. No additional channel failures were encountered during the fourth phase of testing in thermal vacuum. The remaining portion of the thermal vacuum test was completed and the first portion of the test was then rerun with the system at room temperature and pressure (at the end of the thermal vacuum test), only one subcom analog channel was out of tolerance. Some problem with the Raymond tape recorders was experienced during fourth phase testing, the recorders have since been repaired. No electrical problems were encountered with the TME unit.

7.6.3 TEST EQUIPMENT REQUIRED

Test equipment required is listed in paragraph 7.2.3.

7.6.4 PROCEDURES

Refer to the Nimbus B PCM Telemetry Subsystem Acceptance Test Procedure RAD 342 or 343 for all test procedures.

SECTION VIII

FLIGHT SYSTEMS 1 AND 2

PCM AND TME ACCEPTANCE TESTING

8.1 INTRODUCTION

This section contains the history of the acceptance tests performed on the NIMBUS B PCM Telemetry Flight Systems 1 and 2 and includes a discussion of the results, a listing of the test equipment required, and of the test procedures used. The purpose of the acceptance test program was to demonstrate the successful reproduction of the Subsystems. The qualification tests performed on the prototype were designed to demonstrate a sufficiently conservative margin of design safety in the PCM Telemetry Subsystem. This section is divided into a discussion of the Flight System 1 tests and a discussion of the Flight System 2 tests. The discussion of the Flight System 2 tests precedes that of Flight System 1 since the tests on Flight System 2 were completed first because of the MOSFET problem.

8.2 FLIGHT SYSTEM 2

This section contains the history of the acceptance testing of the Flight System 2 PCM and TME units.

8.2.1 PCM UNIT

Flight 2 testing of the PCM Unit is divided into two phases. The sequence of tests performed in each phase is shown below. After the first phase of testing, the PCM unit was opened for repairs. The second phase of testing then took place when all repairs were completed. The Flight 2 system completed the room ambient acceptance test without any discrepancies.

Phase I

1. Vibration
    a. Vertical axis (sine)
    b. Lateral axis (sine)
    c. Longitudinal axis (sine)
    d. Longitudinal axis (Random)
    e. Lateral axis (Random)
    f. Vertical axis (Random)

2. Stop of first phase testing

Phase II

1. Vibration

   a. Longitudinal (Random) axis

2. Thermal Vacuum

   a. +50°C for 24 hours

   b. 0°C for 24 hours

   c. +5°C for 48 hours

   d. +45°C for 48 hours

   e. +5°C for 48 hours

   f. +45°C for 48 hours

   g. R/A (last test)

3. Stop of second and final testing phase of Flight 2

8.2.1.1 VIBRATION.

8.2.1.1.1 RESULTS.

a. Phase I

In the first phase of testing, only the PCM unit was vibrated as the TME had already successfully completed vibration during Flight 1 testing. All channels were good going into first phase testing and no channel failures were experienced in any of the six phases of vibration. The channels and current monitored during vibration tests were stable and all circuits functioned well.

b. Phase II

In the second phase of vibration, only the PCM unit was vibrated. All channels were good going into second phase testing and no channel failures were experienced in the Longitudinal Random axis. The channels and current monitored during vibration tests were stable and all circuits functioned well.

8.2.1.1.2 TEST EQUIPMENT REQUIRED. The following test equipment was required for Phase II:

a. Tektronix 545A Scope

b. Type CA or 1A1 Pre-Amp

c. Type D Pre-Amp

d. HP 3460-A DVM

e. Simpson 260 or equivalent V.O.M.

f. HP Wide Range Oscillator Model CDR 200

g. HP Frequency Counter Model 524C

h. HP Frequency Converter Model 525C

i. HP Power Meter Model 434A

8.2.1.1.3 PROCEDURES. Refer to the Nimbus B PCM Telemetry Subsystem Acceptance Test Procedure RAD 342 and 343 for all test procedures. The room ambient acceptance test serves as the Pre-test for vibration.

8.2.1.2 THERMAL VACUUM.

8.2.1.2.1 RESULTS.

a. Phase I

Just before going into Phase I termal vacuum tests, a malfunction occurred in PCM 1 and testing was curtailed.

b. Phase II

During Phase 2 thermal vacuum tests on the Nimbus B Telemetry Subsystem, no electrical failures were experienced, all circuits functioned normally.

8.2.1.2.2 TEST EQUIPMENT REQUIRED. Refer to paragraph 8.2.1.1.2.

8.2.1.2.3 PROCEDURES. Refer to paragraph 8.2.1.1.3.

8.2.2 TME UNIT

The TME used on Flight 2 was originally scheduled for installation in Flight 1, thus testing of the TME started during the first phase of Flight 1 testing.

Prior to running the room ambient ATP, the TME had to be opened twice to correct wiring errors not detected in preliminary checkout.

The room ambient acceptance test was completed without any discrepancies. The following test sequence was performed in Environmental testing.

Phase I

1. Vibration
    a. Longitudinal axis (sine)
    b. Longitudinal axis (Random)
    c. Lateral axis (sine)
    d. Lateral axis (Random)
    e. Vertical axis (sine)
    f. Vertical axis (Random)
2. Abbreviated Thermal Cycle
    a. +55°C (stabilized for one hour)
    b. -5°C (stabilized for one hour)
3. Thermal Vacuum
    a. +50°C for 24 hours
    b. 0°C for 24 hours
    c. +5°C for 48 hours
    d. 45°C for 48 hours
    e. +5°C for 48 hours
    f. +45°C for 48 hours
    g. R/A (last test)
4. Stop of first and final testing phase of TME.

8.2.2.1 VIBRATION.

8.2.2.1.1 RESULTS. The TME unit completed all vibration tests successfully. The signals and current monitored during vibration tests were stable and all circuits functioned well.

8.2.2.1.2 TEST EQUIPMENT REQUIRED

a. Tektronix 545A Scope

b. Type CA or 1A1 Pre-amp

c. Type D Pre-amp

d. HP 3460-A DVM

e. Simpson 260 or equivalent V.O.M.

f. HP Wide Range Oscillator Model CDR200

g. HP Frequency Counter Model 524C

h. HP Frequency Converter Model 525C

i. HP Power Meter Model 434A

8.2.2.1.3 PROCEDURES. Refer to the Nimbus B PCM Telemetry Subsystem Acceptance Test Procedure RAD 342 and 343 for all test procedures. The room ambient acceptance test serves as the Pre-test for vibration.

8.2.2.2 ABBREVIATED THERMAL CYCLE.

8.2.2.2.1 RESULTS. The TME unit completed all phases of this test successfully. No problems were encountered.

8.2.2.2.2 TEST EQUIPMENT REQUIRED. Refer to paragraph 8.2.2.1.2.

8.2.2.2.3 PROCEDURES. Refer to paragraph 8.2.2.1.3.

8.2.2.3 THERMAL VACUUM.

8.2.2.3.1 RESULTS. The TME completed all phases of thermal vacuum testing successfully. No problems were encountered.

8.2.2.3.2 TEST EQUIPMENT REQUIRED. Refer to paragraph 8.2.2.1.2.

8.2.2.3.3 PROCEDURES. Refer to paragraph 8.2.2.1.3.

8.3 FLIGHT SYSTEM 1

This section contains the test history of the Flight System No. 1 of the Nimbus B PCM Telemetry System consisting of the Pulse Code Modulation (PCM) Unit Serial No. 0002 and the Telemetry Electronics (TME) Unit Serial No. 0003. This section contains the entire test history of PCM Unit Serial No. 0002 including the testing accomplished in May-June 1967

prior to the MOSFET device change and the final phase of testing January-February 1968 accomplished after the MOSFET device change was incorporated into this unit. The test history and test data for TME Unit Serial No. 0002 occurring in the May-June 1967 period was included in the Flight System No. 2 Test Data Report delivered with the Flight System No. 2 Test Data Report delivered with the Flight System No. 2 equipment and is not included as part of this report. However, this report does include the entire test history and test data for the TME Unit Serial No. 0003 and the PCM Unit Serial No. 0002.

8.3.1 PCM UNIT SERIAL NO. 0002

The testing of the PCM Unit divided into five phases. The first four phases cover the tests conducted on the PCM Unit Serial No. 0002 in the May-June 1967 period prior to the MOSFET device change. Phase 5 covers the tests performed on the PCM Unit after this change.

8.3.2 PCM UNIT PHASE I TEST HISTORY 20-22 MAY 1967

8.3.2.1 PRETEST HISTORY. The PCM history before going into acceptance test and environmental testing is as follows:

a. PCM compressed (first time), had to be reopened due to system failure.

b. PCM compressed (second time), had to be reopened due to system failure.

c. PCM compressed (third time), checked o.k. and was packaged.

d. PCM Box had to be reopened due to wiring error in J1 and J13 connectors (system did not have to be restrung).

e. PCM was repackaged and was ready for Room Ambient acceptance test.

8.3.2.2 ROOM AMBIENT ACCEPTANCE TEST. The PCM unit had no problems during the Room Ambient Acceptance Test.

8.3.2.3 ENVIRONMENTAL TESTING. The tests performed on the PCM unit during environmental testing with the following results are listed below:

a. Vibration (Longitudinal Sine)

No problems with the PCM Unit.

b. Vibration (Longitudinal Random)

The following failures were experienced in the PCM unit:

1. PCM 1

a. Prime Digital Channel failures.
DGP-54, 16, 52, 19, 55, 17, 51, 20, 53.

b. Subcom Digital Channel failures.
DG-16, 156, 86, 226, 87, 227, 17, 157, 18, 158, 19, 159, 20, 160, 51, 121, 52, 261, 53, 54, 262, 124, 263, 125, 264, 55 and 265.

c. Subcom Analog Channel failure.
1/16A 275, 277, 279, 281, 283, 287, 291 and 295.

d. Digital words feeding through on the analog check due to the loss of the overvoltage pulse.
1/16D 25, 28, 31, 34 and 39.

2. PCM 2

a. Subcom Digital Channel failure.
DG 20.

b. Subcom Analog Channel failure.
Same as PCM 1 Subcom test.

c. Vibration (Lateral Sine)

No additional problems.

d. Vibration (Lateral Random)

No additional problems.

e. Vibration (Vertical Sine)

No additional problems.

f. Vibration (Vertical Random)

No additional problems.

g. Abbreviated Thermal Cycle

A quick thermal cycle (from -5 to +55°C) was performed on the PCM uncovering the following additional problems:

1. Loss of sync on PCM 1 at the -5°C pt.

2. Possible additional channel failures were encountered, these will be checked and covered in a later report if they are a problem.

8.3.2.4 PCM UNIT REPAIRS AFTER THE FIRST ENVIRONMENTAL TESTING PHASE. The discrepancies pointed out in paragraph C above under Environmental Testing were resolved. The findings and corrections made are as follows.

8.3.2.4.1 PCM 1

a. Prime Digital Channel Failures DGP-54, 16, 52, 19, 55, 17, 51, 53, and 20.

1. Discrepancy - All read zero when ones were fed into the digital channels.

2. Action - Replaced A12 on output board 1 in PCM 1. This flatpack appeared to have a body to drain short as a + voltage was observed on the output of this flatpack.

b. Subcom Digital Channel Failures DG-16, 156, 86, 226, 87, 227, 17, 157, 18, 158, 19, 159, 20, 160, 51, 121, 52, 261, 53, 54, 262, 124, 263, 125, 264, 55, and 265.

1. Discrepancy - All read zero when "ones" were fed into the digital channels.

2. Action - See Prime Digital Channels, PCM 1.

c. Time Code

1. Discrepancy - (This failure was left out of the preliminary report 1210-4120-0043 dated 22 May 67). Loss of bit 2^3 (most significant bit in time code.) Read one all the time.

2. Action - See Prime Digital Channels, PCM 1.

d. Subcom Analog Channel Failures 1/16A, 275, 277, 279, 281, 283, 287, 291, and 295.

1. Discrepancy - All read high.

2. Action - Replaced A51 on submatrix Card B3.

e. Digital words feeding through on the analog check 1/16D, 25, 28, 31, 34, and 39.

1. Discrepancy - The -15V overvoltage line was being shorted to the +6V body supply due to a short in MOS gate A51 between the body (Pins 6, 7, or 9) and the source (probably Pin 11).

2. Action - A51 replaced (See item 4 under PCM 1).

8.3.2.4.2 PCM 1 AND 2 FAILURES

a. Subcom Digital Channel Failure DG 20.

1. Discrepancy - Digital channel read "1" all the time on both PCM's.

2. Action - Replaced A39 on submatrix card A1.

b. Subcom Analog Channels 1/16A 241, 237, 233 replaced A17 on submatrix card B3.

8.3.2.4.3 PCM 2

a. Subcom Analog Channel failures same as Items 4 and 5 under PCM 1.

8.3.2.4.4 THERMAL CYCLE

a. Discrepancy - Loss of sync on PCM 1 at the -5°C pt.

b. Action - Replaced A55 on output board 1 of PCM 1 (a Westinghouse gate).

8.3.2.4.5 FAILURES PROBABLY DUE TO OPENING SYSTEM

a. Discrepancy - Loss of row 5, 6, 7, and 8 on submatrix board A3 and B3 when PCM 2 was on.

b. Action - Replaced NPN driver A29 on submatrix board A3

NOTE

Failure report 01910 states Submatrix B3, assembly #516531-G3; this should have read Submatrix A3 assembly #516430-G3 .

The unit underwent an abbreviated ATP and was readied for vibration.

8.3.2.5 SUMMARY. The PCM was reopened and all cards inspected for lifted flatpack leads and/or bad flatpacks. Paragraph D covers the cause of the failures listed in this report. The PCM was vibrated after repairs were completed. The unit then went into the normal Thermal Cycle test.

8.3.3 PCM UNIT PHASE II TEST HISTORY 26-27 MAY 1967

The tests performed on the PCM unit during Phase 2 of environmental testing with results and corrective actions are as follows:

8.3.3.1 VIBRATION (LONGITUDINAL AND RANDOM).

a. Vibration (Longitudinal Sine)

No problems were encountered.

b. Vibration (Longitudinal Random)

1. PCM 1

a. Discrepancy - Loss of the 2^2 bit in all words.

b. Action - Replaced MOS gate A14 on output board 2A.

2. PCM 1 and PCM 2

a. Discrepancy - Prime digital word 6 read through on prime analog check.

b. Action - Replaced MOS gate A38 on prime board.

c. Discrepancy - Subcom digital-subframe 2, word 4 read all ones.

d. Action - Replaced MOS gate A11 on submatrix card A2.

3. PCM 2

a. Discrepancy - Analog subcom-subframe 2, words 12, 28, 31, 35, 39, 43, 47, 51, 55, and 59.

NOTE

These words were probably out on PCM 1 too, but could not be checked due to the loss of the 2^2 bit.

b. Action - Replaced A11 on submatrix card A2 (See Item 2 under PCM 1 and 2).

4. Problems Due to Opening System

a. Discrepancy - Loss of digital channels DG 241, 242, 243, 244, 245 (26 bit) read "1" all the time.

b. Action - Amp-interconnect 321 on submatrix card A4 was replaced.

8.3.4 PCM UNIT PHASE III TEST HISTORY 2-3 JUNE 1967

The tests performed on the PCM unit during Phase III of environmental testing with the following results and corrective actions are as follows:

8.3.4.1 VIBRATION.

a. Vibration (Longitudinal Random)

1. PCM 1 and PCM 2 Test Results

a. Discrepancy - Subcom analog channel read high, failure occurred in Subframe 7, Word 23 (1/16 A169). Five additional subcom analog channels were slightly degraded but were in spec. These channels were in Subframe 7, Words 7, 15, 31, 55, and 47.

b. Action - Replaced MOS Gate A16 on submatrix, Card A3 seemed to have a drain to gate short during vibration, however, the channel read normal after remaining at +55°C for awhile during the thermal cycle.

b. Vibration (Longitudinal Random)

No additional channel failures

8.3.4.2 THERMAL CYCLING.

a. +55°C

1. Failure and Corrective Action

a. Discrepancy - Recoder #1 started drawing excessive current in the P.B. Mode.

b. Action - A short was discovered in the recorder cabling and has been repaired.

2. Failure and Corrective Action

a. Discrepancy - Several prime analog channels on PCM 1 failed. Words 10, 18, 34, 42, and 50 read low.

b. Action - Replaced Westinghouse Gate A11 on Output Board 1A.

3. Failure and Corrective Action

a. Discrepancy - During the +55°C portion of thermal cycling on the Flight 1 Nimbus B Telemetry Subsystem the PCM 2 unit began to randomly drop several bits of data from the data train. Further investigation uncovered a circuit in the Shift Register and Split-Phase Converter Module that was causing the trouble.

b. Action - R61 in the Shift-Register Module was changed from an 18K to a 6.8K. A report has been written covering the change.

b. -5°C

All channels read normal during this test and after returning to room ambient. No new channel failures were experienced.

8.3.4.3 PROBLEMS DUE TO OPENING SYSTEM.

8.3.4.3.1 FAILURE AND CORRECTIVE ACTION.

a. Discrepancy - Cold solder joint on flatpack A51, Pin 8. This flatpack is located on Output Board 1A.

b. Action - Pin 8 resoldered.

8.3.3.3.2 FAILURE AND CORRECTIVE ACTION

a. Discrepancy - During a preliminary temperature run a Westinghouse gate failed at the +55°C end in PCM 1. The gate was located on output board 1A and was flatpack A31. A second gate was installed on the board with the same failure mode indications.

b. Action - Both gates had data code 612 which is from the group of gates that should not be used in the system. A later data coded gate was used and the problem was cured.

8.3.4.4 RETEST. The PCM unit was repaired and retested.

8.3.5 PCM UNIT PHASE 4 TEST HISTORY 15 JUNE 1967

The tests performed on the PCM unit during Phase 4 of environmental testing with the following results and corrective action are as follows. This paragraph concludes the test history of PCM Unit Serial No. 0002 to the time that the MOSFET problem caused a halt to further testing.

8.3.5.1 VIBRATION (LONGITUDINAL RANDOM).

a. PCM 1 and 2

1. Discrepancy - Subcom analog channels 1/16A10, 13,17, and 21 read out of tolerance. Channels appeared to be open.

2. Action - A cold solder joint was discovered on Pin 1 of flatpack A31 on submatrix card A1.

8.3.5.2 VIBRATION (LONGITUDINAL RANDOM).

The PCM Unit was turned upside down and vibrated a second time with the following additional failures:

a. PCM 1 and 2

1. Discrepancy - Subcom analog channels 1/16A25, 29, 35, 39, 43, 47, and 32 read out of tolerance. Appeared to have a gate-to-drain short.

2. Action - Flatpack A11 on submatrix card A3 was replaced.

NOTE

It was assumed that the above items would cure all problems encountered during vibration; however, NASA stopped further testing until the MOS gate problem could be resolved.

8.3.6 PCM UNIT (AND TME UNIT SERIAL NO. 0003) PHASE V TEST HISTORY 28 JANUARY THROUGH 11 FEBRUARY 1968

This phase of testing of Flight System I of the Nimbus B PCM Telemetry involved both the PCM and TME Units, PCM Serial No. 0002 and TME Serial No. 0003. The system was vibrated both sine and random in lateral, longitudinal and vertical axis without failures on 28 January 1968.

The system began thermal vacuum on 29 January 1968 and completed thermal vacuum without failure on 10 February 1968 and the post-thermal vacuum test was completed on 11 February 1968 without failures. A minor design anomaly was uncovered in testing at General Electric. Due to the fact it is not detrimental to system mission performance, the problem will not be corrected and the system will be shipped on a waiver of this anomaly. See the January 1968 Monthly Progress Report for a discussion of the problem.

8.3.7 TME UNIT SERIAL NO. 0003 TEST HISTORY

Refer to paragraph 8.3.6.

8.3.8 TEST EQUIPMENT REQUIRED

The following test equipment was required. The environment test equipment used is listed in the individual environmental acceptance test reports supplied with the test reports shipped with Flight System 1.

	Description and Part Number		Serial No.	Calibration Date Due
a.	Oscilloscope RM 45A		2160	6-9-67
b.	Plug-In Type 1A1		105595	5-26-67
c.	Oscillator Type 200 CDR		42905	10-27-67
d.	Digital Voltmeter Type 3460A		105668	32-7
e.	Simpson Model 270		211402	33-7
f.	BTE		0003	
g.	KEPCO P/S	SC-32-0.5	27565	8-11-67
h.	Plug-In	Type D	212898	34-7
i.	P/S KEPCO	ABC 40-0.5 M	301051	11-10-67

8.3.9 TEST PROCEDURES

Refer to paragraph 8.2.1.1.3.