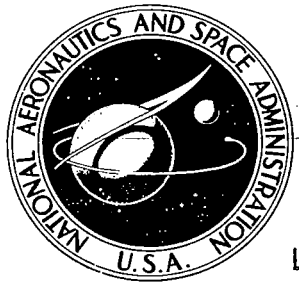
NASA CONTRACTOR REPORT



MOS FIELD-EFFECT-TRANSISTOR TECHNOLOGY

by J. T. Wallmark, W. A. Bösenberg, E. C. Ross, D. Flatley, and H. Parker

Prepared by
RADIO CORPORATION OF AMERICA
Princeton, N. J.
for Langley Research Center

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MOS FIELD-EFFECT-TRANSISTOR TECHNOLOGY

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RCA Laboratories

SUMMARY

Under the scope of this contract, integrated MOS circuit technology, as part of a laminated ferrite memory project, has been investigated. The prime target has been the development of a 64-transistor word-driver circuit, but the advances in technology have been applied also to a 100-transistor digit-driver circuit, an 85-transistor word-decoder circuit, and a 100-transistor load circuit for the decoder.

The more noteworthy advances in technology under the contract fall in the following main areas: A contact metallization technique compatible with the low-temperature, low-pressure circuit connection technique used; a circuit encapsulation and passivation technique compatible with the packaging and connection technique; a low-temperature-deposited crossover insulation technique with low pinhole probability even at moderate steps and low and reproducible influence on the surface potential in the gate region. By applying results obtained on other projects at RCA Laboratories, a packaging technique allowing a large number of connections on 0.010-in. centers with high yield and long life, and also a technique for fabrication of MOS transistors with excellent operating life characteristics, have been incorporated.

The advances have resulted in the fabrication of word-driver strips with the expected performance and with acceptable yield (5% for full strips; 30% counting half-strips).

Sufficiently good circuits have been obtained for preliminary tests. One test has been run incorporating only the word driver connected to a ferrite array. A second, more advanced test is being planned incorporating most of the memory driving circuits.

In one particular area considerable understanding has been gained, leading to definite practical results of significance to this project and also to other related projects. This area is silver contact stability, a key point in the circuit packaging scheme, and of which a detailed account is given in this report.

In other areas where exploratory work was made the problems encountered were too great and, inasmuch as the solutions to the problems were not essential to the realization of an operating memory system, the work in these areas was curtailed and instead concentrated on essential bottlenecks. Such areas were: insulators for the gate region (silicon nitride, vanadium pentoxide), insulators for the crossovers (silicon nitride, phosphor silicate glass), gate healing techniques, mask limitations on yield, etc.

INTRODUCTION

The limited capacity of random-access memories available in today's computing systems - of the order of 10^6 bits - severely limits the capability of these systems. For the commercial environment, economic considerations primarily limit the capacity of core stores, the most widely used form. With the recent introduction of novel electronic selection schemes and the adoption of simplified core wiring and stacking, capacities in excess of 10^7 bits have become economically feasible.

For space and military environments, the maximum usable core capacity is determined by considerations other than economics. Size, weight, power consumption, reliability, etc., are generally more important than the exact cost per bit. A number of devices in addition to ferrite cores are under intensive development for space and military environments.

Laminated ferrite memory stacks operated with integrated Metal-Oxide-Semiconductor (MOS) transistor circuits are eminently suited to a space or military environment. The memory offers bit densities unmatched by other techniques. Operation with low drive currents (low power) yields relatively high sense signals. The combination of low drive power and high output is essential for the successful use of integrated semiconductor circuits.

The integration of laminated ferrite stacks with integrated MOS circuits is expected to yield a memory system with a capacity in excess of 10^7 bits operating at a few microseconds cycle time. Low power, small size, tolerance to severe environments, as well as low bit cost, is possible with these systems.

Briefly, a laminated ferrite array is a monolithic sheet of ferrite with an embedded matrix of conductors fabricated by a batch process. The embedded conductors form two sets of insulated, mutually orthogonal windings. Operation is in a word-organized mode with one set of windings used for read-write energization, and the other set for the sense digit function.

An MOS transistor is formed by diffusing and metallizing two isolated n-type regions in a p-type crystal to form the source and drain electrodes. An oxide layer is formed on the crystal surface between the source and drain regions, and a metal layer, the gate electrode, is deposited on top of the oxide. These transistors can be fabricated as integrated arrays to be used either for switching applications or as amplifying units. Further, complementary types (p-regions diffused in n-crystals) can also be fabricated.

One possible organization of the memory is illustrated in the exploded view of Figure 1. Only two ferrite planes are shown, each containing 256 words of 100 bits (25,600 bits). Thus, a memory of 10^6 bits would consist of about 40 such planes stacked vertically. Each plane is driven by four MOS word-driver strips. Several planes in parallel are driven by a set of MOS decoder strips with associated decoder load units, consisting of complementary MOS transistors. At the end terminals of the digit-side windings are

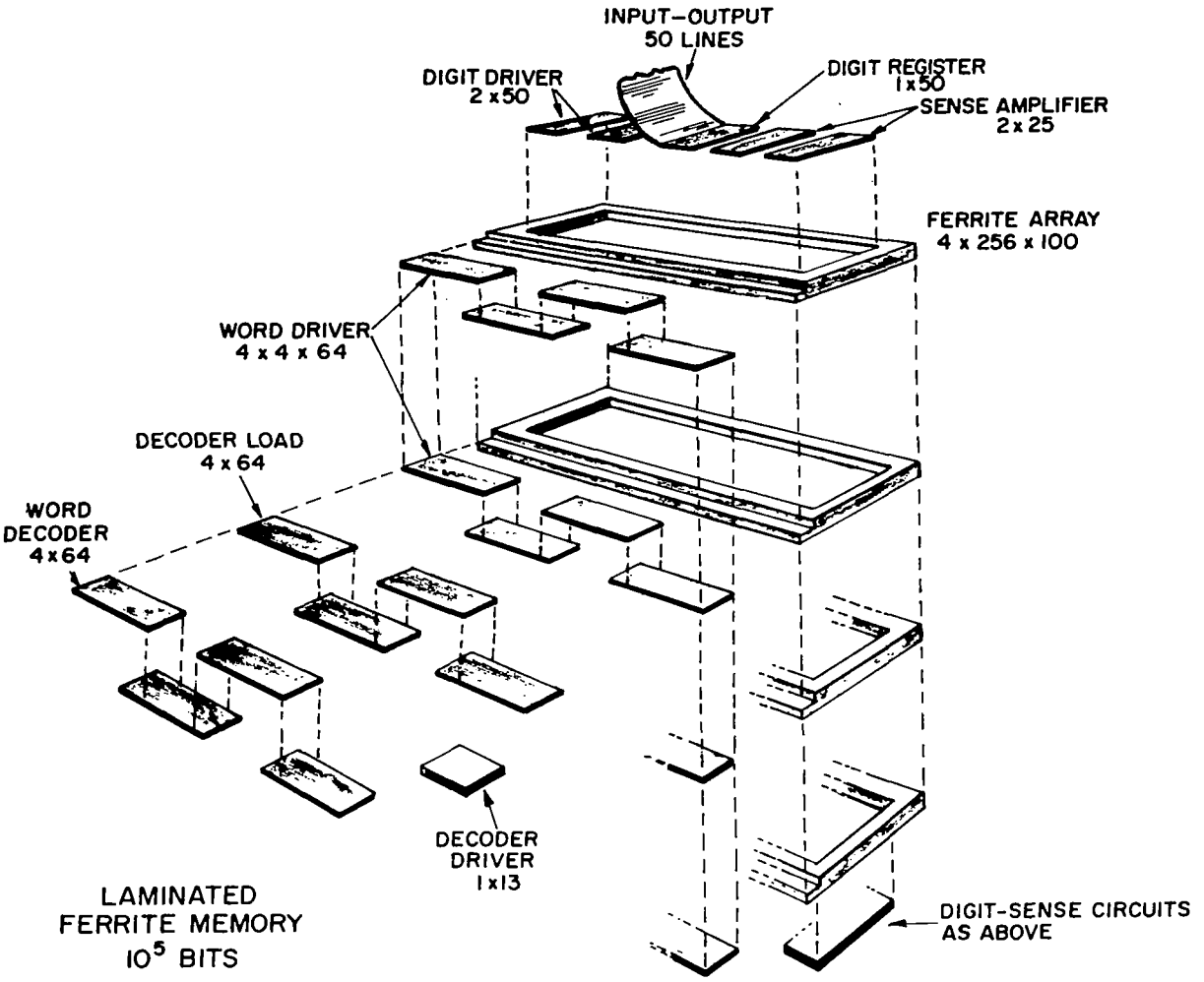


Figure 1. Exploded view of a laminated ferrite memory system assembly. Two ferrite planes, each containing 256 by 100 bits and associate circuitry, are shown.

terminating resistors, a pair of MOS digit driver strips, and a sense amplifier strip for each stack.

Preliminary estimates, which have been further substantiated during this contract, indicate that a random-access memory system with the following characteristics may be realized by integrating laminated arrays with integrated MOS circuits.

Memory capacity	1.3×10^7 bits
Number of words	65,536
Number of bits per word	200
Ferrite stack bit density	10^4 bits/in.^{2} 2×10^5 bits/in.^{3}
Ferrite stack volume	65 in.^{3}
Memory system volume (ferrite stack and electronics)	130 in.^{3}
Memory system weight	15 lbs.
Average power consumption for a 2-μsec random-access cycle	100 W

For the above-specified memory, the equivalent serial information rate is 10^8 bits/second. Reducing the equivalent serial information rate reduces the power consumption. For a maximum rate of 10^6 bits/second, the estimated average power consumption is less than 10 watts.

The scope of the present contract has been the development of MOS field-effect transistor technology to the point where word-driver strips encompassing 64 interconnected transistors may be fabricated with a reasonable yield and with sufficient performance to drive a practical ferrite array. At the same time, the word-driver transistors and the ferrite array have to be packaged with a method that is compatible with the ferrite as well as the silicon technology encompassing all other circuits of the system, and that holds promise of meeting the demands of space as well as ground use.

This report consists of two parts. Part I summarizes the overall results of the work done under the contract. Part II contains a complete report of all the work done on one of the key aspects of the system, the connection method. This part of the work was carried to a very satisfactory conclusion.

The work described in this report was pursued at RCA Laboratories, Princeton, New Jersey, in the Computer Research Laboratory, Dr. Jan A. Rajchman, Director. Dr. Rabah Shahbender was the Project Supervisor and Dr. J. Torkel Wallmark was the Project Scientist. In addition to the Members of the Technical Staff listed on the cover, the following contributed to the program: Mr. P. Asbeck, Mr. C. A. Reed, Dr. Anthony D. Robbi, Mr. James Tuska, and Mr. Joseph L. Walentine. Word-driver strips were fabricated under RCA funds by Norman H. Ditrick and Harold W. James under the supervision of Dr. Richard Glicksman, all of RCA Electronic Components and Devices, Somerville, New Jersey.

PART I

MOS FIELD-EFFECT-TRANSISTOR TECHNOLOGY FOR FERRITE MEMORIES

MOS Word-Driving Circuit. -- The construction of the word-driver circuit and the packaging used to connect it in the system are described in Figures 2 through 6 and the accompanying text. Figure 2 shows the basic MOS transistor, which is used with minor variations in all the driving circuits. The transistor is a silicon n-channel depletion-type, insulated-gate field-effect transistor with phosphorus-diffused source and drain regions, aluminum gate metallization, and chromium-silver source-drain metallization. The gate insulator is silicon dioxide, thermally grown in dry oxygen, 800 Å thick. On top of the gate region, blanketing the gate metal, is a 3000-Å-thick low-temperature deposited silicon dioxide layer covering also the gate metal. Outside the active device region is a 10,000-Å-thick thermal silicon dioxide and an additional 3000-Å-thick layer of deposited oxide. The semiconductor fabrication procedure is described in more detail in Appendix A.

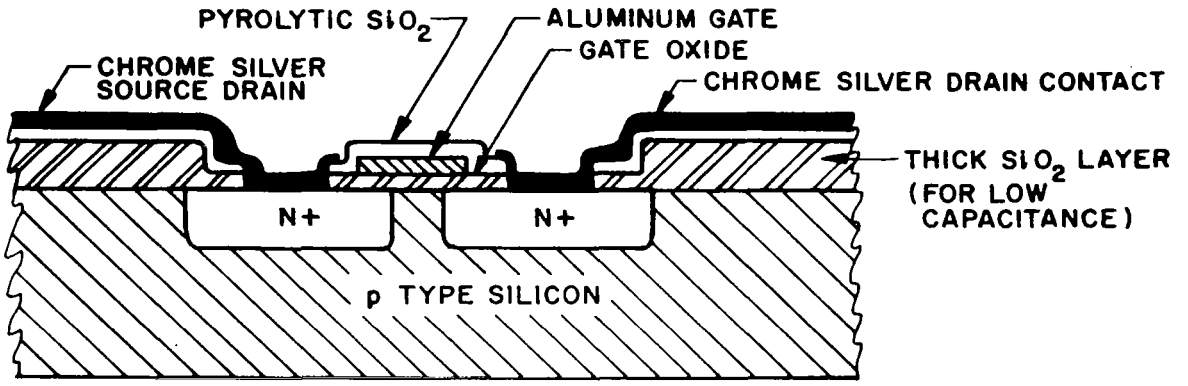


Figure 2. Schematic cross section of a word-driver transistor.

In the top view of Figure 3, six transistors of the 64-transistor strip are shown. The transistors are on 0.010-in. centers and occupy a strip with a width of 0.040 in. With contact areas included, the width of the strip is 0.072 in. The width of the gate metallization is 0.0005 in. and the underlying channel length is 0.0003 in. The sources are all connected together by a common source bar, insulated from the underlying gate connections by a deposited silicon dioxide layer, 3000 Å thick.

Typical I-V characteristics for the word-driver transistors are shown in Figure 4. The drain current at a drain voltage of 4 V and zero gate voltage is about 17 mA corresponding to a moderately depletion-type transistor. With -3 V on the gate, the drain current is reduced to a few microamperes.

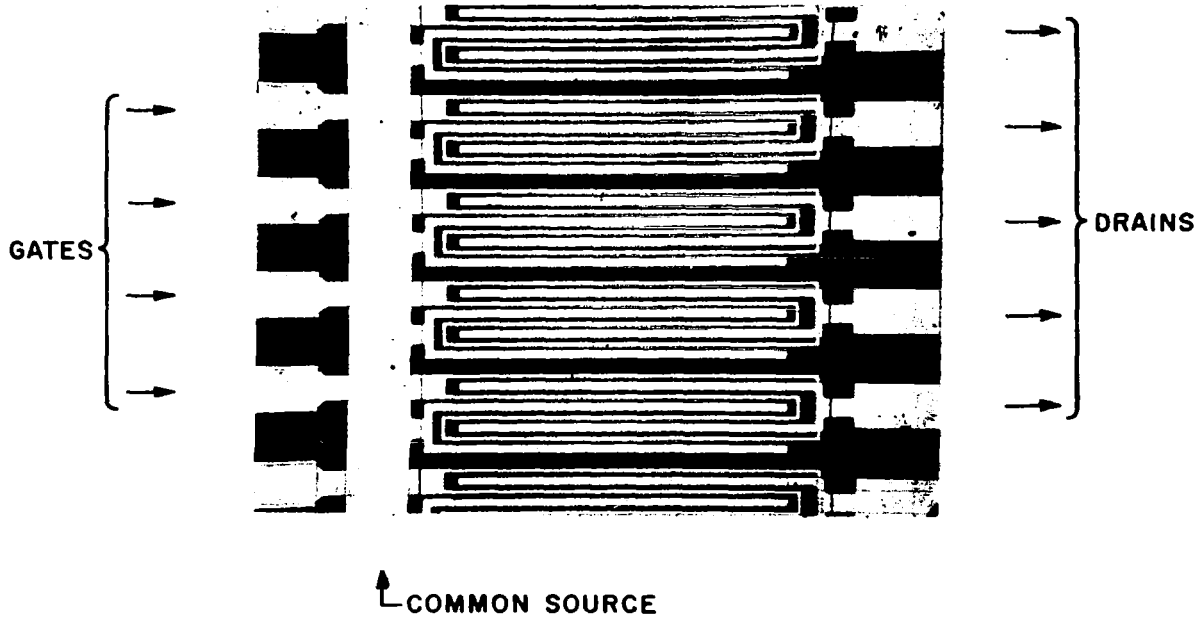
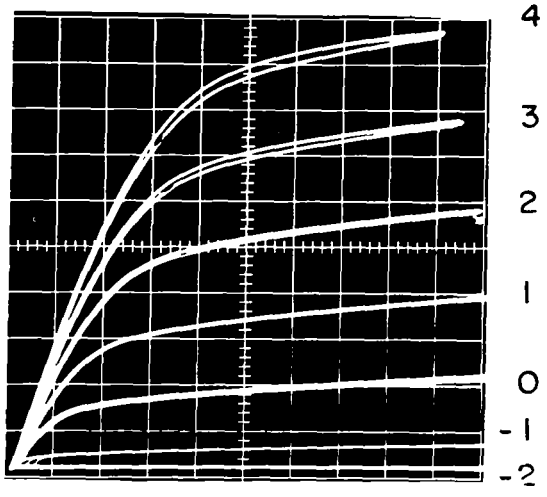


Figure 3. Top view of part of word-driver strip (six transistors).



VERTICAL, DRAIN CURRENT – 20 mA/div
HORIZONTAL, DRAIN VOLTAGE – 1 V/div
PARAMETER, GATE VOLTAGE – 1 V/step

Figure 4. Typical current-voltage characteristics of word-driver transistor. Substrate connected to source.

A complete word-driver strip is mounted in a plastic or glass frame with 132 leads as shown in Figure 5. The frame dimensions are 0.94 in. x 0.32 in., not counting the leads. The connections are made by a solder-reflow technique using a double probe welder and pure tin as solder.

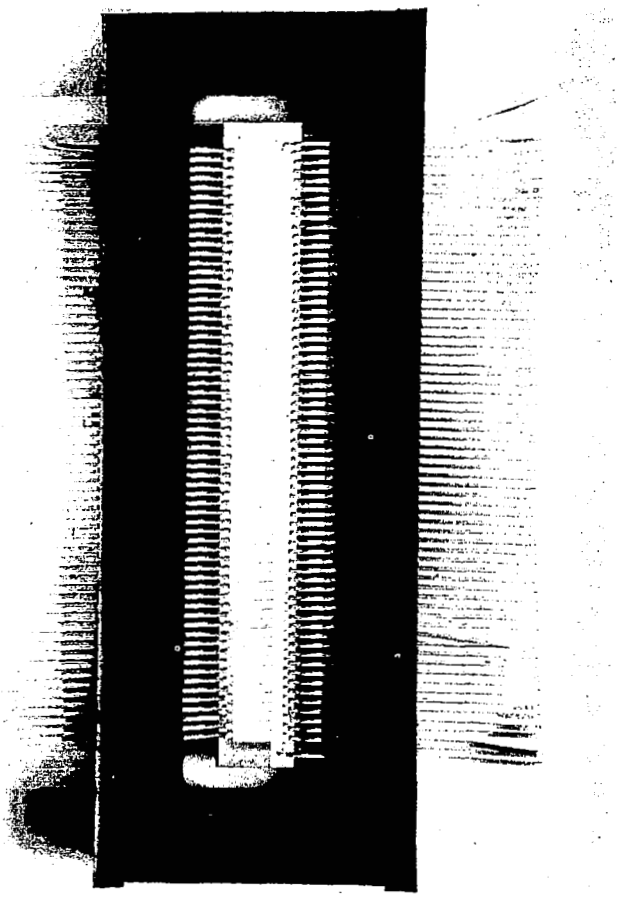


Figure 5. 64-transistor word-driver strip mounted in frame.

A word driver is mounted on a circuit board, as shown in Figure 6, together with a ferrite array mounted in a frame, again by using the same technique of solder reflow. The ferrite array in the frame, and also the other driver circuits, are mounted in similar frames that allow a certain amount of interlocking to accommodate the entire system.

The general memory system approach has been retained through the contract period, and the work has concentrated on the bottlenecks of the technology, which may be understood against the background of this summary.

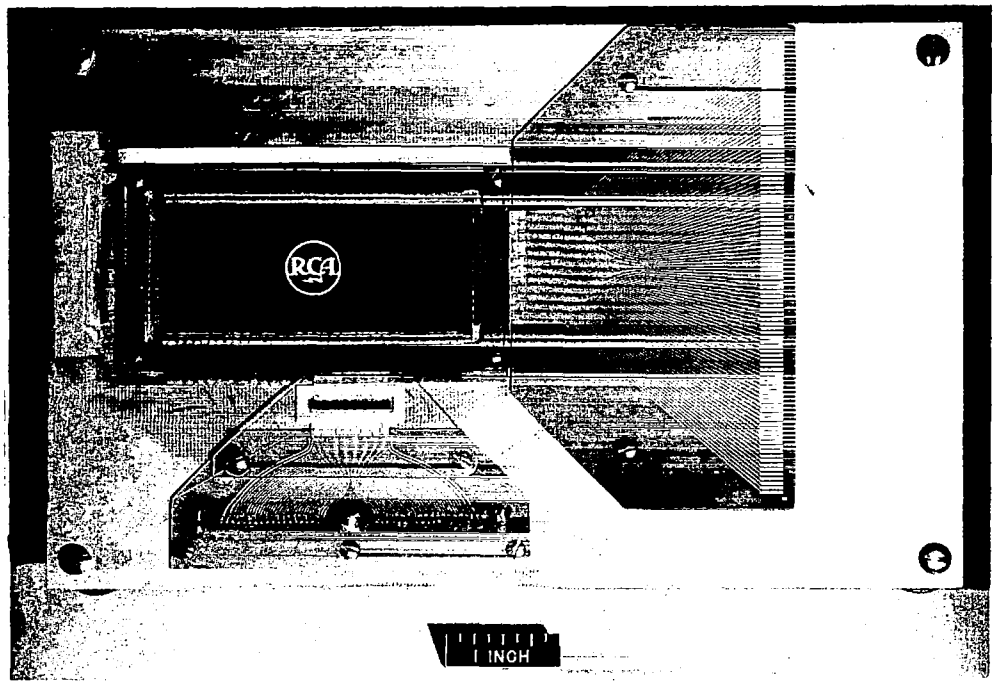


Figure 6. Preliminary systems test vehicle encompassing laminated ferrite frame and word-driver strip.

The Contact Metallization. -- Considerable effort has been devoted to the development of contact metallization which would provide good ohmic contacts to the electrodes, allow the relatively high peak currents (0.1 A for the word driver) without excessive voltage drop, not give pinhole short circuits through the various insulating layers either by itself or by the method used in depositing the layer, be compatible with the solder-reflow soldering technique, and finally provide sufficient life and stability characteristics. During the fourth quarter, this work has matured, and a reasonably complete picture of the stability of silver metallization has emerged. A practical method of stabilizing such layers without jeopardizing the other desirable characteristics, particularly the solderability, has been found in an overlay method using chromium and silicon dioxide. The account of this work follows in Part II of this report.

Circuit Encapsulation and Passivation. -- The circuit life characteristics have met three different limiting phenomena during the course of the contract. The first is the now well-known instability of the thermal oxide gate insulation, on which considerable work has been done elsewhere at these Laboratories.

A complete report on this work is being published elsewhere.*[1] Drawing upon the results of this work it is believed that sufficient stability can now be obtained by relatively simple changes in the processing of the circuits, mainly in sufficiently clean methods for growing the thermal oxide and depositing the gate metal layer. During this contract, the clean oxide conditions described in the paper[1] have been used during the third and fourth quarters, while the clean metallization, also described in the paper, has been introduced on a preliminary basis during the latter part of the fourth quarter. The results closely duplicate the results reported.

The second limiting phenomenon has been the instability of the chromium-silver source-drain metallization. This has been overcome as described in detail later in this report.

The third limiting phenomenon has been the sensitivity of the driving circuits to mechanical and chemical abuse during use in laboratory ambients, and in testing and handling. For this reason, a surface passivation method has been tried out and tested in preliminary accelerated life tests, and a plastic package has been designed and tested, although as yet only in very preliminary fashion. This work is also described in detail in Part II of this report.

Deposited Crossover Insulation. -- One of the essential features of these circuits, as with most integrated circuits containing a large number of units, are the multilayer connections, in this case two layers. In one of the methods used for such multiple-layer interconnections silicon dioxide is deposited at relatively low temperature (300 to 500°C) by decomposing silane. While this method is easy to apply to small-area crossovers over an essentially flat surface, it becomes very difficult to use in large-area crossovers, particularly when the surface contains steps over which the crossover must go, because of the probability of pinholes in the insulator. Considerable work has been done to perfect the method of laying down a layer with low pinhole probability. The crossover fabrication procedure is described in more detail in Appendix B.

Silicon Nitride as a Gate Insulator. -- Silicon nitride with a bulk dielectric constant of 9 is basically superior to silicon dioxide with a bulk dielectric constant of 4 as a dielectric layer for the gate region. However, another necessary requirement of the gate insulator is that the charge in the insulator or at the interface can be controlled at sufficiently low values. In preliminary experiments this was not achieved.

Silicon nitride layers, 2000 Å thick, were deposited on MOS word-driver transistors. A heavy inversion layer resulted in a drain current of 500 mA at zero gate voltage. This current is too large to cut off with a reasonable gate voltage.

Silicon nitride layers were also used in MOS capacitors. On 10 Ω-cm p-type material the flat-band voltage is between -1 and -2 V. Under 300°C ion drift conditions no positive or negative ion drift occurred. Instead, electron and hole traps were formed close to the silicon nitride-silicon

* Literature references are indicated as superscripts in this report.

interface. Inasmuch as more work is required to obtain satisfactory silicon nitride techniques, this work was curtailed.

Device Yield in Fabrication. -- The present status of the fabrication technology is best summarized by Figures 7 through 9 which show a detailed breakdown of the yield situation for the last 20 word-driver strips fabricated. Figure 7 shows overall views of two complete wafers, each with ten driver strips of 64 transistors. While good transistors are represented by blanks, each faulty transistor has been marked according to a simple code which indicates the type of fault. In addition, for each strip the number of good units is indicated, as is the maximum spread in drain current within the strip. On each wafer there is a systematic variation of the drain current which has been indicated by equi-current contours. The reason for the current variation is related to the difference in processing experienced by the various parts of the wafer.

Gate short-circuits have been the most prevalent failure mechanism; in earlier units this occurred through the silicon dioxide crossovers, but in the units shown in Figure 7 this occurred through the thermal gate oxide. The next most prevalent failure mechanism has been series resistance in the source-drain contacts, possibly caused by insufficient removal of oxide at the contact areas. The dominance of these two failure mechanisms suggests that high yield could be reached if these are eliminated.

Another aspect of yield, the uniformity of electrical characteristics of the transistors, is illustrated in Figures 8 and 9. Figure 8 shows the drain current measured at a drain voltage of 4 V and zero gate voltage for the best strip obtained, in which all 64 transistors are good. Figure 9 shows results on a more typical strip for two different gate voltages. The uniformity of current, as judged from preliminary systems tests, is probably higher than necessary. The results of the circuit tests are shown in Appendix C.

A further aspect of yield, not borne out by these initial measurements, is the fact that in preliminary system tests a few transistors developed gate short-circuits. Inherent weak gate insulation is believed to be the reason. On this basis a certain amount of stress testing is being introduced prior to systems packaging.

The total yield based on the last two wafers as deduced from Figure 7 is 5%. However, if the slight complication of mounting half-strips encompassing 32 consecutive good units side by side is accepted, the total yield would be 30%.

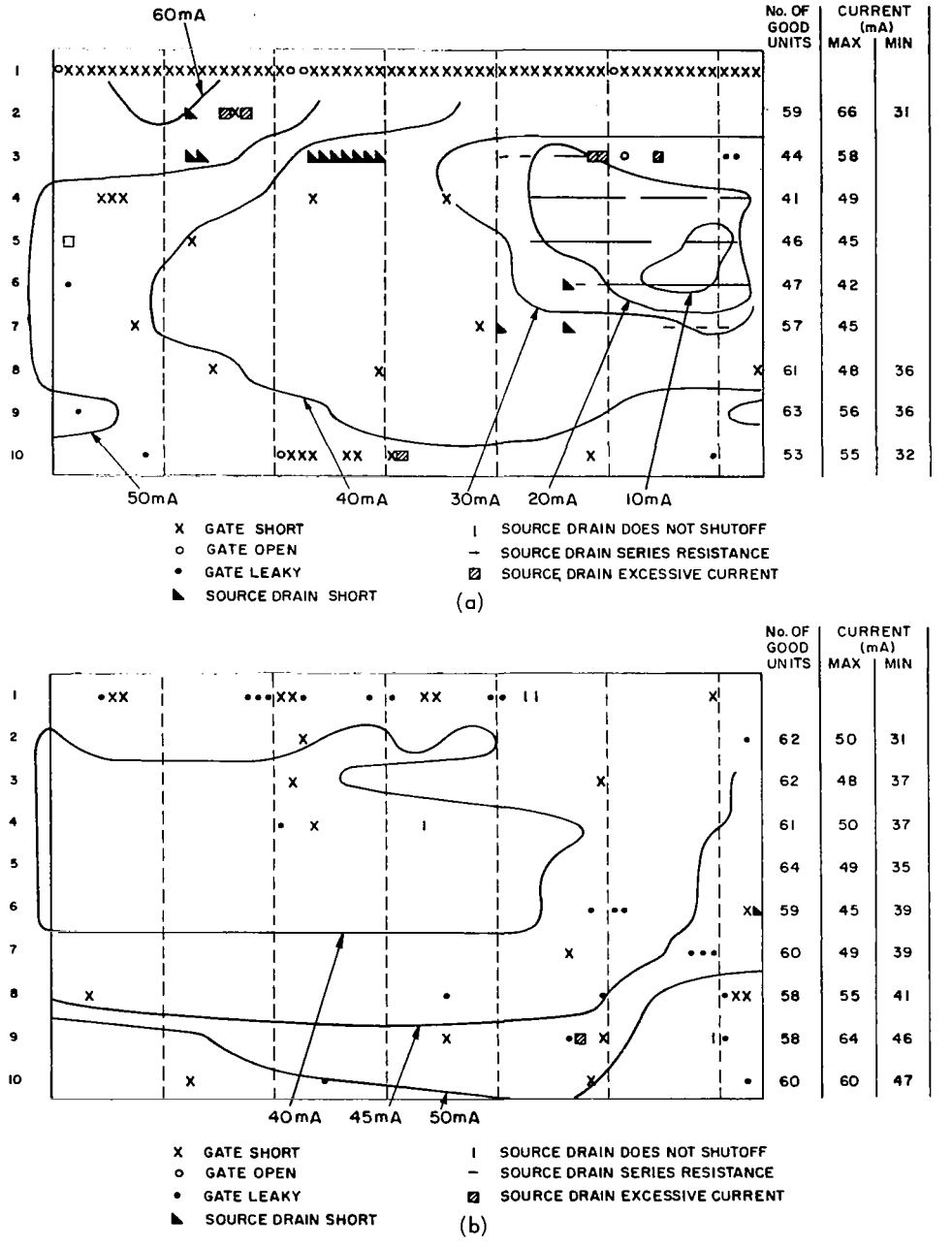


Figure 7. Picture of entire wafer, each with 10 driver strips, and each driver strip with 64 transistors. Defective units are indicated. Contours show equal drain current at V_{SD} = 4 V, V_G = 0 V. Number of good units per strip and the maximum and minimum drain current for each strip are given to the right.

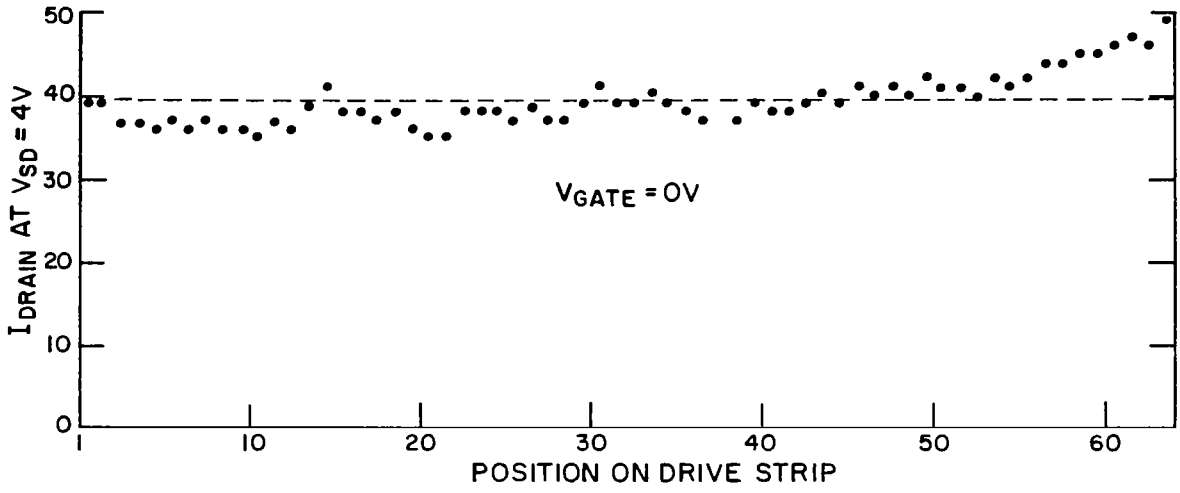


Figure 8. Drain current at V_{SD} = 4 V and V_G = 0 V for driver strip with 100% good units. Maximum deviation is $39 \pm \frac{9.7}{4.3}$ mA.

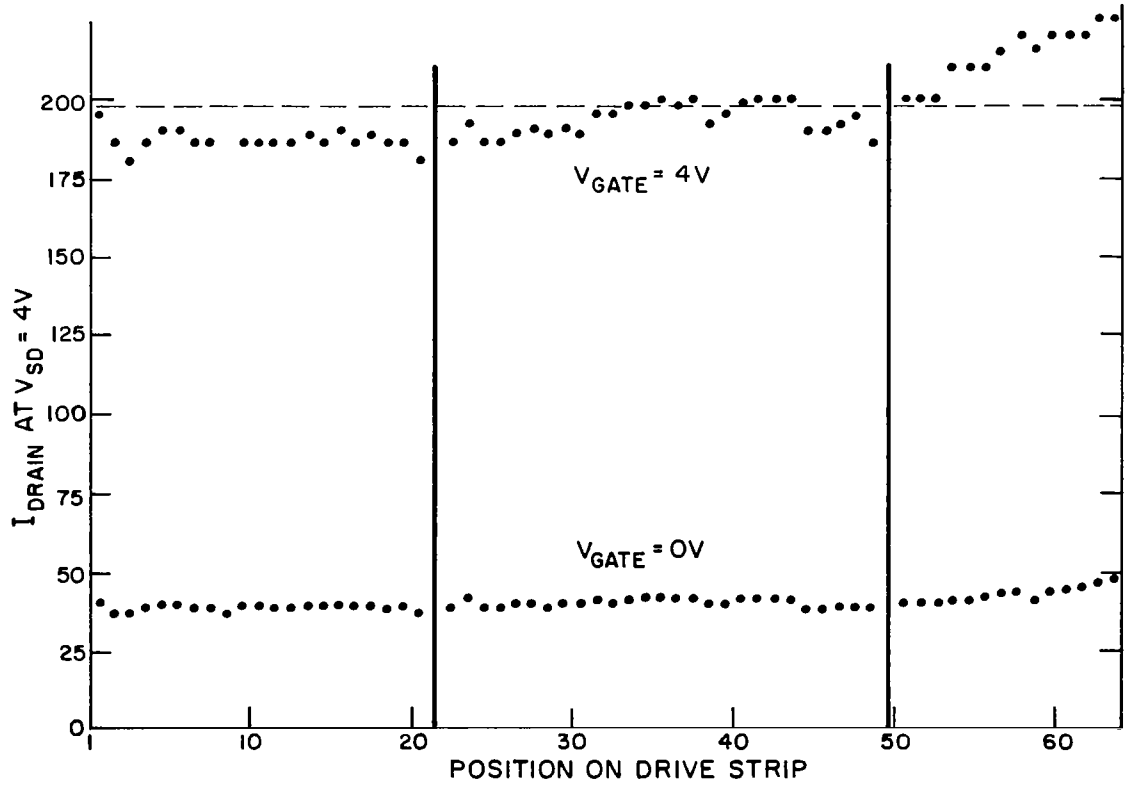


Figure 9. Drain current at V_{SD} = 4 V, and V_G = 0 V and 4 V for typical driver strip. Two units indicated by vertical bars have gate short circuits.

PART II

PREVENTING DETERIORATION OF CHROMIUM-SILVER METALLIZATION ON SILICON DEVICES

Introduction

During the development of new integrated circuits containing two dissimilar materials, silicon and ferrite,[2,3] it became necessary to provide solderable contacts to join the silicon-based devices to the ferrite matrix. A very desirable contact material for soldering, which is compatible with silicon technology, is silver. Such contacts, fabricated by chromium-silver metallization, have been used in experimental devices.* One drawback is their tendency to deteriorate after only few months under laboratory conditions. A typical picture of such deteriorated contacts on experimental MOS field-effect transistors in an advanced stage of deterioration is shown in Figure 10.

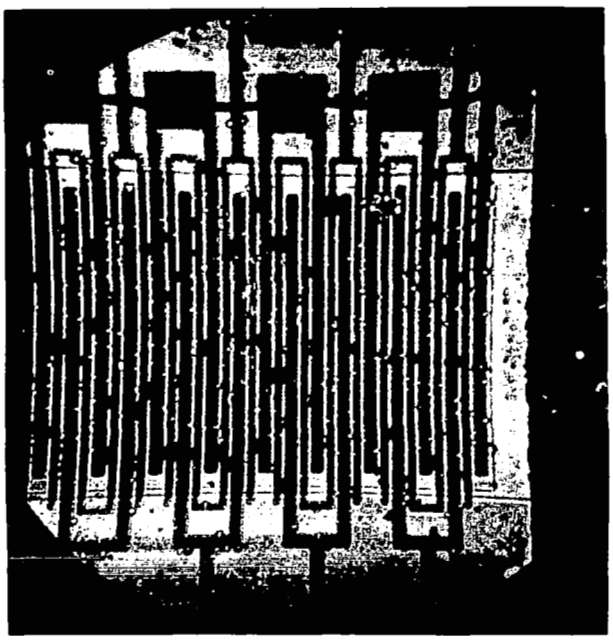


Figure 10. Experimental MOS field-effect transistor showing advanced deterioration of chromium-silver metallization on source and drain.

The work reported here encompasses the identification of the mechanism responsible for this deterioration and a practical method of eliminating it. The report is divided in two parts. Part A. is qualitative, containing a

* W. Triggs, RCA Electronic Components and Devices, Somerville, N. J., personal communication.

description of the physical phenomena, interpretation of experiments performed and results. Part B. is quantitative, forming the basis for the first part.

A. Qualitative Analysis of Contact Deterioration

Fabrication of Chromium-Silver Contacts. -- Before application of the chromium-silver contacts, the source and drain regions of the MOS field-effect transistors have been opened by the usual photoresist technique, whereby the silicon oxide has been removed, leaving bare silicon. In the removal procedure -- in the etching and washing in distilled water and in exposure to the ambient -- the bare silicon surface is re-equipped with an "oxide" layer about 10 to 30 Å thick. Thereafter, the silicon slice is inserted in a vacuum, and chromium and silver are evaporated onto it. Actually, it would be desirable to make the contacts entirely of silver, since the conductivity of silver is higher than that of chromium. However, it is found in practice that silver does not adhere sufficiently well to the surface. Therefore, a layer of chromium, which adheres very well to both silicon and its oxide, as well as to silver, is introduced between the silicon substrate and the silver layer. The procedure is to evaporate about 200 Å of chromium, then about 200 Å of chromium and 600 Å of silver simultaneously, and finally about 2000 Å of silver. The mixture of the two metals ensures mechanical as well as interatomic bonding between the two layers. Electrical measurements of the devices show good ohmic contacts with no sign of interface resistance.

Effects of Contact Deterioration. -- The three most obvious effects of contact deterioration are: (1) a gradual appearance of nonlinear series resistance at the metal-silicon interface, (2) a visual change of the structure of the metal layer, and (3) a reduced adherence of the layer to the substrate. In the final stages, electrical contact to the silicon is lost, and the metal layer breaks up into small granules, which may even appear outside the area originally occupied by the metal. The electrical change is shown in Figure 11, which shows the I-V characteristics of two representative MOS field-effect transistors. The original characteristics are shown in Figure 11(a). Figure 11(b) shows the characteristics of the same two transistors after being heated in air for 15 minutes at 350°C.

The third effect of the contact deterioration is a reduced adherence of the metal layer to the silicon. Figure 12 shows scraping tests on two samples of evaporated chromium-silver strips on heavily n-type silicon. The strip in Figure 12(a) is shown as it comes from the metallization process while the strip pictured in Figure 12(b) has been treated in air at 475°C for 25 minutes. Both strips have been scraped with a knife. While the metal layer adheres very well in the unheated sample, the metal layer on the heated sample can be easily removed by scraping.

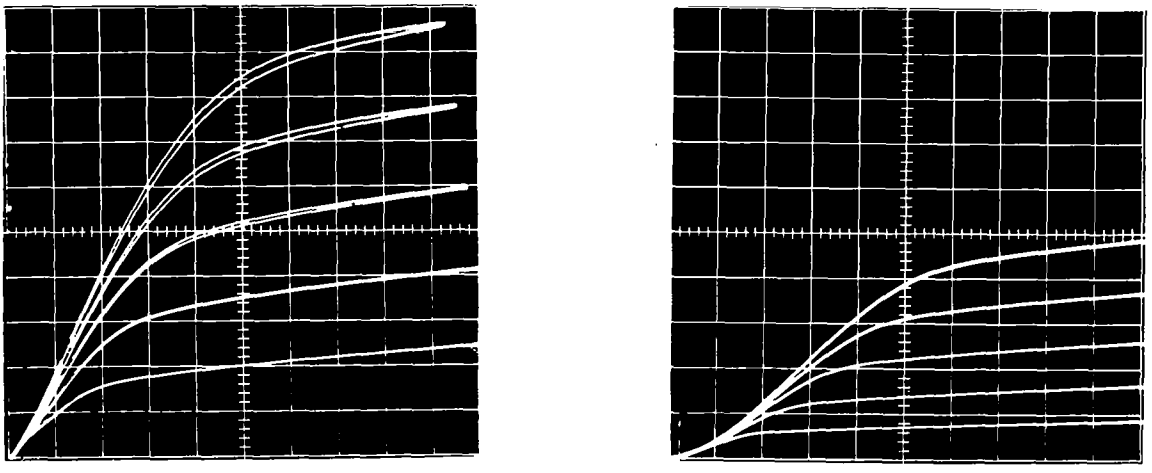


Figure 11. Drain current-drain voltage characteristics of MOS field-effect transistor showing change by contact deterioration. Parameter is gate voltage. (a) Before deterioration. (b) After being heated to 350°C in air for one hour.

Physical Process Responsible for the Deterioration -- Figure 13 shows several transistors with chromium-silver metallization for the source and drain contacts and with aluminum for the gate contact; the transistors have been heated in air at 350°C for one hour (the aluminum gate has not deteriorated). The appearance of the metallization suggests that the silver atoms have moved over the surface and agglomerated at nucleation centers where droplets have formed. It appears that the thermal energy imparted to the silver atoms is sufficient to break the bonds between some of them, leaving them free to migrate about the surface. If the silver atoms were free to migrate, it would be natural that the very large stored surface energy in the thin silver layer caused by surface tension would be released and the system would move toward a state of lower stored energy in which the silver would form a number of spheres (ideally one sphere where the surface energy would be minimum). The location of a sphere would then be governed by energy consideration similar to nucleation of crystal growth, and the balls might be expected to form at surface defects.

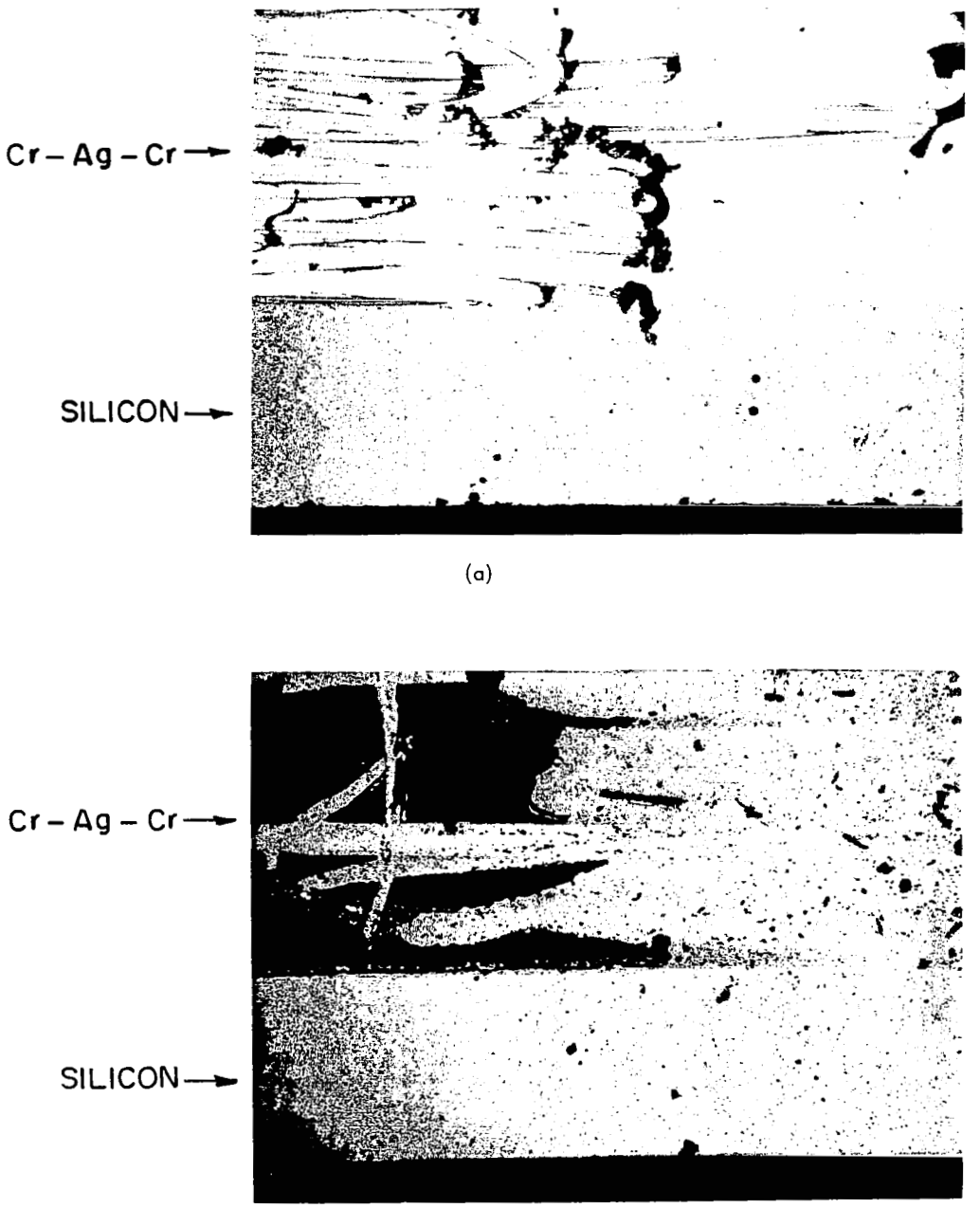
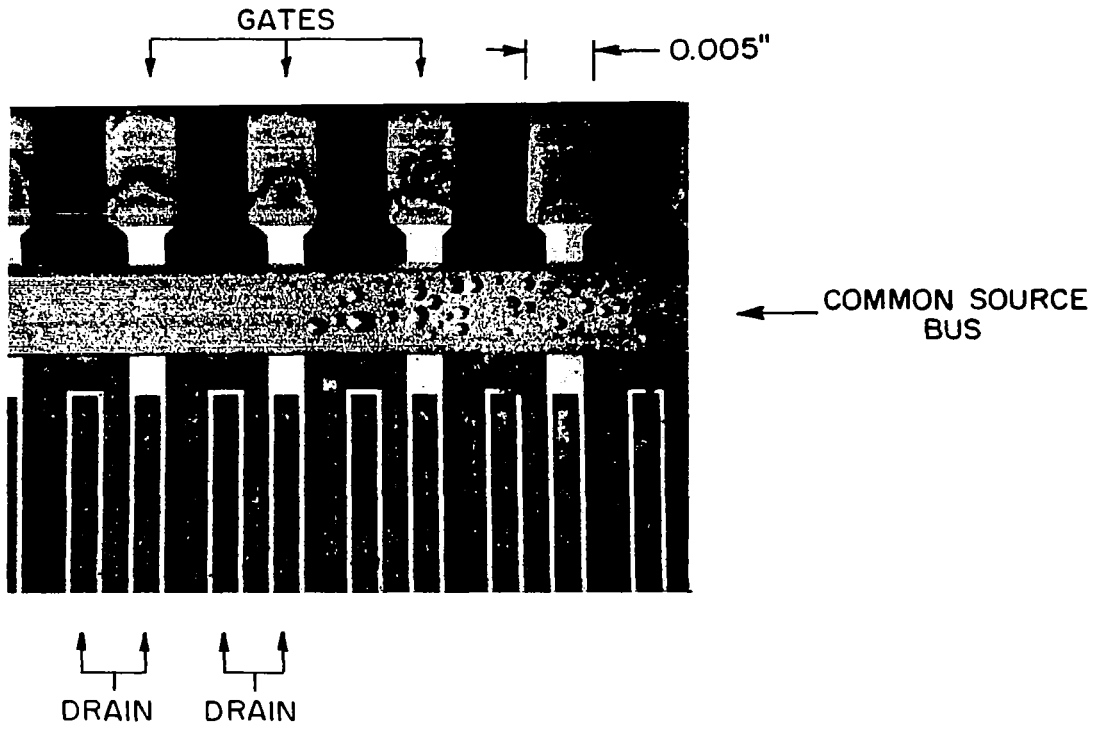
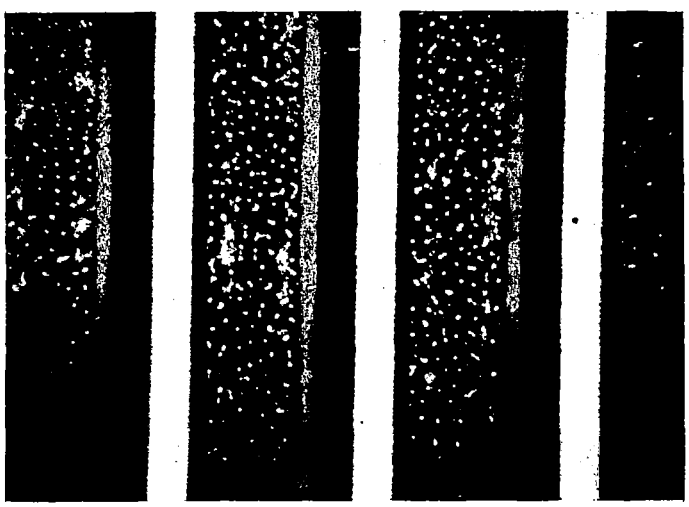


Figure 12. Chromium-silver strips on heavily doped n-type silicon after having been scraped with a knife. (a) Before deterioration. (b) After deterioration by heating to 475°C in air for 25 minutes.





(b)

Figure 13. MOS field-effect transistor with chromium-silver metallization for source and drain contacts, aluminum for the gate. The transistor has been heated at 350°C in air for one hour.

To verify the above hypothesis samples of chromium-silver strips on silicon were prepared in the same manner as the contacts to the transistors were prepared. The surface of the silicon [(100) orientation, 10 Ω-cm, p-type] was doped in a phosphorus diffusion furnace to degenerate n-type material in the same manner as when the source and drain regions were formed. The metal layers were evaporated as previously discussed, and the strips were defined by photoresist techniques.

The strips were then heated in air at various temperatures for different periods of time, and their resistance was measured after each heating period. To simplify the testing no attempt was made to measure the direct contact resistance between the metal layer and the silicon. The resulting data, which show the manner in which the resistance of the strips changed with time at a particular temperature, are given in Figure 14. From these data an activation energy of 0.9 eV is derived as described in Part II-B. This is a reasonable figure as shown by the following considerations. It is well known that the activation energy for movement of silver atoms over a single-crystal silver surface is 0.45 eV.[4] The activation energy for silver atoms moving over a silicon surface (111) has been given as 0.71 eV.[5] A slight increase above this value may be attributed to the thin chromium layer, the function of which is to increase the bond strength to the silicon surface. A summary of pertinent activation energies is given in Table I.

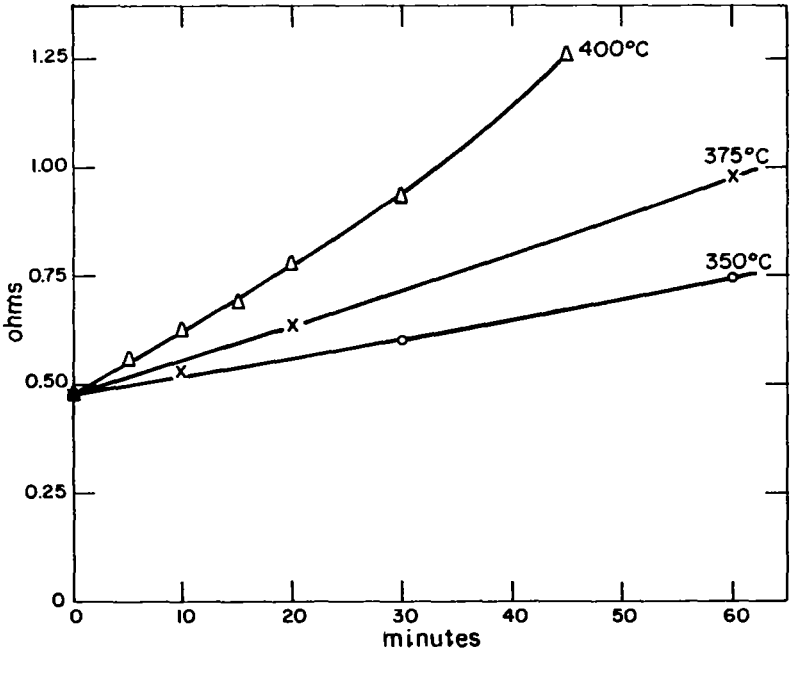


Figure 14. Resistance versus time of four strips of chromium-silver on silicon which have been heated at 350°, 375°, and 400°C. The resistance measurements are made at room temperature.

TABLE I

PERTINENT ACTIVATION ENERGIES FOR SILVER MIGRATION

Substrate and Overcoat (if any)	Diffusion Path	Temperature Range Used (°C)	Activation Energy (eV)	Reference
Ag Single crystal	Surface	225 - 350	0.45	4
Ag Polycrystalline	Grain Boundary	375 - 500	0.88	4
Ag Single crystal	Bulk	500 - 950	1.98 -2.18	4
Si Single crystal (100)	Surface	300 - 1000	0.71	5
Si + Cr Single crystal (100)	Surface	300 - 400	0.9	This Work
Si + Cr Single crystal (100) Cr overcoat	Interface or Penetration	400 - 500	1.4	This Work
Si + Cr Single crystal (100) Cr + SiO_2 overcoat	Interface	400 - 500	> 1.4	This Work

In some cases, although not on the strips in this experiment, an initial small reduction of a few percent of the resistance was observed during the first minutes of heating, interpreted as a sintering of the layer.

The migration of chromium, on silicon, can be ruled out by the following considerations. Chromium atoms present on the surface are very active chemically and in contact with the ambient form chromium oxide, Cr_2O_3, in a well-known passivation reaction. The energy of formation of Cr_2O_3 is high, 11.5 eV, so that the molecules would be stable at the temperatures used here. The movement of the oxide molecules is much less probable than movement of silver atoms because of their large mass.

The decrease in adherence of the silver layer with time is consistent with the hypothesis of silver migration and surface tension. When the silver surface is reduced by the balling of the silver layer, the mechanical joint obtained by coevaporation of chromium and silver is severed. The silver layer pulls away from the very irregular chromium layer, forming drops resting on

the top of the highest parts of the chromium. With the mechanical bond gone the only bond remaining is the intermetallic one between silver and chromium atoms over part of the area. Thus, the adherence is greatly reduced. A further contributing factor may be oxidation of the chromium. The reduced mechanical contact would give easy access for oxygen along the interface. The adherence of silver to chromium oxide would be weaker than the metallic bond to chromium metal.

The conclusion to this experiment then is that the evidence supports the view that silver migration is responsible for the deterioration of chromium-silver contacts. Further evidence related to surface tension follows.

Protection by an Additional Chromium Layer. -- Once the deterioration mechanism was understood it was also clear how the deterioration could be reduced. If the migration of silver is indeed one of surface diffusion, with silver atoms jumping from bond to bond on the surface, then their movement could be hindered by covering the surface with another layer, forcing the silver atoms to move not on a free surface but along the interface between the two layers. A suitable layer existed in the form of silicon dioxide deposited by decomposing silane at a moderate temperature.[6] However, at the temperature used, considerable deterioration took place before enough cover had been deposited to prevent deterioration. Therefore, the expedient of using an intermediate layer of chromium deposited at room temperature to protect the silver layer during application of the oxide cover was resorted to. Also, the adherence of the oxide overcoat to the silver layer would be increased by the additional chromium layer between the two.

A chromium layer that is too thin is not continuous, and therefore little effect can be expected. On the other hand, a layer that is too thick interferes with soldering. The first step was to investigate the influence of this additional chromium layer without the oxide overcoat. The second chromium layer was deposited in the same manner as the first, i.e., by following the deposition of the 2000-Å silver layer by a thin layer of about 800 Å of chromium and silver deposited together, and then a 200-Å chromium layer on top.

A number of metal strips on silicon were again prepared, this time with the chromium-silver-chromium structure, but otherwise similar to the ones described earlier. The strips were then heated at various temperatures in air. The results are shown in Figures 15 and 16.

It appears that the deterioration now proceeds in three distinct stages. The first stage is characterized by a relatively small increase in resistance with time. In the second stage, a plateau is reached where the resistance remains approximately constant. As the temperature is increased the rate of rise increases and the plateaus appear at lower values of resistance. The first and second stages are illustrated in Figure 15.

Because of the few points on the curves near the origin, the initial part of the 500° curve has been drawn free-hand. The values deduced from this plot for the activation energies of the first stage and the third stage of deterioration are 1.4 eV and 0.8 eV, respectively.

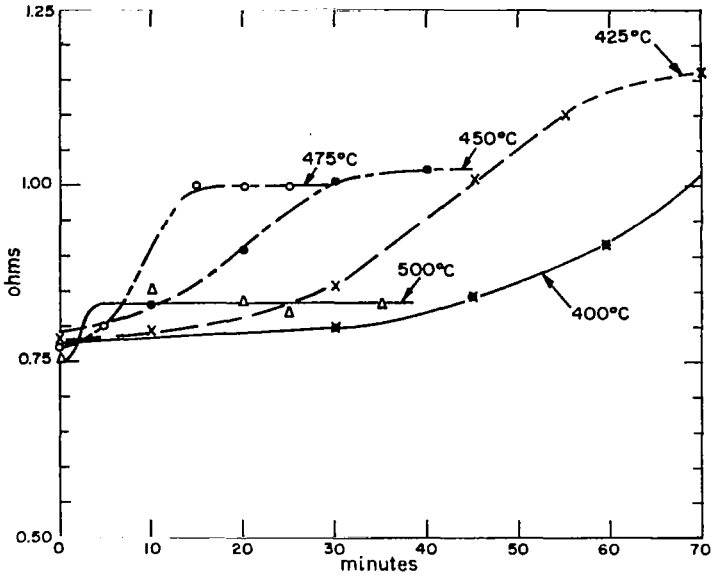


Figure 15. Resistance versus time of four strips of chromium-silver-chromium which have been heated to 400°, 425°, 450°, 475°, and 500°C. The resistance measurements are made at room temperature.

The interpretation of these results is as follows. During the first stage, the migration of silver is hindered by the overlying layer of chromium, forcing the silver to follow the interface between the two, or to penetrate the layer which is extremely thin and therefore not completely continuous. It is known that the activation energy of silver moving on the surface of silver is 0.45 eV, but on grain boundaries between crystals in polycrystalline silver it is 0.88 eV, an increase of 0.43 eV. It is therefore reasonable to assume that the activation energy for silver moving on (chromium) silicon, 0.9 eV, should increase to about 1.4 eV by a covering layer which would force interface migration or migration through the layer.

The second stage of deterioration where the resistance reaches a limiting value requires a more detailed discussion. A simple explanation might be that the contact to the underlying silicon has changed, so that the metal strip is shunted by the resistance through the heavily doped silicon substrate which would be constant. To test this, the center third of the strip of one of the metal strip samples, in which the resistance has saturated at about 1 Ω, was removed by scraping it off the silicon with a sharp tool. The resistance measured between the two end contacts was now approximately 50 Ω which is within a factor of two of the calculated resistance of the silicon slab. This resistance is too high to be responsible for the plateau.

Instead, the explanation appears to be the following. When the silver layer "balls up" two competing processes set in. One process is the arrival at a particular ball (or droplet) of silver atoms through random migration

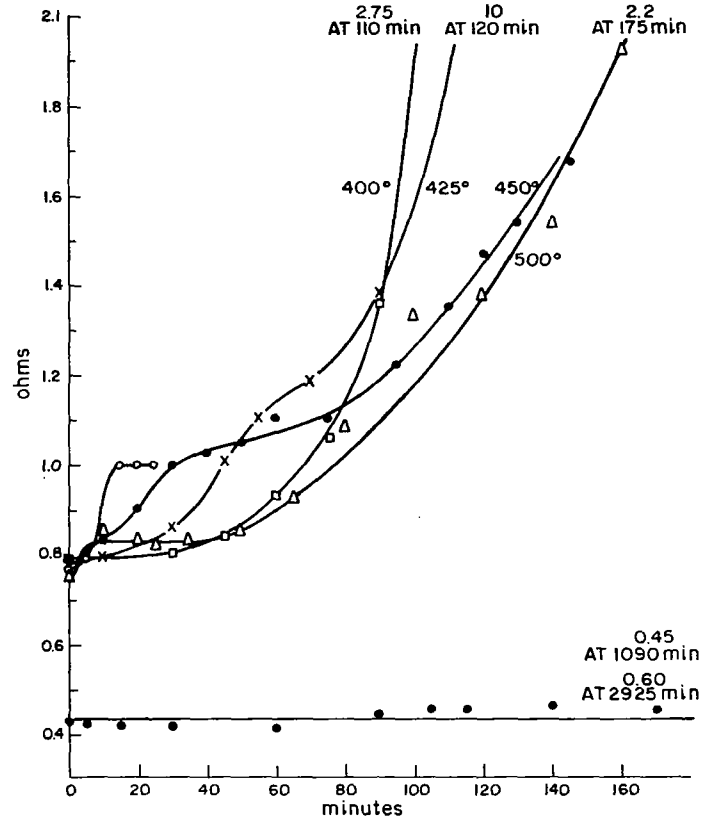
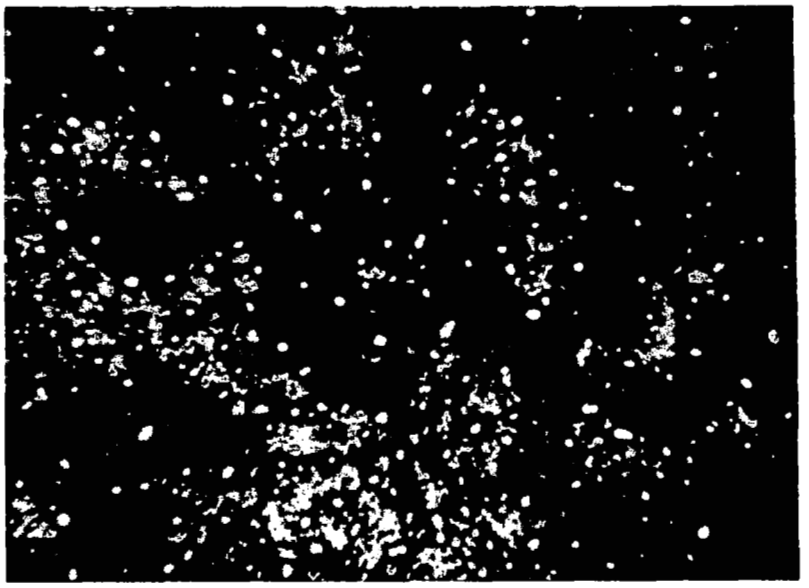


Figure 16. Resistance versus time of the same strips as in Figure 6, but extended to longer time. Strip at 350°C from different batch.

across the surface where they are "swallowed up" and incorporated in the ball. The other process is the escape from the ball of silver atoms which have acquired sufficient thermal energy. In leaving the ball, the atoms have to overcome the barrier at the surface of the ball represented by surface tension. Typical pictures of the surface are shown in Figure 17.

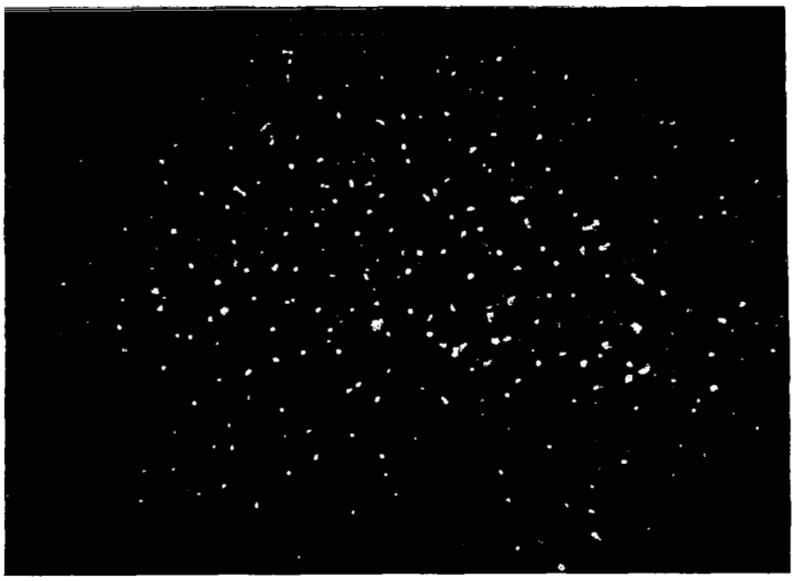
After the plateaus have been reached a third stage comprising a further increase in resistance takes place, which proceeds until the layer becomes discontinuous and the resistance goes to infinity. This is illustrated in Figure 16.

In this final third stage, the silver layer is starting to break up and the activation energy for surface diffusion therefore has decreased (for diffusion over the bare spots) from 1.4 eV to 0.9 eV. The resistance increase is very slow at low temperature (350°C) because of the slow surface diffusion at that temperature. At very high temperature (500°C), it is also slow because of the reduced surface tension which does not induce the formation of balls as strongly as at lower temperature. Therefore, the deterioration proceeds most rapidly at an intermediate temperature, about 400°C.



(a) Cr – Ag – Cr SAMPLE SATURATED AT 450°C

5μ



(b) Cr – Ag – Cr SAMPLE SATURATED AT 500°C

Figure 17. Enlarged picture of the chromium-silver-chromium strips heated to 450° and 500°C in air. Mean diameters of droplets are 2.0 and 1.6 μm, respectively.

In the presence of water vapor this most sensitive temperature is lowered from about 400°C to about 350°C, indicating that the deterioration is more rapid in moist ambients.

Experimental Determination of the Critical Temperature. -- The fact that, at the critical temperature, the surface tension goes to zero should be observable under the microscope as a disappearance of the balling. On a strip heated at 550°C there was evidence of some balling of the silver layer, indicating that the critical temperature postulated may have been somewhat low. At 650°C however, the balling was absent. At this temperature, the layer still breaks up by the violent motion of the silver atoms but in a mosaic rather than in balls. The layer also retreated from the surface, the oxidation mechanism postulated still being active, but the pattern of retreat was different. As very high temperatures are of interest for the contact problem only as far as the low-temperature phenomena can be scaled for the purpose of accelerated life tests, no further investigations above 500°C were made.

Protection by an Additional Oxide Layer. -- With the additional chromium metallization described in the previous section offering a temporary protection, it is now possible to lay down on the surface an additional silicon dioxide layer by decomposition of silane at moderate temperature. This oxide coat offers the following benefits:

(a) A mechanical protection against surface damage in handling during assembly of the system.

(b) A chemical barrier against the diffusion to the surface of the active region of the transistors of water vapor and other contaminants from the ambient, which accelerate deterioration of the device.

(c) A mechanical and chemical blanket to constrain silver migration.

(d) An electrical barrier preventing electrical charges from approaching too closely to the active region of the transistors.

The deposition of the oxide takes place at 330°C in a special deposition chamber shown in Figure 18. The total time at the high temperature is about ten minutes.

To establish the fact that the oxide cover, apart from the heating effect during deposition, has in itself no effect on the performance of the transistors, the following experiment was performed. The electrical characteristics of several transistors were measured. Then they were covered with several thousand angstroms of SiO_2, the contacts were opened up with photoresist methods, and the electrical characteristics remeasured. The results are shown in Figure 19.

Comparative Evaluation of Protected and Unprotected Transistors. -- Figure 20(a) is a photograph of several transistors with chromium-silver metallization without a further overcoat. Figure 20(b) is a sample from the same

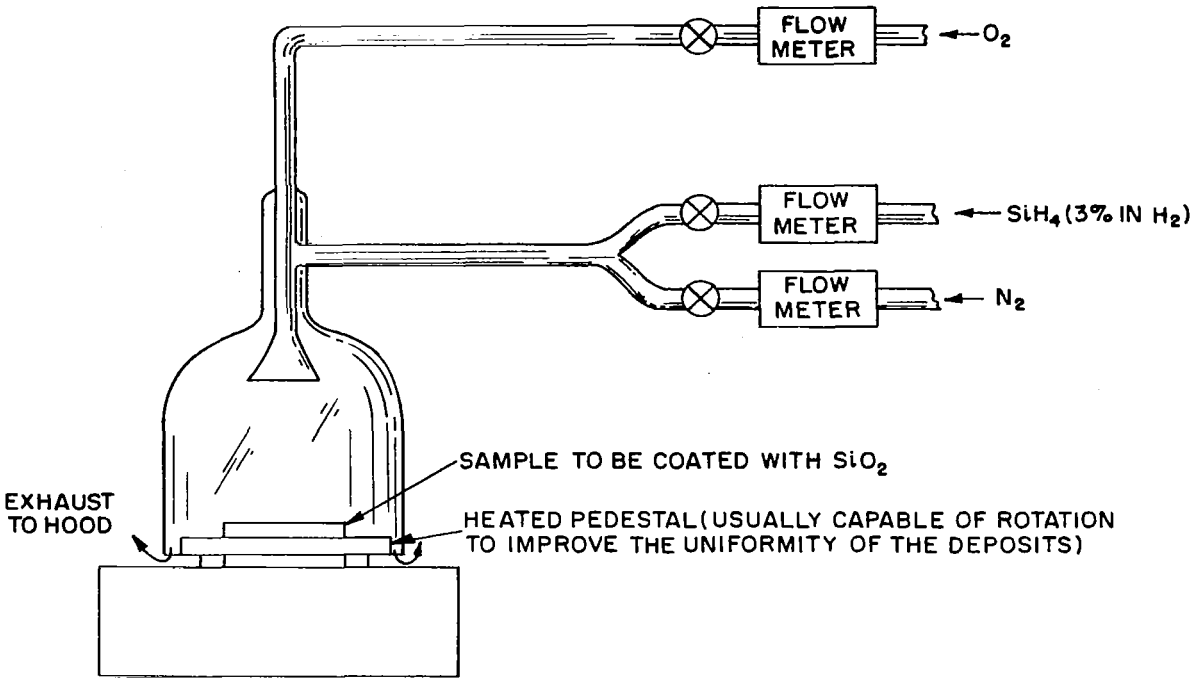
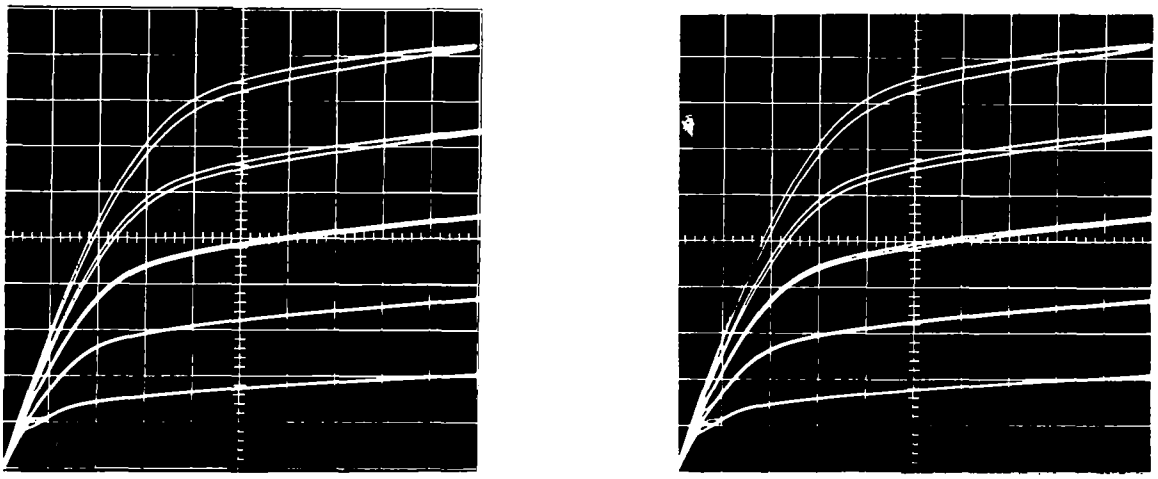


Figure 18. Deposition chamber for SiO_2 deposition. Wafer is heated to 330°C. Silane (SiH_4) and oxygen are introduced at the top, depositing SiO_2 through the reaction $SiH_4 + 2O_2 \rightarrow SiO_2 + 2H_2O$.

wafer which has been covered with a film of SiO_2 to a thickness of about 5000 Å. Note that the slight discoloration of the chromium-silver in areas of Figure 20 indicates that the 10-minute heating cycle at 330°C before the silicon dioxide was deposited was sufficient to initiate deterioration of the contacts. The blisters on the common source bus in Figure 20(b) are not typical and are due to the poor adhesion of a reinforcing layer of chromium-silver applied to the finished units to increase their current-carrying capability. Figure 20(c) is a sample with chromium-silver-chromium metallization which was covered with a layer of silicon dioxide simultaneously with the strip in Figure 20(b). The metallized portions of this sample showed no evidence of deterioration during the glassing operation, as was expected.

Figures 21(a), (b), and (c) show photographs of the above samples after they were heated simultaneously for one hour at 350°C in air. Note that even though the unprotected sample is completely destroyed, the two encapsulated samples show no further signs of deterioration.



(a) Before Glassing

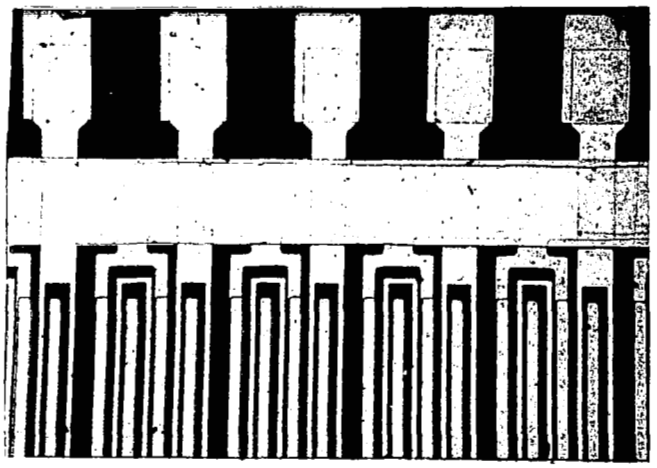
(b) After Glassing & Opening Contact Areas

H = 1V/div
V = 20 mA/div
V_S = 1V/STEP

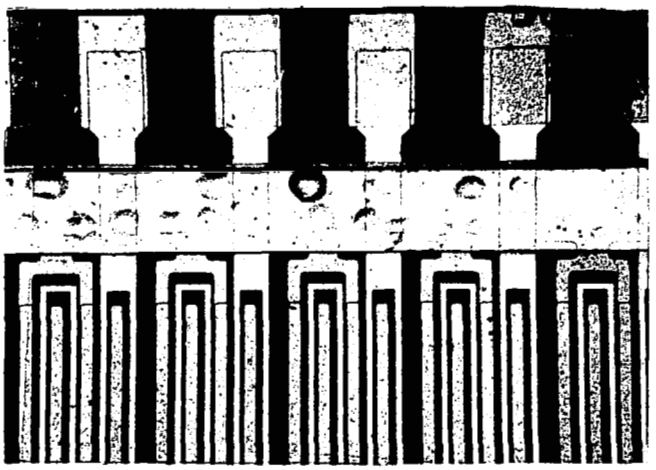
Figure 19. Drain I-V characteristics of transistor with Cr-Ag metallization on source and drain. (a) Before oxide coating. (b) After oxide coating and opening of contact area with photoresist.

Figure 22 shows representative electrical characteristics of two of the chromium-silver transistors shown in Figure 20(b) and 21(b) which were covered with SiO_2. Figure 22(a) shows the original characteristics before they were encapsulated; Figure 22(b) shows the characteristics after one-hour heating cycle and after the contact areas were opened with photoresist techniques. These transistors suffered only a slight shift of their drain I-V characteristics which may be ascribed to a change in interface states at the gate oxide-silicon interface. This phenomenon is not directly associated with the encapsulating silicon dioxide layer. The unprotected transistors were inoperative due to drain contact open circuits.

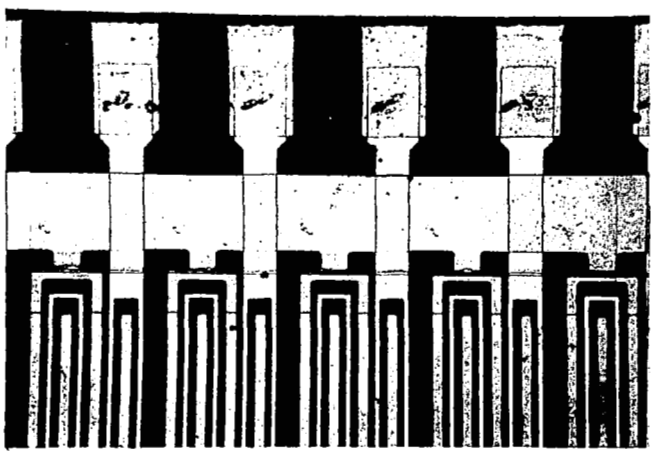
Influence of Water Vapor. -- Water vapor has been found to be a strong agent in the deterioration of many semiconductor parameters. It was found that the addition of water vapor to the ambient greatly accelerated also the deterioration of the metal films. To show the relative protective effects between a thin layer of chromium and a thin layer of chromium with a silicon-dioxide



(a) Cr–Ag

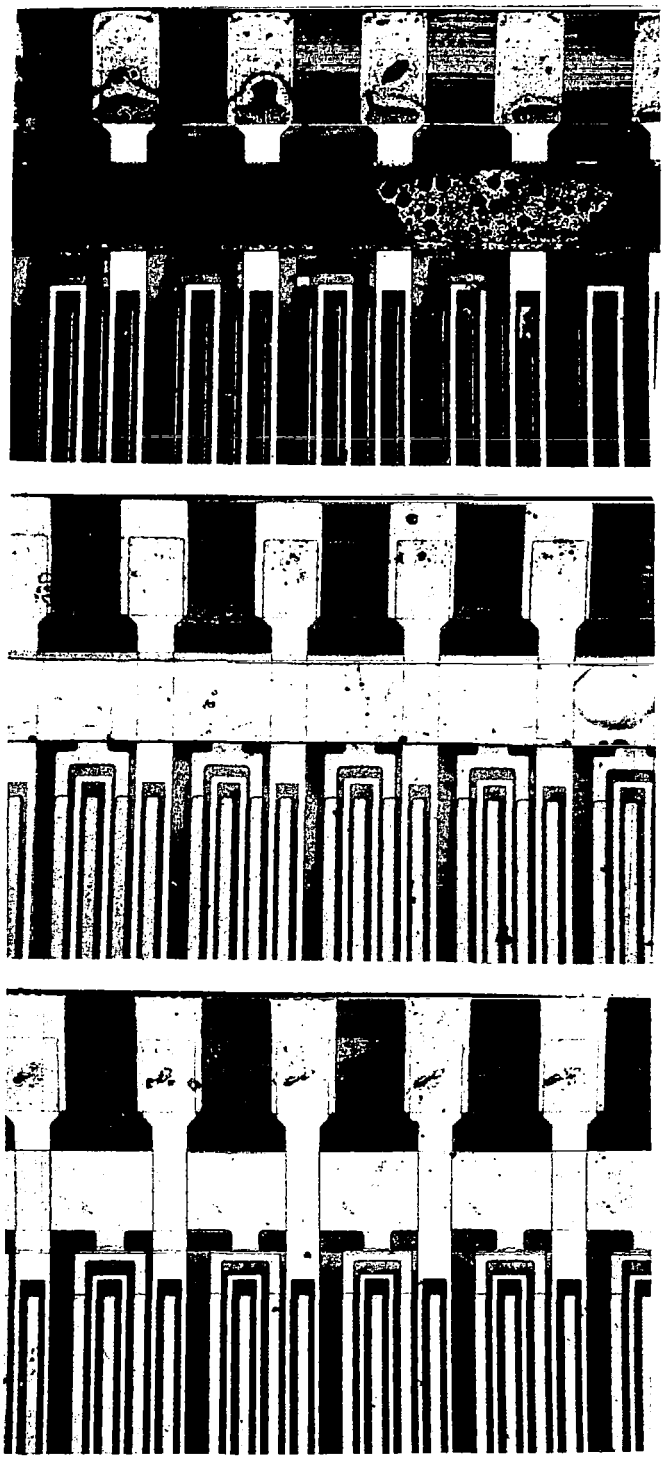


(b) Cr–Ag–SiO_2



(c) Cr–Ag–Cr–SiO_2

Figure 20. Transistors covered with (a) Cr-Ag, (b) Cr-Ag-SiO_2, (c) Cr-Ag-Cr-SiO_2. Note that in (b) the ten-minute heating cycle to deposit SiO_2 has caused lifting of the reinforcing bar and some deterioration of the silver layer.

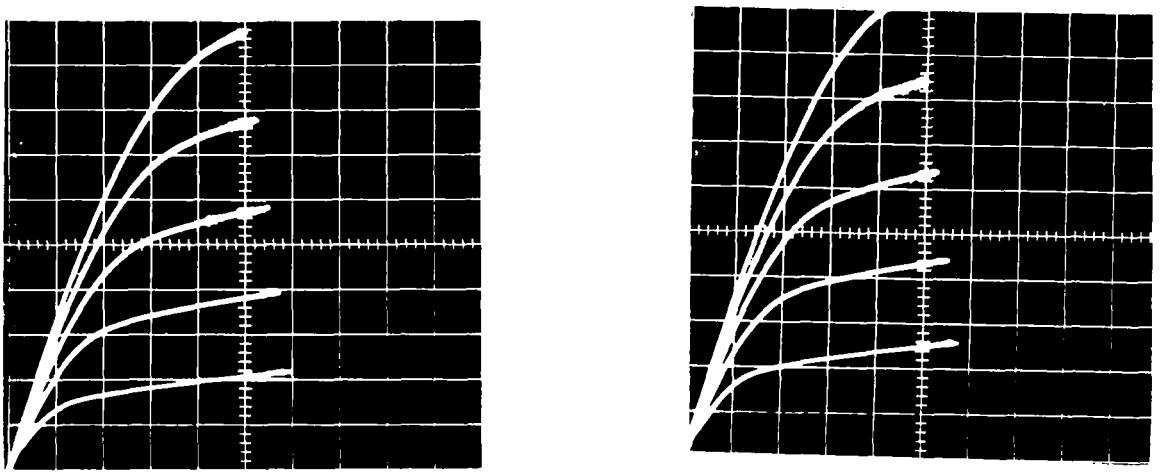


(a) Cr – Ag

(b) Cr – Ag – SiO_2

(c) Cr – Ag – Cr – SiO_2

Figure 21. Same transistors as in Figure 10 after heating at 350°C for one hour in air. The silver layer in (a) severely deteriorated. Unit (b) has not changed much. Unit (c) is unchanged.



(a) Before Encapsulation (b) After Encapsulation

H = 1V/div
V = 20mA/div
V_G = 1V/STEP

Figure 22. Drain I-V characteristics of the same transistor as shown in Figures 10(b) and 11(b). (a) Before oxide overcoat. (b) After oxide overcoat and heating at 350°C for one hour in air.

film deposited over the transistors, several samples were heated simultaneously in a steam ambient for one hour at about 300°C. The results are shown in Figure 23.

The unprotected chromium-silicon sample is completely destroyed in Figure 23(a). The sample in Figure 23(b) has only a thin layer of chromium over the silver for protection, but the results are remarkably good. The deterioration is more pronounced where the metal is in touch with the silicon contact areas. This is consistent with the finding that surface diffusion is considerably faster on a silicon surface with many defects than on a surface free of defects. The heavy doping of the source-drain region is known to introduce a high concentration of defects. The transistors that had an upper chromium layer and were then encapsulated by silicon dioxide show the least amount of deterioration.

To determine the relative importance of water vapor some resistor strips similar to the ones described above were subjected to high-temperature aging in the water vapor atmosphere. The results showed a maximum deterioration

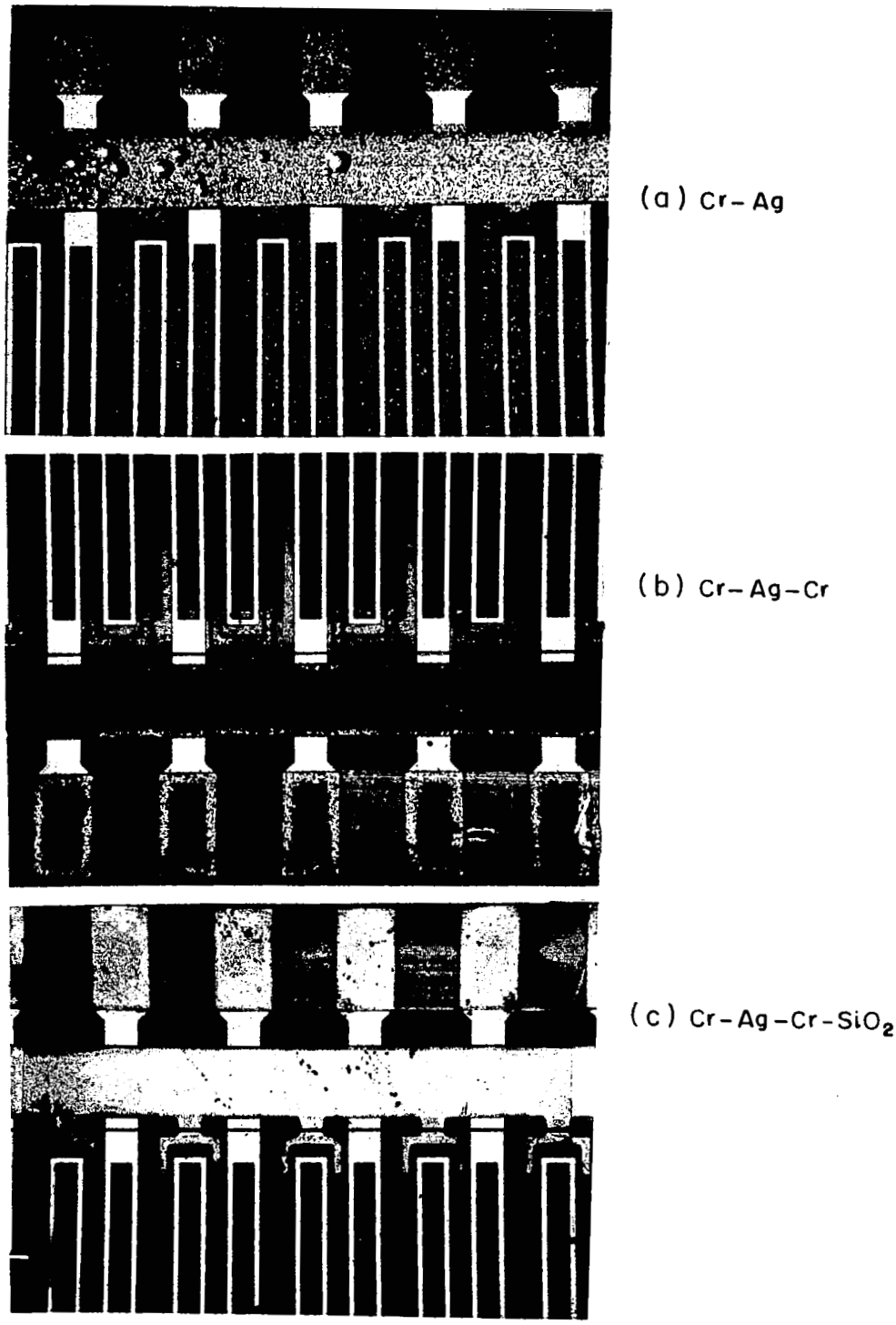


Figure 23. Units similar to the ones in preceding figures, after heating at 300°C for one hour in water vapor. Unit (a) has severely deteriorated, unit (b) has also deteriorated, while unit (c) has deteriorated somewhat, mainly over the bare silicon areas.

rate at 360°C (compared with 400°C in room air), whereas at 280° and 400°C the rates of deterioration were lower.

A typical sequence, which shows deterioration at 360°C more clearly than at other temperatures because of the large balls at this temperature, is shown in Figure 24.

B. Quantitative Analysis of the Contact Deterioration

To analyze the contact deterioration, the main deterioration mechanism will be treated as a problem of viscous flow. In viscous flow there are two main temperature-dependent parameters. The first of these is surface tension which provides the driving force for the granulation of the layers. The second factor is viscosity which is the rate-determining parameter.

To simplify the analysis, the metal layer will be divided into two superimposed layers. It will be assumed that in the top layer silver atoms move over silver with an activation energy of 0.9 eV, and in the bottom layer, silver atoms move over single-crystal silicon (chromium on silicon) with an activation energy that is much larger. The top layer will always be continuous (disregarding statistical fluctuations with time) because even after silver balls have formed a steady-state condition is reached. In this condition, the number of silver atoms arriving at the droplets (where they are "swallowed up") equals those leaving (thus forming a continuous layer). The top layer in the steady state may then be considered as two layers, one consisting of hemispherical granules and the other continuous. A schematic diagram is shown in Figure 25. As indicated in the previous section, the fraction of the top layer found in the granules and in the continuous layer varies with temperature. One reason for treating the two layers differently is that while the top layer is always continuous, the bottom layer reacts, leaving bare (chromium on) silicon. This may occur because a temporarily bared hole in the second layer allows the chromium to oxidize whereafter the surface is not wet by silver (the adhesion is low). From then on the hole enlarges as fast as the silver atoms diffuse away.

The analysis will start with a derivation of the resistance of a conducting layer when holes are forming, from which the activation energy for surface migration is derived. Then the plateaus in the resistance curves are analyzed using the multi-layer approximation described above. From this model the characteristic features of the deterioration curves will be derived; first the droplet size as a function of temperature, then the time required to reach steady state for the top layer, and finally the rate of deterioration for the bottom layer, the latter being the most serious mechanism which ultimately leads to open circuits.

The Resistance of a Discontinuous Layer. -- To interpret the experimental data on the resistance changes in the metal film as it breaks up we need to find the resistance as a function of fractional coverage of the substrate.

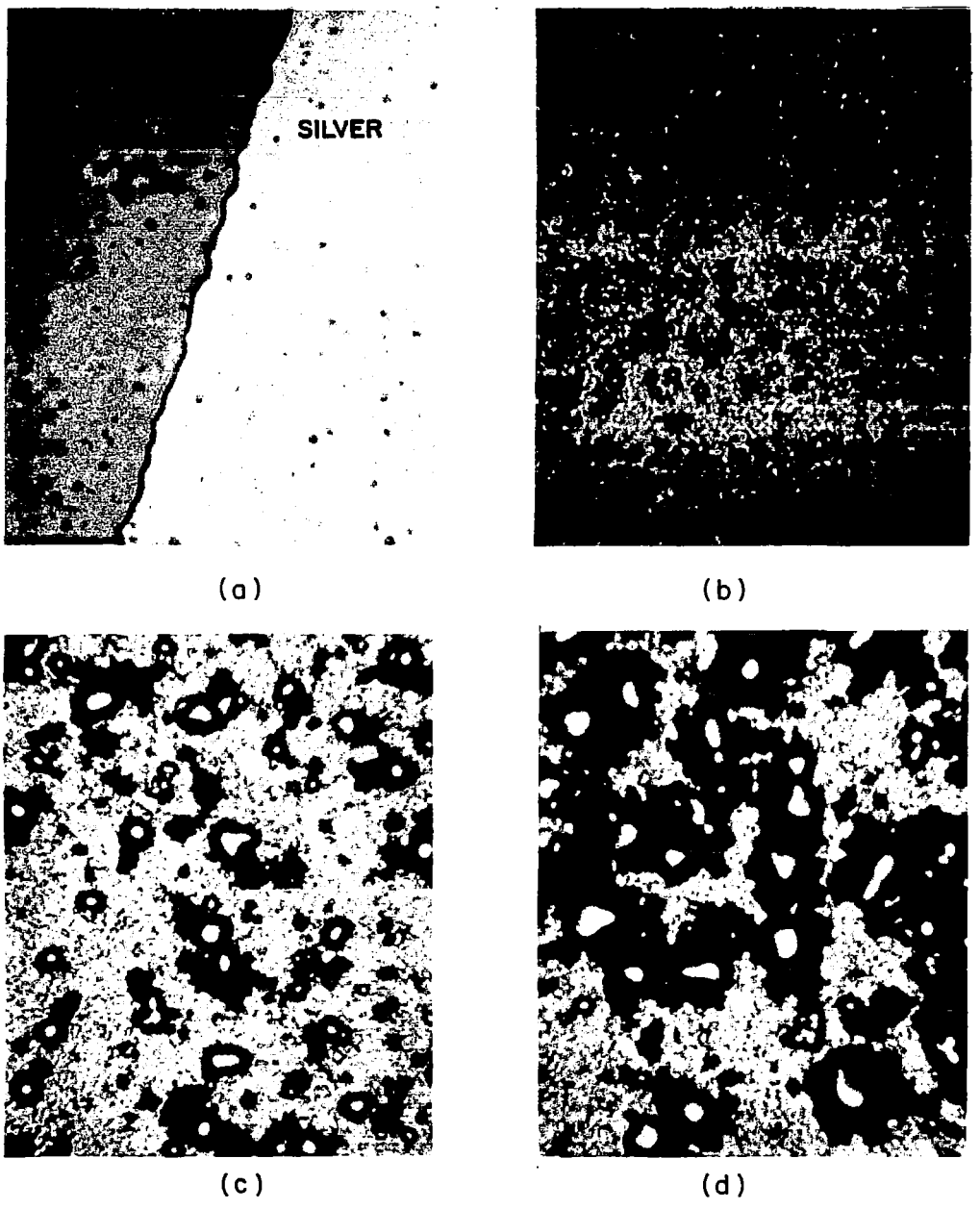


Figure 24. Chromium-silver-chromium film heated at 350°C in air + water vapor. (a) Before heating. The (dark) silicon surface shows defects caused by the high dropping. The (light) metal film is smooth; some surface defects are blanketed. $R/R_o = 1$. (b) After 15 min. Many small droplets (hemispheres, diam. ~ 1 μm) have formed. The film is mottled. $R/R_o = 0.91$. (c) After 55 min. The droplets have coalesced. Holes have appeared in the film. $R/R_o = 1.87$. (d) After 70 min. The film is completely deteriorated and electrically discontinuous although unbroken areas remain. Largest droplets ~ 6 μm in diam. $R/R_o = \infty$.

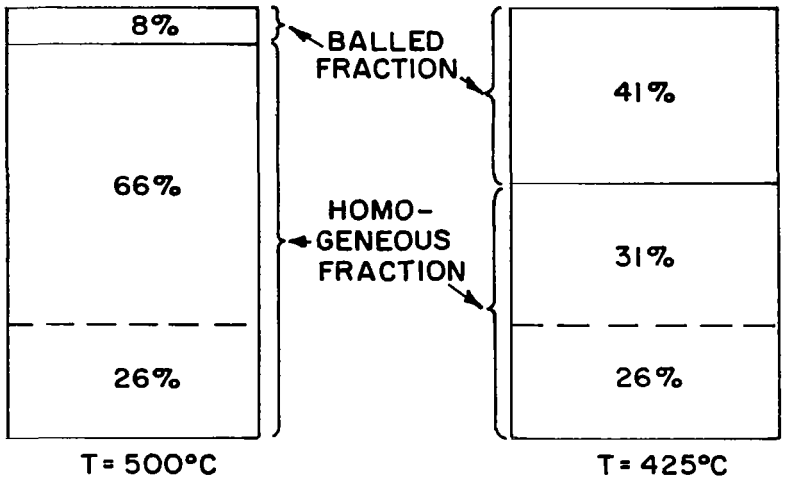


Figure 25. Schematic representation of the contributions to the conductance of the metal layer of the balled fraction, the uniform fraction in equilibrium with the droplets, and the uniform bottom layer.

Assume a homogeneous conducting layer of uniform thickness on top of a conducting substrate. Assume that the first layer starts to break up simultaneously at N statistically distributed spots per unit surface area. The creep velocity with which the retreating edge of each hole moves is determined by the rate at which the atoms diffuse away. The distance which the edge has retreated is therefore linear in time:

$$x = v\ t \tag{1}$$

where v is the creep velocity and t is time. The creep velocity will be temperature-activated like the diffusion velocity

$$v = v_o \exp(-qE/kT) \tag{2}$$

where

v_o is a constant

q is the electronic charge (1.6×10^{-19} Coulomb)

k is Boltzmann's constant (1.38×10^{-23} Joule/°K)

T is the absolute temperature

E is the activation energy

For small t the overlap of holes may be disregarded. Then the conductance σ of the layer, disregarding conductivity changes with temperature, is proportional to the surface still covered

$$\sigma = \sigma_o\ [1 - N\pi\ (vt)^2] \tag{3}$$

For $N\pi (vt)^2 \ll 1$ (small t) the resistance R is

$$R \approx R_o [1 + N\pi (vt)^2] \tag{4}$$

R approaches infinity when $N\pi (vt)^2 = 1$. For a conducting layer on top of an insulating substrate an interruption at any part of the layer makes the resistance infinite. The probability of such an interruption can be calculated but will be neglected here.

While the first case, a conducting film on a conducting substrate, applies to the top part of the metal film, the second case, a conducting film on an insulating substrate, applies to the bottom part of the metal film. To derive the activation energy for surface migration from resistance versus time measurements such as shown in Figures 15 and 16, horizontal lines may be drawn through the figures, giving the same relative deterioration at various temperatures at the intersections with the curves. For two different temperatures, then,

$$R/R_o = 1 + N\pi (v_1 t_1)^2 = 1 + N\pi (v_2 t_2)^2 \tag{5}$$

or

$$t_1 \exp(-qE/kT_1) = t_2 \exp(-qE/kT_2) \tag{6}$$

From Eq. (6)

$$E = \frac{\ln t_2/t_1}{q/k (T_2^{-1} - T_1^{-1})} \tag{7}$$

From this expression the activation energies in Table II have been derived.

TABLE II

DERIVATION OF ACTIVATION ENERGIES

Figure	R/R_o	t_2	t_1	T_2	T_1	E
14	1.5	60	17.8	400	350	0.88
15	1.1	28	13	450	425	1.4
16	1.8	120	90	500	425	0.79

The Plateaus in the Resistance versus Time Curves. -- For the model assumed above (Figure 24) the conductance may be obtained by addition of three items. For layer 1 (the part of the layer that balls) the conductance is

$$\sigma_1 = \sigma_{10} [1 - N\pi (v_1 t)^2] \tag{8}$$

For layer 2 (the part of the layer that remains spread) the conductance in steady-state conditions is, as will be shown later,

$$\sigma_2 = c \cdot \exp(-qE/kT) \tag{9}$$

For layer 3 (the bottom part of the film characterized by an activation energy for creep of 0.9) the conductance is

$$\sigma_3 = \sigma_{30} \left[1 - N\pi (v_2 t)^2\right] \tag{10}$$

The resulting resistance is

$$R = \frac{1}{\sigma_1 + \sigma_2 + \sigma_3} \tag{11}$$

When $t = 0$, $R_o = \frac{1}{\sigma_{10} + \sigma_2 + \sigma_{30}}$. The appearance of the relative resistance R/R_o for two different temperatures is shown in Figure 26.

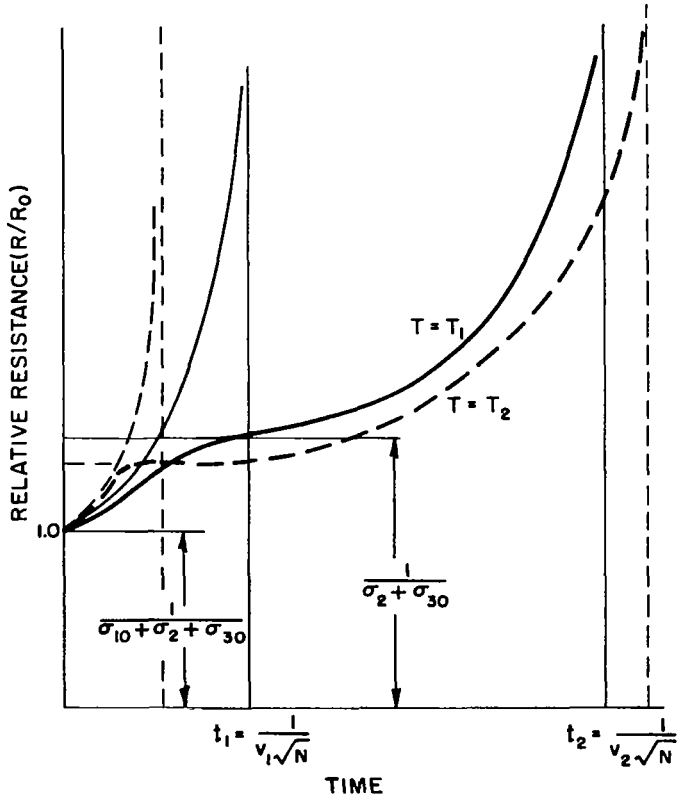


Figure 26. General appearance of the resistance at two different temperatures, predicted from Eq. (11).

If $v_2 \ll v_1$, then for medium 1, after it has deteriorated

$$\sigma_1 = 0$$

$$\sigma_3 \approx \sigma_{30}$$

$$R \approx \frac{1}{\sigma_2 + \sigma_{30}} \tag{12}$$

From Eq. (12), σ_2 and σ_{30} may be determined by fitting to experimental data on R for two different temperatures.

If $t = 0$, then

$$\sigma_1 = \sigma_{10}$$

$$R = \frac{1}{\sigma_{10} + \sigma_2 + \sigma_{30}} \tag{13}$$

From Eq. (13), σ_{10} may be determined by fitting to the experimental data at different temperatures. From the data in Figure 15 the values in Table III have been calculated. Below 425°C the data are not very accurate as the condition that t be small (or σ_3 constant) is not fulfilled. However, in general, the fit is good.

TABLE III

RELATIVE CONDUCTANCE AT VARIOUS TEMPERATURES

Temperature (°C)	$\frac{\sigma_{10}}{\sigma_{10}+\sigma_2+\sigma_{30}}$	$\frac{\sigma_{30}}{\sigma_{10}+\sigma_2+\sigma_{30}}$	$\frac{\sigma_2}{\sigma_{10}+\sigma_2+\sigma_{30}}$
500	0.084	0.282	0.634
475	0.206	0.282	0.513
450	0.324	0.282	0.393
425	0.410	0.282	0.308
400	0.485	0.282	0.234
350	0.693	0.282	0.125

The Droplet Size in the Deteriorated Film. -- We will assume that in the balling process we may treat the silver as a liquid even though the time scale is very much longer than for most ordinary liquids.

When a particle is "swallowed up" by a spherical droplet the surface of the droplet increases. The increase of the surface energy, E, for one unit increase in surface area is[7]

$$E = \gamma - T \frac{d\gamma}{dT} \tag{14}$$

where T is the absolute temperature and γ is the surface tension given by[8]

$$\gamma = \gamma_o \left(1 - \frac{T}{T_c}\right)^{1.2} \tag{15}$$

where T_c is the critical temperature of the liquid and γ_o is the surface tension at 0°K.

When a particle of volume V is "swallowed up" by a spherical drop of radius r_o it grows to a new radius r satisfying

$$\frac{4}{3} \pi r_o^3 + V = \frac{4}{3} \pi r^3 \tag{16}$$

The corresponding change in surface, $\triangle S$, is obtained from

$$\triangle S = 4 \pi (r^2 - r_o^2) \tag{17}$$

With $V \ll r_o^3$ Eq. (17) may be expanded in a series and combined with Eq. (17) to give

$$\triangle S \approx \frac{V}{2r_o} \tag{18}$$

Then the change in surface energy for each particle entering (or leaving) the droplets is

$$\triangle E = E \triangle S \tag{19}$$

This energy may be thought of as an activation energy. In steady state it must be equal to the activation energy for surface diffusion. From Eqs. (14), (15), and (18)

$$\triangle E = \frac{V\gamma_o}{2r} \left[\left(1 - \frac{T}{T_c}\right)^{1.2} + 1.2 \frac{T}{T_c} \left(1 - \frac{T}{T_c}\right)^{0.2} \right] \tag{20}$$

Equation (20) relates the radius of the droplet to the temperature. From inspection of films treated at different temperatures, as in Figure 17, the mean size of the droplets at a given temperature may be estimated. If the radius is r_1 after steady-state conditions have been reached at the temperature T_1, and r_2 at the temperature T_2, we have by insertion in Eq. (20)

$$\triangle E = \frac{V\gamma_o}{2r_1} \left[\left(1 - \frac{T_1}{T_c}\right)^{1.2} + 1.2 \frac{T_1}{T_c} \left(1 - \frac{T_1}{T_c}\right)^{0.2} \right] \tag{21}$$

$$\Delta E = \frac{V\gamma_o}{2r_2}\left[\left(1 - \frac{T_2}{T_c}\right)^{1.2} + 1.2\,\frac{T_2}{T_c}\left(1 - \frac{T_2}{T_c}\right)^{0.2}\right] \qquad (22)$$

Dividing Eq. (21) with Eq. (22) gives

$$\frac{r_2}{r_1}\left[\left(1 - \frac{T_1}{T_c}\right)^{1.2} + 1.2\,\frac{T_1}{T_c}\left(1 - \frac{T_1}{T_c}\right)^{0.2}\right] = \left[\left(1 - \frac{T_2}{T_c}\right)^{1.2} + 1.2\,\frac{T_2}{T_c}\left(1 - \frac{T_2}{T_c}\right)^{0.2}\right] \qquad (23)$$

From Eq. (23) T_c may be solved. Subsequently, from Eq. (23) the size of the droplets at any temperature may be determined. From measurement on Figure 18,

$$R_{450} = 2.0\ \mu m$$

$$R_{500} = 1.6\ \mu m$$

Then from Eq. (23)

$$T_c = 800°K\ (527°C)$$

After insertion in Eq. (23) the droplet sizes in Table IV were calculated.

TABLE IV

DIAMETERS OF DROPLETS AT VARIOUS TEMPERATURES

Temperature (°C)	Diameter of hemisphere (μm)	Phase 2 Time to steady state (minutes)	Phase 3 Time to 10% deterioration (minutes)
500	1.6*	5.7	39.8
475	1.82	10.6	28.4
450	2.0*	30*	28.4
425	2.06	63	33.6
400	2.14	194	45*
350	2.26	1600	103
100	2.56	3×10^9	3×10^6

* Experimental values used to calculate other values.

The Time to Reach Steady-State Conditions. -- Once the droplet size in the steady state is known, it is possible to derive the time to reach steady-state conditions from the known diffusion rate of silver. The time t_1 required to transport the content of a sphere of radius r_1 at the temperature T_1, when the activation energy for diffusion is E, is obtained from

$$\frac{4}{3}\pi r_1^3 = C_1 t_1 \exp\left(-\frac{qE}{kT_1}\right) \tag{24}$$

where C_1 is a constant

$$\frac{4}{3}\pi r_2^3 = C_1 t_2 \exp\left(-\frac{qE}{kT_2}\right) \tag{25}$$

Division of Eq. (24) with Eq. (25) gives

$$\frac{t_2}{t_1} = \left(\frac{r_2}{r_1}\right)^3 \exp\left[-\frac{qE}{k}\left(\frac{1}{T_2} - \frac{1}{T_1}\right)\right] \tag{26}$$

With E = 1.4 eV and using the best value from Figure 15, t_{450} = 30 minutes, the values in Table IV have been calculated from Eq. (26). Of particular interest is the time at operating temperature, say 100°C, which is now many years.

Deterioration of the Bottom Layer. -- The final part of the resistance versus time curves will now be analyzed when the resistance approaches infinity as the holes in the film enlarge until the film becomes discontinuous. The reason why the film retracts, leaving the surface bare, in spite of the escape mechanism assumed above for silver atoms leaving the balls, is not clear. It is believed that oxidation of the underlying chromium is involved, the chromium oxide offering much less adhesion to the silver atoms than metallic chromium. If the film through statistical variations would temporarily become very thin at one spot, the resulting oxidation would then leave it permanently bare. From this spot the film would retract as fast as the silver atoms would diffuse away.

Treating the retraction of the edge like a problem of viscous flow, analogous to the elongation of a bar when a stress is applied, we may write

$$x = \frac{s}{\eta} t \tag{27}$$

where s is the stress applied and η is the viscosity coefficient. The stress applied in this case is the surface tension

$$s = \gamma_o \left(1 - \frac{T}{T_c}\right)^{1.2} \tag{28}$$

The viscosity coefficient is

$$\eta = \eta_o \exp\frac{qE}{kT} \tag{29}$$

where E is the activation energy for creep.

Differentiation of Eq. (27) gives

$$v = v_{\infty}\left(1 - \frac{T}{T_c}\right)^{1.2} \exp\left(-\frac{qE}{kT}\right) \qquad (30)$$

This function is plotted in Figure 27. This function is zero at T = 0 because the atoms do not have enough energy to move. It is also zero at $T = T_c$

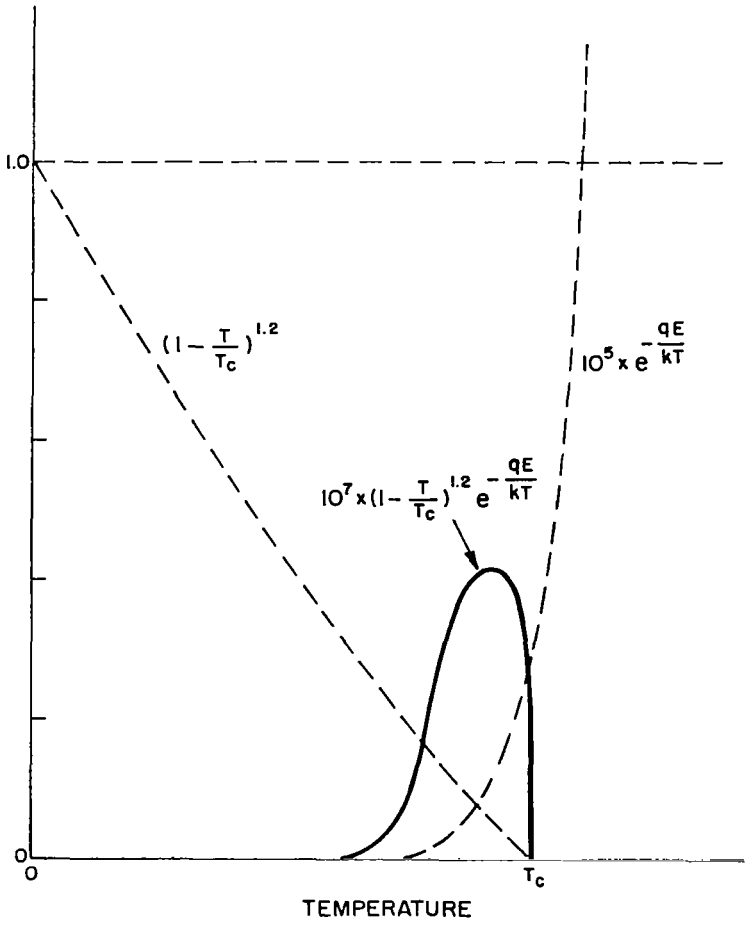


Figure 27. The rate of retraction of the metal layer versus temperature. The dashed lines represent surface tension and the inverse of the viscosity coefficient.

because the surface tension vanishes. At an intermediate temperature the function has a maximum. Turning now to Figure 16 we find that at 350°C the deterioration rate is very small. In the vicinity of 400°C the deterioration rate is highest and as the temperature is further increased the deterioration rate again becomes lower.

Inserting E = 0.88 eV and T_c = 800°K into Eq. (30), we obtain the maximum point at T = 460°C. This is somewhat high as the maximum degradation rate in Figure 16 seems to be close to 400°C.

Using Eq. (30) and inserting one experimental point from Figure 16, that of 10% increase in resistance of the metal layer at 400°C at 45 minutes, the corresponding values at other temperatures have been derived and are shown in Table IV. The calculated times show a minimum at about 460°C.

Of particular interest is the fact that at 350°C the deterioration should start at about 103 min. while in Figure 16 it starts after more than an order of magnitude longer time. The reason for this is that the top layer, with a higher activation energy, does not deteriorate until at about 1600 min. which is the correct order of magnitude and therefore provides a protection inhibiting the bottom layer degradation. Extrapolated to 100°C the deterioration time has been increased from 3 x 10^6 min. ($\approx$ 5 years) to about 5000 years.

The droplet sizes at low temperatures, e.g., 350°C in water vapor, were frequently considerably larger. This appeared to be caused by two or more droplets coalescing, induced by the bottom layer retraction. In this case, the shape of the droplets was not hemispherical but showed two or more prongs. Disregarding such droplets, the average diameters of the droplets were determined from micrographs and are shown in Table IV. This is strong evidence that the overlay of chromium provides a good protection of the silver layer below about 400°C.

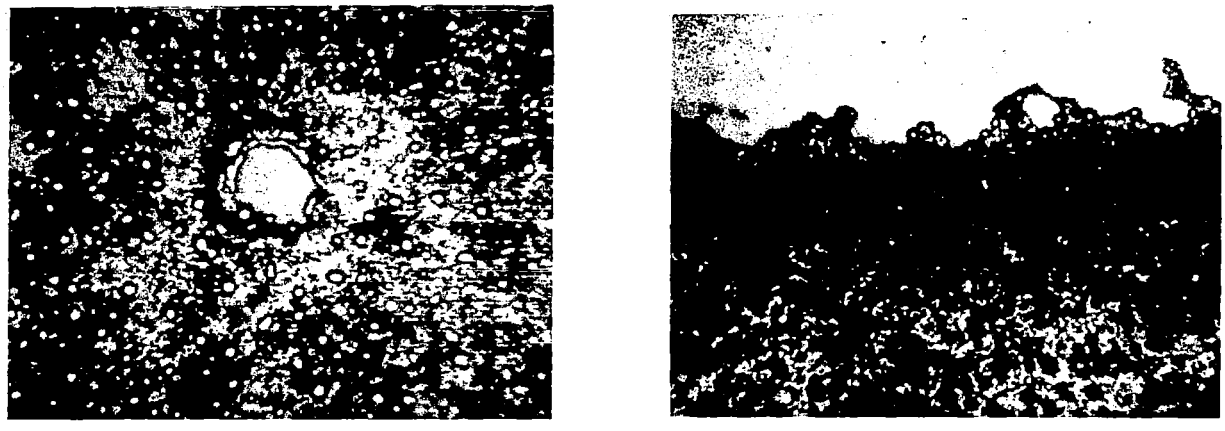
Another piece of evidence is the manner in which the (bottom) silver layer retracts from the surface of the silicon at different temperatures. At high temperature, e.g., 500°C, the retraction starts at many places, independent of the location of the droplets. At low temperature, e.g., 350°C, the retraction always starts around the droplets. In terms of the model presented this is understandable as at low temperature the droplets should grow large, and little silver should be thermally emitted from the droplets. In the growing stage, therefore, the area around a droplet should be depleted of silver, allowing the retraction mechanism to start.

This means also that at low temperature, the steady-state situation may never be reached, and yet considerable deterioration could start at local weak points. For example, pinholes in the silver layer could be expected to start retraction. Occasionally such holes have been observed. An example is shown in Figure 28(a). Similarly, the edge of the metal contact should initiate retraction. The edge of a strip heated at 450°C in air for 145 minutes is shown in Figure 28(b). It should be compared with the edge in Figure 24.

A further check of the activation energies is provided by a comparison of the degradation rates during phases 1 and 3. It appears from Figure 16 that the degradation rates at about 400°C are equal.

Then for phase 1

$$v_{400} = v_o \exp\left(-\frac{qE_1}{kT}\right) \tag{31}$$



(a) (b)

Figure 28. (a) Hole in film enlarged through retraction, probably caused by oxidation proceeding from the initial hole. Chromium-silver-chromium strip heated at 475°C for 25 minutes in air. (b) Edge of strip heated to 450° for 145 minutes in air.

and for phase 3

$$v_{400} = v_o \left(1 - \frac{T}{T_c}\right)^{1.2} \cdot \exp\left(-\frac{qE_3}{kT}\right) \qquad (32)$$

Setting Eqs. (31) and (32) equal gives

$$E_3 - E_1 = 0.53 \text{ eV}$$

which is the difference expected from earlier derivations within each phase.

CONCLUSIONS

An integrated word-driver circuit for laminated ferrite memories using 64 MOS field-effect transistors has been developed. Each transistor is capable of 100-mA current pulses with a drain voltage of 4 V and the gate pulsed from -2 to +2 V. With 100-nsec rise-time on the gate, the rise-time on the drain driving a Phase II ferrite[9] was 160 nsec, which is compatible with memory operation.

The fabrication technology has been developed to the point where a complete driver strip with all 64 units good has been obtained. Counting half-strips, a 30% yield of strips with 32 consecutive good units has been obtained on the last 20 strips.

The uniformity of electrical characteristics from transistor to transistor, and from strip to strip, has been very good. The drain current at fixed voltages has varied typically between $\pm$ 15% for the entire strip.

The most prevalent failure mechanisms have been gate short circuits, in earlier units through the silicon dioxide crossovers and in later units through the thermal silicon dioxide. The next most prevalent failure mechanism has been series resistance in the source drain contacts, possibly caused by insufficient removal of oxide. The dominance of these two failure mechanisms suggests that high yield could be reached if these are eliminated.

The strips have been mounted in plastic frames with leads on 0.010-inch centers. The mounting is done by a solder-reflow technique which has been developed to the point of approaching 100% yield. Preliminary experiments with a plastic package encompassing the frame have been carried out.

To fit the solder reflow technique for connections a chromium-silver source-drain contact method has been worked out encompassing a chromium-silicon dioxide overlay to reduce silver migration during life. The behavior of the silver layer under accelerated life tests has been investigated. It has been found that the overlay increases the activation energy for surface migration from 0.9 eV to more than 1.4 eV. On the basis of these accelerated life tests a mean life in air at 100°C of about 100 years has been extrapolated. However, operating life tests, above those offered by preliminary tests, have yet to be made.

A silicon dioxide crossover technique using thermal decomposition of silane has been perfected to the point of very low pinhole frequency. However, further study of the nature of pinholes in this oxide may be profitable if more complex circuits or higher yields are desired.

A first test encompassing a word-driver strip manually connected to, and driving a Phase I ferrite laminate,[3] has been run. The test gave encouraging results about the performance of the driver transistors. The sense signals were all bipolar and had a magnitude of about 1 mV.

However, some transistors developed gate short-circuits during use, probably caused by weak oxide insulation. In the future, electrical stress testing of the transistors before they are connected in the system is contemplated. The remaining transistors withstood read-write cycling for about 100 hours without change. A more advanced system's test with word-driver, digit-driver, decoder, and decoder-loads, and line terminations connected to the ferrite frame is now being planned.

RECOMMENDATIONS

Based on the work done under this contract the following further steps are recommended to provide feedback on the systems performance of the laminated ferrite memory and to further increase the performance of MOS field-effect transistor circuits.

1. Follow up a system's test encompassing all the drive circuitry, viz.: word-driver, digit-driver, decoder, decoder-loads, line termination circuits, and ferrite memory arrays.

2. Develop further refinements of the technology of the field-effect transistors, particularly eliminating the gate short-circuits and the source-drain series resistance. Study the nature of pinholes in deposited silicon dioxide so that more complex circuits with multiple crossovers can be fabricated.

3. Complete all driver circuits, word-driver, digit-driver, word-decoder, decoder-loads, and line terminations, with a reasonable yield.

4. Develop a more advanced package based on a glass-metal frame offering superior rigidity with less strain from thermal mismatch than the plastic package, and allowing a temperature at least 220°C for circuit passivation and accelerated life tests.

5. Carry out operating life tests with driver strips passivated by the new chromium-silicon dioxide overlay technique, mounted in glass frames, and incorporating the new clean technology fabrication for increased stability of transistor characteristics.

6. As the technology of silicon nitride becomes better developed, make a renewed attempt to incorporate it as an active gate insulator, and possibly also as a crossover insulator.

7. Evaluate the solder reflow technique for connections, and compare it with the thermal compression bonding technique and the ultrasonic bonding technique. Investigate particularly the possibility of making simultaneous connections in batch-processing fashion. Evaluate quantitatively the main advantages of the technique, such as very low thermal and mechanical stress.

8. Investigate silicon-on-sapphire as a material for the word-driver circuit. Evaluate the increase in speed obtained by the reduction of the source capacitance and the increase in speed in the decoding-word driving chain of transistors.

APPENDIX A

DRIVER STRIP FABRICATION PROCEDURE

Further details of the different steps are given under separate headings below.

FABRICATION PROCEDURE

1. Clean wafer (see below).
2. Grow oxide in steam at 1150°C for 45 minutes.
3. Apply KPR photoresist (see below).
4. Etch wafer in buffer etch.
5. Remove KPR.
6. Clean wafer.
7. Grow oxide in steam at 1150°C for 30 minutes.
8. Define source-drain pattern with KPR.
9. Repeat steps 4 through 6.
10. Diffuse source-drain at 1050°C using phosphorus oxychloride ($POCl_3$) in oxygen ambient.
    a. 100% O_2 flow over $POCl_3$ for 7 minutes.
    b. 30% O_2 flow through furnace bypassing $POCl_3$ for 18 minutes.
11. Repeat steps 3 through 6.
12. Apply gate oxide.
    a. Dry O_2 at 1050°C for 15 minutes.
    b. A tetraethyl orthosilicate and trimethyl phosphate mixture is cracked at 730°C in an argon ambient to form a SiO_2 layer. Total deposition time is 2-1/4 minutes.
    c. Dry O_2 at 1050°C for 7 minutes to densify deposited SiO_2.
13. Anneal in H_2 at 500°C for 15 minutes.
14. Evaporate aluminum for gate.
15. Apply KPR photoresist, expose and etch unwanted aluminum.
16. Apply low-temperature silicon dioxide through metal mask for cross-over insulation.
17. Evaporate chromium and silver from separate sources for source and drain.
    a. Chromium for 30 seconds, corresponding to 200 Å.
    b. Chromium and silver for 30 seconds, corresponding to 800 Å.
    c. Silver for 2 minutes, corresponding to 2400 Å.
18. Apply KPR photoresist, expose, etch, and remove KPR.
19. Test wafer.
20. Scribe and dice.

MATERIAL

The silicon wafers are epitaxial p on p+ material. The p-type region is 6 to 10 Ω-cm; the p+ type region is 0.007 Ω-cm material. The wafers are 1 in. to 1-1/8 in. in diameter and from 6 to 10 mils thick; they are oriented on the (100) plane to facilitate dicing.

CLEANING PROCEDURE

Step 1. Wafer is placed in a beaker with a 10 part distilled water to 1 part HF solution and allowed to stand for 5 minutes at room temperature.

Step 2. The solution is decanted and the wafer is rinsed 2 or 3 times with distilled water.

Step 3. The next solution is 4 parts distilled water, 1 part ammonium hydroxide, and 1 part unstabilized hydrogen peroxide. The solution is heated to boiling for 5 minutes.

Step 4. Repeat Step 2.

Step 5. The next solution is 4 parts distilled water, 1 part hydrochloric acid, and 1 part unstabilized hydrogen peroxide. The solution is heated to boiling for 5 minutes.

Step 6. Repeat Step 2.

Step 7. The final solution is distilled water that is heated for 5 minutes and then decanted; the beaker and wafer are boiled dry.

Note: Step 1 is used only when starting new wafers. All other times the cleaning procedure starts from Step 2.

KPR PROCEDURE

1. Wafer is spin-coated with KPR and prebaked at 75°C for 5 minutes.
2. The wafer is exposed through the proper mask using a high-intensity mercury arc lamp for 3 minutes.
3. Developed for 4 minutes.
4. Post-baked at 120°C for 5 minutes.

ETCHING PROCEDURE

1. The wafer is placed in a buffer etch to remove (a) specific areas of oxide or (b) the metal pattern, if any.
2. KPR is removed using a 1 part hydrogen peroxide and 1 part sulfuric acid solution when no metal is on the wafer.
3. When the wafer has a metallized pattern then J-100 is used to remove KPR (a commercial solvent).

APPENDIX B

LOW-TEMPERATURE DEPOSITION OF SILICON DIOXIDE FROM SILANE

The low-temperature deposition of silicon dioxide is achieved using the oxidation reaction of silane in oxygen

$$SiH_4\ (g) + 2\ O_2\ (g) = SiO_2\ (s) + 2\ H_2O\ (g)$$

The apparatus used for the deposition is shown in Figure 18. The wafers are placed on a rotating heated pedestal. The oxygen and the silane (the latter diluted in nitrogen) are metered out into the Pyrex reaction chamber through separate lines.

Although reaction can occur at wafer temperatures as low as 200°C, temperatures of 320 to 330°C were used to produce a uniform film.

The gas flows at standard conditions were as follows

N_2	2200 cc/min
O_2	60 cc/min
3% SiH_4 in N_2	230 cc/min

The thickness of the film was monitored during growth by noting the change in interference color. Most films grown were of the order of 4000 Å thick.

Under certain deposition conditions, particularly low temperature and excess silane, the silicon dioxide particles grow quite large and settle on the surface as a grainy layer, clearly visible under the microscope (200 X). If the larger particles are small enough (< 1 μ) the layer may still be continuous and show a pinhole density not too different from that of smoother layers. However, if a large particle settles on the surface it may not be bound sufficiently well by the oxide but may be flushed off by the gas or by the etch and rinse. In its place remains a thin region which naturally shows an excess pinhole density. Such spots have a color different from the surrounding area.

The standard deposition procedure is as follows:

1. The pedestal is heated to 320-330°C.
2. Nitrogen is turned ON.
3. Wafers are placed in reactor.
4. After 5 minutes silane is turned ON.
5. After another 30 seconds the oxygen is turned ON.
6. When the oxide has reached desired thickness, the silane is turned OFF. Deposition rate is about 800 Å/minute.
7. After one minute, wafer can be removed from reactor.
8. Silane lines are flushed with pure nitrogen and all gases are turned OFF.

APPENDIX C

TEST VEHICLE OPERATION

by
A. D. Robbi and J. W. Tuska

A. Introduction

This appendix summarizes the operation of a test vehicle combining a type 47* ferrite laminate memory plane with 256 x 100 crossovers on 10-mil centers and a simulated MOS transistor switch strip. The simulated switch strip consists of sixteen 10-lead sockets, partially populated with encapsulated MOS switch transistors. The transistors used are sections (4 drain contacts, 4 gate contacts, common source, and substrate) of the 64-switch strip units developed under the contract.

B. Word Driver Transistors

The completely integrated word driver strip encompassing 64 transistors described in the main part of the report, and on which preliminary system tests were made, ran into life problems at the termination of the contract period. The plastic frame used for mounting the strip contains a hardener, an aliphatic amine, which over the course of three months reacted with the silicon dioxide of the gate insulation, lowering the gate breakdown voltage from about 60 V to about 10 V. The reaction is speeded up when the mounted strips are stored in closed boxes, as routinely done, and retarded when the strips are out in the open to permit system testing.

For this reason unmounted strips were cut in pieces, with each piece encompassing four driver transistors. Each quadruple is mounted in a TO-5 can with ten leads. The mounting is shown in Figure 29. Single transistors lost in the cutting and mounting process or during the testing are disconnected by physically removing the gate and drain leads on the can (pin chart shown in Figure 29).

As the strips were stored for about nine months in a dry box prior to encapsulation and the encapsulation procedure is not optimized, the life of the encapsulated units is uncertain. All transistors were tested on a curve-tracer. Those passing the test specifications given below are used for the system.

Current-Voltage Characteristics

Test Conditions: With source grounded and substrate at -9 V, the drain is swept to +4 V with the gate stepped from 0 to +4 and to -4 V in 1-volt steps.

*Developed under Contract NASw-979, Phase II.

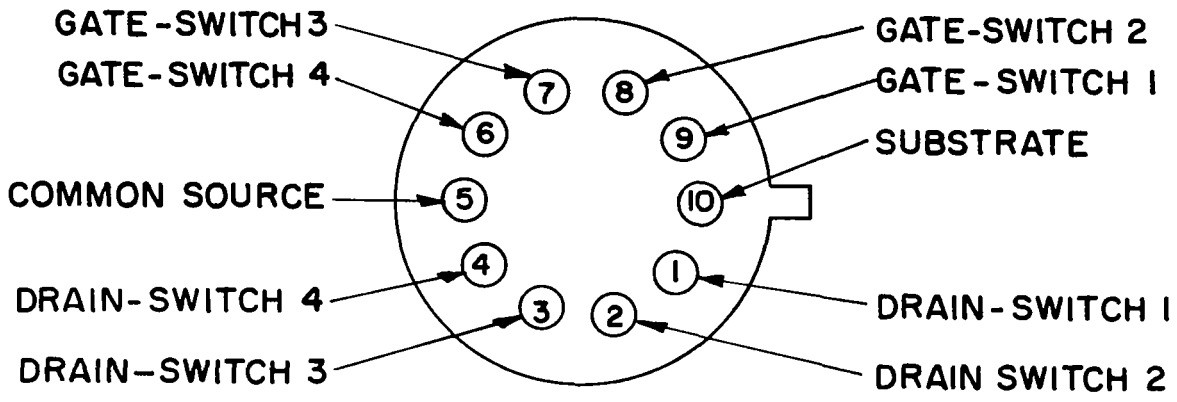


Figure 29. Bottom view of the MOS transistor word switch.

Acceptance Specifications: At V_D = 4 V, V_G = 2 V, V_{sub} = -9 V, I_D = 85-125 mA. At V_D = 4 V, V_G = -3 V, V_{sub} = -9 V, $I_D \leq 0.050$ mA.

Gate Breakdown

Test Conditions: With source grounded the gate is biased to -20 V.

Acceptance Specifications: $I_G \leq 0.025$ mA.

Diode Breakdown

Test Conditions: With substrate grounded the drain and source are biased to -13 V.

Acceptance Specifications: $I_D + I_S \leq 0.050$ mA.

C. Test Vehicle

The test vehicle consists of a type 47* ferrite laminated containing 256 x 100 crossovers, with 64 word lines connected via an etched circuit board to an array of 16 sockets. This facilitates the connection of up to 64 MOS transistor word switches. The 100 digit lines are accessible via an etched fan pattern board (with the exceptions of lines 8 and 94 which are open). The physical location of the laminate, MOS transistor switches and connectors, and the identification of specific word and digit lines are shown in Figure 30.

The individual MOS transistor word switch gates, plus the common substrate and source connections are accessed from two 38-pin plugs (Mating Connector Amphenol "Micro-Min" 74-104). The locations of these connections are shown in Figure 31.

*Developed under Contract NASw-979, Phase II.

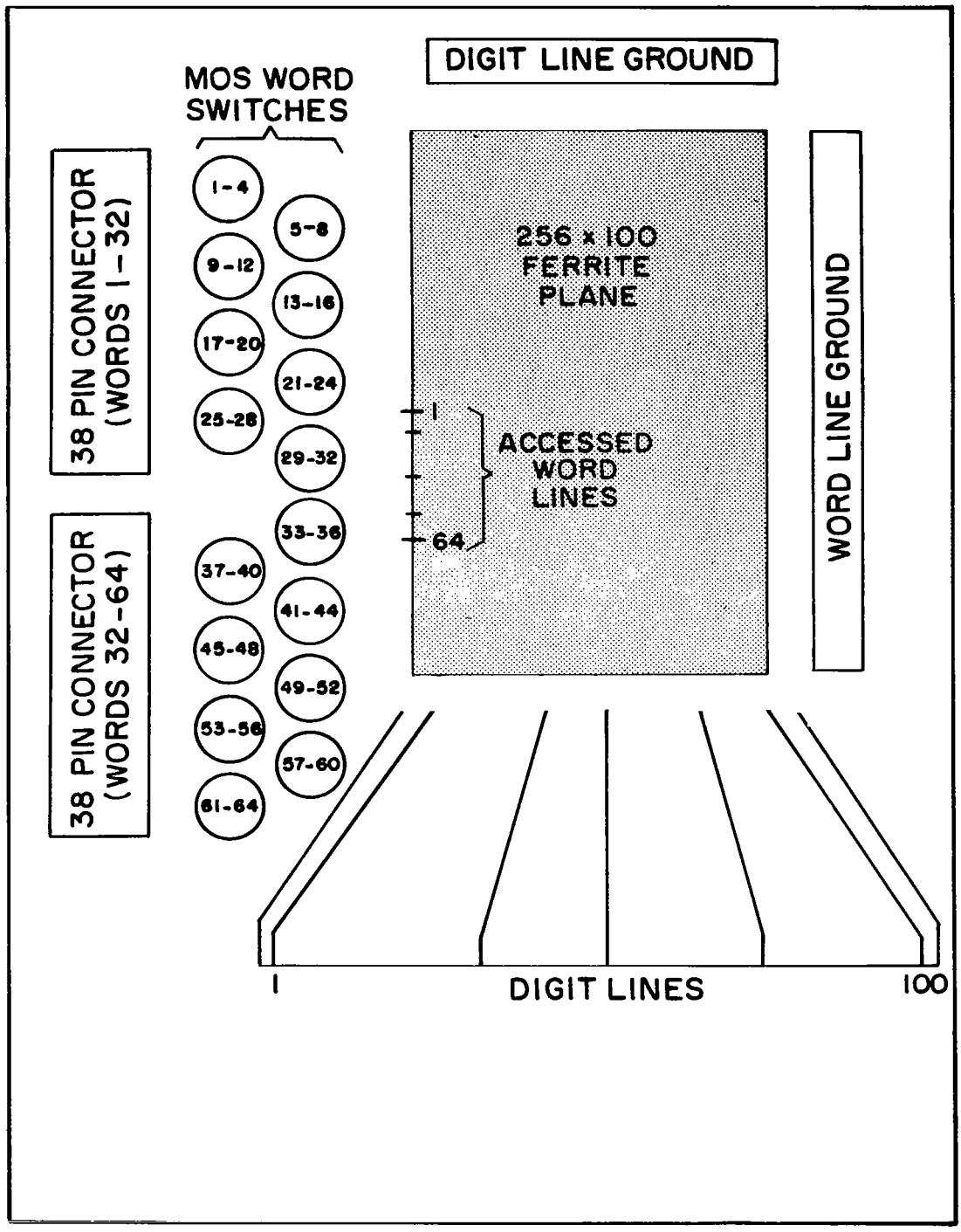


Figure 30. Top view of the MOS transistor ferrite laminate system.

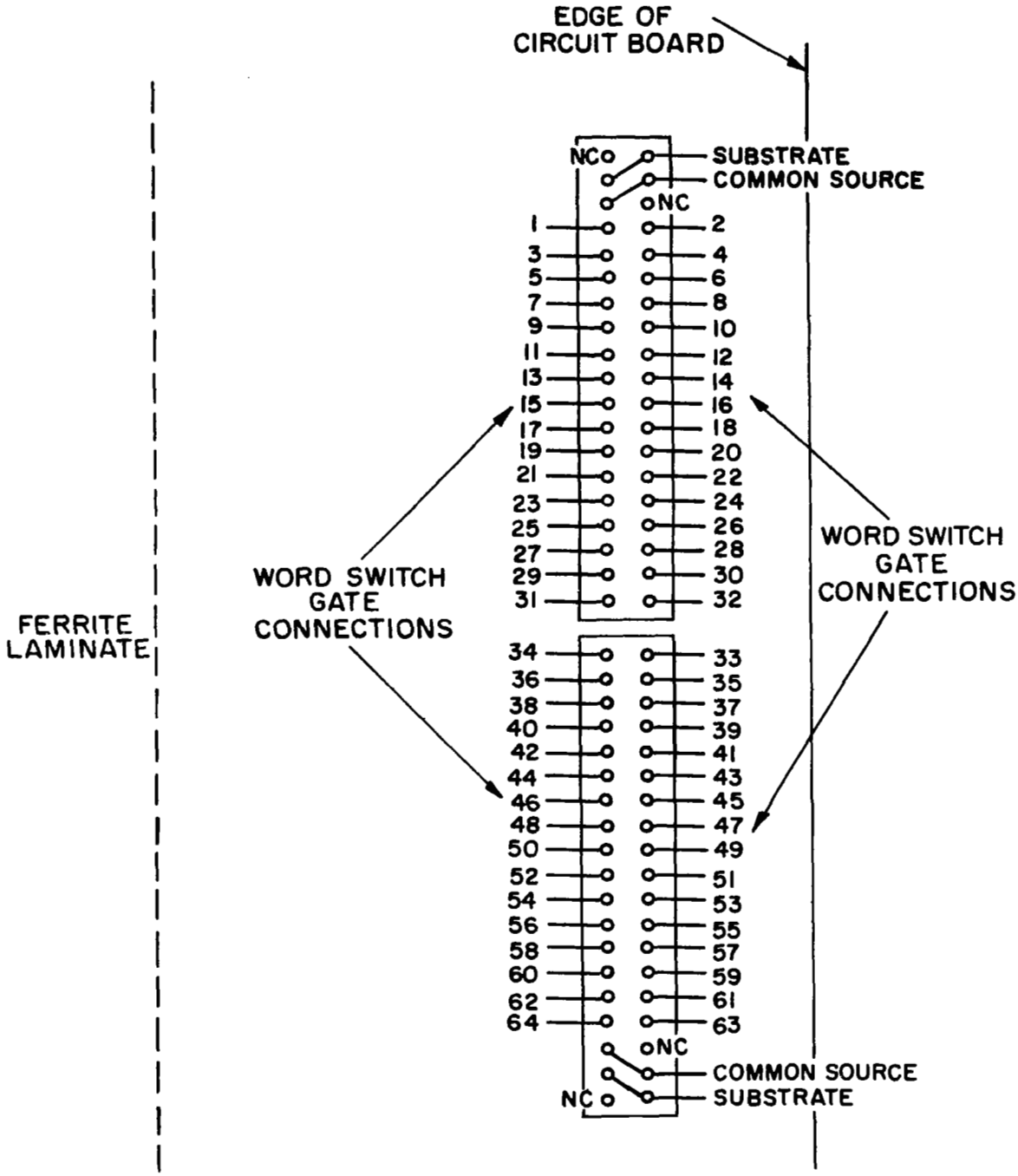


Figure 31. Bottom view of the circuit connection locations.
Connectors: Amphenol "Micro-min" 74-103.

D. Operating Conditions

Figure 32 shows the connections for the bias supplies and the pulse generators for operating the MOS transistor switch ferrite laminate test vehicle. The MOS transistor word switches are held nonconducting by a negative gate bias applied to the MOS gate through a 10-kΩ resistor. In cases of gate leakage or failure, the resistor functions as a current limiter and facilitates the identification of the faulty gate. Selection of an individual MOS switch is by application of a positive pulse of amplitude 10 V above the 8-V negative bias. Implementation of the gate selection switch, shown in Figure 32, for the tests described below have been both a rotary mechanical switch and an electronically driven reed relay tree.

The 0.2-msec risetime of the gate pulse controls the word READ current risetime, and the fall time of the gate pulse controls the fall time of the word WRITE current. Figure 33 illustrates the timing and voltage levels of the gate and READ and WRITE voltages applied to the MOS transistor switches. The voltage levels shown in the upper trace of this figure (READ-WRITE voltage at common source — no switches conducting) should not be exceeded by more than 20% to prevent unwanted conduction in the case of the negative READ voltage or transistor breakdown in the case of the positive WRITE voltage. The -8 volt level for the gate "off" state as shown in the lower trace is ample to maintain the nonconducting status of the switches for the source voltages shown. The gate pulse amplitude controls primarily the amplitude of the positive WRITE current. The READ current amplitude is controlled by adjustment of the negative voltage level of the generator.

The center trace of Figure 34 shows the typical source current resulting from the conduction of a single MOS switch under the voltage level conditions previously discussed. The lower trace shows the capacitive charging currents resulting from the application of the generator voltages without switch conduction. Thus, the currents actually delivered to a selected memory word are the differences between those two traces. A significant departure from the waveforms shown is generally indicative of a faulty MOS switch. The most likely failure is spurious conduction due to a leaky gate. This type of fault can be corrected by cutting (at the transistor header) the gate and drain pins of the faulty switch. Failure of the source-to-substrate diodes requires removal of the entire can.

For memory operation, DIGIT currents overlap in time the WRITE current as indicated in the upper trace of Figure 34. The digit current is held constant at 16 mA for all the data to follow. The full test program of memory currents for one-crossover-per-bit operation is shown in Figure 35. READ and WRITE currents always occur as pairs as shown in Figure 34. The program yields output signals which are disturbed both prior to and after writing. The data to follow are taken with this program.

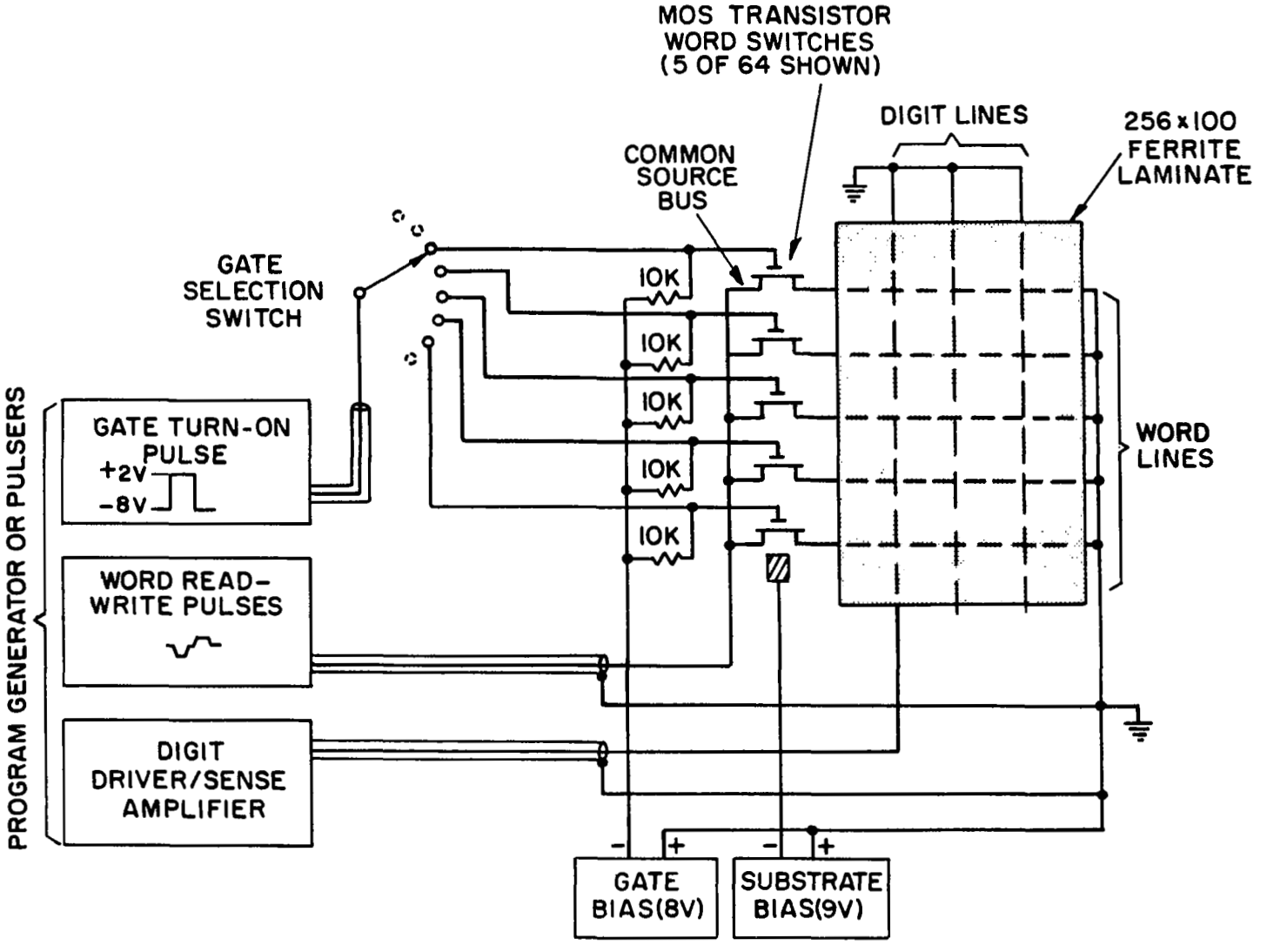


Figure 32. System connections and circuit.

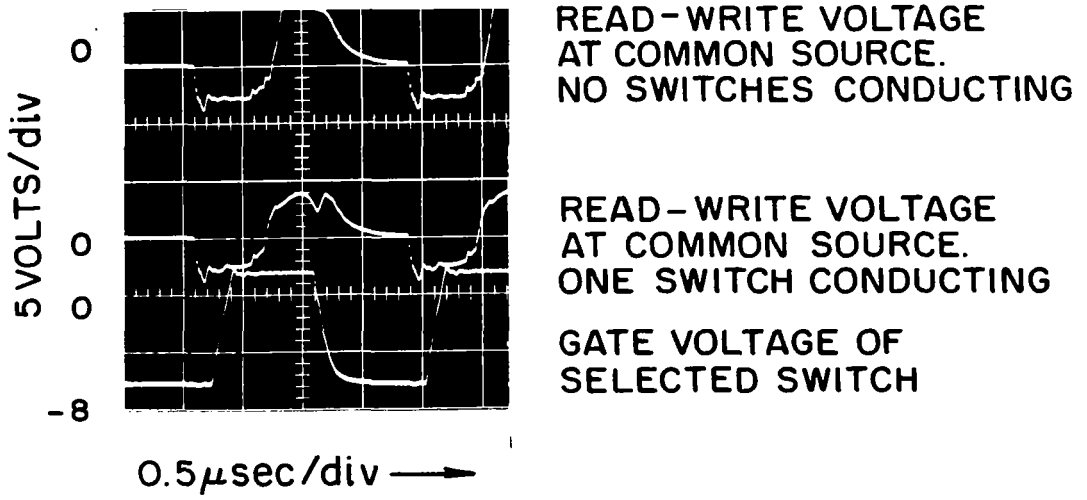


Figure 33. Switch voltages.

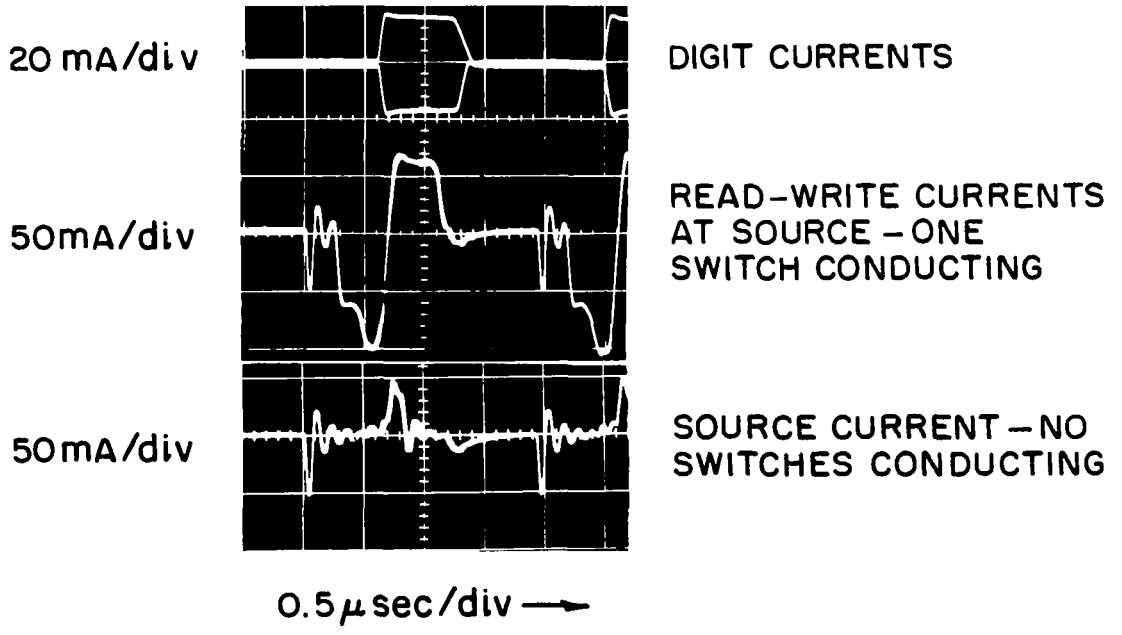


Figure 34. Memory currents.

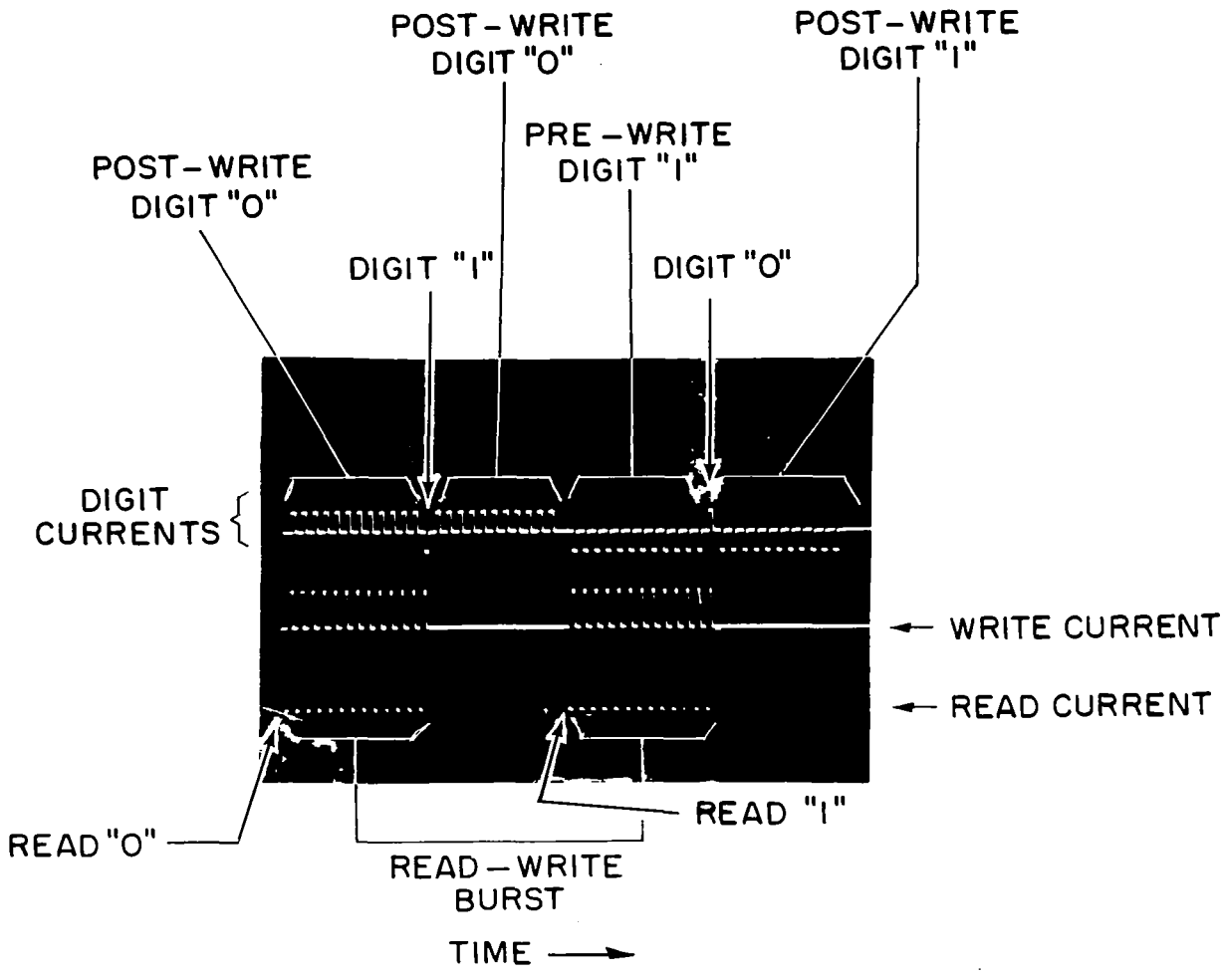


Figure 35. Pulse program for bipolar digit, one-crossover-per-bit operation.

E. System Performance

Peak word currents delivered to the memory plane by the various MOS switches in the test vehicle are given in Table V. These data were obtained by selecting the MOS switches with a rotary mechanical switch.

Missing entries in Table V are indicative of faulty MOS switches. Variations in the read currents are indicative of variation in MOS switch terminal characteristics rather than nonuniformity of the laminate.

TABLE V

READ AND WRITE CURRENTS IN TEST MODEL

WORD No.	CAN - UNIT No.	No.	READ (mA) Current	WRITE (mA) Current	WORD No.	CAN - UNIT No.	No.	READ (mA) Current	WRITE (mA) Current
1	1	1	115	65	33	9	4	120	65
2		3	115	65	34		3	120	65
3		2	115	65	35		2	120	65
4		-	-	-	36		1	120	65
5	2	4	100	60	37	10	4	115	65
6		3	100	60	38		3	115	65
7		2	90	60	39		2	115	65
8		1	90	60	40		1	115	65
9	3	4	115	65	41				
10		3	115	65	42				
11		-	-	-	43				
12		1	115	65	44				
13	4	4	115	65	45	12	4	115	65
14		-	-	-	46		-	-	-
15		-	-	-	47		2	110	65
16		-	-	-	48		1	110	65
17	5	4	100	65	49	13	-	-	-
18		3	85	65	50		3	100	60
19		-	-	-	51		2	95	55
20		1	95	65	52		-	-	-
21	6	4	120	65	53	14	4	115	65
22		3	120	65	54		3	115	65
23		2	120	65	55		2	115	65
24		1	120	65	56		1	115	65
25	7	-	-	-	57	15	4	115	65
26		3	120	65	58		3	115	65
27		2	110	65	59		-	-	-
28		-	-	-	60		-	-	-
29	8	4	110	65	61		-	-	-
30		3	120	65	62		-	-	-
31		2	120	65	63		-	-	-
32		-	-	-	64		-	-	-

The operation of the memory system in a one-crossover-per-bit mode with bipolar digit currents should result in a positive "1" signal and a negative "0" signal. A reed relay tree is used for gate selection, and the full program shown in Figure 35 is applied in time sequence to each of 32 different memory words. The particular switches selected are 1-8, 17-24, 33-40, and 49-56. During the test 29 of the 32 switches were operable. Minimum and maximum "1" and "0" sense signals for every tenth digit line (a total of eleven lines), as the words are scanned, are plotted in Figure 36. The digit lines at the very edges of the plane are not fully operable because of low "1" signals. In general, it was found that the minimum signals were developed at bit locations serviced by an MOS switch with relatively low READ current, such as number 18.

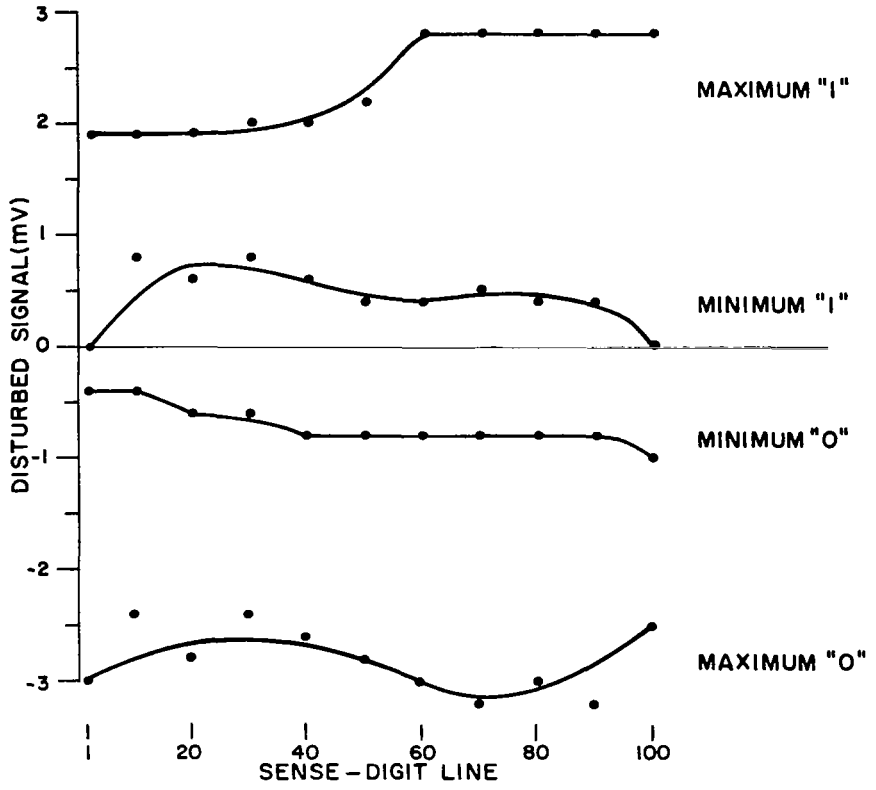


Figure 36. Sense digit line, one-crossover-per-bit performance.

To improve the "1"/"0" discrimination, the system may be operated in a unipolar digit, two-crossovers-per-bit mode. In this mode, two adjacent digit lines are used to store a bit of information. The sense signal is the differential voltage between the two lines, resulting in cancellation of common inductive and capacitive noise. The capacitive noise is negligible; so the benefit of this mode of operation is the cancellation of inductive noise. To store a binary "1" a negative digit current pulse is applied to one line of the pair; to store a "0" the other line is pulsed. The linear section of an integrated differential sense amplifier (RCA TA5196) is used as a scope preamplifier (gain of 300). The same 32 words as in the previous test are scanned. The superposed sense signals for pair #25 (digit lines 49, 50) are shown in Figure 37. The minimum and maximum sense signals, defined as before, for all 50 bits are plotted in Figure 38. The operation is superior to the one-crossover-per-bit mode. As before, edge effects result in poor discrimination at the two outermost bits. However, the discrimination over the rest of the plane is improved by about a factor of 2.

Based on the data presented in this appendix, a summary of the operating characteristics for a one-crossover-per-bit and a two-crossovers-per-bit mode

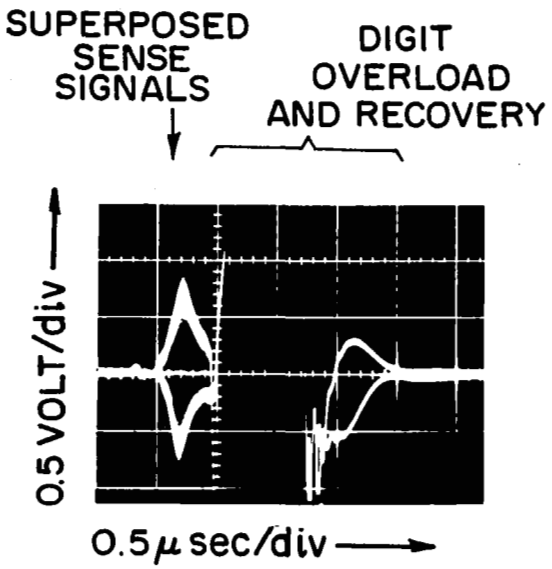


Figure 37. Amplified sense signals from digit pair 25, digit lines 49, 50 (32 words scanned − 2 switches not conducting).

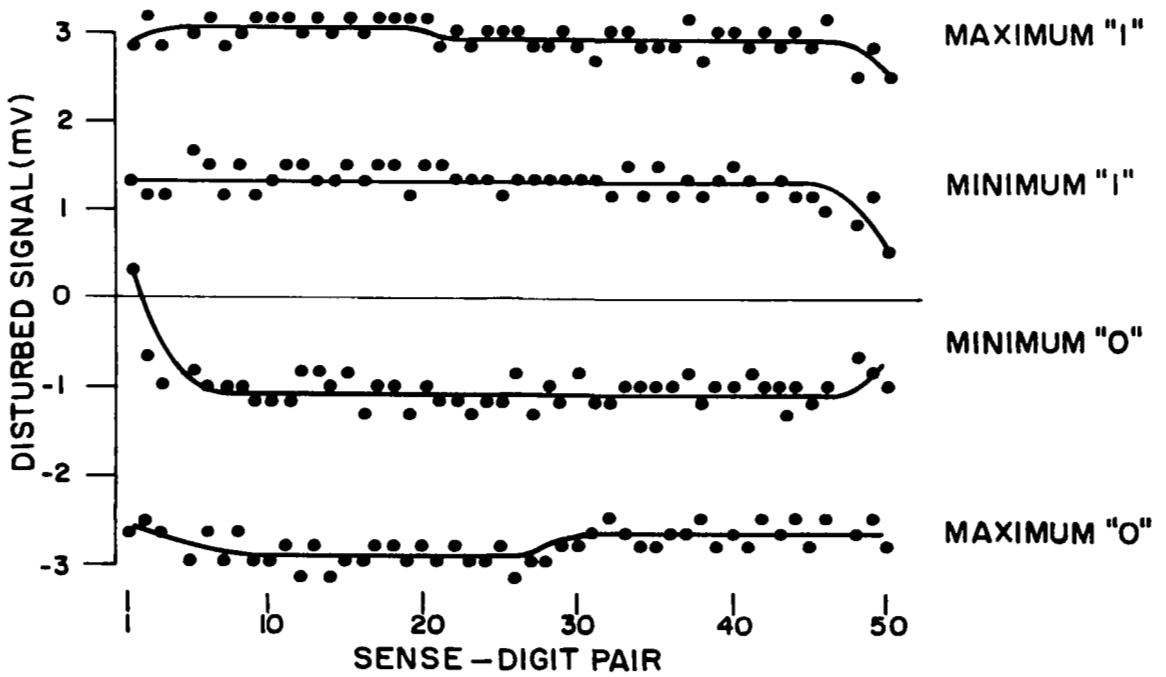


Figure 38. Two-crossovers-per-bit performance.

is given in Table VI. The drive currents, cycle time, and power dissipation for either operating mode is essentially the same. The two-crossovers-per-bit mode requires a slight increase in the word power because of increased back voltage. However, since most of the word power is a result of the common source capacitance charging current, the increase in dissipation due to increased back voltage is small. Further, in an actual operating system, the dissipation in the digit-sense circuits far exceeds the word system power. On this basis, the two-crossovers-per-bit mode offers attractive advantages in terms of operating margins, higher sense outputs, and greater laminate yield.

TABLE VI

SUMMARY OF OPERATING CHARACTERISTICS OF TEST VEHICLE

	ONE CROSSOVER/ BIT	TWO CROSSOVERS/ BIT
Read Current Amplitude Risetime 50% Duration	 115 0.25 μsec 0.5 μsec	 115 0.25 μsec 0.5 μsec
Write Current Amplitude 50% Duration	 65 0.25 μsec	 65 0.25 μsec
Digit Current Amplitude 50% Duration	 16 mA 0.5 μsec	 16 mA 0.5 μsec
Sense Signal Average Minimum Amplitude 50% Duration	 ±0.6 mV 0.25 μsec	 ±1.2 mV 0.25 μsec

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