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FINAL REPORT

for

Development of Multiple Source - Multiple Low Voltage
Converter-Regulator Power Supply with Automatic
Failure Sensing and Redundant Switching
(30 June 1966 - 30 July 1967)

Contract No. NAS 5-10148

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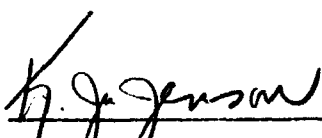
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CONVERTER-REGULATOR POWER SUPPLY WITH AUTOMATIC
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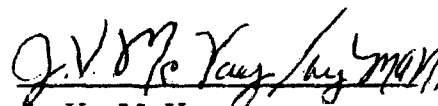
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Goddard Space Flight Center
Greenbelt, Maryland

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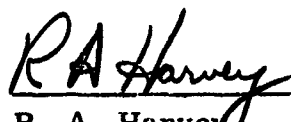

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CONTENTS

- SUMMARY (p. 1)
- I. ACTIVITIES OF THE FOURTH QUARTER (p. 4)
- A. INTRODUCTION (p. 4)
- B. TECHNICAL DISCUSSION (p. 5)
1. Electrical Design Review (p. 5)
 2. Reliability Analysis of the Redundant LIVCR Configuration (p. 17)
 3. Testing and Performance (p. 34)
 4. Redundant Configuration Considerations (p. 36)
 5. Package Layout and General Operating Procedures (p. 39)
- II. REVIEW OF PROGRAM ACCOMPLISHMENTS (p. 44)
- A. SYNCHRONIZATION OF FOUR REDUNDANT LIVCS (p. 44)
- B. LIVC FAILURE SENSING AND ISOLATION (p. 46)
- C. PWM REGULATOR POWER SECTION FAILURE SENSING AND ISOLATION (p. 47)
- D. PWM DRIVE AND CONTROL WITH FAILURE SENSING AND ISOLATION (p. 49)
- E. DECREASING UNBALANCE IN THE LIVC FEEDBACK TRANSFORMER (p. 51)
- III. NEW TECHNOLOGY (p. 53)
- IV. CONCLUSIONS AND RECOMMENDATIONS (p. 54)

APPENDIX A - RELIABILITY DATA (p. 58)

APPENDIX B - EVALUATION REPORT (p. 72)

ILLUSTRATIONS

Figure

- | | |
|----|---|
| 1 | LIVCR G2554A1, Top View (p. 6) |
| 2 | Block Diagram - G2554A1 (p. 7) |
| 3 | Circuit Diagram for Redundant LIVCR with Automatic Failure-Compensation Model (p. 9) |
| 4 | PWM Drive and Control Failure Sensing and Compensation - G2554A1 (p. 10) |
| 5 | Sensing and Isolation of Shorted PWM Transistor G2554A1 (p. 11) |
| 6 | Failure Sensing and Isolation at LIVCs Input (p. 12) |
| 7 | Reliability Figures (p. 18) |
| 8 | Efficiency Characteristics of Redundant LIVCR - G2554A1 (p. 37) |
| 9 | LIVCR G2554A1, Front View (p. 40) |
| 10 | LIVCR G2554A1, Back View (p. 41) |
| 11 | Synchronization Circuit for Four LIVCs (p. 45) |
| 12 | Sensing and Isolation of LIVC Output Capacitor Failures (p. 48) |
| 13 | Sensing and Isolation of Shorted PWM Output Capacitor and Free-Wheeling Diode (p. 50) |
| 14 | Current Feedback Control Circuit for Equal Transformer Drive (p. 52) |

TABLE

Table

- | | |
|---|---|
| I | Typical LIVC Efficiency (Common Inputs) (p. 35) |
|---|---|

SUMMARY

This report describes work performed during the fourth quarter on contract NAS 5-10148 (section I) and summarizes the complete program (section II).

With use of the practical, automatic, failure-sensing and redundant-switching circuitry developed during this program, it is now possible to fabricate reliable, efficient electrical power systems necessary for future, long-duration space missions.

A primary goal of this program was development of automatic, failure-sensing and compensation circuitry for the redundant low input voltage converter regulator (LIVCR) to increase reliability of the conversion-regulation function. The strong dependence of mission success on the maintained supply of electrical power and the paramount importance of high reliability in space applications motivated the effort on this program.

Reliability of the power system on long-time space missions can be significantly enhanced by incorporation of the developed circuitry in conjunction with the basic LIVCR. Additional benefits derived from the technology include: (1) increased flexibility facilitated by a basic modular design of respective LIVCR redundant subsections, (2) elimination of the need for telemetry monitoring and command switching, (3) increased system stability, and (4) decreased time elapse between failure occurrence and compensation.

The program approach included four major tasks: (1) LIVC synchronization, (2) automatic failure sensing and compensation, (3) decreased unbalanced in single LIVC, and (4) redundant configuration considerations.

LIVC synchronization circuitry was established for four parallel LIVCs. This was an extension of the circuitry established on NAS 5-9212. It enables the designer to increase the degree of redundancy and retain advantages of phase-separated synchronization. Those advantages include increased stability and reliability through reduction of line transients.

A major task in any failure compensation system is to identify the malfunctioning circuit block and to effectively remove or isolate that block. It is desirable to accomplish this with a minimum of sense lines and discrimination. The element actually providing isolation capability must also efficiently connect the block in the system when the block is operational. The circuitry developed on this program satisfies these requirements.

A most significant development is the low-loss LIVC transistor input switch which inherently provides automatic failure compensation. Failure modes which can be isolated include shorted LIVC input capacitor, power transistor, and power transformer. Complementary circuitry can be added to isolate output rectifiers and capacitor failures. In addition to the automatic compensation feature, this switch is more efficient, smaller, lighter, and less costly than many competitive electro-mechanical devices performing the same function.

The redundancy and failure compensation in the pulse width modulation (PWM) regulator is divided into the power section and the drive and control section. Isolation for shorted PWM chopping transistors in the parallel power sections is provided with a controlled switch. Failures in the free-wheeling diode and output capacitor can be isolated with the same controlled switch with the technology developed. The PWM drive and control circuitry was modified to facilitate the automatic failure sensing and compensation; the compensation circuitry automatically selects the drive and control circuit, in standby redundancy, that is operational.

The occurrence of unbalance in the LIVC oscillator is reduced by a closed-loop control of the current feedback transformer.

The common radioisotope thermoelectric generator (RTG) output-common LIVC input configuration promotes simplicity in switch circuitry for maximum usage of operational sections, even after some failures occur.

However, the common LIVC input should be avoided if an SCR overvoltage circuit is incorporated, unless each LIVC is capable of handling the total RTG output. Considerations of a shunt-type PWM regulator to provide both RTG overvoltage protection and output voltage regulation may be worthwhile in future work.

A 375-watt LIVCR, incorporating many of the techniques developed on this program, has been delivered to NASA/GSFC. A reliability analysis to indicate general reliability trends was completed for the model and results are presented herein. Design advantages predicted during the program have been borne out by the performance of the delivered model. The established technology provides the designer increased capability in specifying power systems for space applications.

I. ACTIVITIES OF THE FOURTH QUARTER

A. INTRODUCTION

This section describes the technical research, development, and tests performed during the fourth quarter of contract NAS 5-10148, "Development of Multiple Source - Multiple Low Voltage Converter-Regulator Power Supply with Automatic Failure Sensing and Redundant Switching". This program has been a continuation and amplification of work completed under contract NAS 5-9212. The purpose of this program was the development of technologies for providing highly reliable LIVCR systems for space applications. The following were major areas of work required to define these technologies:

1. Development of automatic failure-sensing and compensation circuitry for the LIVC sections, PWM regulator power sections, and PWM regulator drive and control section of the redundant LIVCR.
2. Development of circuitry to establish phase-separated synchronization of redundant LIVCs.
3. Investigation of techniques to eliminate half-cycle unbalance in the LIVC power oscillator and to generally improve LIVC performance.
4. Development and study of circuitry to provide over-voltage protection for thermoelectric generators.
5. Consideration of techniques for switching redundant RTG sources.

The technologies developed during this program were applied to the fabrication of a 375-watt, breadboard-type LIVCR model for operation from a thermoelectric generator. The LIVCR model was delivered to NASA/GSFC.

The primary effort this fourth quarter involved fabrication and testing of the 375-watt, redundant LIVCR model with automatic failure sensing and compensation. During the fabrication and design testing, several design modifications, not indicated to be necessary during modular testing, were incorporated to improve the performance of the total LIVCR configuration. These modifications included:

1. A small filtering and resistor turn-off addition for the LIVC input switch.
2. Modification of the respective drive circuits for the PWM chopping transistor and for the transistor switch selecting the drive and control for the PWM chopping transistor.
3. Introduction of a monostable circuit to condition the regulator low-output voltage signal and a bistable operation of the failure identification logic for the drive and control section.
4. Replacement of the transistor control on the PWM power section isolation switch with an SCR.

These design modifications and results of the Design and Evaluation Department preshipment testing are discussed in the following paragraphs. The results of the LIVCR analysis conducted by the Reliability group are also presented.

B. TECHNICAL DISCUSSION

1. Electrical Design Review

The redundant low input voltage converter regulator with automatic failure compensation delivered on this contract is shown in figure 1. The Honeywell model number assigned is G2554A1. As shown in the block diagram of figure 2, the model includes: (1) four parallel redundant LIVC sections, (2) three parallel redundant PWM regulator power sections, and (3) two standby redundant PWM drive and control sections. The technology incorporated and contributing to improved power conditioning for space

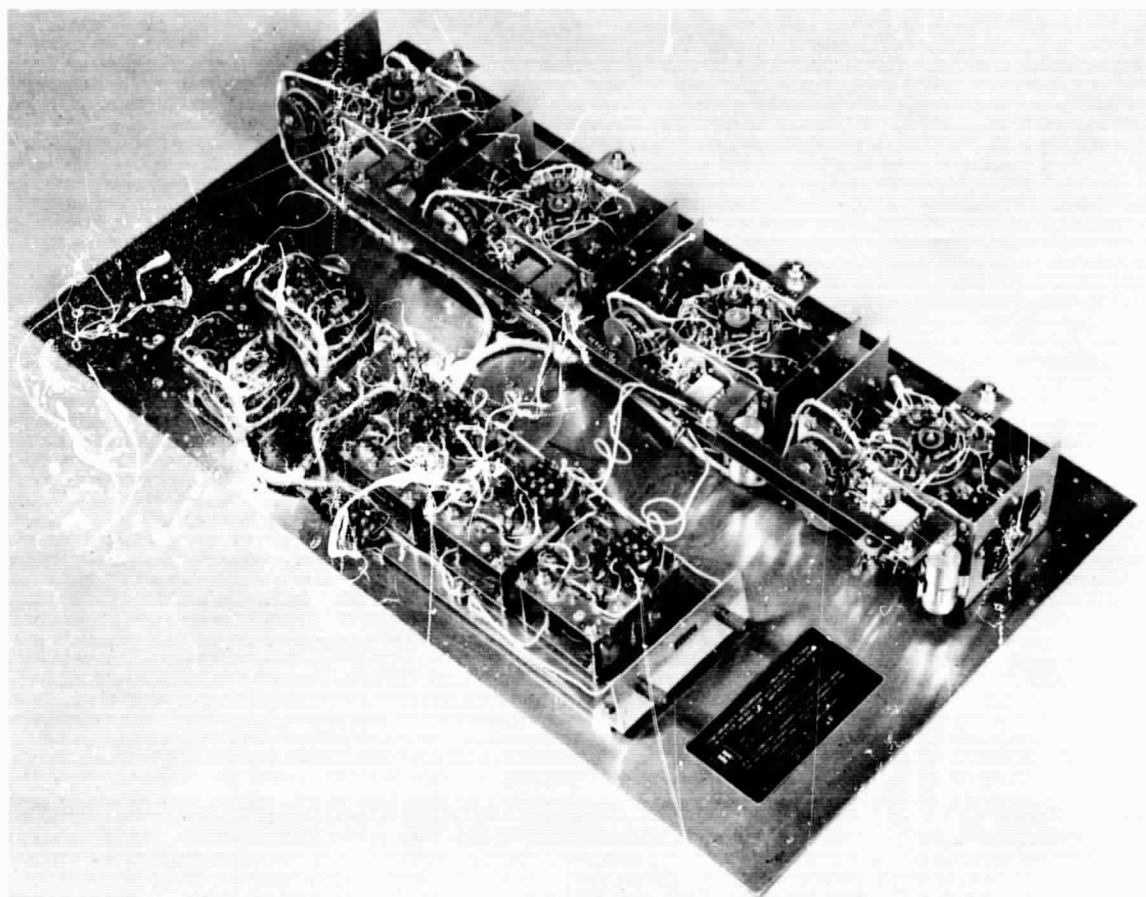


Figure 1 - LIVCR G2554A1, TOP VIEW

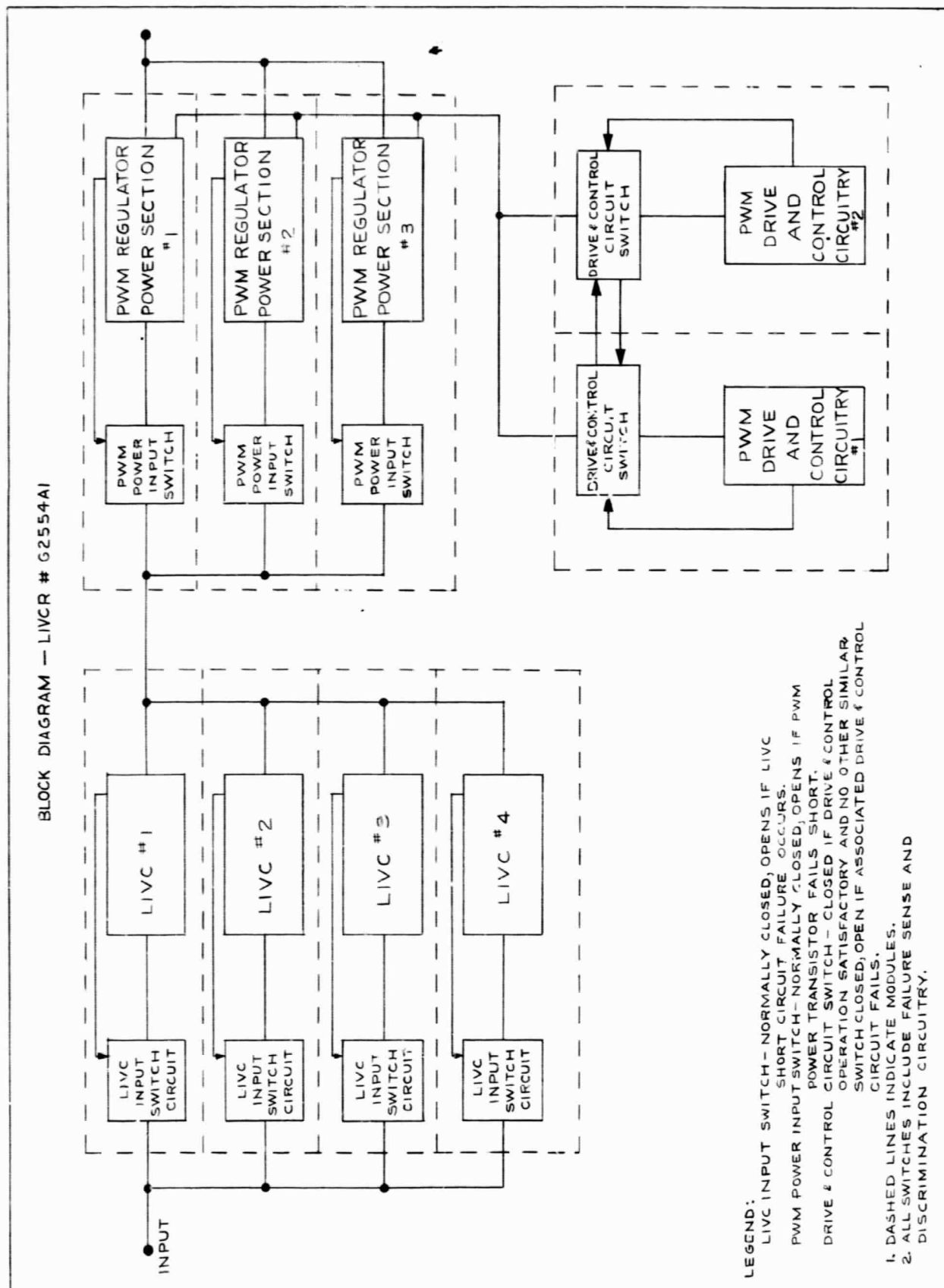


Figure 2 - BLOCK DIAGRAM - G2554A1

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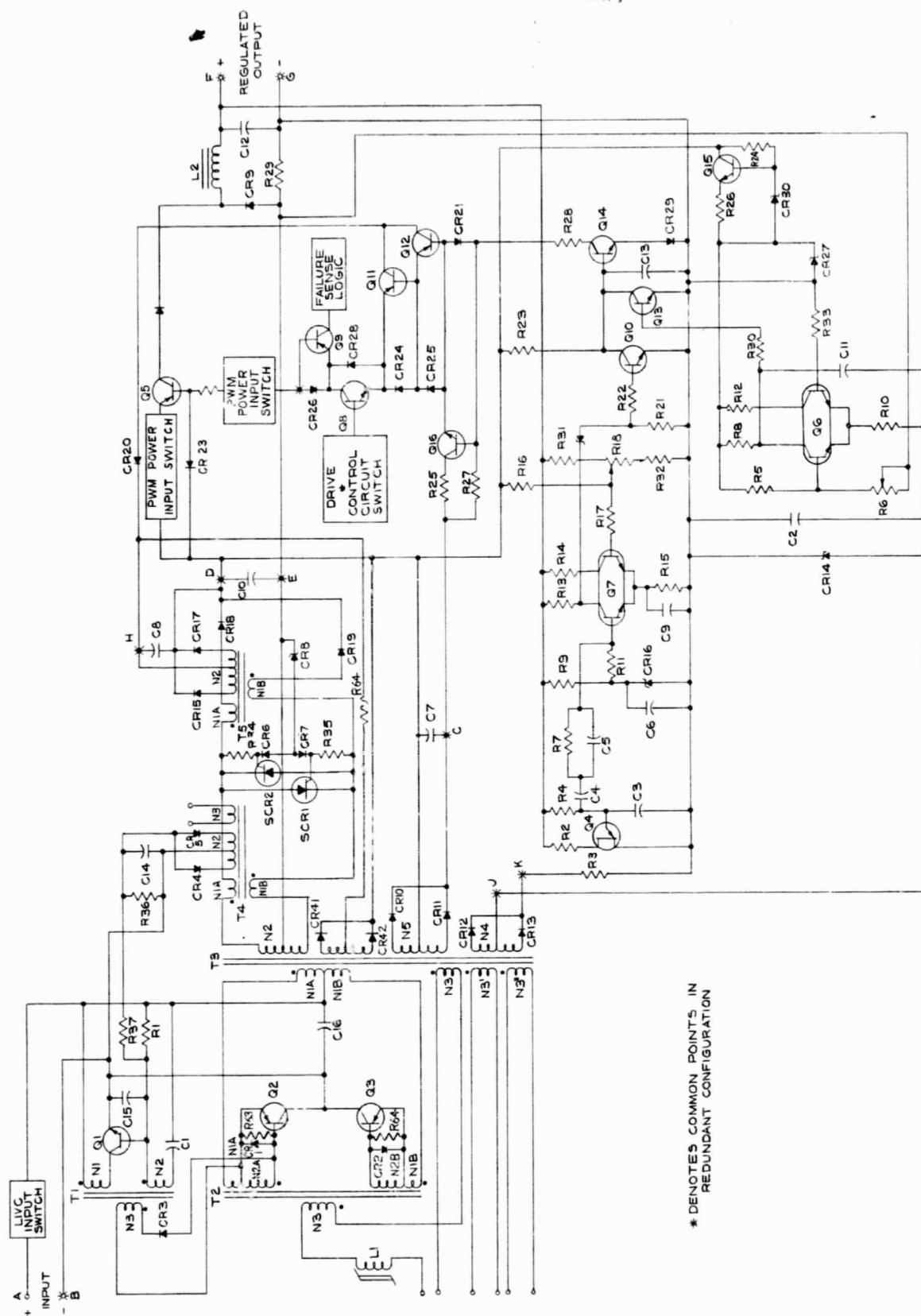
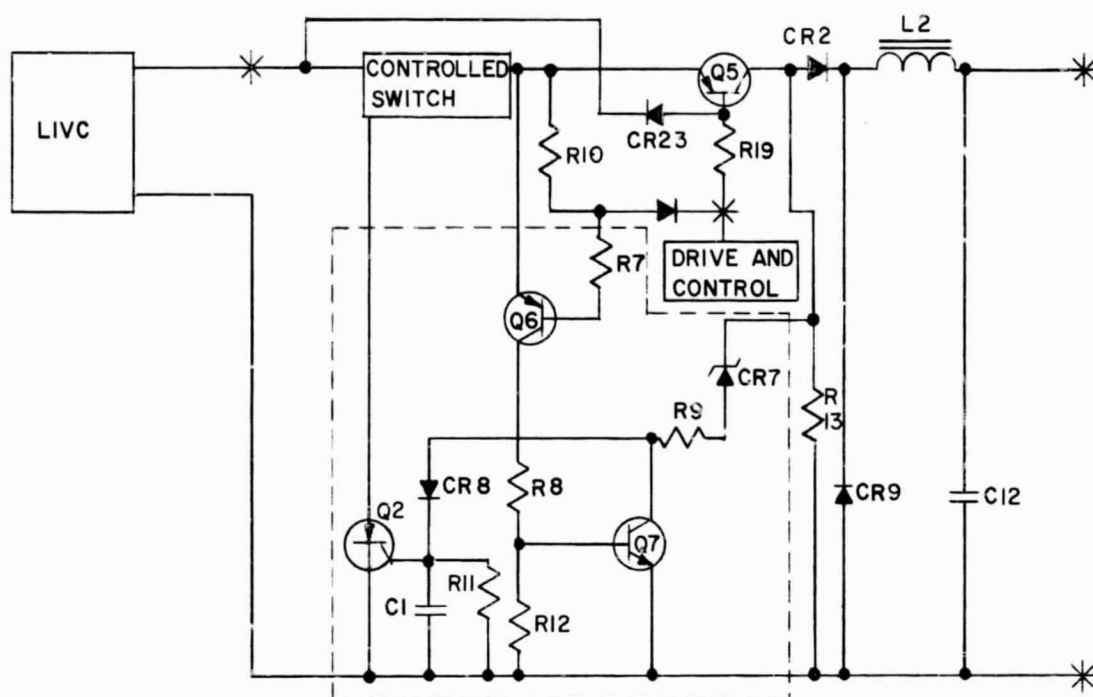


Figure 3 - CIRCUIT DIAGRAM FOR REDUNDANT LIVCR WITH AUTOMATIC FAILURE - COMPENSATION MODEL



Figure 4 - PWM DRIVE AND CONTROL FAILURE SENSING AND COMPENSATION - G2554A1



* DENOTES COMMON POINTS IN THE REDUNDANT CONFIGURATION

Figure 5 - SENSING AND ISOLATION OF SHORTED PWM TRANSISTOR - G2554A1

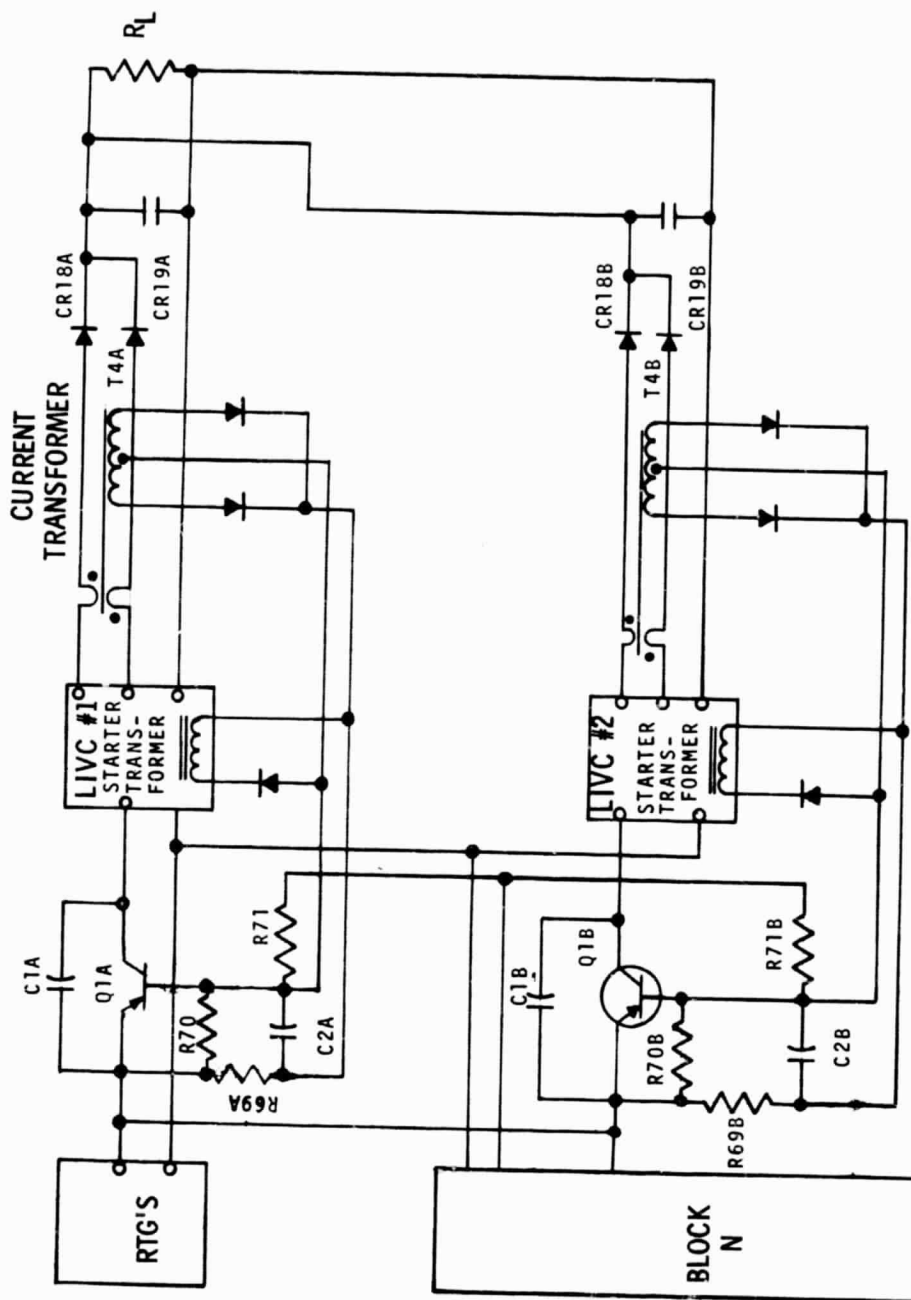


Figure 6 - FAILURE SENSING AND ISOLATION AT LIVCS INPUT

Q5 during this light load condition. When the regulator output current increases, the current proportional energy supplied increases and dominates as does the Q5 drive requirement. Therefore, drive proportional to that required is established at heavy load without requiring excessive drive power at light loads.

A constant-current drive for transistor switch Q8 has been introduced to remove a parallel path condition for drive currents (for Q8 versus Q5) which would have resulted in unsatisfactory operation. While the drive current paths for Q5 and Q8 are still essentially in parallel, control can now be exercised so that the drive current to Q8 is limited to a value which allows circuit design to also insure adequate drive to Q5. In the previous approach (figure 2, first quarterly report), the drive to each was dependent on semiconductor and resistor voltage drops in the respective parallel paths. While the circuit was designed to generally effect greater drive to Q5 than Q8, it was found that load and input voltage variations could quite easily upset the desired proportion, resulting in unsatisfactory operation. With the constant current control introduced, the desired operation was characteristic throughout the load and input voltage ranges. It should be noted that R62 and CR40 have been added to keep the Q17 leakage current to a sufficiently low value when Q20 is off.

Revisions in the automatic failure-sensing circuitry primarily involve: (1) introduction of a monostable stage to condition the low-output voltage signal and (2) a more direct bistable operation of respective section logic transistors (Q21). Refer to figure 4. These revisions were found to be advantageous during testing of the total redundant LIVCR, especially in the noisy environment of the laboratory. The monostable stage is directly applicable to increased stages of redundancy; the bistable operation obviously would require some modifications if additional redundancy is desired.

The monostable stage includes R38-R45, Q18, Q19, CR32-CR35, C17, and C18. Drive is normally supplied through R39 to Q18 so that Q19 is also held on. When the output voltage drops, CR32 and R39 no longer conduct; drive is supplied through R43 to Q18; Q19 is turned off and a voltage pulse is applied to R56 through C18 and CR35. C17 performs a speedup action and also slightly lengthens the time Q19 is held off. CR33 raises the Q19 emitter potential to facilitate turnoff; CR34 provides a discharge path for C18 when Q19 turns on again.

The bistable operation of Q21A and Q21B is effected by R55-R59 and C19 in the respective sections. When a pulse is applied to R56 through CR35, the Q21 (A or B) previously on, turns off, and the resulting pulse through C19 turns on the other Q21. R58 provides the DC drive path necessary. When a low voltage is indicated, both Q20's are also momentarily turned on through R51 to facilitate the transition between redundant sections.

The basic operation of the automatic failure-sensing circuitry for the PWM drive and control remains the same. A failure in the drive and control is still indicated and causes a new circuit to be used when:

1. The regulator output voltage is too low, or when
2. The regulator output voltage is too high and drive current is being supplied.

The high-voltage failure is indicated when CR31 conducts. If drive is being supplied, Q22 is off and the high-voltage signal flips Q21's and Q20's.

A small filter and regulation section for the failure-sensing logic has been provided by CR38, C20, and R54. This decreases possibility of noise and voltage fluctuations upsetting the normal logic operation.

b. Failure Sensing and Isolation of the PWM Chopping Transistor - The circuitry to sense and isolate a shorted PWM chopping transistor is shown in figure 5. This circuit includes several modifications of the circuit previously reported (figure 3, third quarterly report).

A significant modification is that the transistor controlling the relay isolation switch has been replaced with an SCR (Q2). The SCR introduces a latching action which makes it more directly amenable to a transistor replacement of the relay. It is emphasized that the relay has been included primarily to facilitate visual monitoring during model failure mode exercising. A transistor could easily be incorporated as a replacement.

A diode (CR10) has been introduced to provide reverse voltage protection for the Q6 emitter-base. Inclusion of R10 helps keep Q6 held off when no drive is applied to the chopping transistor Q5.

The point at which conduction of the chopping transistor Q5 is sensed has been moved to the Q5 collector. CR2 has been introduced for isolation to enable the circuitry to identify which of the redundant power sections has the shorted Q5. This isolation diode CR2 could also have been introduced at the regulator output. Locating CR2 at the output, however, would increase the losses during normal operation because of its continuous conduction there and would slow the correction of a failure mode. CR7 conducts whenever Q5 conducts (assuming adequate input voltage). The CR7 conducted signal, however, is shunted to ground through Q7 whenever drive is also supplied to Q5. Conduction of Q5 without drive constitutes a failure and Q2 then activates the controlled switch to isolate the failed chopping transistor.

c. Failure Sensing and Isolation at the LIVC's Input - The LIVC input switch circuitry to isolate failures of input capacitors, power transistors, or transformers, as shown in figure 6, is essentially the same as previously reported (figure 2, third quarterly report). The only modifications involve a resistor (R70) emitter-base to decrease leakage current and a resistor (R69) to provide a small amount of filtering for the base drive signal.

Testing of the redundant configuration emphasized the importance of properly sizing the filter capacitor, C2, and resistor, R70. Generally speaking, the input switch and associated LIVC in the configuration are easier to start when they are operated from independent RTG inputs. When the inputs are common, a large filter capacitor (greater than 33 MFD) makes it difficult to start all units in the configuration. This difficulty is due to the fact that C2 must charge to a value sufficient to maintain Q1 on when the LIVC is initially pulsed on by the starting circuit. If the capacitor is too large, its charge time (finite wire resistance, etc.) will be longer and result in an insufficient voltage buildup to sustain operation. The addition of R69 tends to slow C2 discharge without increasing charge time, but its size is limited by the allowable power dissipation and transformer T4 size.

Decreasing the resistance of R70 makes starting more difficult, especially in a common-input configuration. When the inputs are common, this resistance should be greater than when independent inputs are characteristic. When the inputs are independent, it is desirable, and in fact necessary, that R70 be smaller. A smaller R70 decreases Q1 leakage. Also, R70 must be of sufficiently low resistance to avoid actually forward biasing the emitter-base of Q1 when it should be off. Forward biasing could result if R70 is large by current flow from an RTG at 6 volts (unloaded) through R70 and R71 to the normal 3 volt RTG level of operational units and back to the common RTG negative. Recommended resistor values are indicated in the operating instructions.

2. Reliability Analysis of the Redundant LIVCR Configuration

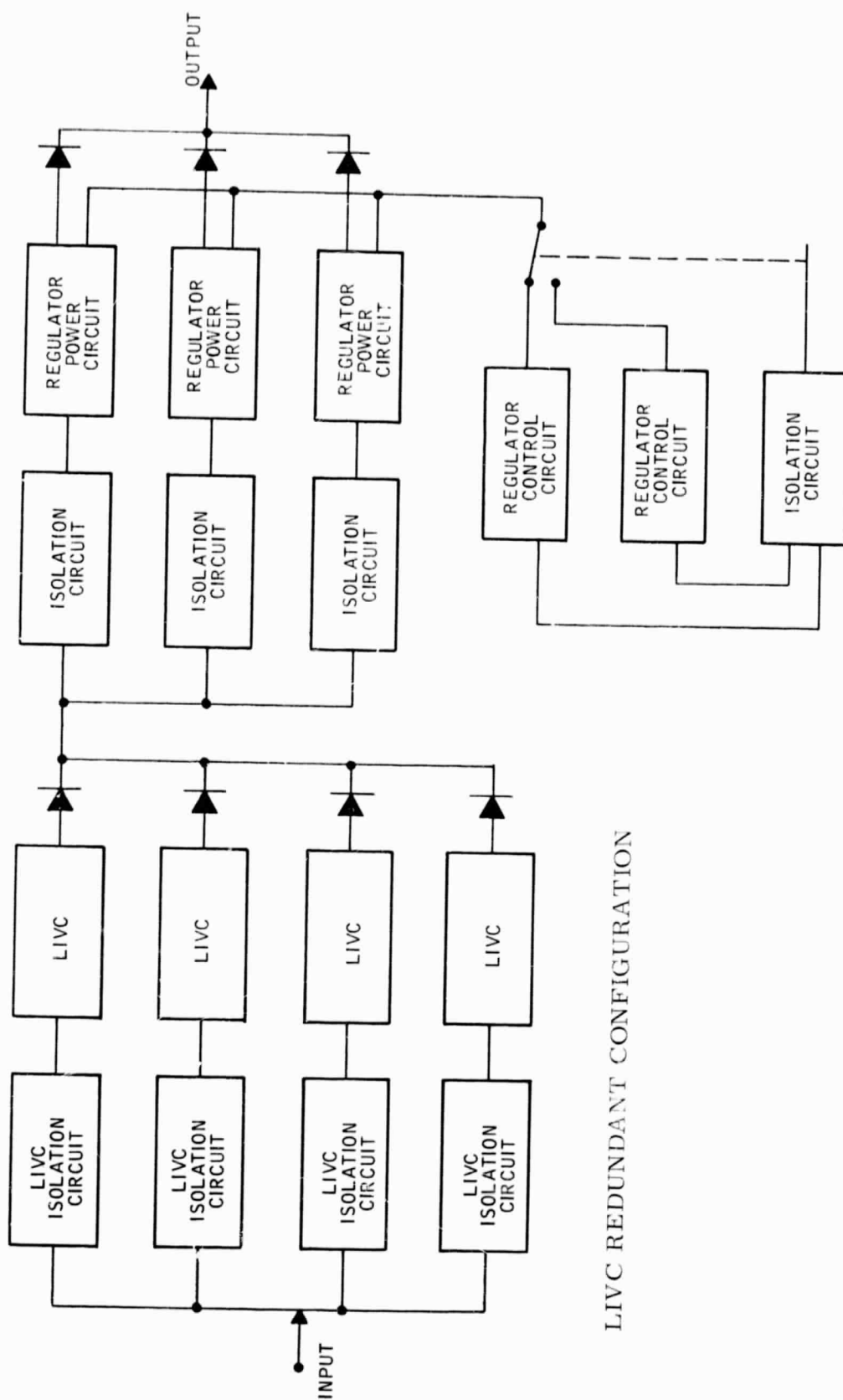
Analysis of the subject power-conversion system revealed a 99.44 percent probability of successfully completing a three-year mission. Additional analysis revealed that the reliability could be increased to 99.78 percent by addition of the LIVC output capacitor and pulse width modulator output capacitor and free-wheeling diode failure sense and isolation circuits.

The LIVCR configuration shown in figure 7-I was analyzed to determine the probability of successfully completing a three-year mission without a system failure.

The assumptions made in the analysis were as follows:

1. The exponential probability function is applicable.
2. Reliability estimates were based on the use of "high-rel" parts. Failure rates were not those of the hardware presently in use, but were realistic failure rates obtainable through usage of the "high-rel" parts.
3. Failures due to parameter variations were not considered in the analysis. When the LIVCs are to be incorporated into a spacecraft system, a detailed parameter variation analysis of the firm design should be conducted, and the effects of possible tolerance failures incorporated into the reliability assessment.
4. Reliability of the starting circuits of the LIVC and associated regulation and control circuits was considered to approach one. The reliability analysis of the firm design of a system to be used in a spacecraft application should also include a detailed analysis of the start-up reliability.
5. All parts are operated at 50 percent of rated stress except the converter power transistors and the regulator drive control switching transistors which were assumed to be operated at less than 10 percent of rated stress.

The probability equations generated for use in the analysis contain approximations for simplification. However, since the equations yield a somewhat pessimistic evaluation of system reliability, use of the equations to simplify the analysis is considered justified.



LIVC REDUNDANT CONFIGURATION

Figure 7-1 - RELIABILITY FIGURES

The reliability analysis was conducted by first separating the power-conditioning system into its three basic parts; i. e. , the inverter section, the regulator power section, and the regulator control section.

a. Analysis of the LIVC Section - System requirements dictate that three inverters must deliver power to the load for mission success. In figure 7-II, the blocks A_1 , A_2 , A_3 , and A_4 represent the failure isolation switches and the blocks B_1 , B_2 , B_3 , and B_4 represent the LIVCs. Each block exhibits a probability of failing in either an open or a short circuit failure mode. A short circuit in the "A" blocks is defined as a short from input to output that would effectively defeat the failure isolation function. A short in the "B" block(s) represent(s) a failure mode that would short the input power supply.

Under conditions of 25 percent degradation, the system will fail if more than one of the four inverters is not delivering power to the system. Therefore, any combination of failures that will prohibit more than one of the four inverters from delivering power to the load or any combination of failures that will short circuit the RTG power source will result in system failure. By use of this data, the probability of system failure was determined in the following manner:

I. If A_1 opens, system failure will occur if:

- a. A_2 or A_3 or A_4 opens
- b. B_2 or B_3 or B_4 opens
- c. B_2 or B_3 or B_4 shorts

which is represented mathematically by the following expression:

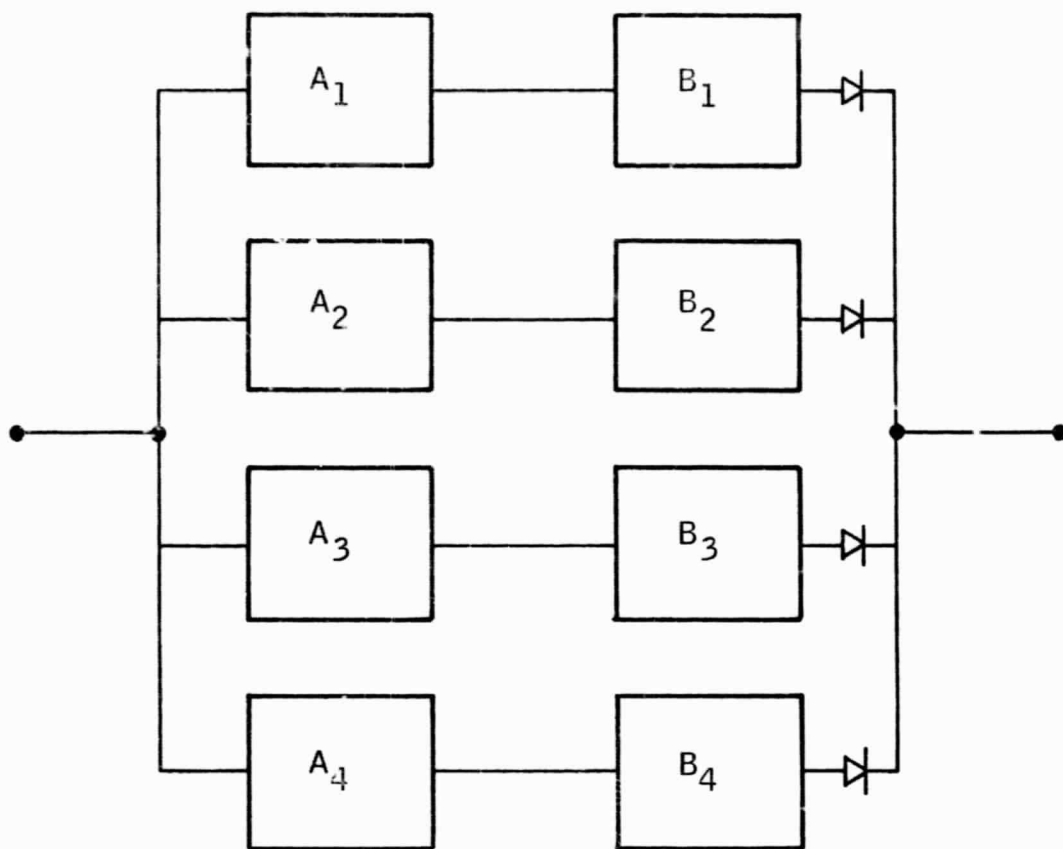


Figure 7-II - FAILURE ISOLATION AND LIVC BLOCKS

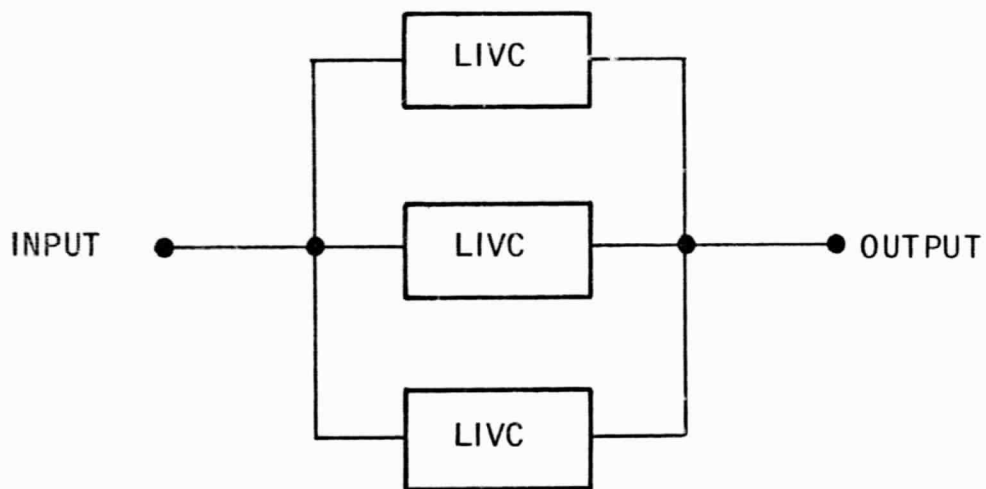


Figure 7-III - NON-REDUNDANT LIVCS

$$\begin{aligned}
 1. \quad P_F = & P_{A10} \cdot P_{A20} + P_{A10} \cdot P_{A30} + P_{A10} \cdot P_{A40} + P_{A10} \cdot P_{B20} \\
 & + P_{A10} \cdot P_{B30} + P_{A10} \cdot P_{B40} + P_{A10} \cdot P_{B2S} + P_{A10} \cdot P_{B3S} \\
 & + P_{A10} \cdot P_{B4S}
 \end{aligned}$$

Where: P_F = The probability of system failure

P_{A10} = The probability of A_1 failing in an open circuit failure mode.

P_{B10} = The probability of B_1 failing in an open circuit failure mode.

P_{B2S} = The probability of B_2 shorting in a short circuit failure mode.

II. If A_1 shorts, system failure will occur if B_1 fails in a short circuit failure mode. This is represented mathematically by:

$$2. \quad P_F = P_{A1S} \cdot P_{B1S}$$

Where: P_{A1S} is the probability of A_1 shorting and

P_{B1S} is the probability of B_1 shorting

Continuing the analysis for each condition by which failure may occur yields:

3. B_1 open condition

$$\begin{aligned}
 P_F = & P_{B10} \cdot P_{A20} + P_{B10} \cdot P_{A30} + P_{B10} \cdot P_{A40} + P_{B10} \cdot P_{B20} \\
 & + P_{B10} \cdot P_{B30} + P_{B10} \cdot P_{B40} + P_{B10} \cdot P_{B2S} + P_{B10} \cdot P_{B3S} \\
 & + P_{B10} \cdot P_{B4S}
 \end{aligned}$$

4. B₁ shorted condition

$$P_F = P_{B1S} \cdot P_{A20} + P_{B1S} \cdot P_{A30} + P_{B1S} \cdot P_{A40} + P_{B1S} \cdot P_{B20} \\ + P_{B1S} \cdot P_{B30} + P_{B1S} \cdot P_{B40} + P_{B1S} \cdot P_{B2S} + P_{B1S} \cdot P_{B3S} \\ + P_{B1S} \cdot P_{B4S}$$

5. A₂ open condition

$$P_F = P_{A20} \cdot P_{A30} + P_{A20} \cdot P_{A40} + P_{A20} \cdot P_{B30} + P_{A20} \cdot P_{B40} \\ + P_{A20} \cdot P_{B3S} + P_{A20} \cdot P_{B4S}$$

6. A₂ shorted condition

$$P_F = P_{A2S} \cdot P_{B2S}$$

7. B₂ open condition

$$P_F = P_{B20} \cdot P_{A30} + P_{B20} \cdot P_{A40} + P_{B20} \cdot P_{B30} + P_{B20} \cdot P_{B40} \\ + P_{B20} \cdot P_{B3S} + P_{B20} \cdot P_{B4S}$$

8. B₂ shorted condition

$$P_F = P_{B2S} \cdot P_{A30} + P_{B2S} \cdot P_{A40} + P_{B2S} \cdot P_{B30} + P_{B2S} \cdot P_{B40} \\ + P_{B2S} \cdot P_{B3S} + P_{B2S} \cdot P_{B4S}$$

9. A₃ open condition

$$P_F = P_{A30} \cdot P_{A40} + P_{A30} \cdot P_{B40} + P_{A30} \cdot P_{B4S}$$

10. A₃ shorted condition

$$P_F = P_{A3S} \cdot P_{B3S}$$

11. B₃ open condition

$$P_F = P_{B30} \cdot P_{A40} + P_{B30} \cdot P_{B40} + P_{B30} \cdot P_{B4S}$$

12. B₃ shorted condition

$$P_F = P_{B3S} \cdot P_{A40} + P_{B3S} \cdot P_{B40} + P_{B3S} \cdot P_{B4S}$$

13. A₄ shorted condition

$$P_F = P_{A4S} \cdot P_{B4S}$$

Combining terms

$$\begin{aligned} P_F = & P_{A0}^2 + P_{A0}^2 + P_{A0}^2 + P_{A0} \cdot P_{B0} + P_{A0} \cdot P_{B0} + P_{A0} \cdot P_{B0} \\ & + P_{A0} \cdot P_{BS} + P_{A0} \cdot P_{BS} + P_{A0} \cdot P_{BS} + P_{AS} \cdot P_{BS} + P_{A0} \cdot P_{B0} \\ & + P_{A0} \cdot P_{B0} + P_{A0} \cdot P_{B0} + P_{B0}^2 + P_{B0}^2 + P_{B0}^2 \\ & + P_{B0} \cdot P_{BS} + P_{B0} \cdot P_{BS} + P_{B0} \cdot P_{BS} + P_{A0} \cdot P_{BS} \\ & + P_{A0} \cdot P_{BS} + P_{A0} \cdot P_{BS} + P_{B0} \cdot P_{BS} + P_{B0} \cdot P_{BS} \\ & + P_{B0} \cdot P_{BS} + P_{BS}^2 + P_{BS}^2 + P_{BS}^2 + P_{A0}^2 + P_{A0}^2 \\ & + P_{A0} \cdot P_{B0} + P_{A0} \cdot P_{B0} + P_{A0} \cdot P_{BS} + P_{A0} \cdot P_{BS} \\ & + P_{AS} \cdot P_{BS} + P_{A0} \cdot P_{B0} + P_{A0} \cdot P_{B0} + P_{B0}^2 + P_{B0}^2 \\ & + P_{B0} \cdot P_{BS} + P_{B0} \cdot P_{BS} + P_{A0} \cdot P_{BS} + P_{A0} \cdot P_{BS} \end{aligned}$$

$$\begin{aligned}
& + P_{B0} \cdot P_{BS} + P_{B0} \cdot P_{BS} + P_{BS}^2 + P_{BS}^2 + P_{A0}^2 + P_{A0} \cdot P_{B0} \\
& + P_{A0} \cdot P_{BS} + P_{AS} \cdot P_{BS} + P_{A0} \cdot P_{B0} + P_{B0}^2 + P_{B0} \cdot P_{BS} \\
& + P_{A0} \cdot P_{BS} + P_{B0} \cdot P_{BS} + P_{BS}^2 + P_{AS} \cdot P_{BS} \\
& = 6 P_{A0}^2 + 12 P_{A0} \cdot P_{B0} + 12 P_{A0} \cdot P_{BS} + 4 P_{AS} \cdot P_{BS} + 6 P_{B0}^2 \\
& \quad + 6 P_{BS}^2 \\
& = 6 (4.7 \times 10^{-3})^2 + 12 (4.7 \times 10^{-3} \times 7.9 \times 10^{-3}) \\
& \quad + 12 (4.7 \times 10^{-3} \times 6.3 \times 10^{-3}) + 4 (1 \times 10^{-3} \times 6.3 \times 10^{-3}) \\
& \quad + 6 (7.9 \times 10^{-3})^2 + 6 (6.3 \times 10^{-3})^2 * \\
& = 0.00157
\end{aligned}$$

$$R \cong 99.84\%$$

An analysis was conducted to determine the improvement in reliability attained through the addition of the redundant inverter and the failure sensing and isolation circuits. The probability of failure of the non-redundant inverter shown in figure 7-III is equal to: P_F (total) = $3 P_F$ (LIVC) as all of the inverters must supply power to the system. Either a short or an open circuit in any of the three inverters will constitute a system failure; therefore,

$$P_F \text{ (LIVC Section)} = 3 (P_{FS} + P_{F0})$$

Where P_{FS} = Probability of a short circuit

and P_{F0} = Probability of an open circuit

$$P_F \text{ (LIVC Section)} = 3 (0.0063 + 0.0075) = 0.0214*$$

(This compares to a $P_F = 0.00157$ for redundant inverters.)

* Reference: tables A-1 through A-4.

b. Analysis of Power Regulator Section - Blocks A_1 , A_2 , and A_3 in figure 7-IV perform the function of isolating blocks B_1 , B_2 , and B_3 from the system if a short circuit failure occurs. Two B blocks are needed for system requirements. If a channel fails shorted; i. e., $A_1 \cdot B_1$ or $A_2 \cdot B_2$ or $A_3 \cdot B_3$ fails shorted, a system failure will occur.

The probability of failure of the power regulator is therefore determined as follows: P_F (system)

$$1. \quad P_{A10} \cdot P_{A20} + P_{A10} \cdot P_{A30} + P_{A10} \cdot P_{B20} + P_{A10} \cdot P_{B30} \\ + P_{A10} \cdot P_{B2S} + P_{A10} \cdot P_{B3S}$$

$$2. \quad P_{A1S} \cdot P_{B1S}$$

$$3. \quad P_{B10} \cdot P_{A20} + P_{B10} \cdot P_{A30} + P_{B10} \cdot P_{B20} + P_{B10} \cdot P_{B30} \\ + P_{B10} \cdot P_{B2S} + P_{B10} \cdot P_{B3S}$$

$$4. \quad P_{B1S} \cdot P_{A20} + P_{B1S} \cdot P_{A30} + P_{B1S} \cdot P_{B20} + P_{B1S} \cdot P_{B30} \\ + P_{B1S} \cdot P_{B2S} + P_{B1S} \cdot P_{B3S}$$

$$5. \quad P_{A20} \cdot P_{A30} + P_{A20} \cdot P_{B30} + P_{A20} \cdot P_{B3S}$$

$$6. \quad P_{A2S} \cdot P_{B2S}$$

$$7. \quad P_{B20} \cdot P_{A30} + P_{B20} \cdot P_{B30} + P_{B20} \cdot P_{B3S} + P_{B2S} \cdot P_{A30} \\ + P_{B2S} \cdot P_{B30} + P_{B2S} \cdot P_{B3S}$$

$$8. \quad P_{A3S} \cdot P_{B3S}$$

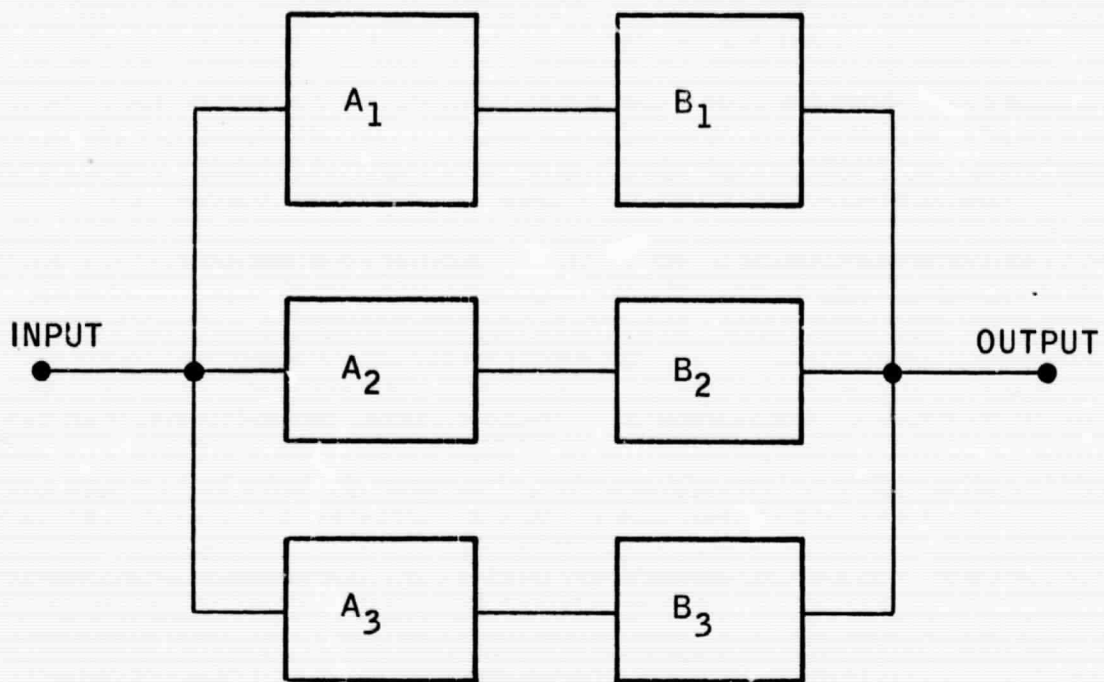


Figure 7-IV - FAILURE ISOLATION AND REGULATOR POWER SECTIONS

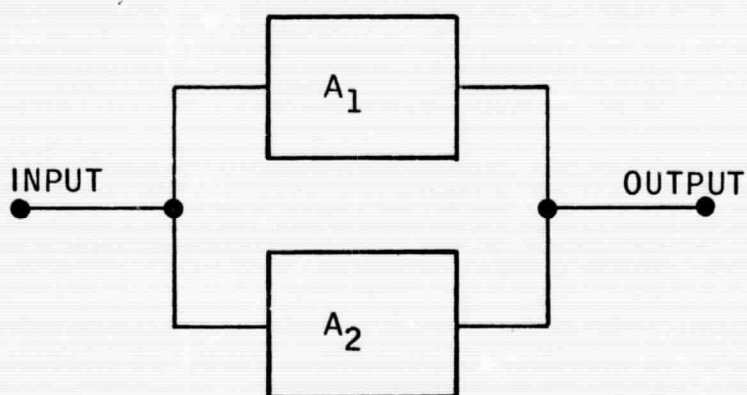


Figure 7-IV - NON-REDUNDANT REGULATOR POWER SECTION

If $P_{A1} = P_{A2} = P_{A3}$ and $P_{B1} = P_{B2} = P_{B3}$

Then

$$\begin{aligned}
 P_F (\text{system}) = & P_{A0}^2 + P_{A0}^2 + P_{A0} \cdot P_{B0} + P_{A0} \cdot P_{B0} + P_{A0} \cdot P_{BS} \\
 & + P_{A0} \cdot P_{BS} + P_{AS} \cdot P_{BS} + P_{A0} \cdot P_{B0} + P_{A0} \cdot P_{B0} \\
 & + P_{B0}^2 + P_{B0}^2 + P_{B0} \cdot P_{BS} + P_{B0} \cdot P_{BS} + P_{A0} \cdot P_{BS} \\
 & + P_{A0} \cdot P_{BS} + P_{B0} \cdot P_{BS} + P_{B0} \cdot P_{BS} + P_{BS}^2 + P_{BS}^2 \\
 & + P_{A0}^2 + P_{A0} \cdot P_{B0} + P_{A0} \cdot P_{BS} + P_{AS} \cdot P_{BS} + P_{A0} \cdot P_{B0} \\
 & + P_{B0}^2 + P_{B0} \cdot P_{BS} + P_{AS} \cdot P_{BS}
 \end{aligned}$$

$$\begin{aligned}
 \text{Combining terms: } & 3 P_{A0}^2 + 6 P_{A0} \cdot P_{B0} + 6 P_{A0} \cdot P_{BS} + 3 P_{AS} \cdot P_{BS} \\
 & + 6 P_{B0} \cdot P_{BS} + 3 P_{B0}^2 + 3 P_{BS}^2
 \end{aligned}$$

$$\begin{aligned}
 P_F = & 3 (P_{A0}^2 + P_{B0}^2 + P_{BS}^2 + P_{AS} \cdot P_{BS}) \\
 & + 6 (P_{A0} \cdot P_{B0} + P_{A0} \cdot P_{BS} + P_{B0} \cdot P_{BS})
 \end{aligned}$$

Therefore:

$$\begin{aligned}
 P_F = & 3 [(1.2 \times 10^{-4})^2 + (2.3 \times 10^{-3})^2 + (4 \times 10^{-4})^2 \\
 & + (1.2 \times 10^{-4}) (4 \times 10^{-4})] \\
 & + 6 [(1.2 \times 10^{-4}) (2.3 \times 10^{-3}) + (1.2 \times 10^{-4}) (4 \times 10^{-4}) \\
 & + (2.3 \times 10^{-3}) (4 \times 10^{-4})] \\
 = & 0.000024 \text{ and Reliability} = 0.999976
 \end{aligned}$$

$$\text{As: } P_{A0} = 0.00012^*$$

$$P_{AS} = 0.002$$

$$P_{B0} = 0.0023$$

$$P_{BS} = 0.0004$$

An analysis was also conducted to determine the improvement in reliability attained through the addition of the redundant power regulator and the failure - sensing and isolation circuits.

In the non-redundant configuration shown in figure 7-V, if either A_1 or A_2 short circuit (input to output), a power-conditioning system failure would result. An open circuit failure in either inverter would also result in a system failure. The probability of failure for the non-redundant configuration is therefore:

$$P_F = P_{A1S} + P_{A2S} + P_{A10} + P_{A20}$$

If A_1 is identical to A_2 then

$$P_F = 2(P_{AS} + P_{A0})$$

Where P_{AS} = Probability of a short circuit

and P_{A0} = Probability of an open circuit

The probability of failure for the regulator section is:

$$P_F = 2(0.0004) + 2(0.0023)$$

$$= 0.0008 + 0.0046$$

$$= 0.0054$$

(This compares to $P_F = 0.000024$ for redundant power sections.)

* Reference tables A-6 through A-8 in the appendix section.

c. Analysis of the Regulator Drive Control Section - The probability of success for the standby redundant regulator drive control section shown in figure 7-VI was determined by the standby redundancy relationship*:

$$R = e^{-\lambda_o t} \left[1 + \left(\frac{\lambda_o}{\lambda_s} \right) (1 - e^{-\lambda_s t}) R_{sw} \right]$$

Where:

λ_o = The failure rate of the primary drive control

R = The reliability of the redundant configuration

λ_s = The failure rate of the standby circuit

t = The mission time duration

R_{sw} = The switching reliability

$$\lambda_o = \lambda_s = 0.057/1000 \text{ hours}^{**}$$

$$t = 2.63 \times 10^4 \text{ hours}$$

$$\lambda_o t = \lambda_s t = 5.7 \times 10^{-7} \times 2.63 \times 10^4 = 14.99 \times 10^{-3}$$

$$e^{-\lambda_o t} = e^{-\lambda_s t} \approx 0.85$$

$$R = 0.985[1 + 1(1 - 0.985) 0.9989]^{**}$$

$$= 0.985 [1 + 1(0.01498)]$$

$$R = 0.99976$$

*"A Comprehensive Reliability Analysis of Redundant Systems," R. S. Pringle and P. M. Gresho, Journal of Spacecraft, Volume 4, Number 5, May, 1967.

** Reference: table A-10

*** Reference: table A-11

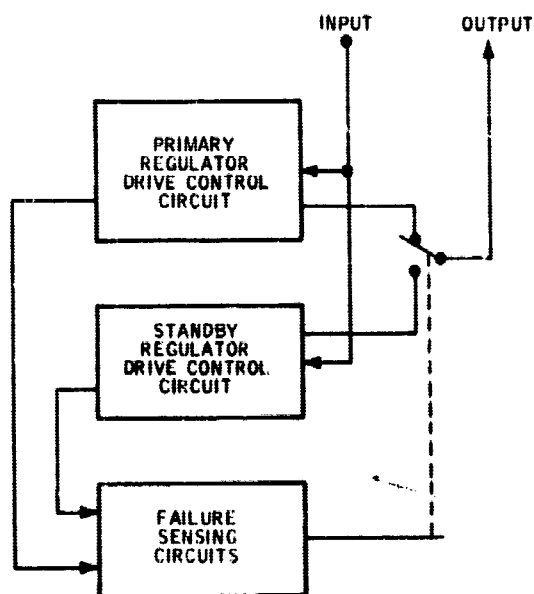


Figure 7-VI - REGULATOR DRIVE CONTROL REDUNDANT CONFIGURATION

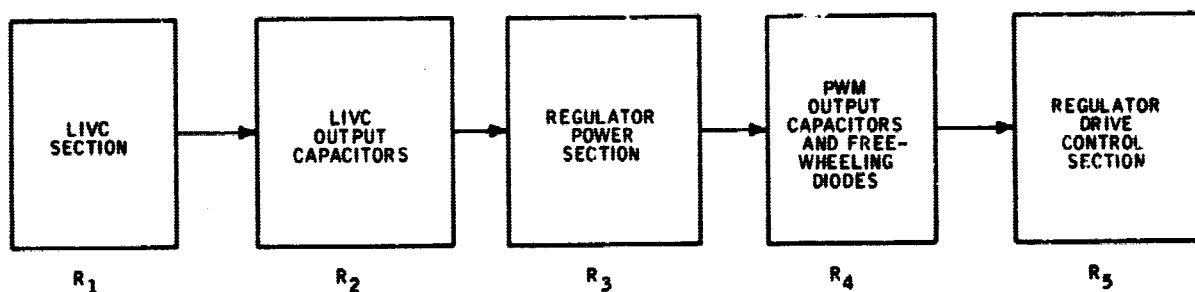


Figure 7-VII - REDUNDANT LIVCR RELIABILITY DIAGRAM

d. Analysis of Power Regulator Section with Output Capacitor Failure

Isolation Provisions - Addition of the PWM output capacitor and free-wheeling diode failure-sensing and isolation circuits required addition of the output capacitor and free-wheeling diode failure rates into the probability equation given in the analysis of the tri-redundant regulator. Therefore:

$$P_F = 3 (P_{A0}^2 + P_{B0}^2 + P_{BS}^2 + P_{AS}P_{BS}) \\ + 6 (P_{A0}P_{B0} + P_{A0}P_{BS} + P_{B0}P_{BS})$$

is applicable. Added components effectively increased P_{A0} from 0.00012 to 0.0007. P_{AS} and P_{B0} did not change and P_{BS} increased from 0.0004 to .0030.

$$P_{A0} = 0.0007, P_{AS} = 0.002$$

$$P_{B0} = 0.0023, P_{BS} = 0.003$$

$$P_F = 3 (P_{A0}^2 + P_{B0}^2 + P_{BS}^2 + P_{AS}P_{BS}) \\ + 6 (P_{A0}P_{B0} + P_{A0}P_{BS} + P_{B0}P_{BS}) \\ = 3 [(7 \times 10^{-3})^2 + (2.3 \times 10^{-3})^2 + (3 \times 10^{-3})^2 + (2 \times 10^{-3})(3 \times 10^{-3})] \\ + 6 [(7 \times 10^{-4})(2.3 \times 10^{-3}) + (7 \times 10^{-4})(3 \times 10^{-3}) \\ + (2.3 \times 10^{-3})(3 \times 10^{-3})] \\ = 3 [49 \times 10^{-6} + 5.29 \times 10^{-6} + 9 \times 10^{-6} + 6 \times 10^{-6}] \\ + 6 [1.61 \times 10^{-6} + 2.1 \times 10^{-6} + 6.9 \times 10^{-6}] \\ = 3 (69.3 \times 10^{-6}) + 6 (10.6 \times 10^{-6}) = 207.9 \times 10^{-6} + 63.6 \times 10^{-6} \\ = 271.5 \times 10^{-6} = 2.71 \times 10^{-4} \\ = 0.9997$$

e. Analysis of LIVC Section with Output Capacitor Failure Isolation Provisions -

The LIVC output capacitor failure-sensing and isolation circuit effectively reduces probability of system failure due to a shorted capacitor to a negligible value. Addition of the circuit does, however, increase the probability of failures that would isolate a power converter from the system. The failure rate for open inverter failures was increased by 0.0057 percent / 1000 hours. (See appendix A, tables 12 and 13.)

The LIVC redundant equation

$$P_F = 6P_{A0}^2 + 12P_{A0}P_{B0} + 12P_{A0}P_{BS} + 4P_{AS}P_{BS} + 6P_{B0}^2 + 6P_{BS}^2$$

was used to evaluate the revised reliability estimate for the LIVC section. The revised reliability of the LIVC sections and the now included output capacitor is 0.9983.

f. Resulting Redundant LIVCR Configuration Reliability - Subsequent to the determination of the reliability of the LIVC, regulator power, and regulator drive sections, a new probability diagram for the total power-conditioning system was drawn as shown in figure 7-VII. The system reliability is therefore the product of the probability of success of the sections; i. e.,

$$\begin{aligned} R_{\text{system}} &= R_1 \times R_2 \times R_3 \times R_4 \times R_5 \\ &= 0.9984 \times 1.9989 \times 1.9999 \times 0.9974 \times 0.99976* \end{aligned}$$

*Reference: tables A-1 through A-11.

Since the system operation has been described by a series probability diagram, it can be easily shown that reliability improvement can be achieved by combining these system functions in a logical manner. This has been done by combining the PWM output capacitors and free-wheeling diodes as an integral part of the regulator power section and also by combining the LIVC output capacitors with the LIVC section. These combinations are presented in the following paragraphs with the PWM output capacitor and free-wheeling diode failure-sensing and isolation circuit combined with the regulator power section.

The system reliability computation, R system, was then computed in the manner shown below:

$$\begin{aligned}
 R_{\text{system}} &= R(\text{LIVC Sections}) \times R(\text{LIVC output capacitors}) \\
 &\quad \times R(\text{Regulator power section}) \times R(\text{Regulator drive control}) \\
 &= 0.9984 \times 0.9989 \times 0.9997 \times 0.99976 \\
 &= 99.68\%
 \end{aligned}$$

The system reliability computation, R system, with the LIVC output capacitor and the PWM output capacitor and free-wheeling diode failure-sensing and isolation circuits, was then computed in the following manner:

$$\begin{aligned}
 R_{\text{system}} &= R(\text{LIVC Section}) \times R(\text{Regulator power section}) \\
 &\quad \times R(\text{Regulator drive control section}) \\
 &= 0.9983 \times 0.9997 \times 0.99976 \\
 &= 99.78\%
 \end{aligned}$$

3. Testing and Performance

Testing conducted on the total LIVCR redundant configuration included quite extensive design testing and Evaluation Department preshipment testing (appendix B). These tests were conducted in addition to the design evaluation of each module's performance and of the interface between specific modules performed earlier in the program. The primary difference noted in testing the total configuration (versus simple modules, etc.) was the small signal noise generated by some sections which then affected performance of others. The noise generation was amplified by line fluctuations and other noise inherent in the laboratory. The generated noise primarily affected the failure identification logic. While the initial performance which resulted was not totally unacceptable, design changes were made to eliminate the noise influence on performance.

Specific modes of operation which were improved include: (1) the positive and immediate correction of all failures regardless of the previous order of failure simulations and (2) the decreased time required to sense and isolate or correct a simulated failure. The response time between failure occurrence and correction exhibited by the delivered model is not the minimum attainable with the technology implemented. The performance exhibited, however, is adequate to prove feasibility of the concepts. Knowing specific requirements of a real application would allow the designer to specify component values to move the performance characteristics in the direction desired.

During evaluation of the LIVCR performance, the four redundant LIVCs were first operated into a resistive load. Phase separation of approximately 45° was found to be characteristic throughout the testing with four units operational. The failure isolation circuitry performed satisfactorily both with common and independent LIVC inputs from simulated RTGs. When operating from a common input, the efficiency of the configuration decreased only slightly (few percent), while maintaining the load when an LIVC failure was simulated and effectively isolated. During operation from separate

inputs, the efficiency of the configuration did not change, but the total source power which could be utilized was decreased when an LIVC failure was simulated (no source switching). The typical LIVC efficiencies measured are shown in table I.

TABLE I
TYPICAL LIVC EFFICIENCY
(COMMON INPUTS)

<u>Number of Operating LIVCs</u>	<u>Input Voltage</u>	<u>Output Voltage</u>	<u>Output Power (Watts)</u>	<u>Efficiency</u>
1	3.0	38.0	75	87%
1	3.8	50.0	75	92%
2	3.0	38.0	150	87%
3	3.0	38.0	206	86%
4	3.0	38.0	265	86%

The LIVC efficiency was still increasing with load, indicating that the fixed losses were still greater than those proportional to load. All efficiency figures include the losses of the input transistor switch. It should be noted that the output voltage is quite high (38 volts at 3.0 volts in), considering the 28-volt regulator output. While this requires that the regulator work harder and decrease its efficiency, the higher LIVC output voltage separates the input voltage level at which the regulator input impedance changes and the maximum power point voltage of the intended RTG source. The indicated separation, while more than adequate, tends to promote a smoother transition through the maximum power point. A regulated output is actually allowed with input voltages as low as 2.6 volts, providing the source power capability is adequate.

The efficiency characteristics of the total LIVCR redundant configuration is shown in figure 8. Efficiencies of greater than 75 percent are realized over the load range of approximately 125 watts to 375 watts. The losses of the LIVC input switch and other failure isolation circuitry are included in this determination. Utilizing the information in figure 8 and table I, a regulator efficiency of approximately 90 percent is characteristic with a 3.0-volt LIVC input. As stated previously, the regulator efficiency would be higher if the LIVC output voltage were lower.

There is reason to believe that the output ripple reported in appendix B includes some line ripple. The ripple period is indicated to be 4 milliseconds which corresponds more to the line frequency of the source (simulating the RTG) than the 2.7-kilohertz frequency of the regulator.

The overall performance of the redundant LIVCR was measured to be quite satisfactory. The advantages of the technology incorporated, borne out in laboratory testing, indicate a significant contribution to power-conditioning capabilities for future space flight application.

4. Redundant Configuration Considerations

The specification of a redundant RTG-LIVCR configuration is dependent on (1) the failure modes predominant in respective sections, (2) the relative ease with which these modes can be compensated for in specific configurations, and (3) operating characteristics of each section, during normal conditions, which are a function of the configuration. Some initial consideration was given to various configurations in the third quarterly report (section I. B. 5, pp. 20-25). In that discussion, it was implied that proven reliability figures for the RTG had not been secured; the lack of proven reliability data makes it unrealistic to positively recommend specific configurations involving the RTG. General observations concerning the RTG configuration and additional effects on the LIVCR, however, are discussed in the following paragraphs.

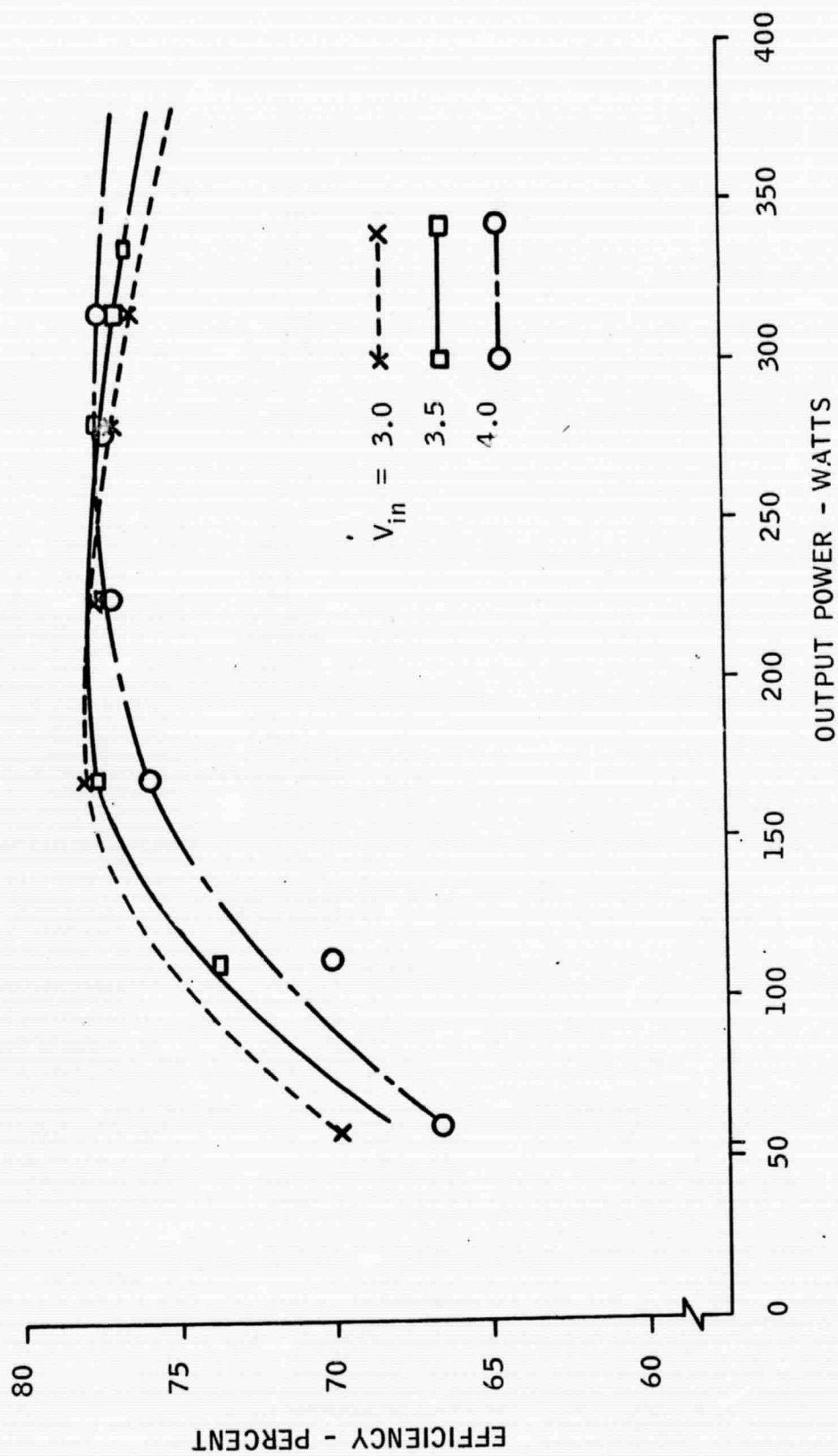


Figure 8 - EFFICIENCY CHARACTERISTICS OF REDUNDANT LIVCR -
 G2554A1

A common RTG output-common LIVC input would yield the simplest failure-isolation circuitry for each, while realizing maximum usage of operational modules after redundant failures. Incorporation of an SCR overvoltage circuit (Figure 3) for the RTGs in each LIVC output, however, is not then permissible unless each LIVC in the redundant configuration is capable of handling the total RTGs maximum output current. The firing of a single SCR circuit would require the associated LIVC to handle the total RTG output for that half-cycle. The SCR circuit to fire, and the LIVC to conduct, next would be somewhat random and depend on specific SCR gate characteristics and the external load. In each case, however, the single LIVC must indeed be capable of handling the total RTG output. Sizing each LIVC to handle this maximum current will require a significant sacrifice (increase) in total LIVC weight and volume unless the degree of redundancy is limited to two. With a redundancy of only two, each must be designed to handle full RTG output anyway; however, if a redundancy of three were characteristic, the designer would normally expect that each would instead be required to handle a maximum of one-half the RTG output (assuming one failure allowable). Requiring each of three to handle full rather than one-half the RTG output would result in approximately twice the total LIVC size and weight; the sacrifice becomes even more severe as redundancy is increased.

An approach which may lend itself to a common RTG output-LIVC input without requiring a weight sacrifice involves a transistor, shunt-type PWM regulator in the common LIVC output. The shunt PWM regulator would then provide both output voltage regulation and RTG overvoltage protection. The LIVC output would then be short-circuited for a portion of each regulator cycle, even during normal load conditions. The LIVCs would normally share current quite well with a common output short circuit; if current sharing is not realized, a current level sense transformer controlling the input switch could be incorporated to protect against excessive current conduction by any one LIVC. A very significant and undesirable feature of this mode of operation,

however, is that synchronization of the redundant LIVCs could be upset by operation of the shunt PWM regulator. It is possible that LIVC synchronization can be maintained, however, if the shunt PWM regulator frequency is an even multiple of the LIVCs and is synchronized with the LIVCs.

Separate LIVC inputs provide several LIVC operating advantages; however, more complex switching provisions at the RTG-LIVC interface are required for maximum usage of operational modules after redundant failures. The advantages include: (1) more positive current sharing, (2) allowing use of SCR overvoltage circuits, and (3) easier LIVC starting. Additional switch paths (versus common input) would have to be provided to enable an RTG to be used after its originally associated LIVC fails, or vice versa.

A realistic configuration compromise may involve limited common inputs. For example, two sets of two parallel-connected RTGs could power two sets of two parallel LIVCs. Several other alternatives exist to make both a common input or a separate input configuration feasible. The final configuration chosen will be dependent on power levels involved and more complete RTG reliability data.

5. Package Layout and General Operating Procedures

The package layout of the delivered model (Honeywell #G2554A1) is basically of the breadboard, modular addition type. A top view of the model is shown in figure 1; front and back views are shown in figures 9 and 10 respectively.

Each of the four redundant LIVCs has a self-contained transistor input switch; the terminals of the transistor switch can be seen in figure 9 on the positive input plates. Small signal interwiring between LIVCs provides the connections necessary to effect phase-separated LIVC oscillator synchronization.

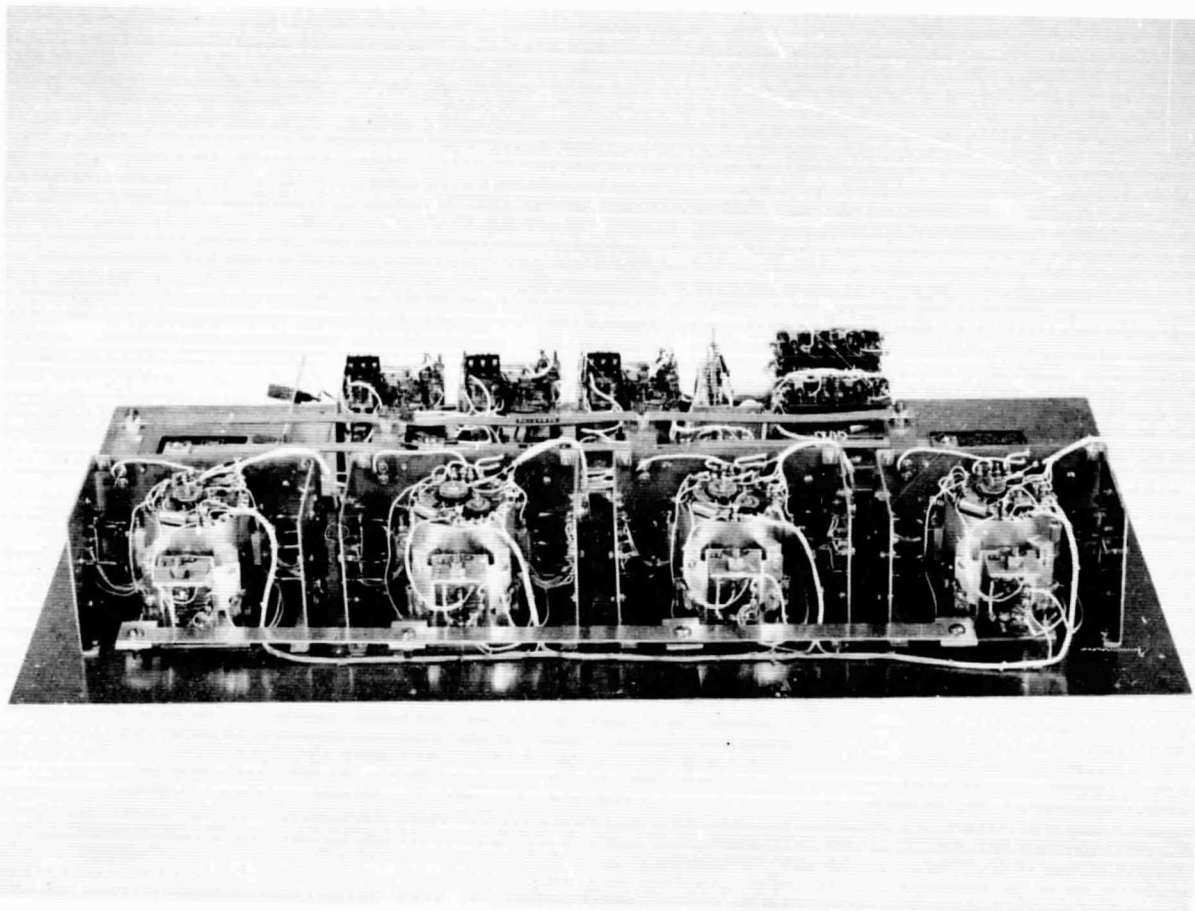


Figure 9 - LIVCR G2554A1, FRONT VIEW

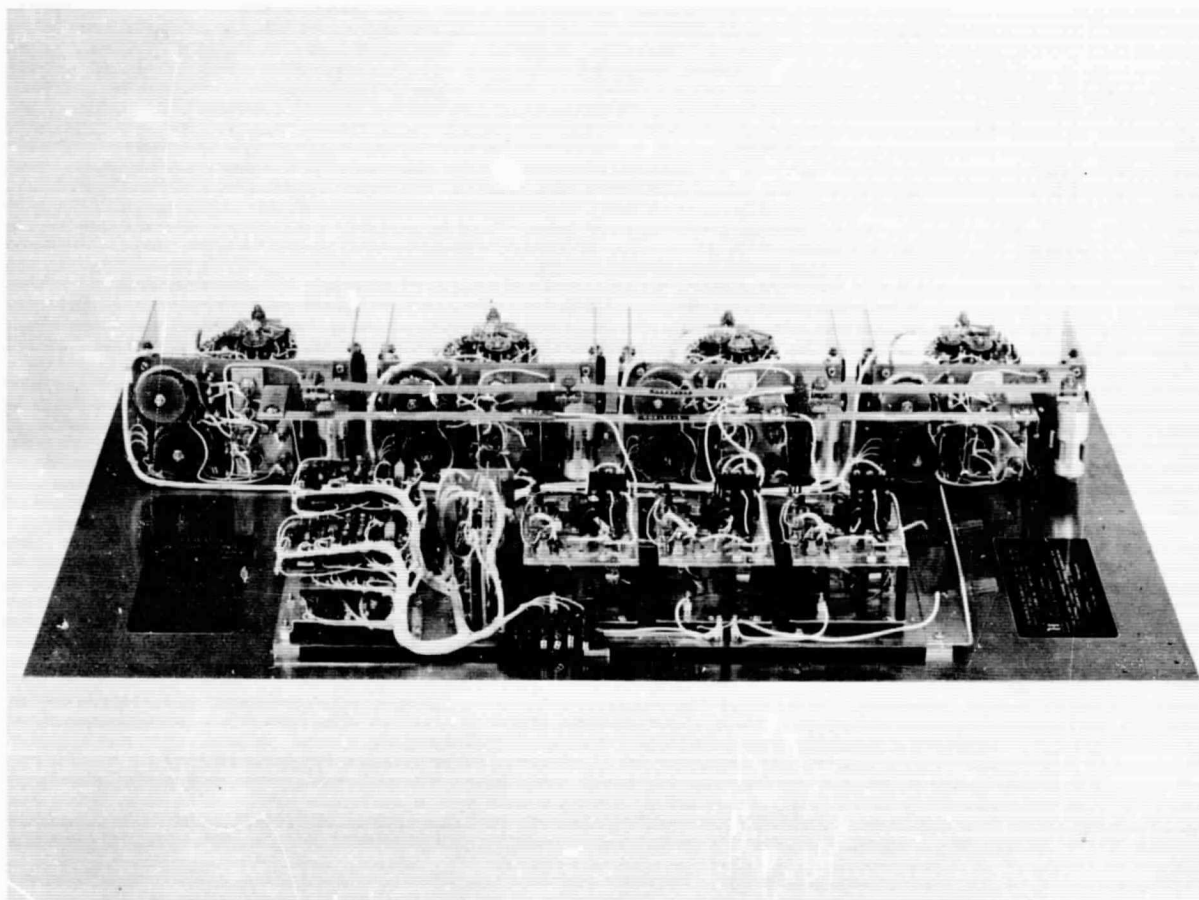


Figure 10 - LIVCR G2554A1, BACK VIEW

The three redundant PWM regulator power sections are located near the regulator output terminals (figure 10). The respective failure-sensing and isolation circuitry is located on board number 14; the output capacitors and choke coils are located on board number 15.

The two redundant PWM regulator drive and control with automatic failure-sensing circuits are located near the operating instruction tag. The top two boards (number 19 and number 20) in each stack contain the regulator control electronics; circuit boards number 21 contain the high-voltage sensing and failure identification circuits; the bottom boards, number 22, contain drive circuit elements and the respective drive isolation switches. The low-voltage sensing and conditioning circuitry is located on board number 17 between the drive and control electronics and regulator power sections.

The operating instructions indicated on the model are reasonably complete. They will be repeated here, however, with additional explanation for report completeness.

1. Do not exceed input voltage of 6.0 volts. If the voltage were exceeded, voltage stress exceeding the ratings would be put on the input switch (when off) and the secondary circuitry.
2. If SCR circuits are connected, operate only with separate LIVC inputs from high-impedance sources. A common input or a low-impedance source connection could cause excessive individual LIVC loading when its SCR circuit fires.
3. To connect the SCR circuit, wire zener diode (45 to 60 volts) on each LIVC output with cathode on terminal 1 and anode on terminal 2. The zener diode will connect the SCR gates to allow firing upon receiving a high-voltage signal.

4. If operated from separate high-impedance sources, the 100-ohm resistor on the input switch should be changed to 22 ohms (R70 on schematic). See figure 6. If the resistor (R70) is too large, the voltage drop across it will turn on the input switch even when it is desired off.
5. To reset relays isolating PWM power transistors, LIVCR input power should be removed. The relays latch when activated and voltage must be decreased to break latching current flow.
6. To simulate PWM control, "no drive failure," short point 3 (base of Q14 on schematic) to ground. Other points for failure simulation can also be selected on circuit boards if desired.
7. To simulate PWM control, "drive, or full on, failure," short point 4 (collector of Q14) to ground. Again this is one of several possible simulations, but is quite representative and convenient for exercising the failure-sensing and compensation circuitry.

The output voltage and overload current set points can be adjusted with potentiometers R18 and R6 respectively. The output voltage levels for the respective control circuits have purposely been set differently to aid in determining which is assuming control.

II. REVIEW OF PROGRAM ACCOMPLISHMENTS

A. SYNCHRONIZATION OF FOUR REDUNDANT LIVCs

The synchronization circuitry developed by Honeywell on contract NAS-5-9212 for two and three redundant LIVCs respectively was extended on this contract (NAS-5-10148) to provide phase-separated synchronization of four redundant LIVCs. The synchronization circuit, as incorporated in the delivered model, is shown in figure 11. General design postulates used in its development and the performance exhibited is commensurate with that for two and three LIVCs. The basic circuitry algebraically sums individual LIVC phase voltages; application of those summations to respective LIVCs frequency determining inductors effects phase separation between respective oscillator switchings. Advantages provided by this operation are: 1) reduction of line transients and related component stress, 2) improved stability, and 3) the provision for polyphase AC outputs.

Specific operating characteristics before and after failure simulation in respective LIVCs include:

1. Synchronization frequency is proportional to the LIVC input voltage. The frequency increases approximately 25 percent when only three of four are operating; frequency increases 33 percent (compared to four operating) when only two of four are operating.
2. Phase separation is maintained. When four LIVCs are operational, phase separation is approximately 45 degrees. If failures occur, separation is dependent on failure but minimum of 30 degrees is maintained in all cases.
3. Synchronization is reliably established upon starting the LIVCs.
4. Failures of single LIVCs are not adversely linked to other operational LIVCs.

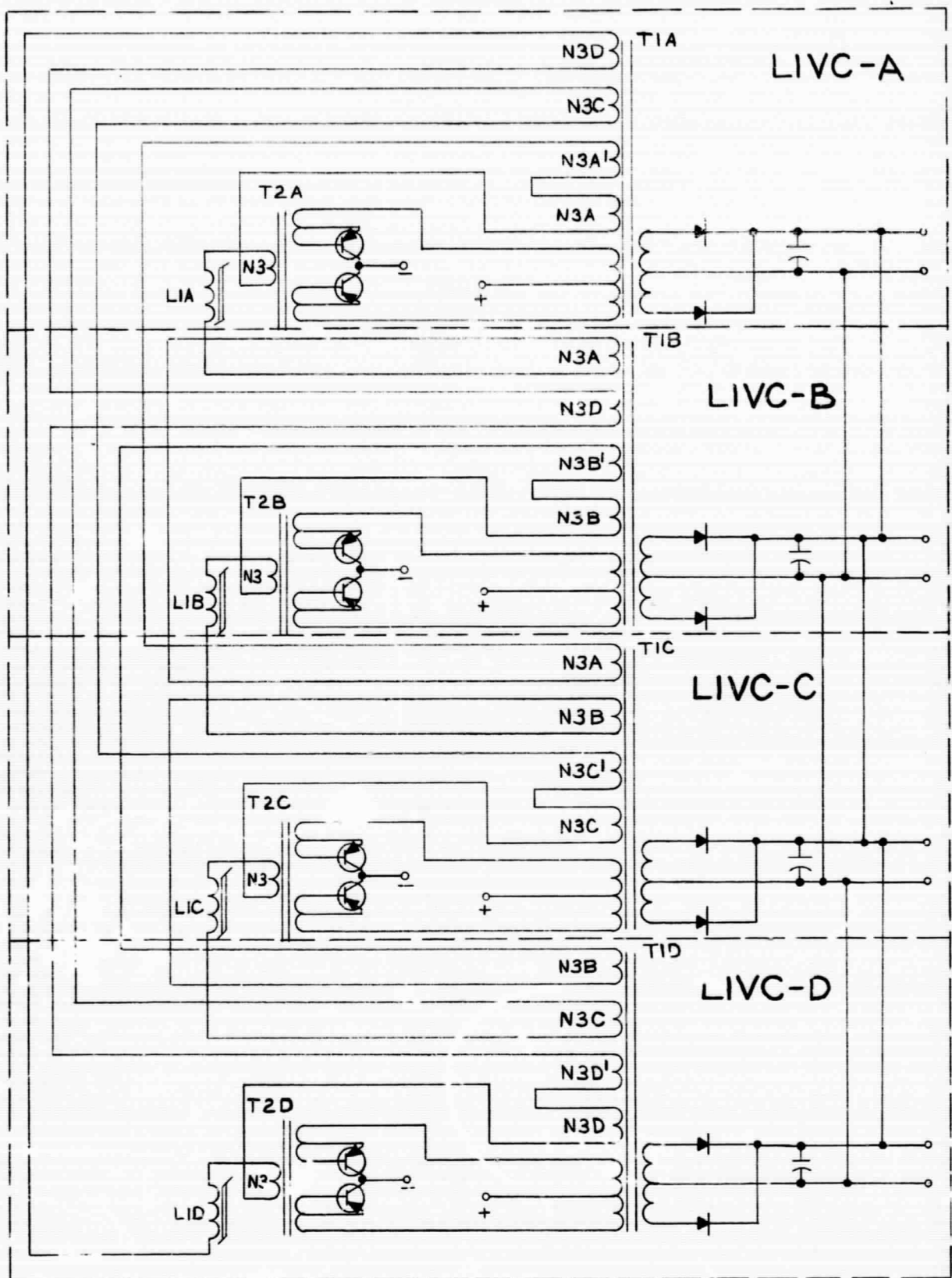


Figure 11 - SYNCHRONIZATION CIRCUIT FOR FOUR LIVCS

5. The basically desirable features of current feedback LIVCs are maintained.

The stated performance has been proven through quite extensive laboratory testing and is indeed borne out by the delivered model's performance. This extended technology provides the designer additional latitude in specifying the degree of LIVC redundancy for space power applications.

A second approach, to synchronize four LIVCs, was also considered (figure 7, first quarterly report); however, the approach presented in figure 11 is much more feasible.

B. LIVC FAILURE SENSING AND ISOLATION

One of the most significant accomplishments during this program has been the development of a low-loss, controlled transistor switch for parallel LIVCs inputs. This development enables the designer to realize true redundancy in a parallel LIVC configuration to effect higher conversion function reliability. Size and weight of the transistor switch is less than many competitive electromechanical devices for the same function. The comparable transistor switch cost would be less, efficiency higher. Automatic LIVC failure-sensing and compensation inherent in the provided switch drive circuit enables one to decrease the time between failure occurrence and connection. Decreased failure correction response time reduces the time during which substandard performance may be characteristic and the time a specific component may be overstressed by the failure's presence.

The circuit diagram for the LIVC input switch is shown in figure 6. A current transformer provides drive to the transistor switch with a nearly constant forced current gain. Neglecting slight changes in the LIVC efficiency, the ratio of input current to power transformer

output current is constant; the transistor switch drive current is a direct ratio of the power transformer output current. Transistor switch power loss, including drive circuitry in the delivered model, is typically 10 watts with 100 amperes input. Efficient switch connection is provided even with an LIVC output short circuit. Effective isolation is provided by the switch if drive is removed.

The automatic LIVC failure compensation inherent in the current transformer drive isolates failures, including an LIVC short circuit in the input capacitor, power transistors and power transformer. Isolation of output rectifier failures is also inherently provided if an isolation diode is incorporated between individual LIVCs rectified outputs and the common regulator input.

A circuit used in conjunction with the input switch to isolate LIVC output capacitors is shown in figure 12. This circuit was discussed in detail in the third quarterly report (pp. 13-15). Inclusion of this circuit is left to the designer's discretion and would depend primarily on the type of output capacitor used. The reliability analysis conducted did indicate an increase in reliability from 0.996 to 0.998 with the circuit inclusion and the failure rates assumed.

C. PWM REGULATOR POWER SECTION FAILURE SENSING AND ISOLATION

The PWM power section failure-compensation circuitry effectively isolates the most common failure mode, a short of the chopping or regulating transistor if it occurs. An open-circuit-type failure provides its own isolation. The short-circuit failure is defined when the transistor conducts but no drive is being supplied to it.

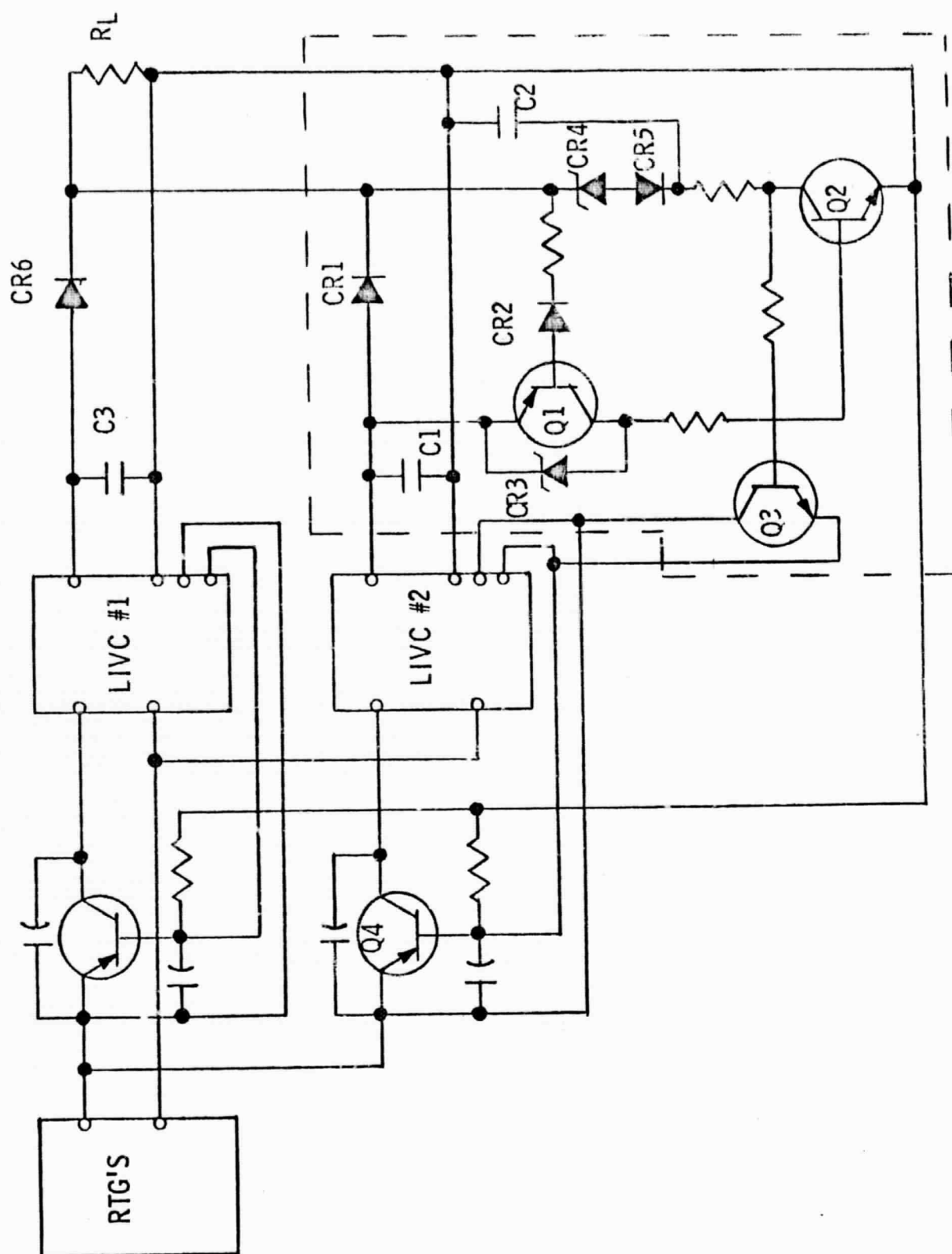


Figure 12 - SENSING AND ISOLATION OF LIVC OUTPUT CAPACITOR FAILURES

This failure is effectively sensed and isolated with the circuit of figure 5. A relay serves as the isolating switch in the delivered model; however, a transistor could instead be incorporated to provide the isolation.

The isolating switch can also be used to compensate for PWM free-wheeling diode or output capacitor failures if used with the circuit in figure 13. This circuit was not incorporated in the delivered model. The reliability analysis conducted the fourth quarter did indicate an increased power section (three redundant branches) from 0.997 to 0.999 with the circuit inclusion and for the failure rates assumed.

D. PWM DRIVE AND CONTROL WITH FAILURE SENSING AND ISOLATION

The model delivered on this program incorporates two standby redundant PWM drive and control circuits. Automatic failure compensation is provided through performance sense circuitry, logic failure identification, and transistor switches. A failure in the drive and control circuitry is defined when:

1. The output voltage is low and no drive is being supplied, or when
2. The output voltage is high and drive is being supplied.

When a failure is sensed, the circuit controlling is automatically removed and a new functional circuit is introduced. Several modifications in the drive circuitry were implemented to improve the performance over wide load and input voltage ranges during this program.

The circuit, as implemented in the model, is shown in figure 4. The circuit features bistable operation of the respective failure identification logic, shaping of the low-voltage signal, and adequate drive to the chopping transistor and the circuit select transistor switch during all modes of operation.

E. DECREASING UNBALANCE IN THE LIVC FEEDBACK TRANSFORMER

A circuit was developed during the second and third quarter to equalize the volts per turn on the current feedback transformer during succeeding half-cycles. Equalizing the volts per turn and assuming equal duration of succeeding half-cycles effects equal flux change and balance in the transformer core. The closed-loop approach, shown in figure 14, involves:

1. Sensing the volts per turn.
2. Comparing the sensed voltage to the average of several cycles.
3. Subtracting drive current from that power transistor which exhibits a higher drive-winding voltage.

The fixed amp-turn input (for a specific LIVC at current) to the current transformer and the resistive characteristics of the power transistors emitter-base junctions are inherent properties used to an advantage in achieving control. Equal volts per turn on succeeding half-cycles are not necessarily characteristic immediately on starting, but are established within a few cycles. While shown to be effective, this circuit is meant only to supplement matching of transistor emitter-base characteristics and transformer design to avoid half-cycle unbalance. The circuit does have significant advantages in that control can be exercised without excessive power dissipation.

This circuit was not incorporated in the delivered model because (1) no half-cycle unbalance was noted during testing and (2) half-cycle unbalance, should it occur, is not a severe problem when operating from the intended RTG sources.

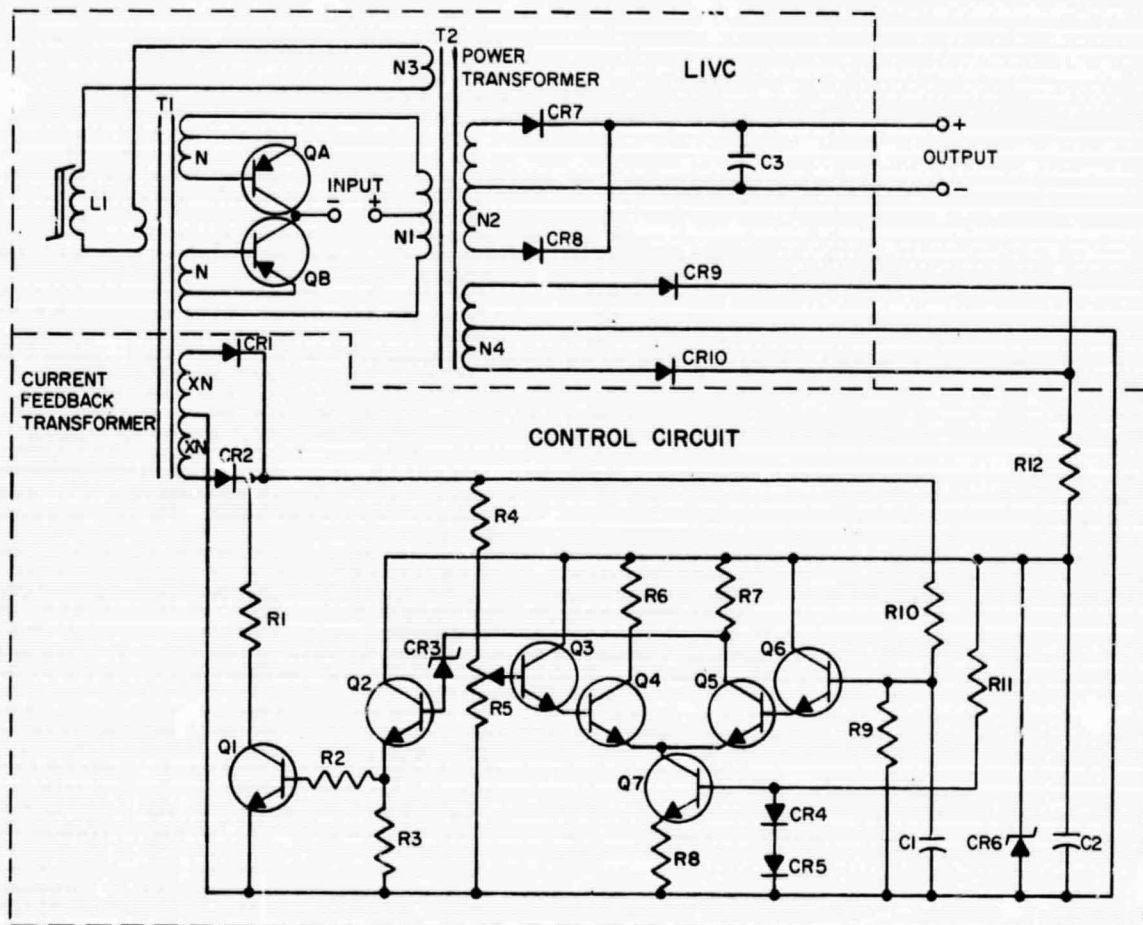


Figure 14 - CURRENT FEEDBACK CONTROL CIRCUIT
FOR EQUAL TRANSFORMER DRIVE

III. NEW TECHNOLOGY

The new technology established on this program has been reported in previous quarterly reports. During this fourth quarter, some of these circuits have been modified but modifications primarily involved actual implementation rather than basic concepts. The most significant accomplishments of the program are the following:

1. Phase-separated synchronization of four redundant LIVCs.
2. A low-loss transistor input switch and associated drive circuit to provide isolation of failures in parallel LIVCs.
3. Failure-sensing and isolation circuitry for the parallel PWM regulator power sections.
4. Failure-sensing and compensation circuitry to automatically select one of two PWM drive and control sections in standby redundancy.
5. Closed-loop control in the LIVC current feedback transformer to decrease half-cycle unbalance.

These concepts have been proven in laboratory testing and appear to be significant advances in the field of power conditioning for space applications.

IV. CONCLUSIONS AND RECOMMENDATIONS

This program (NAS-5-10148) has contributed significant improvements in power-conditioning technology for space applications. The increased reliability afforded the power system by these developments directly increases the probability of success for the total space mission. Because the successful operation of the data-gathering system, telemetry, etc., are directly dependent on the supply of electrical power, proper operation of the power system is indeed a key factor in determining mission success. The results of this program increase the probability of not only supplying electrical power, but minimizing momentary interruption of the power for the full duration of the long-time space missions planned in the future. In essence, the results from this program enable the designer to fully realize the high reliability potential established in the previous program (NAS-5-9212).

The automatic failure-correction circuitry developed reduces the time required for failure correction and reduces the time period during which substandard power supply performance may exist. The automatic features decrease the telemetry channels required as they eliminate the need for telemetry monitoring and command switching in the space power supply redundant sections.

Synchronization circuitry for four LIVCs maintains approximately 45-degree phase separation between respective oscillator switchings. Phase separation between operating units is also maintained after failures occur in individual LIVCs. The phase-separated operation reduces line transients and component stress, improves stability, and provides a capability for polyphase AC outputs.

The equality of phase separation is dependent on equal LIVC input voltages and identical switching inductors.

The design guidelines and basic operation of the synchronization circuit for four LIVCs is commensurate with those established on contract NAS-5-9212 for two and three LIVCs respectively.

An LIVC transistor input switch can provide efficient connection and/or effective isolation for LIVCs in a parallel configuration. The transistor switch drive circuit effects a constant forced current gain and inherently provides an automatic failure sensing and compensation through the switch. The reliability analysis conducted during the fourth quarter, with the switch included in a four redundant system, indicates a conversion function failure decrease from 0.0214 to 0.00157 for a three-year mission using failure rates stated in appendix A.

The LIVC failure-isolation circuitry, incorporated in the delivered model, isolates short-circuit failures of the input capacitor, power transistors, and power transformer. Introduction of an output isolation diode enables the incorporated circuit to isolate output rectifier failures. Complementary circuitry enables output capacitor failures to be isolated with the LIVC input switch and output isolation diode.

The nominal voltage and switching requirements of the LIVC transistor input switch allow the transistor to be selected for lower saturation voltage properties than would be characteristic if these requirements were more stringent.

The PWM regulator power sections connected in parallel provide redundancy through the automatic failure-isolation circuitry. The projected failure probability would decrease from 0.0054 to 0.000024 on a three-year mission, according to failure rates of appendix A and a redundancy of three.

A complementary circuit to enable the designer to isolate failures in the free-wheeling diodes and output capacitor can be effectively incorporated, if desired.

The relay isolating switch incorporated for each PWM power section, in the delivered model, could be replaced with a transistor. However, drive circuit provision would have to be incorporated for the transistor.

The PWM regulator drive and control circuit modifications incorporated on this program facilitate isolation of failures and insure adequate drive over widely varying input voltage and load ranges. The regulator drive is basically proportional to LIVC output current but is supplemented by voltage proportional drive at light load.

The PWM regulator drive and control failure compensation circuitry performs very satisfactorily in selecting one of two circuits in standby redundancy. Bistable operation of respective failure-identification logic and other signal processing significantly reduces the circuits' susceptibility to noise.

A closed-loop control on the LIVC current feedback transformer can reduce core unbalance tendencies in the same manner. The circuit approach developed is intended to complement, rather than replace, established techniques to reduce half-cycle unbalances.

A common RTG output-common LIVC input configuration yields the simplest failure-isolation circuitry for each, while realizing maximum usage of operational modules after redundant failures.

The SCR overvoltage (of RTG) circuit provides significant advantages in its simplicity and effective operation. However, this circuit should not be incorporated in single LIVC outputs of a redundant configuration, when a common LIVC input is characteristic, unless each LIVC is capable of handling the maximum total RTG output.

A shunt-type PWM regulator which provides RTG overvoltage protection and output regulation should be considered in future work. It is recommended that the shunt regulator frequency be an even multiple of the LIVCs and synchronized to avoid upsetting LiVC synchronization.

APPENDIX A

RELIABILITY DATA

TABLE A-1
 P_0 DETERMINATION FOR LIVC
 FAILURE-SENSING AND ISOLATION CIRCUIT
 (PIECE-PART DRIFT FAILURE MODES NOT CONSIDERED)

PART AND REFERENCE DESIGNATION	FAILURE RATE %/1000 HRS.	FAILURE MODES THAT EFFECTIVELY OPEN THE CIRCUIT	OCCURENCE OF THE FAILURE MODE(S) *	TOTAL FAILURE RATE %/1000 HOURS
TRANSISTORS Q_1 AND Q_2	0.0062	OPEN EMITTER OR BASE ON BOTH TRANSISTORS	10	0.0012
CAPACITOR C-2	0.002	SHORT OR OPEN	95	0.0019
DIODE CR2, CR3	0.010	SHORT OR OPEN	55	0.0110
TRANSFORMER	0.010**	SHORT OR OPEN	37	0.0037
			TOTAL	0.0178

* REFERENCE: G.E. MANUAL TRA-873-74

** ESTIMATE BASED ON CONSTRUCTION OF DEVICE, AND ELECTRICAL STRESS REQUIREMENTS.

$$P_0 = 1 - e^{-\lambda t} = 1.78 \times 10^{-7} \frac{\text{FAILURES}}{\text{HOUR}} ; t = 2.63 \times 10^4 \text{ HOURS}$$

$$\lambda t = 4.68 \times 10^{-3} \approx 0.0047; e^{-\lambda t} \approx 0.9953$$

$$P_0 = 1 - 0.9953 = 0.0047$$

TABLE A-2
 P_S DETERMINATION FOR LIVC
 FAILURE-SENSING AND ISOLATIONCIRCUIT (INPUT-OUTPUT)
 (PIECE-PART DRIFT FAILURES NOT CONSIDERED)

PART AND REFERENCE DESIGNATION	FAILURE RATE %/1000 HRS.	FAILURE MODES THAT EFFECTIVELY SHORT THE CIRCUIT	% OF TOTAL F_T THAT THE FAILURE MODE OCCURS *	FAILURE RATE OF THE SHORT CIRCUIT FAILURE MODE
TRANSISTORS Q_1 AND Q_2	4 (0.0062)	SHORT: BASE-EMITTER, BASE-COLLECTOR OR COLLECTOR-EMITTER	15	0.0037 %/1000 HOURS
TOTAL				0.0037 %/1000 HOURS

* REFERENCE: G.E. MANUAL
 TRA-873-74

$$P_S = 1 - e^{-\lambda t}$$

$$\lambda = 3.7 \times 10^{-8} \frac{\text{FAILURES}}{\text{HOUR}} ; t = 2.63 \times 10^4 \text{ HOURS}$$

$$\lambda t = 3.7 \times 10^{-8} \times 2.63 \times 10^4 = 9.73 \times 10^{-4}$$

$$P_S \approx 0.001$$

TABLE A-3
P_O DETERMINATION OF THE LIVC
(PIECE PART DRIFT FAILURE MODES NOT CONSIDERED)

PART(S) AND REFERENCE DESIGNATION(S)	FAILURE RATE %/1000 HRS.	FAILURE MODES THAT EFFECTIVELY OPEN THE LIVC	OCCURENCE OF THE FAILURE MODE* (%)	TOTAL FAILURE RATE %/1000 HOURS
DIODES, CR1, CR2	0.00075	BOTH SHORTED	40	0.0006
DIODES CR5, CR6	0.00075	BOTH SHORTED	40	0.0006
TRANSISTORS, Q ₂ AND Q ₃	10 (0.0062)	SHORT: BASE-EMITTER	2.5	0.00155
TRANSFORMER T-1	0.100	SHORT OR OPEN	24	0.0240
TRANSFORMER T-5	0.100	OPEN N ₁ OR N ₂	3.3	0.0033
TOTAL				0.030

* REFERENCE: G.E. MANUAL TRA-873-74

$$P_0 = 1 - e^{-\lambda t}$$

$$\lambda = 3.0 \times 10^{-7} ; t = 2.63 \times 10^4 \text{ HOURS}$$

$$\lambda t = 3.0 \times 10^{-7} \times 2.63 \times 10^4 = 7.89 \times 10^{-3}$$

$$e^{-\lambda t} \cong 0.9921$$

$$P_0 = 1 - 0.9925 \cong 0.0079$$

TABLE A-4
P_S DETERMINATION FOR THE LIVC
(PIECE PART DRIFT FAILURE MODES NOT CONSIDERED)

PART (S) AND REFERENCE DESIGNATION (S)	FAILURE RATE %/1000 HRS.	FAILURE MODES THAT EFFECTIVELY SHORT THE LIVC	OCCURENCE OF THE FAILURE MODE(S)* (%)	TOTAL FAILURE RATE %/1000 HOURS
POWER TRANSISTORS Q ₂ , Q ₃	10 (0.0062)	SHORT: COLLECTOR- EMITTER, COLLECTOR- BASE	12.5	0.00775
TRANSFORMER T ₁	0.100	N ₃ OPEN	2	0.002
TRANSFORMER T ₅	0.100	SHORT: N ₁ , N ₂ , N ₃ , N ₄ , N ₅ ; OPEN: N ₃	14.2	0.0142
TOTAL				0.02395

* REFERENCE: G.E. MANUAL TRA-873-74

$$P_S = 1 - e^{-\lambda t}$$

$$\lambda = 2.4 \times 10^{-7}; t = 2.63 \times 10^4$$

$$\lambda t = 6.3 \times 10^{-3}; e^{-\lambda t} = 0.9937$$

$$P_S = 1.0000 - 0.9937 = 0.0063$$

TABLE A-5
P_S DETERMINATION (PROBABILITY OF SHORT)
LVC OUTPUT CAPACITOR

PART AND REFERENCE DESIGNATION	FAILURE RATE %/1000 HRS.	FAILURE MODES THAT EFFECTIVELY SHORT THE LVC	% OF THE TOTAL F _r THAT THE FAILURE MODE OCCURS	F _r OF THE SHORT FAILURE MODE %/1000 HRS.
CAPACITOR, ALUMINUM	0.0019	SHORT	50*	0.001
			TOTAL	0.001

STRESS RATIO = $\frac{30}{75} = 40\%$ NOMINAL. ∴ F_r @ 25°C = 0.019%/1000 HOURS

÷ 10 = 0.0019% FOR "HI-REL" PARTS IN SPACE APPLICATION.

*ESTIMATED, DUE TO LACK OF DATA SOURCE. ALSO ASSUMED AN OPEN FAILURE RATE OF 0.001%/1000 HOURS.

4 CAPACITORS X 0.001 = 0.004%/1000 HOURS

$$R = e^{-\lambda t}$$

$$\lambda = 4 \times 10^{-8}, t \approx 2.63 \times 10^4; \lambda t = 0.0011$$

$$P_S = 0.0011$$

TABLE A-6

P_S DETERMINATION (P_{AS})
PWM TRANSISTOR FAILURE SENSING AND ISOLATION
(PIECE-PART DRIFT FAILURES NOT CONSIDERED)

PART AND REFERENCE DESIGNATION	FAILURE RATE %/1000 HRS.	FAILURE MODES THAT EFFECTIVELY SHORT THE CIRCUIT	% OF THE TOTAL F _T MODE OCCURS*	FAILURE RATE OF THE SHORT FAILURE MODE
TRANSISTOR Q ₂	0.001	SHORT: BASE-EMITTER, OR OPEN BASE, EMITTER OR COLLECTOR	25	0.00025 %/1000 HRS.
CAPACITOR C ₁	0.002	SHORT	20	0.0004 %/1000 HRS.
RESISTOR R ₉	0.0001	OPEN	10	0.00001 %/1000 HRS.
TRANSISTOR Q ₆	0.001	SHORT: COLLECTOR-EMITTER OR COLLECTOR-BASE	12.5	0.00012 %/1000 HRS.
TRANSISTOR Q ₇	0.001	SHORT: COLLECTOR-EMITTER OR COLLECTOR-BASE	5	0.00005 %/1000 HRS.
ZENER DIODE CR ₉	0.003	OPEN CIRCUIT	10	0.0003 %/1000 HRS.
CIRCUIT BREAKER CB ₁	0.005	OPEN COIL OR LATCHING MECHANISM FAILURE	100**	0.005 %/1000 HRS.
DIODE CR ₈	0.0004	OPEN	20	0.00008 %/1000 HRS.
CR ₁₀	0.0004	SHORT	40	0.00016 %/1000 HRS.
TOTAL				0.00637 %/1000 HRS.

* REFERENCE: G.E. MANUAL TRA-873-74

** ESTIMATED FAILURE RATE $P_S = 1 - e^{-\lambda t}$

$$\lambda = 6.37 \times 10^{-8}, t = 2.63 \times 10^4$$

$$\lambda t = 6.37 \times 10^{-8} \times 2.63 \times 10^4 = 1.67 \times 10^{-3} \approx 0.002$$

$$P_S \approx 0.002$$

TABLE A-7
P_O DETERMINATION (P_{AO})
PWM TRANSISTOR FAILURE SENSING AND ISOLATION
(PIECE-PART DRIFT FAILURES NOT CONSIDERED)

PART AND REFERENCE DESIGNATION	FAILURE RATE %/1000 HRS.	FAILURE MODES THAT EFFECTIVELY OPEN THE CIRCUIT	% OF THE TOTAL F _T THAT THE FAILURE MODE OCCURS*	F _T OF THE OPEN FAILURE MODE %/1000 HOURS
TRANSISTOR Q ₂	0.001	SHORT: COLLECTOR-EMIT- TER OR COLLECTOR-BASE	5	0.00005
RESISTORS R ₇ , R ₈	0.0002	OPEN	10	0.00002
TRANSISTOR Q ₆	0.001	SHORT: BASE-EMITTER OR OPEN BASE, EMITTER OR COLLECTOR	12.5	0.000125
TRANSISTOR Q ₇	0.001	SHORT: BASE-EMITTER OR OPEN BASE, EMITTER OR COLLECTOR	25	0.00025
TOTAL				0.000445

* REFERENCE: G.E. MANUAL TRA-873-74

$$P_0 = 1 - e^{-\lambda t}$$

$$\lambda t = 4.45 \times 10^{-9} \times 2.63 \times 10^4$$

$$\lambda t = 1.17 \times 10^{-4} \approx 0.0012$$

$$P_0 \approx 0.00012$$

TABLE A-8

P_S DETERMINATION
PWM TRANSISTOR CIRCUIT

PART AND REFERENCE DESIGNATION	FAILURE RATE %/1000 HRS.	FAILURE MODES THAT EFFECTIVELY SHORT THE CIRCUIT	% OF THE TOTAL F THAT THE FAILURE MODE OCCURS*	F OF THE SHORT FAILURE MODE %/1000 HOURS
TRANSISTOR Q_5	2 (0.006)	SHORT; COLLECTOR-EMIT- TER OR COLLECTOR BASE	12.5	0.0015
TOTAL				0.0015

$$P_S = 1 - e^{-\lambda t}$$

$$\lambda t = 1.5 \times 10^{-8} \times 2.63 \times 10^4 = 3.94 \times 10^{-4}$$

$$P_S \approx 0.0004$$

P_O DETERMINATION, PWM TRANSISTOR CIRCUIT

PART AND REFERENCE DESIGNATION	FAILURE RATE %/1000 HRS.	FAILURE MODES THAT EFFECTIVELY OPEN THE CIRCUIT	% OF THE TOTAL F THAT THE FAILURE MODE OCCURS*	F OF THE OPEN FAILURE MODE %/1000 HOURS
RESISTOR R_6	0.0001	OPEN	10	0.00001
TRANSISTOR Q_5	2 (0.006)	SHORT; BASE-EMITTER	5	0.00060
PWM OUTPUT CAPACITOR	0.0032	OPEN	50**	0.0016
PWM FREE- WHEELING DIODE	0.005	OPEN	20	0.0010
TOTAL				0.0087

* REFERENCE: G.E. MANUAL TRA-873-74

** ESTIMATE

$$P_O = 1 - e^{-\lambda t}$$

$$\lambda t = 8.7 \times 10^{-8} \times 2.63 \times 10^4 = 2.29 \times 10^{-3} \approx 0.0023$$

$$P_O \approx 0.0023$$

TABLE A-9
(PROBABILITY OF SHORT CIRCUIT) PWM
OUTPUT CAPACITOR AND FREE-WHEELING DIODES

PART AND REFERENCE DESIGNATION	FAILURE RATE (F _r) %/1000 HRS.	FAILURE MODES THAT WILL SHORT THE CIRCUIT	% OF THE TOTAL F _r THAT THE FAILURE MODE OCCURS	F _r OF THE OPEN FAILURE MODE %/1000 HOURS
PWM OUTPUT CAPACITOR	0.0032	SHORT	50	0.0016
PWM FREE - WHEELING DIODE	0.005	SHORT	35	0.0018
TOTAL				0.0033

$$P_S = 1 - e^{-\lambda t}$$

$$\lambda t = 3 (3.3 \times 10^{-8} \times 2.63 \times 10^4) = 2.6 \times 10^{-3}$$

$$P_S = 0.0026$$

TABLE A-10
RELIABILITY ESTIMATE
REGULATOR DRIVE CONTROL CIRCUITS

PART NAME	PART TYPE	N	GENERAL FAILURE RATE %/1000 HOURS	TOTAL FAILURE RATE %/1000 HOURS
RESISTOR	TIN OXIDE	17	0.0006	0.0102
RESISTOR	WIRE WOUND	2	0.0009	0.0018
DIODES	GENERAL-PURPOSE	6	0.00075	0.0045
DIODES	ZENER	2	0.003	0.006
TRANSISTOR	UNIUNCTION	1	0.010	0.010
TRANSISTOR	SMALL SIGNAL	6	0.001	0.006
TRANSISTOR	MEDIUM SIGNAL	1	0.002	0.002
TRANSISTOR	POWER, Gc., 10% STRESS	1	0.00432	0.00432
CAPACITOR	SOLID TANTALUM	6	0.002	0.012
CAPACITOR	CERAMIC	1	0.00075	0.00075
TOTAL = $\lambda_0 = \lambda_s$				0.057

$$\lambda_0 t = \lambda_s t = 0.01499$$

$$R = e^{-\lambda t} \approx 0.985$$

TABLE A-11

DETERMINATION OF R_{SW}

REGULATOR DRIVE CONTROL SWITCHING TRANSISTORS

Failure Rate = 0.0043%/1000 Hours X 2 transistor = 0.0086

(percentage of failures due to shorts)

$$= 0.0086 \times 12.5\% = 0.0011$$

$$R_{SW} = e^{-\lambda} = .9989$$

TABLE A-12

P₀ DETERMINATION

(Probability of failure-sensing circuit failing in a mode that would isolate the inverter from the system)

LIVC output capacitor short-circuit, failure-sensing circuit

PART AND REFERENCE DESIGNATION	FAILURE RATE %/1000 HRS.	FAILURE MODES THAT WILL RESULT IN AN OPEN INVERTER	% OF THE TOTAL F _T MODE OCCURS*	F _T OF THE OPEN FAILURE MODE (%/1000 HOURS)
CR3, SILICON ZENER DIODE	0.003	OPEN	20	0.0006
Q ₁ , TRANSISTOR GERMANIUM	0.006	SHORT: BASE-EMITTER OR OPEN BASE, EMIT- TER OR COLLECTOR	17.5	0.0011
Q ₂ , TRANSISTOR, PLANAR, SILICON	0.006	SHORT: BASE-EMITTER OR OPEN BASE, EMIT- TER OR COLLECTOR	10.5	0.0006
Q ₃ , TRANSISTOR, PLANAR, SILICON	0.006	SHORT: COLLECTOR- EMITTER OR COLLEC- TOR-BASE	12.5	0.0008
CR2, GERMANIUM DIODE	0.0008	OPEN	10	0.0001
CR4, ZENER DIODE	0.003	SHORT	30	0.0009
R ₁ , RESISTOR FILM	0.0009	OPEN	85	0.0008
R ₃ , RESISTOR FILM	0.0009	OPEN	85	0.0008
TOTAL				0.0057

* REFERENCE: G.E. MANUAL TRA-873-74

$$P_0 = 1 - e^{-\lambda t}$$

$$\lambda t = 5.7 \times 10^{-8} \times 2.63 \times 10^4 = 1.5 \times 10^{-3}$$

$$P_0 = 0.0015$$

P_S DETERMINATION (PROBABILITY OF FAILURE-SENSING FAILURE)

LIVC OUTPUT CAPACITOR SHORT-CIRCUIT,

FAILURE-SENSING CIRCUIT

PART AND REFERENCE DESIGNATION	FAILURE RATE (F_f) %/1000 HRS.	FAILURE MODES THAT DISABLE FAILURE- SENSING CIRCUIT	% OF THE TOTAL F_f THAT THE FAILURE MODE OCCURS*	F_f OF THE DISABLE FAILURE MODE (%/1000 HOURS)
CR3, ZENER DIODE	≈ 0.003	SHORT	30	0.001
Q ₁ , TRANSISTOR	≈ 0.006	SHORT: COLLECTOR- EMITTER OR COL- LECTOR-BASE	12.5	0.0008
Q ₂ , TRANSISTOR	≈ 0.006	SHORT: COLLECTOR- EMITTER OR COLLEC- TOR-BASE	12.5	0.0008
Q ₃ , TRANSISTOR	≈ 0.006	SHORT: BASE-EMITTER OR OPEN COLLECTOR, EMITTER OR BASE	25	0.0015
CR2, GERMANIUM DIODE	≈ 0.0008	SHORT	30	0.0002
CR4, ZENER DIODE	≈ 0.003	OPEN	20	0.0006
CR5, SILICON DIODE	≈ 0.0008	OPEN	20	0.0002
TOTAL				0.0051

THE PROBABILITY OF A FAILURE OCCURRING THAT WOULD
NOT BE SENSED BY THE FAILURE-SENSING AND ISOLATION
CIRCUIT WOULD THEREFORE BE:

$$P_S = 1 - e^{-\lambda t}$$

$$\lambda t = 5.1 \times 10^{-8} \times 2.63 \times 10^4 = 1.34 \times 10^{-3}$$

$$P_S = 0.0013$$

$P_{FAILURE} = P_f$ (CAPACITOR SHORT) $\times P_S$ (PROBABILITY OF FAILURE-SENSING CIRCUIT FAILURE)

$$= 0.0004 \times 0.0013 = 0.00000052$$

* REFERENCE: G.E. MANUAL TRA-873-74

APPENDIX B

EVALUATION REPORT

Date: September 15, 1967

Report No. OEXM 17185

UNIT TESTED:

One redundant low input voltage converter-regulator with automatic compensation, manufactured by Honeywell Ordnance Engr. Tech. Lab.

OBJECT OF TEST:

To determine the operating characteristics of the LIVCR while varying input and output parameters. Measure V_{in} , I_{in} , V_{out} , I_{out} , $V_{out-ripple}$, oscillator frequency, and phase separation for $I_{out} = 2, 4, 6, 8, 10, 12$ amp and $V_{in} = 3.0, 3.5, 4.0, 4.5$ V. Also, measure phase separation and calculate efficiency.

CONCLUSION:

The LIVR regulated the output voltage within the limits of $\pm 1.8\%$ and -0.0% of the prescribed $28V$ for all parameter changes and maintained an efficiency above 60.5% throughout.

The Functional Failure Isolation Circuitry operated satisfactorily.

PROCEDURE:

A 300 amp power supply in series with a 10 k potentiometer was connected by four - 12" lengths of nickel-chromium wire, each to one of the LIVCR inputs. (Fig. 1) This particular arrangement was used to simulate the low impedance source (~ 100 milliohms) for which the unit was designed.

A parallel combination of a 22Ω and/or a 14Ω slide wire resistor provided the load.

D'Arsonval type meters were used to monitor the input and output voltage and current. (1.0% accuracy) The output ripple voltage was observed by placing a C.R.O. across the output terminals. Oscillator frequency and phase separation was monitored by placing the scope in the LIVCR converter circuit.

PROCEDURE (Cont.)

A short in any of the converter circuits would constitute a failure of that particular section, therefore, the failure isolation i.e. redundancy, of the LIVCR was checked by placing shorts in each of the four converter circuits while observing the output.

RESULTS:

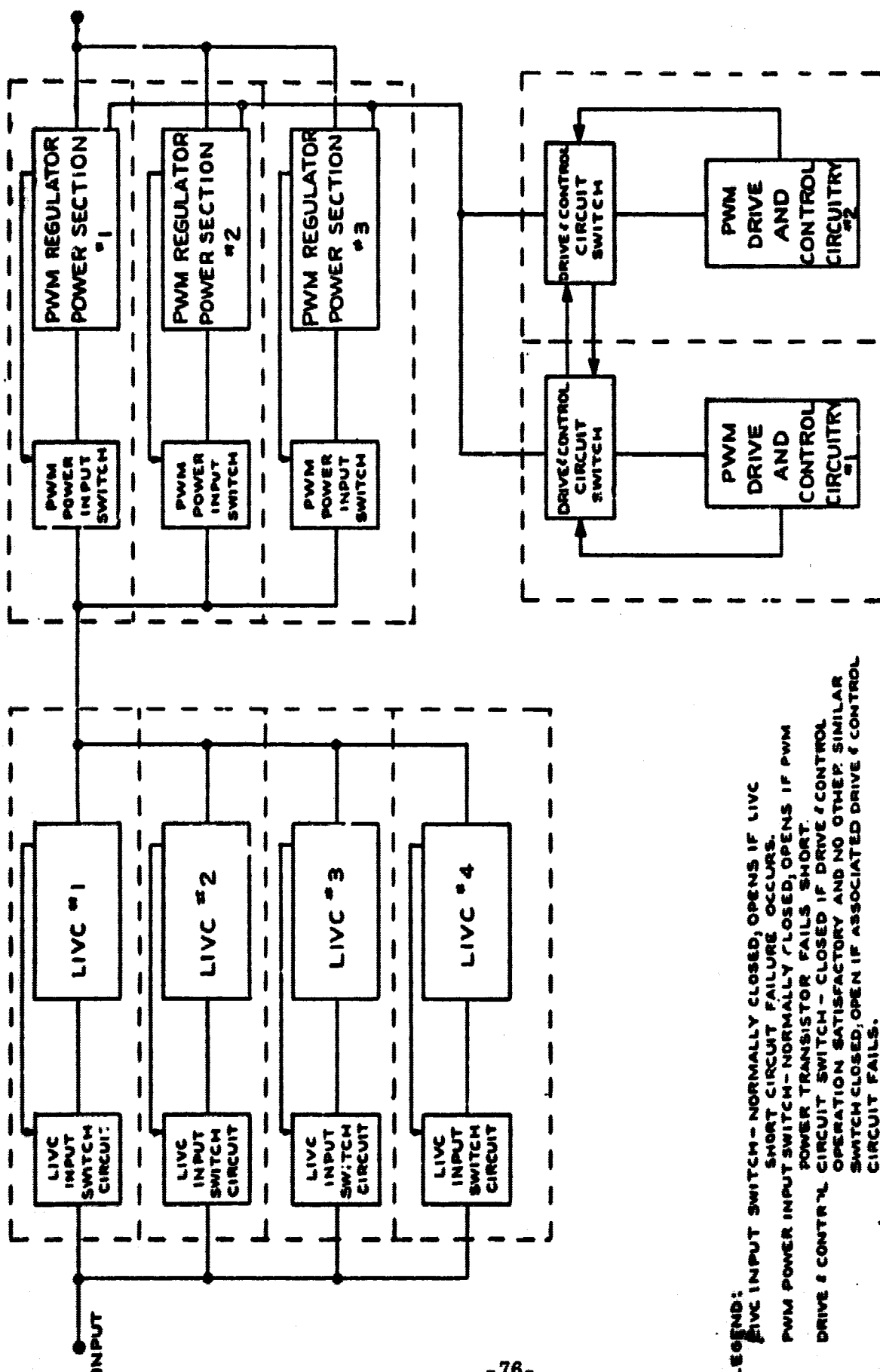
TABLE #1

LIVCR

<u>I_{out}(a)</u>	<u>V_{out}(v)</u>	<u>I_{in}(a)</u>	<u>V_{in}(v)</u>	<u>V_{ripple}(mv)</u>	<u>Eff.(%)</u>	<u>fosc.(KHz)</u>	<u>**Phase Sep.</u>
2.0	28.3	27.0	3.0	100MV	69.9	2.64	OK
2.0	28.3	22.1	3.5	105	73.4	2.86	OK
2.0	28.4	21.5	4.0	110	66.5	3.12	OK
2.0	28.5	21.0	4.5	110	60.4	3.44	OK
4.0	28.2	45.0	3.0	110	83.5	2.5	OK
4.0	28.1	44.0	3.5	110	73.2	2.86	OK
4.0	28.2	40.0	4.0	140	70.6	3.14	OK
4.1	28.5	38.0	4.5	150	67.0	3.52	OK
6.0	28.1	72.5	3.0	110	77.9	2.5	OK
6.0	28.4	63.0	3.5	130	77.4	2.77	OK
6.0	28.5	56.5	4.0	150	75.9	3.12	OK
6.0	28.5	52.0	4.5	170	73.0	3.44	OK
8.0	28.0	97.0	3.0	90	77.0	2.5	OK
8.05	28.2	84.0	3.5	110	77.5	2.86	OK
8.1	29.5	75.0	4.0	120	77.0	3.13	OK
8.1	28.5	68.5	4.5	180	74.5	3.44	OK
10.0	28.0	123.0	3.0	80	75.9	2.5	OK
10.05	28.4	105.0	3.5	120	77.5	2.94	OK
10.07	28.4	93.0	4.0	170	77.0	3.12	OK
10.08	28.5	84.0	4.5	180	75.9	3.58	OK
11.0	28.0	134.0	3.0	90	76.5	2.62	OK
11.05	28.1	116.0	3.5	130	76.5	2.86	OK
11.07	28.4	102.0	4.0	180	77.0	3.23	OK
11.19	28.5	92.5	4.5	300	74.5	3.56	OK
11.5			3.0	No Regulation due to power			
12.0			3.0	limitation of source			
12.0	28.1	126	3.5	140	76.5	2.24	OK
12.2	28.3	116	4.0	210	73.5	2.48	OK

* See Figure #2

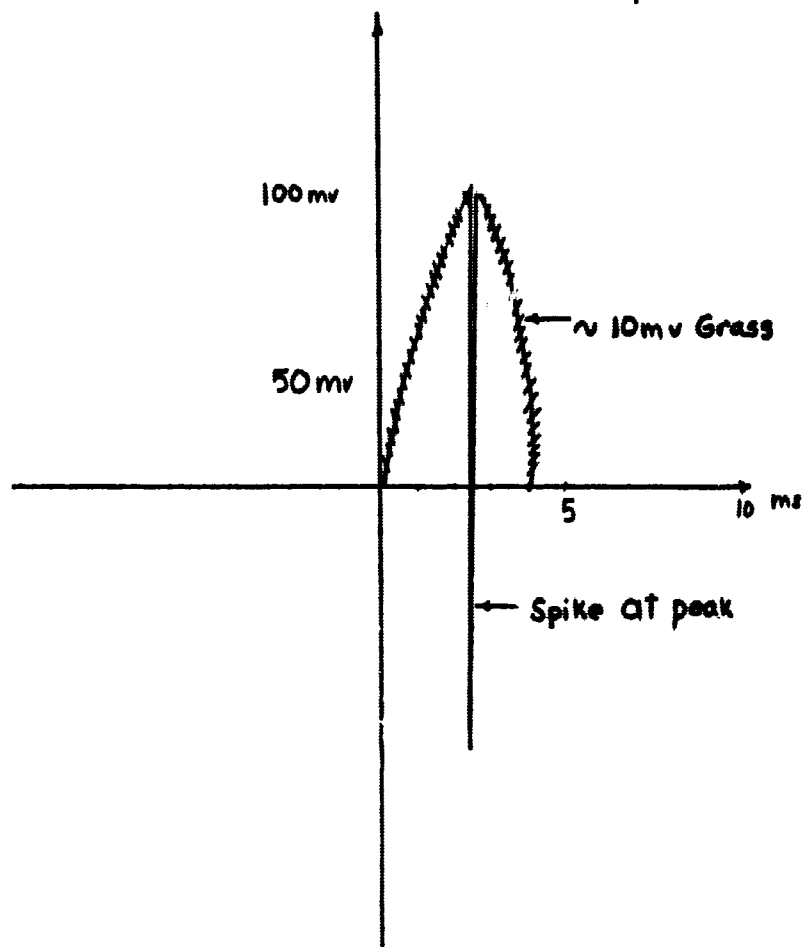
** Phase separation checked at I_{out} = 2 amp and V_{in} = 3.0V which yielded a separation of 43.2°, 39.6°, 52.4° and 45°. Through the remainder of the test, phase separation was noted and marked "OK" on data sheet.



LEGEND:

- 1 LVC INPUT SWITCH - NORMALLY CLOSED, OPENS IF LVC SHORT CIRCUIT FAILURE OCCURS.
- 2 PWM POWER INPUT SWITCH - NORMALLY CLOSED, OPENS IF PWM POWER TRANSISTOR FAILS SHORT.
- 3 DRIVE & CONTROL CIRCUIT SWITCH - CLOSED IF DRIVE & CONTROL OPERATION SATISFACTORY AND NO OTHER SIMILAR SWITCH CLOSED, OPEN IF ASSOCIATED DRIVE & CONTROL CIRCUIT FAILS.
- 4 DASHED LINES INDICATE MODULES.
- 5 ALL SWITCHES INCLUDE FAILURE SENSE AND DISCRIMINATION CIRCUITRY.

Figure #1



Example Sketch of D.C. Ripple Voltage

I_{out} @ 3.5% 2 amp.	Spike -150 mv.
4	-200
6	-200
8	-170
10	-120
12	-190

Figure 2