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SELF-SYNCHRONIZING BI-ORTHOGONAL CODED PCM TELEMETRY SYSTEM

by Warner Miller, Ronald Muller, Thomas Taylor, and John Yagelowich

Goddard Space Flight Center
Greenbelt, Md.

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ABSTRACT

This report describes the complete design, theory, and experimental statistics of a self-synchronizing, biorthogonal coded PCM telemetry system for space communications. By selecting a proper code set, word synchronization is acquired without using a parallel channel and is maintained at a signal-to-noise ratio below 4 db. With the code's property of comma freedom, word synchronization can be achieved with a circuit requiring only a few logic modules. With the use of this circuit, signal detection can be performed in real time without the use of a computer. The measured probability of word error corresponds to a signal-to-noise ratio that is within 1 db of theoretical predictions; this is 3 db better than is obtained with the standard PCM systems now used on spacecraft.

CONTENTS

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INTRODUCTION

Goddard Space Flight Center has proposed to launch a series of unmanned spacecraft for exploration of the major planets of the solar system and the galactic space beyond the solar magnetosphere. In September 1965, the Information Processing Division of Goddard Space Flight Center proposed a Galactic Probe Communications and Data Handling Subsystem (Reference 1) employing a self-synchronizing bi-orthogonal binary code. This code set was proposed instead of the often used uncoded pulse-code-modulated (PCM) system because it improves the signal-to-noise ratio (SNR), when the transmission channel is perturbed by additive white gaussian noise and the codes are detected by being correlated with their stored replicas. This improvement will enable the spacecraft to communicate 41 percent further with a given probability of bit error and and with the same transmitter power. In December 1965, a study was initiated to determine the performance of the proposed communication subsystem. A prototype of the coder and decoder was then built to verify the predictions. This report describes the complete design of the self-synchronizing, bi-orthogonal communication subsystem.

A similar bi-orthogonal coded communication system (called Digilock) was employed on one of the Pioneer spacecraft. This report describes those areas where the systems differ and presents design results where similarity exists. The proposed communication system has the following advantages over the system used on the Pioneer spacecraft:

1. The transmitted code set has a superior self-synchronizing property,
2. The detector uses a phase-lock loop,
3. Word synchronization is achieved without a computer,
4. Detection can be performed in real time,
5. The system is simpler and less expensive to implement.

GENERAL SYSTEM DESCRIPTION

The coded system for deep-space communication consists of a spaceborne source, a gaussian additive noise channel, and a ground receiver unit. The spaceborne unit receives a random binary

signal from the spacecraft data handling subsystem and transforms it into bi-orthogonal code words. This code set is again modified by a code with self-synchronization properties. The resultant binary code set has both bi-orthogonal and self-synchronization properties and needs only a single communication channel. No additional channel bandwidth is required for the word synchronization information.

Basically, the ground receiver unit consists of a digit conditioner, a storage unit, a set of cross-correlators, a maximum likelihood detector, and a word synchronizer. A block diagram of the system is shown in Figure 1. The digit conditioner input is the coded source digits, which have been perturbed by channel noise. The output is a stream of periodic pulses which are synchronous with the incoming source digits (hereafter referred to as digit clock) and an analog signal generated by integrating coded source digits and channel noise for a digit clock period.

Correlating the received signal with stored replicas of the code set is accomplished by first storing the analog level from the digit conditioner for one word period. This stored information is then correlated with the stored code replicas; one correlator is used for each possible source code. For best detection of these codes, the time at which one received code ends and the succeeding code begins must be known accurately. Hereafter, this time is referred to as code synchronization time or code synchronization. A bi-orthogonal code set has the property that if any code word is correlated with all words belonging to the set, then the code word will correlate with itself and with its complement code to E volts and minus E volts respectively and all other correlation values will be

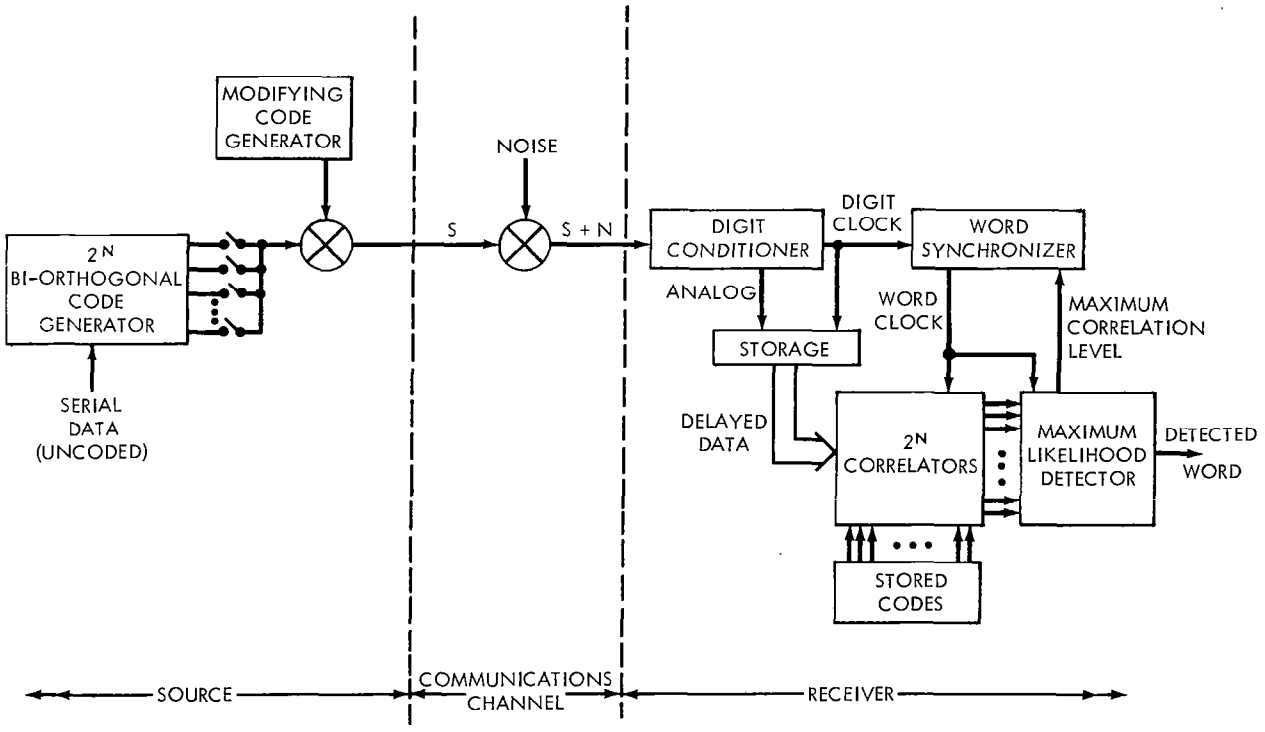


Figure 1—Source and receiver block diagram.

zero. When gaussian noise perturbs a transmitted code and this noisy signal is cross-correlated with all members of the code set, then each correlator's output will be normally distributed about the noise-free correlation values once synchronization is obtained. The maximum likelihood detector selects the correlator with the maximum correlation level, thereby providing the optimum decision (Reference 2). This decision is made for each word-period at word synchronization time. The detected digital information is now ready for the data processing equipment.

Word synchronization is obtained by utilizing the self-synchronization property of the source code-set and the derived digit clock. The digit clock is used to generate word pulses. Coherence between these derived word pulses and the code synchronization time is obtained by using the self-synchronization property of the code set. In the out-of-phase position, the maximum correlation level at the correlator outputs, in the absence of noise, can vary from a maximum of E volts to a minimum of minus E volts. It has been found in this class of codes that the code set with the lowest average correlation in the out-of-phase positions will have the best synchronization property. This stems from the fact that coherence is achieved by synchronizing on the maximum correlation value per word period, which should occur at word synchronization time. One method of judging the self-synchronization property of a code set is to note the maximum correlation level in the out-of-phase positions and the number of digit disagreements that had to occur to give that level. This number of disagreements is called the *index of comma freedom* for the code set. The set with the highest index of comma freedom has the best self-synchronization property.

A word error detector has been incorporated to provide a quantitative measure of the overall system performance. Word errors are detected by comparing a known source signal before coding (generated with a simulator) with the detected signal at the output of the maximum likelihood detector.

DESIGN THEORY

The coder receives a binary signal from the spacecraft data handling subsystem and transforms it into bi-orthogonal code words. Each generated code word contains the same number of digits. The usual code set generated is referred to as the first-order Reed-Muller codes (Reference 3). One method of constructing the Reed-Muller code words is by means of the Kronecker product construction of Hadamard orthogonal matrices of order 2:

$$\begin{bmatrix} 0 & 0 \\ 0 & 1 \end{bmatrix}.$$

This set of two orthogonal code words enables the communication of one bit of information. To increase the number of information bits that can be communicated through the channel, more code words are required. An orthogonal matrix of higher order 2^n is obtained by forming the n-fold Kronecker product of the Hadamard orthogonal matrix of order 2. This matrix of order 2^n enables

CODE NUMBER	CODE															
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
2	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
4	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
6	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0
8	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1
10	0	1	0	1	1	0	1	0	0	1	0	1	1	0	1	0
12	0	0	1	1	1	1	0	0	0	0	1	1	1	1	0	0
14	0	1	1	0	1	0	0	1	0	1	1	0	1	0	0	1
16	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
18	0	1	0	1	0	1	0	1	1	0	1	0	1	0	1	0
20	0	0	1	1	0	0	1	1	1	1	0	0	1	1	0	0
22	0	1	1	0	0	1	1	0	1	0	0	1	1	0	0	1
24	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0
26	0	1	0	1	1	0	1	0	1	0	1	0	0	1	0	1
28	0	0	1	1	1	1	0	0	1	1	0	0	0	0	1	1
30	0	1	1	0	1	0	0	1	1	0	0	1	0	1	1	0

NOTE: ONLY ONE-HALF OF THE BI-ORTHOGONAL CODE SET IS RECORDED; THE OTHER CODES ARE FORMED BY COMPLEMENTING EACH OF THE ABOVE CODES.

Figure 2—Reed-Muller code set.

the communication of n bits of information. A 16-order matrix defines the Reed-Muller code set that was used (Figure 2).

The property of orthogonality is such that when phase-coherence exists between the transmitted code words x_i and the locally generated codes x_j, the correlation between them will be

$$c_{ij} = \frac{1}{w} \sum_{i=1}^{w} \sum_{j=1}^{w} x_i x_j = 0 \quad \text{for} \quad i \neq j ,$$

and

$$= 1 \quad \text{for} \quad i = j ,$$

where w is the number of digits per code word. Furthermore, w is also the order of the Hadamard matrix used to define the code set.

A bi-orthogonal code set can be generated from the orthogonal code set by including the complement of the orthogonal set. The foregoing second-order Hadamard orthogonal matrix can be expanded into the following bi-orthogonal set:

$$\begin{bmatrix} 0 & 0 \\ 0 & 1 \\ \hline 1 & 1 \\ 1 & 0 \end{bmatrix} .$$

A bi-orthogonal code set enables the communication of one bit of information more than the orthogonal set without increasing the quantity of digits per code word. The required channel bandwidth decreases by $(n - 1)/n$ if the information is bi-orthogonally coded. The correlation property of the bi-orthogonal code set is the same as that of the orthogonal code set except when the complement code is correlated; the correlation with the complement code is -1.

For a bi-orthogonal code set, the number of digits per word needed to convey n information bits can be determined from the expression

$$w = 2^{n-1} .$$

When comparing bi-orthogonal coding to standard PCM, the channel bandwidth increases by $2^{n-1}/n$. However, for deep-space communications, the information rates are normally low, and the required channel bandwidth is usually available.

Word Synchronization

The previous analysis assumes word synchronization, which in most analyses is taken for granted. Sometimes it is transmitted on a parallel channel and consequently subtracts from the available signal power. The following paragraphs describe an analysis of word synchronization as obtained by selecting a proper code set.

Word synchronization information is added to the code set by performing a modulo-two addition of a modifying code and the Reed-Muller bi-orthogonal code set. The resultant code set also has the bi-orthogonal property. (This follows from matrix theory.) Other code sets can be generated by

1. Interchanging rows,
2. Interchanging columns, and
3. Changing the sign of every element in a column.

None of these operations disturbs the bi-orthogonal property.

A search was made for a modifying code that generated a code set with maximum comma-freedom index. For a sixteenth-order bi-orthogonal code set, the maximum index of comma freedom attainable is two. This was determined by a computer programmed to search all bi-orthogonal code sets of order 16 for the maximum index of comma freedom. The procedure used was to first modify the sixteenth-order Reed-Muller code set by changing the sign of every element in a column or columns with a modifying code that contained 16 digits. In order that all bi-orthogonal code sets would be tested, the computer register that generated the modifying code was programmed to start from zero and step in increments of one up to 2^{16}. For every generated code set, each code word was correlated with the other code words of the set in each of the out-of-phase positions. Every combination of code words was considered. If the highest correlation level for the code set in the out-of-phase position differed from the maximum correlation level of 16 by two or more, the modifying code and the comma-freedom index were printed. There were 7296 codes having an index of comma freedom of two, but none were higher than this. A modifying code developed by Stiffler (Reference 4) is included in this set of codes. Stiffler's comma-freedom-of-two modifying code is:

0111 0101 0110 0100

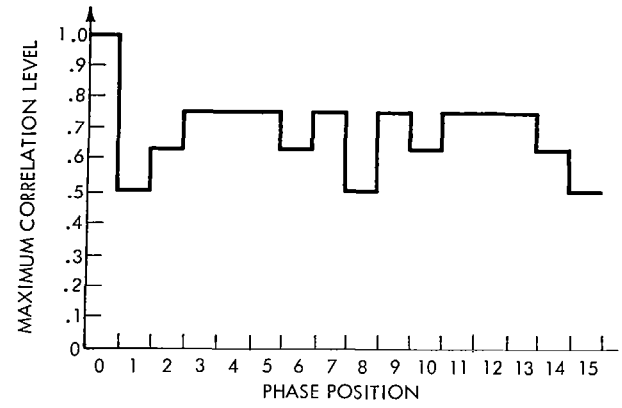
A code set generated with this modifying code is shown in Figure 3. The modifying code used in the Digilock system has a comma-freedom of zero.

Another program was written to determine the maximum correlation level at each phase position for all code word combinations of both the Stiffler and the Digilock code sets. Figure 4 shows the results. Note that the Digilock code set has a maximum correlation of 1.0 in out-of-phase position 8. This property would make the code set undesirable for acquiring word synchronization, because an ambiguous-phase state exists. However, no ambiguity exists in the code set generated using Stiffler's modifying code. Maximum correlation occurs only at the correct word phase time.

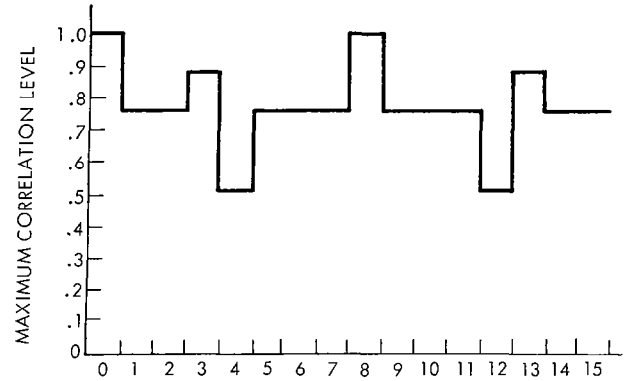
CODE NUMBER	CODE 1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
0	1	0	0	0	1	0	1	0	1	0	0	1	1	0	1	1
2	1	1	0	1	1	1	1	1	1	1	0	0	1	1	1	0
4	1	0	1	1	1	0	0	1	1	0	1	0	1	0	0	0
6	1	1	1	0	1	1	0	0	1	1	1	1	1	1	0	1
8	1	0	0	0	0	1	0	1	1	0	0	1	0	1	0	0
10	1	1	0	1	0	0	0	0	1	1	0	0	0	0	0	1
12	1	0	1	1	0	1	1	0	1	0	1	0	0	1	1	1
14	1	1	1	0	0	0	1	1	1	1	1	1	0	0	1	0
16	1	0	0	0	1	0	1	0	0	1	1	0	0	1	0	0
18	1	1	0	1	1	1	1	1	0	0	1	1	0	0	0	1
20	1	0	1	1	1	0	0	1	0	1	0	1	0	1	1	1
22	1	1	1	0	1	1	0	0	0	0	0	0	0	0	1	0
24	1	0	0	0	0	1	0	1	0	1	1	0	1	0	1	1
26	1	1	0	1	0	0	0	0	0	0	1	1	1	1	1	0
28	1	0	1	1	0	1	1	0	0	1	0	1	1	0	0	0
30	1	1	1	0	0	0	1	1	0	0	0	0	1	1	0	1

NOTE: ONLY ONE-HALF OF THE BI-ORTHOGONAL CODE SET IS RECORDED; THE OTHER CODES ARE FORMED BY COMPLEMENTING EACH OF THE ABOVE CODES.

Figure 3—Stiffler code set.



(a) CODE SET USING STIFFLER MODIFYING CODE



(b) DIGILOCK CODE SET

Figure 4—Maximum correlation level at each phase position for stiffler and digilock code sets.

The foregoing analysis assumed a noiseless communication channel. The following statistics show that correct phase can also be detected when gaussian noise is added to the communication channel. In developing the statistics, a signal-to-noise ratio of a 4 db at the output of the communications channel is used. This figure is the result of a worst-case calculation in a deep-space probe study using a bi-orthogonally coded system (Reference 1, pp. 3-3 to 3-5). Signal-to-noise ratio is defined as ST/N_0, where S is the signal power; T the information bit period; and N_0 the noise spectral density.

The procedure used to determine word synchronization statistics of a code set transmitted through a gaussian noise channel consists of three steps:

1. A computer was programmed to generate a bi-orthogonal code set by using the Stiffler modifying code.
2. The computer was programmed to generate all 32^3 combinations of code word pairs.

For each code combination and phase position, the probability that a given number of agreements of 16 will occur was determined. The probability of having k equal 16 agreements occurring at a given phase position δ is referred to as $p_k(v_1)$. Results of the computer computations are

recorded in Table 1. The correlation depends on the number of digit agreements per word (k) and the channel noise. With no channel noise, this level is referred to as the noise-free correlation level (L). This level L can be determined by taking the difference between the maximum and the actual number of digit agreements per word (16 - k), and subtracting from this the mean agreement level (8). This quantity is then normalized by dividing the foregoing with the mean agreement level, so that the maximum correlation is one. In order that the derived equation will be consistent with the implemented system, the foregoing quantity is multiplied by E which is the maximum noise-free correlation voltage. The resultant equation is

$$L = \left(1 - \frac{16 - k}{8}\right) E \ .$$

3. After determining the noise-free statistics, the remaining problem is to include the effect of noise with the correlation voltage. With noise added, the probability that the correlation voltage will exceed a given threshold level T_h is defined as $p_k\ (v_2)$. Thus,

$$p_k\ (v_2) = 1 - \frac{1}{\sigma\sqrt{2\pi}} \int_{-\infty}^{T_h} e^{-(v-L)^2 / 2\sigma^2}\, dv \ .$$

Table 1

Probability that a given number of correlation will occur (Stiffler).

Phase Position	Correlation Level								
	16/16	15/16	14/16	13/16	12/16	11/16	10/16	9/16	8/16
1	—	—	—	—	1.56×10^{-2}	9.34×10^{-2}	1.88×10^{-1}	1.56×10^{-1}	4.7×10^{-2}
2	—	—	—	7.81×10^{-3}	3.13×10^{-2}	7.00×10^{-2}	1.25×10^{-1}	1.72×10^{-1}	9.4×10^{-2}
3	—	—	9.76×10^{-4}	5.85×10^{-3}	2.54×10^{-2}	7.58×10^{-2}	1.40×10^{-1}	1.68×10^{-1}	8.40×10^{-2}
4	—	—	3.91×10^{-3}	—	5.47×10^{-2}	—	2.46×10^{-1}	—	1.95×10^{-1}
5	—	—	4.88×10^{-4}	7.81×10^{-3}	2.83×10^{-2}	7.04×10^{-2}	1.32×10^{-1}	1.72×10^{-1}	8.9×10^{-2}
6	—	—	—	7.81×10^{-3}	3.13×10^{-2}	7.00×10^{-2}	1.25×10^{-1}	1.72×10^{-1}	9.4×10^{-2}
7	—	—	9.76×10^{-4}	7.81×10^{-3}	2.92×10^{-2}	7.00×10^{-2}	1.24×10^{-1}	1.72×10^{-1}	9.6×10^{-2}
8	—	—	—	—	6.25×10^{-2}	—	2.49×10^{-1}	—	1.88×10^{-1}
9	—	—	9.76×10^{-4}	7.81×10^{-3}	2.92×10^{-2}	7.00×10^{-2}	1.24×10^{-1}	1.72×10^{-1}	9.6×10^{-2}
10	—	—	—	7.81×10^{-3}	3.13×10^{-2}	7.00×10^{-2}	1.25×10^{-1}	1.72×10^{-1}	9.4×10^{-2}
11	—	—	4.88×10^{-4}	7.81×10^{-3}	2.83×10^{-2}	7.04×10^{-2}	1.32×10^{-1}	1.72×10^{-1}	8.9×10^{-2}
12	—	—	3.91×10^{-3}	—	5.47×10^{-2}	—	2.46×10^{-1}	—	1.95×10^{-1}
13	—	—	9.76×10^{-4}	5.85×10^{-3}	2.54×10^{-2}	7.58×10^{-2}	1.40×10^{-1}	1.68×10^{-1}	8.40×10^{-2}
14	—	—	—	7.81×10^{-3}	3.13×10^{-2}	7.00×10^{-2}	1.25×10^{-1}	1.72×10^{-1}	9.4×10^{-2}
15	—	—	—	—	1.56×10^{-2}	9.34×10^{-2}	1.88×10^{-1}	1.56×10^{-1}	4.7×10^{-2}

The standard deviation of the noise at the correlator output is calculated, assuming a worst-case signal-to-noise ratio of 4 db:

$$ST\ N_0 \qquad 4\ \text{db} \ .$$

$$N_0 = ST\ 2.51 \ .$$

There are five information bits per word, allowing 32 code words. Thus the correlation period is $T_w = 5T$. The noise variance as a function of N_0 and T_w is given by $\sigma^2 = N_0/T_w$. By substitution, the standard noise deviation is $\sigma = 0.283\ E$, where E is the rms signal level.

A transformation of variable $t = (v - L)/\sigma$ is used to transform this curve into the standard normal curve which follows

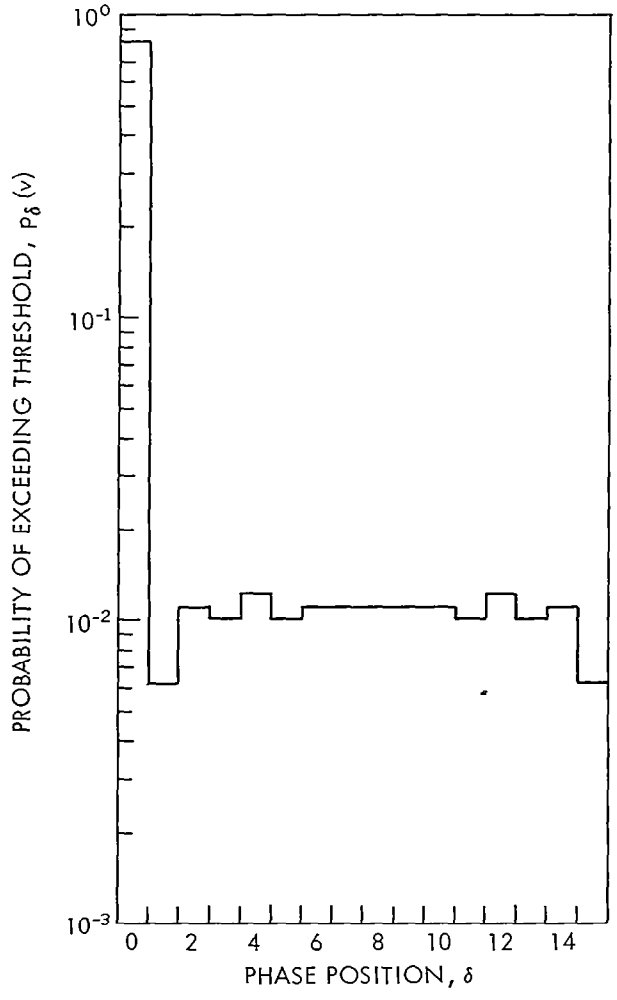


Figure 5—Probability of exceeding threshold at each phase position for Stiffler code set (SNR = 4 db).

$$P_k(v_2) = \frac{1}{2}\left(1 - \frac{1}{\sqrt{2\pi}}\int_{-x}^{x} e^{-t^2/2}\,dt\right) \ .$$

where $x = (T_h - L)/\sigma$. Solutions of the integral for various values of x are taken from Reference 5.

From the foregoing statistics, $P_k(v)$ is calculated from

$$P_k(v) = P_k(v_1)\,P_k(v_2) \ .$$

which is the probability that a given threshold is exceeded for a given noise-free correlation level. The probability that a given threshold is exceeded in a given phase-position δ is then determined by summing $P_k(v)$ for all possible noise-free correlation levels. Thus,

$$P_\delta(v) = \sum_{k=0}^{16} P_k(v) \ .$$

Figure 5 shows theoretical statistics of $P_\delta(v)$ at each phase position, for a code set generated using the Stiffler modifying code. The calculation assumed a threshold level of 3/4 E, random data words, and an SNR of 4 db.

As a means of comparing the synchronization ability of code sets, a confidence factor (C.F.) equation was developed by taking a ratio of the maximum probability that a correlation will exceed

threshold in the out-of-phase positions $\left[\text{max. } p_\delta(v)\right]$ to the probability that the correlation will exceed threshold at word synchronization time $\left[p_0(v)\right]$. This equation is

$$\text{C.F.} = 1 - \frac{\text{max. } p_\delta(v)}{p_0(v)} \cdot \quad \text{for} \quad \delta \neq 0 .$$

When comparing code sets, the statistics should be obtained using the same SNR and threshold level. For the foregoing calculations, the Stiffler modified code set has a confidence factor of 0.9875. A later table will show experimental confidence factors for the Reed-Muller, Digilock, and Stiffler code sets.

Detection by Correlation

Theoretical analysis was made to determine the probability of word error for a system that will demodulate a set of 2^n bi-orthogonal code words with n information bits. This derivation assumed perfect word synchronization and sampling of the correlator outputs every nT seconds at correct phase time (i.e., δ equal to zero). The decision selects the correlator with the greatest positive voltage at the correct phase time. The correct word will be selected if the positive outputs of all other correlators are less than that of the transmitted code correlator. Assume that a transmitted word produced a mean voltage of $+E$ at synchronization time on the correct correlator. The probability that the correct code will be selected is

$$P_c(n) = \int_0^\infty p(x)\,dx \left[\prod_{j=1}^{2^{(n-1)}-1} P(y_j < x)\right] ,$$

where $p(x)$ is the output density function of the correct correlator, and

$$P(y_j < x) = \int_{-x}^{x} p(y_j)\,dy_j$$

is the probability that the output of the jth incorrect correlator will be less than the correct correlator output.

Assuming gaussian densities,

$$P_c(n) = \int_0^\infty \frac{e^{-(x-E)^2/2\sigma^2}}{\sqrt{2\pi}\,\sigma}\,dx \left(\int_{-x}^{x} \frac{e^{-y^2/2\sigma^2}}{\sqrt{2\pi}\,\sigma}\,dy\right)^{2^{n-1}-1}$$

making a transformation of variable

$$v = \frac{x-E}{\sigma} \quad \text{and} \quad z = \frac{y}{\sigma}$$

and recalling that

$$\frac{E}{\sigma} = \left(\frac{SnT}{N_0}\right)^{1/2} ,$$

the probability of word error is

$$P_w(n) = 1 - P_c(n) ,$$

$$P_w(n) = 1 - \int_{-(S_nT/N_0)^{1/2}}^{\infty} \frac{e^{-v^2/2}}{\sqrt{2\pi}}\, dv \left\{ \int_{-\left[v+(S_nT/N_0)^{1/2}\right]}^{v+(S_nT/N_0)^{1/2}} \frac{e^{-z^2/2}}{\sqrt{2\pi}}\, dz \right\}^{2^{n-1}-1} .$$

Plotted results for a system that has n equal to five is shown in Figure 6. These results and the derivation of the foregoing equation can be found in Reference 6.

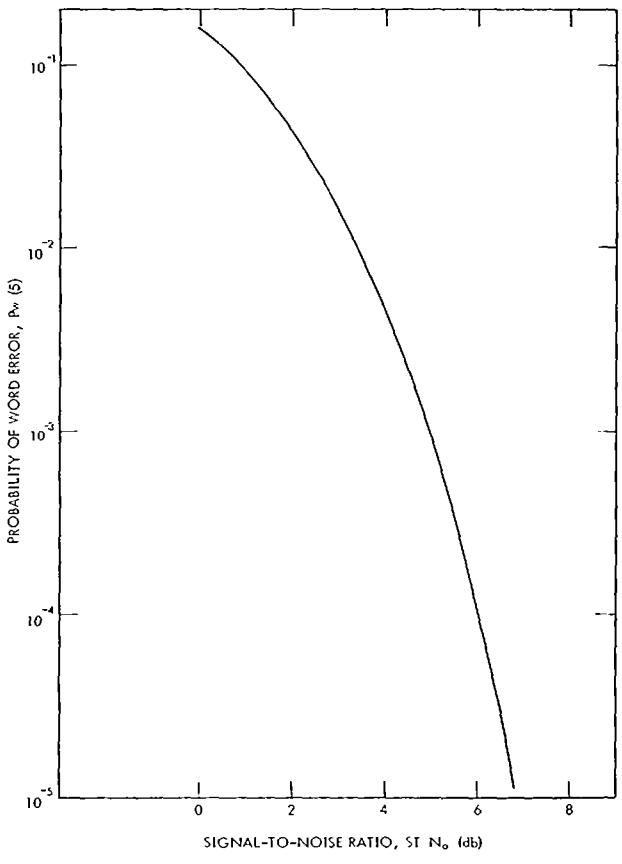


Figure 6—Probability of word error for a bi-orthogonal code of order 16.

DETAILED SYSTEM DESCRIPTION

Basically, the system is comprised of a signal simulator, code detector, test equipment, and power supplies. With the exception of test equipment, all active components are solid-state devices. Microcircuit modules are used to perform most of the digital logic. The use of solid-state devices enables the entire system to be housed in a single equipment rack (Figure 7).

When the communication source is a spacecraft, the decoder input is a bi-orthogonally coded signal with a self-synchronizing property. Data rates can be 10, 100, 1000, and 10,000 digits per second. The lowest two rates are usually used when communicating from deep space; the 1000-dps rate is used for near-earth communication, and the highest rate is used to check the spacecraft before launch. The system's output is decoded binary data, plus timing needed by the data processing equipment.

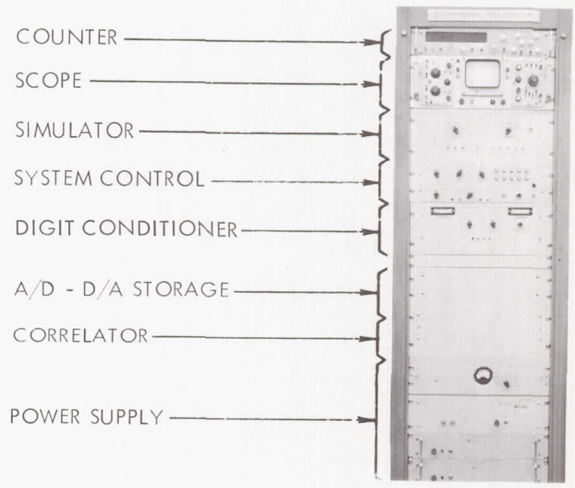
The spacecraft subsystem blocks the information into 5-bit words before coding. As more bits per word are used the system's complexity increases rapidly. For an n-bit, bi-orthogonally coded system, the detector needs at least $2^{(n-1)}$ correlators. Hence, system complexity increases directly with system accuracy, while system performance increases exponentially. A 5-bit system appears to offer a good compromise between additional complexity and improved performance.

Signal Simulator

As an aid in troubleshooting and calibrating the detector, a signal simulator is included in the system. This simulator can generate any bi-orthogonal code set of order 16. A word comparator circuit is also included to detect words that are in error. From this, a quantitative measure of detector performance is obtained. The simulator subsystem is made up of five functional blocks—the time generator, Reed-Muller code generator, modifying code generator, a binary data generator, and word comparator (Figure 8).

The time generator supplies digit clock, word clock, and other timing pulses needed by other circuits in the simulator. These internal timing pulses are generated from circuits that gate the output of a square-wave oscillator.

Information bits to be coded also can be generated internally and can be combined into three data formats. One format is a predetermined, repetitive pattern. Another data format is a random pattern. In the random format, each bit state is determined by sampling a noise voltage generated with a diode. If the noise voltage is positive at sample time, the generated bit state is a logical 1. If the noise voltage is negative at sample time, the generated bit state is a logical 0. The third data format is termed "cycle mode." In this mode, the binary information is obtained from a register which is stepped in sequence; in this manner, the simulator is cycled through all possible code formats. The cycle mode was implemented to generate dynamic and predictable data.



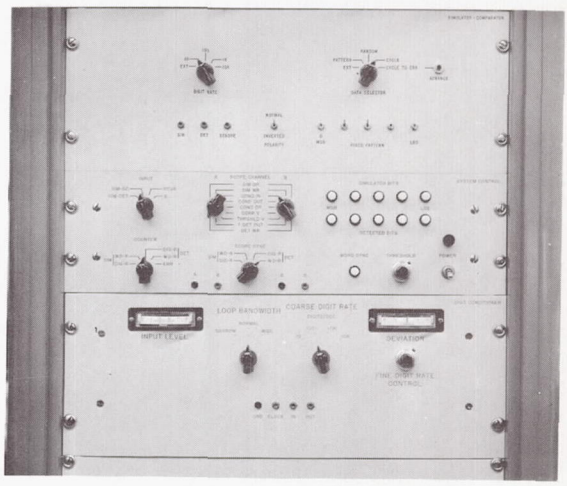


Figure 7—Photograph of the bi-orthogonal code detector.

The spaceborne portion of the system is similar in logic design to the Digilock system. These systems differ only in the modifying code that produces the self-synchronization property. Logic and timing diagrams pertaining to the code generator are shown in Figures 9 and 10. All components used in the construction of the generator are low-power microcircuits; the majority of them are simple flip-flops and gating circuits. Estimated power consumption for the code generator is 80 milliwatts.

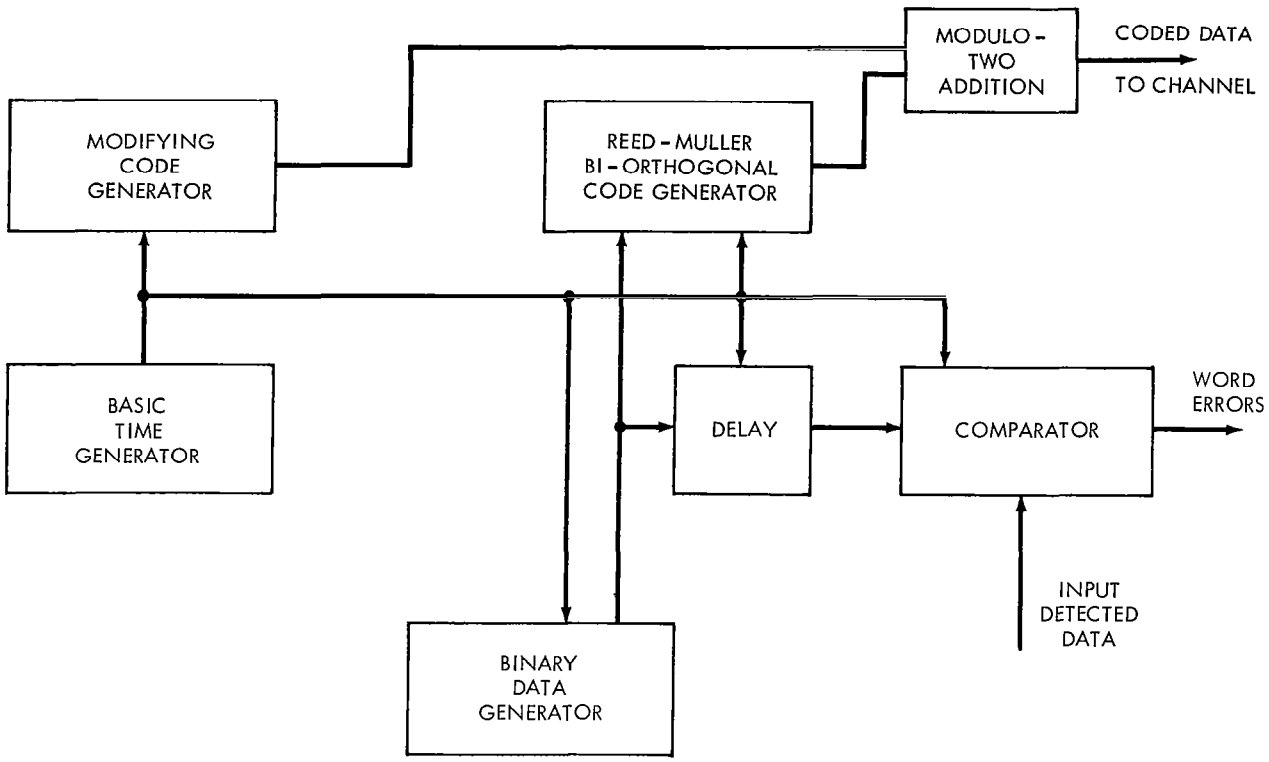


Figure 8—Simulator block diagram.

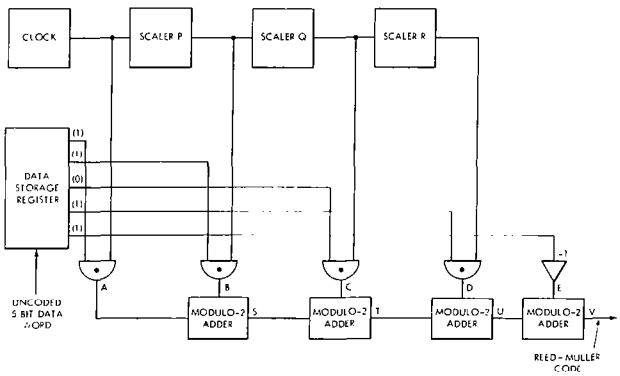


Figure 9—Logic diagram of code generator.

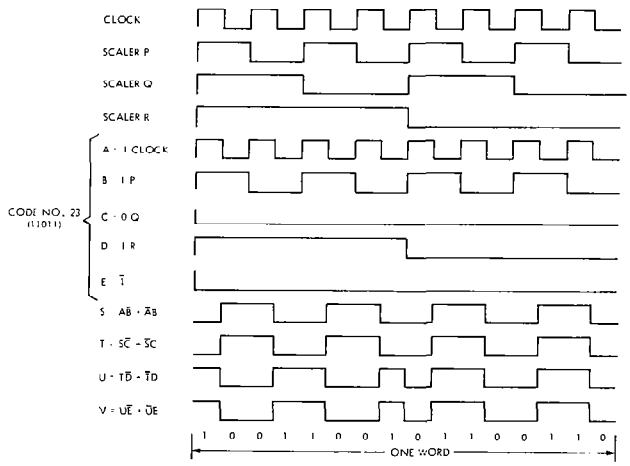


Figure 10—Timing diagram of code generator.

As is shown in Figure 9, a 16-order Reed-Muller bi-orthogonal code set is selected for transmission by the state of the five information bits in the storage register at the end of each word period. The timing sequence used to gate data from the register to the modulo-two adders is governed by a series of scalers. The Reed-Muller code is the output of the fourth modulo-two adder. A modulo-two addition of this code and a Stiffler modifying code generate the bi-orthogonal code with the self-synchronizing property. The latter code is transmitted through the communication channel.

A diode matrix is used to generate the modifying code. The unit is designed to generate any 16-digit modifying code. The desired code is programmed with switches, which control the logic level into the diode matrix. When the switches are all in the 1 state (i.e. the modifying code is all 1's), the Reed-Muller code is transmitted.

A comparator circuit determines whether the detected data word is in error. This is done by comparing, bit-by-bit, the detected data word with the delayed data word from the simulator. If an error is detected in any bit position of the word, a single pulse is sent to an event counter, which accumulates the total word error for a given time interval. Since the data rate and total number of word errors per time interval are known, the probability of word error is the ratio of total word errors to the total words transmitted.

An unavoidable system time delay occurs between the transmission of a data word and detection of that same data word. Most of the system delay occurs in the correlator, where the delay is one word period. Another discrete delay occurs in the digit conditioner. Here the delay is one digit period, which results from the data integrator. A variable delay occurs in the communication channel filter. This delay is bounded between zero time delay for wide-band filtering, and one-half of a digit period delay for narrowband filtering. (This assumes, of course, that the channel filter passes at least the fundamental frequency of the digit.) The discrete delays are easily compensated for with shift registers gated with the proper pulses. The variable delay is compensated for by generating a strobe pulse with one-eighth digit resolution and gating the data through a shift register with this strobe. With the combined use of these delays, the reference data can be delayed until they can be compared in time with the detected data.

Digit Conditioner

The digit conditioner is the first unit to process the signal as it is received from the communications channel. This unit performs two major functions: it provides the digit clock, which is coherent with the incoming signal for use in the word synchronizer circuitry; and it integrates the received signal for later use in the correlator circuitry. The digit conditioner operates at the same four rates as the simulator. A phase-lock loop (PLL) is used to generate the digit clock. The available loop bandwidths—1.5, 3.0, and 6.0 percent of the operating digit rate—are termed narrow, normal, and wide. Figure 11 shows the measured phasing capability of a PLL of a unit currently in operation at NASA STADAN tracking stations. The unit loop bandwidth is 1.5 percent. This curve indicates that digit synchronization is provided at signal levels calculated for the worst-case conditions (i.e., a 4-db SNR).

The integration process performed on the received signal is straightforward. The type of circuitry used to perform the integration is referred to as integrate and dump (I & D) filtering. Integrate and dump filters are matched filters for unfiltered binary signals (Reference 7, pp. 235-237). In the operation of an I & D filter, a digit clock is used to reset an integrator to a 0-volt initial condition at the start of each received digit. A sample and hold (S & H) circuit follows the integration process. The circuit uses the digit clock to sample the integrator output voltage at the end of each integration period. This voltage is then stored for one-half of a digit period, thus

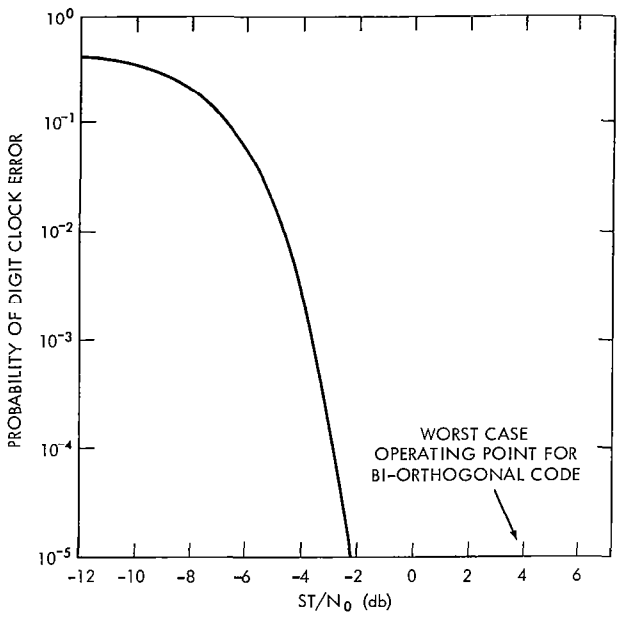


Figure 11—Phasing capability of phase-lock loop.

allowing time for the storage unit to operate on the signal level. So that no signal energy is lost in processing, two I & D filters are switched alternately. While one I & D filter integrates the received signal, the other is sampled and reset to 0 volts. Logic and timing diagrams are shown in Figures 12 and 13. The logic diagram indicates an output that is sent to a transition detector. In the following paragraph it will be shown that this signal aids the PLL in acquiring digit synchronization.

Basically, the PLL is a Costas-type loop with I & D filters used in the detectors. This technique differs from the most PPL's in that data transmissions are detected by a linear process of integration rather than by a nonlinear process of clipping and differentiation. There are two I & D filters. One filter operates with the in-phase clock (hereafter referred to as the in-phase integrator); the other filter operates with the complement clock. This filter is referred to as the out-of-phase integrator. The in-phase integrator output drives the transition detector. This detector first determines whether the integration level at the end of a digit period is positive or negative with respect to ground, and detects the digit as a 1 or a 0 (if the level is positive, the integrated digit is a 1; if it is negative, the integrated digit is a 0). The signal is now in digital form and a decision as to whether a transition has occurred can be made with standard logic. When a transition occurs, control information is gated into a voltage-controlled oscillator (VCO). This control voltage (e) results from the out-of-phase integration across a data transition. When no phase error exists between the input signal edge and the generated clock, the resultant voltage level from the out-of-phase integrator at the end of the integration period is 0 volts. When a phase error exists, there is a control voltage at the end of the integration period. The transition detector gates this error voltage to control the VCO. Figure 14 shows the linear relationship between the control voltage (e) and the degree of phase offset angle (ϕ). The output signal from the VCO drives a flip-flop divider chain from which the clock pulses are derived. The operating rate of the PLL is changed by switching flip-flops either in or out

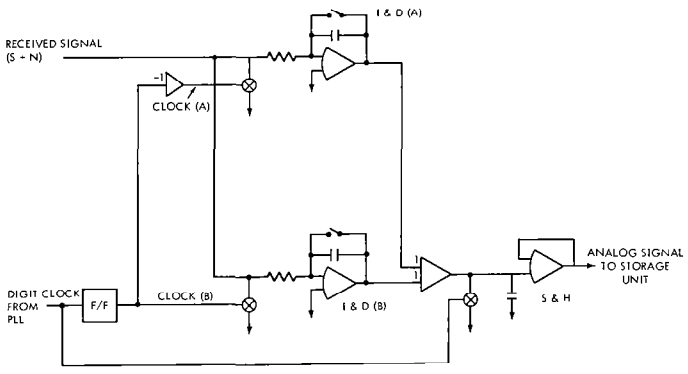


Figure 12—Logic diagram of digit conditioner data processing.

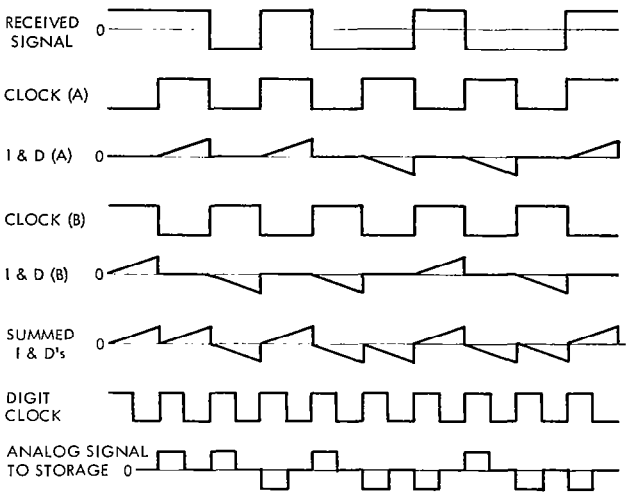


Figure 13—Timing diagram of digit conditioner data processing.

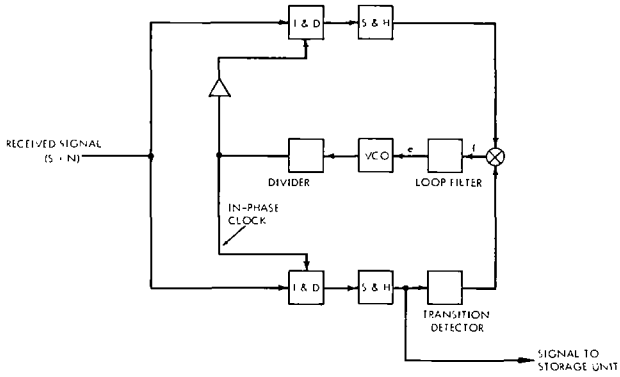


Figure 15—Logic diagram of phase-lock loop.

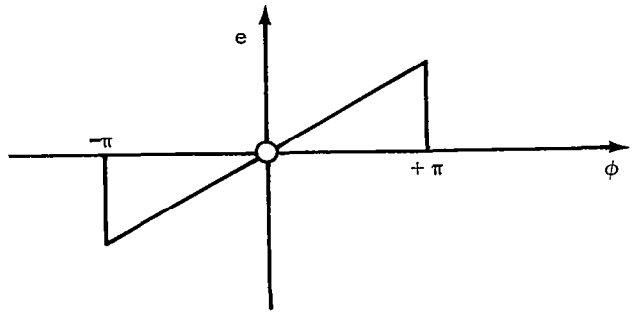


Figure 14—Relationship between control voltage and phase offset in the phase-lock loop (SNR = ∞).

of the divider chain. A block diagram and a timing diagram are shown in Figures 15 and 16, respectively.

The loop bandwidth can be determined by knowing the characteristic of the loop filter and the tracking bandwidth. A schematic diagram of the filter is shown in Figure 17. The filter has a pole at T_1 and a zero at $\mathcal{C}T_1$; this is determined from the filter transfer function

$$F_1(s) = K_1 \frac{1 + s\mathcal{C}T_1}{1 + sT_1},$$

where

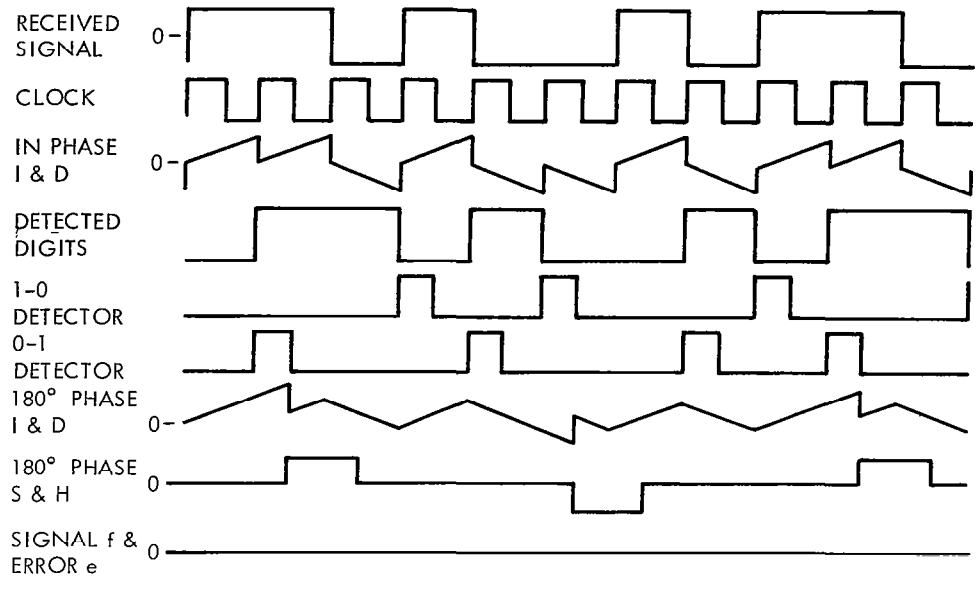
$$K = \frac{R_1 + R_2}{R_0},$$

$$\mathcal{C} = \frac{R_1}{R_1 + R_2}, \quad \text{and} \quad T_1 = R_2 C_1.$$

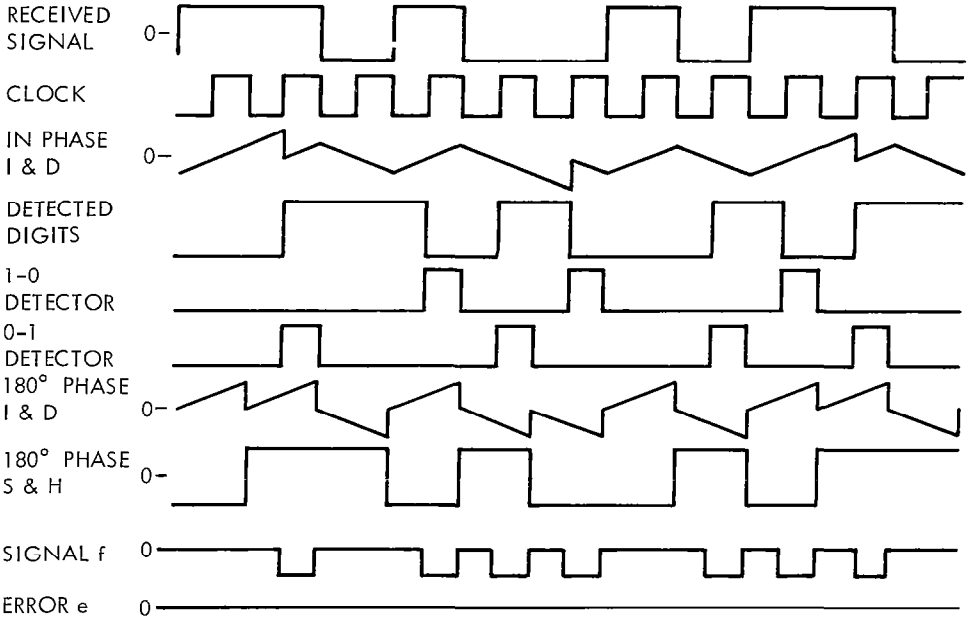
The VCO transfer function

$$F_2(s) = \frac{K_2}{s}$$

shows that another pole exists at $s = 0$. If the foregoing transfer functions and the tracking bandwidth are known, a Bode plot can be constructed, which represents the open-loop frequency response of the PLL. From this plot and a Nichols chart, the closed-loop response can be determined. Figure 18 shows both the open- and closed-loop response for normal bandwidth mode. Note that only



(a) CORRECT PHASE, ϕ = 0 DEGREE



(b) INCORRECT PHASE, ϕ = 180 DEGREES

Figure 16—Timing diagram of phase-lock loop.

one-half of the bandwidth is shown, and that the noise bandwidth is measured at the half-power point. Each of the other bandwidths is implemented by maintaining θ and K_1 constant, and changing T_1 by varying R_2. By changing R_2 the other two resistors R_0 and R_1 must be varied to keep θ and K constant. When the digit rate is changed, C_1 is varied in order that the loop bandwidth will maintain a

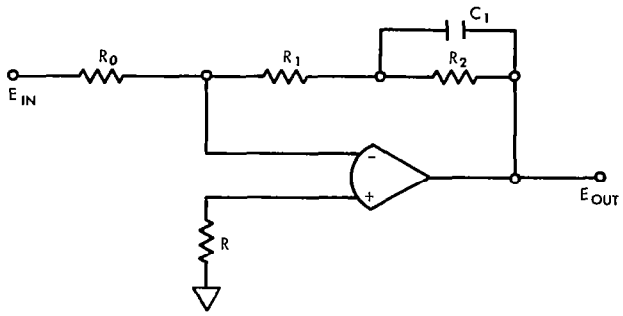


Figure 17—Phase-lock-loop filter.

constant percentage of the operating rate. The change in capacitor value is directly proportional to the change in operating rate.

Storage

The storage unit retains the integrated value of all received digits until correlation can be made between them and the stored replicas of the codes. Each correlation is performed over one 16-bit word period, thereby requiring the storage unit to store 16 digits. It would not be feasible to provide this amount of analog storage for the system's four operating rates, especially for 10 dps. For this reason the storage is done digitally, followed by reconversion to an analog signal.

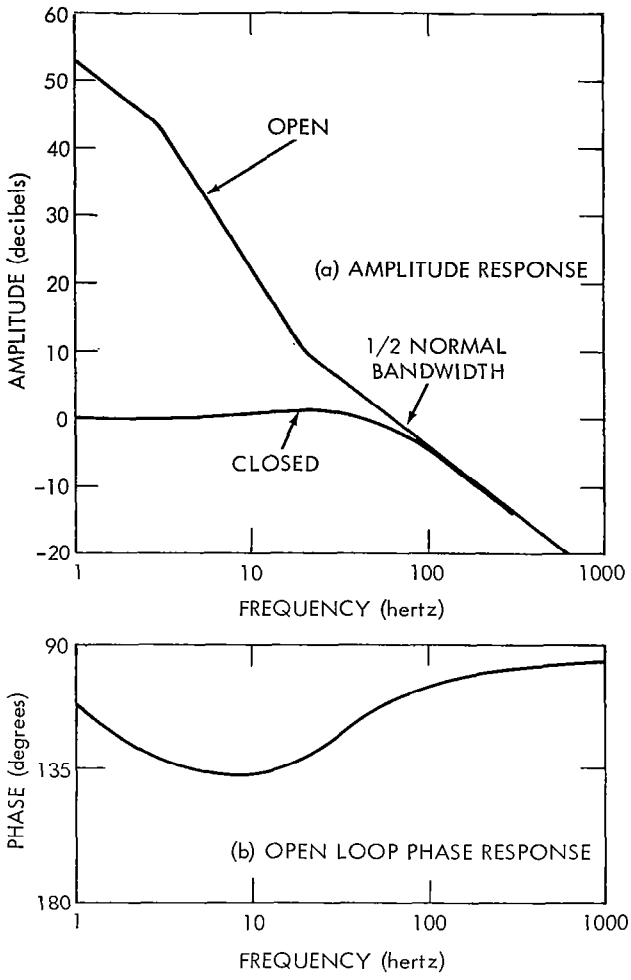


Figure 18—Open- and closed-loop Bode plot of phase-lock loop.

The first operation performed on the analog signal from the digit conditioner is conversion to a digital signal. The analog-to-digital conversion uses a successive approximation technique to derive the binary code. Digit clock from the digit conditioner is used as a command to start the conversion. Conversion takes less than 20 microseconds for a digitization to 32 levels. This is sufficient to prevent degradation of the detection efficiency. This conclusion is based on experimental data in which the probability of word error was measured as a function of the digitizing accuracy for various SNR's. During the test, digit and word pulses needed for the detectors were wired from the simulator so that word errors can not be attributed to synchronization. Figure 19 shows the plotted results for various SNR's.

After the analog-to-digital conversion, each digital signal is shifted in parallel into a five-stage storage register. When the next digit clock pulse occurs, this signal is shifted to another set of five storage registers, and the newest signal is shifted into the first register. Note that the information pertaining to a digit is contained within each set of five registers. In all, there are 16 sets

of five registers, one set of five registers for each digit of a code word. These 80 registers provide sufficient data storage since the storage time is slaved to the digit clock.

Each set of five registers is then combined with 16 digital-to-analog converters to provide 16 analog stored signals. The signals are then inverted by analog amplifiers operating at unity gain, making a total of 16 analog signals and their complements available for the correlation process which follows.

Correlator

The correlator consists of a decoding matrix, 32 correlators, and a maximum likelihood detector. Inputs to the unit are delayed signals from the storage unit and digit clock from the digit conditioner.

The decoding matrix forms the stored replicas of the transmitted code set in such a way that all bi-orthogonal code sets which can be generated from the Reed-Muller code set can be decoded. Input signals to the matrix from the storage unit are delayed in order that each digit of a code word will be present during the same time interval. This time interval lasts for one digit period within which all 32 code replicas are correlated with the delayed signal. The output signals from the matrix are then summed with resistors at the input to operational amplifiers. There are 32 operational amplifiers, each with 16 summation resistors which are used to provide the correlation value of all stored code words with the incoming word. The correlator with the greatest positive current into the summation node (hence, highest correlation value) at word synchronization time is chosen as the most likely code transmitted. The chosen code is the detected signal which is the system output to the data processing equipment.

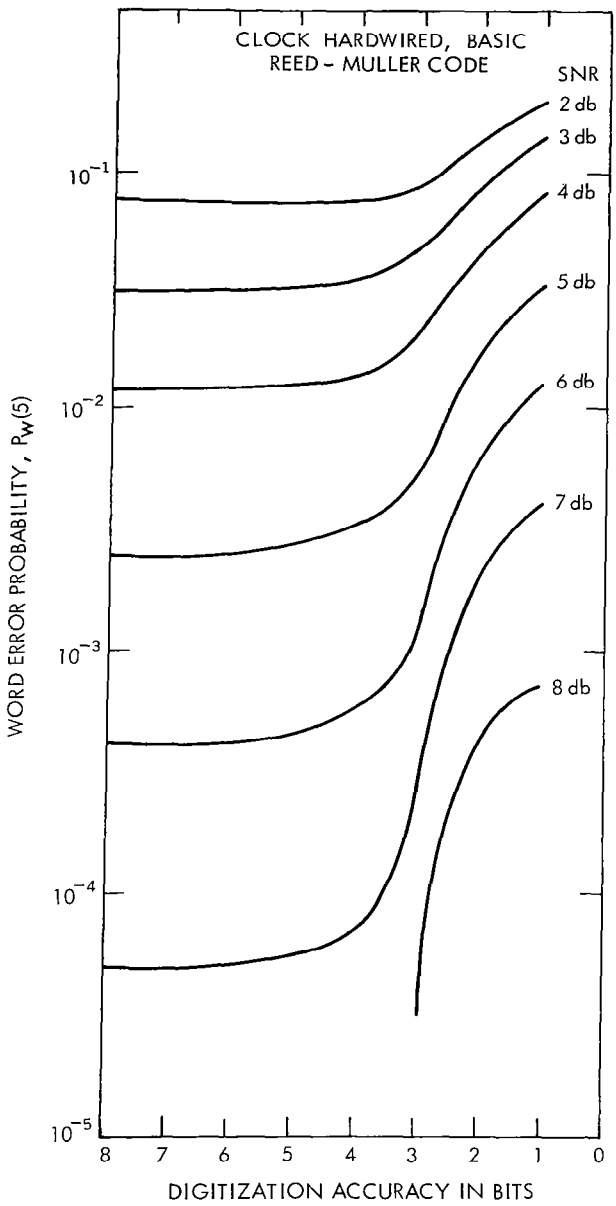


Figure 19—Probability of word error vs digitization accuracy of A-to-D, D-to-A converter.

As an aid in explaining the correlation circuitry, the system will be scaled to detect a second-order bi-orthogonal code. Scaling will only affect the number of summation resistors needed per

correlator and the total number of correlators needed to detect the code set. This code set is shown below. A decoding circuit that could detect this code is shown in Figure 20.

Code number	Code	
	B_1	B_2
0	0	0
1	0	1
2	1	1
3	1	0

For the purpose of analysis, assume that code zero is transmitted. In this case, correlator zero will have the highest correlation value at its summation junction N_0, and this correlator output voltage will be the most negative. This negative voltage will forward-bias diode D_0 and back-bias diodes D_1, D_2, and D_3. In addition, this negative voltage will be fed back through operational amplifiers 4 and 5 to the correlator feedback resistors R_0, R_1, R_2, and R_3. The correlator zero feedback loop will be closed since the resistance of diode D_0 will be small. Hence, the gain of this correlator will be unity. Similarly, the gain of the other correlators will be maximum since the diodes in their feedback path are back-biased. Consequently, correlator zero, which has the highest

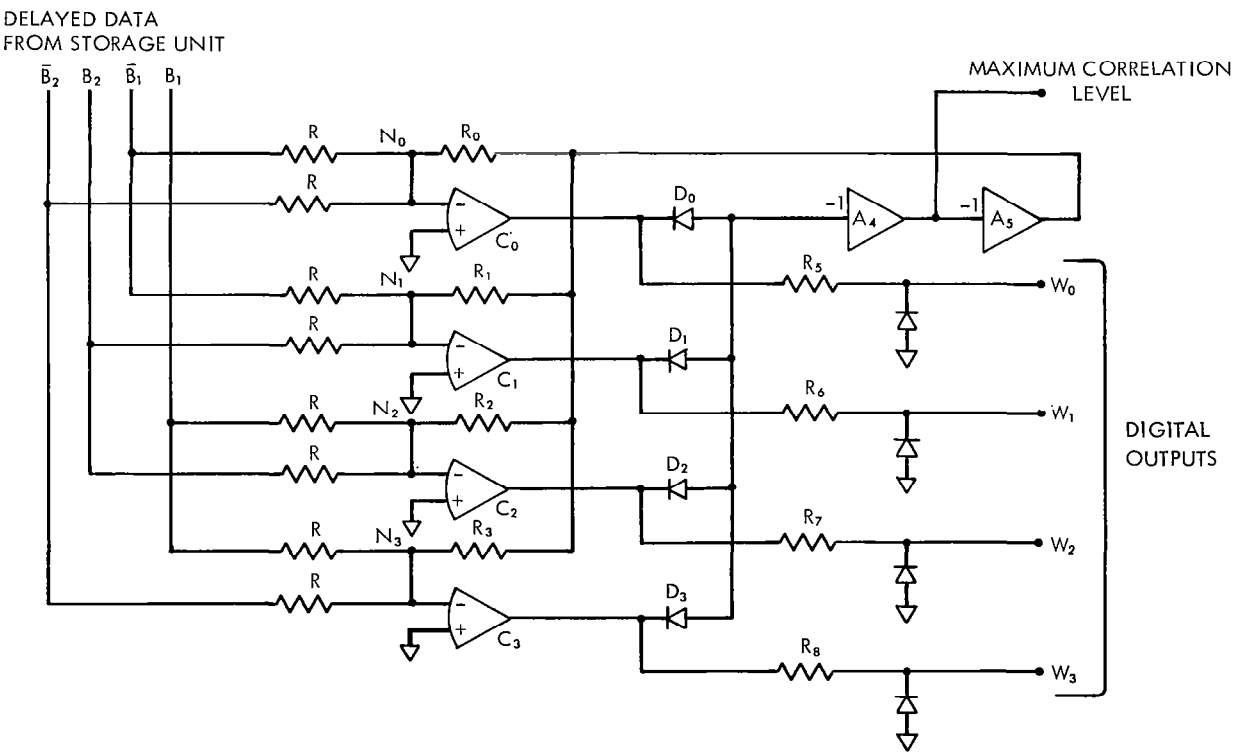


Figure 20—Scaled correlator circuit diagram.

correlation level at its summation junction, will be the controlling correlator. Its output voltage will be negative, and the other correlators will be at a maximum positive voltage. Adding another feedback diode and biasing resistors to the amplifiers will clamp the output voltages to any desired logic level. These networks are not shown in Figure 20 since they would unnecessarily complicate the drawing. Each correlator output signal can be converted to a digital signal by adding an isolation resistor (R_5 through R_8) and a diode to ground. These digital outputs are labeled W_0, W_1, W_2, and W_3 in the circuit diagram.

The maximum likelihood detector samples the four correlator output digital signals at word synchronization time and determines which code has been transmitted. This determination is made digitally with gates that are strobed with word rate pulses.

Word Synchronizer

The inputs to the word synchronizer are digit clock pulses and the maximum correlation level; the output is a synchronous word rate pulse which is used as a strobe in the maximum likelihood detector. The maximum correlation level from the correlators is compared to a threshold level. If the maximum correlation output exceeds this threshold voltage, the detector generates a pulse the duration of which is a function of the time in which the correlation exceeds the threshold voltage. These pulses are called correlation-greater-than-threshold pulses ($C > T_h$).

Several types of word synchronizing circuits were considered. The one chosen was selected on the basis of a compromise between acquisition and holding characteristics and minimum circuit complexity. A functional block diagram of the word synchronizer is shown in Figure 21. As indicated, digit clock is divided to word rate with a four-stage divider. These word rate pulses control the correlation-greater-than-threshold pulses into an in-phase and out-of-phase averaging circuit, which is used to determine word synchronization time. These two averaging circuits are binary scalers of length N. For the unit employed, the value of the scale factor N was four. The chosen scale factor depends on the system word synchronization philosophy. For instance, if a higher confidence in word synchronization is desired, the value of N should be increased. However, a penalty occurs because acquisition time also will be increased. By decreasing N, there will be a lower confidence in word synchronization, but acquisition time will decrease. The value of N then depends on where the code detector is positioned (i.e., in a field installation, or at a data processing facility). Also included as part of the out-of-phase averager is a weighting function of 15. This scale factor is needed since there are 15 out-of-phase positions for each in-phase position.

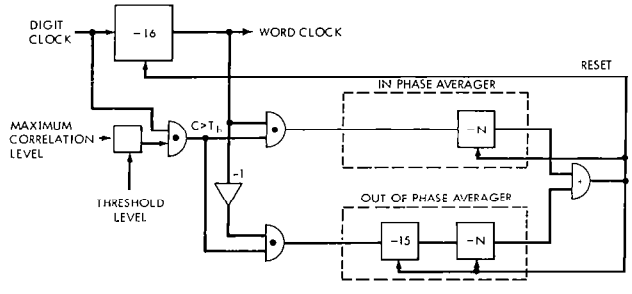


Figure 21—Word synchronization circuitry.

Initially, a phase position is chosen at the first $C > T_h$ pulse to be the correct phase. This phase position is tested by comparing the average number of $C > T_h$ pulses occurring in this phase position

with the average pulses that occur in all the other phase positions. If the in-phase scaler is filled before the out-of-phase scaler, the correct clock phase has been chosen and word synchronization can be assumed. However, if the other scaler wins, all the dividers are reset, and a new phase position must be chosen. This hunting continues until the unit acquires the correct clock phase. When this occurs, the in-phase scalers always win, provided that the system isn't perturbed by noise. When noise causes false correlations greater than threshold to occur, the unit operates in the same manner except that it occasionally loses synchronization. Theoretical and experimental statistics can verify this, when one considers various threshold levels and the probability of exceeding a given threshold for the Stiffler code set and at a SNR of 4 db. These statistics were obtained for both the in-phase and out-of-phase positions. The out-of-phase statistics were summed and the resultant was divided by the weighting function 15. A plot of these statistics shown in Figure 22 indicates close agreement between the experimental and theoretical statistics. Figure 22 also shows that the ratio of out-of-phase to in-phase statistics is insensitive to small variations of the threshold level.

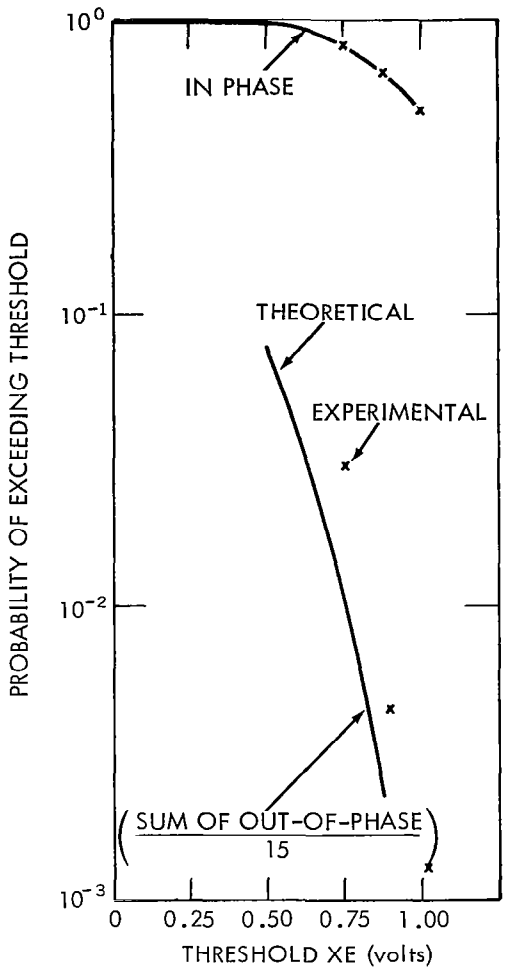


Figure 22 —Word synchronization statistics for several threshold levels (SNR = 4 db).

EXPERIMENTAL RESULTS

Experimental tests were conducted with the system described to verify the self-synchronizing capability of a code which has a comma-freedom-of-two property, and to verify that the overall probability of word error approaches the system's theoretical limit. These tests were performed in the laboratory with the communications channel simulated by a white gaussian noise source. A low-pass filter with a bandwidth to match the bandwidth available at the NASA STADAN tracking stations was used to simulate the IF filtering of an RF receiver. The SNR at the system input was defined as ST/N_0, where S is the rms signal power, T is the information bit period, and N_0 is the rms noise power per cycle.

Word synchronization statistics were obtained by correlating a delayed strobe pulse with a pulse that was developed when the maximum correlation exceeded threshold. From this correlation, the probability that the maximum correlation level will exceed a given threshold and at a given phase position was obtained. Statistics for each phase positions were also obtained by varying the strobe pulse delay. The first test in the configuration shown in Figure 23 was performed with the

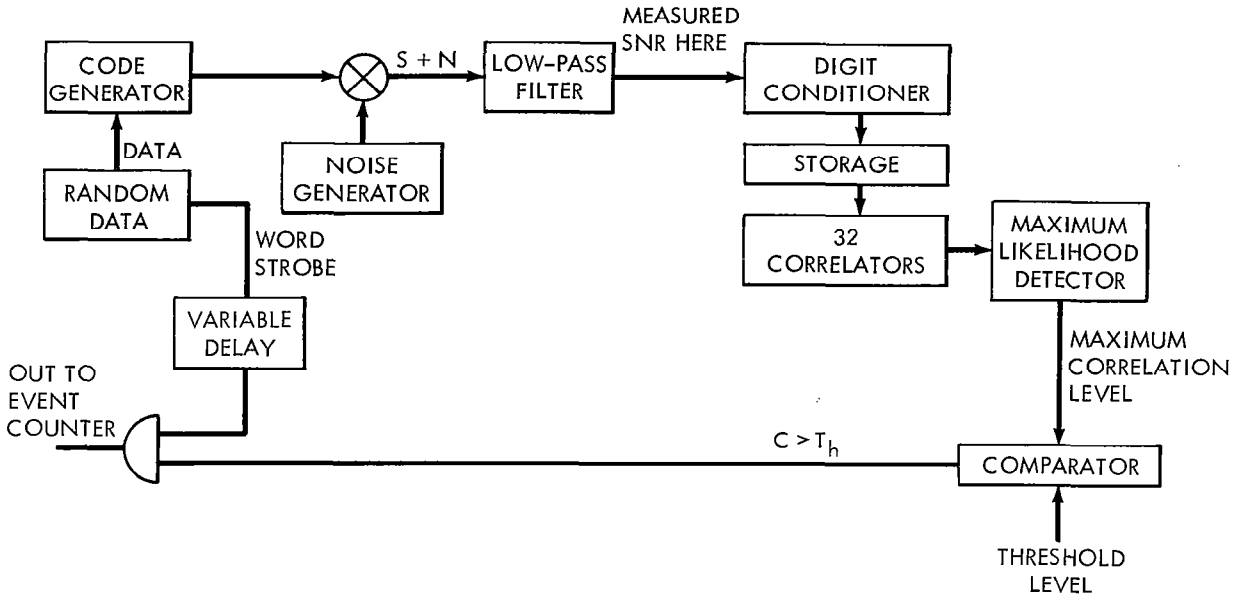


Figure 23—Word synchronization test configuration.

Stiffler code set, random data, a SNR of 4-db, and a threshold level of 0.75 E. This threshold level was calculated from

$$L = \left[1 - \frac{(16 - k)}{8}\right] E ,$$

where k is the number of digit agreements. With k equal to 14, L is equal to 0.75 E. This level was selected on the basis of the codes comma-freedom-of-two property. As can be observed from Figure 24, experimental and theoretical statistics show agreement within experimental accuracy.

Statistics for the Reed-Muller and Digilock code sets were obtained with the same test configuration and conditions as the previous two tests. From the statistical results, which are plotted in Figure 25, a confidence factor was obtained and is shown in Table 2. The Stiffler experimental statistics are also replotted in Figure 25.

Table 2

Confidence Factor for Reed-Muller, Digilock and the Stiffler Code Set at an SNR of 4 db and a Threshold Level of 0.75 E.

Code Set	C.F.
Reed-Muller	0.6875
Digilock	0.7750
Stiffler	0.9375

Statistics to determine the probability of word error were obtained by using the test configuration shown in Figure 26. Two tests were performed. One test was conducted with word synchronization derived from the comma-freedom-of-two property of the code set; the other test used word clock from the simulator. These tests were performed with the Stiffler code set, random data, and a Threshold level of 0.75 E. As can be observed from Figure 27, there is little degradation by deriving word synchronization from the code set. The overall system probability of word error is within 1.0 db of the theoretical curve.

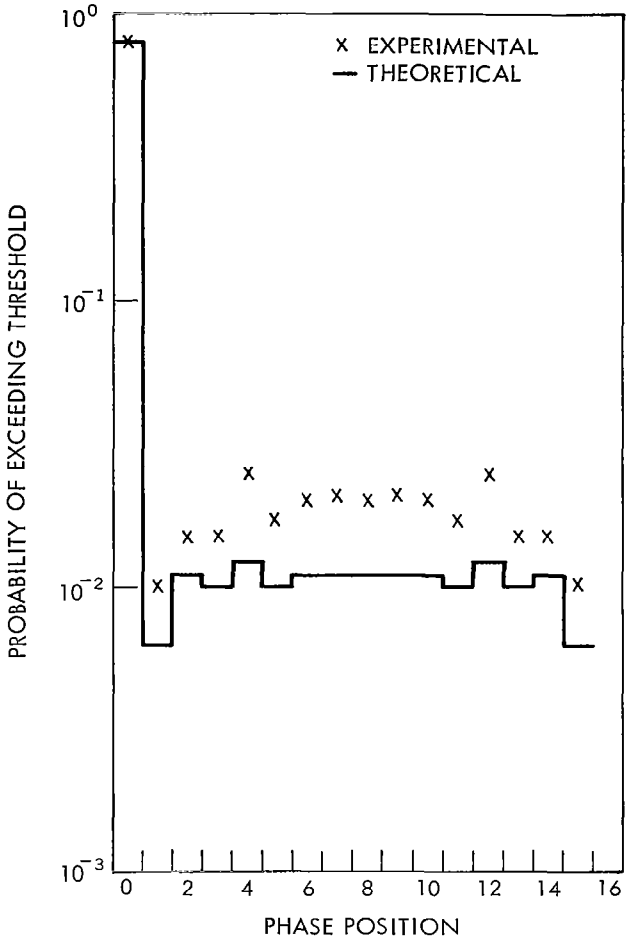


Figure 24—Word synchronization statistics for a constant threshold of 0.75 E (SNR = 4 db).

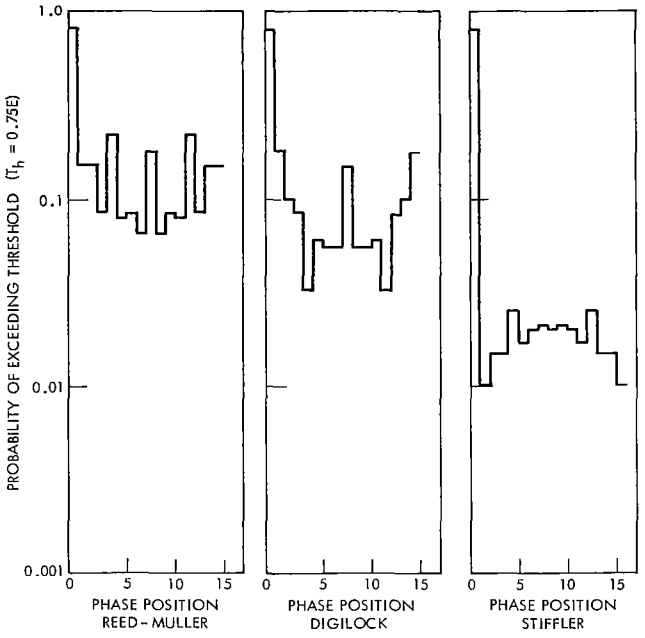


Figure 25—Word synchronization statistics for Reed-Muller, Digilock, and Stiffler code sets with T_h = 0.75 E and a 4-db SNR.

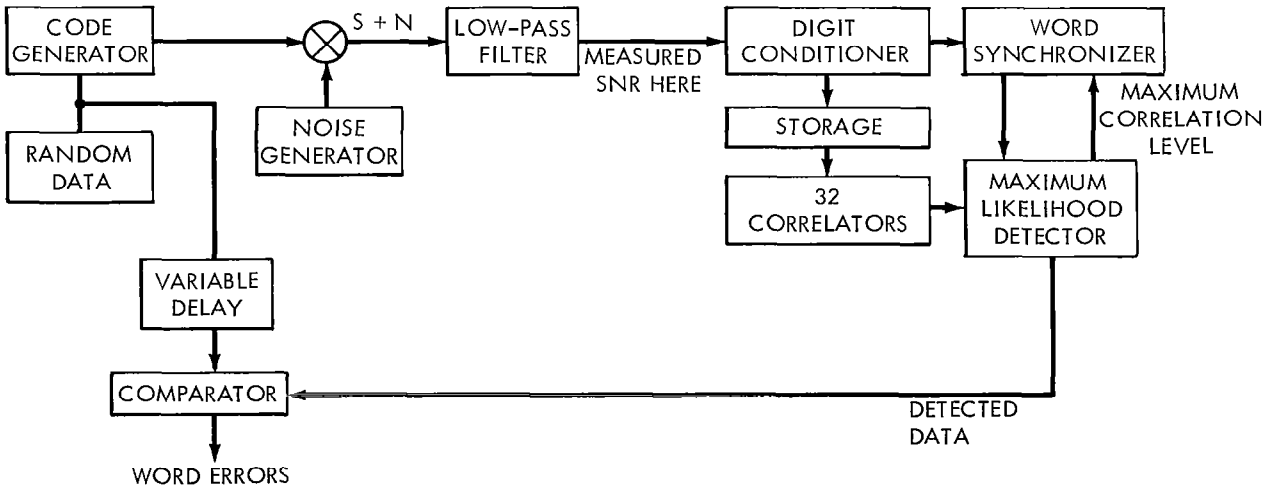


Figure 26—Test configuration used to obtain probability of word error.

CONCLUSIONS

The test results indicate that word synchronization can be acquired without utilizing a parallel channel by selecting a proper code set (i.e., Stiffler code set). With this proper code set, synchronization can be maintained below the worst-case SNR of 4 db, as shown in Figure 27. The code's comma-freedom-of-two property enables word synchronization to be achieved with a circuit requiring only a few logic modules and does not require a computer. Using the word synchronization circuitry, detection can be performed in real time. This is a requirement of data processing equipment that is maintained at NASA field installations.

Measured probability of word error is within 1 db of theoretical predictions. This figure is approximately 3 db better in performance than the standard pulse-code-modulated systems that are now used on spacecraft.

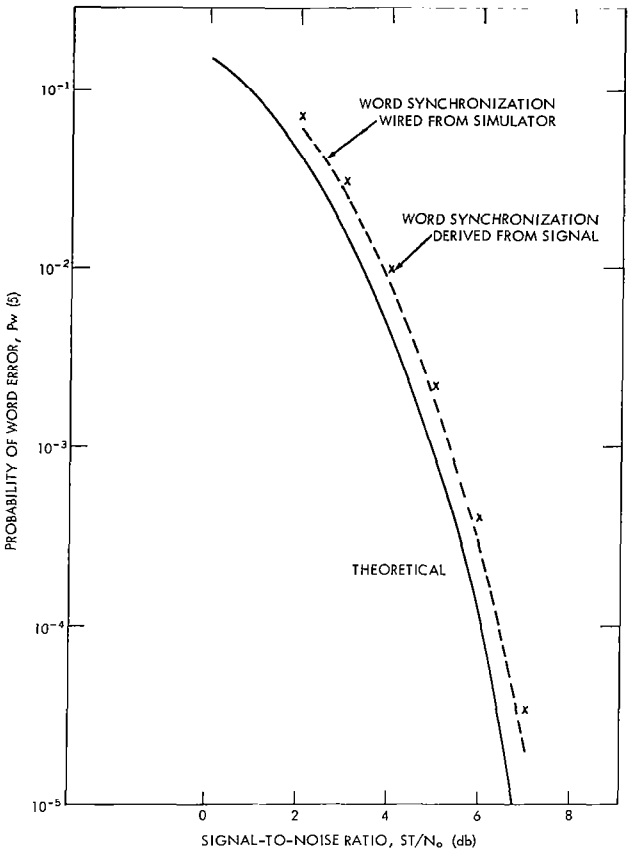


Figure 27—Probability of word error experimental statistics.

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REFERENCES

1. Purcell, J., et al., "A Proposal for the Galactic Probe Communications and Data Handling Subsystem," Goddard Space Flight Center, September 1965.

2. Reza, F. M., "An Introduction to Information Theory," New York: McGraw-Hill, 1961.

3. Reed, I. S., "A Class of Multiple-Error-Correcting Codes and the Decoding Scheme," *IRE Transactions on Information Theory*, PGIT-4, September 1954.

4. Stiffler, J. J., "Self-Synchronizing Binary Telemetry Codes," Ph. D. Dissertation, Dept. of Electrical Engineering, California Institute of Technology, 1962.

5. "Tables of Normal Probability Functions," U. S. Dept. of Commerce, National Bureau of Standards, Applied Math Series, #23.

6. Viterbi, A. J., "On Coded Phase-Coherent Communications," *IRE Transactions on Space Electronics and Telemetry*, March 1961.

7. Wozencroft, J. J., and Jacobs, I. M., "Principles of Communication Engineering," New York: John Wiley and Sons Inc., 1965.