NASA CR- 86105

FLUIDIC DECODER AND DISPLAY DEVICE

By Jacq Van Der Heyden

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Prepared Under Contract NAS 12-532 by
Martin Marietta Corporation
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TECHNICAL RESPONSIBILITY

This program is sponsored by the Electronic Research Center of the National Aeronautics and Space Administration, Cambridge, Massachusetts, under Contract NAS 12-532. The NASA monitoring scientist is Mr. E. H. Hilborn. The program manager at the Martin Marietta Corporation, Orlando, Florida, is Mr. Philip C. Gregory. The principal investigator is Mr. Jacq Van Der Heyden.

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SUMMARY

This study, performed for the Electronic Research Center of the National Aeronautics and Space Administration by the Martin Marietta Corporation under Contract NAS 12-532, demonstrates the feasibility of a fluidic decoder and display device for use on board a spacecraft. To provide meaningful restraints for the type of decoder and display device to be investigated, the typical requirements of a conventional decoder and display device as used on board a spacecraft were taken as guidelines for this study. The resulting system may be used in place of the relay-type hardware currently planned for this application. However, application of the results of the investigation is by no means restricted to spacecrafts. The device may find suitable application in a variety of aerospace and industrial pneumatic or fluidic systems where decoder and displays are required.

Feasibility was demonstrated through a study program, analysis of alternatives, and the development of a demonstration unit which has been successfully operated, and delivered as part of this contract.

The advantages of a fluidic decoder and display device are:

1 Conserves power sources by operating with available gases normally found in a space system.

2 Provides a longer life expectancy than field effect electroluminescent displays.

3 Improves readability under high ambient light conditions.

The primary advantage achieved through use of fluidics will be the savings in power required to drive the decoder. The power source for the fluidic logic and readouts is found in the pneumatic systems carried on board spacecraft for other purposes. The power is obtained "free" by utilizing the energy available in the gas stored at high pressures. This energy, available in the gas, is presently wasted as the gas is expanded from storage pressure to working pressure through pneumatic regulators. The power for the fluidic logic package is obtained by passing part of the gas around the regulators. The gas will be returned uncontaminated to the system.

The second advantage of a fluidic decoder and display device is the capability of the thermochromic readouts which provide a longer life expectancy than electroluminescent-type displays. This has distinct advantages for space missions of long duration.

INTRODUCTION

This report describes the program objectives and results of a feasibility study of a fluidic decoder and display device for use on board a spacecraft.

The advantage of such a system is the use of gases available in the spacecraft as the power supply without increasing the total amount of gases required for the mission.

This report contains:

1. A technical discussion of the investigations performed on each of the subsystems comprising a complete decoder and display device.

2. A description of the portable feasibility demonstration model built under this contract.

FLUIDIC DECODER AND DISPLAY SYSTEM DESCRIPTION

A fluidic decoder and display system, as it could be used in a spacecraft, upon command displays numerical information stored in an electronic digital computer. Figure 1 is a block diagram of the system. As shown in this illustration the electronic binary information available in the computer is, upon command, translated into binary pneumatic signals by the electro-fluid converter.

Thus, the desired information is available in pneumatic binary form in the register. The mode selector determines if the binary-to-octal converter or the binary-to-binary coded decimal converter supplies signals to the display decoder logic module. The display decoder logic module activates the display panel. The remaining parts of the system are the pneumatic power supply and a power turndown system that conserves pneumatic power between readout commands. The power distribution system provides pneumatic power to the various fluidic subsystems shown in the block diagram.

The system is comprised of the following subsystems:

1. Electro-fluid converter
2. Register
3. Mode selector
4. Binary-to-octal converter
5. Binary-to-binary coded decimal converter
6. Display decoder logic
7. Display
8. Pneumatic power supply
9. Power turndown system.

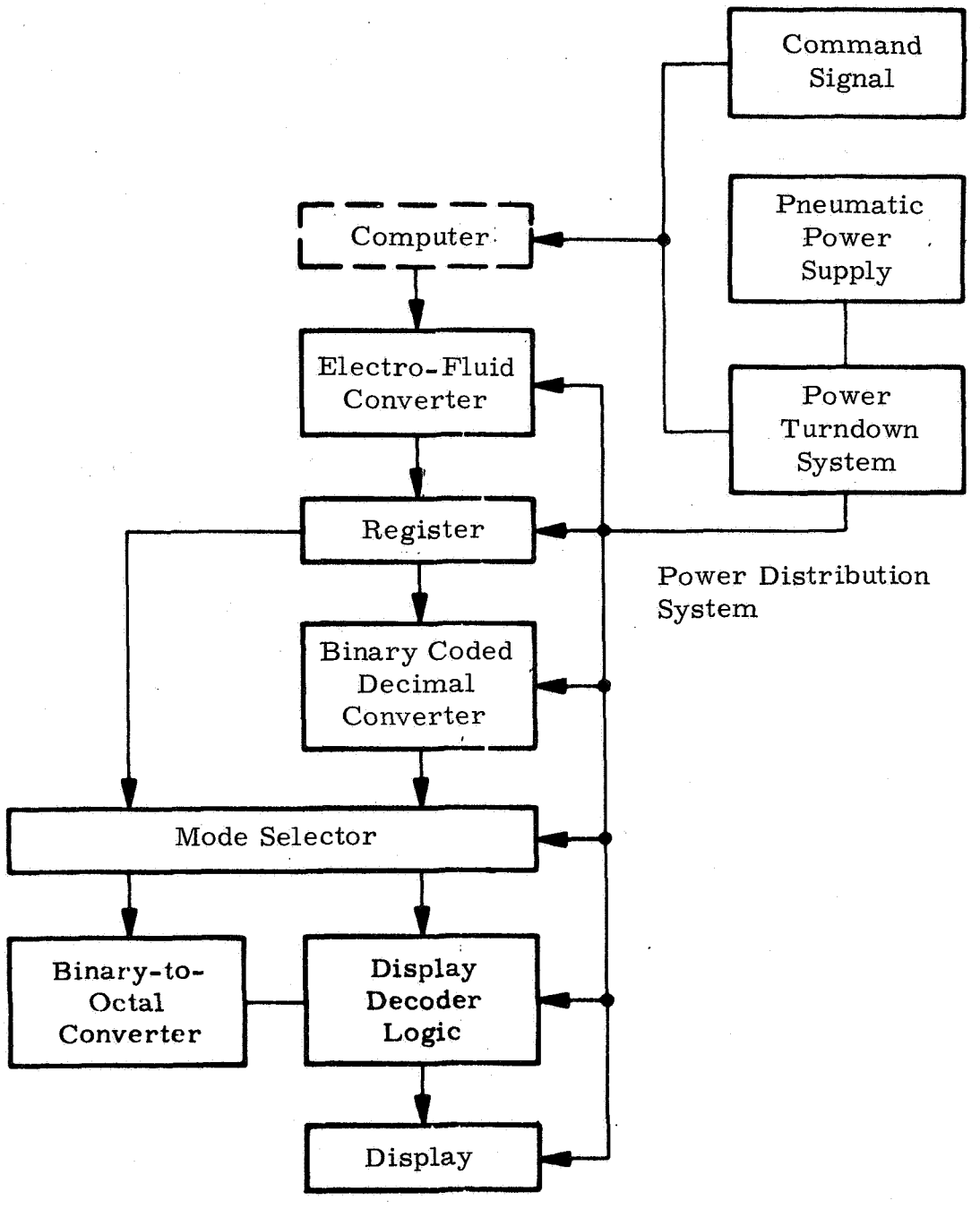


Figure 1. Fluidic Decoder and Display Block Diagram

Electro-Fluid Converter

The function of the electro-fluid converter is to translate the incoming electrical signals into pneumatic signals of sufficient power to operate the fluidic logic elements in the remaining part of the decoder and display device. The available electrical signal is a 20 V square wave of 15 ms duration. It is postulated that only a 10 mA current is available, because of computer limiations. The amount of pneumatic power required to obtain switching flow for the miniature fluidic elements is small. The low power requirements made it possible to consider several concepts of electro-fluid interface devices.

Register

The function of the register is to store, for further processing, the binary information supplied by the computer via the electro-fluid interface. The register consists of fluidic flip-flops that perform the function of a memory. The logic design of the register depends on the type of electro-fluid interface selected for this application. Both parallel and serial operation of the interface is possible. In parallel operation all 16 bits of binary information will be transferred to the register simultaneously (Figure 2). A serial operated shift register reduces the number of electro-to-fluid converters to two (Figure 3). This arrangement will require some additional fluidic logic to perform the shifting function of the register. Serial operation will require more logic elements in the register, which will influence the reliability and the power consumption of the decoder and display unit.

Mode Selector

The function of the mode selector is to activate either the binary-to-octal converter or the binary-to-binary coded decimal converter as a signal processor. The selection of these converters depends on the presence, or absence, of a plus or minus sign in the information obtained from the computer. Figure 4 shows the mode selector block diagram together with the adjacent logic modules such as the register, the binary-to-binary coded decimal converter, the binary-to-octal converter, and the display logic module.

Binary-to-Octal Converter

Binary-to-octal conversion is accomplished by dividing the binary number into groups of three bits and substituting the corresponding decimal number for each group of three binary bits (Table I). Obviously, the register contents can be used directly as Y, X, and W inputs to the display logic module. The function of the binary-to-octal converter is to generate a zero signal in all V channels

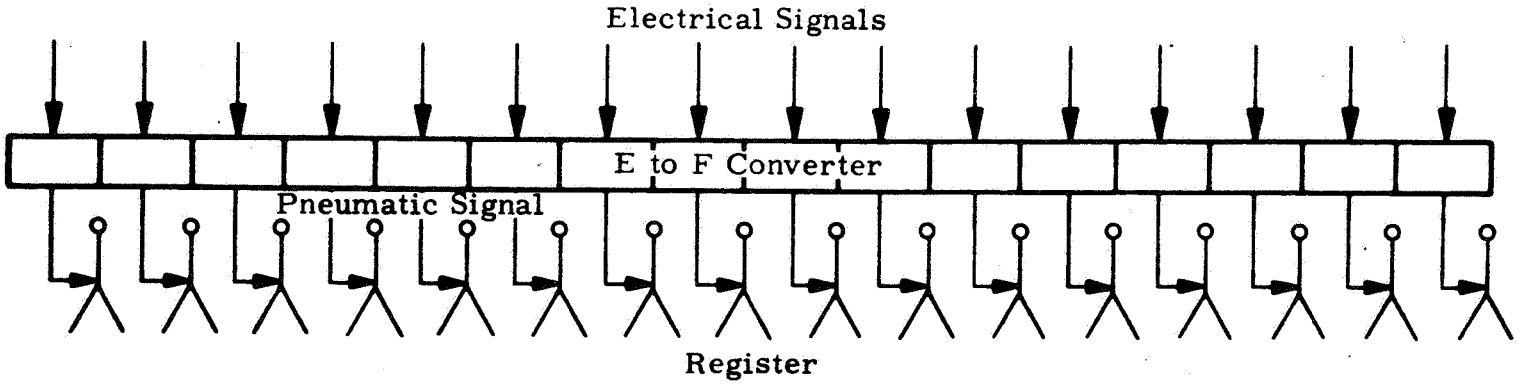


Figure 2. Parallel Register

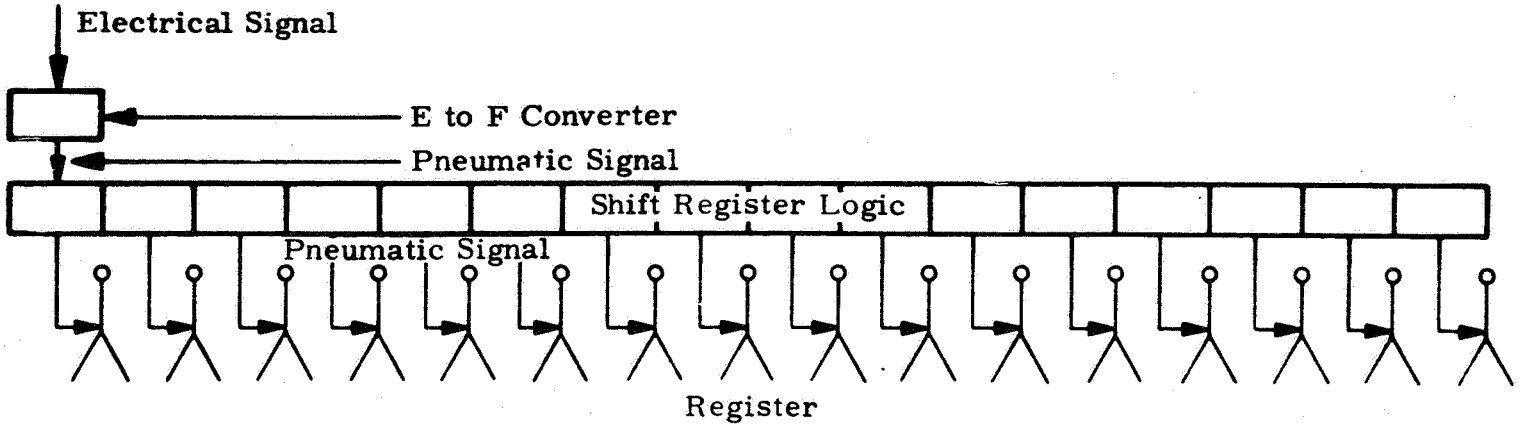


Figure 3. Serial Register

TABLE I

BINARY-TO-OCTAL CONVERSION

---R_{10}	R_9	R_8	R_7	R_6	R_5	R_4	R_3	R_2	R_1	Register
--0	1	1	1	0	0	0	1	1	0	Example of register contents
--0	1	1	1	0	0	0	1	1	0	Octal grouping
	W_3	X_3	Y_3	W_2	X_2	Y_2	W_1	X_1	Y_1	
-		7			0			6		Octal coding

to ensure the proper display of the octal number. The V signals will be zero when the M signal is absent (see Figure 4).

Binary Coded Decimal Converter

The computer information to be displayed is available in the computer in straight binary form. The five decimal digits correspond to 16 binary bits and two sign bits that must be decoded into binary coded decimal digits. Table II illustrates the conversion to be performed; column 1 shows a selection of the numbers displayed; column 2 shows part of the binary information available from the computer; and column 3 shows the binary coded decimal information necessary to activate the display. The conversion from binary-to-binary coded decimal units can be accomplished with a binary coded decimal converter.

Figure 5 shows a block diagram of one bit of a binary coded decimal converter. The inputs R_1 through R_4 signify the binary inputs. The outputs V, W, X, and Y are in binary coded decimal form and are used by the display decoder logic modules to activate the displays.

The binary-to-binary coded decimal converter consists of several adders indicated as A and two OR gates and an AND gate. Since only octal readouts are furnished in the demonstration model, the development of the binary-to-binary coded decimal converter was not undertaken.

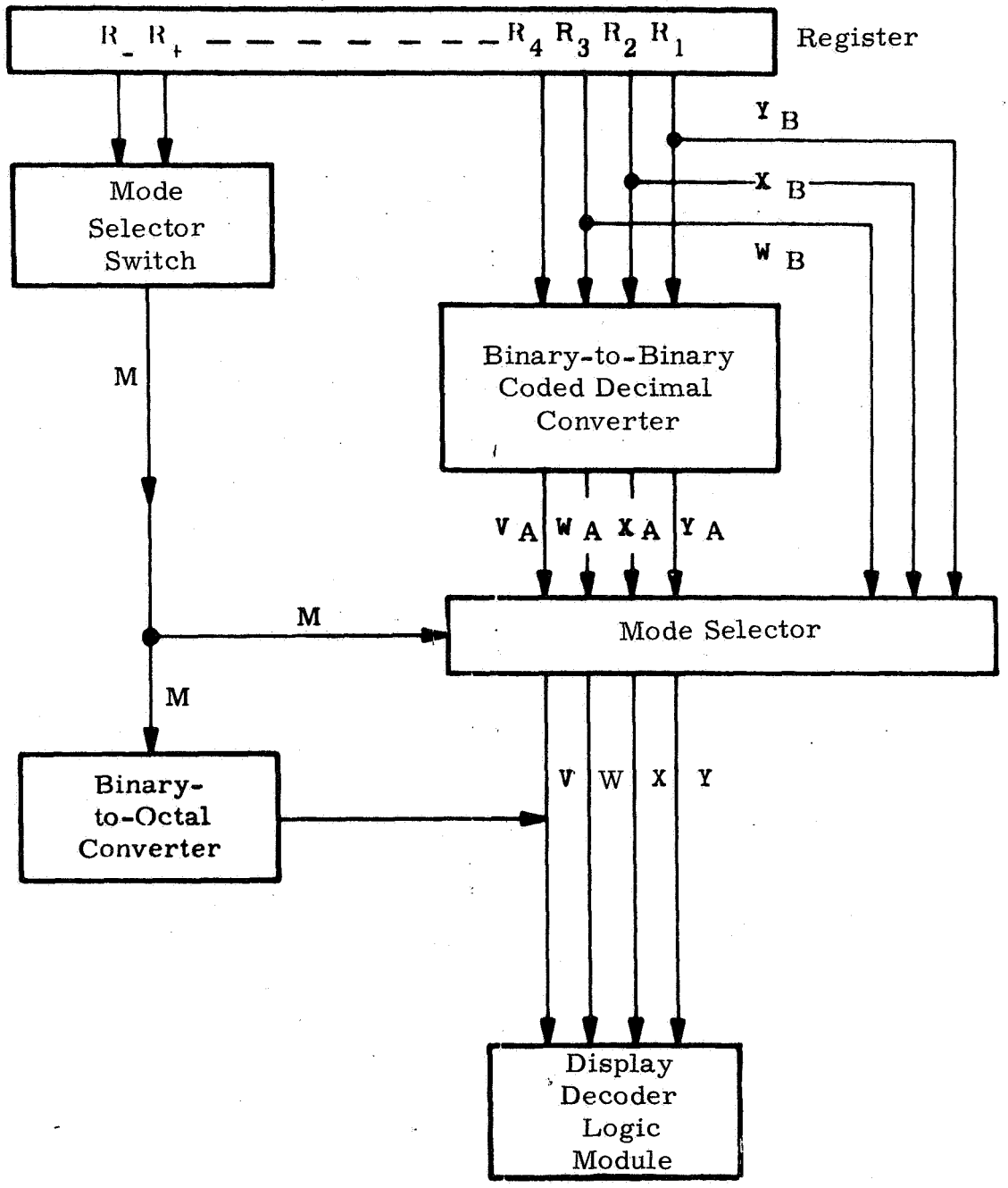


Figure 4. Mode Selector Block Diagram

TABLE II

BINARY-TO-BINARY CODED DECIMAL CONVERSION

Column 1 Number to be Displayed	Column 2 Binary Information from Computer (Only 7 Out of 16 Bits Shown)							Column 3 Binary Coded Decimal Information (3 Out of 5 Bits Shown)											
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	1
2	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	1	0	
3	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	1	1	
4	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	1	0	0	
5	0	0	0	0	1	0	1	0	0	0	0	0	0	0	0	1	0	1	
6	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	1	1	0	
7	0	0	0	0	1	1	1	0	0	0	0	0	0	0	0	1	1	1	
8	0	0	0	1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	
9	0	0	0	1	0	0	1	0	0	0	0	0	0	0	1	0	0	1	
10	0	0	0	1	0	1	0	0	0	0	0	0	0	1	0	0	0	0	
11	0	0	0	1	0	1	1	0	0	0	0	0	0	1	0	0	0	1	
12	0	0	0	1	1	0	0	0	0	0	0	0	0	1	0	0	1	0	
19	0	0	1	0	0	1	1	0	0	0	0	0	0	1	1	0	0	1	
20	0	0	1	0	1	0	0	0	0	0	0	0	0	1	0	0	0	0	
21	0	0	1	0	1	0	1	0	0	0	0	0	0	1	0	0	0	1	
98	1	1	0	0	0	1	0	0	0	0	0	1	0	0	1	1	0	0	0
99	1	1	0	0	0	1	1	0	0	0	0	1	0	0	1	1	0	0	1
100	1	1	0	0	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0
101	1	1	0	0	1	0	1	0	0	0	1	0	0	0	0	0	0	0	1
102	1	1	0	0	1	1	0	0	0	0	1	0	0	0	0	0	0	1	0
Signal	C_7	C_6	C_5	C_4	C_3	C_2	C_1	V_3	W_3	X_3	Y_3	V_2	W_2	X_2	Y_2	V_1	W_1	X_1	Y_1

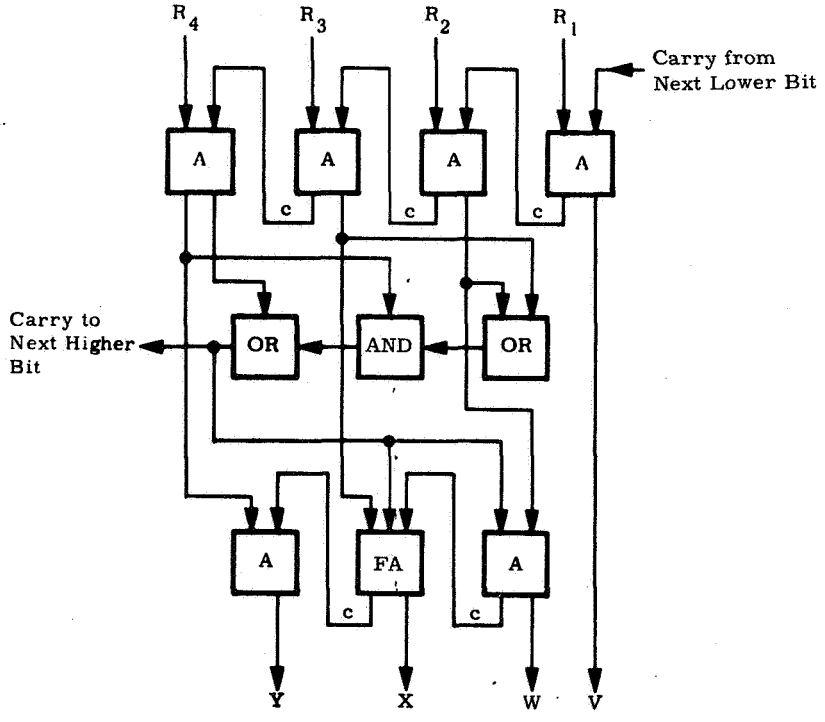


Figure 5. Binary-to-Binary Coded Decimal Converter

Display Decoder Logic

The decoder logic transforms the binary information into corresponding signals to the readout. The readout consists of an array of readout modules. The display of decimal digits is accomplished by admitting pneumatic signals to the individual sections of the display as shown in Figure 6. To form the decimal digits, each display module is divided into seven circuits labelled A through G (Figure 7). Table III shows the relationship between the displayed number, the binary four bit information from the computer, and the sections of the display panel which are to be activated to create the corresponding decimal number; a fluidic logic circuit will be used to convert this information.

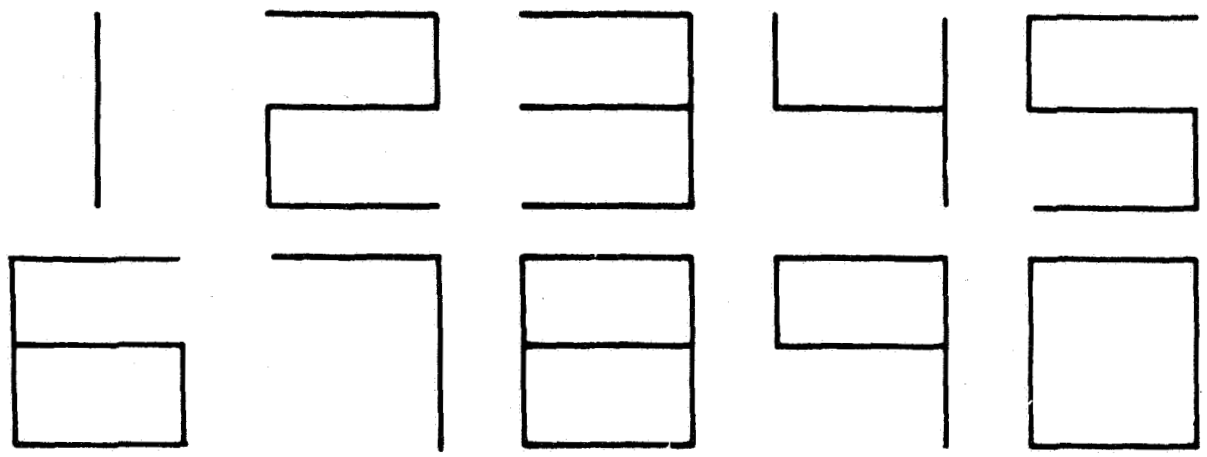


Figure 6. Display of Decimal Digits

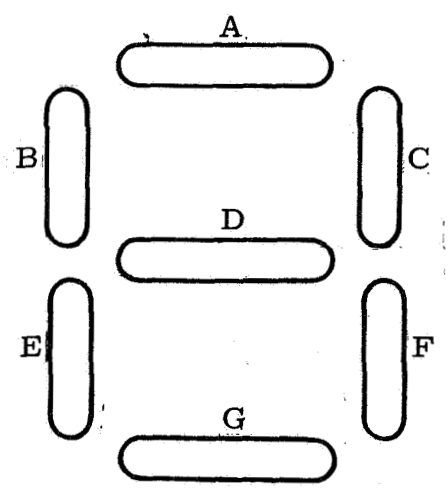


Figure 7. Indicator Matrix

TABLE III

PANEL SECTION ACTIVATION

Decimal No. to be Displayed	Binary Info From Computer				Panel Sections to be Activated						
	V	W	X	Y	A	B	C	D	E	F	G
0	0	0	0	0	1	1	1	0	1	1	1
1	0	0	0	1	0	0	1	0	0	1	0
2	0	0	1	0	1	0	1	1	1	0	1
3	0	0	1	1	1	0	1	1	0	1	1
4	0	1	0	0	0	1	1	1	0	1	0
5	0	1	0	1	1	1	0	1	0	1	1
6	0	1	1	0	1	1	0	1	1	1	1
7	0	1	1	1	1	0	1	0	0	1	0
8	1	0	0	0	1	1	1	1	1	1	1
9	1	0	0	1	1	1	1	1	0	1	0

Display

The numerical characters will be displayed on a multibar indicator matrix as shown in Figure 7. Actually only seven indicators are required per array. Indicator combinations varying in number from two to seven will be used to create the arabic characters. For example, the character eight, when displayed, requires all seven indicator positions to be activated.

Pneumatic Power Supply

Power consumption of the fluidic decoder and display device is an important consideration since it is one of the limiting factors in spacecraft design. Since the energy available in the gases carried by the spacecraft ordinarily is expended in an irreversible throttling process such as through regulators, the power for a fluidic display device can be considered free. The gas supply used by the fluidic display system will be returned to other parts of the pneumatic system.

Power Turndown System

The function of the power turndown system is to conserve the amount of gas used by the display and decoding circuits when these circuits are not in use between two subsequent readout commands.

TECHNICAL DISCUSSION

Electro-fluid Converter

The function of the electro-fluid converter is to translate the incoming electrical signals into pneumatic signals of sufficient power to operate the fluidic logic elements in the remaining part of the decoder and display device. The available electrical signal is a 20V square wave of 15 ms duration. As a design goal, the maximum load which can be driven with this signal will not require a current higher than 10 mA. The amount of pneumatic power required to obtain switching flow for the miniature fluidic elements is extremely small. A total electrical-to-pneumatic energy transfer efficiency of one percent generates enough pneumatic power to operate a fluidic element with the electrical signal available. These low energy requirements made it possible to consider several concepts of electro-fluid interface devices. The following concepts have been investigated, in order to obtain the optimum design for this particular application:

1. Thermal switching device
2. Permanent magnet flapper valve
3. Solenoid valve
4. Piezoelectric crystal device.

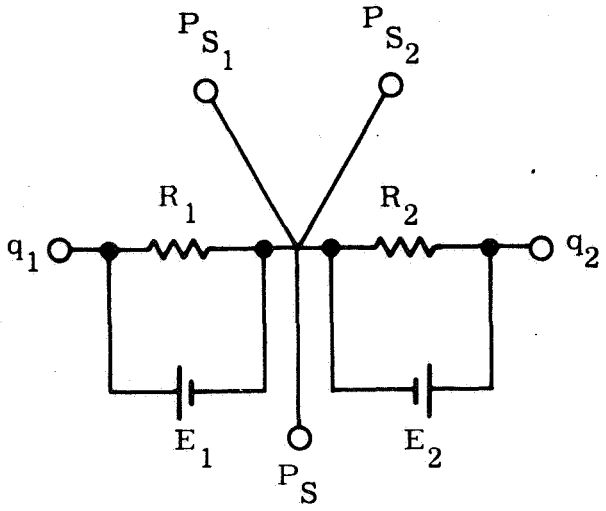
Thermal Switching Device. - The type of thermal switching device considered uses the electrical input to modulate the pneumatic control signal by heating the gas. This affects the gas density and, therefore, the flow and pressure of the incoming signal. Figure 8 shows schematic representation of two heater type thermal switching devices. One of the devices is connected to a bistable fluidic element. The second schematic shows the arrangement for a monostable element input.

The following relationship exists between the available input energy and the required output energy:

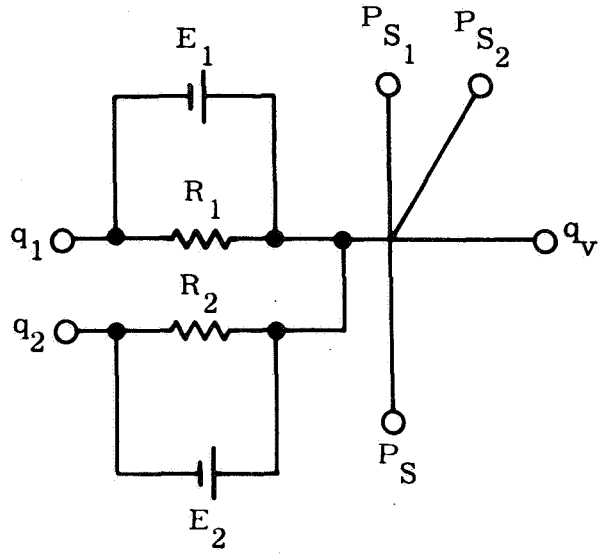
Power required to switch the fluidic element is

$$P = Q \Delta P, \qquad (1)$$

where Q is required input flow and ΔP is switching pressure; typically



Bistable Thermal, Electric-to-Fluid Interface



Monostable Thermal, Electric-to-Fluid Interface

P_S = Supply Pressure

P_{S_1} = Signal Pressure (1)

P_{S_2} = Signal Pressure (0)

q_1, q_2 = Control Flow

q_v = Monstable Vent Flow

R_1, R_2 = Thermal Element Resistance

E_1, E_2 = Electric Signal

Figure 8. Thermal Switching Devices

$$P = 0.9 \text{ in}^3/\text{min} \times 0.5 \text{ psi}$$

$$= 6.6 \times 10^{-4} \text{ ft lb/s}$$

Switching time is approximately 100 μs; therefore, the total energy required to switch the element is

$$E = 6.6 \times 10^{-4} \frac{\text{ft lb}}{\text{s}} \times 10^{-4} \text{s}$$

$$= 6.6 \times 10^{-8} \text{ ft lb} \qquad (2)$$

The heat, which is generated by passing a current through a resistor or filament located in the control orifice of an element, is transmitted into the control flow. This energy is available to control the element switching function, providing sufficient efficiency can be obtained.

The energy in the form of heat is:

$$H = RI^2t \text{ joules}$$

$$= 20 \times 10^2 \times 10^{-4} \times 15 \times 10^{-3}$$

$$= 300 \times 10^{-5} \text{ joules} \qquad (3)$$

Since 1 ft lb = 1.355 joules, theoretically, with 100 percent efficiency, the required amount of energy was available to switch the element.

Several thermal switching devices were investigated experimentally. Basically, they all consisted of a resistance wire suspended across the control channel of a fluidic element. These wires were made of tungsten and were 0.002 x 0.020 inch tungsten ribbon. In general, it was found that the electrical power input required for a pneumatic power output sufficient to cause switching was excessively high.

Electrical energy levels of 3 to 4 watts were necessary to obtain switching pressures compatible with the input requirements of the fluidic elements. The thermal capacity of the surrounding hardware and the fluidic channel cannot be minimized sufficiently to obtain lower energy levels than 3 watts. Another problem with the thermal interface device is caused by the thermal inertia of the device and the inflowing gas. The observed response time of 15 seconds is quite long and is not compatible with the required once per second updating capability of the decoder and display device.

Further work may conceivably reduce the response time to a lower level by using properly insulated materials for channel walls of the fluidic passages.

However, using these dissimilar materials as an integrated package will cause manufacturing problems, and it is highly improbable that the response time of 15 seconds can be reduced to fractions of a second as required. The experimental results eliminated this method as an acceptable solution to the interface problem.

Permanent Magnet Flapper Valve. - Several switching devices working on the principle of the permanent magnet flapper valve were considered for application to the electro-to-pneumatic interface for the decoder and display.

Figure 9 illustrates a magnetic flapper valve concept. The flapper valve consists basically of a nozzle (shown enlarged in the illustration) and a movable diaphragm. Diaphragm movement, caused by an electromagnetic force induced by a coil, results in a change in nozzle opening. An increase in nozzle opening decreases the impedance seen by the gas flow through the nozzle, which causes

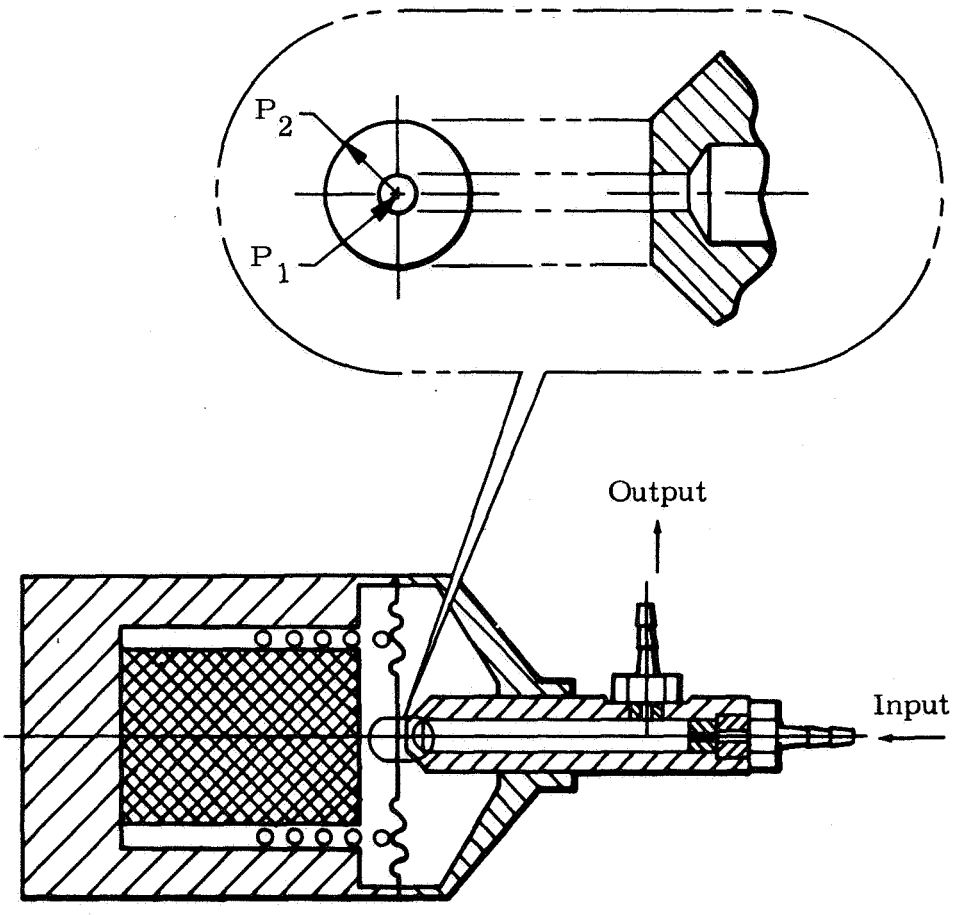


Figure 9. Electromagnetic Flapper Valve

a drop in the pressure of the input signal. Figure 10 shows, schematically, the test setup used for this investigation. Figure 11 shows the relationship of the input frequency of the electrical signal and the magnitude of the output pressure. With this particular unit, peak performance was obtained at frequencies below 250 Hz. However, operation at frequencies up to 1000 Hz is possible.

Frequencies of typical output signals at 1000 and 500 Hz for a fluidic logic gate driven by the flapper valve are shown in Figure 12, in which the time base was 1 ms/cm. The input signal to the moving coil was a 1 kc, 5V peak-to-peak sine wave (Figure 12a, upper trace). The output of the fluidic logic gate at this frequency is shown in the lower trace of the figure. Obviously sufficient pneumatic power is generated to switch the fluidic logic gate and miniaturization of this unit could result in a device which can be used for this application. A drawback to this type of a device is the moving coil configuration which is sensitive to adverse environmental conditions.

The theory of the device is best developed by treating the electrical and mechanical circuits separately, then tying them together through the cross coupling terms. Since the electric part of the device is an RLC circuit its differential equation can be written directly. However, a mechanical cross coupling term must be added to make the system consistent; thus,

$$L\,q + R\,\dot{q} + \frac{q}{C} + B\,\ell\,\dot{s} = e^{jwt} \tag{4}$$

where

B = magnetic flux

ℓ = length of moving coil

e^{jwt} = driving electro motive force

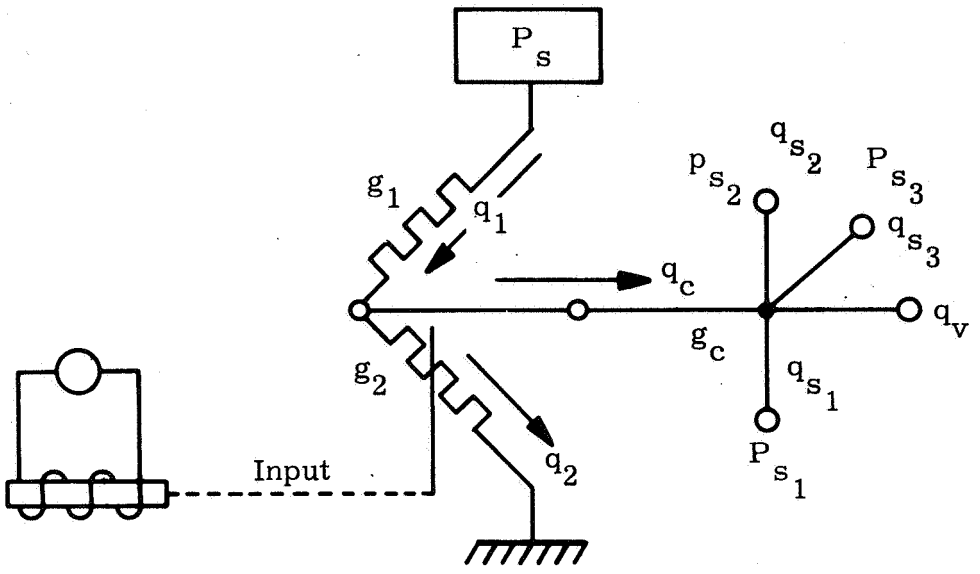
$\dot{s}$ = coil velocity

$\dot{q}$ = electrical change

Similarly, the mechanical equation is

$$M\ddot{S} + R_m\,\dot{s} + \frac{S}{C_m} - B\,\ell\,\dot{q} = 0 \tag{5}$$

where it is assumed that no mechanical force is applied and $B\,\ell$ is the cross coupling term. The steady state solution is



P_s = Supply Pressure

q_1 = Supply Orifice Flow

g_1 = Supply Orifice Conductance

q_2 = Flapper Orifice Flow

g_2 = Flapper Orifice Conductance

q_c = Control Orifice Flow

g_c = Control Orifice Conductance

P_{s_1} = OR Gate Supply Pressure Flow

q_{s_1} = OR Gate Supply Flow

q_v = OR Gate Vent Flow

p_{s_2} = OR Gate Stable Leg Pressure

q_{s_2} = OR Gate Stable Leg Flow

P_{s_3} = Signal Leg Output Pressure

q_{s_3} = Signal Leg Output Flow

Figure 10. Test Setup for Electromagnetic Flapper Valve

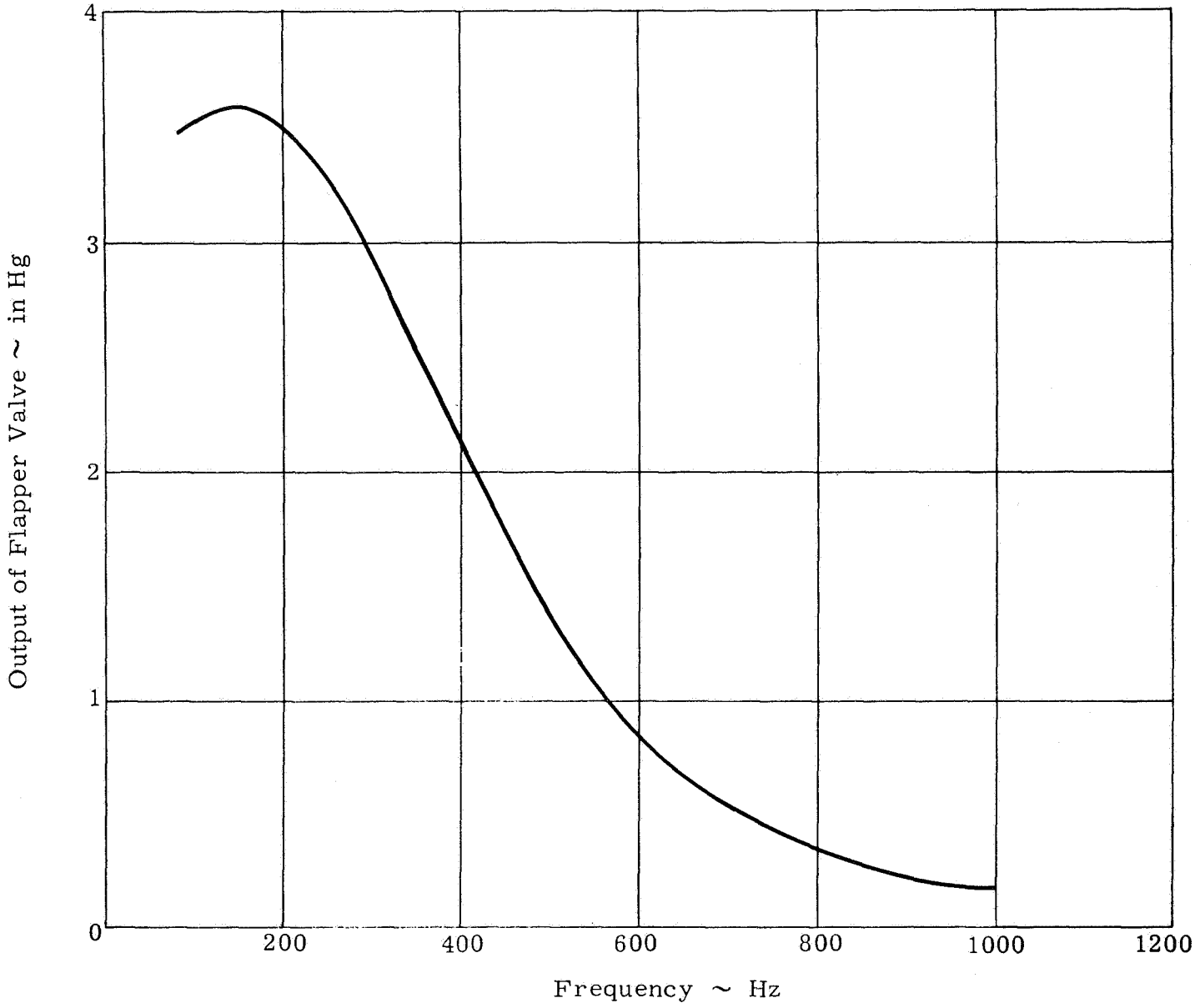
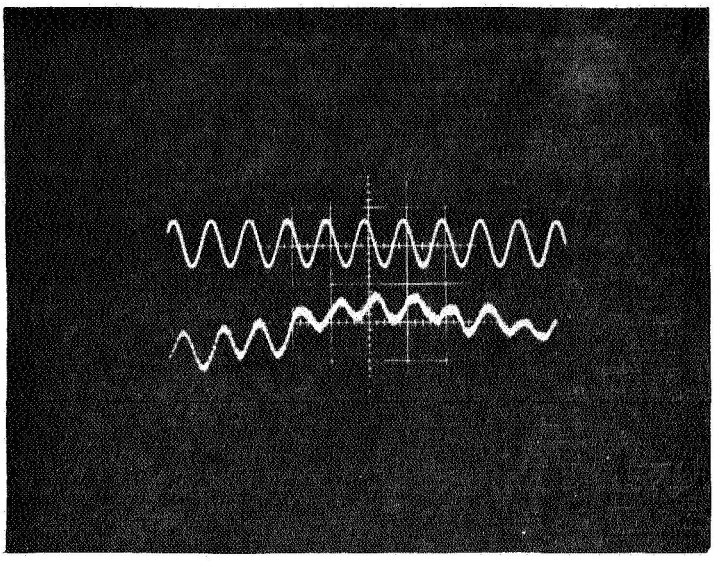
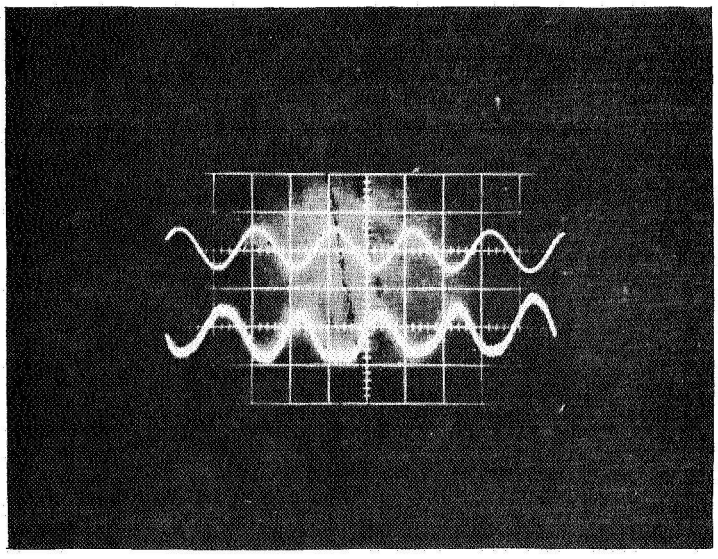


Figure 11. Electrodynamic Fluidic Interface



a. 1000 cps



b. 500 cps

Figure 12. Flapper Valve Input/Output Signals

$$E = Z_{12}\,\dot{S} + Z_{11}\,I \tag{6}$$

$$0 = Z_{22}\,\dot{S} - Z_{12}\,I$$

where

Z_{11} = impedance of electrical circuit

Z_{22} = mechanical impedance

Z_{12} = cross coupling impedance

Solving for current and velocity from the above set of simultaneous equations obtains:

$$I = \frac{E\,Z_{22}}{Z_{11}Z_{12} + Z_{12}^2} \text{ current} \tag{7}$$

$$S = \frac{E\,Z_{12}}{Z_{11}Z_{12} + Z_{12}^2} \tag{8}$$

From these equations, the current is directly dependent upon the mechanical impedance of the device, and the velocity of the coil is directly dependent on the cross coupling impedance.

The output characteristics of the flapper valve is determined from

$$q = \frac{\pi x^3 \Delta P}{6\mu \ln (r_1/r_2)} \tag{9}$$

where μ is the fluid viscosity; ΔP is the pressure drop across the orifice; r_1 is the hole radius; r_2 is the outer radius of the nozzle face; x is the flapper distance. The total force on the flapper can be approximated in the linear area by:

$$F = \frac{\pi(r_2^2 - r_1^2)\,\Delta P}{2 \ln(r_2/r_1)} \tag{10}$$

The force imparted to the plate will be approximately twice that for a sharp edge nozzle. However, it has been determined experimentally that this force will have negligible effect on the performance of the flapper valve.

Efforts were made to miniaturize the flapper valve and to substitute a fixed coil and moving plate type design for the moving coil. The first of such a device that was tested, as shown in Figure 13, consists of a flapper oriented in front of a large vent port about which the electromagnet is wound. When the electromagnet is pulsed the flapper is drawn over the vent port, thus generating a pneumatic pulse.

The dimensions of the valve tested are also given in Figure 13. This size was chosen for convenience, and future development would lead to a much smaller size.

The maximum input voltage was three volts, and the valve input pressure was 1 pound per square inch. The rise in output pulse pressure was 0.35 psig and the maximum pulse pressure was 0.45 psig. The lag time, as measured from the initiation of the electrical signal to the start of the pressure pulse, was three milliseconds, which is acceptable.

The power requirement for the device was somewhat high; however, this could easily be improved by using a greater number of turns of a finer wire for the coil and reducing the size.

Further miniaturization was accomplished by building and testing an electromechanical device which utilized a modified electrical relay specifically built for airborne application. Since power levels required to obtain suitable pneumatic signals are of the same order of magnitude as the level required for miniature airborne relay switches, advantages can be gained by use of a proven electromechanical actuator design.

By replacing the electrical switching part of the relay with a pneumatic flapper valve all the proven performance characteristics of the relay such as reliability, shock and vibration resistance, are retained. These characteristics would have to be proven for completely new developments. The power levels required to obtain switching and the operating time constants are well within those set as a guideline for this application.

The interface device was fabricated from a standard horizontally mounted (printed circuit board) "crystal-can"-size relay. One set of contacts was removed and a tubing tee was attached to one of the pins formerly used to support the contacts (see Figure 14). The glass bead attached to the relay armature which originally was used to activate the contacts fit snugly in the inside diameter of the tubing in one leg of the tee. Supply pressure was applied to another leg of the tee and a pressure gauge to the remaining leg. With a supply pressure of 1.0 psig, a 0.6 psi differential was obtained upon application of power to the coil. Step function and frequency response tests were then run with the results obtained as shown in Figure 15. Although designed for a nominal coil

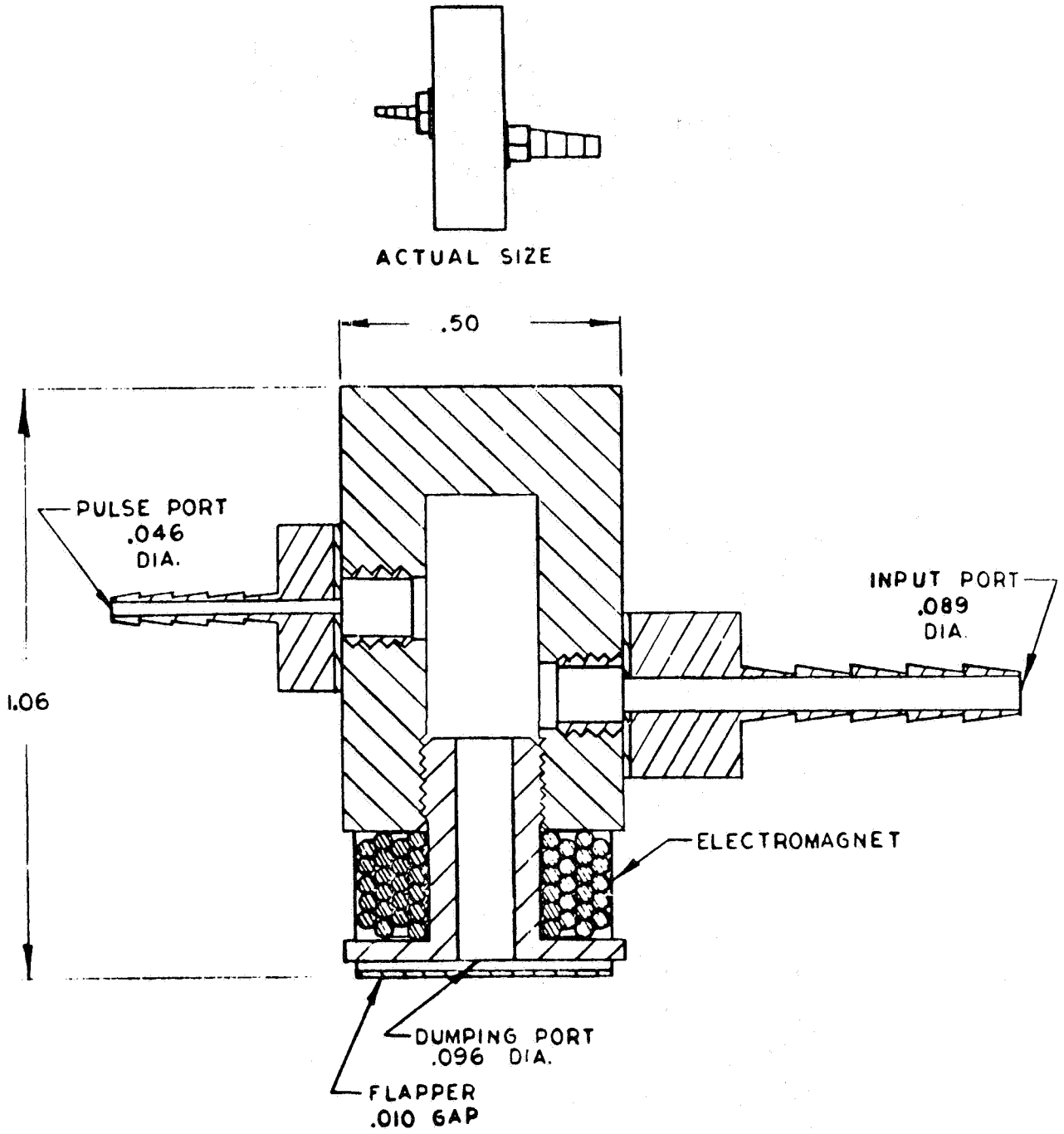


Figure 13. Fluidic Pulse Valve for Input Interface

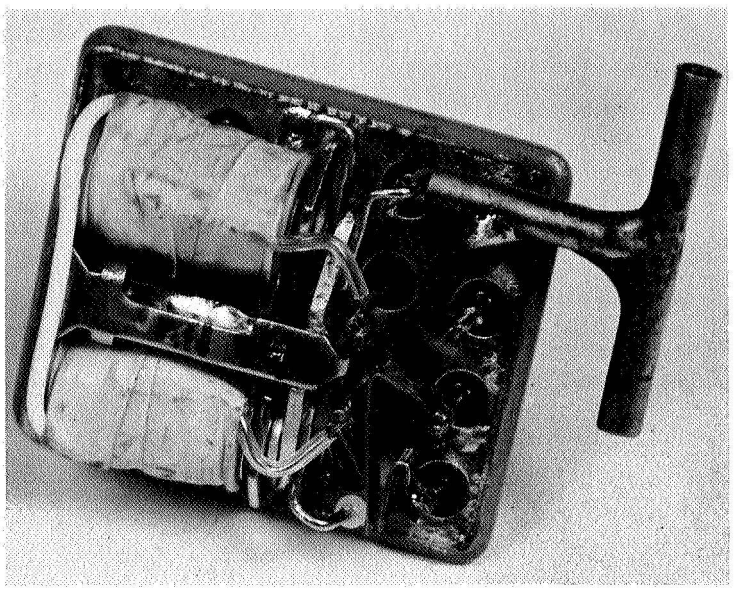
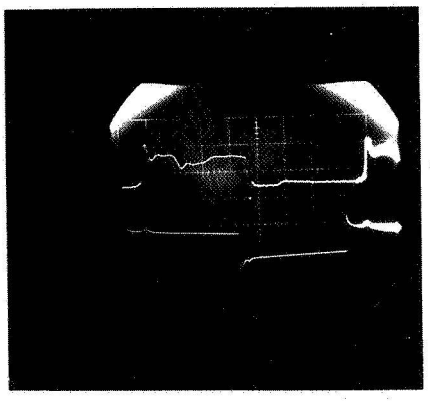


Figure 14. Electro-Fluid Interface



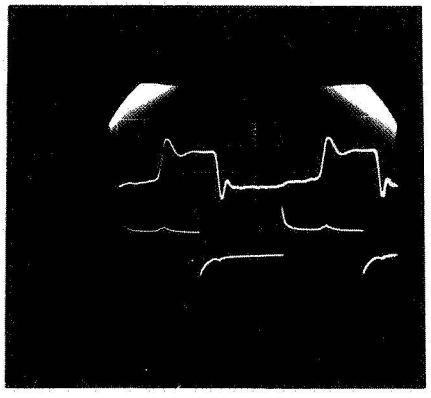


Figure 15. Interface Response Test Data

voltage of 26.5 Vdc, reliable operation could be obtained with coil voltages as low as 14 volts. Since the coil resistance is approximately 575Ω, operation at 14 volts produced a current of ≈ 25 mA. The proven high reliability of this relay mechanism could be retained in this interface when the power consumption is reduced and power consumption could be reduced substantially if the coil resistance were increased. Similar relays with coil resistance approximately 2000Ω would drop coil current to 10 mA at 20 volts. A possible drawback is the life of the glass bead seating against the end of the brass tube. A solution to this would be to make the tube of hard teflon or other high quality plastic which would reduce wear on the glass bead and provide a better seal as well.

Solenoid Valve. - Another candidate for an electromechanical interface device is illustrated in Figure 16. A commercially available miniature solenoid actuator is used to obtain an electromechanical bleedoff valve. The particular solenoid actuator was obtained from Electromechanisms, Incorporated. Dimensions and operating characteristics are shown in Figure 17. This solenoid

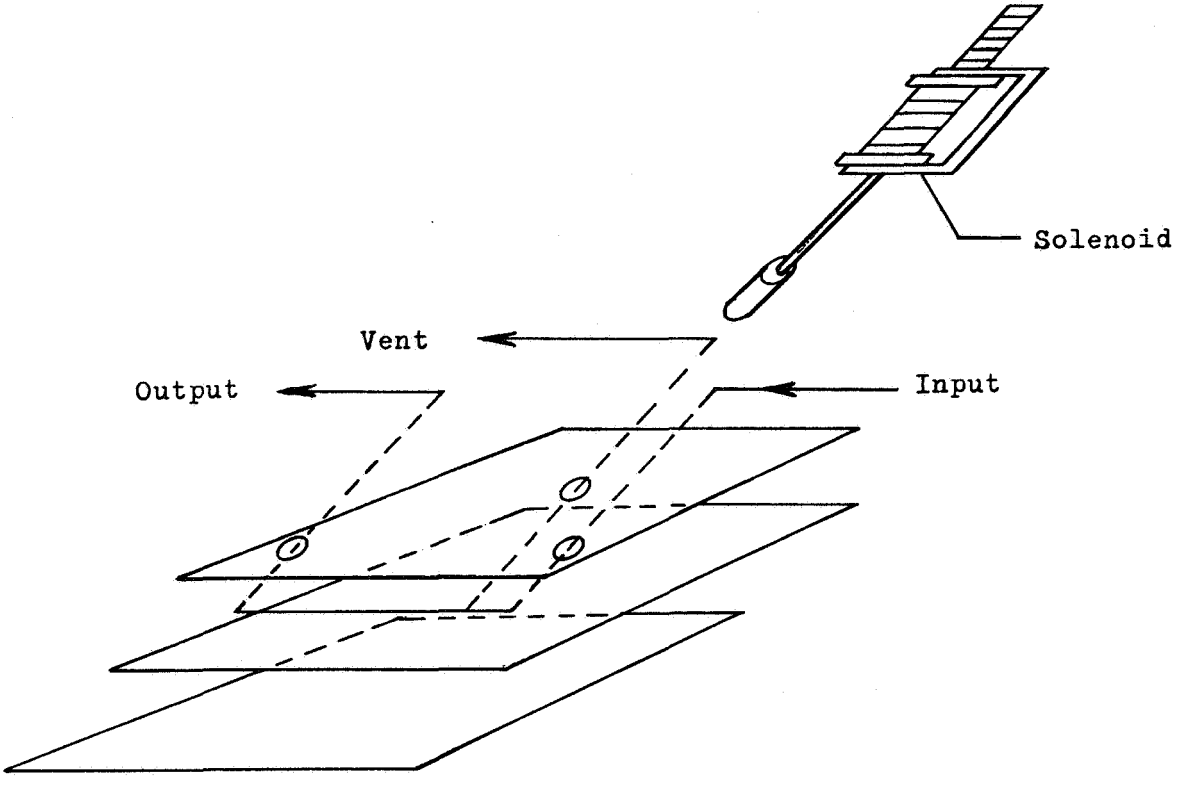
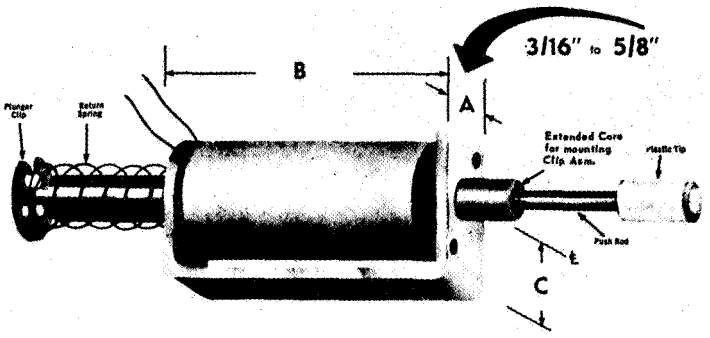


Figure 16. Solenoid Interface



SPECIFICATIONS

	SP-18
A	.180
B	.403
C	.145
MAX. STROKE	3/16"
WATTS (at nominal voltage)	1.5
WEIGHT (oz.)	.05
MOUNTING HOLES — Root Dia. for Std. Taps	#0 .046 D. 2-Back
STD. LENGTH PUSH ROD — From frame, rigid coil models	1/2"

NOMINAL VOLTAGE 100% DUTY OZ. FORCE WITH PLUNGER AT —					2 X NOMINAL VOLTAGE 25% DUTY [20 Sec. Max.] OZ. FORCE WITH PLUNGER AT —					4 X NOMINAL VOLTAGE 6% DUTY [5 Sec. Max.] OZ. FORCE WITH PLUNGER AT —				
Closed	1/16"	1/8"	1/4"	3/8"	Closed	1/16"	1/8"	1/4"	3/8"	Closed	1/16"	1/8"	1/4"	3/8"
10	3/4	3/8			14	1 1/2	3/4			16	2 1/2	1 3/4	3/4	

Figure 17. Miniature Solenoid

actuator can be incorporated into an electromechanical valve suitable for application to miniature fluidic circuits as shown in Figure 18. The solenoid actuation mechanism works like a four-way valve design. When the solenoid is not actuated as shown in Figure 18, the gas supply is connected to the X outlet ports. The $\overline{X}$ signal ports are connected to atmospheric pressure.

Actuation of the solenoid results in the plunger moving upwards thus bringing the two closing discs into the position shown by phantom lines in the illustration. Now the supply pressure is connected to the $\overline{X}$ signal port and the X signal port is vented.

The advantage of this design is the compatibility with fluidic integrated circuits as presently produced at Martin Marietta Corporation.

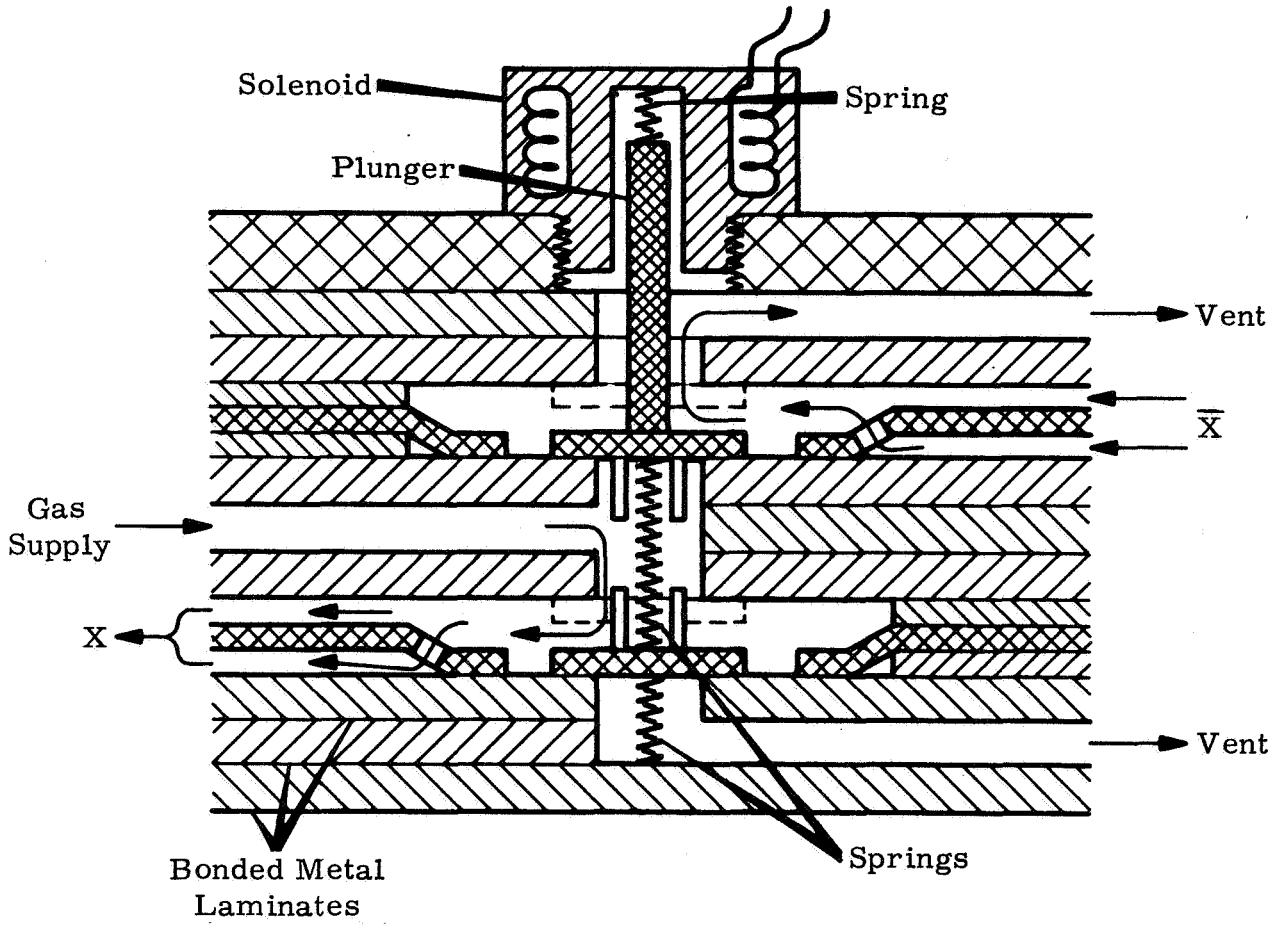


Figure 18. Etched Solenoid Valve

The main assembly of the solenoid valve can be etched into metal planes and bonded in one assembly with the fluidic circuits, which are produced in the same manner using etching and bonding techniques described elsewhere in this report.

Piezoelectric Crystal Devices. - Piezoelectric crystal devices were considered as a possible electro-fluid converter. One of the concepts considered is a crystal operated poppet valve. Figure 19 shows the piezoelectric crystal type poppet valve. The device works as follows: pressure is applied to pressure port P_1; upon excitation of the crystal, the piezoelectric action opens the poppet valve and admits the pressure to port P_2, which is connected to the fluidic element. The following equations describe the expected motion of the device:

For longitudinal low frequency excitation of piezoelectric crystals the elongation and force are, respectively,

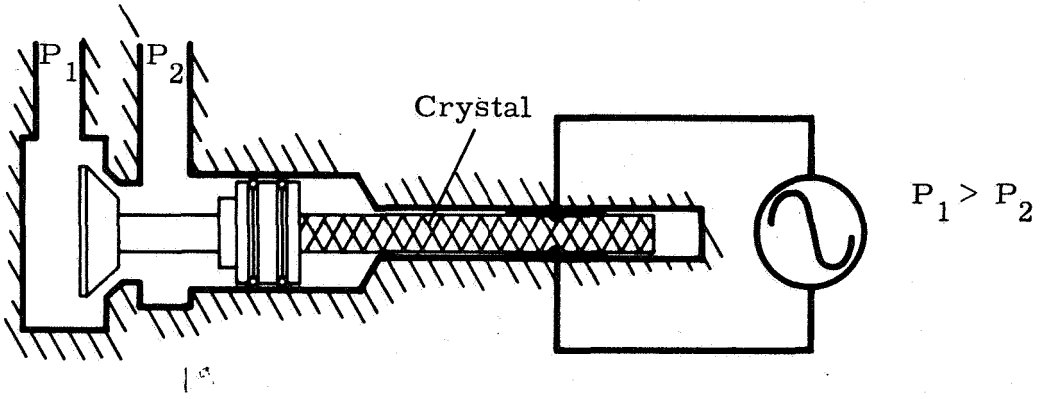


Figure 19. Piezoelectric Crystal Type Poppett Valve

$$\Delta 1 = d_{31} \frac{V1}{t} \tag{11}$$

$$F = d_{31} \frac{Vw}{S_{22}^{E}} \tag{12}$$

where d_{31} = piezoelectric constant relating strain to the applied electric field, the electric displacement, and the dielectric constant.

V = applied potential;

1, t, and w = the crystal length, thickness, and width, respectively; and

S_{22}^{E} = elastic compliance.

The above equations also apply to rectangular devices working in longitudinal elongation.

For the longitudinal type plunger valve, applying Equation (11), the displacement for Glennite HST-41 with a 20 volt signal, for example, would be

$$\Delta 1 = V_t^{1} d_{31}$$

$$= 20V \frac{0.1 \text{ meter}}{0.001 \text{ meter}} 140 \times 10^{-12} \frac{\text{meter}}{\text{volt}}$$

$$= 0.28 \times 10^{-2} \text{ cm.} \tag{13}$$

Theoretically, while marginal, this is sufficient displacement to actuate a valve to drive a standard 4 mil fluidic element. However, problems arise when

reasonable constraints are placed on the size of the interface device. The initial efforts were arbitrarily restricted to an overall size of 1.25 x 1 x 0.5 inch. It is felt that larger units are not compatible with the miniature fluidic logic modules. Since the small unit size precludes the use of transformers, the input signal voltage level is 10V. As the piezoelectric displacement is directly proportional to the available voltage, only minute dimensional changes can be obtained. The problem is complicated by the fact that a heat source is necessary to operate the thermochromic display unit. The elongation of the interface parts due to thermal expansion over the required temperature range is of the same order of magnitude as the expected piezoelectric displacement.

For these reasons the investigation of piezoelectric interfaces was restricted later on in the program to the use of bimorph type piezoelectric devices which give considerably more displacement for reasonable electrical inputs.

Figure 20 depicts the bimorph flapper valve concept.

With a constant pressure P_s applied to the flapper valve a signal ΔP will appear at the output when an electrical signal is applied to the element. The displacement for series connection is given by

$$x = 2\, d_{31}\, V \frac{L^2}{t^2} \tag{14}$$

$$= 2 \times 140 \times 10^{-12} \frac{\text{meters}}{\text{volt}}\ 100\text{V}\ \left(\frac{0.1}{0.001}\right)^2$$

$$= 2.80 \times 10^{-2}\ \text{cm}$$

This value can be doubled when a parallel connection is used.

The signal ΔP is determined from

$$\Delta P = \frac{6\mu\ \ln(r_2/r_1)\, q}{x^3} \tag{15}$$

where

μ = viscosity of fluid

r_1 = inner diameter of face

r_2 = outer diameter of face

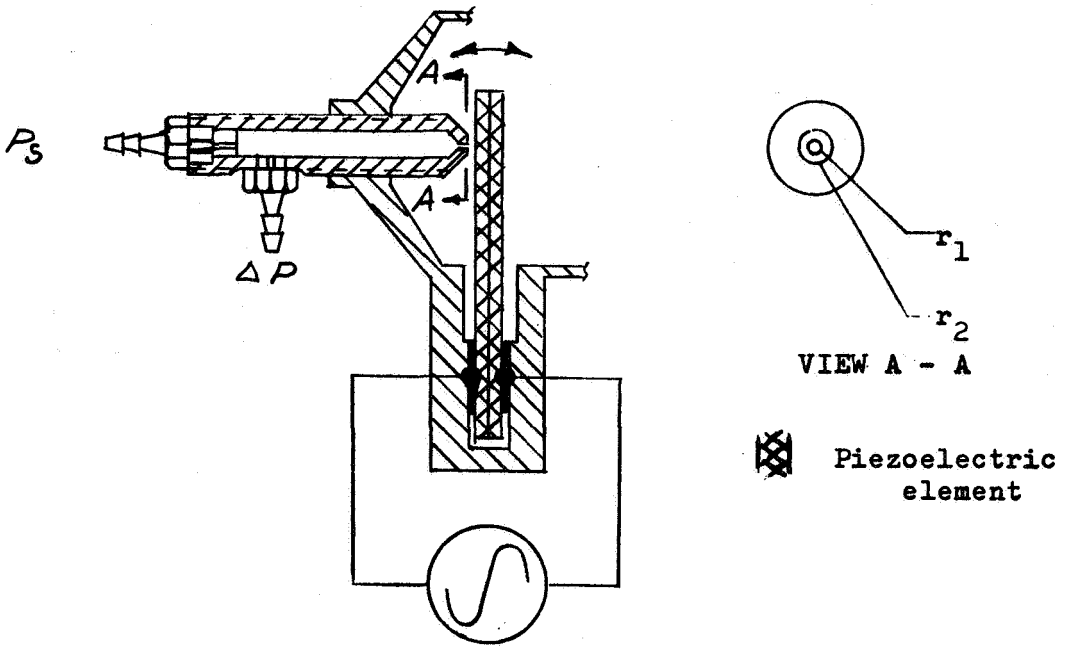


Figure 20. Bimorph Piezoelectric Flapper Valve

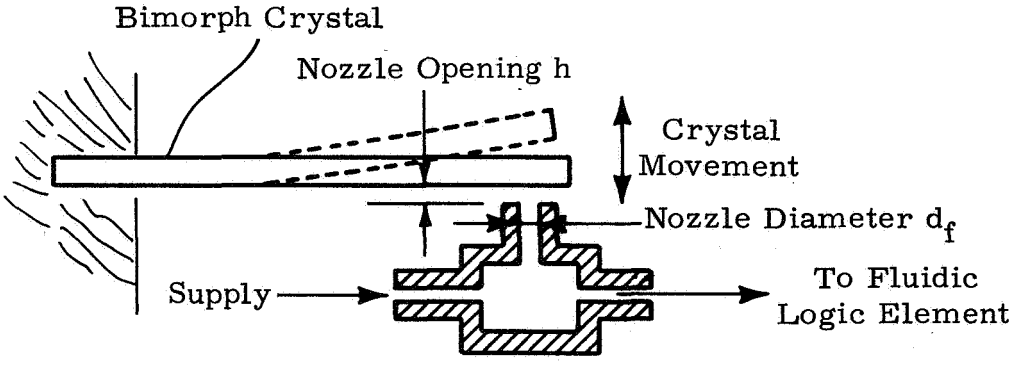


Figure 21. Flapper Valve Schematic

q = flow, cc/min

x = flapper displacement

The analysis indicates that a displacement of 2.80×10^{-2} cm could be obtained, theoretically, with a 100 volt signal across a crystal 0.1 meter in length and 0.001 meter thick. This displacement is theoretically sufficient to obtain a pneumatic signal powerful enough to switch a miniature fluidic gate.

Piezoelectric crystals were obtained from the Piezoelectric Division of the Clevite Corporation in Beford, Ohio. These bimorph crystals are made from a material designated PZT5B which is a combination of lead zirconate-lead titanate ceramics. The crystals measure 1.25 inch long by 0.25 inch wide and have a cross-section 0.024 inch thick. The Clevite part number for these crystals is 60359.

Bimorph piezoelectric crystals consist of two crystal plates secured together in such a manner that the applied voltage causes the two plates to deform in opposite directions, resulting in a twisting or bending action.

Since the crystals are of the bimorph type they are used in a flapper valve type configuration, as shown schematically in Figure 21. In this configuration the supply flow enters a cavity which has two outlets. One outlet is connected to the control port of a miniature fluidic element; the second outlet port is formed by the piezoelectric crystal which covers a nozzle. Movement of the flapper in the direction indicated in Figure 21 will change the nozzle opening and the impedance seen by the nozzle output flow. This change in impedance will change the pressure inside the cavity which is also the pressure seen by the control port of the fluidic logic element.

Obviously, the efficiency of the flapper valve will diminish when the nozzle itself, rather than the flapper, restricts the output flow from the cavity.

Thus

$$A_F < A_N \tag{16}$$

where:

A_F = flapper valve area in inches

A_N = nozzle cross sectional area in inches

$$A_F = \pi d_j h \tag{17}$$

where:

d_j = nozzle diameter in inches

h = distance from tip of nozzle to flapper

$$A_N = \frac{\pi d_j^2}{4} \tag{18}$$

Substitution of (17) and (18) into Equation (16)

$$\pi d_j h < \frac{\pi d_j^2}{4}$$

$$h < 1/4\ d_j \text{ or } h_{max} = 1/4\ d_j$$

For optimum impedance matching, the average flapper valve impedance should be equal to the impedance associated with the fluidic element. Since both the fluidic element control port and the flapper valve have the same inlet pressure, the impedances of these orifices are proportional to the orifice area, thus

$$A_{FA} = A_C. \tag{19}$$

where

A_{FA} = average flapper valve area in inches

A_C = control port area of fluidic element.

Assuming that for the flapper valve the average orifice area is equal to one-half the maximum area

$$A_{FA} = 1/2\ A_{F\,max} \tag{20}$$

$$\therefore A_C = 1/2\ A_{F\,max} = 1/2\ \pi d_j h_{max} \tag{21}$$

$$= 1/2\ \pi d_j (1/4\ d_j)$$

The control port area of a standard miniature fluidic element is 36×10^{-6} in^2, thus,

$$\frac{\pi}{8} d_j^2 = 36 \times 10^{-6}$$

$$d_j = 9.6 \times 10^{-3} \text{ inch}$$

Impedance considerations also govern the supply orifice area selection. A good match may be obtained by making the supply orifice area equal to the element control port area.

$$A_s = \frac{\pi}{4} d_s^2 = 36 \times 10^{-6} \tag{22}$$

where

A_s = supply orifice area in square inches

d_s = supply orifice diameter in inches

$d_s = 7 \times 10^{-3}$ inch.

The expected displacement of the piezoelectric flapper can be calculated by considering the equivalent circuit as shown in Figure 22. This illustration depicts the coupling obtained between the electrical and mechanical parameters which govern the action of the device. The following units are used in the equivalent circuit:

C_e = capacitance in farads

N = electromechanical gain in coulombs per meter

C_m = mechanical compliance in meters per ton

M = effective mass in kg.

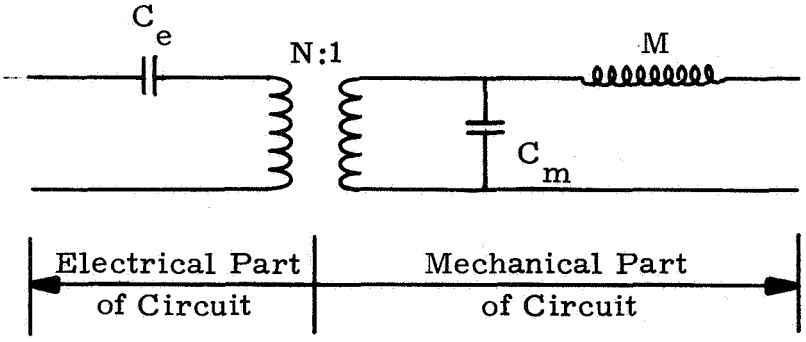


Figure 22. Equivalent Circuit

For parallel operation of the crystal structure the crystals used for the interface (PZT5B) exhibit the following properties:

$$C_e = 2000 \frac{LW}{T} \text{ pF} \quad (23)$$

$$N = 0.3 \frac{L}{WT} \text{ meters/coulomb} \quad (24)$$

$$C_m = 2.8 \times 10^{-9} \frac{L^3}{WT^3} \text{ meters/newton} \quad (25)$$

$$M = 0.033 \text{ LWT kg.} \quad (26)$$

L, W, and T are crystal length, width and thickness, in inches.

For a device driven at nonresonant frequencies with negligible load, the displacement is

$$\Delta h = QN. \quad (27)$$

where

Q = charge

$Q = VC_e$

V = potential in volts

For a 20 volt signal on the experimental crystals

$$Q = 20\, C_e = 20 \times 2000 \frac{LW}{T} = 4 \times 10^{-7} \text{ coulombs}$$

$$N = 0.3 \frac{L}{WT} = 24 \text{ meters/coulomb}$$

$$\Delta h = 24 \times 4 \times 10^{-7} = 100 \times 10^{-7} \text{ meters (0.0004 inch)}$$

The change in orifice area of the flapper valve obtained with this displacement is

$$\pi \Delta h d_j = \pi \times 4 \times 10^{-4} \times 9.6 \times 10^{-3} = 135 \times 10^{-7} \text{ inch}^2. \quad (28)$$

This amounts to approximately 16 percent of the average flapper orifice area, which is sufficient to obtain a pressure change in the cavity to switch the fluidic element.

Figure 23 shows schematically the design of the first experimental piezoelectric interface device built. A base plate provided the gas supply and output ports. The nozzle was etched from copper laminates. The etching process was chosen for fabrication of the nozzle because of the ease of manufacturing small, close tolerance, orifices. The piezoelectric crystal was clamped onto the base

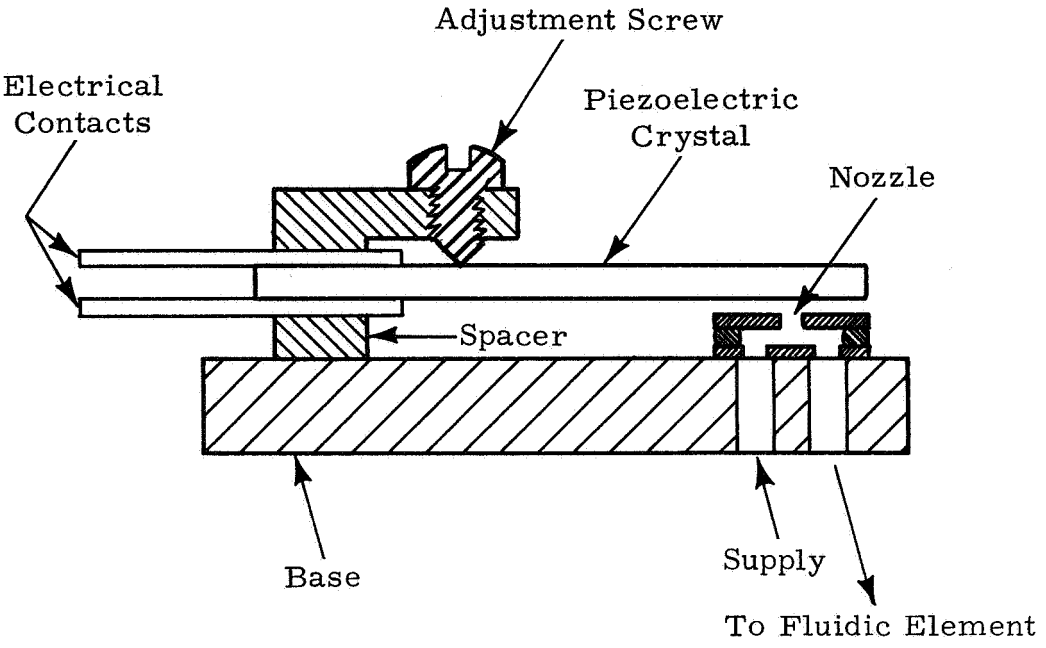


Figure 23. Schematic of E to F Interface

and positioned at approximately the required distance from the nozzle with a spacer. The final adjustment of this distance was done with an adjustment screw.

Figure 24 shows test results obtained with the device. Pressure changes in the cavity feeding the fluidic element control port were of sufficient magnitude to switch the fluidic element when a 25 volt ac signal was imposed upon the crystal.

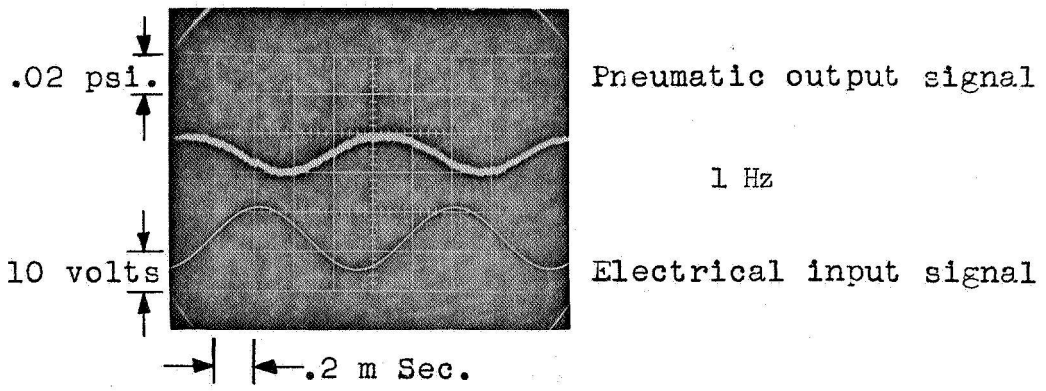
Figure 24 shows the electrical input wave form and the pneumatic output signal wave form at various frequencies. The highest frequency at which the device was tested was 1200 Hz for two reasons:

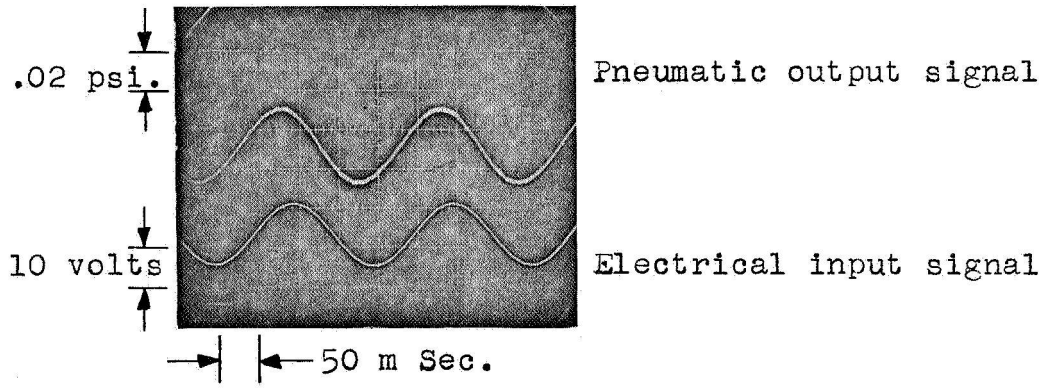
1 The particular low frequency signal generator used in the test was at the end of its range and,

2 Higher frequencies will certainly not be seen in this particular application. In fact, satisfactory performance at frequencies up to about 50 Hz will suffice.

The design goal for the electro-to-fluid interface was to obtain a pneumatic output of sufficient magnitude to switch a fluidic element with a 20 volt signal of 15 msec duration. Since the first unit performed satisfactorily only with signal levels higher than 25 volts, a more efficient design was necessary.

Output Pressure of Piezoelectrical Interface





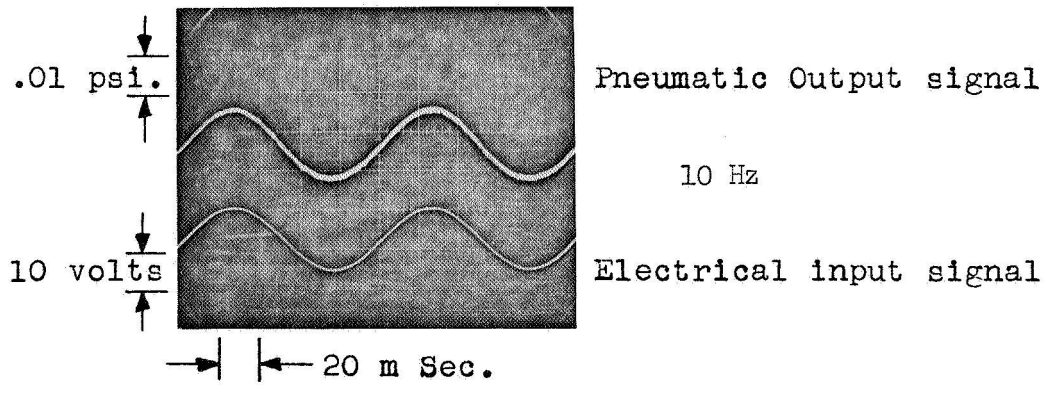
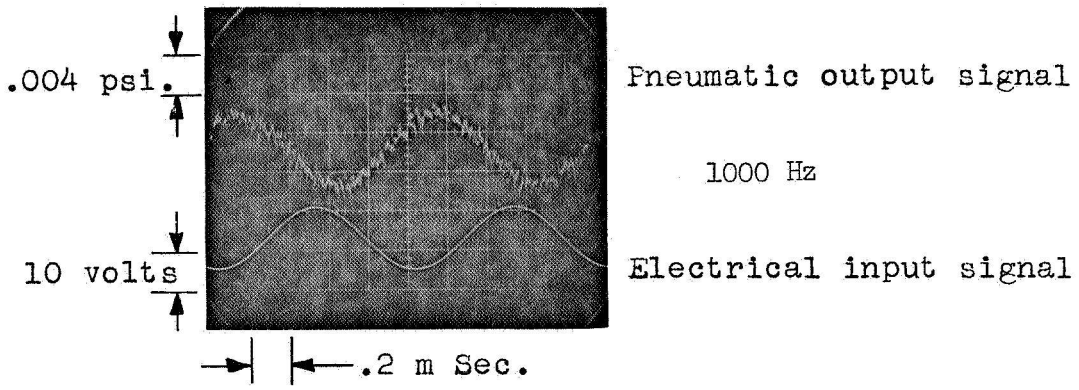
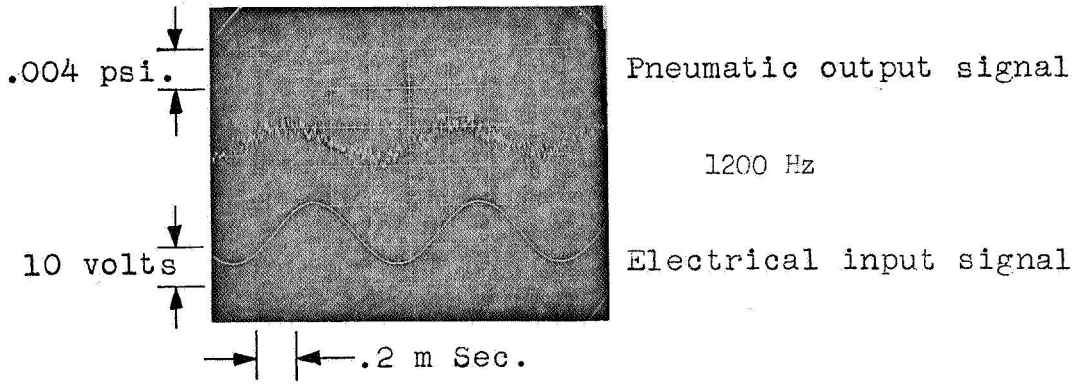
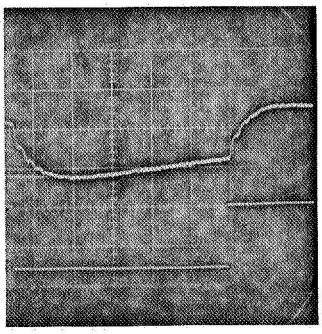


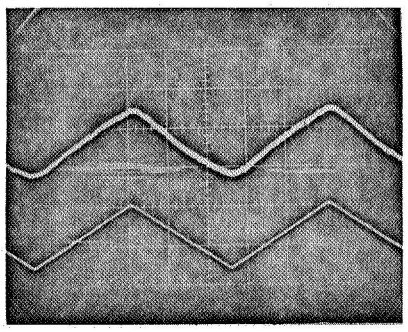
Figure 24. Input/Output Wave Forms





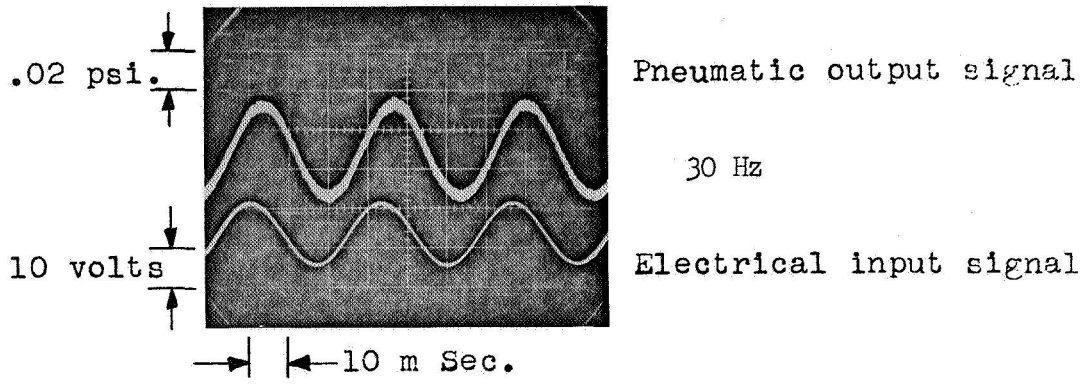


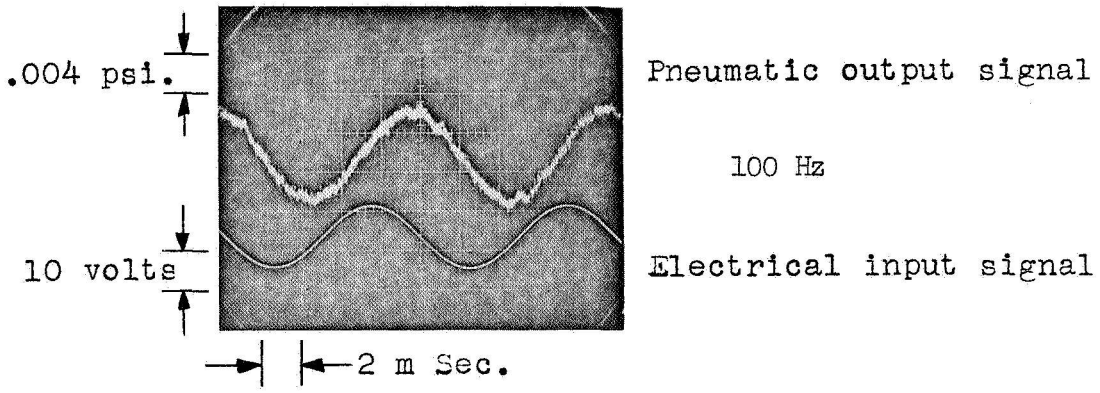
10 Hz
Square Wave



10 Hz
Triangular Wave

Figure 24. (Cont)





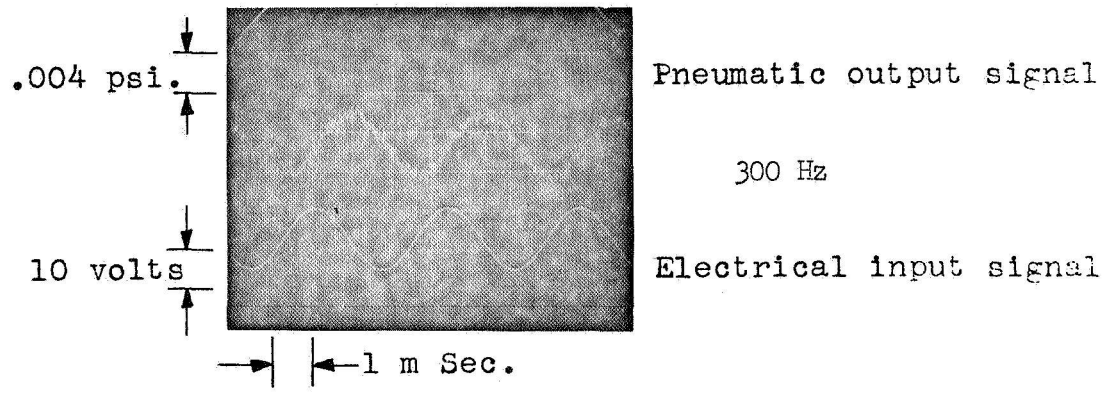


Figure 24. (Cont)

Obviously, the amount of flexure obtainable with the design shown in Figure 23 is limited by the position of the adjustment screw. In the design shown, the screw limits the effective length of the piezoelectric crystals. The bending action will take place with the adjustment screw as a pivot point. A more effective design is shown in Figure 25. In this device, the nozzle is part of a flexible strip of metal. The metal strip has an internal channel which forms the cavity used in the previous design. The adjustment screw now regulates the position of the nozzle with respect to the flapper. This way, the maximum usable length of the piezoelectric flapper is utilized.

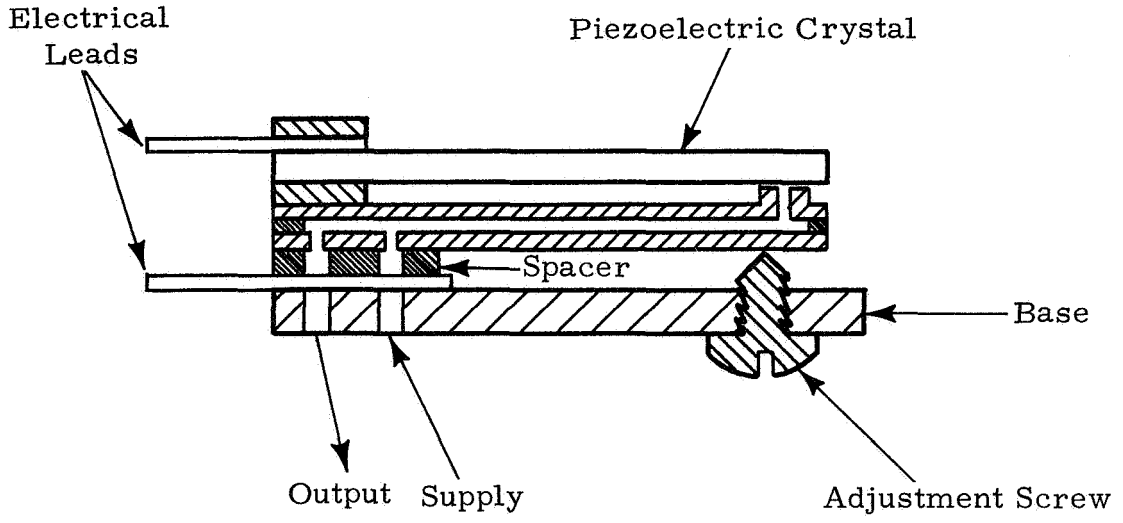
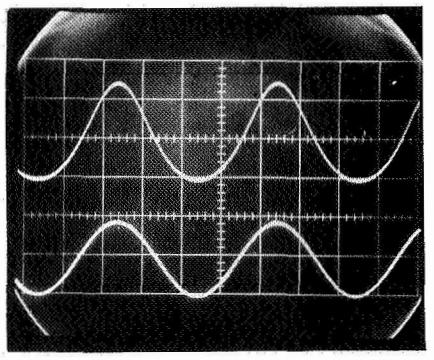


Figure 25. Design of E to F Interface

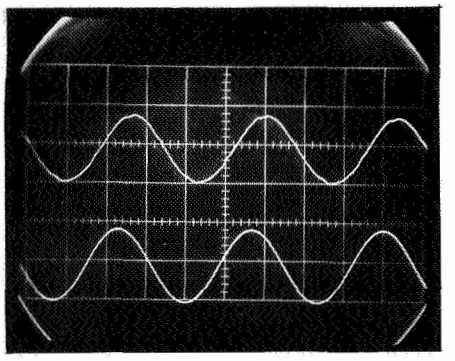
Test results obtained with this device are shown in Figure 26, which shows response at frequencies up to 300 Hz to an input sine wave. The input signal was 20 volts peak-to-peak. The output signal was measured with a pressure transducer. Figure 27 is a plot of signal attenuation and phase shifts versus frequency obtained from the test data shown in Figure 26. The response curve shows a typical first order break at around 16 Hz. Subsequent testing of the pressure transducer together with pneumatic lines used to connect the output of the interface device with this transducer indicates that the first order break is caused by the transducer setup and not by the interface device. When the effects of the pressure transducer response are eliminated from Figure 27, the curve representing the response of the electro-to-fluid interface is flat to at least 300 Hz.



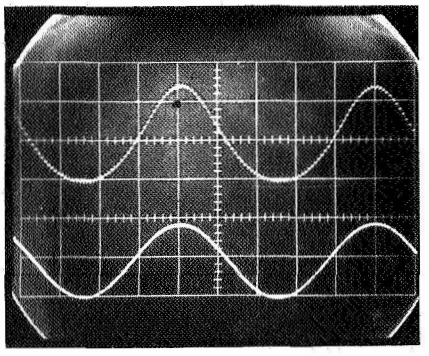
Pneumatic Output

Electrical Input

0.5 Hz



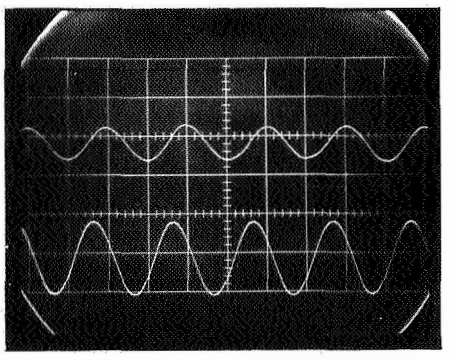
30 Hz



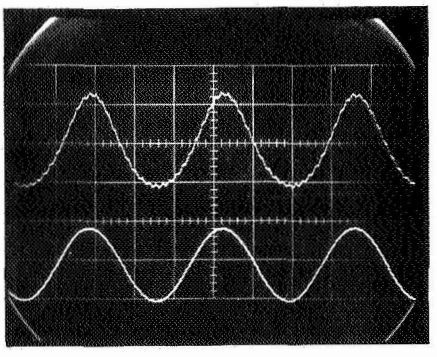
Pneumatic Output

Electrical Input

1.0 Hz



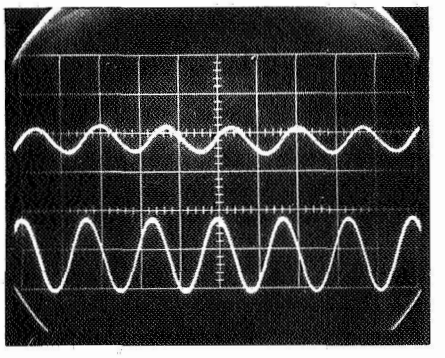
100 Hz



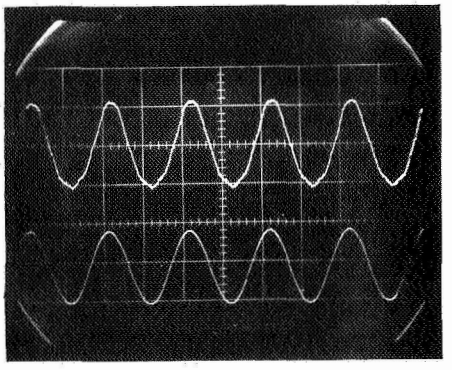
Pneumatic Output

Electrical Input

3.0 Hz



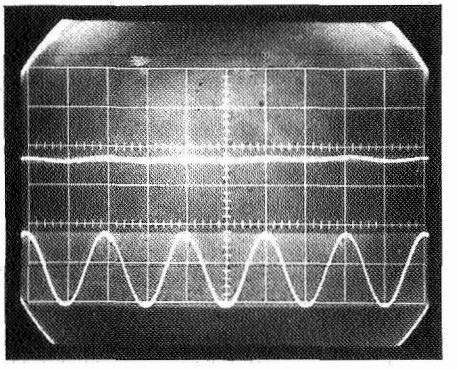
300 Hz



Pneumatic Output

Electrical Input

10 Hz



1000 Hz

Figure 26. Wave Forms E to F Interface

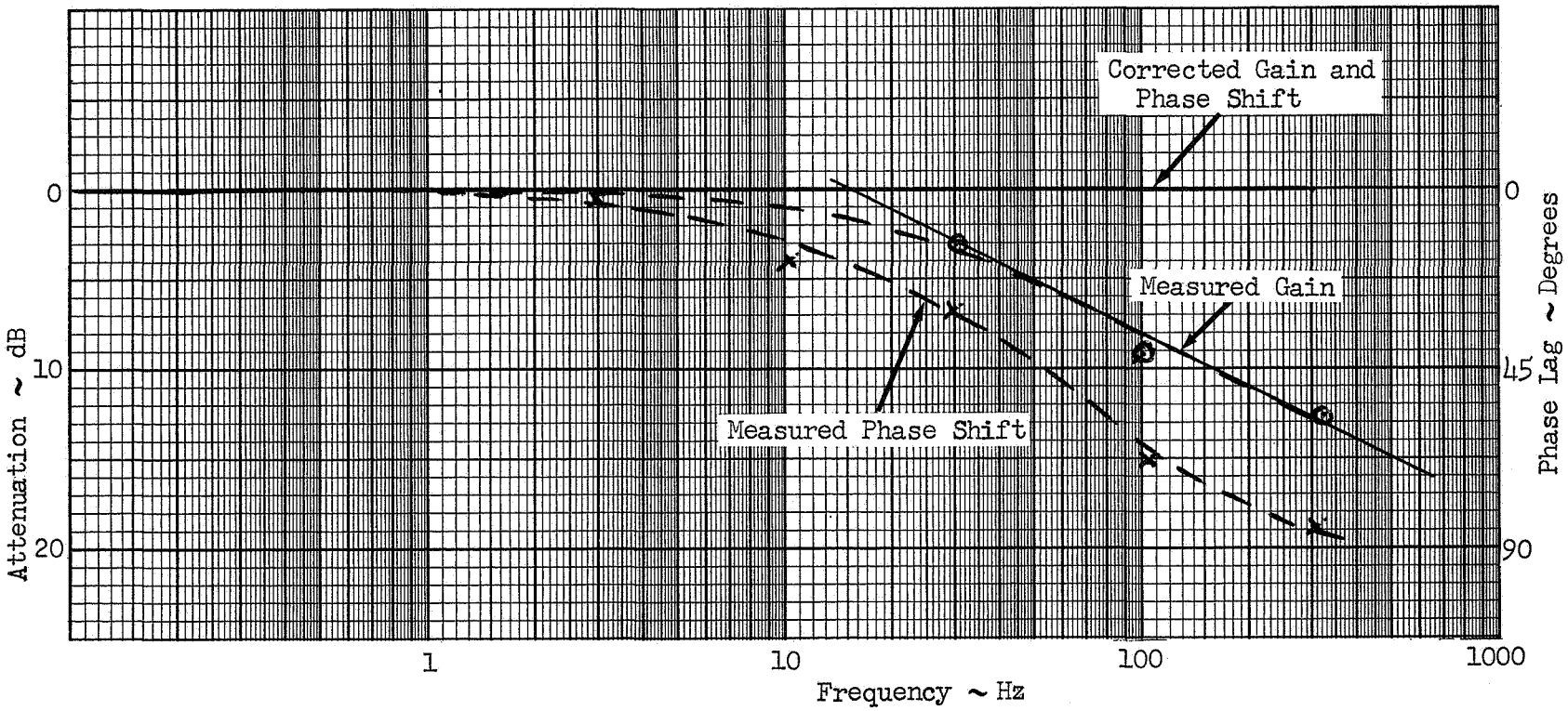


Figure 27. Frequency Response Crystal Interface

Tests performed to obtain information on the minimum driving voltage which still generates a powerful enough signal to drive a miniature fluidic element indicate that a 15V signal is sufficient. This is well within the limits of 20V set as a design goal. Of the two units actually built according to the new design, one unit actually was capable of driving a fluidic element with a 10 volt signal. The second unit did not generate sufficient power at 15 volts, due to a possible difference in crystal structures (the experimental crystals were obtained as samples) or a difference in orifice sizes of the nozzles, which may account for some mismatch in impedance.

The experimental test set up is illustrated in Figure 28. This illustration shows the crystal-type interface and a fluidic element connected with a hose connection. Test results are recorded in Figures 26 and 27.

A compact integrated circuit electro-to-fluid interface device was built in order to eliminate the hose connections between the crystal-type interface flapper valve and the fluidic amplifier. This integrated device is shown in Figure 29. Care was taken to maintain the identical fluidic element configuration in both the nonintegrated and the integrated package.

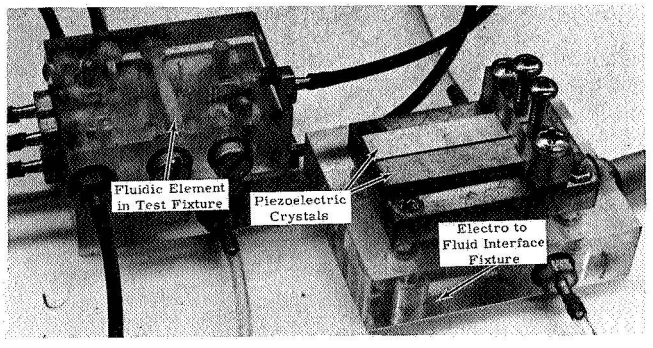


Figure 28. Experimental Crystal Interface

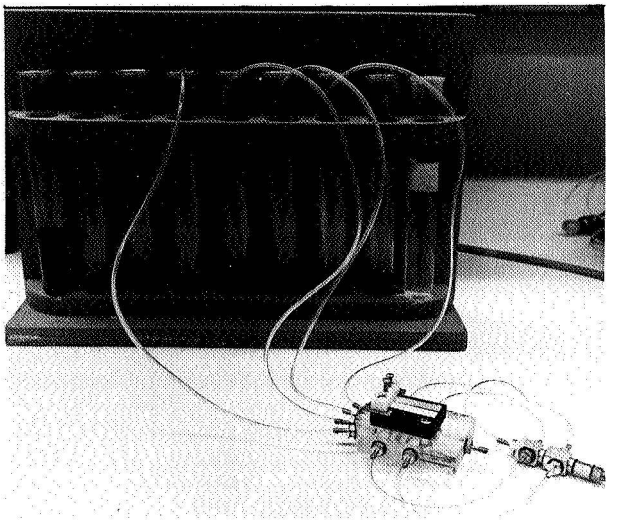


Figure 29. Integrated Interface Test

Test results obtained with the integrated designs indicated that somewhat higher input signal levels were required to operate the device. Reliable operation could only be obtained with voltage levels of approximately 50 volts coupled with careful selection of the fluidic elements driver by the electro-to-fluid interfaces. The difference in operating level is believed to be caused by pneumatic resonance of the signals which enhance the signal strength in the non-integrated package.

Attempts to obtain the same resonance signal amplification in the integrated package failed. Due to the fact that the resonant lines when built into the integrated package will have more pneumatic resistance (affected by the smaller size), the signal amplification obtained through the resonance phenomena is nullified by the added resistance to be overcome.

Two possible solutions for the reduction of the necessary electrical input signal levels are:

1 Increase the sensitivity of the fluidic elements.

2 Increase the size of the bimorph piezoelectric crystal.

Fluidic elements with higher sensitivities than those obtained with standard Martin Marietta 0.004 inch elements are presently under investigation. However, no firm results can be reported at this date since the investigation of the high sensitivity elements are not completed as yet.

The second solution required crystals of approximately 2 inches in length for signal levels of 20 volts. A two inch long crystal is too large for this application and consequently will not be considered as a suitable unit at this time.

Decoder Logic Modules

Logic Design. - The decoder logic module transforms the binary information into corresponding signals to the readout.

The readout, the signal processing, and the relationships between the displayed number, the binary four bit information from the computer, and the sections of the display panel are described in Section II of this report.

A fluidic logic circuit converts this information. From Table III, in Section II, the Boolean relationships of the computer information and the panel activation are established. For example, panel section A will be activated when the numbers 0, 2, 3, 5, 6, 7, 8, and 9 are displayed. The Boolean expression for A is:

$$A = \overline{V}\,\overline{W}\,\overline{X}\,\overline{Y} + \overline{V}\,\overline{W}\,X\,\overline{Y} + \overline{V}\,\overline{W}\,X\,Y + \overline{V}\,W\,\overline{X}\,Y$$
$$+ \overline{V}\,X\,Y\,Z + V\,\overline{X}\,\overline{Y}\,\overline{Z} + V\,\overline{X}\,\overline{Y}\,Z + \overline{V}\,W\,X\,\overline{Y}$$

where V represents a one or "on" signal in bit V and $\overline{V}$ is a zero in this channel. Considerable redundancy is still present in this expression. Eliminating these redundancies through conventional methods of logic design will result in the minimum expression:

$$A = X + V + \overline{W}\,\overline{Y} + W\,Y$$

The following expressions are similarly obtained for the remaining parts of the display unit:

$$B = \overline{X}\,\overline{Y} + V + W\,\overline{X} + W\,\overline{Y}$$
$$C = \overline{W} + \overline{X}\,\overline{Y} + X\,Y$$
$$D = V + W\,\overline{X} + X\,\overline{Y} + \overline{W}\,X$$
$$E = \overline{W}\,\overline{Y} + X\,\overline{Y}$$
$$F = \overline{X} + W + Y$$
$$G = \overline{W}\,\overline{Y} + \overline{W}\,X + X\,\overline{Y} + W\,\overline{X}\,Y$$

Figure 30 shows a possible logic implementation of the display logic module. The binary input signals V W X and Y activate logic gates of the display logic module. The output gates A through G provide the signals to the panel section of the display modules to be activated. The logic functions in the decoder logic module are performed by fluidic OR-NOR logic elements. Figure 10 shows a typical NOR logic element.

When an input signal appears at the control port, the NOR output is off and is denoted by a zero (0). When the input signal is removed from the control port, the NOR output is on and denoted by a one (1).

The OR output in our application of the gate is not used and is therefore vented to atmosphere. The NOR output signal is used exclusively throughout the display logic module. A more reliable performance can be obtained this way.

During an investigation of the performance of a prototype of the actual logic elements to be used in the logic module it became obvious that the logic gates could reliably be used at lower input power levels, providing that certain multiple type fan-out circuitry could be avoided. In order to capitalize on this possibility of using lower supply pressures for the logic module, and thus reducing

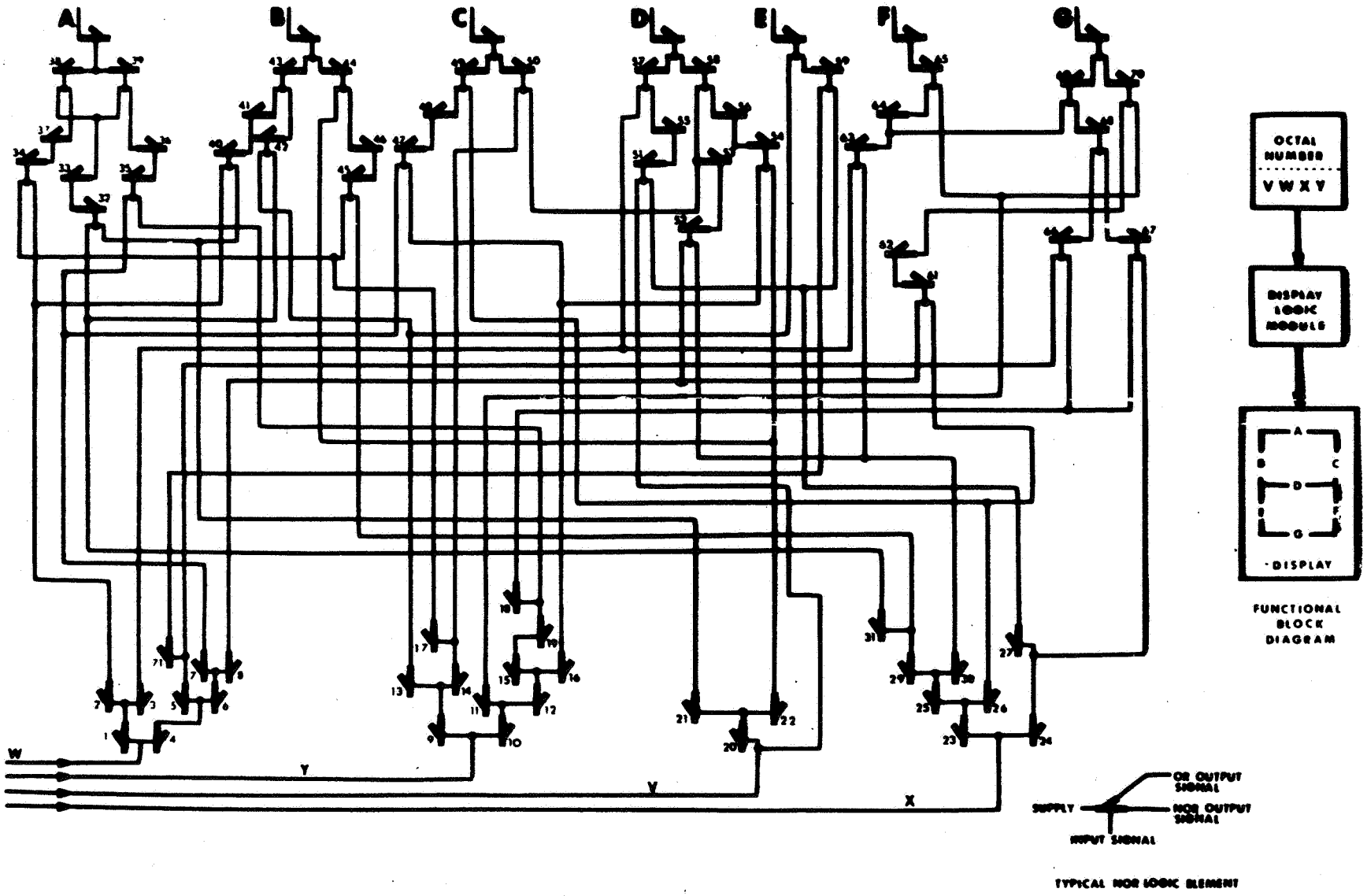


Figure 30. Schematic of Display Logic Module

the amount of pneumatic power necessary to drive the decoder, the logic design was revised to eliminate these multiple fan-out circuits. The revised logic diagram is shown in Figure 11. Each gate in the logic diagram has been assigned a number, 1 through 78, and the output gates to the panel sections are lettered A through G.

Table IV shows the Boolean representation of the input signal to each of the logic gates shown in Figure 31. The logic diagram shown in Figure 31 has been checked out by means of a "truth" table (Table V). The table shows the output state of each logic gate in the logic diagram for each of the 16 possible combinations of inputs. Several of the inputs will not be used since out of the 16 possible input combinations only 10 combinations (0 through 9) are meaningful.

The demonstration model which will decode the binary information into an octal display will use the numbers 0 through 7 only. However, the logic design has been executed with binary to octal as well as binary to decimal decoding in mind. If so desired at a later date the complete decoder logic module as presently designed can be used for both decoding schemes.

Logic Element Specifications. - The logic modules, of which five are required for the display model, are shown schematically in Figure 31. Each contains 85 logic gates. The display logic module was built as a laminar construction, in alternate layers of laminates containing logic elements and laminates containing the interconnecting channels.

A test program was conducted to determine the performance characteristics of the logic gates. These performance tests show fan-in and fan-out capabilities of the individual gates. Performance characteristics are shown in Figure 32.

This figure illustrates the relationship between output flow and output pressure from a logic gate and input pressure and input flow into the control port of the logic gate. The switching zone denotes the limits of the control signal pressure at which the logic gate switches from one state to the other.

Figure 33 shows the relationship of back pressure and flow into a logic gate when the gate is turned off. Figure 34 shows the various possibilities of logic gate interaction which can be found in the logic diagram, Figure 31. Figure 32 shows the matching of the flow and pressure from the output port of one logic gate into the control port of another gate. This hookup is schematically shown in Figure 34a. The point where the two curves cross in Figure 32 is the operating point of this particular hookup, since at that point the pressure output from one gate equals the input from the next gate and also the output flow from one gate is equal to the input flow into the next gate. Obviously, the pressure found at the crossover point should be higher than the switching zone pressure in order to ensure that proper switching of the downstream gate is accomplished. Similarly, Figure 35 shows the matching of the circuit shown in Figure 34b.

TABLE IV

BOOLEAN REPRESENTATION OF INPUT SIGNALS

Gate	Output Signal	Gate	Output Signal	Gate	Output Signal
1	$\overline{W}$	27	$\overline{X}$	53	$\overline{W} + \overline{X}$
2	W	28	X	54	$Y\,\overline{V}$
3	$\overline{W}$	29	$\overline{X}$	55	$\overline{V} + X$
4	W	30	X	56	$\overline{Y} + V$
5	$\overline{W}$	31	$\overline{X}$	57	$\overline{W}\,\overline{X}\,\overline{V} + \overline{W}\,\overline{X}\,Y\,\overline{V}$
6	W	32	$\overline{X}\,\overline{V}$	58	$W\,X\,Y\,\overline{V}$
7	$\overline{W}$	33	$X + V$	59	$W\,\overline{X}$
8	W	34	$\overline{W}\,Y$	60	X
9	$\overline{W}$	35	$W\,\overline{Y}$	61	$W\,\overline{X}$
10	$\overline{Y}$	36	$\overline{W} + Y$	62	$\overline{W} + X$
11	Y	37	$W + \overline{Y}$	63	$\overline{W}\,X$
12	$\overline{Y}$	38	$W\,X\,Y\,\overline{V}$	64	$W + \overline{X}$
13	Y	39	$W\,\overline{X}\,Y\,\overline{V}$	65	$X\,\overline{W}\,\overline{Y}$
14	$\overline{Y}$	40	$W\,\overline{V}$	66	$\overline{W}\,Y$
15	Y	41	$W + V$	67	$X\,Y$
16	$\overline{Y}$	42	$\overline{X}\,\overline{Y}$	68	$W\,\overline{X} + Y$
17	Y	43	$\overline{W}\,X\,\overline{V} + \overline{W}\,Y\,\overline{V}$	69	$W\,X\,Y + \overline{W}\,\overline{X}\,Y$
18	$\overline{Y}$	44	$W\,X\,Y\,\overline{V} + X\,Y\,\overline{V}$	70	$W\,\overline{X}\,\overline{Y}$
19	Y	45	$X\,Y$	71	$\overline{X}$
20	$\overline{Y}$	46	$\overline{X} + \overline{Y}$	72	$X + V$
21	$\overline{V}$	47	$W\,Y$	73	$\overline{W} + \overline{X}$
22	V	48	$\overline{W} + \overline{Y}$	74	$W + \overline{X}$
23	V	49	$W\,Y\,\overline{X}$	75	$\overline{W}\,X$
24	$\overline{V}$	50	$W\,X\,\overline{Y}$	76	X
25	V	51	$\overline{V}\,\overline{X}$	77	$\overline{X}$
26	V	52	$W\,X$	78	X

Gate	Output Signal	Gate	Output Signal
A	$X + V + \overline{W}\,\overline{Y} + W\,Y$	E	$\overline{W}\,\overline{Y} + X\,\overline{Y}$
B	$\overline{X}\,\overline{Y} + V + W\,\overline{X} + W\,\overline{Y}$	F	$\overline{X} + W + Y$
C	$\overline{W} + \overline{X}\,\overline{Y} + X\,Y$	G	$\overline{W}\,\overline{Y} + \overline{W}X + X\,\overline{Y} + W\,\overline{X}\,Y$
D	$V + W\,\overline{X} + X\,\overline{Y} + \overline{W}X$		

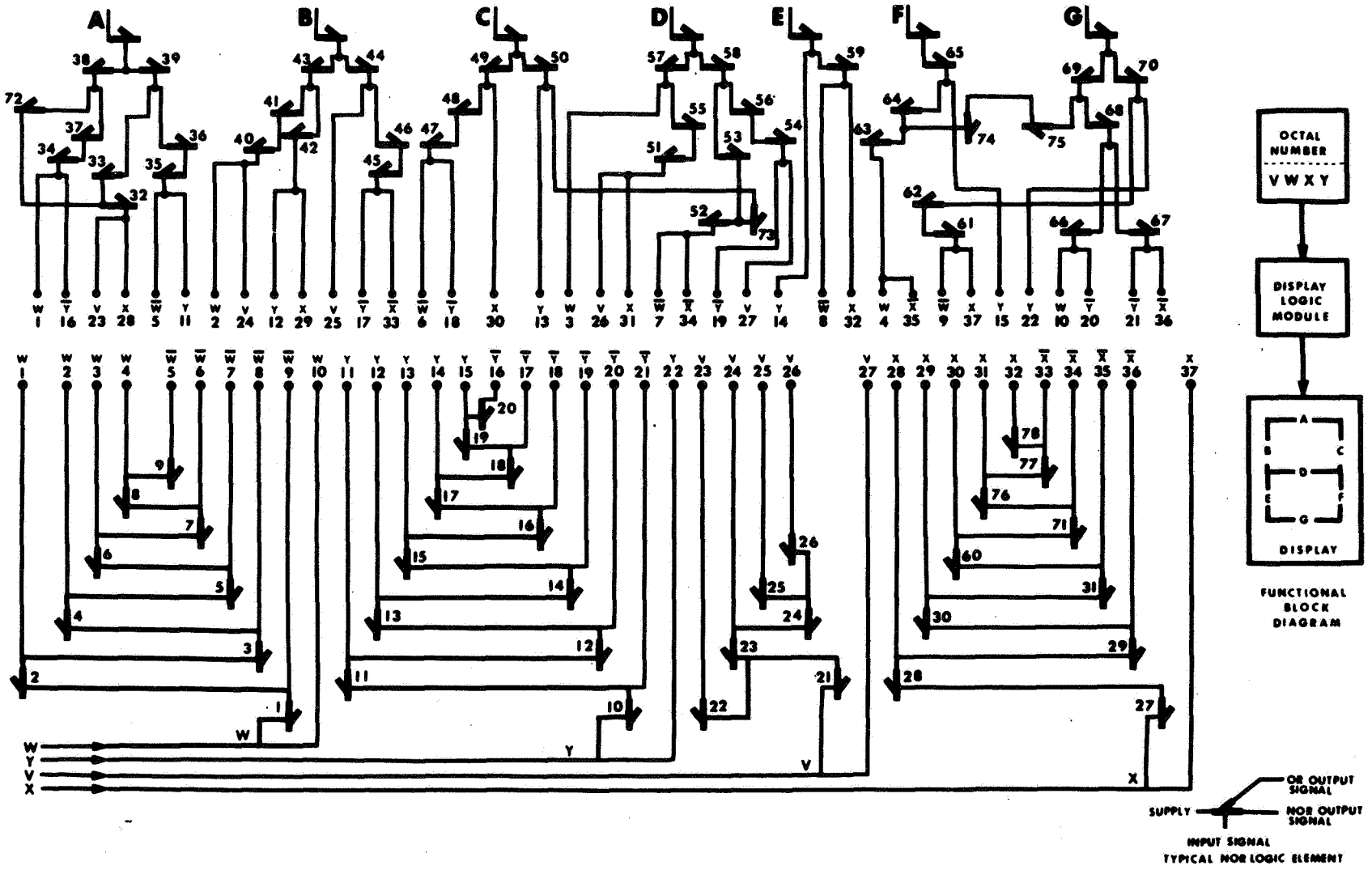


Figure 31. Schematic of Display Logic Module

TABLE V

TRUTH TABLE OF DISPLAY LOGIC MODULE

	Binary Input				Logic Gate Number Corresponding to Logic Diagram														
	W	X	Y	V	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
1	0	0	0	0	1	0	1	0	1	0	1	0	1	1	0	1	0	1	0
2	0	0	0	1	1	0	1	0	1	0	1	0	1	1	0	1	0	1	0
3	0	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
4	0	0	1	1	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
5	0	1	0	0	1	0	1	0	1	0	1	0	1	1	0	1	0	1	0
6	0	1	0	1	1	0	1	0	1	0	1	0	1	1	0	1	0	1	0
7	0	1	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
8	0	1	1	1	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
9	1	0	0	0	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0
10	1	0	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0
11	1	0	1	0	0	1	0	1	0	1	0	1	0	0	1	0	1	0	1
12	1	0	1	1	0	1	0	1	0	1	0	1	0	0	1	0	1	0	1
13	1	1	0	0	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0
14	1	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0
15	1	1	1	0	0	1	0	1	0	1	0	1	0	0	1	0	1	0	1
16	1	1	1	1	0	1	0	1	0	1	0	1	0	0	1	0	1	0	1
	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35
1	1	0	1	0	1	1	0	0	1	0	0	1	0	1	0	1	1	0	0	0
2	1	0	1	0	1	0	1	1	0	1	1	1	0	1	0	1	0	1	0	0
3	0	1	0	1	0	1	0	0	1	0	0	1	0	1	0	1	1	0	1	0
4	0	1	0	1	0	0	1	1	0	1	1	1	0	1	0	1	0	1	1	0
5	1	0	1	0	1	1	0	0	1	0	0	0	1	0	1	0	0	1	0	0
6	1	0	1	0	1	0	1	1	0	1	1	0	1	0	1	0	0	1	0	0
7	0	1	0	1	0	1	0	0	1	0	0	0	1	0	1	0	0	1	1	0
8	0	1	0	1	0	0	1	1	0	1	1	0	1	0	1	0	0	1	1	0
9	1	0	1	0	1	1	0	0	1	0	0	1	0	1	0	1	1	0	0	1
10	1	0	1	0	1	0	1	1	0	1	1	1	0	1	0	1	0	1	0	1
11	0	1	0	1	0	1	0	0	1	0	0	1	0	1	0	1	1	0	0	0
12	0	1	0	1	0	0	1	1	0	1	1	1	0	1	0	1	0	1	0	0
13	1	0	1	0	1	1	0	0	1	0	0	0	1	0	1	0	0	1	0	1
14	1	0	1	0	1	0	1	1	0	1	1	0	1	0	1	0	0	1	0	1
15	0	1	0	1	0	1	0	0	1	0	0	0	1	0	1	0	0	1	0	0
16	0	1	0	1	0	0	1	1	0	1	1	0	1	0	1	0	0	1	0	0

TABLE V (Cont)

	Binary Input				Logic Gate Number Corresponding to Logic Diagram															
	W	X	Y	V	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	
	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55
1	1	1	0	0	1	0	1	0	0	0	1	0	1	0	0	1	0	1	0	0
2	1	1	0	0	0	1	1	0	0	0	1	0	1	0	0	0	0	1	0	1
3	1	0	1	0	1	0	0	1	0	0	1	0	1	0	0	1	0	1	1	0
4	1	0	0	0	0	1	0	0	0	0	1	0	1	0	0	0	0	1	0	1
5	1	1	0	0	1	0	0	1	0	0	1	0	1	0	0	0	0	1	0	1
6	1	1	0	0	0	1	0	0	0	0	1	0	1	0	0	0	0	1	0	1
7	1	0	0	0	1	0	0	1	1	1	0	0	1	0	0	0	0	1	1	1
8	1	0	0	0	0	1	0	0	0	1	0	0	1	0	0	0	0	1	0	1
9	0	1	0	1	0	1	1	0	0	0	1	0	1	0	0	1	0	1	0	0
10	0	1	0	0	0	1	1	0	0	0	1	0	1	0	0	0	0	1	0	1
11	1	1	0	0	0	1	0	0	0	0	1	1	0	1	0	1	0	1	1	0
12	1	1	0	0	0	1	0	0	0	0	1	1	0	1	0	0	0	1	0	1
13	0	1	0	0	0	1	0	0	0	0	1	0	1	0	1	0	1	0	0	1
14	0	1	0	0	0	1	0	0	0	0	1	0	1	0	1	0	1	0	0	1
15	1	1	0	0	0	1	0	0	1	1	0	1	0	0	0	0	1	0	1	1
16	1	1	0	0	0	1	0	0	0	1	0	1	0	0	0	0	1	0	0	1
	56	57	58	59	60	61	62	63	64	65	66	67	68	69	70	71	72	73	74	75
1	1	1	0	0	0	0	1	0	1	0	0	0	1	0	0	1	0	1	1	0
2	1	0	0	0	0	0	1	0	1	0	0	0	1	0	0	1	1	1	1	0
3	0	1	0	0	0	0	1	0	1	0	1	0	0	1	0	1	0	1	1	0
4	1	0	0	0	0	0	1	0	1	0	1	0	0	1	0	1	1	1	1	0
5	1	0	0	0	1	0	1	1	0	1	0	0	1	0	0	0	1	1	0	1
6	1	0	0	0	1	0	1	1	0	1	0	0	1	0	0	0	1	1	0	1
7	0	0	0	0	1	0	1	1	0	0	1	1	0	0	0	0	1	1	0	1
8	1	0	0	0	1	0	1	1	0	0	1	1	0	0	0	0	1	1	0	1
9	1	0	0	1	0	1	0	0	1	0	0	0	1	0	1	1	0	1	1	0
10	1	0	0	1	0	1	0	0	1	0	0	0	1	0	1	1	1	1	1	0
11	0	0	0	1	0	1	0	0	1	0	0	0	1	0	0	1	0	1	1	0
12	1	0	0	1	0	1	0	0	1	0	0	0	1	0	0	1	1	1	1	0
13	1	0	0	0	1	0	1	0	1	0	0	0	1	0	0	0	1	0	1	0
14	1	0	0	0	1	0	1	0	1	0	0	0	1	0	0	0	1	0	1	0
15	0	0	1	0	1	0	1	0	1	0	0	1	0	1	0	0	1	0	1	0
16	1	0	0	0	1	0	1	0	1	0	0	1	0	1	0	0	1	0	1	0
	76	77	78		A	B	C	D	E	F	G									
1	0	1	0		1	1	1	0	1	1	1									
2	0	1	0		1	1	1	1	1	1	1									
3	0	1	0		0	0	1	0	0	1	0									
4	0	1	0		1	1	1	1	0	1	0									
5	1	0	1		1	0	1	1	1	0	1									
6	1	0	1		1	1	1	1	1	0	1									
7	1	0	1		1	0	1	1	0	1	1									
8	1	0	1		1	1	1	1	0	1	1									
9	0	1	0		0	1	1	1	0	1	0									
10	0	1	0		1	1	1	1	0	1	0									
11	0	1	0		1	1	0	1	0	1	1									
12	0	1	0		1	1	0	1	0	1	1									
13	1	0	1		1	1	0	1	1	1	1									
14	1	0	1		1	1	0	1	1	1	1									
15	1	0	1		1	0	1	0	0	1	0									
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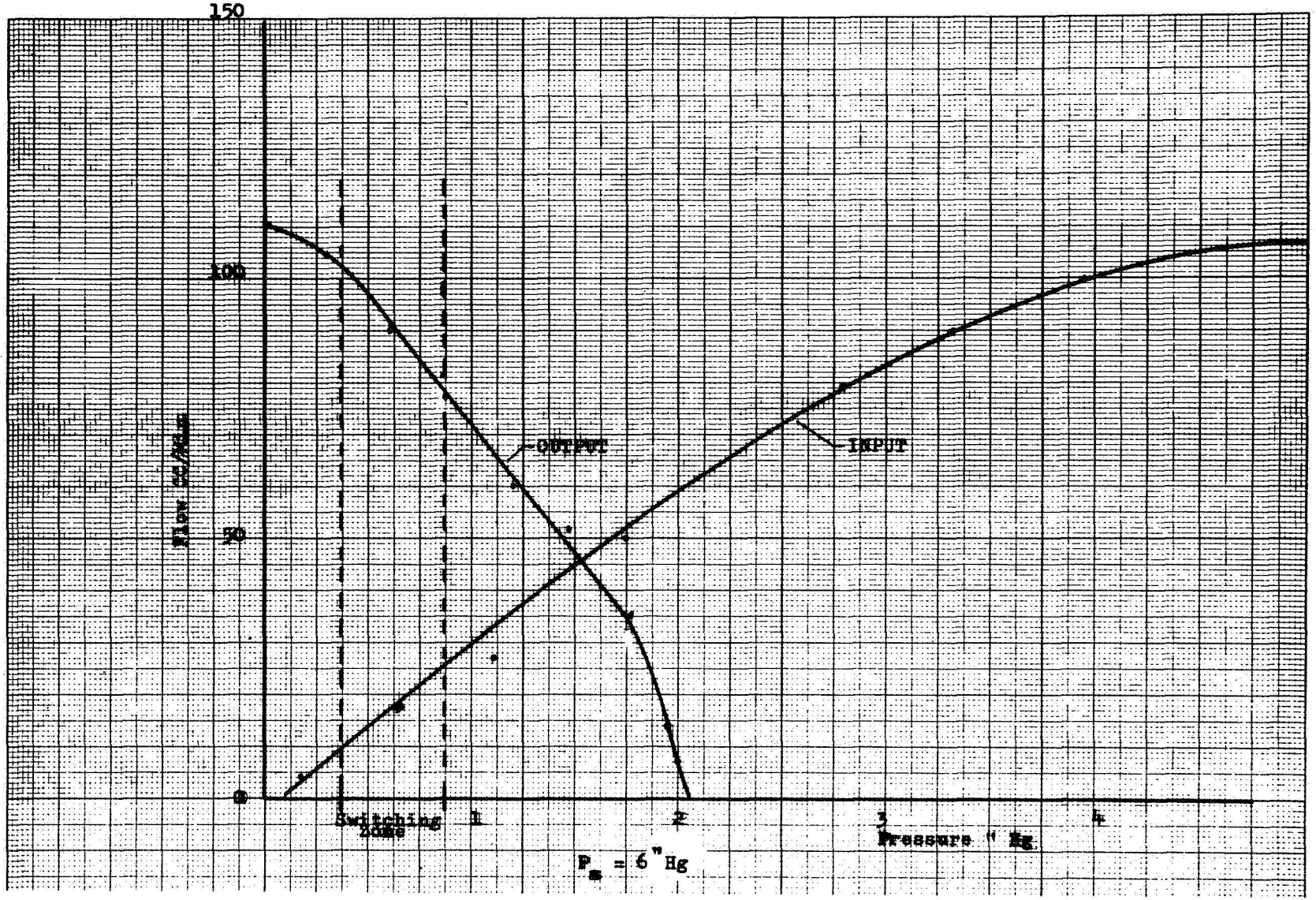

Figure 32. Performance Characteristics of Logic Gate

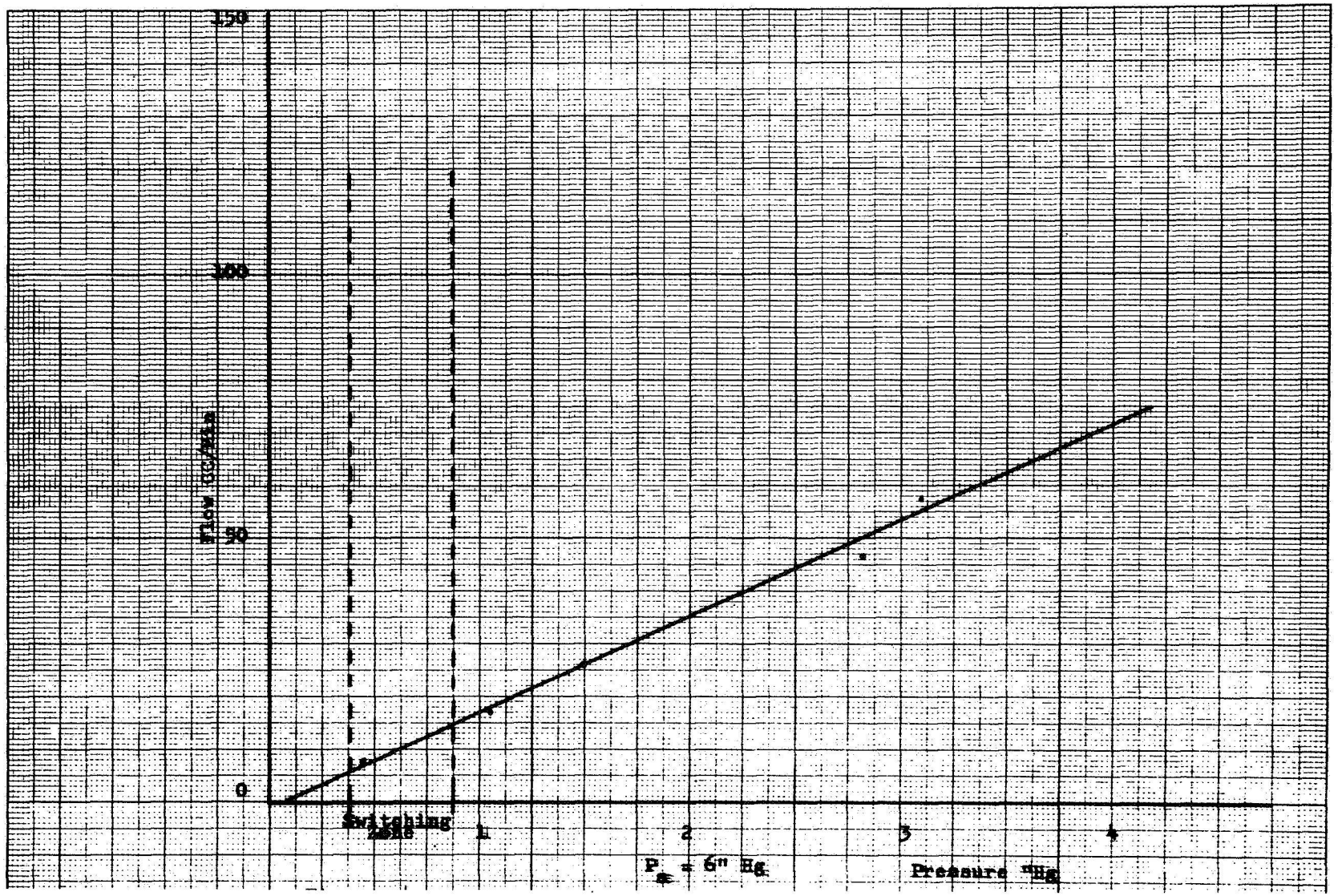

Figure 33. Back Pressure - Flow Relationship

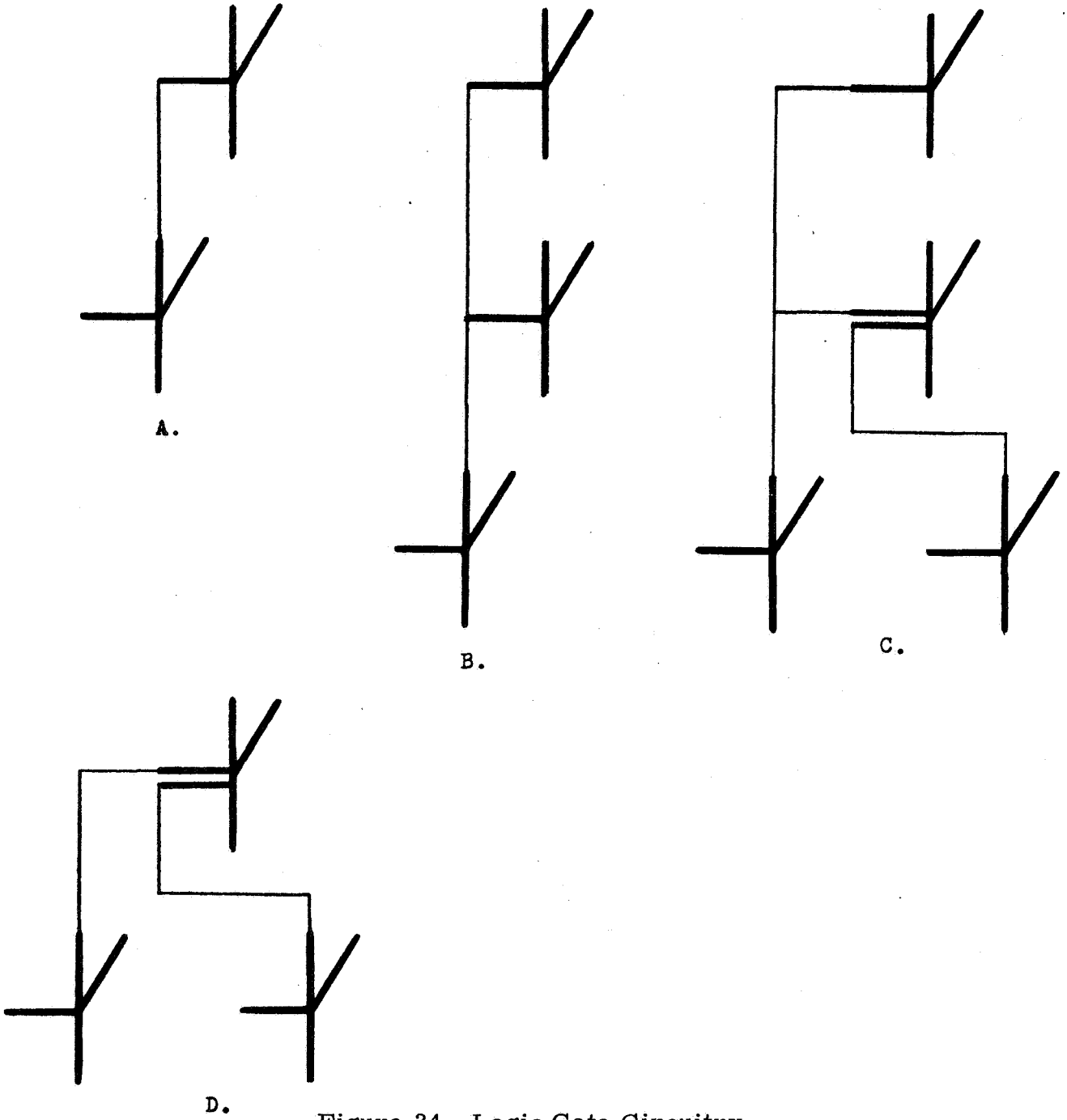

Figure 34. Logic Gate Circuitry

The input curve is obtained by multiplying all values of the input curve of Figure 32 by a factor of two. The output curve is identical to the curve shown in Figure 32. By adding the input flow pressure curve from Figure 35 to the back pressure curve of Figure 33, the circuit requirements for the circuit shown in Figure 34c can be investigated, as shown in Figure 36. Similarly, Figure 37 shows the matching of the circuitry of Figure 34d. All possible combinations shown have a crossover pressure higher than the maximum switching pressure, thus ensuring proper working of the circuit.

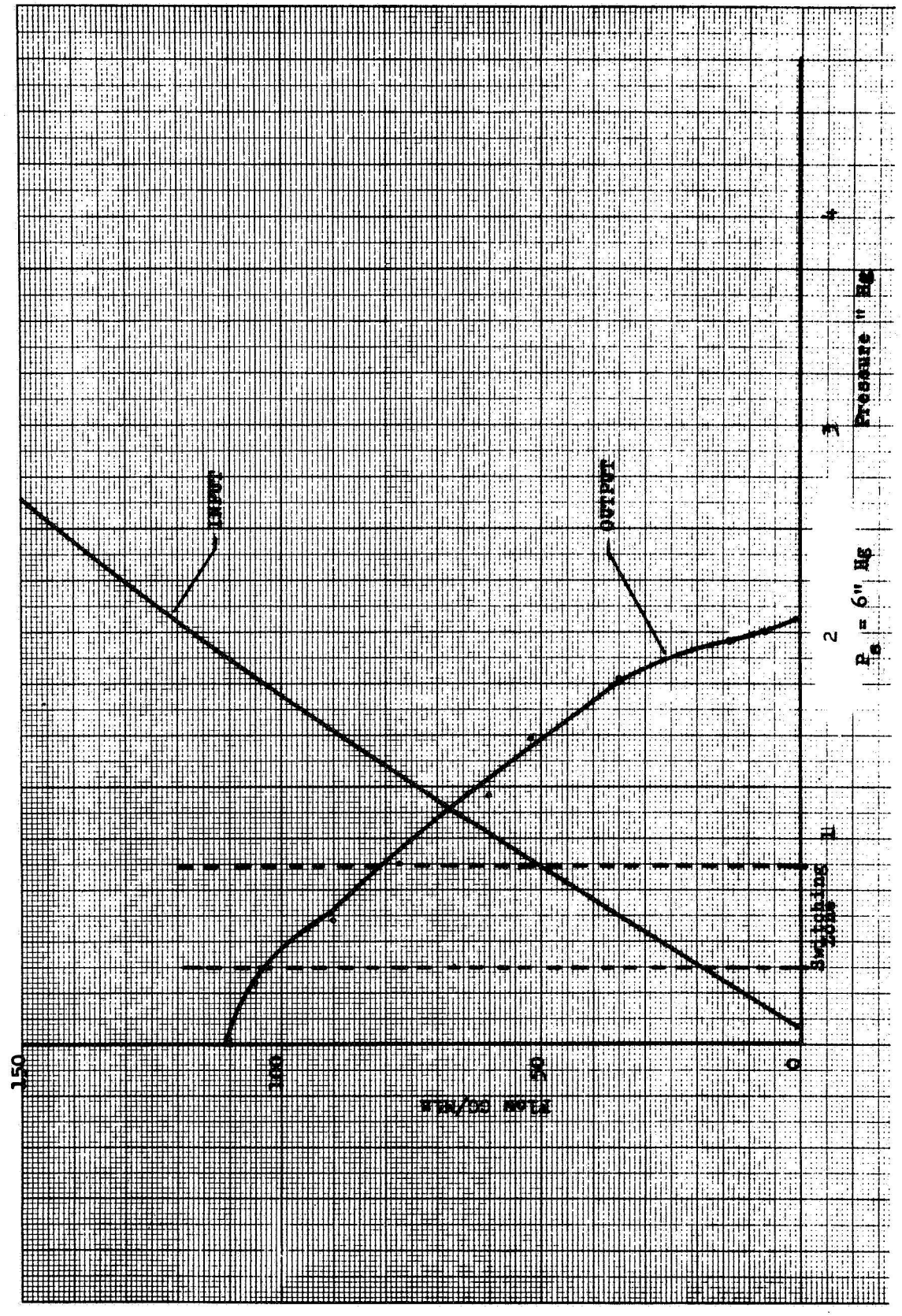

Figure 35. Fan-out Operating Characteristics

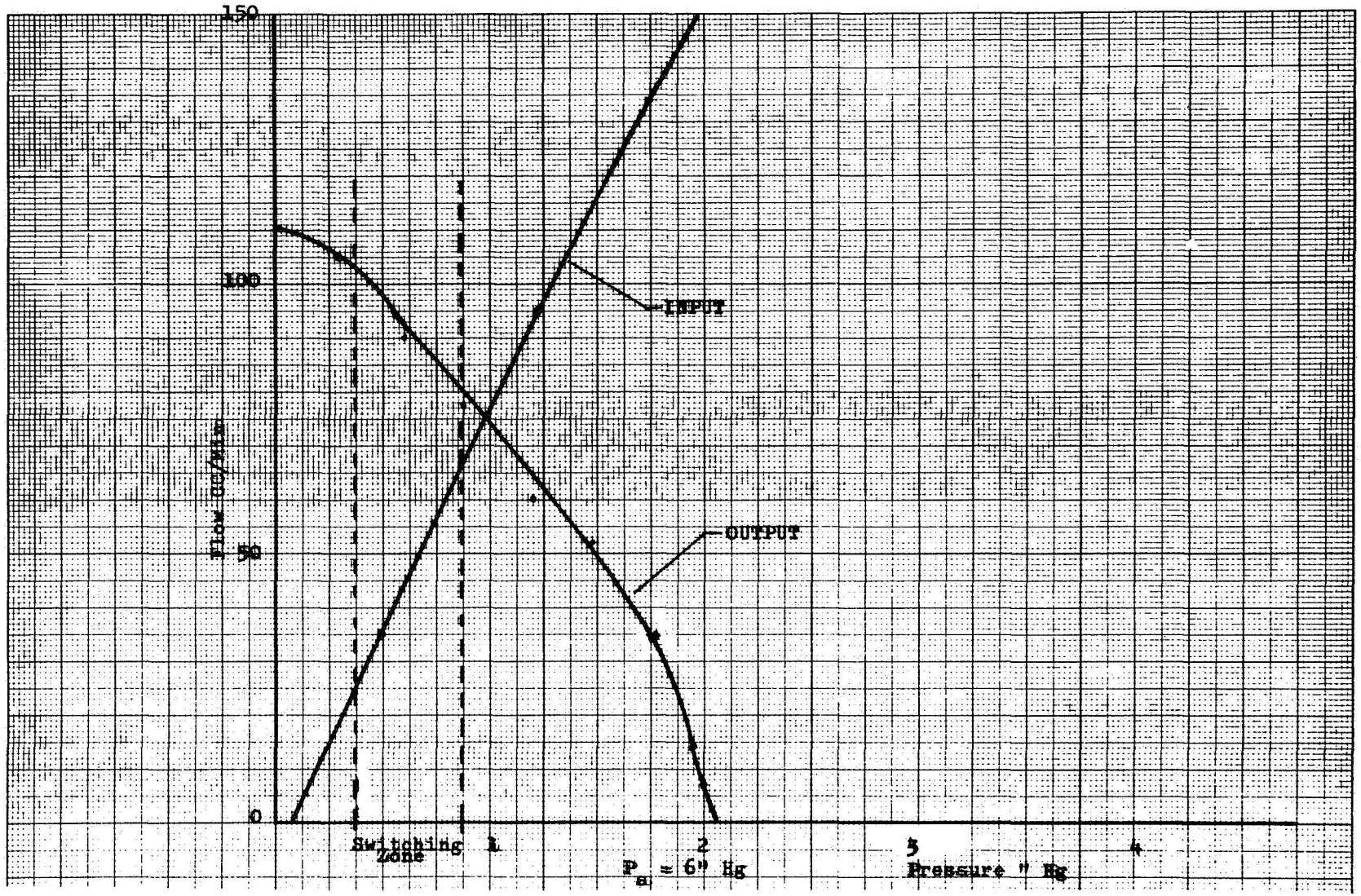

Figure 36. Fan-out Operating Characteristics

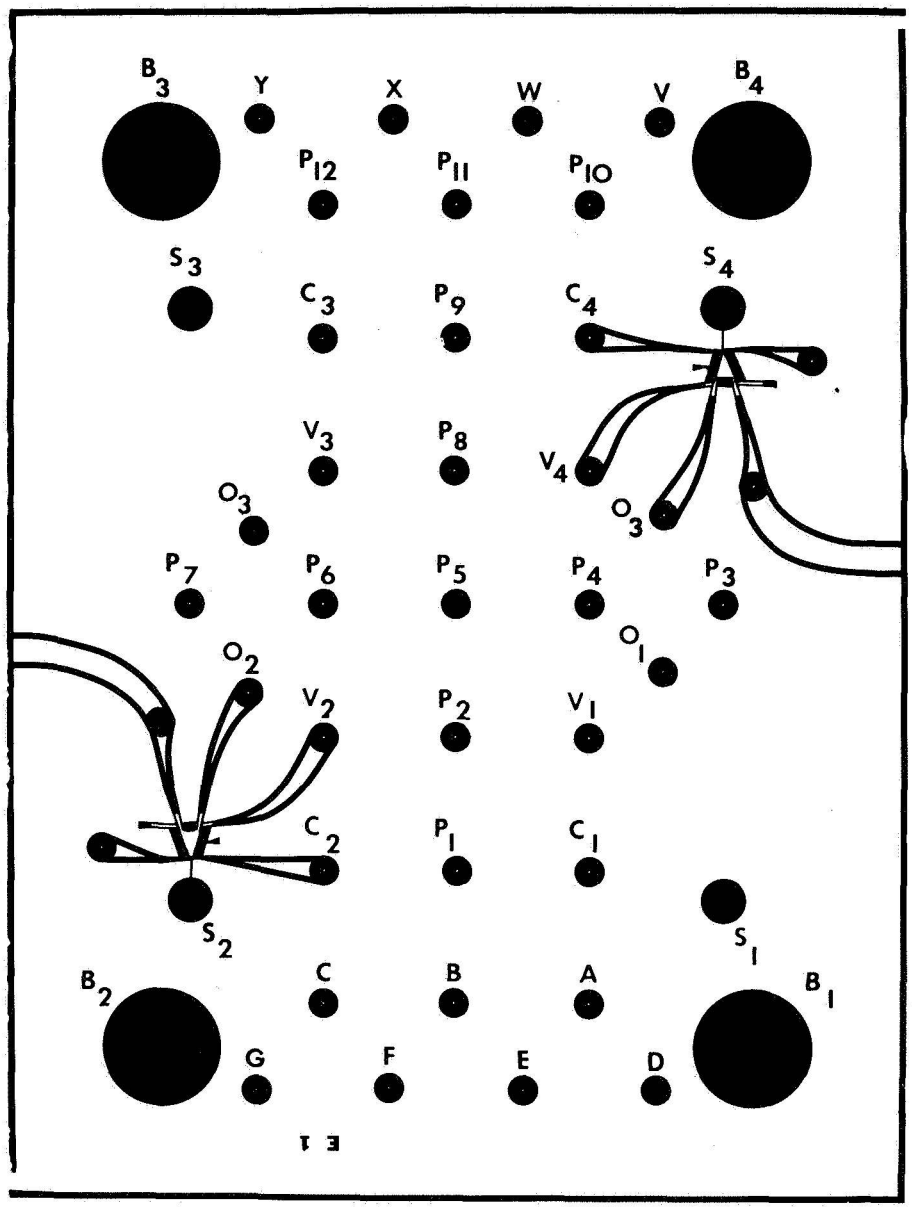

Figure 37. Element Plane Configuration

Circuit Layout. - Figure 37 is a representation of the actual element plane configuration. The actual element planes used for the decoder logic module are approximately one-fifth the size shown in Figure 38. Supply, control and output channels are indicated. The module built out of alternate layers of element planes and signal transfer planes can be held together with four small bolts or can be bonded together with a diffusion type bonding process. The hole pattern shown in Figure 18 serves to carry signals from elements situated on other planes on either side of the plane shown. If 85 gates are used to implement one decoder logic module, 43 element planes will be needed to complete the logic design. Together with 50 transfer planes for signal transfer and

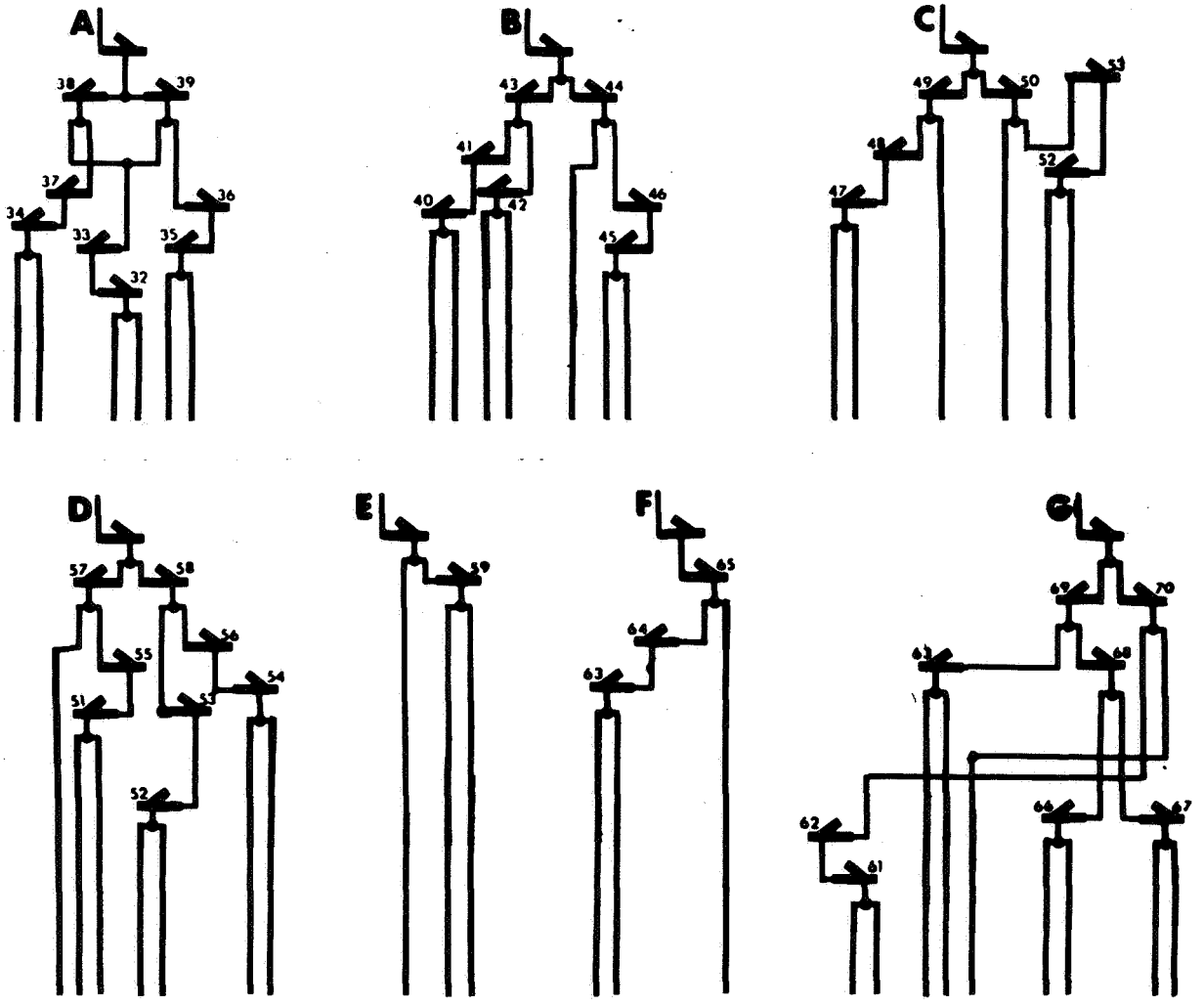

Figure 38. Decoder Submodules

special planes to vent the appropriate signal ports the total thickness of the logic package will be approximately 0.50 inches thick. The logic gate density of the decoder logic module is approximately 200 gates per cubic inch. This density is not the ultimate obtainable density. However, since the dimensions of each complete module are only 0.50 x 1.25 x 0.95 inches no further efforts were made towards miniaturization.

The following functions are associated with the hole pattern as shown in Figure 37:

1 A through G - output signals to display module

2 B_1 through B_4 - bolt hole used in assembly

3 C_1 through C_4 - control signals to logic gates

4 0_1 through 0_4 - output signals from logic gates

5 P_1 through P_{12} - transfer holes carrying signals from adjacent planes

6 S_1 through S_4 - supply to logic gates

7 V through Y - input signals from register

8 V_1 through V_4 - vent channels to ambient environment

In the logic module assembly the element planes are alternately used as shown in Figure 37 and rotated 180 degrees around one of the major axes of the element plane. In other words, when an element plane in the assembly is used in the configuration shown, i.e., when gates are present in the No. 2 and No. 4 position, the next element plane in the logic module assembly will have the elements located in the No. 1 and No. 3 position.

Assembly and Test. - In order to obtain simpler production, assembly, and testing procedures, the logic design was first broken down into seven sections as shown in Figure 38. These sections corresponded to the A through G outputs of the readouts.

The testing of the seven different submodules was accomplished by using an input simulator that feeds signals to the submodules. To keep the power consumption of the decoder logic module down to a reasonable minimum, one of the criteria used in checking the logic module performance was the ability of the complete module to function at a supply pressure of less than 10 inches of Hg. The following specifications were adhered to during the testing:

1 Supply pressure 10 inches of Hg maximum and 7 inches of Hg optimum, and

2 Control pressure 3.5 inches of Hg ± 0.5 inches of Hg.

In order to eliminate feedback from one submodule to another when the seven subassemblies are working together as a complete decoder, some isolation elements were added. The revised logic schematics are shown in Figure 39. This illustration shows the logic of the decoder as used in the demonstration model. The logic design shown appears to be the most economical design from a power consumption standpoint. Several gates can be eliminated from the design when higher supply pressures than those presently used are allowed. However, there is a tradeoff between the decrease in flow requirements due to the reduction in the amount of gates versus the increase on supply pressure necessary to operate a simpler design. This tradeoff favors the design operating from the lower supply pressure when compared on a power consumption basis.

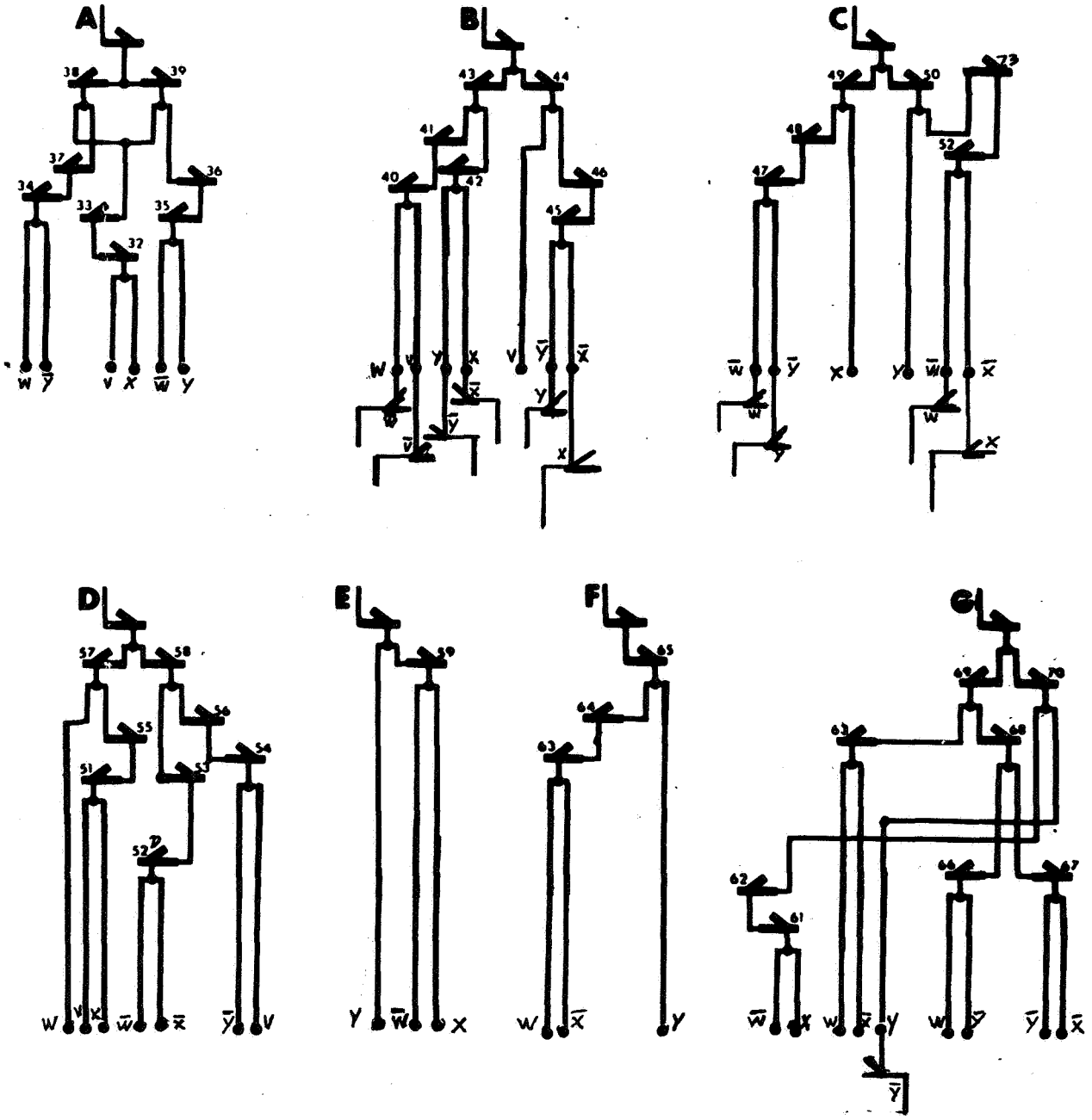

Figure 39. Decoder Submodules with Isolation Stages

Display Modules

The display units will use the pneumatic output of the decoder logic modules to activate the numerical characters on a readout matrix as explained in Section II of this report. The first efforts during this contract concentrated on the application of thermochromic materials to obtain a visual display. Thermochromic materials such as silver mercury iodide (Ag_2HgI_4) exhibit color changes when heated and revert to their original color when cooled. The color conversion depends on a change in the light reflecting properties of the ma-

terial and not on the emission of light as with electroluminescent materials. In this particular material the transition occurs at 50.5°C.*

Figure 40 shows the construction of two prototypes of a thermochromic display device which has been investigated. Both units consist of a brass ferrule with a disc coated with thermochromic material. One of these units had a solid copper disc coated with thermochromic material ($Ag_2Hg\ I_4$) fastened to the end of the ferrule. Gas outlet ports were provided, circumferentially. Initial testing of this device indicated that time constants of up to 15 seconds were common for this design.

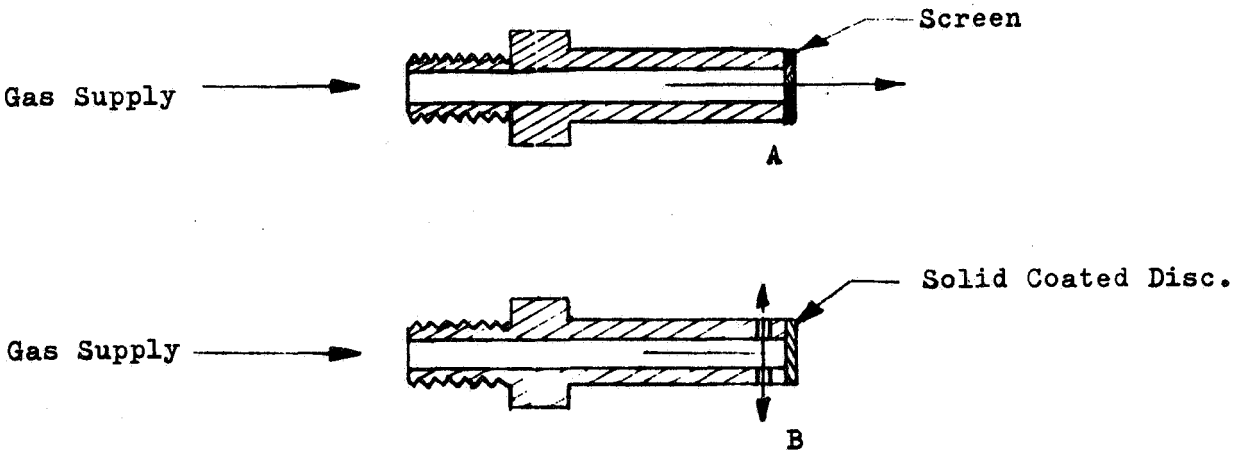

Figure 40. Thermochromic Display Test Modules

Efforts to decrease the time constant by using a better insulating material for the ferrule by using a ceramic pipe and using a thin copper disc (0.002 inch) as a substrate for the thermochromic material were not satisfactory. The measured time constant was at least one order of magnitude away from the design goal of 1 second, which is necessary to comply with the once per second updating requirements for the design units.

The second configuration, shown in Figure 40, was built with a stainless steel wire screen containing 125 wires of approximately 0.004 inch diameter per inch. This device exhibits a fast enough reversal time to obtain a once per second updating capability. However, the appearance of the thermochromic material, as coated on the screen, is not as bright as on the solid disc, and a great deal of the contrast between the two colors is lost.

A more attractive approach to the thermochromic display matrix design is depicted in Figure 41. This approach actually uses a reversed process from the units previously tried. By heating the thermochromic display permanently, to a point slightly above the conversion temperature of 50.5°C, with a nichrome

*Further information on thermochromic materials may be found in NASA reports CR-80016 and CR-86031.

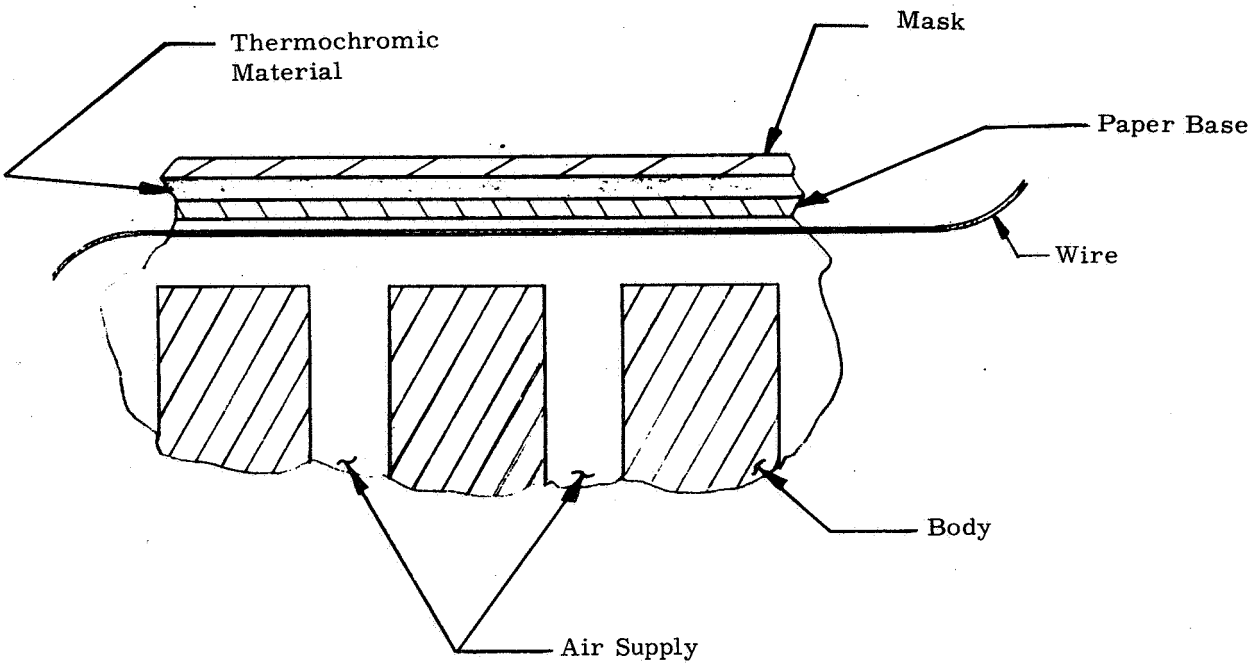

Figure 41. Thermochromic Display Matrix

wire, the inactivated state of the display will be the high temperature state of the thermochromic material. Ambient (room) temperature gas will cool the display locally and convert the thermochromic material to the low temperature state. The thermochromic materials are covered by a mask which matches the high temperature color of the thermochromic material.

Experiments with a prototype of the design shown in Figure 32 showed that adequate conversion time constants can be obtained by maintaining a small air gap between the heater wire and the paper thermochromic substrate. The distance between the heating wire and the paper substrate is critical but could be maintained with careful assembly procedures.

Investigations were conducted to determine the possibility of enhancing the contrast of the two color states of the thermochromic material by applying filtering techniques to the reflected light. Figure 42 shows the intensity of the reflected light (on an arbitrary scale) versus the wavelength for the thermochromic material $Ag_2Hg\ I_4$ for both color states. Figures 43 and 44 show light transmittance versus wavelength for two commercially available filter materials. As shown in Figures 45 and 46 more contrast between the two color states of the basic thermochromic materials can be obtained when a loss of the total amount of reflected light is permissible. Visual comparison tests indicated that the most legible display was still obtained without the described filters. Based on these results, the unfiltered version was retained as the most desirable design.

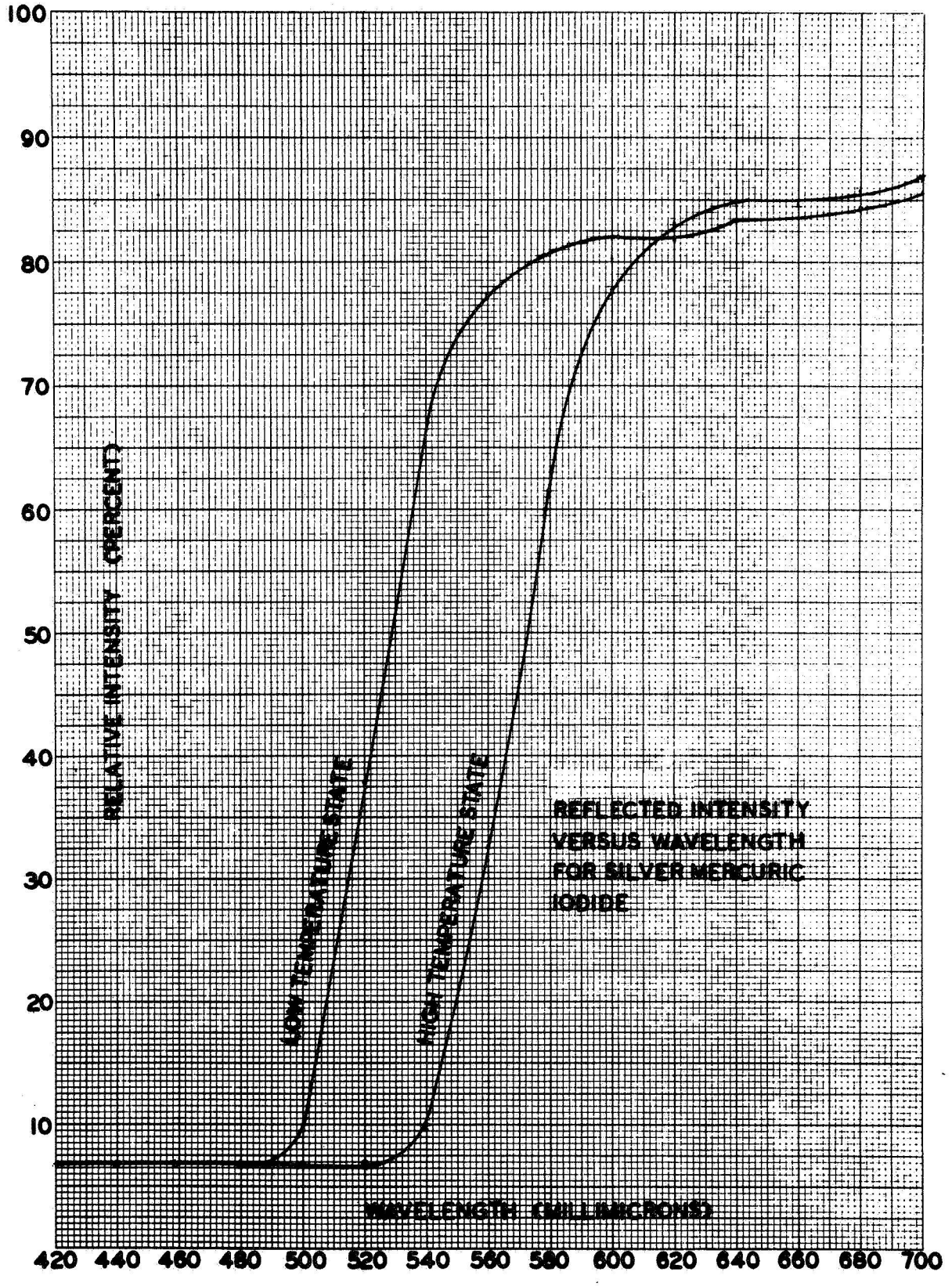

Figure 42. Reflected Intensity versus Wavelength for Silver Mercuric Iodide

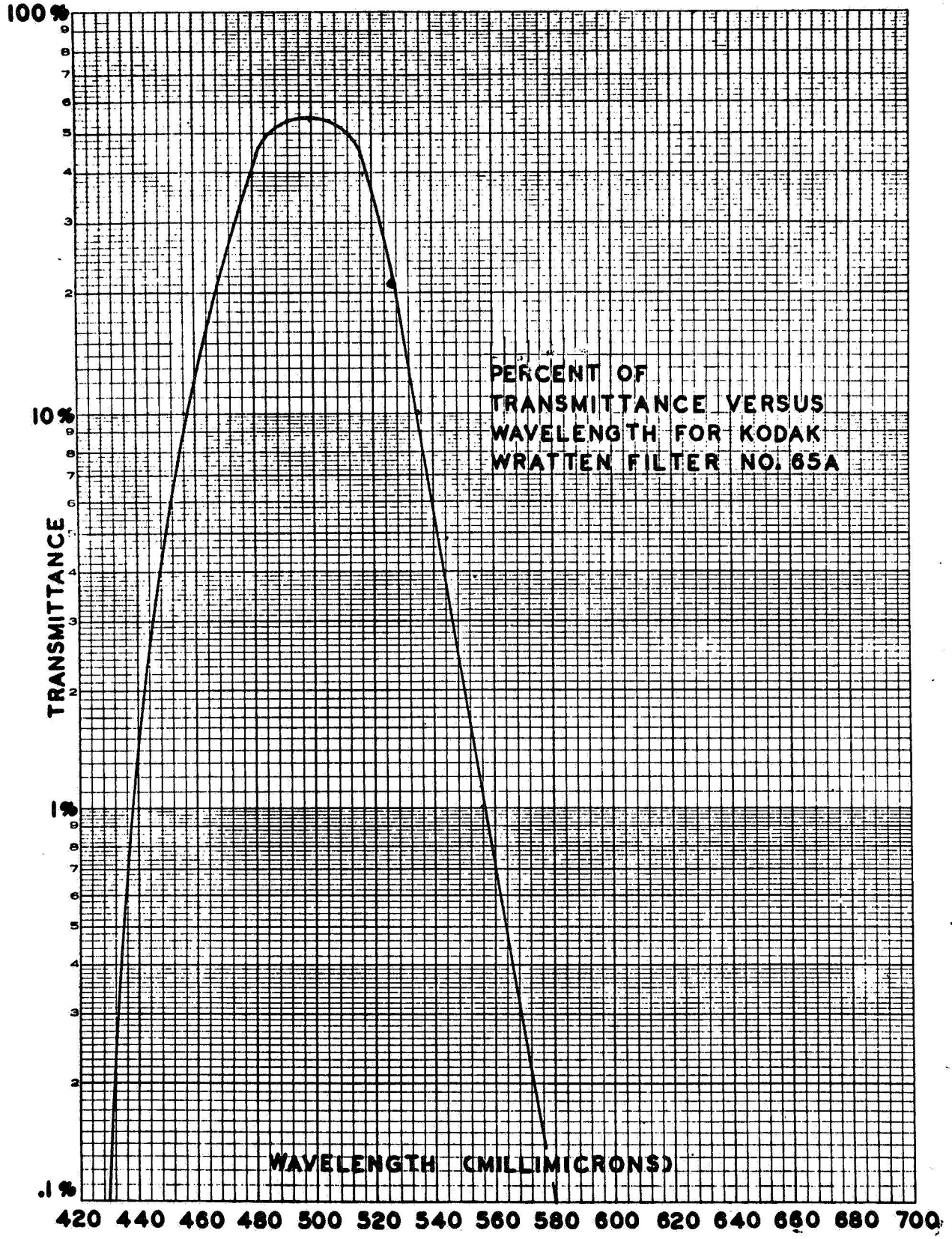

Figure 43. Percent of Transmittance versus Wavelength for Kodak Wratten Filter No. 65A

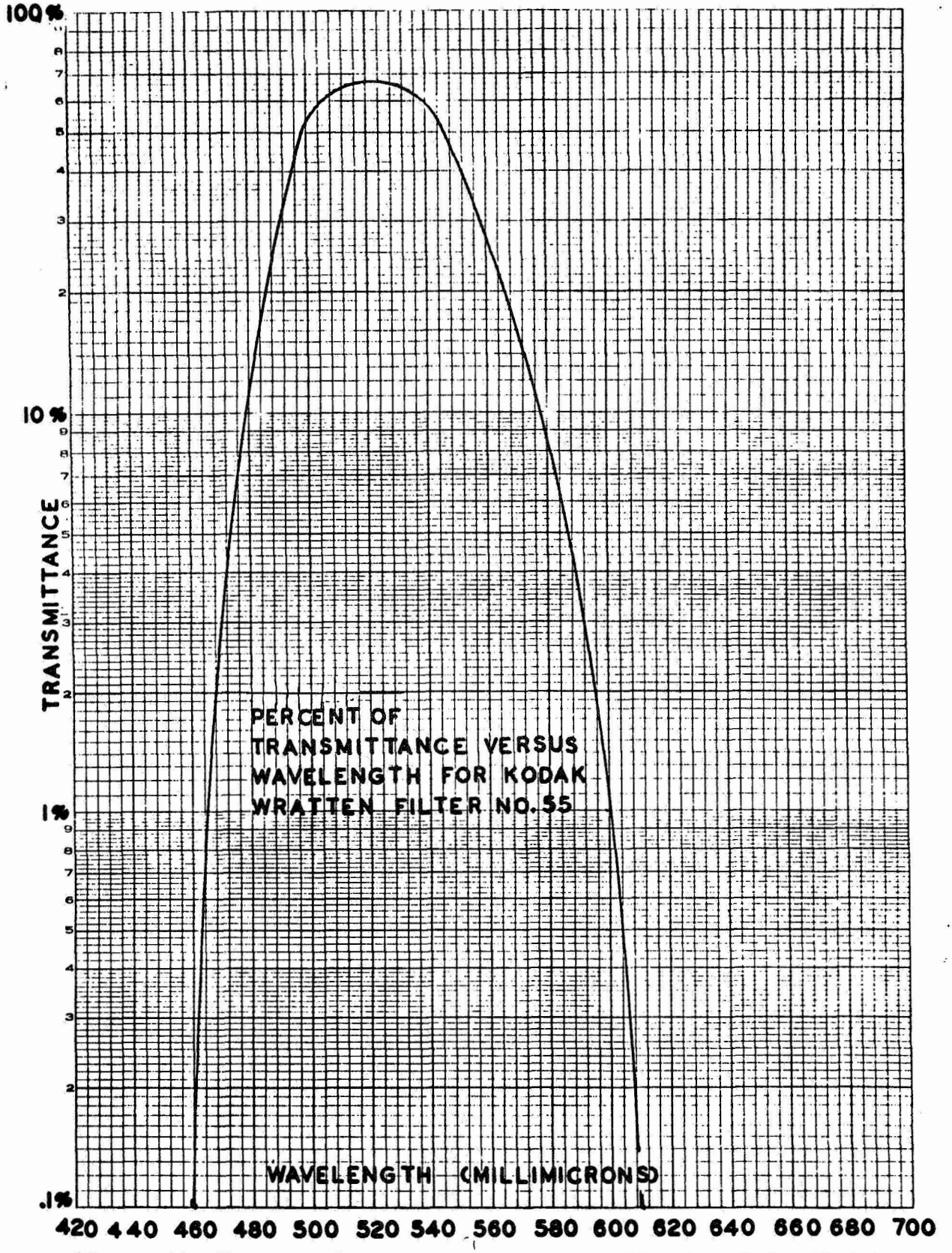

Figure 44. Percent of Transmittance versus Wavelength for Kodak Wratten Filter No. 55

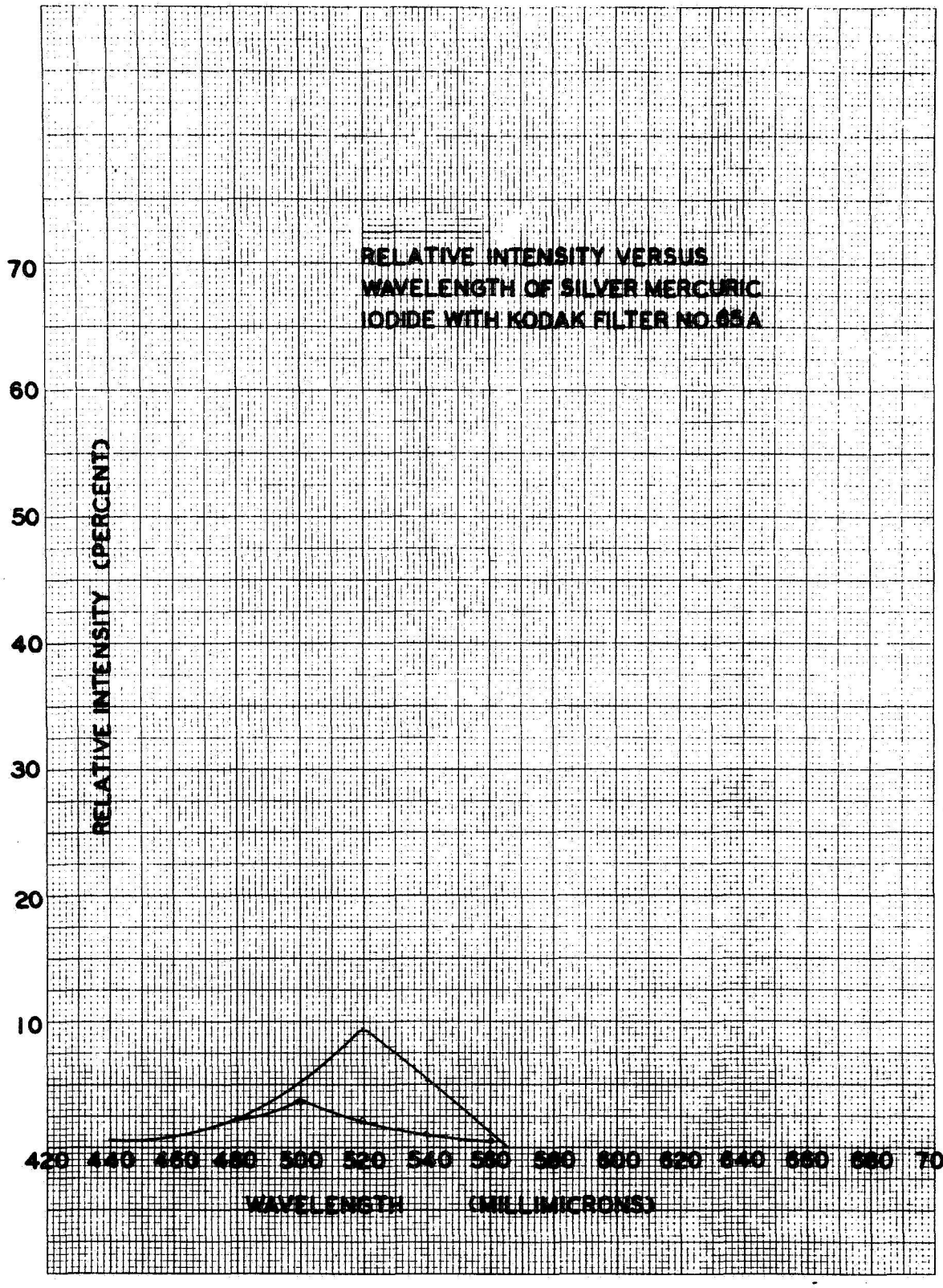

Figure 45. Relative Intensity versus Wavelength of Silver Mercuric Iodide with Kodak Filter No. 65A

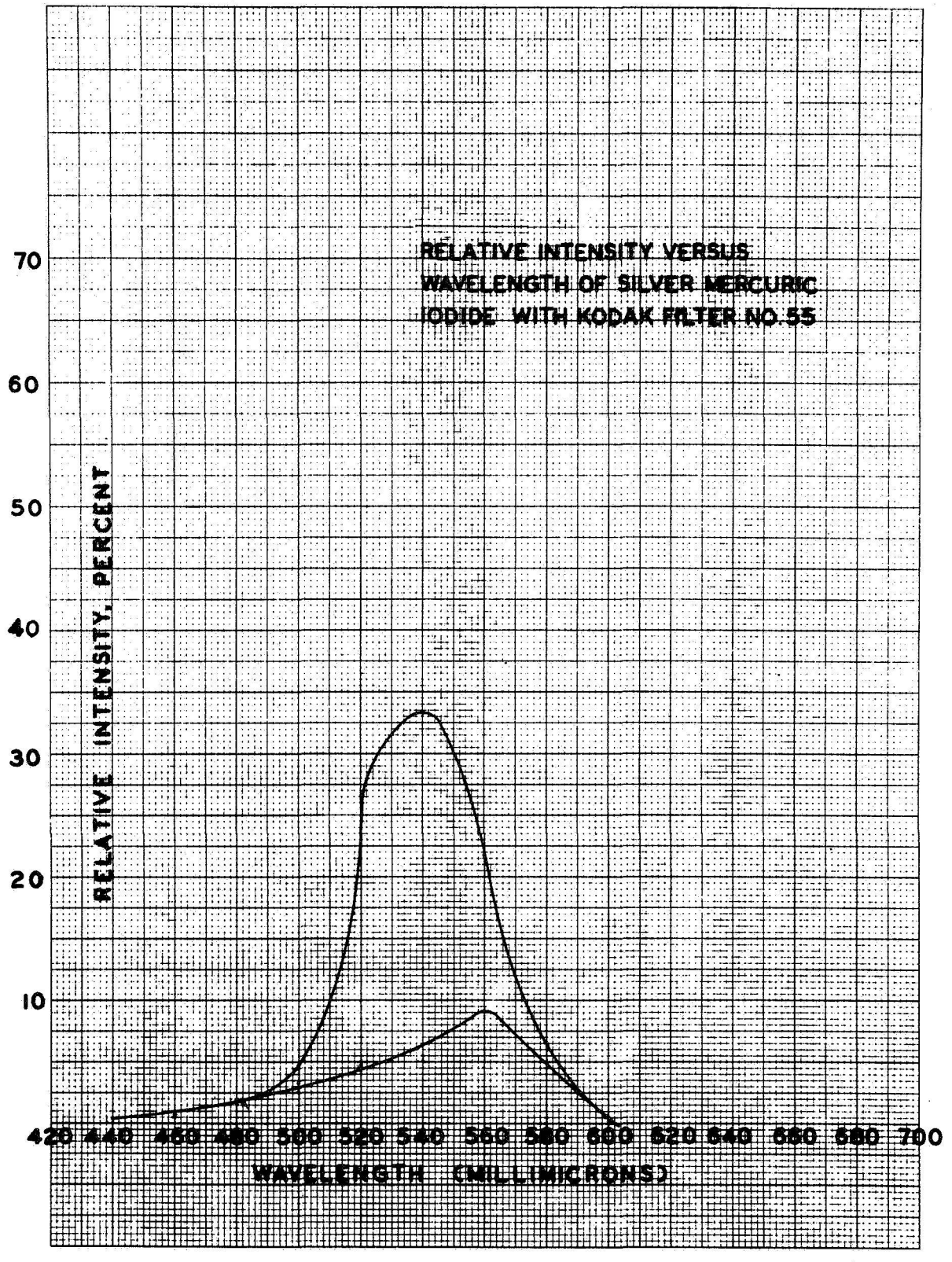

Figure 46. Relative Intensity versus Wavelength of Silver Mercuric Iodide with Kodak Filter No. 55

The base of the module which contains the heating wire and the channels for gas used for cooling part of the thermochromic material is made from aluminum. After machining operations, the base is hardcoated to form an insulation for the bare nichrome heating wire.

Response tests on a previously built prototype display module indicate that the required one cycle per 2 second response can be obtained. A 2 second cycle period will, of course, result in a once per second updating capability.

Observations indicated that a somewhat smaller size of the displayed character than previously used 1 inch high characters would be more in line with the overall size of the display and decoder unit. The character size was standardized on 0.75 inch high by 0.50 inch wide.

Register

The function of the register is to store the binary information supplied by the computer via the electro-fluid interface for further processing. The register consists of fluidic flip-flops which perform the function of a memory. The logic design of the register depends on the type of electro-fluid interface used. Both parallel and serial operation of the register is possible. Figure 3 in Section II of this report shows, schematically, the difference between serial and parallel operated registers.

The choice between parallel and serial operation of the register is governed by the following considerations:

1 Parallel logic requires more electrical connections between electronic computer and electro-to-fluid interface. Seventeen connections are used in parallel to transmit 16 bits of binary information. Serial logic reduces this to 3 wire connections. Obviously, a 3 wire connector interface between computer and decoder is simpler, lighter, and more reliable than a 17 wire connector.

2 Parallel logic requires 16 separate electro-to-fluid interface devices. Serial logic requires 2 electro-to-fluid interface devices. This affects space requirements and reliability.

3 Parallel logic requires 31 fluidic logic gates to implement a fluidic register. Forty-eight logic gates are required to build a serial register. Both serial and parallel fluidic registers are within the state of the art of the fluidics technology. It may be possible, with some development effort, to reduce the number of gates required from 48 to 32 for a 16-bit serial register.

4 Parallel logic has a better time response capability than serial logic. In the parallel logic operation all sixteen binary signals are transmitted from the electro-to-fluid interface devices simultaneously. The electrical signal has a 15 ms duration. Assuming that a 15 ms interval is observed during transmission of electrical signals, the transmission capability for the parallel circuit is 30 ms per 16 bits, or, an operating rate of 33.3 Hz. The serial logic design requires that the 16 binary bits are transmitted, sequentially, to the fluid register. The total transmission time, therefore, is 450 ms. The maximum operating frequency will thus be approximately 2 Hz when simple serial logic is used. The updating requirement for the decoder and display device is 1/2 Hz. Consequently, both serial and parallel logic arrangements are sufficiently fast to meet the requirements.

5 The electro-to-fluid interface devices considered for this application require a space of approximately 0.25 cubic inch per interface. Parallel logic arrangements thus require a volume of 16 x 0.25 = 4 cubic inch for the interface devices. Serial arrangements require a 2 x 0.25 = 0.5 cubic inch space. Certainly the serial arrangement will be more in keeping with the total volume of 6.25 cubic inch, which was the goal set for the total volume of the decoder and display.

The considerations are summarized in the following table:

TABLE VI

COMPARISON PARALLEL AND SERIAL LOGIC

	Parallel	Serial
Electrical connections	17	3
E to F interfaces	16	2
Fluidic logic gates	31	32-48
Max operating speed	33.3 Hz	2 Hz
Volume	4 in^3	0.5 in^3

The obvious choice is a serial register arrangement, providing one could be developed that requires only 32 logic elements. The only drawback to a serial arrangement is the long cycle time. However, the cycle time obtainable with a serial register is more than sufficient to meet the requirements. In order to evaluate the feasibility of using a serial arrangement attempts were made to develop a serial shift register.

Figure 47 shows the logic design of a 2-bit shift register, utilizing 3 elements per bit. A 16-bit register can be built up from 8 circuits, as shown in Figure 47, arranged serially. The binary information from the electro-to-

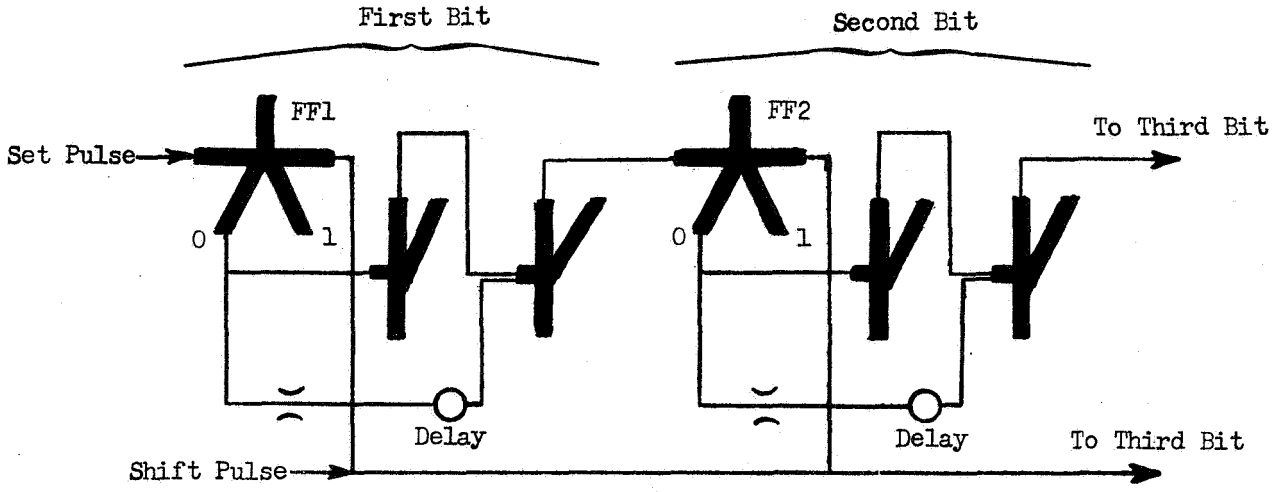

Figure 47. Two-bit Shift Register

fluid interface comes in through two parallel lines designated, "Shift Pulse" and "Set Pulse." The set pulse will set the fluidic flip-flop FF1, to the required value, 0 or 1. The shift pulse will cause the flip-flop in the second bit (FF2) to take on the same state as FF1. Flip-flop 1 is now cleared to be set to the next appropriate value. By continuously shifting the state of one flip-flop to the next flip-flop, a complete 16-bit register can be filled with binary information through the two incoming channels. The flip-flops (FF1, FF2, etc.) are used as inputs to the decoder logic module of the decoder and display device.

The circuit shown in Figure 47 was first built from standard fluidic elements with 0.010 inch, square nozzles because the logic elements were readily available at the start of this program. Performance of two bits of the shift register, implemented in this manner, was satisfactory.

In order to conserve power, the circuit was duplicated with elements with 0.004 inch nozzle widths. Again performance was satisfactory.

However, relatively high supply pressures (15 psig) were necessary to maintain uniform operation. At supply pressure levels of 3.5 to 5 psig, as used for the decoder logic modules, performance was acceptable. However, delay times created by the delay line circuit were erratic as soon as integrated circuits were used to implement the logic functions.

The apparent reason for the erratic switching times were traced to noise in the control signals. Unavoidably, the relatively long delay lines (approximately 5 inches) when compressed into an integrated circuit of a size compatible with the rest of the logic package contained several sections of relatively high resistances due to the "foldaway" design.

The points of high resistance coupled with the capacitances inherently associated with fluid transmission lines apparently created several resonance cavities each with an unique frequency and each generating noise. Furthermore, sharp bends in the fluid passages, unavoidable in this compact design, are also known to enhance low signal-to-noise ratios of transmitted signals.

Based on experimental results with four different circuit layouts of the shift register design implemented with miniature fluidic elements with 0.004 inch nozzles and operating at pressures of 3.5 to 5 psig, it was decided that the performance of the shift register was not reliable under these conditions.

Satisfactory performance with higher supply pressures (15 psig) was attained and implementation of the circuits in an on-board configuration is possible.

To explore other possibilities for acceptable designs requiring less supply power, a new shift register circuit was developed. The new circuit eliminates individual delay lines from each of the 15 required stages. They are replaced by an extra shift signal which is a reciprocal of the main shift signal employed in the more conventional designs. The circuit is schematically shown in Figure 48.

Operation of the circuit can be explained by an example. Assuming that a "one" signal is available in flip-flops A and at corresponding output stage B, the function of the register is to transfer this signal to the next stage. This is accomplished with the shift signals $\overline{S}_1$ and $\overline{S}_2$ which are present continuously. Shifting is accomplished by the temporary absence of signals $\overline{S}_1$ and $\overline{S}_2$ in this order.

The assumed state of flip-flop A will cause OR-NOR gate C to be "on" continuously, turning gate E off. Gate D which is off will not influence the state of gate F. When the $\overline{S}_2$ signal is temporarily removed, only gate F can be turned on, thus switching flip-flop G into the "one" position if it was not already there. Similarly, removal of the $\overline{S}_1$ signal will transfer the state of the G flip-flop into the H flip-flop which, in turn, will switch the J flip-flop. Thus by switching the $\overline{S}_2$ and $\overline{S}_1$ signals in this order the signal previously available as output flip-flop B of one stage is now transferred to the output flip-flop J of the next stage.

A shift register constructed according to the circuit shown in Figure 48 requires an input or first stage as shown in Figure 49. This first stage was built from one of the regular shift register bits with minor modifications.

A unique feature of the design shown in Figure 48 is the repetition of certain grouping of elements and their connections making it possible to build each bit of the shift register from two identical half bits combined with an output stage. This feature simplified fabrication and test of the register.

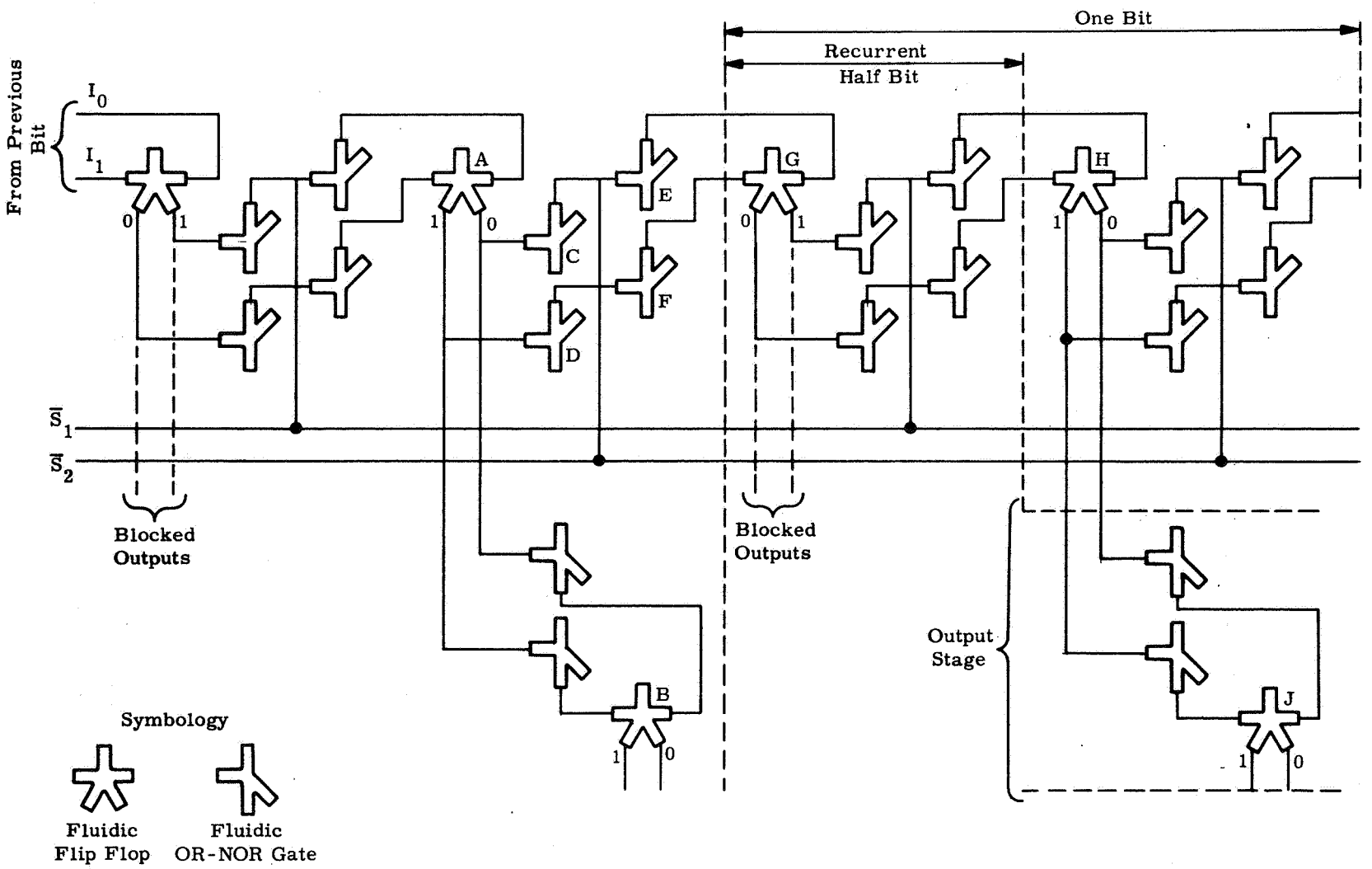

Figure 48. Shift Register Circuit

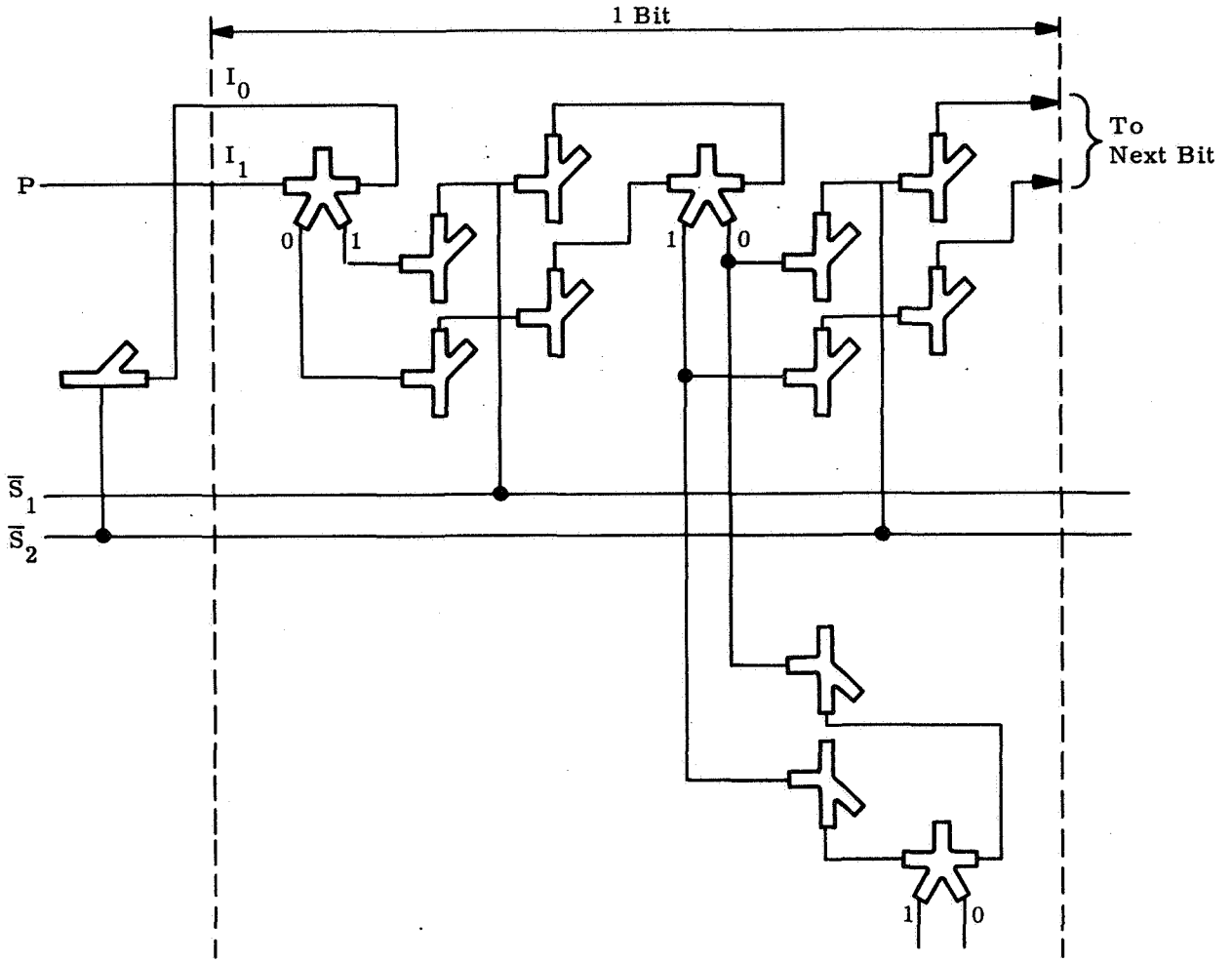

Figure 49. Shift Register Input Circuit

Fifteen bits of the shift register have been built and tested. Performance was judged satisfactory at the required pressure levels of 3.5 to 5 psig. Figure 50 is a photograph of eight bits of the shift register assembled into one package. The other seven bits are packaged in a separate assembly. The fifteen bits can be packaged in one stack, however, difficulties are encountered in handling the 30 required output signals plus shift pulses and power supply input connections in the available surface area.

The circuit, shown in Figure 48, was developed from a much simpler circuit, shown in Figure 51.

Difficulties with impedance matching, which again only became manifest at the low input power levels, required isolation amplifiers between shift signal operated OR-NOR gates and the flip-flops. An example of these isolation stages are gates C and D in Figure 48. The output stages were added to the design as shown in Figure 51 to obtain an isolated and more powerful output signal.

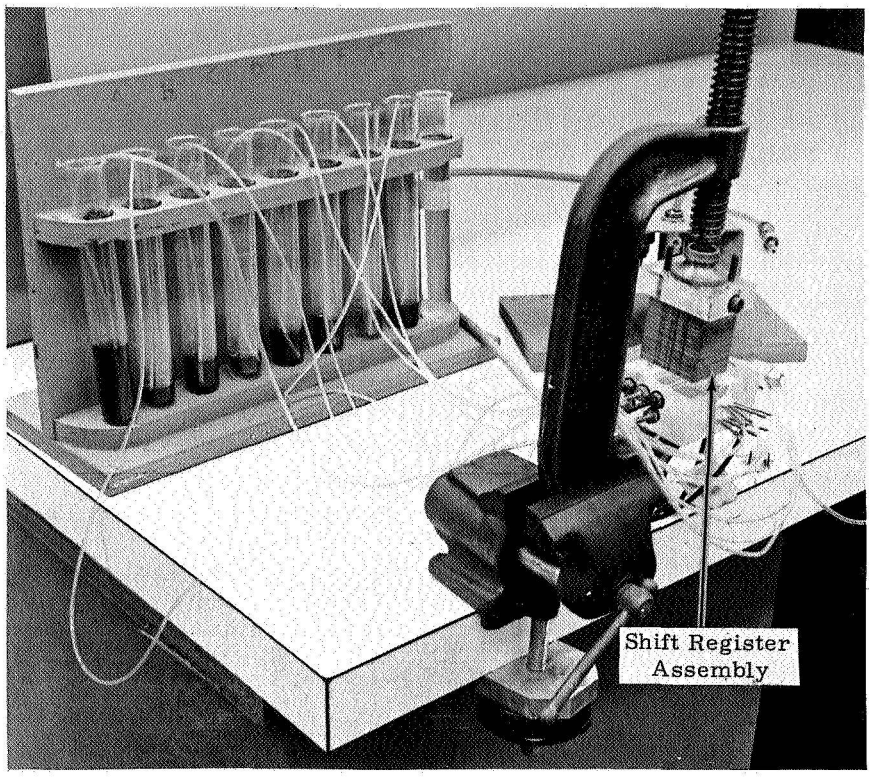

Figure 50. Eight-bit Shift Register

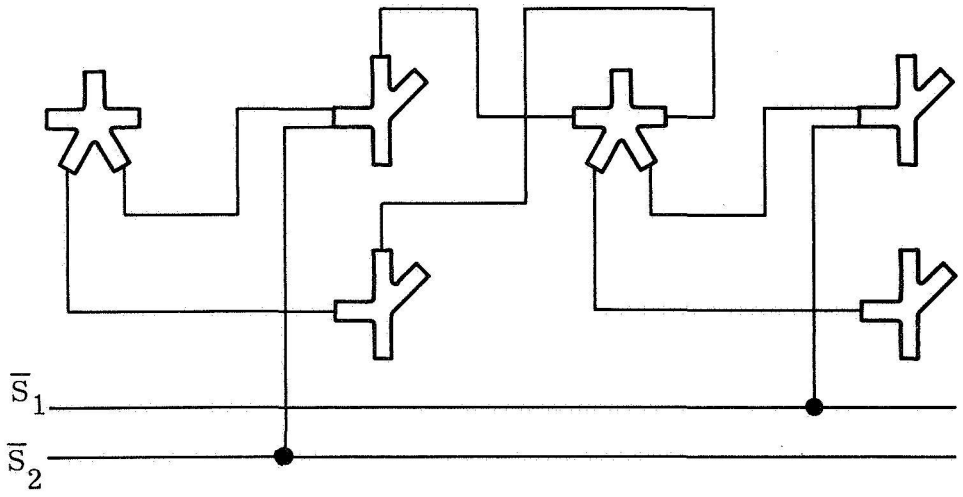

Figure 51. Shift Register Submodule

In order to obtain a properly working shift register, careful matching of the input-output impedances of connecting gates is required. Experiments show that a 15-bit register is too sensitive to variations in pressure to be applicable to the required system without modification. Less sensitive gates for this circuit are required for reliable operation.

Since parallel operation does not require such sensitive circuitry, the use of parallel logic for the shift register operation of the fluidic decoder and display device is recommended.

However, future development in fluidic logic gates should be monitored because even with the larger amount of logic gates, a serial register operating at low supply pressures is more economical from a power consumption point of view than a high pressure simple circuit as shown in Figure 47.

When this circuit is compared with the circuit of Figure 48, the power consumption can be calculated. The circuit shown in Figure 52 contains only three elements per stage while the schematic illustrated in Figure 48 uses 13 elements.

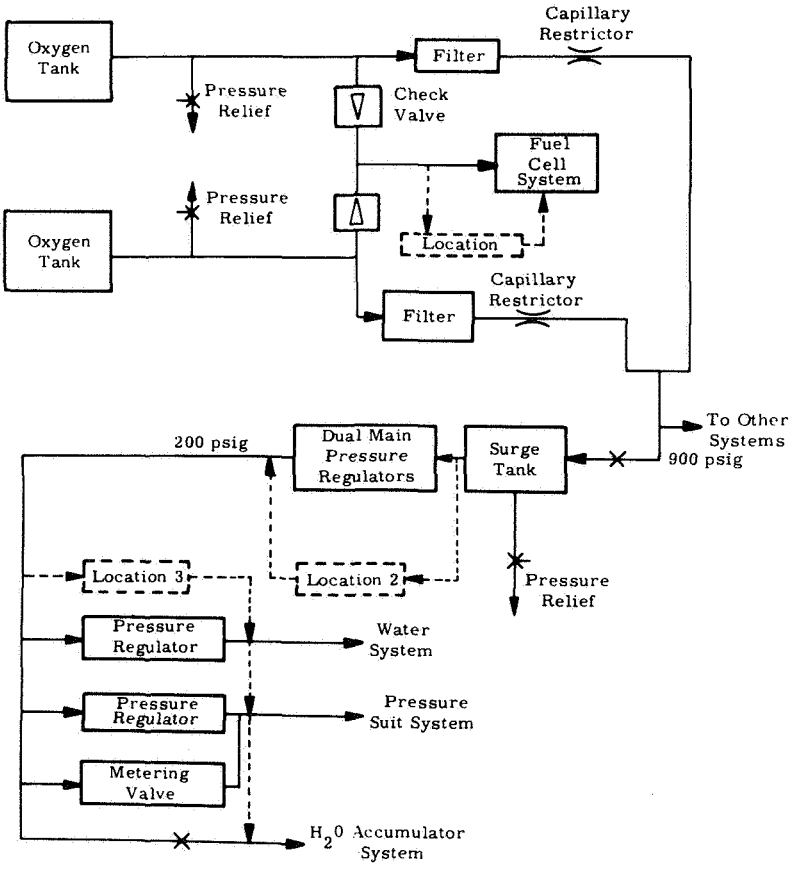

Figure 52. Pressure Sources for Fluidic Systems

Pneumatic power is the product of mass flow and supply pressure power. Therefore, consumption can be expressed as:

$$C = KWP \tag{29}$$

where

C = power consumed
K = proportionality constant
W = mass flow of gas
P = supply pressure of gas

For subsonic flow, the gas flow can be expressed as a function of pressure.

$$W = K_1\sqrt{P} \tag{30}$$

providing that temperature stays constant. Substitution of Equation (30) into (29) gives:

$$C = KK_1 P^{3/2} = K_2 P^{3/2} \tag{31}$$

where

$$KK_1 = K_2 .$$

Experiments established that the simple circuit as shown in Figure 48 required 15 psig for reliable operation. Power consumed per gate for this circuit is thus:

$$C_1 = K_2(15)^{3/2}$$

For the more complicated circuit a supply pressure of 3.5 psig is sufficient, consequently power requirements are:

$$C_2 = K_2(3.5)^{3/2} \tag{32}$$

The power ratio $\frac{C_1}{C_2}$ is now

$$\frac{C_1}{C_2} = \frac{K_2(15)^{3/2}}{K_2(3.5)^{3/2}} \approx 4^{3/2} = 8$$

Therefore, one gate in the circuit shown in Figure 21 will consume as much power as eight gates in the circuit illustrated in Figure 48. Since the element ratio of the circuits is 3 to 13, the more complicated circuit is more economical on a power consumption basis by a factor of $3/13 \times 8 \approx 1.9$.

Pneumatic Power Supply and Gas Consumption

Power consumption of the fluidic decoder and display device is an important consideration since it is one of the limiting factors in spacecraft design. Since the energy available in the gases carried by the spacecraft ordinarily is expended in an irreversible throttling process such as through regulators, the power for a fluidic display device can be considered free. The gas supply used by the fluidic display system can be returned to other parts of the pneumatic system with only a slight pressure drop.

Two main subsystems of spacecraft of conventional design can be used as a source for power for the fluidic display unit. These two main systems are:

1 Fuel cells used as power generators

2 Environmental control system.

Fuel Cells Used as Power Generators. - When using fuel cells as power generators, a cryogenic storage subsystem will supply hydrogen and oxygen gas to the power generating system. The amount of gas released by the cryogenic storage tanks is normally controlled by heating the gas in the tanks. The amount of heat generated depends on the demands placed on the power generating subsystem. Based on consumption experienced in previous flights, approximately 4.5 lb of oxygen will be used per hour. Hydrogen is also stored onboard in proportions suitable for fuel cell demands.

The Environmental Control System. - This system performs various functions such as water pressurization, suit pressurization, etc., and also supplies the life support oxygen.

A simplified schematic of the oxygen system presently proposed for a short range Apollo mission is shown in Figure 52. Even though the schematic is incomplete it illustrates some of the possible methods of tapping the pneumatic power source of a spacecraft without any loss in the total amount of gas available for other spacecraft functions. As evidenced from the figure, two oxygen tanks feed the fuel cell circuit through two check valves. A possible supply of gas for the fluidic decoder and display device is the fuel cell circuit (Location 1 in Figure 53). Gas can be taken from the upstream side of this circuit and returned to the fuel cells when utilized by the fluidic device. A similar circuit can be visualized in the hydrogen line feeding the fuel cell.

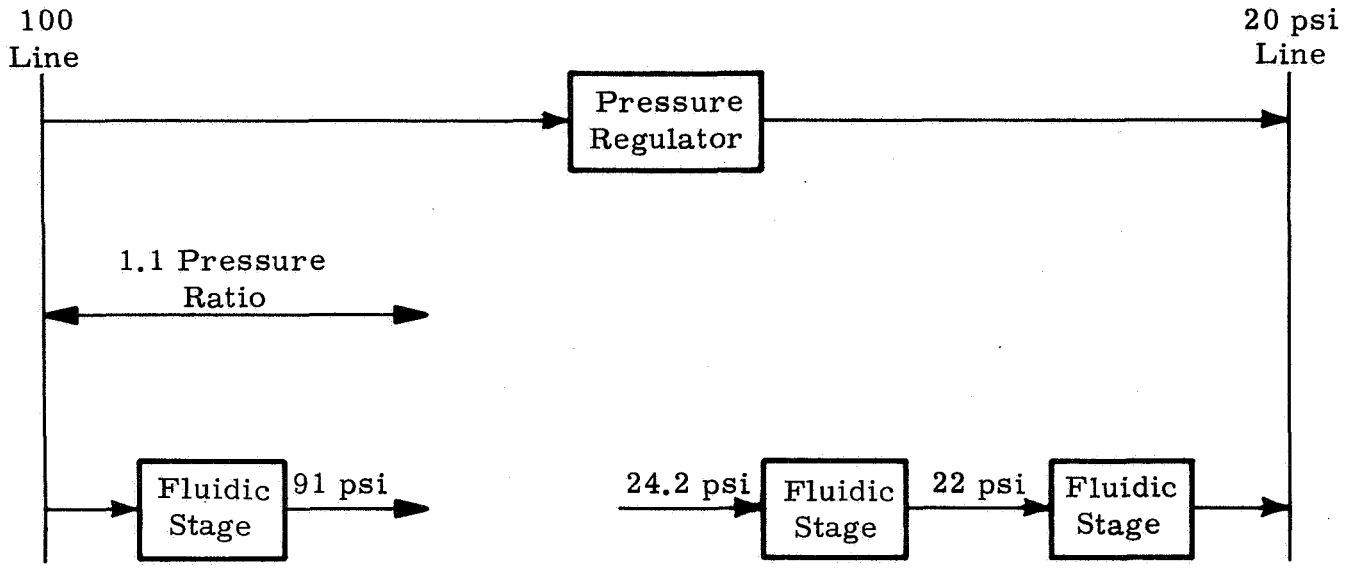

Figure 53. Fluidic Stages

Locations 2 and 3 are situated in the environmental control system. When the fluidic system is built around the dual main pressure regulator, the gas will be taken from the 900 psig supply line and returned at 100 psig downstream in this regulator. The stored energy which was partly wasted by the regulator system is thus utilized in the fluidic system. Flow will be 0.45 lb of oxygen per hour under normal conditions.

A similar free supply of energy is available when the system is used to by-pass part of the gas around any of the pressure regulators supplying the water system, the pressure suit system, or other low pressure life support systems. Experiments verified by analysis indicate that the flow consumption of one fluidic element is 60 cc/min at a supply pressure of 10 cm Hg.

The total number of elements in each decoder, as presently developed, is 63. The thermochromic readout modules require a gas flow equivalent to 51 elements for proper operation.

Total gas consumption for one readout module is:

$$(63 + 51)\ 60 = 6.85 \times 10^3 \text{ cc/min}$$

For five readout modules the total flow will be approximately 3.5×10^4 cc/min.

As previously mentioned, the life support system for three people requires a steady flow of 0.45 lb/hr which is equivalent to 2.5×10^3 cc/min.

The life support system regulator regulates pressure from 100 down to 20 psi. Several stages of fluidic logic can be placed in series in between these two pressure levels. The functioning of the fluidic elements is generally dependent upon the pressure ratio of inlet-to-ambient pressure on the elements. When the ambient pressure of one fluidic stage is made equal to the supply pressure of the next stage, as shown in Figure 53, the same gas flow can be used several times without any detrimental effect to either the life support gas system or the fluidic system.

A typical pressure ratio as used in the decoder logic built under this program is 14.7 +1.6/14.7 or approximately 1.1. With this pressure ratio of 1.1, seventeen stages can be interposed between the 100 psi supply line and the 20 psi low pressure line each with a pressure ratio of 1.1 across the stage.

Realizing that actual flow requirements per element will increase with increased back pressure, each succeeding stage will accommodate 9 percent less elements. Since the total flow available was established as 2.5×10^3 cc/min and the total required flow is 3.5×10^4 cc/min, the last stage will accommodate

$$\frac{2.5 \times 10^3}{3.5 \times 10^4} \times 100 = 7.15 \text{ percent}$$

of the total elements of the decoder. The next-to-last stage will accommodate 0.91 of 7.15 percent or 6.5 percent. Any stage accommodation can be derived in a similar manner. Two thirds of the total requirements for the decoder will be met by first bypassing the one regulator. Other stages can be built into circuits bypassing the pressure regulators for the water system, the pressure suit system, and the cabin pressure system.

Obviously, using only one bypass circuit is more desirable than tapping from several sources since this reduces the number of connections, the amount of plumbing, total weight, and reliability.

Since continuous operation of the decoder logic modules is not required for the functioning of the decoder, a fluidic pressure turndown valve can be employed. A fluidic pressure turndown valve suitable for application to the decoder is a fluidic vortex valve which is schematically shown in Figure 54.

The vortex valve consists of a cylindrical chamber with a radial inlet port for the supply flow and a tangential inlet for the control signal. The output port is situated axially in the center of the cylindrical chamber. When no control flow is present, the inlet flow follows a direct path through the valve towards the output port. When control flow is admitted to the device the momentum interchange between the tangentially entering control flow and the radial input flow will force the fluid to spiral around the output port which increases the

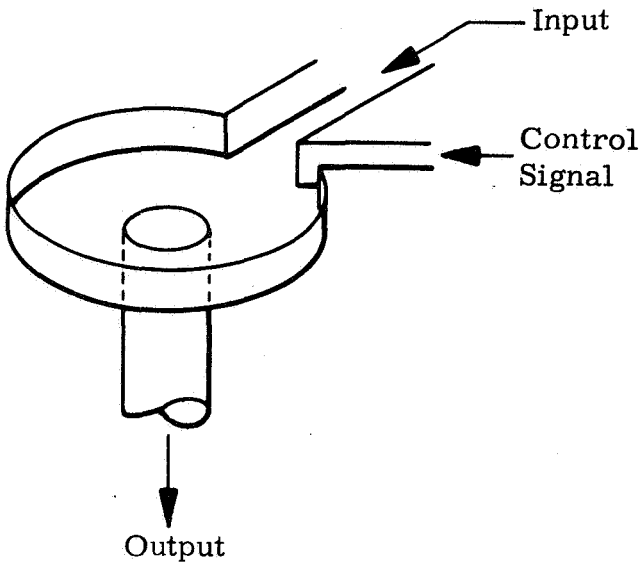

Figure 54. Vortex Valve

impedance seen by the input flow and thus reduces the total output flow. Figure 55 shows a typical performance curve of a vortex valve. The output flow reaches a maximum for a ratio of control pressure to supply pressure equal to one. Increased control pressure will diminish output flow. The total output flow, which consists of the input flow and the control flow, will reach a minimum when the supply flow is zero. Additional control pressure will, of course, result in an increase in output flow since more control flow is introduced.

The amount of flow turndown obtainable with a vortex value depends largely on the density and the viscosity of the fluid. Conventional designs of vortex valves used in control systems will typically reduce the flow by a factor of approximately 6.5. However, if additional outlet ports in the vortex valve can be provided, complete shutoff of the flow to the proposed system can be accomplished. A installation resulting in 100 percent flow shutoff is depicted in Figure 56. In this system the gas flow to the fluidic display device can be reduced to zero providing gas can be bled off to the other systems continuously. This setup can be used, when the bleed off flow is used as breathing oxygen in the crew's environmental control system. To keep flow at an absolute minimum, the use of a power turndown vortex valve in an on-board fluidic decoder and display device is recommended.

FEASIBILITY DEMONSTRATION MODEL

As part of contract NAS 12-532 a model fluidic decoder and display device was built in order to demonstrate the functioning of an on-board system.

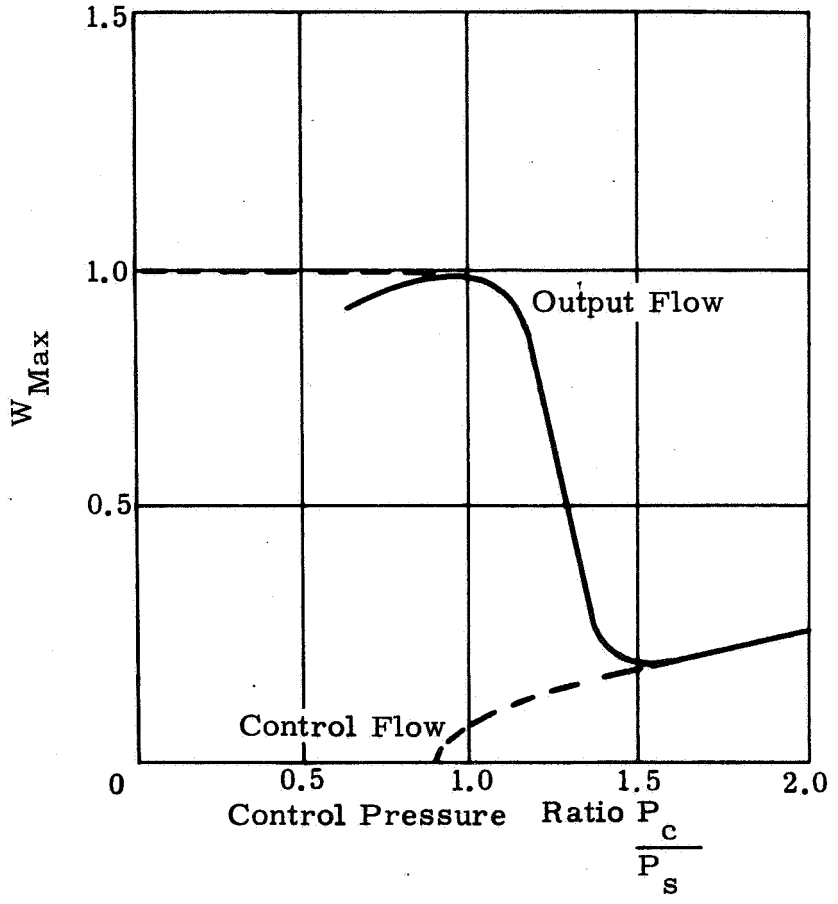

Figure 55. Vortex Valve Configuration and Flow Turndown Performance

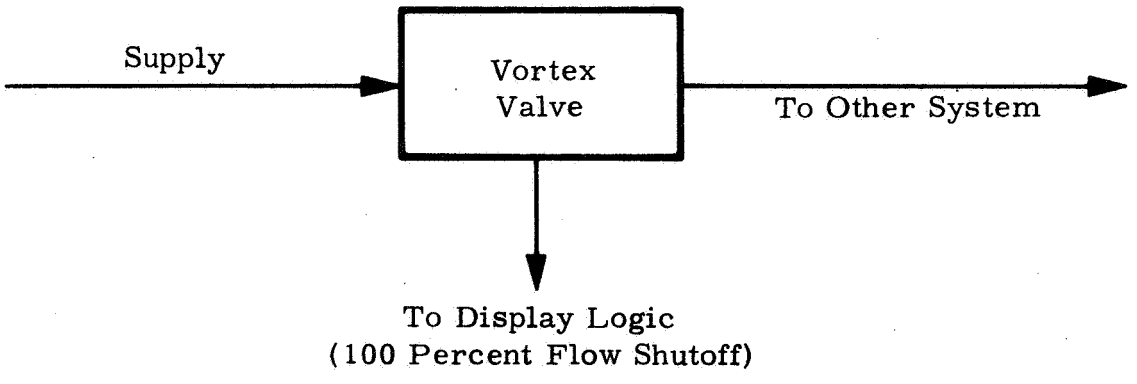

Figure 56. Vortex Valve Shut-off Schematic

The demonstration model consists basically of the same parts or subassemblies as the unit which could be built for on-board use.

In order to facilitate demonstrations at locations where gas supplies are not readily available, a small air compressor was used as a gas supply rather than a tank of compressed gas which would be available on-board a spacecraft. The electrical computer inputs are simulated by an electrical selector switch. Figure 57 is a photograph of the demonstration model. Each of the subassemblies of the demonstration model are described in this section.

Figure 57. Demonstration Module

Computer Input Simulation

The register inputs which are obtained from the on-board computer under normal operating conditions of the decoder and display device are simulated by an electrical selector switch on which any combinations of "ones" and "zeros" can be selected for the binary electrical input to the demonstration model.

The selector switch can be set for manual control or automatic stepping. In the manual mode the binary number to be decoded can be changed with a push button switch.

In the automatic mode of operation, the binary number to be decoded will change continuously. The updating rate for the numbers to be displayed can be varied from once per 0.1 seconds to once every three seconds.

Electro-to-Fluid Interface

The study of electro-to-fluid interfaces reported in section III of this report resulted in two possible candidate subsystems.

Solenoid Valve. - The first candidate was a solenoid valve which can be readily integrated with the fluidic circuitry as presently manufactured.

Piezoelectric Flapper Valve. - The second candidate was the piezoelectric crystal flapper valve.

Since more development work is necessary before the piezoelectric-type interface is suitable for use with integrated circuits, the solenoid type valve has been selected for use in the demonstration model.

Prototype Interface Design. - The demonstration model hardware has been designed in such a way that either one of the two types of interfaces can be used with a minimum amount of change in the adjoining hardware. If reliable operation of the piezoelectric type interface is obtained later, the solenoid valves can be replaced with the piezoelectric devices.

Decoder Logic Modules

The decoder logic modules are identical to those described in the Technical discussion, Section III. All design and construction details as well as test data are included in that section.

The demonstration model consists of three readout modules capable of translating 9 binary bits of computer information into 3 octal numbers.

Power Supply

The feasibility demonstration model is powered by air from a pneumatic compressor which is driven by an electric motor. In the actual airborne configuration, the decoder and display system will be driven by oxygen used for the life support system. However, gas tanks are cumbersome for portable demonstration units and a simple compressor was chosen to replace these tanks in the demonstration model.

Since the demonstration model is portable, an effort was made to obtain the smallest and lightest possible compressor and motor combination operated on 115V, 60 cycle, ac power.

A survey was made of companies known to manufacture pneumatic compressors to determine if their models could meet or exceed the following specifications:

1. Input power: 115 Vac 60 Hz
2. Output pressure: 15 lb/in^2 minimum
3. Output flow: 4 scfm minimum
4. Type compressor: centrifugal
5. Gaseous media: filtered dry air
6. Lubrication: solid lubricants
7. Type motor: squirrel cage, single phase, open construction
8. Cooling: air cooled.

Originally, consideration was given to using airborne pneumatic equipment in the actual system. However, most airborne systems use 400 Hz ac power so the electric motors furnished with this equipment were not compatible with the necessary input power requirements. Conversion of these motors to 115V 60 Hz ac power is costly and not considered feasible for the application.

The power suppy that comes closest to the specification is a model 0522-P102-C271X manufactured by Gast Manufacturing Corporation, Benton Harbor, Michigan. This model is still considered heavy for the application (27 lb).

CONCLUSIONS

Based on the results of this study and the operation of the demonstration model of the fluidic decoder and display device, developed under this contract, a design and development phase should be initiated for the readout part of the decoder and display device and for a piezoelectric-type electro-to-fluid interface.

The use of such an electro-to-fluid interface is by no means restricted to applications described in this report. It could also be used in most fluidic systems which require electrical signals as driving signals.

The fluidic logic elements are usable in circuits as they now exist. No further design or development programs are necessary for their utilization.

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13. ABSTRACT

This report, under Contract NAS 12-532, demonstrates the feasibility of the fluidic decoder and display device for use on board a spacecraft. This system may be used in place of the relay-type hardware currently planned for this operation. The advantages of the fluidic decoder and display device are that it conserves power sources by operating with available gases normally found in a space system and it provides a longer life expectancy than electroluminescent displays.

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