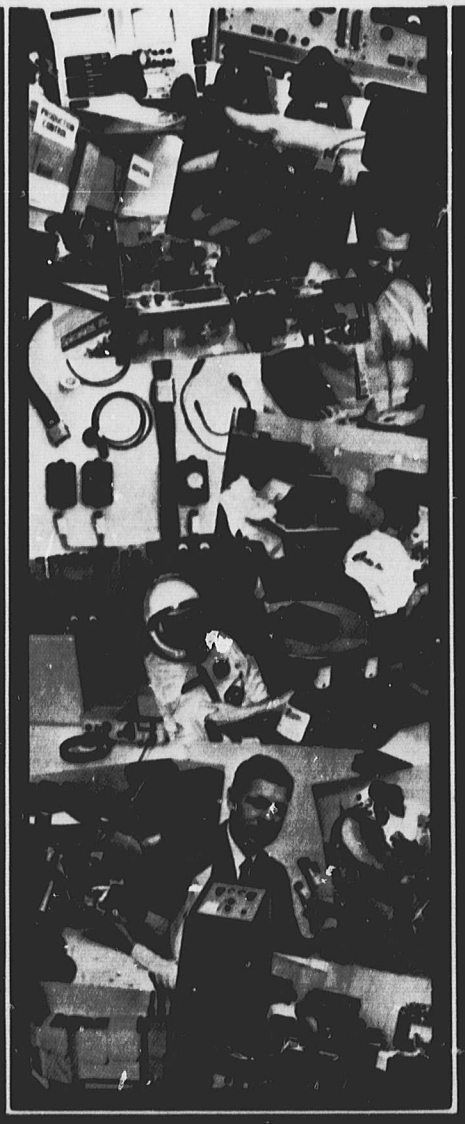
FINAL REPORT

CONTRACT NO. NAS 9-5431

APOLLO MEDICAL EXPERIMENTS SYSTEM

Spacelabs, Inc.



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FINAL REPORT

CONTRACT NO. NAS 9-5431

APOLLO MEDICAL EXPERIMENTS SYSTEM

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I INTRODUCTION

The Medical Experiments Program conducted by NASA as a part of Project Apollo involves the measurement of various physiological phenomena under conditions imposed by the Apollo flight environment.

Spacelabs, Inc. was contracted to design, develop and manufacture flight-rated equipment necessary to perform four of the in-flight physiological measurements.

The Medical Experiments System consists of:

- Phonocardiogram Subsystem (PCG)
- Electroencephalogram Subsystem (EEG)
- Vectorcardiograph Subsystem (VCG)
- Thoracic Blood Flow Measurement Subsystem (ZCG)

All of the above systems with the exception of the Electroencephalogram are concerned with the measurement of cardiac activity. The Phonocardiogram detects Korotkow sounds, the Thoracic Blood Flow Measurement System determines thoracic impedance variations, while the Vectorcardiograph System provides a vector representation of standard Electrocardiogram signals. The Electroencephalogram System detects and provides a measurement of the well-known brainwave activity.

The system is powered by a common power supply, which was contracted for development as a part of the VCG Subsystem.

The Contract was awarded to Spacelabs, Inc. in December of 1965, and the design, development, and production of the system was completed in August of 1968.

Inasmuch as the program was conducted over a 2-1/2 year period and involved the development of four individual subsystems, it is difficult to easily present a concise view of the Contract performance and results. As a consequence, the report is divided into sections, each of which independently discusses one particular aspect of the total effort. The Program Chronology, which precedes the technical content of the report, highlights the major program events and serves to provide a brief overview of the program.

II PROGRAM CHRONOLOGY

The Program Chronology which follows is a narrative of the month-by-month progress of the program. Because detail would be difficult to hold in perspective, the presentation has been limited to a brief discussion of the highlights.

December 1965

The Contract was awarded in December of 1965. Immediately following award of the Contract, preliminary Systems Engineering was initiated with major emphasis on design and development of the PCG Subsystem. The development schedule for the PCG Subsystem was accelerated in order to meet scheduled flight requirements.

Early in the program, management and production plans were prepared for submittal to NASA.

January 1966

Early in January, the prototype PCG transducers were delivered, and fabrication of the qualification test units was well underway. Production deliveries were scheduled to begin on March 15, immediately following completion of the qualification testing.

Subsystem and circuit analysis on the remaining subsystems progressed according to schedule, and together with preliminary product design were

scheduled for a preliminary Design Review early in February. Of major concern during this period was the definition of the subsystem harness configurations and performance parameters.

February 1966

The temperature requirements for the PCG transducer resulted in a fabrication problem. The material exhibited an instability at elevated temperature. A Materials Consultant was called in to discuss the instability and the fabrication techniques in an effort to solve the problem. In view of the fact that a different material suitable for use on the Apollo Program could not be located, an Engineering Change Proposal was submitted to NASA recommending a maximum temperature of 120°. By limiting the temperature to 120°, the stability problem no longer existed. As a result of these problems, a schedule slippage occurred which delayed the estimated completion of qualification testing to the middle of April. This forced a change in the delivery of the initial production units.

During this period, considerable effort was expended on the definition of production harnesses for the other subsystems. Final circuit and product design of these systems was in progress. Fabrication of the deliverable breadboards was in progress and on schedule.

March 1966

Problems continued to plague the development of the PCG Subsystem after a solution to the materials problem discussed above. Additional program

delays were experienced due to delayed delivery of Special Test Equipment required for the production acceptance test. This particular problem resulted in approximately one month of schedule delay. During this time, other methods of evaluating the transducer calibration were pursued jointly with NASA technical personnel.

Definition of the remaining subsystems, including the overall mechanical configuration and harnesses, was being pursued with the cooperation of NASA technical personnel.

A technical meeting with the Principal Investigator, the NASA Technical Monitor, and Spacelabs representatives was held at the University of Minnesota to discuss the problems associated with, and the general progress of, the ZCG Subsystem.

April 1966

During April, the PCG problems continued to have a detrimental effect on delivery schedules. Several housings were supplied to NASA for evaluation. Additionally, an annealing process was incorporated into the fabrication technique in order to minimize the dimensional instability exhibited by the transducer housing.

The calibration equipment necessary for the PCG production acceptance test was received and development of a special adapter was initiated.

A Program Design Review Meeting was held on April 13 and 14, during which the construction materials and fabrication processes relative to the PCG were examined in detail.

Design of the EEG Subsystem was completed and most of the documentation required by Contract had been submitted to NASA for approval.

During the April Design Review, considerable discussion of the calibration technique employed in the VCG Subsystem resulted in a tentative decision on the part of NASA to incorporate a change. Changes in the ZCG calibration requirements were also discussed in detail, and as a result it was decided that Spacelabs would submit an Engineering Change Proposal defining the changes necessary to the Equipment Specification to accomplish the equipment modification.

Evaluation of the VCG Subsystem by the Principal Investigator began.

ZCG breadboard subsystems were delivered to both the Principal Investigator and the NASA Technical Monitor.

May 1966

The PCG transducer entered qualification during May. In order to expedite delivery, an attempt was made to obtain a certified statement as to the nutrient characteristics of the bonding material being used in the transducer. In the absence of a certification, the transducer would have to be subjected to a 28-day fungus test.

Production of the EEG prototype was temporarily stopped by NASA direction pending an investigation into the bandwidth/noise trade-offs. An attempt to widen the bandwidth to increase the versatility of the signal conditioner was contemplated by NASA. However, should the increased bandwidth result in a significant increase in noise, the Specification would remain as originally written.

During this period, NASA deleted the EEG harness requirement in order to permit additional time to study the problems inherent in its design.

An Engineering Change Proposal was submitted, which redefined the Equipment Specifications. Its effect on the VCG and ZCG Subsystems amounted to changes in the calibration technique, certain of the performance specifications, and the packaging configuration.

June 1966

Qualification of the PCG transducers was completed and post-qualification examination concluded.

Three production PCG transducers were delivered and the remaining seven were in production and on schedule.

The VCG Subsystem breadboard was returned to Spacelabs for modification in accordance with an arrangement agreed upon by NASA, the Principal Investigator and Spacelabs.

Component procurement difficulties resulted in completion delays of the prototype EEG unit. Components used in the EEG were scheduled for delivery in sufficient time to meet schedule; however, the manufacturer lost an entire lot, and as a consequence the schedule slipped approximately 30 days.

The ZCG Subsystem was nearing redesign completion and the breadboards were being modified to incorporate the changes proposed in Engineering Change Proposal No. 5.

July 1966

Five production PCG transducers were delivered in July in sufficient time to prevent jeopardizing flight schedule or experiment status. Additional transducer production was stopped in accordance with the Technical Monitor's instructions, and the fabrication of two test specimens was initiated. Additional testing was considered necessary to solve questions relative to the performance of the transducer under conditions of severe humidity.

Due to the airline strike which occurred during this month, time was lost during the shipment of the VCG breadboard system to the Principal Investigator. The ZCG Subsystem breadboards were returned to Spacelabs for modification. Documentation effort on both the VCG and the ZCG continued. During this period, Design Acceptance Test Procedures were submitted for approval.

August 1966

The PCG Qualification Report was completed and scheduled for delivery to NASA the following month. Additional testing of the test specimens was completed successfully, and it was concluded that the equipment operated properly in the required humidity environment. Five additional PCG transducers were fabricated and delivered to NASA.

The EEG Subsystem prototype and qualification units were acceptance tested. During the acceptance test, it was noted that the input impedance of the amplifier was out of specification. A series of tests were conducted, and it was determined that capacitive feedback to the amplifier occurred as a result of the physical layout of the package. An analysis of the problem concurred with empirical results and a decision was made to redesign the EEG package.

Testing and modification of both the VCG and ZCG breadboards continued during the month of August. The final redesign of the VCG packaging was initiated and the packaging effort on the ZCG was completed. Material procurement for the entire program was reinitiated and the Program Schedule was updated.

September 1966

Conclusion of the PCG effort occurred in August, and final approval of the Qualification Test Report was pending.

The EEG Signal Conditioner was repackaged and two prototypes were fabricated.

The VCG breadboard was resubmitted to the Principal Investigator. The package design of the DC-DC Converter, which was contracted as a part of the VCG Subsystem, was in the final stages of package design.

Fabrication of acceptance and qualification test units was in progress, and additional documentation was being prepared for submittal to NASA.

During the month of September the NASA Quality Assurance Representative visited Spacelabs to discuss various contractual items. Qualification requirements were definitized, and the disposition of particular components was determined.

October 1966

Engineering evaluation of the prototypes, which were fabricated subsequent to repackaging, was nearing completion.

The VCG breadboard subsystem was completely modified in accordance with NASA instructions and returned for evaluation and approval. Final package design of the DC-DC Converter was completed. Engineering drawings were released to Operations for preparation of production procedures.

The ZCG Subsystem drawings and Parts Lists were also released to Operations in preparation for production. Pre-delivery Acceptance Test Procedures were completed and submitted to NASA for approval.

November - December 1966

The EEG prototype units were completed and the prototype signal conditioners were scheduled for shipment in January. The VCG and ZCG Subsystems were being redesigned to reflect the requirements of NASA Modification No. 9.

At this time, the final requirements for the DC-DC Converter were still under consideration, and as a consequence further design effort was held.

January - February 1967

The EEG prototype units were shipped and fabrication of the qualification units was nearing completion.

The VCG breadboard was shipped early in January and system approval was received late in January for the configuration defined by NASA Modification No. 9.

The DC-DC Converter was redefined by NASA Modification No. 9, and subsequently by NASA Modification No. 12. Design changes and document modifications reflecting these changes were in progress.

System approval for the ZCG configuration reflected through NASA Modification No. 12 was granted late in January and final design was underway.

March 1967

The EEG Signal Conditioner was in acceptance test and details of the qualification testing were being established.

Final design of the VCG Subsystem was completed and modification of system drawings and documentation was underway. Final procurement of components for the fabrication cycle was initiated.

Electronic design of the DC-DC Converter was completed and packaging design was in progress. Completion of drawings and documentation associated with the Converter was scheduled for April.

Technical difficulties during the redesign of the ZCG resulted in some delays. However, these problems were resolved and final product design was nearing completion.

April 1967

Progress toward completion of the manufacturing data requirements continued throughout the month of April on all subsystems.

May 1967

The completion of reliability analysis for the ZCG Subsystem, and quotes on qualification testing for the EEG and VCG, were being reviewed. In view of the fact that the VCG and the EEG qualification units were scheduled to be completed near the same time, it was planned to qualify these systems simultaneously.

Difficulties were encountered with the EMI requirements relative to the DC-DC Converter, and design modification was initiated to correct the problem.

The ZCG Subsystem continued through the packaging and procurement cycle. Testing was underway to evaluate performance relative to RFI requirements.

June 1967

Subcontractor qualification of EEG and VCG Subsystem had been negotiated and qualification testing was scheduled to begin early in July.

Design modification of the DC-DC Converter continued somewhat behind schedule due to the requirement for modifying the package configuration imposed by requirements of MIL-I-26600.

Production of the ZCG prototype and qualification units was underway and scheduled for completion during July.

July 1967

The qualification of the EEG Signal Conditioner was held pending subsystem disposition by NASA. The VCG Subsystem qualification testing was in progress.

Electronic design of the DC-DC Converter was completed. Packaging design was underway and was scheduled for completion in August.

Fabrication and testing of the ZCG prototype and qualification subsystems continued.

August 1967

End item testing of the EEG Signal Conditioners was completed and units were being held pending shipping instructions from NASA.

Qualification of the VCG Subsystem continued, and preliminary production of the VCG flight units was underway.

The DC-DC Converter successfully passed preliminary RFI interference testing and progress toward the completion of the packaging continued.

Production of the prototype and qualification of the ZCG Subsystem continued.

September 1967

The EEG Subsystems were still being held pending NASA execution of Modification No. 13 to the Contract.

The prototype VCG Subsystem was completed and shipped to NASA, and qualification testing was successfully completed.

The DC-DC Converter prototype and qualification units were being manufactured and were scheduled for completion in October.

Completion of the design acceptance testing of the VCG had been scheduled for completion by this time; however, during system integration it was determined that changes in the internal shielding and cable routing would improve system performance. Additionally, effort continued on the current

source output impedance problem, which resulted in an improved transformer configuration.

October 1967

Modification No. 13 to the Contract was received and implementation of the requirements was initiated.

The EEG qualification units were shipped to NASA, and fabrication and testing of the ECG Signal Conditioners required in accordance with Modification No. 13 began.

The VCG Qualification Test Report was received from the Subcontractor. After review, the Qualification Test Report and the qualification units were shipped to NASA.

Production of the VCG flight units was proceeding on schedule.

Fabrication of the DC-DC Converter prototype was in progress and scheduled for completion by the end of November.

The transformer modification to the ZCG current source had been completed and design acceptance testing and shipment of the prototype unit was scheduled to occur during December.

November 1967

Progress toward the completion of all subsystems continued with problems developing with the DC-DC Converter only. These problems involved

procurement lead time and converter case fabrication problems. Because of stringent technical requirements, the decision to x-ray the first articles received was made, and as a result schedule slippage occurred.

December 1967 - August 1968

The VCG flight systems were completed and shipped to NASA on ./10/68.

The DC-DC Converter was complete through qualification testing in April. In the interest of schedules, and based on the results of the early phases of qualification testing, the flight units were released to Manufacturing early and cycled through the manufacturing phase to a point just short of final encapsulation. After successful completion of the qualification test, the fabrication of the flight units was completed. Shipment of the qualification and flight units was scheduled for May.

The ZCG prototype was completed and successfully passed design acceptance testing. The prototype and one STE harness was shipped to NASA during January. Fabrication and testing of the qualification units was underway when a problem relative to the stability of the current source was detected. A program was launched to investigate this problem. Subsequently a meeting was held with NASA personnel during which this problem was resolved.

Delivery of hardware required by the Contract was completed with the shipment of the ZCG Subsystems in August.

III EQUIPMENT DESCRIPTION

Because much of the design of the subsystems contracted is unconventional, a detailed description of the subsystem circuitry is presented herein. In the interest of brevity, detailed description of any conventional circuitry incorporated has been excluded. Prefacing the detailed description of the circuit operation is a brief discussion of the subsystem requirement. This has been included to assist in relating the detailed design requirements to the overall system performance.

A. PCG SUBSYSTEM

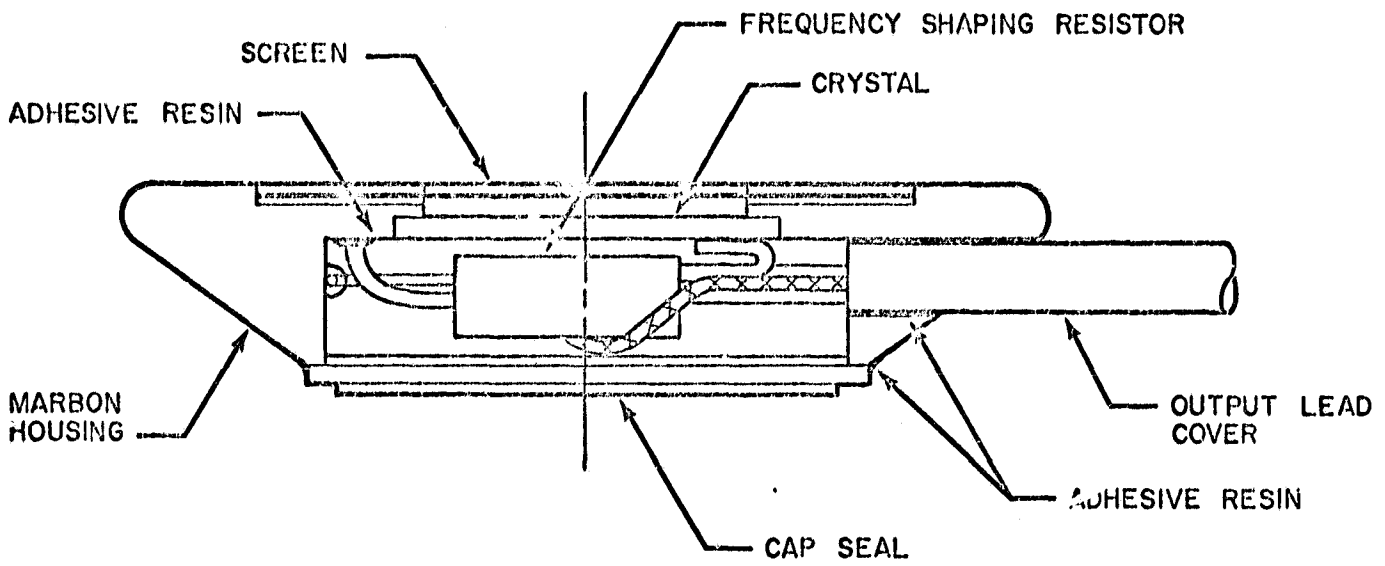
The PCG Subsystem consists of a phonotransducer and a signal conditioning amplifier. Briefly, the phonotransducer is required to detect Korotkow heart sounds and supply an electrical input to the signal conditioning amplifier. The Phonocardiogram Signal Conditioner is required to amplify the input signals and establish the signal bandpass characteristic. The signal conditioner supplies a 0 - 5 volt single-ended output signal and is characterized by a source impedance of less than 200 ohms.

The heart of the PCG transducer is a uranic crystal. Frequency shaping is accomplished by shunting the crystal with a resistance. Since electrically the crystal looks like a capacitance in parallel with a purely resistive component, the inherent time constant of the crystal can be varied by reducing the internal resistive component by means of

series resistance. The high frequency response of the device is extended by careful attention to crystal mounting requirements.

The crystal unit is mounted in a plexiglass assembly (refer to Figure III-1). The crystal and associated components are treated after assembly to protect the device against the effects of humidity. A fine steel mesh protects the crystal face from damage and serves as an ambient pressure vent. The back side of the crystal is vented to ambient pressure by means of fine portholes in the body of the transducer housing. The final assembly is covered with a top cap which is cemented into place with an appropriate resin.

The PCG Signal Conditioner is similar to the EEG Signal Conditioner also being supplied under this Contract. For a detailed description of its operation, refer to Part B. of this section.



AUDIO TRANSDUCER

FIGURE III-1

B. EEG SIGNAL CONDITIONER

A complete EEG Subsystem was originally a part of the contracted effort. A Change in Scope during the program resulted in the elimination of the system requirement. The system originally contracted consisted of two EEG Signal Conditioners and an EEG Electrode and Harness Assembly. The ultimate contractual requirement eliminated the harness and identified the EEG Signal Conditioner as an entity.

The EEG Signal Conditioner is required to detect brainwave signals and to provide specific frequency shaping and input and output impedances. The schematic of the EEG Signal Conditioner is shown in Figure 2 of Appendix C. Functionally, the EEG Signal Conditioner is divided into three main sections:

- Input Isolation and Amplifier
- Intermediate Amplifier
- Output Amplifier

The principal functions of the input amplifier are to provide high input impedance, high common-mode-rejection, and contribute to the overall frequency response. The input amplifier consists of differential compounded amplifiers Q1 and Q2. Separate constant current sources are supplied to the input amplifier, and are shown on the schematic as Q3A and Q3B. The constant current sources play a vital role in common-mode-rejection ratio, both from the standpoint of maintaining balanced operating

biases and providing a high common source impedance as required for high common-mode-rejection. The emitter bypass network is comprised of C1, C2 and R8. The impedance of this network multiplied by the current gain of the input stage is extremely high and results in very little shunting of R1 and R2. The emitter network also establishes the low frequency break-point of the amplifier. It plays an important role in maintaining a low d.c. amplifier gain by virtue of the high d.c. impedance of C1 and C2. The output of the amplifier is generated across R15 and R16 and applied to the intermediate amplifier which follows. A differential high frequency roll-off of 6 db is provided by the RC network consisting of R15 and R16 and C16. It is important to note that the high frequency roll-off characteristic of this network is effective only for differential signals. Because of the difficulty of maintaining precise balances, it is impractical to use a separate filtering capacitor for each of the amplifier output signals. Although it would reduce the amplitude of common signals above the breakpoint, unbalances in the time constants would also result in a differential input signal to the intermediate amplifier.

The intermediate amplifier consists of the Q4/Q6 combination and the Q5/Q7 combination. The intermediate stage is also a differential amplifier and employs emitter feedback for purposes of stabilizing gain and reducing the loading effect on stage 1. Feedback to the emitters from the output at the collectors of Q6 and Q7 is supplied through R18 and R19 to the emitter network consisting of C3, C4 and R17. Additional low frequency roll-off is

obtained as a result of this emitter network. The output of the intermediate amplifier feeds through a π filter where approximately 12 db of additional high frequency roll-off is gained. The output of the filter is supplied to the output amplifier which is operated as a differential d.c. operational amplifier. Signals generated at the collectors of Q8 are supplied to Q9 and Q10, and subsequently to Q12 and Q13. A balanced constant current source, consisting of Q11, provides bias current for the input transistors Q8A and Q8B. The output of the differential amplifier is supplied through CR3 and CR4 through a balanced feedback network to the emitters of the input transistors.

Gain control is introduced by varying the amount of the signal fed back to the input stage. When R38 is adjusted to zero ohms, the divider network consisting of R37, R40 and R39 supplies a small percentage of the output signal through R35 and R36 to the emitters of the input amplifier. The gain of the overall amplifier is therefore maximum. As R38 is adjusted for maximum resistance, a greater percentage of the output signal is supplied to the output amplifiers, and thus the overall output gain is low. The amplifier output is taken from the emitter of Q12 and presented as an output signal at Pin 2 of the output connector.

C. VCG SUBSYSTEM

The VCG Subsystem required for the VCG experiment consists of an electrode and harness assembly containing eight electrodes, a "Frank Lead" signal scaling network, three ECG amplifiers and a control and calibration function. The components of the subsystem developed under Contract were the Frank Lead scaling network, the control and calibration function and the ECG Signal Conditioners. Contracted also as a portion of the VCG Subsystem was a DC-DC Power Converter, which was required to supply regulated prime power to the four subsystems comprising the total instrumentation system. Because the DC-DC Power Converter is not a part of the VCG measurement as such, it has been treated separately in Part E. of this section.

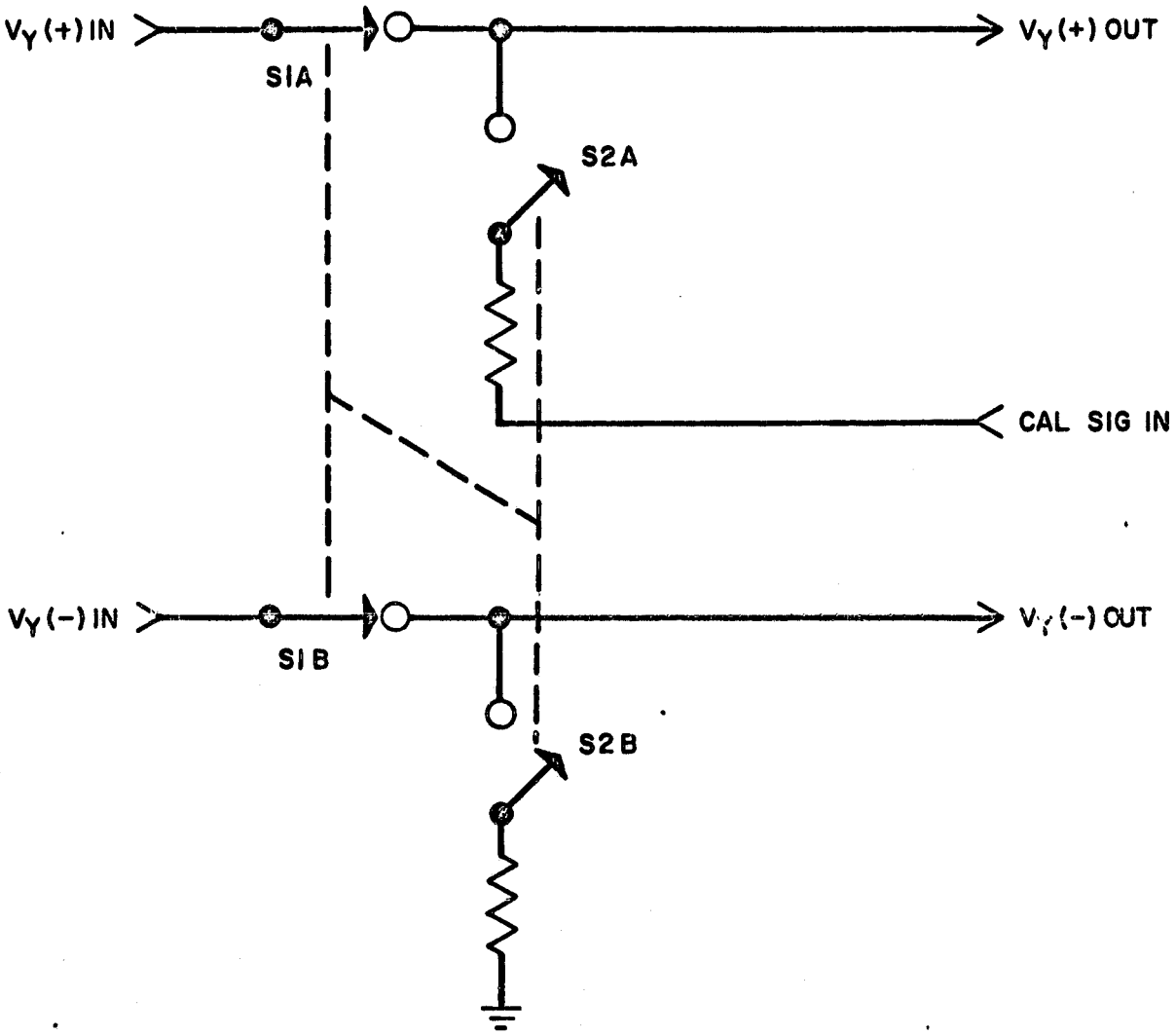
The ECG Signal Conditioners manufactured under this Contract were developed under a previous contract, and therefore only required fabrication and test.

Frank Lead and Input Switch - Circuit Description

Figure 3 in Appendix C (Drawing No. 104380A) shows the Frank Lead and Input Switching Network. At the extreme left of the Figure, the input connections from the eight electrodes to the Frank Lead scaling network are shown. Each of the input signals is referenced to signal common, and by means of the scaling network are converted to a standard amplitude signal, differential in nature, to each of three ECG amplifiers through the switching network shown on the right

half of the Figure. The calibration signal generated in the control and calibrate module is supplied to the switching network at Pin 4 of Output Connector A. A control signal is supplied to the switching network through Pin 2 of Connector B. The switching network appears to be very complicated, primarily because of the number of switching functions required. The V-axis switching network consists of Q5, Q6, Q11, Q12, Q17 and Q18. The operation of the Z and X axis switches is identical to the Y-axis switches, and will therefore not be independently discussed. Figure III-2 shows a simplification of the switching functions. As shown in this Figure, when the calibrate control is actuated, the input signals from the Frank Lead Network are isolated by virtue of S1A and S1B opening. S2A and S2B are simultaneously closed, and the calibration signal supplied to the V-Y (+) output and the V-Y(-) output is returned through S2B to signal common. In the normal mode of operation, S1 is closed and S2 is open, and as a result the calibration signal input is completely isolated from the output signal.

S1A represents Q5 and Q17; S1B represents Q6 and Q18; S2A represents Q11; and S2B represents Q12. The operation of Q11 and Q12 is fairly straightforward. When the control signal is positive, the gates at Q11 and Q12 are biased positive with respect to the source, and the switches are therefore open. Conversely, when the control signal is negative, gate bias is removed, permitting the channel to open.



SIMPLIFIED SWITCHING NETWORK

FIGURE III-2

Because of the differential nature of the Frank Lead input signals and the fact that d.c. signals may be present at the input to the switching network, the implementation of the Q5 and Q6 switches was somewhat more involved. When the control signal is positive, diode CR6 is back-biased. Q18 operates as a source follower. The source of Q18 is therefore maintained only slightly more positive than the gate. In this way, a bias is developed across the gate source junction of Q6, which turns Q6 ON. As a result of the operation of Q18, Q6 is always biased ON by a constant, regardless of the d.c. potential appearing at the source of Q6.

Control and Calibrate Module

The control and calibrate module (Figure 4 of Appendix C) supplies a control voltage to the Frank Lead and input switching network when a manual calibration switch is depressed. It also generates a 1 millivolt peak-to-peak 10 H_z calibration signal which is supplied to the ECG amplifiers through the input switching network.

Manual calibration is enabled by shorting Pin 2 of output connector J2 to the signal common. In the normal mode of operation, with Pin 2 floating, the base of Q4 is returned to -10 volts d.c. through R9 and R21. By virtue of current conduction through R17 and R18, the emitter of Q4 is biased slightly positive with respect to the -10 volt supply. As a result, Q4 base emitter junction is back-biased and the transistor

is in the OFF state. With transistor Q4 OFF, its collector, which is tied to the base of Q1, rises toward the +8 volt supply established by CR4. As a result, Q1 base emitter junction is forward-biased and the transistor saturates, providing a +8 volt control signal at Pin 2 of the input connector J1.

The 1 millivolt peak-to-peak 10 H_z calibration signal is generated in the stabilized multivibrator comprised of Q2, Q3, Q5, Q6 and associated circuitry.

Temperature compensation for frequency and symmetry is provided by Q2 and Q3. Essentially, these are saturating switches which are alternately coupled tc the base network of the multivibrator through steering diodes CR2 and CR3. The output of the multivibrator is taken from the collector of Q6 and fed through R14 through temperature-compensated diode CR10. The amplitude of the calibrate waveform is maintained constant by virtue of CR10. R15, R16 and R_{DV} constitute a divider network which scales the amplitude to the required 1 millivolt peak-to-peak level.

D. ZCG SUBSYSTEM

The ZCG experiment requires measuring both the static and dynamic transthoracic impedances (the dynamic impedance changes being the result of the cardiac activity). Experimentation has suggested the use of a directly measured impedance variation with cardiac cycle, and an impedance variation derived from the rate of change of transthoracic impedance, and a time measurement obtained in part by a PCG measuring system. As a result of these requirements, the ZCG Subsystem provides three outputs. These are:

(a) Base transthoracic impedance.

(b) A direct measurement of impedance variations with the cardiac cycle.

(c) The derivative of the transthoracic impedance.

In addition to providing thoracic impedance data, the ZCG Subsystem requires an internal calibration function which, when manually initiated, will automatically provide prescribed calibration functions for a specific period of time. Due to the complexity of generating dynamic impedance changes, and a suitable derivative thereof, at the point in the system where the thoracic impedance is measured, calibration of the (b) and (c) outputs listed above is provided by generating an internal voltage function which is subsequently operated upon by the respective signal conditioning amplifiers. The base thoracic impedance calibration is derived by automatically switching out the thoracic impedance and switching in its place precision resistors which themselves are automatically varied in accordance with the calibration function requirement.

The ZCG Subsystem consists of five individual modules. Two criteria were used in the selection of the functions within each module. First, an attempt was made to isolate specific subsystem requirements for the purpose of maintaining flexibility and possible future subsystem modification. Secondly, the selection was based on the natural separation suggested by the volume restriction and the desirability of maintaining a constant size for each of the subsystem modules. The five modules which comprise the ZCG Subsystem are:

(a) Current Source

(b) Differential Amplifier and Detector

(c) ΔZ and $\Delta \dot{Z}$ Signal Conditioners

(d) Calibration Function

(e) PCG Signal Conditioner and Phonotransducer

Measurement Technique

Measurement of the transthoracic impedance is accomplished by generating a constant current at a frequency of 122kc through the thoracic cavity and, by means of a differential amplifier, detecting voltage changes which by virtue of the constant current are proportional to thoracic impedance changes. Because of the necessity of avoiding a grounded configuration imposed by other subsystem requirements, the current source and detector is required to be isolated or floating differential systems. The amplitude of

the 122kc voltage detected across the thoracic cavity, and which represents the thoracic impedance, is amplified and converted to a d.c. voltage. From this d.c. voltage, the three output requirements listed above are derived. The base thoracic impedance is presented as a 0 - 5 volt d.c. signal which represents a base thoracic impedance of 10 - 40 ohms, respectively. Cyclic variations of a low level, present on the voltage representing base thoracic impedance and equivalent to plus and minus ½ ohm are amplified by the "ΔZ" amplifier and presented as a 2.5v $\pm$ 2.5v d.c. voltage. The same low level cyclic voltage variations are differentiated, filtered and presented as the derivative output of the system. The $\Delta \dot{Z}$ (derivative) output is biased such that 3.750 volts d.c. represents a zero rate of change of thoracic impedance, 5.00 volts d.c. represents +3 ohms per second change in thoracic impedance, and 0 volts d.c. represents -7 ohms per second rate of change of thoracic impedance.

Current Source

The 122kc current source is shown in Figure 6 of Appendix C. The current source module consists of crystal oscillator Q1, an amplitude regulator comprised of Q2, Q3 and Q4 and an output driver stage consisting of Q5 and Q6.

The operation of this oscillator is well-known and a detailed discussion of its operation and analysis can be found in any standard circuits text-book.

Resistor R3 and capacitor C4 serve as a decoupling filter to isolate the oscillator from the remaining current source circuitry and the +10 volt d.c. supply lines.

The output voltage of the oscillator is fed through C6 to the base of Q2. Inductor L4 serves the purpose of maintaining the bases of Q2 and Q3 at an equal d.c. voltage and providing a reactive load across which the oscillator output voltage is generated. The base of Q3 is maintained at a.c. ground by virtue of capacitor C7. As a consequence, the base of Q2 is driven positive and negative with respect to a.c. ground at a 122kc rate. On the positive cycle of the input signal at the base of Q2, Q2 behaves as an emitter follower. The emitter of Q3 is driven positive with respect to its base and is therefore cut-off. During the negative alteration of the voltage at Q2 base, transistor Q2 is cut-off due to the fact that the voltage at R7 is not permitted to follow. The voltage at R7 with respect to ground is constrained to follow the base voltage of Q3, by virtue of the emitter follower operation of Q3 during this portion of the cycle. The voltage across R7 and R18 is maintained constant through the combined action of CR1, Q4 and Q3. The junction of R8, R18 and CR1 is maintained at a.c. ground potential by C9. The voltage generated across CR1 is coupled through emitter follower Q4 to the base of Q3, and subsequently to the junction of Q3 emitter and R7 as a result of the emitter follower operation of Q3. The temperature stable voltage generated at

the base of Q4 by CR1, with respect to the junction of R18, R8 and C9 by CR1, is transferred to the R7/Q3 emitter junction as a temperature stabilized voltage as a result of the temperature compensating effect of the Q3 PN junction and the Q4 PN junction. The overall result is a constant temperature stable voltage across R7 and R18. As a consequence, a constant Q3 emitter current results. In view of the fact that Q3 is a high gain transistor, a constant collector current is thereby achieved. Because Q3 is alternately conducting and non-conducting at a 122kc rate, the constant current referred to is in fact a current pulse of constant amplitude supplied to the tuned collector circuit of Q3. The pulse of constant amplitude supplied synchronously to the tuned connector circuit results in a constant amplitude 122kc sinewave across the tuned circuit. The upper end of the tuned circuit is maintained at a.c. ground by C5. As a consequence, the output to the driver stage at Q5 base is a constant amplitude with respect to a.c. ground.

The driver stage, consisting of compounded amplifiers Q5 and Q6, presents an extremely high input impedance in order to avoid variations in the tank circuit Q resulting from gain variations in the driver stage over the temperature range. The voltage at Q5 base is transferred to a constant current source as a result of compounded follower amplifiers Q5 and Q6, and is supplied to the primary of the output transformer. The output transformer is balanced and shielded to

provide an isolated constant current drive through coupling capacitors C16 and C17 to the electrodes, which are placed across the thoracic cavity.

Cabling and Interface Requirements

Although the cabling from the current source module to the thoracic cavity and back to the differential amplifier and detector is not considered as a separate subsystem, a separate discussion of the requirements is necessary to a full understanding of the equipment operation.

The ZCG Subsystem modules are located at the mid-section of the subject. The current drive to the thoracic cavity is applied between the subject's neck and a point near the lower end of the thorax. An interconnecting cable is therefore necessary between the current source module and the point of application on the body. Similarly, cabling is required from the detection points located between, and adjacent to, the current source electrodes to the differential amplifier and detector module. Two very significant problems arise as a result of the requirement for interconnecting cabling due, primarily, to the relatively high frequency of the carrier. The first of these problems is that of maintaining high impedance levels required for system accuracy in the presence of significant cabling capacitance. Maintaining high impedance is important at both the current source electrodes and the

detector electrodes, since minimum impedance levels are necessary to maintain required system accuracy. The second problem is associated only with the differential amplifier and detector, and is related to the common-mode-rejection requirements of the system. In view of the fact that the system is required to operate in an isolated, truly differential mode, common-mode signals are expected to be present at the detector electrodes. Any unbalance that occurs as a result of unbalanced cabling between the points of detection and the differential amplifier will be introduced as a system error.

These problems were solved differently for the current source than for the differential amplifier and detector because of differences in affected parameters and required performance. A more detailed discussion of these problems and the reasons underlying the choice of implementation are presented elsewhere herein.

To maintain the high output impedance required of the current source, the interconnecting cable capacitance is made a part of a tuned output circuit. At resonance, the output impedance at the electrodes is limited to the dissipative character of the output circuit and the inherent output i dance of the driver stage.

To maintain high input impedance and to eliminate unbalances resulting from differences in cabling capacitances to the differential amplifier, a different approach was used. In this case, the shields are driven

with the input signals through low impedance amplifiers within the detector module. The shunting effect of the cabling capacitance is thereby reduced to an acceptable level.

Differential Amplifier and Detector

The following functions are performed by the differential amplifier and detector module (Figure 9 of Appendix C):

- Impedance Transformation at Unity Gain
- Shield Drive
- Broadband Carrier Gain
- Narrow Band Carrier Gain
- Carrier Detection
- Modulation Data Amplification

Impedance transformation is accomplished at the input amplifier, which consists of Q1, Q2 and Q3. The input stage is a differential field effect transistor supplied by constant current sources Q3A and Q3B. The field effect transistors are biased to signal common through 1 Meg resistors R2 and R3. The signals at the sources of the source followers Q2A and Q2B are applied to both the shield drive amplifiers and the broadband carrier amplifiers. The shield amplifiers actually perform the dual function of providing drive to the shields and providing a bootstrap drive to

the drain circuits of the input transistor Q2. Bootstrapping of the input transistor is required to reduce gate drain junction capacitance, which significantly lowers the input impedance of the amplifier at the carrier frequency. The shield drive amplifiers receive the input signal from the source of Q2 at the bases of Q6 and Q19.

Since the operation of both shield drive amplifiers is identical, only the operation of the amplifier consisting of Q4, Q5 and Q6 will be discussed. The signal at the base of Q6 is coupled through level changing diode CR2 to the base of Q4. A high impedance emitter circuit and the constant current drive source for CR2 is provided by Q5 and associated circuitry. The d.c. operating point of Q5 is established by resistor divider network R11 and R12. The collector current is established at a fixed level by virtue of the fixed voltage at the base of Q5 and the emitter resistor R8. The signal generated at the base of Q4 is coupled to the emitter circuit and developed across resistors R57 and R6, while the shield and bootstrap drive is supplied from the junction of R57 and R6. R57 serves to inhibit oscillation of the shield drive amplifier. The drive signal thus derived is supplied directly to the input shields at Pin 2 in the case of the amplifier junction described, and Pin 1 of its counterpart. This same signal is supplied to the emitter circuit of Q1. Transistor Q1

is compounded with the input transistor Q2 to increase the transconductance of the input amplifier. The derived signal fed to the emitter circuit of Q1 appears at the drains of transistor Q2 as in-phase and of amplitude equal to the input signal appearing at the gates. R58 in the base circuit of Q1B is a potentiometer, provided for the purpose of balancing the amplifier to maximize common-mode-rejection of the composite input stage.

The broadband carrier amplifier consists of transistor Q7, Q8 and Q9. Q9 represents the constant current source for the differential amplifier comprised of Q7 and Q8. Q7 and Q8 represent a composite amplifier, and are required to increase the open loop gain of the circuit to insure stable closed loop gain. In this particular amplifier, the loop is closed and the gain fixed by virtue of emitter degeneration introduced by R15 and R19. RC networks R61/C17 and R62/C18 are compensation networks which prevent high frequency oscillation of the amplifier. The amplified signal as generated across R13 and R17 is coupled through capacitors C4 and C5 to the next gain stage.

The following stage is a narrow band amplifier consisting of Q10, Q11 and Q12 and associated circuitry. The amplifier is biased by resistor network R23, R26, R27 and R28. Amplifier Q11 is supplied

by constant current source Q12, and degeneration is provided by resistors R30 and R32. Amplifier Q10 is direct-coupled to amplifier Q11 and serves the dual function of providing a high collector biasing impedance and adding the differential signals appearing at the collector of Q11. The collector load on Q11 consists of the resonant circuit comprised of L1, C11 and C12. Capacitor C10 provides d.c. isolation while resistor R36 is selected to establish required circuit Q. The voltage generated across the resonant circuit is coupled through R38 to the input of the impedance transforming amplifiers Q16 and Q13. The latter provides a source of low impedance drive to the detector while presenting an input impedance sufficiently greater than R36 to prevent resonant variations in resonant circuit Q with changes in environment.

The detector circuit consists of diode network CR6 and CR7 in conjunction with a filter consisting of R43 and C14. The input signals are coupled through the detector to C13 to the cathode of CR6. The anode of CR6 is biased at approximately +0.6 volts d.c. by virtue of current supplied through R42 to CR7. During the positive alteration of the carrier diode, CR6 is back-biased and the signal is fed to the filter network consisting of R43 and C14. During the negative alteration, CR6 becomes forward-biased and charges C13. The d.c. reference level is maintained at ground

potential by virtue of the compensating effects of CR6 and CR7. During the next positive alteration, the charge accumulated during the negative alteration is added, and thus the peak-to-peak carrier level is supplied to the filter network. The low pass RC filter integrates the input signal and supplies an input signal proportional to the carrier amplitude to the data amplifier Q14. The breakpoint of the low pass filter is selected to meet the data bandpass requirement and the carrier rejection requirements of the system.

When the transthoracic impedance is 10 ohms, the system is required to supply a 0 volt output signal. However, a transthoracic impedance of 10 ohms results in a finite carrier amplitude and is consequently detected and fed to the output amplifier. To off-set this voltage, a d.c. off-set voltage of opposite polarity is summed with the input signal at the amplifier input.

The data output amplifier consists of transistor Q14 and Q15. The output amplifier is a differential operational amplifier with open loop gain provided by Q14 and Q15B. The feedback network establishing the output gain is comprised of R60, R52 and R53. This amplifier configuration is fairly standard and conforms to standard operational amplifier techniques. The amplifier output

is coupled through Pin 6 and presented as the base transthoracic output signal. The output is also coupled through Pin 7 to the calibrate module, and subsequently to the ΔZ and $\Delta\dot{Z}$ amplifiers.

Throughout the circuit the supply voltage is decoupled as required for proper circuit performance. R22 and C3 are examples of these decoupling networks.

ΔZ and $\Delta\dot{Z}$ Output Amplifiers

The output amplifier module (Figure 8 of Appendix C) consists of five separate functions. These are:

- ΔZ Amplifier
- ΔZ Recovery Circuit
- $\Delta\dot{Z}$ Amplifier
- $\Delta\dot{Z}$ Filtering and Output Amplifier
- $\Delta\dot{Z}$ Signal Limiting Circuit

The ΔZ amplifier consists of an operational amplifier connected in the non-inverting configuration. The amplifier per se, consists of Q3, Q4, Q7, Q8 and Q19. Frequency compensation is provided by C6 and R19. The input signal is coupled through C4 to the gate of Q4B. The output signal is taken from the collector of Q8 and supplies an output through Pin 7 of J1. The output signal is fed through the feedback network, which consists of R24, R20, R55, C7, C16 and C18, to the gate of Q4A. The operational amplifier loop is thus closed.

Because of the extremely low time constants required to achieve the desired low frequency response of the ΔZ amplifier, transient recovery was a significant problem. To improve the recovery time, a sensing circuit consisting of Q12, Q13 and Q16 was incorporated, which closes FET switch Q11 in the event of either an over-voltage or under-voltage condition at the output. When Q11 is closed, it shunts R6 with approximately 1k, thereby reducing the time constant and thus improving the recovery time. The operation of the sensing circuit is fairly straightforward, however, it will be briefly discussed. When the signal at the output exceeds the 5 volt level, CR4 conducts and saturates Q16. When Q16 is saturated, base current is supplied to Q12. Q12 is therefore turned ON, connecting the cathode of CR2 to the supply voltage. The gate circuit of Q11 is isolated and the field effect channel is unrestricted. In the event of an under-voltage, Q13 is saturated. This supplies a back-biasing voltage to Q12. When an under-voltage condition occurs, current is conducted through R30, R31, CR3 and CR7 to the amplifier output. As a result, the voltage at the base of Q12 is lowered and Q12 goes into conduction. CR2 is therefore again back-biased and the field effect switch, Q11, closes.

The $\Delta\dot{Z}$ amplifier is an operational amplifier connected in the inverting configuration. This amplifier is identical to the ΔZ amplifier described above. Differentiation is accomplished by means of the RC

network consisting of C3, R42, C13 and R7. C13 and R42 are included for frequency compensation purposes and they were choosen so as not to affect the differentiation of the input signal resulting from the C3/R7 combination. The derivative amplifier is biased at Q6A gate by means of a divider network supplied from Zener diode CR1. The output of the derivative amplifier is supplied to a high filter which provides the required high frequency roll-off characteristics. The output amplifier is an operational amplifier consisting of Q14, Q15, Q17, Q18 and Q21. It is connected in the inverting configuration with feedback supplied through R38 to the amplifier input.

Diodes CR6 and CR5 limit the excursion of the output signal to between approximately -0.5 volts and +5.5 volts.

ZCG Calibrate Module

The ZCG calibrate module (Figure 7 of Appendix C) performs the following functions:

- Thoracic Impedance/Calibrate Impedance Switching
- Z Calibrate Resistance Cycling
- Calibration Initiation
- ΔZ, $\Delta \dot{Z}$ Calibrate Waveform Generation
- Data/Calibrate Signal Switching

Relay K1 switches the current source drive between the thorax and the calibration resistances network. Relay K2 switches the differential amplifier between the thorax and the calibration resistance network. These relays are actuated by the relay driver circuits Q8 and Q9. Relay K3 is automatically cycled by the multivibrator circuit to provide a step variation in the calibration resistance. The resistance network is designed to simulate precise thorax impedance.

The positive voltage supplied to the junction of R16 and R30 causes forward conduction of CR8, and as a consequence the Darlington combinations Q8 and Q9 saturate and actuate relays K1 and K2.

The positive control voltage supplied to the junction of R16 and R30 back-biases CR13 and enables the multivibrator consisting of Q11 and Q14. K3 is therefore alternately actuated and deactuated.

Calibration is required to be initiated when terminal A2 is grounded. Prior to initiation of calibration, Q1 is conducting by virtue of current supplied to its base through R1. The collector of Q1 is at a relatively low

potential with the result that CR2 does not conduct. As a consequence, CR4 and CR5 are OFF. From the collector of Q4, a positive voltage back-biases CR4 isolating the gate of Q3. Switch Q3 is therefore closed and the detector signal is applied to the ΔZ, $\Delta \dot{Z}$ amplifiers. A negative voltage is applied to the anode of CR3 which results in a negative bias across the source gate junction of Q2 causing switch Q2 to open, and thereby isolating the calibration signal at R27 from the ΔZ and $\Delta \dot{Z}$ amplifiers. When terminal lead 2 is grounded, Q1 is turned OFF and Q4 and Q5 are turned ON. CR4 therefore conducts and reverse-biases Q3, turning if OFF. CR3 is back-biased isolating the junction of Q2 and therefore turning it ON. The positive voltage at the collector of Q5 back-biases CR7 and enables the calibration waveform generator. The calibration signal generated at R27 is supplied through switch Q2 to the ΔZ, $\Delta \dot{Z}$ amplifiers.

The calibration waveform generator is an astable device comprised of Q6, Q7 and Q10. A constant current is supplied by the temperature-compensated composite transistors identified as Q7. This constant current generates a linearly rising voltage across CR2 and CR3 and is supplied as the output signal. When the output signal rises slightly above ground potential,

transistor Q10 conducts. The positive swing of the output voltage is thus limited by the base emitter voltage drop of Q10. The negative voltage drop at the collector of Q10 is coupled through CR4, back-biasing CR6. Q6 opens permitting C2 and C3 to be recharged through R14. When the voltage at the junction of C4 and R21 subsequently rises sufficiently to bring Q6 into conduction, CR5 conducts and establishes a fixed potential at the junction of C2 and C3. The drop at this point is coupled through these capacitors turning Q10 OFF. The output voltage rises linearly again until Q10 is again brought into conduction. The cycle repeats continuously. The output waveform is coupled through source follower Q12 and divider network R24 and R27, and subsequently through switch Q2 to the ΔZ and $\Delta \dot{Z}$ amplifiers. Source follower Q12 is coupled with Q13 to increase transconductance.

E. DC-DC CONVERTER

The DC-DC Converter (Figure 5 of Appendix C) provides a plus and minus regulated 10 volt d.c. supply voltage and a +10 volt unregulated d.c. supply voltage. The DC-DC Converter consists of a preregulator, an inverter, two rectifier circuits and two voltage regulators. Additionally, it contains RF and AF filtering on both the input and output power lines as required to perform to the Specification in the presence of MIL-I-26600 requirements.

The preregulator is a switching type regulator which is incorporated to stabilize the supply voltage to the power inverter and reduce the dynamic range required at the output of the voltage regulators. MIL-I-26600 imposes a 3 volt rms audio ripple component on the input supply voltage. In the absence of a high efficiency preregulator, either a filtering network of unpractical size or dissipation type regulation would be required. The switching preregulator consists of Q1, Q2 and Q3, and is designed to provide a reference voltage at the emitter circuit of the inverter transistors with respect to the prime power line. The voltage supplied to the inverter is sampled at the base of Q3 across the divider network consisting of R5, R6, R7, CR27 and CR28. The voltage at the emitter of Q3 is stabilized with respect to the prime power line by Zener diode circuit CR2 and R4. Variations in the output voltage alter the current supplied by Q3 to the base circuit of Q1, and therefore changes the duty cycle of the switching transistor Q2. When the output voltage causes the

voltage at Q3 to drop below the point required to turn Q3 ON, Q3 supplies current to Q1 base and saturates Q1. When Q1 saturates, it reduces the bias on Q2 below the conduction point and Q2 opens. Energy stored in L1 discharges through CR?6 and through the output circuit. As the energy is dissipated, the output voltage drops below the point required to sustain conduction of Q3. When Q3 turns OFF, transistor Q1 turns OFF, which in turn permits base current drive to Q2 through R1. Q2 conducts and energy is again supplied to the output circuit and begins to build up again in L1. When the output voltage again causes Q3 to conduct, the cycle is repeated. Positive feedback to insure regenerative switching is supplied by the series R2/C2 network. Diode CR1 is included to prevent damage to the circuit in the event input power is incorrectly applied.

The inverter circuit is comprised of Q4, Q5 and associated circuitry. The inverter is a standard square loop transformer coupled circuit and is thoroughly described in standard circuit text. The converter operates at a frequency of approximately 10kc. This frequency was choosen as a result of both power dissipation and harmonic sensitivity of the circuits which it supplies.

The rectifiers are of the bridge type and are identical for both the plus and minus supplies. The output of the rectifiers are supplied to the output regulators which are identical in design. The output regulator is comprised of Q6, Q8, Q9, Q10, Q11 and Q12. The output voltage is sensed

by differential amplifier Q12 which is referenced to a stabilized voltage generated by CR14. An increase in the output voltage increases the voltage at the input circuit to Q12. This voltage change is amplified and supplied to Q11 base. Q11 increases conduction which results in a decrease in base current drive to Q10 by virtue of the fact that the current supplied by Q6 is constant. The series regulator composite consisting of Q8, Q9 and Q10 therefore reduces the voltage supplied to the output circuit. Short circuit current protection is provided by the combined operation of Q6, Q7 and Q20. When the output current exceeds a given value, transistor Q7 is biased ON by virtue of the voltage drop across series sensing resistor R15. As Q7 goes into conduction, Q20 is forced into conduction which reduces the voltage at the emitter of Q6 sufficiently below the base reference voltage to cut the transistor OFF. The current drive to the regulator circuit is thus interrupted and the composite regulator of Q8, Q9 and Q10 opens.

Unregulated 10 volt d.c. is generated by half-wave rectification and filtering in the CR25/C16/R47 network.

The package configuration of the DC-DC Converter is fairly involved, and therefore warrants a detailed discussion. The package configuration reflects two primary problems related to the design and performance of DC-DC Converters. The voltage supplied to the converter has superimposed upon it transients and radio frequency interference in addition to audio

frequency ripple. The primary concern is the radio frequency voltages present on the input line. These radio frequency voltages are inductively, capacitively and electromagnetically coupled into the regulated output lines. To eliminate coupling from input to output, the converter is divided into three sections. The first section contains a 360° RF filter and provides shielding between the input and the converter circuitry. The second section consists of that area either side of the center shield. The third section contains a 360°RF output filter as well as low frequency bypass capacitors, and provides a shield between the converter circuitry and the output lines. Double shielding and filtering is thereby provided to eliminate RF energy from being transferred from the input to the output.

The second major problem involves switching transients inherent in power inverters. To eliminate the switching transients to as great an extent as possible, an internal shield separates the switching regulator and the inverter from the output analog regulators.

The converter circuitry is encapsulated in place and after curing is provided with an RF seal by sandwiching Ecco-shield material between the main package assembly and both covers. The final unit then provides RF shielding both externally and internally.

IV DEVELOPMENT HISTORY

The development history has been included to provide a more detailed view of the subsystems' development, particularly in those areas where problems were encountered. Where appropriate, a view of the Systems Engineering effort required has been included.

Reference to a specific period during which the problems discussed occurred has been minimized, however, the chronological order of the development has been maintained.

A. PCG SUBSYSTEM

Development of the PCG Subsystem began with a detailed design of the microphone assembly. The microphone assembly received the major design emphasis in view of the fact that the signal conditioner was to be a modified ECG and would therefore require relatively little development.

In January of 1966, a little over a month after development began, a determination was made by NASA that the Marbon material used in the microphone housing was not an approved Apollo material because it outgassed under certain of the Apollo environmental conditions. A materials investigation was initiated to determine a suitable substitute for Marbon. Plexiglass was ultimately selected and microphone housing assembly procedures were modified as required.

Development of the PCG transducer and signal conditioner continued. During evaluation of the PCG transducer, it was noted that a change was occurring in the sensitivity and output characteristics. An investigation into this problem conducted by Spacelabs personnel and a Materials Consultant revealed that the plexiglass material was dimensionally unstable. Subsequent study indicated that the dimensional instability was significant only at elevated temperatures. A search for a different material indicated that more dimensionally stable materials were not suitable for use on the Apollo Program primarily because of outgassing characteristics. As a consequence, the maximum operating temperature was reduced by NASA to 120°. Performance of the transducer during and immediately following the cold environmental test was within the Equipment Specification. However, after allowing the transducer to completely return to room temperature, a marked decrease in the sensitivity was noted. In view of the fact that the transducer had indeed failed the test, further qualification was discontinued and the Technical Monitor notified. Investigation showed that the bond between the plexiglass housing and the microphone cyrstal had partially separated. A Materials Consultant was called in to investigate the problem. His conclusions were that there may be some continued difficulty maintaining specific sensitivity after exposure to varying thermal environments, due to the fact that the plexiglass material is dimensionally unstable. He suggested a different bonding material and suggested that should we continue to experience this

difficulty, sensitivity variations could probably be minimized by modifying the design of the microphone. His recommendations were discussed with the Technical Monitor and it was jointly agreed that we should employ the new bonding material and not entertain any thought of redesigning the microphone at this time. The transducer was assembled using the new bonding material and subjected to a very severe temperature and humidity test at Spacelabs facility. The transducer successfully passed the temperature test; however, a problem relative to humidity was noted. The transducer was disassembled and investigation showed that moisture had gained entry into the transducer around the cable sleeving. Steps were taken to correct this problem. The transducer was then subjected to design acceptance tests with the burn-in requirement deleted by direction of NASA.

Later in the program, additional delays were experienced due to the problem of establishing the nutrient character of the transducer components. Evaluation of a special varnish was made to determine its acceptability in preventing fungus.

This problem was ultimately resolved (1) and the transducer successfully completed qualification testing. Subsequently, the flight PCG Subsystems were manufactured, acceptance tested and delivered to NASA.

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(1) Direction was received from NASA as to the course of action to be taken concerning the treatment of the suspect-nutrient bonding material used in the transducer. It was determined that a thermal cure cycle was necessary to render the material acceptable. The curing cycle was made a part of the fabrication process.

B. EEG SIGNAL CONDITIONER

Development of the EEG Signal Conditioner was relatively straightforward when compared with development of the other contracted subsystems. Although technical problems were encountered, the solutions were readily determined.

The only significant problem worth discussing involved the physical packaging of the signal conditioner. The lead routing resulted in capacity feedback to the amplifier input, and as a consequence unbalanced and decreased the input impedance of the signal conditioner when operating in the presence of high source impedances.

The initial units, during the testing of which this problem became evident, were set aside and the signal conditioner was repackaged. The signal conditioners produced subsequently were extensively examined for any evidence of a similar problem with negative results.

C. VCG SUBSYSTEM

In accordance with the Contract Statement of Work, development of the VCG Subsystem began with the Systems Engineering effort. The objective of the Systems Engineering effort was to establish overall system configuration and design requirements as determined both by the specific Contract Specification and the general operational requirements. The elements of this task consisted of:

(a) Signal conditioner configuration and mounting location.

(b) Electrode placement and electrode cable routine.

(c) Electrode cable shielding including the type, extent, and termination thereof.

(d) The means by which the electrode proper and cable should be interfaced.

(e) The overall configuration of the VCG harness assembly from the standpoint of subject comfort, ease of instrumentation, minimum material abuses, and equipment storage.

(f) The means by which the harness assembly should be connected to the signal conditioner cable assembly.

(g) Definition of optimum system interconnecting cabling requirements for the various possible configurations.

Initial Systems Engineering was based on the equipment being mounted to the spacecraft bulkhead. The interface and mounting requirements were discussed jointly with North American and NASA personnel in an effort to establish basic design criteria. As a result of this discussion, a bulkhead-mounted configuration and associated brackets and cabling were

established as the basic configuration. Systems Engineering and design in accordance with these requirements was subsequently undertaken and concluded. During this effort, design of the subsystem circuits was being accomplished in accordance with specific equipment requirements.

Subsequent to this effort and as a result of a meeting with NASA personnel, it was determined that a more flexible configuration would be in the best interests of the Program. The desired changes were definitized in an Engineering Change Proposal submitted by Spacelabs. Subsequently, a Contract Change Notice was issued by NASA which essentially reflected the content of the Engineering Change Proposal. Design changes to reflect the Contract Modification were initiated. Upon completion of the redesign effort, subsystem breadboards were delivered both to NASA and the Contract Principal Investigators for evaluation. Certain changes were requested by the Principal Investigator to make the system more compatible with the objectives of the experiment, Subsequent evaluation and changes resulted in an acceptable configuration and overall performance requirement.

Following approval of the basic design, the production effort was launched. The product design, packaging, evaluation and testing proceeded in a routine manner.

D. ZCG SUBSYSTEM

The first phases of the program required a general Systems Engineering effort. Systems Engineering was necessary to establish specifications for certain portions of the equipment. The term "Systems Engineering" as used here includes study effort on particular phases of the desired performance as well as the general hardware engineering considerations. As the Contract was written, Spacelabs was to investigate electrode configurations and to attempt to determine an electric model for the electrode-thorax system. Other specific functions of the system were not given a set of specifications in order that the Contractor could exercise perogative in optimizing the system. The Subsystem Engineering effort consisted of specific hardware design considerations and study in the following areas.

(a) Electrode placement and electrode cable routine.

(b) Cable shielding requirements and cable type.

(c) Electrode and cable interface considerations.

(d) The overall configuration of the ZCG harness assembly with particular attention to subject comfort, ease of instrumentation, accuracy of placement, minimum material abuses, and equipment storage.

(e) Definition of optimum system interconnecting cable requirements.

(f) Determination of current source requirements including output impedance, balance requirements, dynamic range, amplitude stability, and noise.

(g) Calibration requirements for the system including accuracy and means of implementation and the type of calibration waveform that would be most meaningful to the equipment users.

(h) Phonocardiogram and Phonocardiogram Transducer requirements.

Early in the program, analysis was performed to determine the feasibility of a system which would meet the Contract and perform all functions adequately in application. The net result of that analysis was that in almost all areas new concepts had to be developed to meet the requirements.

Throughout the program, the design of these circuits was continually revised in an attempt to improve their performance. This is particularly true of the detector amplifier and the peak detector. During the early phases of the program, it was determined that crystal-controlled signal source would be required to achieve the accuracies desired. Also, a new harness configuration was developed which was more consistent with equipment performance requirements and optimum manufacturing techniques.

A Design Review Meeting was conducted with the Principal Investigator and NASA personnel to discuss developments to date and to establish desired performance objectives.

The results of the initial development of the current source, configured consistent with package size and power constraints, indicated that the problem of obtaining sufficient isolation and balance at the output, to be

consistent with desired system accuracy, would be extremely difficult if not impossible, and that the means of grounding the electrode system would have to be determined and used as a basis for specifying the characteristics of the interface performance. During this meeting, a need was established to alter the Experimentor's equipment to eliminate errors introduced into the measurement due to capacitive degradation due to output impedance. A significant change in the ZCG interface requirement resulted from this meeting. It was determined that the system should be capable of operating with either a grounded or an ungrounded interface, and further that the ground point may occur anywhere on the subject.

Other results of the meeting included the following changes:

- Increased Frequency Response
- Interface Electrode Impedance Magnitudes
- Additional Calibration Requirements

A formal Design Review was held at Spacelabs on April 13 and 14, 1966. During the course of the Design Review, it was concluded that insufficient information existed on the effect on system accuracy of the grounding scheme. As a result, more detailed examination of this area was considered necessary, and the object of that investigation was to determine the effect on common-mode-rejection voltages generated at the electrodes by moving the ground point around, and what the effects of eliminating that ground would

have fror the standpoint of the grounds provided by the other subsystems. It should be noted that at this point in time a definition of the interface was still not available, although considerable effort toward determining that interface had been expended by the Principal Investigator and Spacelabs.

Development continued up to the time in May when a technical meeting was held at MSC. During that meeting Spacelabs proposed specific changes in the ZCG Subsystem, and as a result Engineering Change Proposal No. 5 was generated.

NASA Modification No. 3, which contained essentially the information in Engineering Change Proposal No. 5, was received by Spacelabs in August of 1966. Redesign of the system along these lines was initiated and progress toward completion of the Contract went along at a fairly acceptable rate. There were, however, outstanding problems in the area of the electrode interface which required continuing investigation on the part of Spacelabs. A detailed discussion of these problems in included in Section V.B.

Contract Modification No. 3 reflected a set of requirements which resulted from several technical conferences. The ZCG Subsystem was redesigned in accordance with these requirements and breadboard systems were delivered to the Principal Investigator and NASA for evaluation. Subsequent modification and evaluation occurred, followed by design approval.

The prototype system successfully passed design verification testing and was delivered to NASA. Subsequent to production of the qualification units, a problem was noted in the subsystem current source. Specifically, the output impedance was marginal. In an effort to correct this problem, changes in the output transformer were investigated and ultimately a new transformer was incorporated. Production of the ZCG Subsystem continued until, mid-way in this effort, another problem related to the current source was discovered. The output level of the current source appeared to be unstable with time and extensive investigation was conducted which included the evaluation of different design approaches and materials. Technical consultants were utilized in an effort to find a solution to the problem. A satisfactory explanation of the drift phenomena could not be found, and transformers not exhibiting the drift problem and acceptable relative to other system requirements could not be manufactured.

The problem was discussed with NASA personnel and in view of the fact that the drift noted was, from an operational standpoint, insufficient to degrade the experiment, further action was not considered necessary.

V TECHNICAL PROBLEMS

A. VCG SUBSYSTEM

Although there were many technical problems encountered in the development of the VCG Subsystem, the most outstanding one was implementing the calibration requirement. As originally contracted, the VCG Subsystem incorporated calibration in the ECG Signal Conditioners as provided in ECG equipment developed and manufactured under separate contract. Because calibration at the mid-point of the ECG amplifier involves the risk that elements of the signal conditioner ahead of the calibration circuitry do not remain constant, it was recommended by the Principal Investigator to introduce the calibration function at the input of the amplifier.

Because of problems encountered in the implementation of the calibration function at the input terminal of the amplifier, attempts were subsequently made to calibrate through the Frank Lead Network. Again, technical requirements were such that practical implementation was not possible, and as a result the calibration was ultimately introduced at the amplifier input by compromising certain performance characteristics.

The principal difficulty encountered in implementing the ultimately choosen calibration technique was that of the introduction of d.c. transients. The transient was generally coincident with approximately 10% of the physical data being processed in view of the fact that the calibration was being introduced automatically on a periodic basis. The compromised performance

involved the elimination of automatic calibration function. The data lost as a result of transients in terms of percentage was in the function of the frequency where manual calibration was initiated. In view of the fact that longer intervals between calibration was considered acceptable relative to subsystem performance, the percentage of data lost was reduced to an acceptable level.

Introducing the calibration function at the input of the amplifier terminals resulted in problems in the following areas:

- Common-Mode-Rejection
- Switch Requirements
- D.C. Transients

The common-mode-rejection requirement for the subsystem was 100 db. This included the degradation through the Frank Lead Network and the performance of the amplifier itself. To introduce the calibration function at the input terminals of the amplifier required providing a switching function which introduced a precisely known voltage in place of the Frank Lead output signals. The input terminals of the amplifier constitute the most sensitive portion of the subsystem. If the circuitry employed to introduce the calibration voltage exhibits finite impedance, it will not only result in a reduced effective amplifier input impedance, but will tend to degrade the common-mode-rejection ratio. The degradation of common-mode-rejection ratio is a result of three principal mechanisms: first, the maximum permissible

unbalance in the Frank Lead Network for a given overall common-mode-rejection ratio is directly proportional to the impedance into which the Frank Lead Network is terminated; secondly, the unbalance in the shunt character of the circuitry incorporated to apply the calibration voltage results directly in the generation of a differential signal in the presence of common-mode signals; and third, unbalances in the series character of the circuitry incorporated to apply the calibration signal to the input of the amplifier reduces the permissible unbalance in the Frank Lead Network. Since there is a practical limit on the degree of balance obtainable in the Frank Lead Network, any additional unbalance series impedance can only serve to reduce the common-mode-rejection ratio.

A detailed examination of the common-mode-rejection problem relative to unbalances at the amplifier input has been included in Appendix D. Had it been possible to use mechanical relays, the problem of common-mode-rejection would never have been a matter of concern. However, the reliability in terms of Mean Time Between Failure for mechanical relays at the use rate under consideration was unacceptably low. As a consequence, it was necessary to resort to solid-state switching. The use of solid-state switching required a consideration of several potential problem areas. Solid-state switching devices exhibit a finite and measurable ON and OFF impedance. The effect of these impedances relative to common-mode-rejection was mentioned above and a detailed analysis is included in the Appendices.

Inasmuch as it is not the magnitude of the series impedances that represents the significant problem, but rather the difference in that absolute impedance, it is important that the differences that exist in terms of percentage relative to the other series impedances in the circuit be held below a given minimum. Associated with the difference in these impedances is the ON-resistance variation with temperature. There is a marked change with temperature and this requires a matching characteristic in order to maintain minimum common-mode-rejection levels.

Problems associated with solid-state switching in this application were:

- Common-Mode-Rejection
- ON-Resistance Variation
- Noise Feedthrough
- Capabilities Requirements
- Calibration Signal Isolation

Because of the finite character of the switch junction impedances, there was a problem relative to noise feedthrough. The noise referred to the input of the signal conditioner is typically less than 10 microvolts peak-to-peak. Connecting additional circuitry at the input terminals, which in turn is connected to control and waveform generation functions, presents the problem of feeding noise through to the input of the amplifier and degrading the overall performance of the system.

The gate voltage requirements posed a particularly difficult problem. Implementation was difficult because it was necessary to generate the correct gate source voltages in the presence of a floating input, and because the available voltage to insure adequate channel pinch-off under all conditions was limited. This particular problem was resolved by incorporating a floating follower type function in conjunction with the switch (refer to Equipment Description).

B. ZCG SUBSYSTEM

Although the frequency of operation was probably the single most difficult problem associated with the development of the ZCG, it is perhaps most meaningful to discuss certain areas as particular problems, even though at lower frequencies they could have been dealt with much more easily.

The two main areas where technical problems caused the most difficulty are frequency of operation and the electrode interface and associated circuits. Another area of interest arose in connection with operation of the ZCG in the presence of a 50kc squarewave. Although this was not a problem as such from the implementation point of view, it is sufficiently important in terms of equipment operation to warrant mention.

Before discussing in detail the above, it should be noted that the overall design of the ZCG Subsystem constituted somewhat of a development problem due to the interrelationship of size, power consumption and performance requirements.

Frequency of Operation

Undoubtedly, the singular aspect of the ZCG Subsystem which resulted in the most difficulty in development was related to its frequency of operation. This point was eluded to above, but because it is so significant, it cannot be over-emphasized. Considering that the system operates only

approximately two octaves below standard AM broadcast frequencies, it can be expected that many of the problems typically encountered with the design of equipment at these frequencies would also be encountered in the development of the ZCG. It is common knowledge that at the AM broadcast frequencies, considerable attention must be given to distributed capacitance, shielding, undesirable feedback effects, etc. These phenomena must be carefully dealt with to insure proper operation even at the consumer level. In the case of the ZCG, design requirements become even more stringent by virtue of the fact that the equipment is required to operate to a specified accuracy over a wide range of temperature and under other equally difficult conditions. One of the more particularly interesting difficult conditions referred to is that of maintaining accuracy while transmitting reference energy through transmission cabling which is subject to constant displacement. Because of the displacement and the nature of the cable, physical changes in the cabling are inevitable, and as a consequence physical parameter changes which influence accuracy result. Perhaps even more important is the fact that to maintain accuracy, it was required that the reference energy be constant in nature when operating into a

terminal load which, for justifiable reasons, could not be well defined and which did not remain constant.

The requirement was ultimately implemented, however, and probably reflects the highest attainable accuracy obtainable at the present level of technology, considering all of the influencing requirements.

Interface and Associated Circuitry

The necessity of having a floating current source added significantly to the problem of its development. Had requirements related to the operation of the ZCG in conjunction with the other subsystems not ultimately prevented grounding one of the current supplying electrodes, a single-ended system, rather than the differentially balanced floating system, could have been developed with considerably less difficulty. Because minor changes in physical proximity and component tolerances resulted in significant effects at these frequencies, the development of a current source accurate to within 1% proved to be a significant task.

Various current source implementation approaches were examined, both analytically and empirically. The three most significant of these included the driven shield, neutralization, and the

tuned system. Each of these techniques exhibited drawbacks. However, the tuned system approach was ultimately selected as the better of the approaches under the imposed conditions. Because the interconnecting cabling was unknown and the nature of the load was difficult to adequately define, it was important to employ the technique that was least dependent upon changes in the physical and physiological parameters associated with the characteristic aspects of the interface.

In the case of the shield drive, it is necessary to provide a nearly unity voltage drive in order to effectively eliminate the unwanted capacitance in the cabling. Two very significant problems arise in the implementation of driving the shields. One is the tendancy of the system to oscillate. Under constant conditions, this problem could be minimized. However, in view of the wide range of environments, reliable stability margin is difficult to maintain. The second problem is related to the shield drive circuitry, from the standpoint of unbalances in the loading on the required floating output stage. At these frequencies it is difficult to obtain both the magnitude of the input impedance of the shield drive amplifiers and the required balance in those impedances. Unbalanced impedances result in common-mode voltages which at these frequencies are difficult to handle.

For a given system accuracy, an increase in the common-mode-rejection capability of the detector circuitry must accompany an increase in the common-mode voltage developed at the amplifier input. In view of the fact that achieving sufficient common-mode-rejection in the amplifier at 122kc was difficult in itself, it was considered unreasonable to select a means of implementing the current source which imposed difficult, if not impossible, additional requirements on an already difficult development task.

An additional problem resulting from the use of driven shields involves noise and is related primarily to the total required system sensitivity. It can be shown that the peak permissible noise voltage at a frequency of 100 cycles per second appearing on the current drive is a maximum of 5 nanovolts. More specifically, a sinusoidal modulation of the current source of peak amplitude of 5 nanovolts and frequencies of 100 cycles will result in a derivative output voltage at the maximum specified noise level. Assuming component values, which will typically be encountered, the noise introduced into the current drive at the electrodes by a unity gain shield drive amplifier will be attenuated by a factor of approximately 100. Assuming that the amplifier produced a modulation of the carrier to the extent of 1 microvolt, the noise then introduced at the

electrodes in the form of a modulated current drive would be 10 nanovolts, and would result in noise exceeding the specification limit by a fac or of 2.

The use of a tuned output drive circuit eliminates the problem of increased common-mode voltages and increased noise modulation. The major shortcoming of this technique is that the capacitance associated with the load constitutes a portion of the tuning capacitance.

Related to the system accuracy is the output impedance of the current sources. Because of the requirement for a floating source, it was necessary to either incorporate balanced solid-state drive circuitry or employ transformer coupling. The solid-state drive circuitry proved to be impractical because of the difficulty of obtaining and maintaining sufficiently high impedance levels with respect to common and minimal unbalances in those impedances.

The transformer coupling technique, while considered the better of the two approaches, presented many development problems. The design of the transformer went through approximately three phases before adequate balance of undistributed and interelectrode reactances and a sufficiently low loss design evolved.

On the receiving and detecting side of the interface, similar problems were encountered. The detecting amplifier was required to operate differentially, present very tightly balanced loads with respect to common, and to exhibit a high input impedance. To attain desired system accuracy, it was necessary to maintain a common-mode-rejection ratio of approximately 60 db. At the operating frequency of 122kc and under the adverse operating conditions, this was very difficult to achieve. It was further complicated by the fact that in order to achieve the required input impedance levels, it was necessary to drive the interconnecting cable shields with the detected signal. This additional requirement tended to degrade the common-mode-rejection performance of the amplifier.

To achieve the high level of input impedance required, three techniques were considered. These were:

- Driven Shields
- Neutralization
- Tuned System

Because the current source portion of the interface operated as a tuned system, a similar technique was avoided in the detecting system because of the operational difficulty of handling doubly tuned networks.

Neutralization techniques were examined because of their success in similar equipments; however, because of the unpredictability of the stability margin due to component variations with environment, this technique was considered unreliable for use in this application.

The discussion of noise above is applicable to the detector interface system. The noise modulation of the detector amplifier resulting from the noise inherent in the shield drive amplifiers is as significant here as was implied in the case of the current drive circuitry, and consequently undoubtedly contributes to the noise present at the system outputs.

50kc Interference

During the development of the ZCG Subsystem, unwanted low level signals of variable amplitude and frequency were noted in the system outputs when the system was operated in the presence of a 50kc squarewave at the detector input terminals. An investigation showed that these unwanted signals were the result of transitory oscillation in the bandpass filter produced by the squarewave input adding to the system carrier. This resulted in an apparent AM

modulated carrier. Since the transitory oscillation occurs at the resonant frequency and the resonant frequency of the filter will produce this apparent AM modulated carrier.

The 50kc waveform that actually appears at the detector electrodes is a distorted squarewave. Certain frequency components of the waveform are close enough to the resonant frequency of the filter to produce the transitory oscillation referred to. This problem is pointed out to provide some insight into the operation of the equipment and to perhaps serve as a guide in its use.

VI SPECIAL CONSIDERATIONS

The subsystem configurations for both the ZCG and the VCG, being divided into separate functional modules, require interconnecting cabling to complete the operational systems. As contracted, the interconnecting cabling and the electrode cabling was commercial-grade in nature, and designed primarily to permit operational testing of the equipment. In the design of interconnecting and electrode cabling for flight use, certain precautions should be observed. It is the intent of this section to establish the guidelines for the design of flight cabling and to point out some of the problems that may be encountered.

A. VCG SUBSYSTEM

Precautions relative to the cabling for the VCG Subsystem are important in two areas only. The first of these is the electrode/Frank Lead module cabling. The potential problems here involve noise and, depending upon the cable length, common-mode-rejection. Inasmuch as the effects of these problems and methods of minimizing resulting errors are well-known by NASA personnel as a result of their experience with ECG electrode interconnecting cable experience, a discussion of these problems has not been included. The second area of concern is the connecting cable between the Frank Lead module and the X, Y and Z ECG Signal Conditioners. Attention should be given to both the shielding and the lead lengths. Shielding should be in accordance with the interconnecting diagrams supplied as part

of the contract documentation.

Lead length constitutes a severe problem in that capacitive unbalances in the interconnecting lines results in the generation of differential signals in the presence of common-mode voltages. Because the lead lengths are relatively short and the operating frequencies are quite low, this problem may not be apparent or recognized to be as significant as it in fact is. The magnitude of the effect of unbalanced capacitance in the, albiet, short interconnecting cables can be better appreciated by understanding that it was necessary to incorporate trimming capacitance in the Frank Lead Network as compensation.

Because of the impracticality of providing capacitive adjustment after the modules were aligned, these capacitors were fixed and sealed with epoxy. To insure that the trimming capacitors were not compensating for unbalances in the interconnecting cabling, the cabling was carefully prepared to guarantee, as closely as possible, equal cable capacitance. From the ideal standpoint, then, the trimming capacitors were adjusted to compensate distributed capacitance in the Frank Lead Network. To insure adequate common-mode-rejection through the entire system, then, it is necessary only that the distributed capacitance of the interconnecting cabling in any future designs be maintained equal.

The rest of the cabling required to interconnect the VCG Subsystem is not critical and should not constitute a design concern.

B. ZCG SUBSYSTEM

Interconnecting cabling for the ZCG Subsystem is important from a design standpoint only for electrode/module interconnection. These interconnecting cables carry the high frequency carrier, and because of the effects of distributed capacitance must be carefully designed. The remainder of the subsystem cabling provides the interconnection to power and low frequency data signals, and therefore requires no extraordinary design and fabrication consideration.

The cable capacitance of the electrode leads connecting the current source module and outer thorax electrodes should be minimized. The output circuit is broadly tuned, with the cable capacitance constituting a part of the tuning capacitance. Should the cable capacitance become large, the circulating tank current will impose a heavy load on the output circuit. Also, excessive capacitance would tune the output circuit such that it was net capacitive. Both of these effects will degrade the accuracy of the current source. It is recommended that the interconnecting cable be as short as possible, and that the cable type chosen exhibits minimum capacitance.

The cabling connecting the inner thorax electrodes to the differential amplifier warrants special attention. The effects of capacitance in this circuit are neutralized by providing signal drive to the shields. Because it is necessary to drive the shields at as close to unity as possible to

effectively neutralize capacitance, and because the closer to unity that the cables are driven the greater the tendancy to oscillate, it is important to consider the effect of excessive cable capacitance on the stability of the system. If the cable capacitance becomes excessive, the drive amplifiers are unduly loaded and the stability margin of the system decreases. It is therefore recommended that minimum length cable be employed which is characterized by relatively low capacitance per foot. Differences in cable lengths are effectively differences in load capacity, and will therefore result in slight differences in the neutralization of the system. These differences, if relatively large, will result in system errors. As a consequence, it is further recommended that the differences in the cable lengths to the thorax electrodes be minimized.

If the precautions outlined above are observed in the design and manufacture of the electrode/module cabling, no difficulty should be encountered relative to the system performance. While it is important to observe the physical character of the cabling as indicated above, careful attention was given to the design of the equipment to insure that a reasonable range of cable parameters could be tolerated without degradation of system performance.

APPENDIX A

SUMMARY OF CONTRACT MODIFICATIONS

MODIFICATION 1 - 3/3/66

This Modification concerns change of delivery addresses.

MODIFICATION 2 - 3/15/66

Modification 2 alters the calibration requirements for the ECG Signal Conditioner associated with the VCG Subsystem.

MODIFICATION 3 - 8/9/66

This Modification reflected a major change in the program scope of work. As a result of this Modification, changes in performance requirements, configuration, deliverable items, and contract schedules occurred.

MODIFICATION 4 - 8/12/66

Modification 4 changed the dimensional requirements imposed on the signal conditioner modules.

MODIFICATION 5 - 9/19/66

Changes in the dimensions of the Converter were covered by this Modification, in addition to a correction relative to dimensions called out in NASA Modification No. 4.

MODIFICATION 6 - 10/10/66

Vibration and qualification reference document requirements were definitized.

MODIFICATION 7 - 11/1/66

Subsystem module nomenclature was defined by this Modification.

MODIFICATION 8 - 11/21/66

This Modification served as a correction to Modification 7.

MODIFICATION 9 - 12/23/66

Modification 9 affected performance requirements of the following subsystems to the extent indicated.

VCG Subsystem:	Deleted timing requirement.
DC-DC Converter:	Modified requirements.
ZCG Subsystem:	Changed and/or redefined Specification relative to transient suppression, noise, and current source impedance.

MODIFICATION 10 - 1/13/67

This Modification reflected changes in the weight and dimensions of certain of the subsystem signal conditioners. Additionally, it defined Specification paragraph renumbering.

MODIFICATION 11 - 2/20/67

Modification 11 reflected contractual price adjustments for Modifications 7 and 8.

MODIFICATION 12 - 1967

This Modification to the Contract definitized measurement techniques and requirements relative to the ZCG Subsystem output noise.

MODIFICATION 13 - 10/5/67

Modification 13 reflected changes in delivery requirements and Contract price adjustments resulting from Modifications 1, 2, 4, 5, 6, and 10.

MODIFICATION 14 - 12/6/67

Transferred authority for final inspection and acceptance of all work on Item 2 of the Contract from NASA/Manned Spacecraft Center to the Defense Contract Administration Services District, Van Nuys, California

MODIFICATION 15 - August 1967

Modification 15 reflected adjustments in item delivery schedules and Contract price.

APPENDIX B

SUBSYSTEMS DOCUMENTATION

PCG SUBSYSTEM

Drawing No.	Title
Subsystem	
104262	Design Acceptance Test Procedure
104375	Design Acceptance Test Data Sheets
Signal Conditioner	
PL104524	Parts List
104523	Schematic
104526	Outline Drawing
104527	Final Assembly
104522	Component Parts Board
104521	Component Parts Assembly
104525	Case Drawing
104528	Nameplates
104561	End Item Test Procedure
104562	End Item Test Data Sheets
Transducer	
PL104119	Parts List
104119	Final Assembly
104111-2	Nameplates
102761	Component Parts Assembly

EEG SUBSYSTEM

Drawing No.	Title
PL104173	Parts List
104175	Schematic
104172	Outline Drawing
104173	Final Assembly
104179	Component Parts Board
104178	Component Parts Assembly
104176	Case Drawing
104177	Nameplates
104410	Design Acceptance Test Procedure
104183	Design Acceptance Test Data Sheets
104182	End Item Test Procedure
104183	End Item Test Data Sheets
104184	Qualification Test Procedure
104185	Qualification Test Data Sheets
104432	Reliability Analysis

VCG SUBSYSTEM

Drawing No.	Title
Subsystem	
104315	Power Requirements
104684	Design Acceptance Test Procedure
104683	Design Acceptance Test Data Sheets
104677	End Item Test Procedure
104678	End Item Test Data Sheets
104601	Qualification Test Procedure
104602	Qualification Test Data Sheets
Frank Lead Network	
PL104381	Parts List
104380	Schematic
104386	Outline Drawing
104384	Final Assembly
104382	Component Parts Board
104383	Component Parts Assembly
104385	Case Drawing
104387	Nameplates
104434	Reliability Analysis
104400	Wiring Diagram

Drawing No.	Title
Control and Calibrate	
PL104391	Parts List
104390	Schematic
104396	Outline Drawing
104394	Final Assembly
104392	Component Parts Board
104393	Component Parts Assembly
104395	Case Drawing
104397	Nameplates
104433	Reliability Analysis

DC-DC CONVERTER

Drawing No.	Title
PL104685	Parts List
104688	Final Assembly
104686	Component Parts Assembly
104727	Component Parts Board
104689	Outline Drawing
104681	Schematic
104694	Case Potting
104695	Nameplates
104682	Transformer
104690	RF Shield I
104691	RF Shield II
104692	RF Shield III
104723	Coil (Toroid)
104763	End Item Test Procedure
104764	End Item Test Data Sheets
104728	Reliability Analysis
104734	Qualification Test Procedure
104735	Qualification Test Data Sheets

ZCG SUBSYSTEM

Drawing No.	Title
Subsystem	
104262	Design Acceptance Test Procedure
104375	Design Acceptance Test Data Sheets
104559	End Item Test Procedure
104560	End Item Test Data Sheets
Current Source	
PL104424	Parts List
104423	Schematic
104447	Outline Drawing
104448	Final Assembly
104422	Component Parts Board
104421	Component Parts Assembly
104425	Case Drawing
104449	Nameplates
Calibrate Module	
PL104429	Parts List
104428	Schematic
104518	Outline Drawing
104519	Final Assembly
104427-2	Component Parts Board

Drawing No.	Title
104426	Component Parts Assembly
104430	Case Drawing
104520	Nameplates
104439	Reliability Analysis

ΔZ, $\dot{\Delta Z}$ Amplifier

PL104414	Parts List
104413	Schematic
104441	Outline Drawing
104442	Final Assembly
104412	Component Parts Board
104411	Component Parts Assembly
104415	Case Drawing
104443	Nameplates
104437	Reliability Analysis

Differential Amplifier and Detector

PL104419	Parts List
104418	Schematic
104444	Outline Drawing

ZCG SUBSYSTEM (Cont'd.)

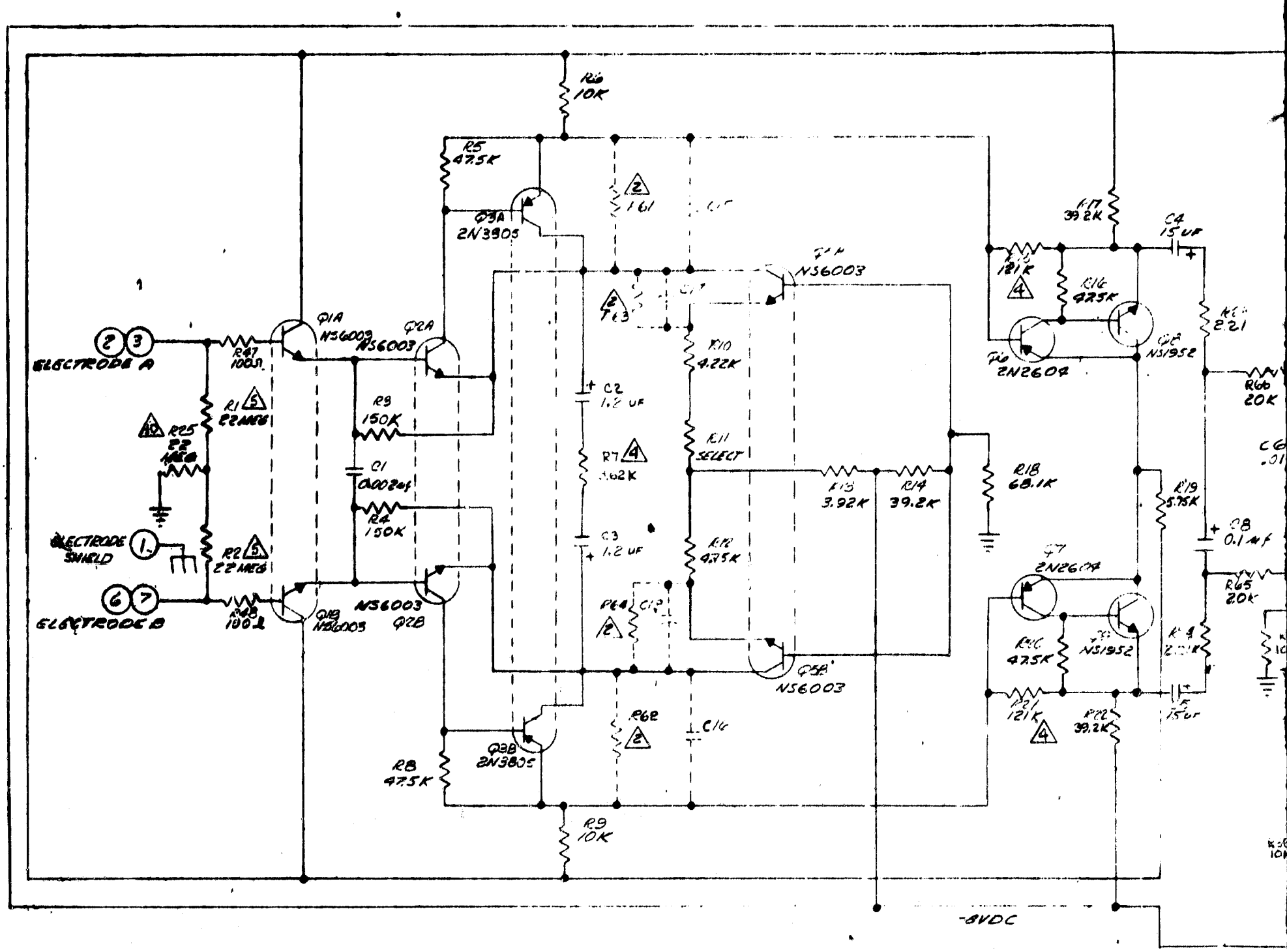
Drawing No.	Title
104445	Final Assembly
104417	Component Parts Board
104416	Component Parts Assembly
104420	Case Drawing
104446	Nameplates
104438	Reliability Analysis

APPENDIX C

SUBSYSTEM SCHEMATIC DRAWINGS

FOLDOUT FRAME 1

DIFFERENCE DESIGNATIONS	
LAST USED	OMITTED
[illegible]	[illegible]
C66	[illegible]
Q11	Q4
C26	



11 FOR TEST PROCEDURE SEE 104548
10 RESISTORS NOTED ARE 1/4 WATT ±5% CARBON COMP.
9 FOR FINAL ASSEMBLY SEE DWG 104527
8 ALL CAPACITANCE VALUES ARE ±10%
7 FOR ENGR. PARTS LIST SEE DWG 104524
6 FOR OUTLINE DRAWING SEE 104526
5 MATCHED PAIR PER SPEC. 601400
4 RESISTORS NOTED ARE ±50 PPM PER °C
3 RESISTORS NOTED ARE 1/10 W, 1% METAL FILM SELECT VALUE PER 102844
2 DOTTED COMPONENTS ARE SELECTED PER 102844
1 RESISTORS ARE METAL FILM 1/10 WATT, ± 1.0%.

NOTES: UNLESS OTHERWISE SPECIFIED

LEGEND

○ INPUT CONNECTOR

◻ OUTPUT CONNECTOR

CAST SYMBOL USED	
R66	
C15	
C13	
C26	
SW1	

FOLDOUT FRAME 2

REVISIONS						
DISPOSITION CODE:	1 MAY BE REWORKED	2 CANNOT BE REWORKED	3 RECORD CHANGE			
	4 NEW SHOP PRACTICE	5 PARTS MADE OBS				
REV STA	WHO MADE	DESCRIPTION	MFG EFF	DISP CODE PART	DISP CODE ASSY	APPROVAL & DATE
A		RELEASE PER E.O. 10158				[illegible] 5-11-67
B		REVISED PER EC# [illegible]214				

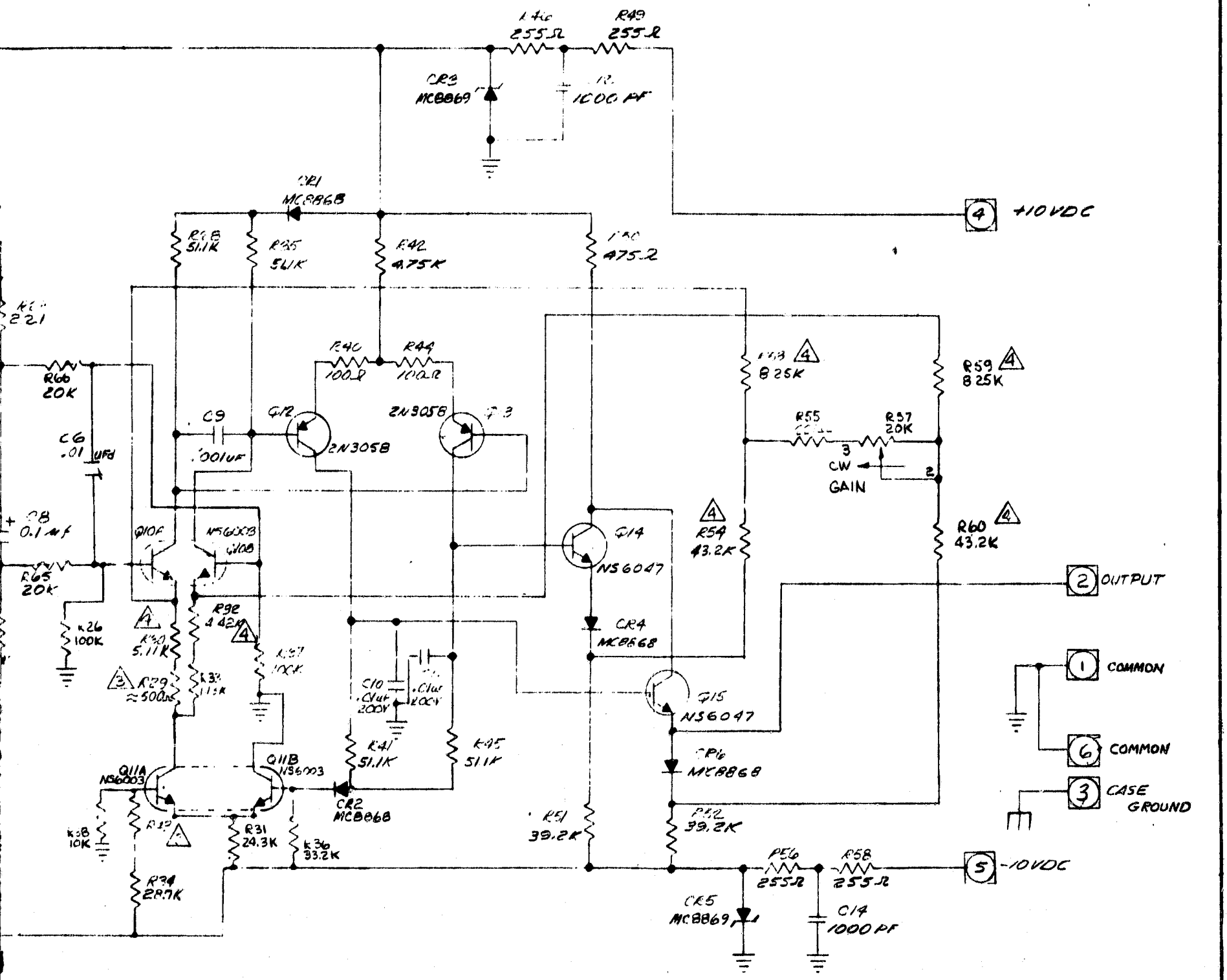


FIGURE 1

SYMBOL USED	SYMBOL NOT USED
R6	R27, R39
R5	Q9
R8	C7, C13
R6	
R11	

QTY PER ASSY	ITEM	PART NO	DESCRIPTION	MATL	MATL SPEC	ZONE

LIST OF MATERIAL

PART NO	REV LTR	MOD NO	NEXT ASSY	NEXT ASSY	FINAL ASSY
APPLICATION				QTY REQ	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE: .XX = ± .03 .XXX = ± .010 X°=0° ± 30'
WEIGHT IS IN LBS & TENTHS
ALL FINISHED SURFACES 125 PER MIL-STD-10
MFR PER SPEC
TOLERANCE SYMBOLS PER MIL-STD-8
ELECTRICAL SYMBOLS PER MIL-STD-15
MECHANICAL SYMBOLS PER MIL-STD-17
WELDING SYMBOLS PER JAN-STD-15

DRAFT	[illegible]	9-2-66
DESIGNER		
STRESS & WEIGHT		
CHECKER	F. Boyer	9-2-66
DESIGN ENG	[illegible]	9-2-66
MFG ENG	[illegible]	9-1-66
SYS ENG	[illegible]	9-6-66
PROJ ENG	[illegible]	9-6-66

CALCULATED WT LB: 1 0 4 5 2 3
PART NO
REFERENCE TO SIMILAR SYS
SIZE D

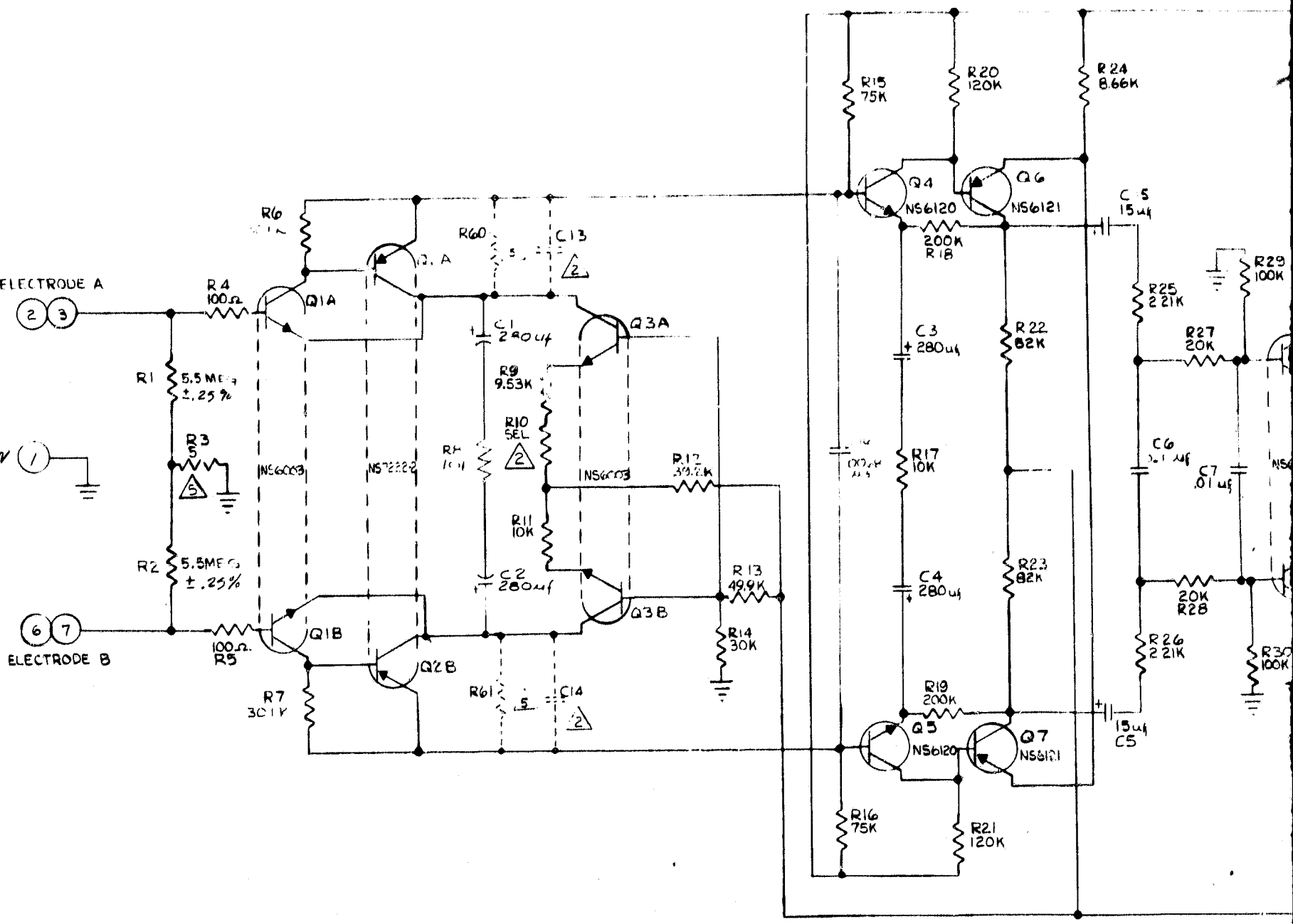
TITLE: SCHEMATIC DIAGRAM PHONOCARDIOGRAM, ECG

Spacelabs, Inc.
15821 LANARK ST.
VAN NUYS, CALIFORNIA

SPEC NO 104823 REV B
SCALE WT EST LB WT CALC LB
SHEET 1 OF 1

FOLDOUT FRAME 1

"REPRODUCIBILITY OF THE ORIGINAL PAGE IS POOR;



5 RESISTORS NOTED ARE 1/4 WATT ± 5% CARBON COMP
4 ALL CAPACITANCE VALUES ARE ±10%

2 SELECTED COMPONENTS
1. RESISTORS ARE METAL FILM 1/10 WATT ±1%
NOTE : UNLESS SPECIFIED OTHERWISE

FOLDOUT Drawing 2

REVISIONS						
DISPOSITION CODE: 1 MAY BE REWORKED; 2 CANNOT BE REWORKED; 3 RECORD CHANGE; 4 NON SHOP PRACTICE; 5 PARTS MADE OBSOLETE						
REV LTR	DISP CODE	DESCRIPTION	MFG EFF	DISP CODE PART	DISP CODE ASSY	APPROVAL & DATE
		PRODUCTION RELEASE				9/-66
A		REVISED PER ECO 00068				2/17/66 PS
B		REVISED PER ECO. 00078				9/16/66

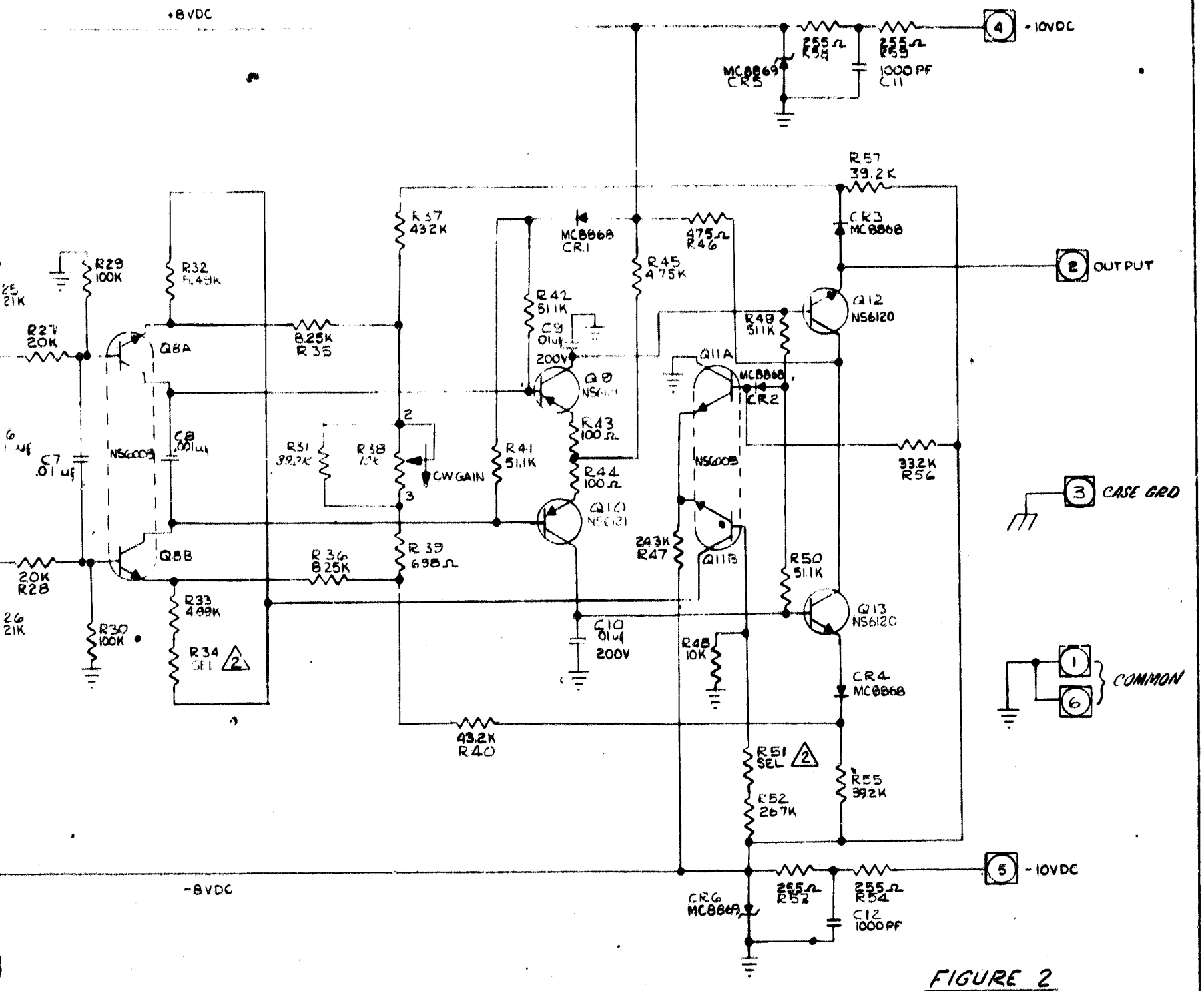


FIGURE 2

QTY PER ASSY	ITEM	PART NO	DESCRIPTION	MATL	MATL SPEC	ZONE

LIST OF MATERIAL

APPLICATION

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES ARE
.XX = ± .03 .XXX = ± .010 3°-0' ± 30'
WEIGHT IS IN LBS & TENTHS
ALL FINISHED SURFACES 125 PER MIL-STD-10
MFR PER SPEC
TOLERANCE SYMBOLS PER MIL STD-8
ELECTRICAL SYMBOLS PER MIL STD-15
MECHANICAL SYMBOLS PER MIL STD 17
WELDING SYMBOLS PER JAN-STD-19

DRAFT	J. Shaw	1/4/66
DESIGNER		
STRESS & WEIGHT		
CHECKER		
DESIGN ENG		
MFG ENG		
STDS ENG		
PROJ ENG		3/1/66

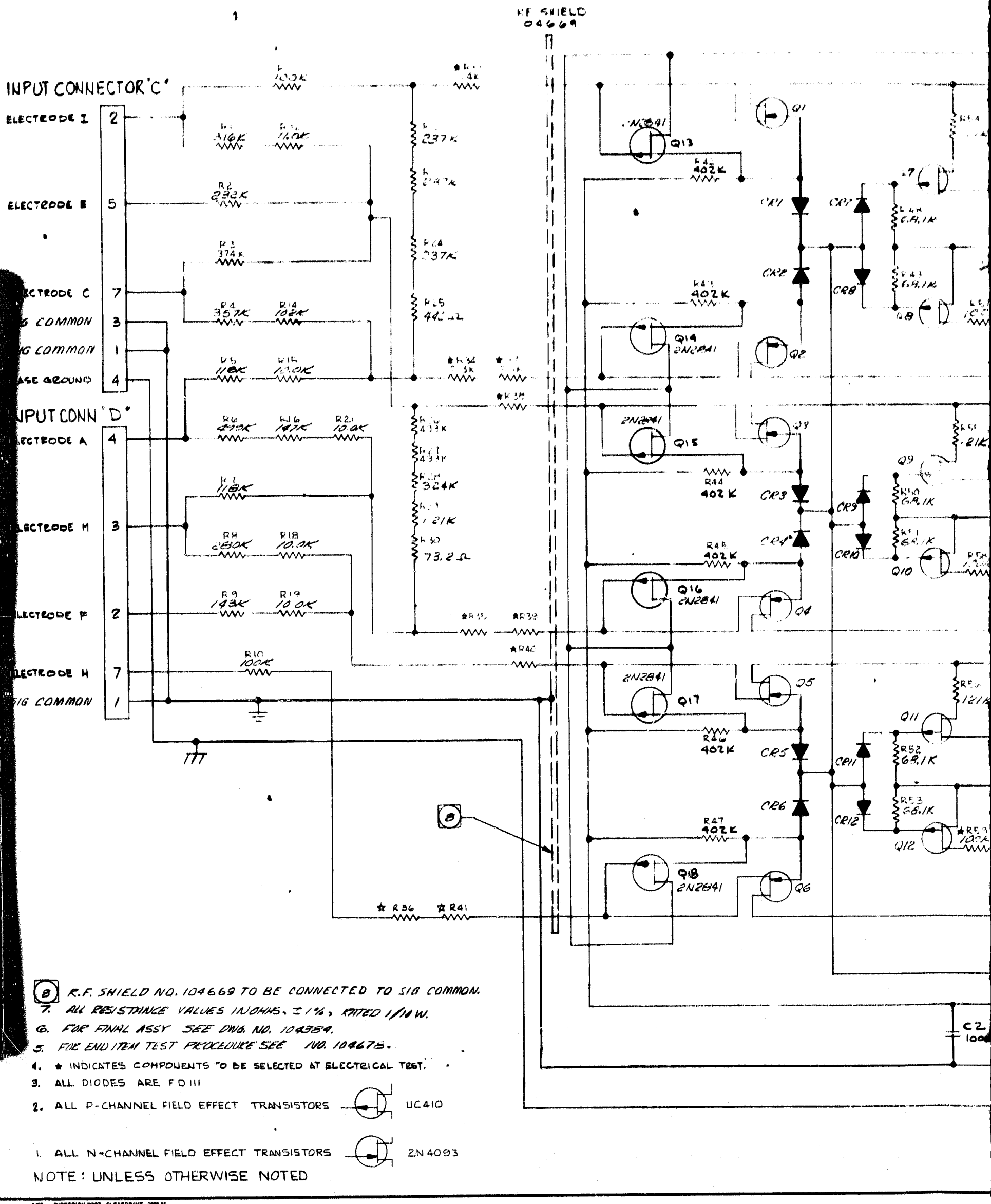
CALCULATED WT LB
PART NO
REFERENCE TO SIMILAR DWG
DWG SIZE D

TITLE
SCHEMATIC, EEG SIGNAL COND

LAYOUT
RELEASE DATE
SCALE — WT ACT — LB WT CALC — LB

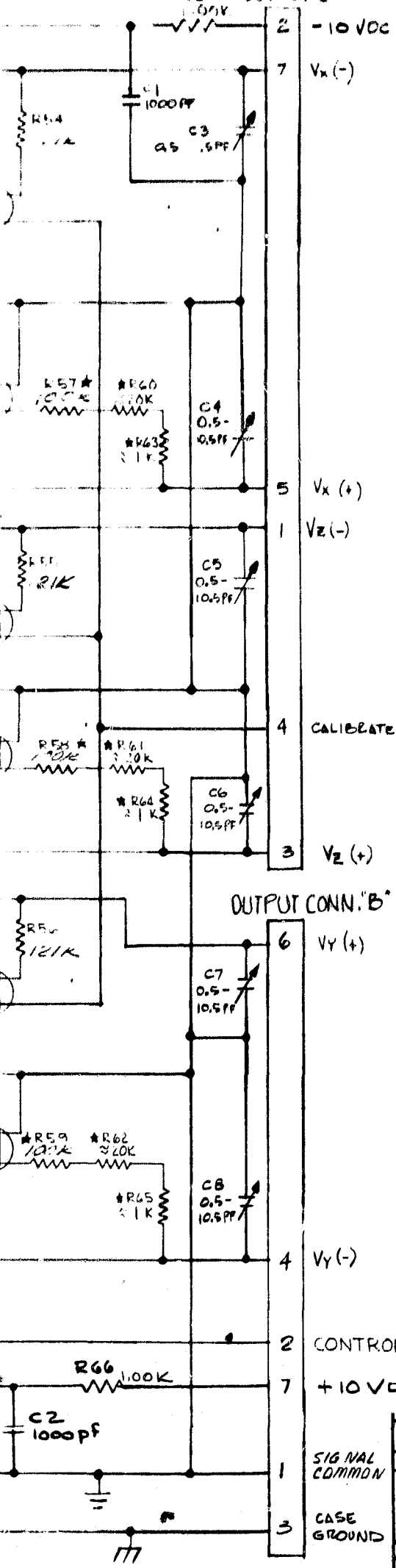
Spacelabs, Inc.
15821 LANARK ST.
VAN NUYS, CALIFORNIA

DWG NO 104175
REV B
SHEET 1 OF 1



8. R.F. SHIELD NO. 104669 TO BE CONNECTED TO SIG COMMON.
7. ALL RESISTANCE VALUES IN OHMS, ± 1%, RATED 1/10 W.
6. FOR FINAL ASSY SEE DWG. NO. 104354.
5. FOR END ITEM TEST PROCEDURE SEE NO. 104675.
4. ★ INDICATES COMPONENTS TO BE SELECTED AT ELECTRICAL TEST.
3. ALL DIODES ARE FD 111
2. ALL P-CHANNEL FIELD EFFECT TRANSISTORS — UC410
1. ALL N-CHANNEL FIELD EFFECT TRANSISTORS — 2N4093

NOTE: UNLESS OTHERWISE NOTED



REVISIONS							
DISPOSITION CODE	1 MAY BE REWORKED	2 CANNOT BE REWRD	3 RECORD CHANGE				
	4 NEW SHOP PRACTICE	5 PARTS MAKE OR			DISP CODE		APPROVAL & DATE
REV LTR	ECO CODE	DESCRIPTION	MFG EFF		PART	ASSY	
A		APOD REL E.O. 00129					[illegible] 4-24-67
B		REVISED PER E.O. 00181					P.I.B. 4-24-67
C		[illegible]					

REF DESIG.	
LAST USED	DELETED
C112	
R67	R31, R32, R13, R20, R17
C8	
Q18	

FIGURE 3

104383

QTY PER ASSY	ITEM	PART NO	DESCRIPTION	MATL	MATL SPEC	ZONE

LIST OF MATERIAL

PART NO	DASH NO	ECO NO	NEXT ASSY	USED ASSY	FSCM NO	APPLICATION	QTY REQ

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
.XX = ± .03 | .XXX = ± .010 | ∠ = 0° ± 30'
WEIGHT IS IN LBS & TENTHS
ALL FINISHED SURFACES 125 µ/ PER MIL-STD-10

MFR PER SPEC

TOLERANCE SYMBOLS PER MIL-STD-8
ELECTRICAL SYMBOLS PER MIL-STD-15
MECHANICAL SYMBOLS PER MIL-STD-17
WELDING SYMBOLS PER JAN-STD-19

DRAFT	F. SILVA	6/16/66
DESIGNER		
STRESS & WEIGHT		
CHECKER	[illegible]	6/15/66
DESIGN ENG	R L C	6 27 66
MFG ENG	[illegible]	4.4.67
STDS ENG		
PROJ ENG	[illegible]	7-27-66

CALCULATED WT LB

PART NO

REFERENCE TO SIMILAR DWG

DWG SIZE D

TITLE
SCHEMATIC DIAGRAM, FRANK LEAD AND INPUT SWITCH (VCG)

LAYOUT

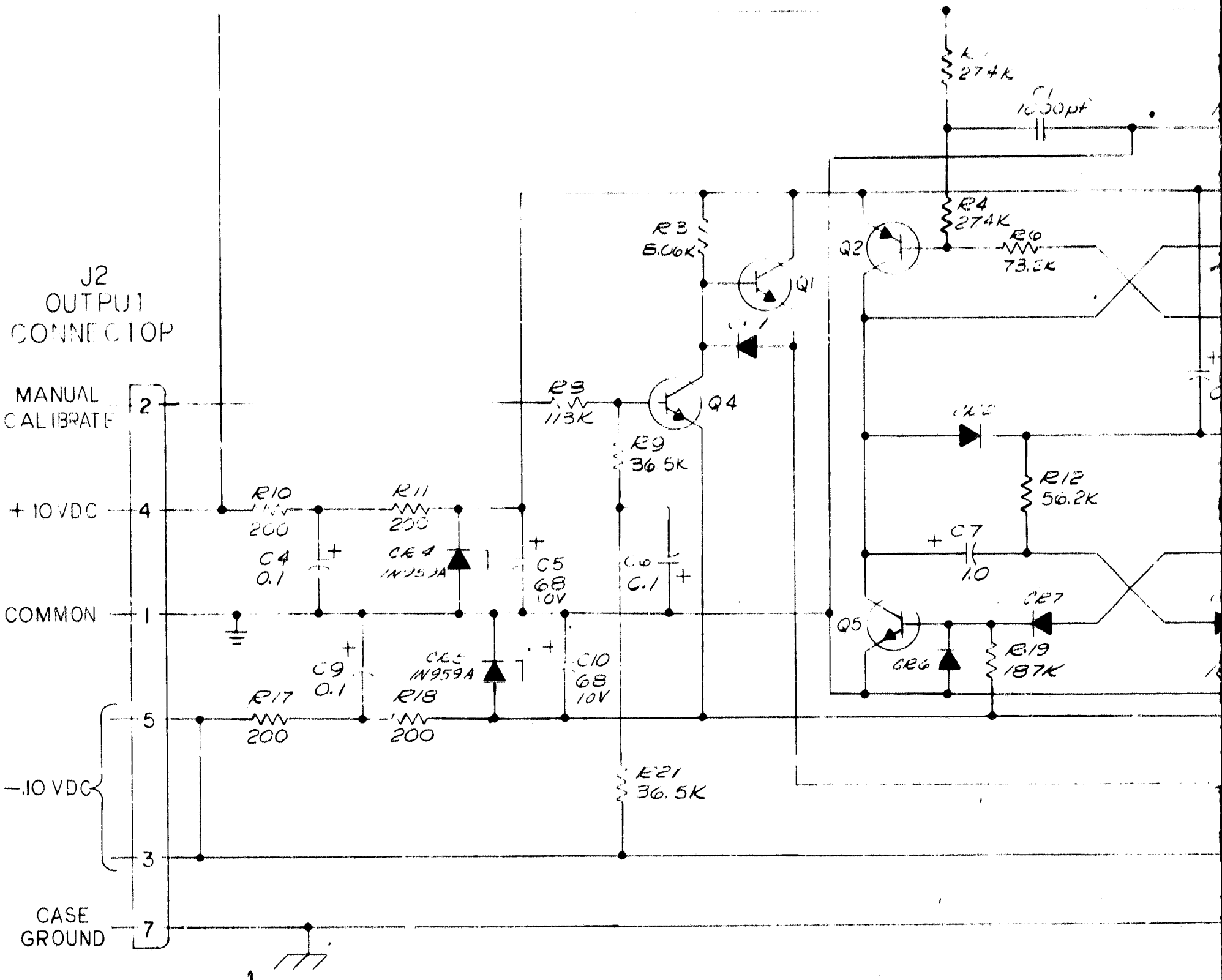
RELEASE DATE

SCALE NONE | WT ACT LB | WT CALC LB | SHEET 1 OF 1

Spacelabs, Inc.
15531 LANARK ST.,
VAN NUYS, CALIFORNIA

DWG NO 104390

REV C



13. FOR IN-LINE TEMPERATURE TEST PROCEDURE SEE DWG. NO. 104676.
12. FOR END ITEM TEST & INSPECTION PROCEDURE (PDA) SEE DWG NO. 104676.
11. FOR FUNCTIONAL TEST PROCEDURE SEE DWG. NO. 104646.
10. FOR WIRING DIAGRAM (SYSTEM) SEE DWG. NO. 104403.
9 FOR COMPONENT PARTS ASSEMBLY SEE DWG. NO. 104393.
8. HIGHEST REFERENCE DESIGNATIONS USED ARE:
   R21, C10, CR10, Q6, RDV1.
7. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN; FOR COMPLETE DESIGNATION, PREFIX WITH UNIT NUMBER OR SUB-ASSEMBLY DESIGNATION (S).
6. RESISTANCE VALUE OF R15 TO BE DETERMINED PER COMPONENT SELECTION PROCEDURE NO. 104529.
5. ALL DIODES ARE FD111.
4. ALL PNP TRANSISTORS ARE 2N3251. (Q2 & Q5).
3. ALL NPN TRANSISTORS ARE 2N3947. (Q1, Q4, Q5, Q6).
2 ALL CAPACITANCE VALUES IN MICRO-FARADS, ±10%, 20VDC.
1. ALL RESISTANCE VALUES IN OHMS, ±1% RATED 1/10W.

14. TEST POINTS ARE SHOWN F
CALIBRATION REF. AND ARE
ITEM. (SEE NOTES 10 THRU

NOTES: UNLESS OTHERWISE SPECIFIED

REVISIONS						
DISPOSITION CODE: 1 MAY BE REWORKED; 2 CANNOT BE REWORK; 3 RECORD CHANGE; 4 NEW SHOP PRACTICE; 5 PARTS MADE OBS						
REV LTR	WORK ORDER	DESCRIPTION	MFG EFF	DISP CODE PART	DISP CODE ASSY	APPROVAL & DATE
A		PRODUCTION REL E.O. 00127				RAB 4-4-67
B		REVISED PER E.O. 00145				RAB 5-1-67

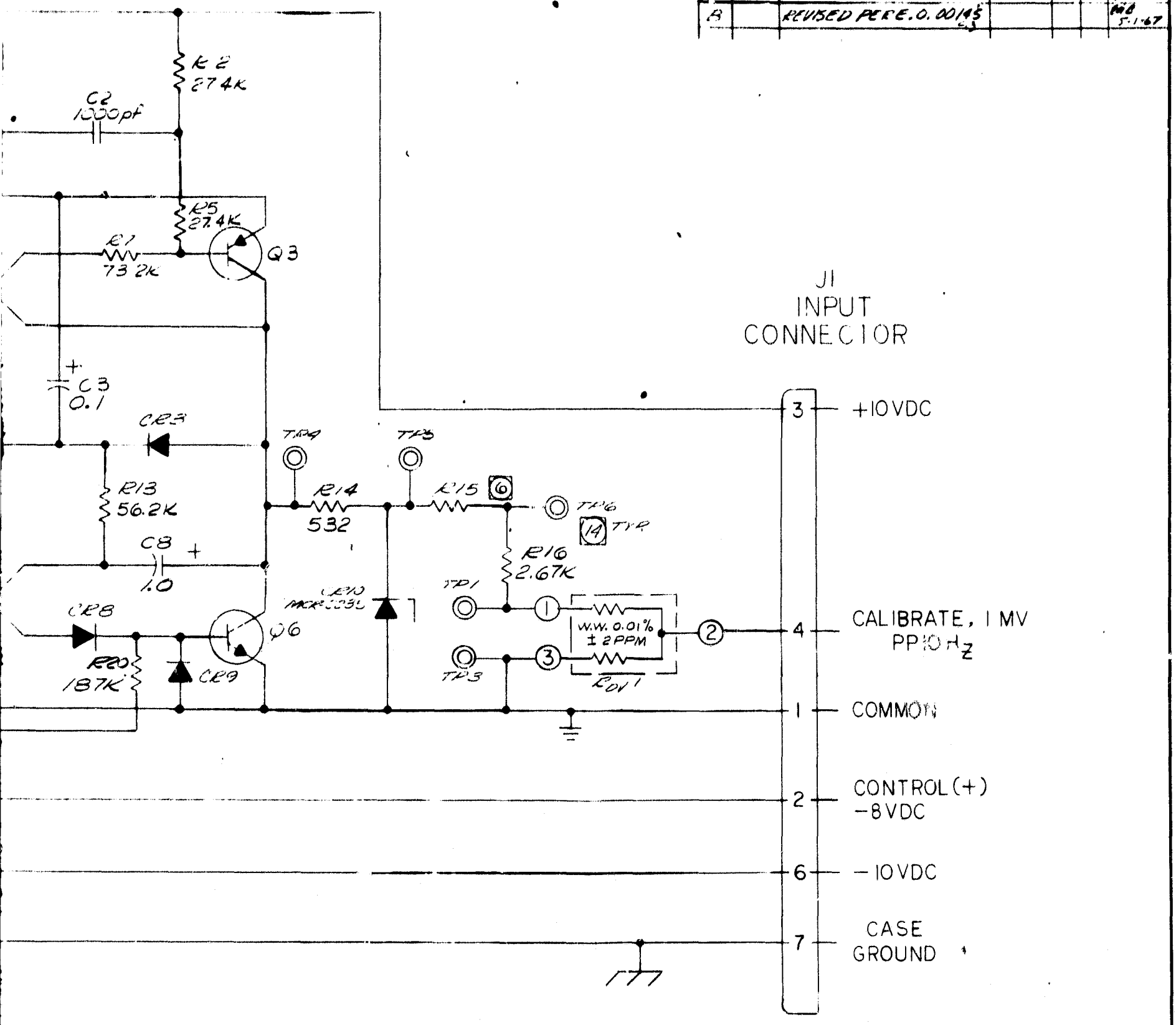


FIGURE 4

SHOWN FOR COMPONENT SELECT
ND ARE NOT REQD. ON END
10 THRU 13 ON DWG. 104393).

QTY PER ASSY	ITEM	PART NO	DESCRIPTION	MATL	MATL SPEC	ZONE

LIST OF MATERIAL

PART NO	MFR	MOD NO	NEXT ASSY	NEXT ASSY	FINAL ASSY	QTY REQ

APPLICATION

104394

CALCULATED WT LB: 104390 PART NO

REFERENCE TO SIMILAR DWG

DWG SIZE: D

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
.X N/A .03 | .XX N/A .010 | ANG N/A ±30'
WEIGHT IS IN LBS & TENTHS
ALL FINISHED SURFACES 125√ PER MIL-STD-10
MFR PER SPEC
TOLERANCE SYMBOLS PER MIL-STD-8
ELECTRICAL SYMBOLS PER MIL-STD-15
MECHANICAL SYMBOLS PER MIL-STD-17
WELDING SYMBOLS PER JAN-STD-15

DRAFT		
DESIGNER	RAMSEY	2-28-67
STRESS & WEIGHT		
CHECKER	P. BROWN	3-2-67
DESIGN ENG	P. BROWN	3-2-67
MFG ENG	[illegible]	4-2-67
STDS ENG		
PROJ ENG	[illegible]	3-29

TITLE: SCHEMATIC DIAGRAM CONTROL & CALIBRATE (VCG)

LAYOUT N/A RELEASE DATE N/A
SCALE NONE WT ACT N/A LB WT CALC N/A LB

Spacelabs, Inc.
15521 LANARK ST.
VAN NUYS, CALIFORNIA

DWG NO 104390 REV B
SHEET 1 OF 1

FOLDOUT FRAME 1

"REPRODUCIBILITY OF THE ORIGINAL PAGE IS POOR;

T1

J1 INPUT CONNECTOR

+28V

CASE GND

+28V RETURN

SHIELD

FILTER

FL1

C22 2.2

C17 4700pf 50V

C1 .1 50V

R1 5.11K

Q1 MHT5004

R3 2.0K

R2 221

C2 30pf

CR26 UTX210

R4 43.2K

C3 1.5 10V

C4 4700pf 50V

CR2 IN962B

R5 5.0K

CR28 FD111

CR27 FD111

Q3 2N3251

R6 10.0K

R7 SELECT

R8 75K

C25 10@35V

C26 10@35V

C5 10@35V

CR1 UTX210

Q2 MHT5004

L1

LC1

C21 .1 50V

R9 511

Q4 MHT5004

CR3 FD111

CR4 FD111

C16 620pf

Q5 MHT5004

UTX210 (4)

CR6 CR7 CR8 CR9 FD111 CR10 FD111 CR11 FD111 CR12 FD111

C8 150 20V

R11 16.2K

UTX210 (4)

CR15 CR17 CR16 CR18 CR19 FD111 CR20 FD111 CR21 FD111 CR22 FD111

C12 150 20V

R20 16.2K

CR25 UTX210

C16 150 20V

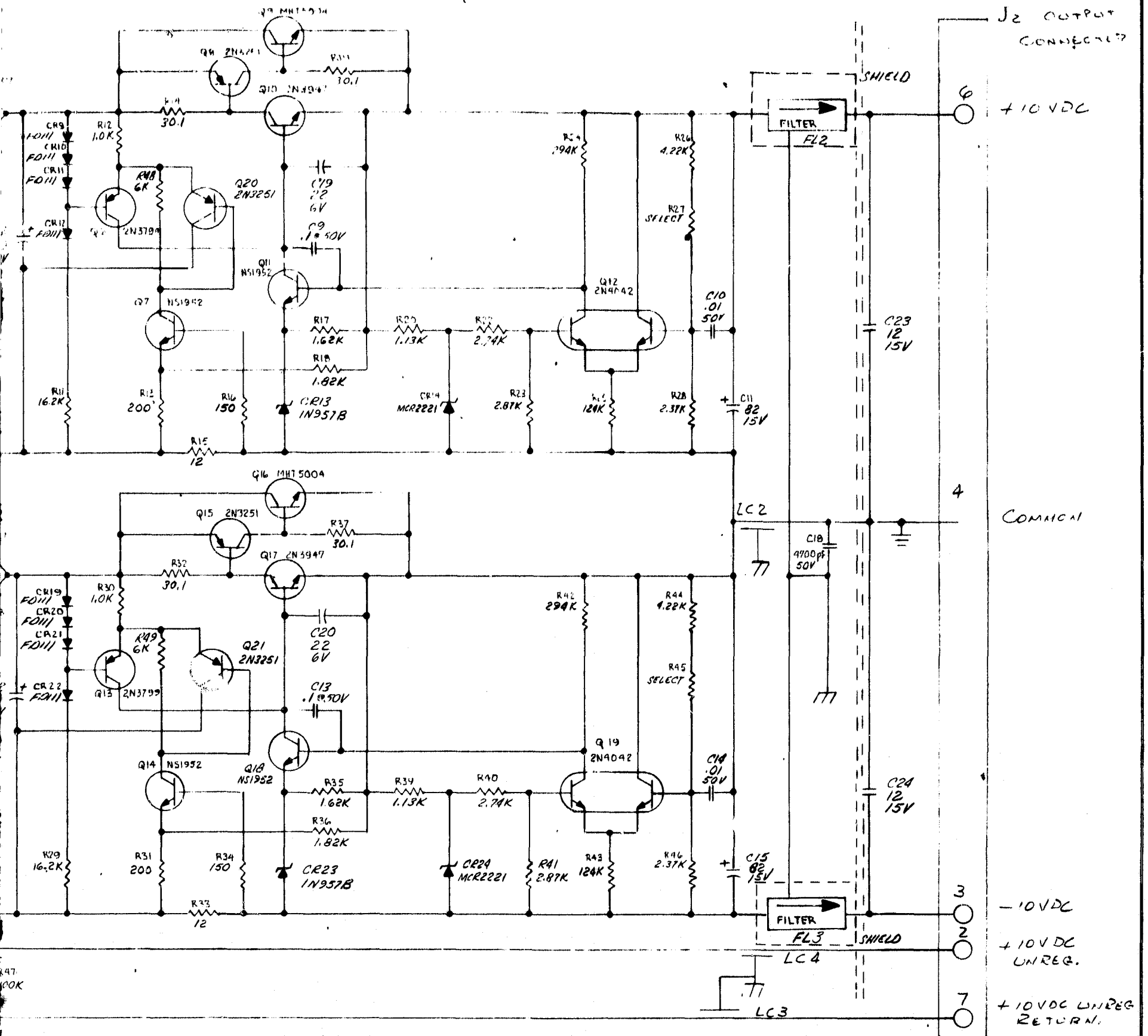
R47 100K

2. ALL CAPACITOR VALUES ARE IN MICROFARADS.
1. ALL RESISTORS ARE IN OHMS, 1/8W, 1%

NOTES: UNLESS OTHERWISE SPECIFIED

FOLDOUT FRAME 2

REVISIONS						
DISPOSITION CODE:		A MAY BE REWORKED B NEW SHOP PRACTICE		C CANNOT BE REWKD. D PARTS MADE OK		E RECORD CHANGE
REV LTR	WORK ORDER	DESCRIPTION	MFG EFF	DISP CODE PART	DISP CODE ASSY	APPROVAL & DATE
N/C		CONTROLLED RELEASE EO 00241				Cal 8-11-67
A		REVISED PER EO 00259				11-2-67
B		REVISED PER EO 00252				11-24-67



QTY PER ASSY	ITEM	PART NO	DESCRIPTION	MATL	MATL SPEC	ZONE

LIST OF MATERIAL

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
.XX = ± .03 | .XXX = ± .010 | X° = 0° ± 30'
WEIGHT IS IN LBS & TENTHS
ALL FINISHED SURFACES 125 √ PER MIL-STD-10
MFR PER SPEC
TOLERANCE SYMBOLS PER MIL-STD-8
ELECTRICAL SYMBOLS PER MIL-STD-15
MECHANICAL SYMBOLS PER MIL-STD-17
WELDING SYMBOLS PER JAN-STD-19

CALCULATED WT LB
PART NO
REFERENCE TO SIMILAR DWG
DWG SIZE D

DRAFT		
DESIGNER	B.C.	9.28.67
STRESS & WEIGHT		
CHECKER		
DESIGN ENG	EAB	9.28.67
MFG ENG	[illegible]	9-28-67
STDS ENG		
PROJ ENG	[illegible]	9.28.67

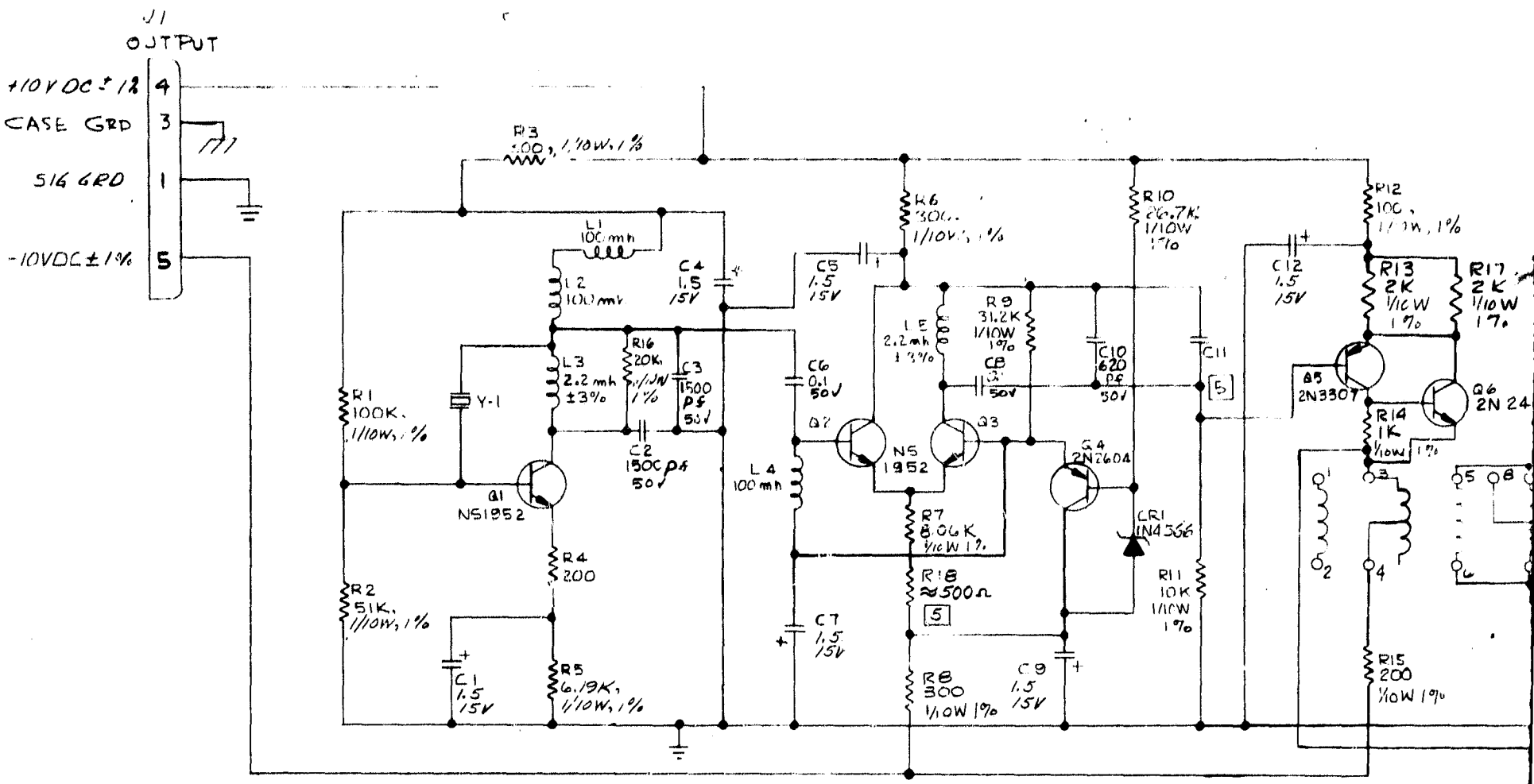
TITLE
SCHEMATIC, DC TO DC CONVERTER

Spacelabs, Inc.

LAYOUT | RELEASE DATE
SCALE NONE | WT ACT LB | WT CALC LB

DWG NO 104681 REV B

SHEET 1 OF 1

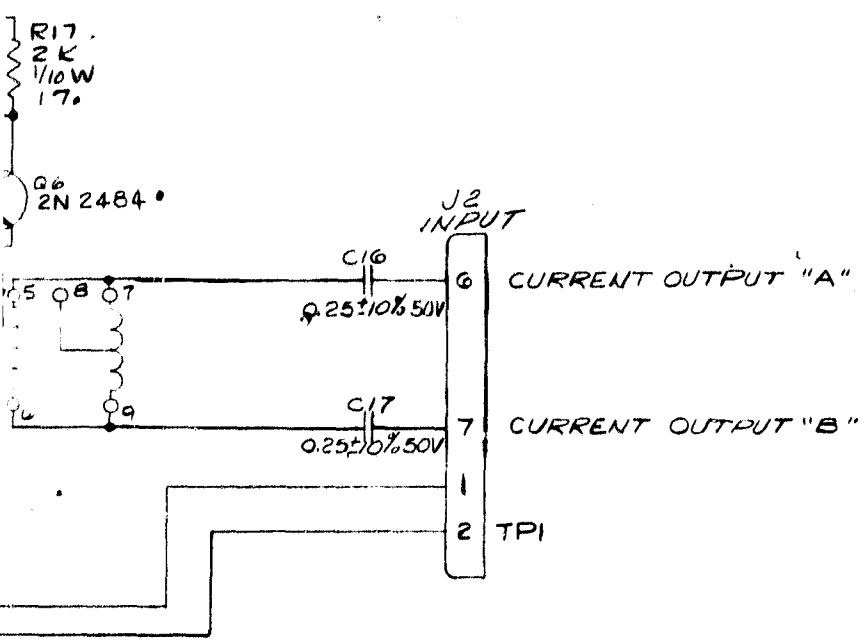


5. TO BE SELECTED AT FINAL ELECTRICAL TEST
4. ALL CAPACITOR VALUES ARE IN MICROFARADS.
3. ALL RESISTOR VALUES ARE IN OHM ± 5% RATED 1/4W.
2. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN, PREFIX WITH UNIT & ASSY DESIGNATION.
1. REF DWG NO: ASSY DWG, 104421
WIRING DIAGRAM, 104409
TEST PROCEDURE, 104550

NOTES: UNLESS OTHERWISE SPECIFIED

FOLDOUT FRAME 2

REVISIONS						
DISPOSITION CODE: 1 MAY BE REWORKED 2 CANNOT BE REWKD 3 RECORD CHANGE 4 NEW SHOP PRACTICE 5 PARTS MADE OK						
REV LTR	WORD CHGS	DESCRIPTION	MFG EFF	DISP CODE PART	DISP CODE ASSY	APPROVAL & DATE
A		RELEASED FOR PRODUCTION 00144				PJB 8-7-67
B		RELEASED PER E.O. 00159				CAB 5-9-67
C		[illegible] PRODUCTION 00232 & 00255				10-24-67 [illegible]



REFERENCE DESIGNATIONS		
LAST USED	DELETED	OUT OF SEQ
C17	1, 3, 4, 5	C5
CR1		
J2		
L5		
Q6		
R17		R16
T1		

FIGURE 6

QTY PER ASSY	ITEM	PART NO	DESCRIPTION	MATL	MATL SPEC	ZONE	PART SER	QTY	MOD NO	NEXT ASSY	NEXT ASSY	STILL ASSY
							APPLICATION					QTY REQ

LIST OF MATERIAL

CALCULATED WT LB

PART NO

REFERENCE TO SIMILAR DWG

DWG SIZE D

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
.XX = ± .03 | .XXX = ± .010 | X° = 0° ± 30'
WEIGHT IS IN LBS & TENTHS
ALL FINISHED SURFACES 125 PER MIL-STD-10
MFR PER SPEC
TOLERANCE SYMBOLS PER MIL-STD-8
ELECTRICAL SYMBOLS PER MIL-STD-15
MECHANICAL SYMBOLS PER MIL-STD-17
WELDING SYMBOLS PER JAN-STD-19

DRAFT	F. SILVA	7/14/66
DESIGNER		
STRESS & WEIGHT		
CHECKER	T. Boyce	8-9-66
DESIGN ENG	[illegible]	9-9-66
MFG ENG	[illegible]	9-3-67
STDS ENG		
PROJ ENG	[illegible]	9-6-66

TITLE
SCHEMATIC DIAGRAM- ZCG, CURRENT SOURCE MODULE

LAYOUT _____ RELEASE DATE

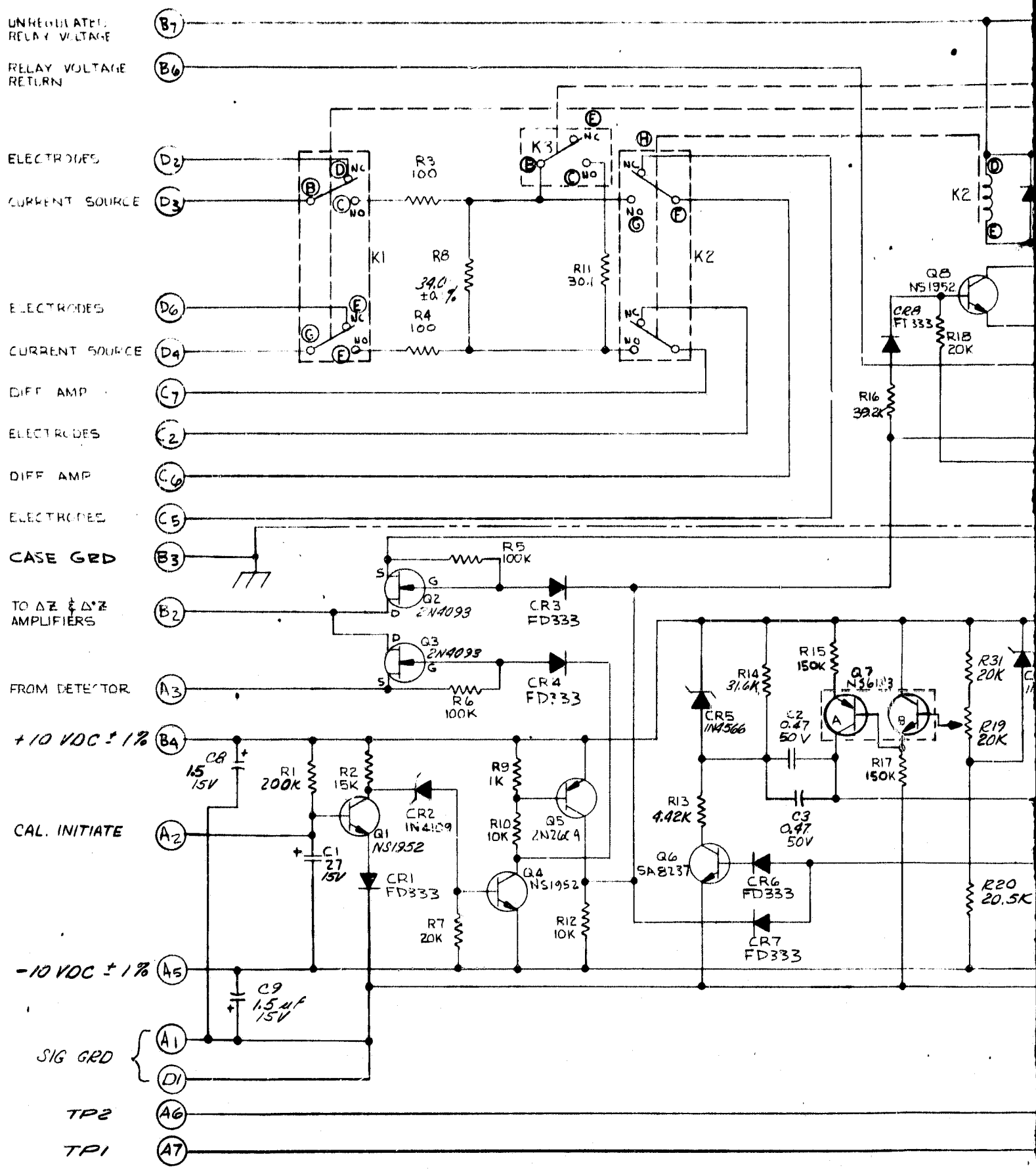
SCALE NONE | WT ACT LB | WT CALC LB

Spacelabs, Inc.
15521 LANARK ST.,
VAN NUYS, CALIFORNIA

DWG NO 104423

REV C

SHEET 1 OF 1



4 ALL CAPACITOR VALUES ARE IN MICROFARADS.

3. ALL RESISTOR VALUES ARE IN OHMS, ± 1% RATED 1/10 W.

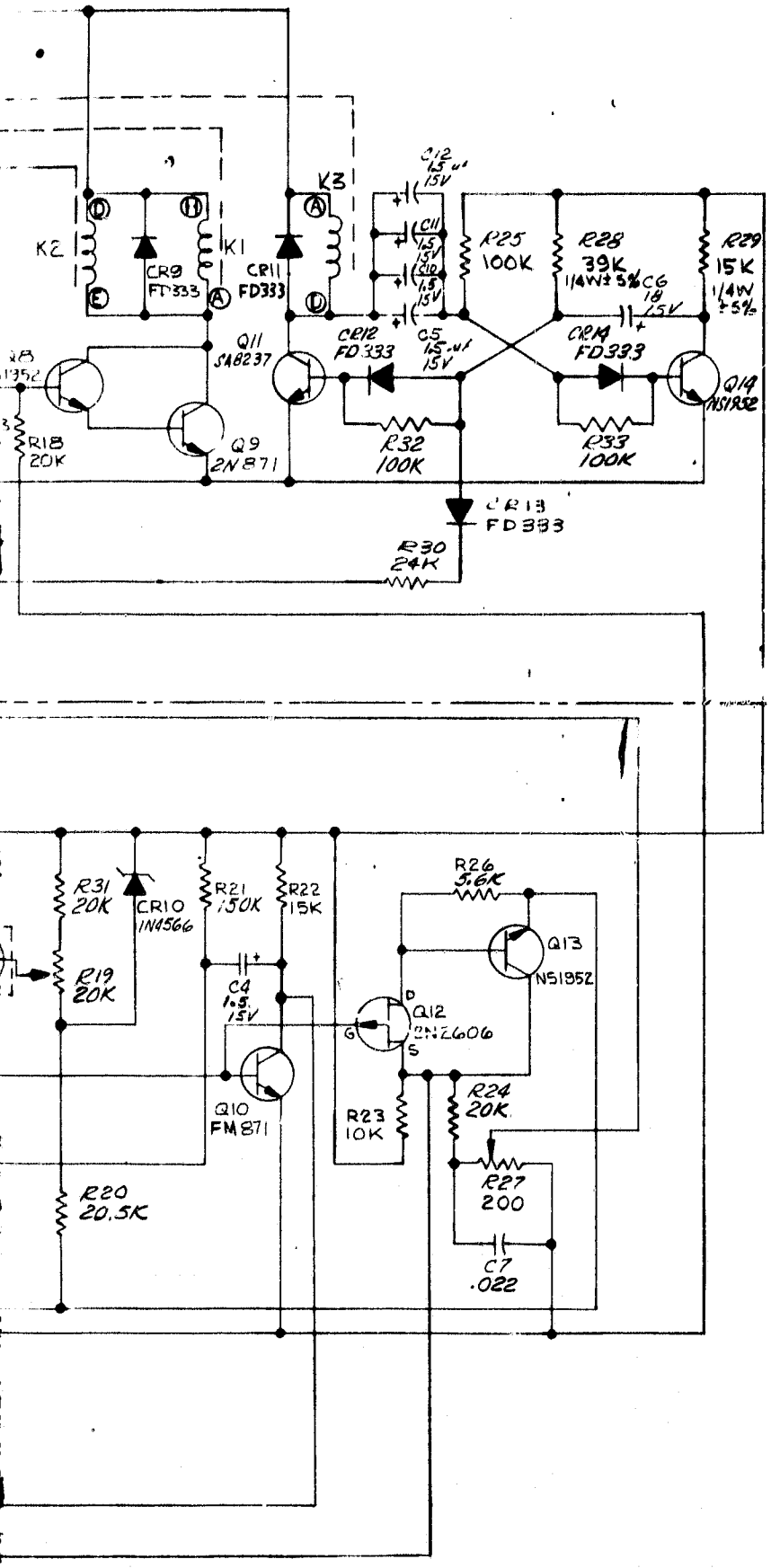
2 PARTIAL REFERENCE DESIGNATION ARE SHOWN; PREFIX WITH UNIT & ASSY DESIGNATION

1 REF DWG NO: ASSY 104426
WIRING DIAGRAM 104409
TEST PROCEDURE 104556

NOTE: UNLESS OTHERWISE SPECIFIED

MOTOROLA DRAWING

REVISIONS						
DISPOSITION CODE:	1 MAY BE REWORKED	2 CANNOT BE REWKD	3 RECORD CHANGE			
	4 NEW SHOP PRACTICE	5 PARTS MADE OK		DISP CODE		APPROVAL & DATE
REV SYM	WORK ORDER	DESCRIPTION	MFG EFF	PART	ASSY	
A		RELEASED FOR PRODUCTION E.O. 00146				CB 5-17-67
B		REVISED PER EO 00274				11-29-67



R F SHIELDING

REFERENCE DESIGNATIONS		
LAST USED	DELETED	OUT OF SEQ
C12		
CR14		
J3		
K2		
Q14		
R33		R30, R31

FIGURE 7

QTY PER ASSY	ITEM	PART NO	DESCRIPTION	MATL	MATL SPEC	ZONE

LIST OF MATERIAL

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE: .XX = ± .03 | .XXX = ± .010 | ANGLES = 0° ± 30'
WEIGHT IS IN LBS & TENTHS
ALL FINISHED SURFACES 125 PER MIL-STD-10

CALCULATED WT LB: 1 0 4 4 2 8

PART NO

MFR PER SPEC

REFERENCE TO SIMILAR DWG

DWG SIZE: D

TOLERANCE SYMBOLS PER MIL-STD-8
ELECTRICAL SYMBOLS PER MIL-STD-15
MECHANICAL SYMBOLS PER MIL-STD-17
WELDING SYMBOLS PER JAN-STD-19

DRAFT	F SILVA	7-5-66
DESIGNER		
STRESS & WEIGHT		
CHECKER	[illegible]	9/6/66
DESIGN ENG	[illegible]	9/9
MFG ENG		
SYDS ENG		
PROJ ENG	[illegible]	9-6-66

TITLE: SCHEMATIC DIAGRAM- ZCG, CALIBRATE MODULE

LAYOUT _____ RELEASE DATE _____

SCALE NONE | WT ACT _____ LB | WT CALC _____ LB

Spacelabs, Inc.
15521 LANARK ST.,
VAN NUYS, CALIFORNIA

DWG NO 104428 REV B

SHEET 1 OF 1

PART NO	QTY	DWG NO	NEXT ASSY	NEXT ASSY	FINAL ASSY
APPLICATION				QTY REQ	

J1
ME-95185

△Z OUTPUT 7
SIGNAL COMMON 1
+10VDC 4
CASE GROUND 3
INPUT (FROM CALIB MODULE) 2
−10VDC 5
△Z OUTPUT 6

R8 3.01K
Q19 2N2605
R14 3.01K
R19 20.0
C6 .056, 50V
R2 75.0K
R9 3.32K
Q3 2N3805
R15 3.32K
Q7 2N2605
CR8 1N746A
C16 .0015 50V
C7 6.8 10V
R20 14.3K ±0.1%
R35 200
Q12 2N2605
Q4 2N2605
R24 887K ¼W, ±0.1%
C17 .01
Q4 2N3934
CR2 1N457
R5 1.00K
C14 1000pf. 50V
R25 39.2K
R27 15.0K
Q11 2N4093
R29 2.00K
C2 1.5, 15V
R3 23.3K
R57 (3)
R6 6.2 MEG ¼W
C12 0.25 50V
C4 0.25 50V
C5 1.5 15V

R4 5.62K
Q2 2N2604
Q1 N51952
R10 3.01K
R16 5.01K
R11 3.32K
R17 3.32K
Q5 2N3805
Q20 2N2605
R21 20.0
C8 .056, 50V
Q9 2N2605
CR9 1N752A
Q10 2N2605
Q21 2N2605
R40 3.01K
R41 3.32K
Q1 2N3
C3 0.47, 50V ±0.25%
R42 100
Q6 2N3934
R1 20.0K
R26 39.2K
R28 5.11K
R32 1.05K
R34 4.12K
R36 44.2K ±0.1%
R38 316K ±0.1%
C9 1.5, 15V
10 0.47 35V
R18 8.06K
R44 (3)(11)
R22 90.9K
R23 4.75K
CR1 IN4565
C13 1000pf 50V
R7 1 MEG ¼W ±0.1%
R13 8.2K
C1 1.5, 15V
R58 10.0K ±1%

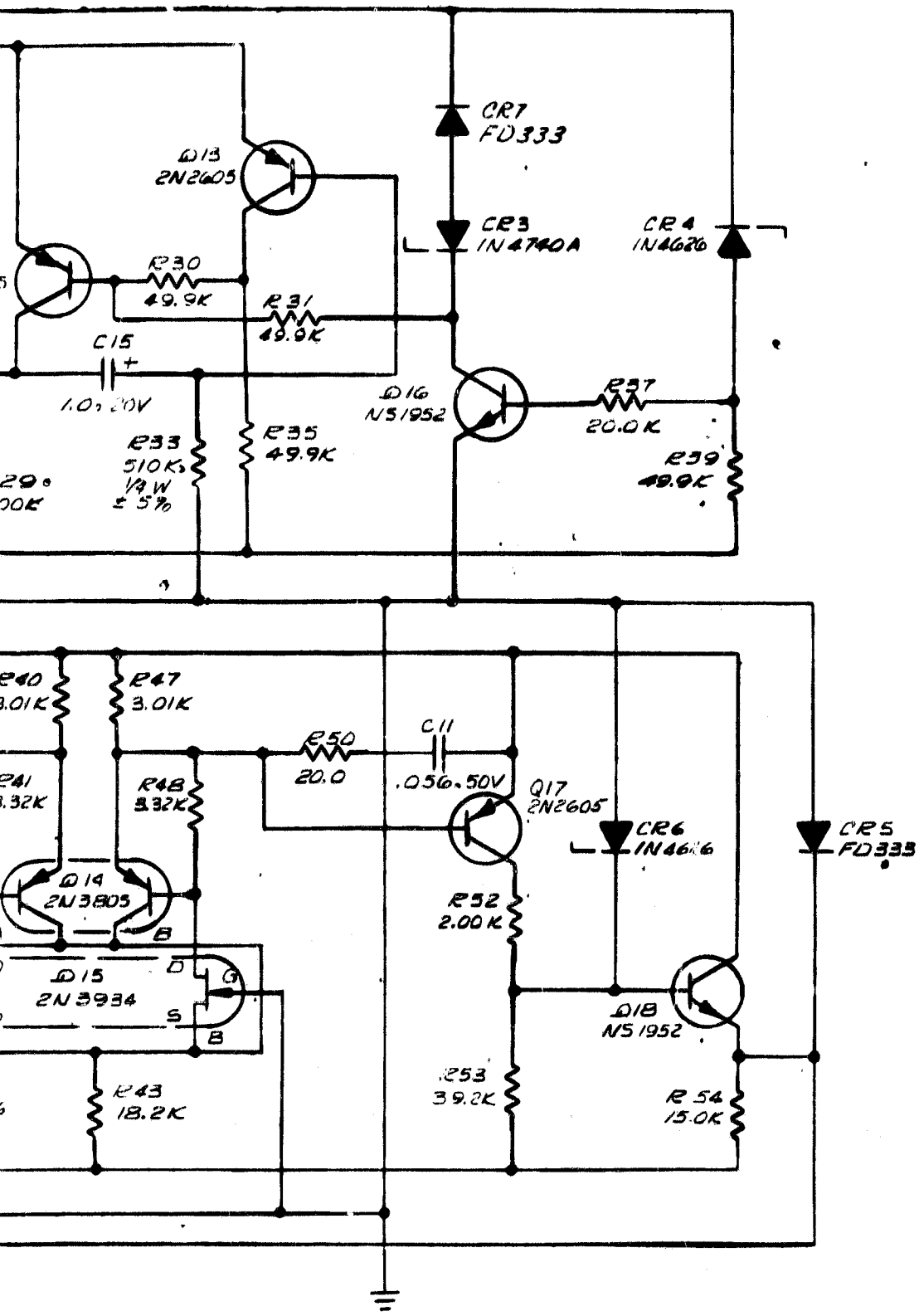
REFERENCE DESIGNATION		
MST USED	DELETED	OUT OF
C17		SCHE
R52	1212	HAS
CR3		VISEL
Q21		QUEST
J-1	———	BEEN
		CKWI

(11) FOR COMPONENT SELECT PROCEDURE SEE DWG NO 104261
10. FOR COMPONENT PARTS ASS'Y. SEE DWG. NO. 104911
9. FOR MYLAR HOLE PATTERN. COMPONENT PARTS BOARD, SEE DWG NO. 104412.
8. FOR FINAL ASS'Y. SEE DWG. NO. 104442.
7. FOR OUTLINE DWG. SEE DWG. NO 104491.
6. FOR ECG SYSTEM WIRING DIAGRAM SEE DWG NO 104407
5. FOR PARTS LIST SEE DWG. NO. PL 104414
4. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN FOR COMPLETE DESIGNATION PREFIX WITH ASS'Y & UNIT DESIGNATION
(3) VALUE TO BE DETERMINED AT ELECTRICAL TEST.
2. ALL CAPACITANCE VALUES IN MICRO FARADS, ± 10%
1. ALL RESISTANCE VALUES IN OHMS, ±1%, RATED 1/10 W.

NOTES: UNLESS OTHERWISE SPECIFIED.

BLOCK DIAGRAMS 2

REVISIONS					
DISPOSITION CODE: 1 MAY BE REWORKED; 2 CANNOT BE REVISED; 3 OBSOLETE CHANGE; 4 NEW SHOP PRACTICE; 5 PARTS MADE OBSOLETE					
REV LTR	ZONE	DESCRIPTION	MFG EFF	DISP CODE PART	DISP CODE ASSY	APPROVAL & DATE
N/C		PRODUCTION RELEASE EO 00211				6/27/67
A		REVISED PER EO 00206				8/9/67
b		REVISED PER EO 00 267				9/8
C		REVISED PER EO 00460				



DESIGNATIONS	
	OUT OF SEQUENCE
	SCHEMATIC HAS BEEN RE-VISED & NO SE-QUENCE HAS BEEN INCORP-ORATED

FIGURE 8

QTY PER ASSY	ITEM	PART NO	DESCRIPTION	MATL	MATL SPEC	ZONE

LIST OF MATERIAL

APPLICATION

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE: .XX = ± .03, .XXX = ± .010, X° = 0° ± 30'
WEIGHT IS AS LBS & TENTHS
ALL FINISHED SURFACES 125 PER MIL-STD-10
MFR PER SPEC
TOLERANCE SYMBOLS PER MIL-STD-8
ELECTRICAL SYMBOLS PER MIL-STD-15
MECHANICAL SYMBOLS PER MIL-STD-17
WELDING SYMBOLS PER MIL-STD-22

CALCULATED WT LB: 1 0 4 4 1 3
PART NO
REFERENCE TO SIMILAR DWG
DWG SIZE: D

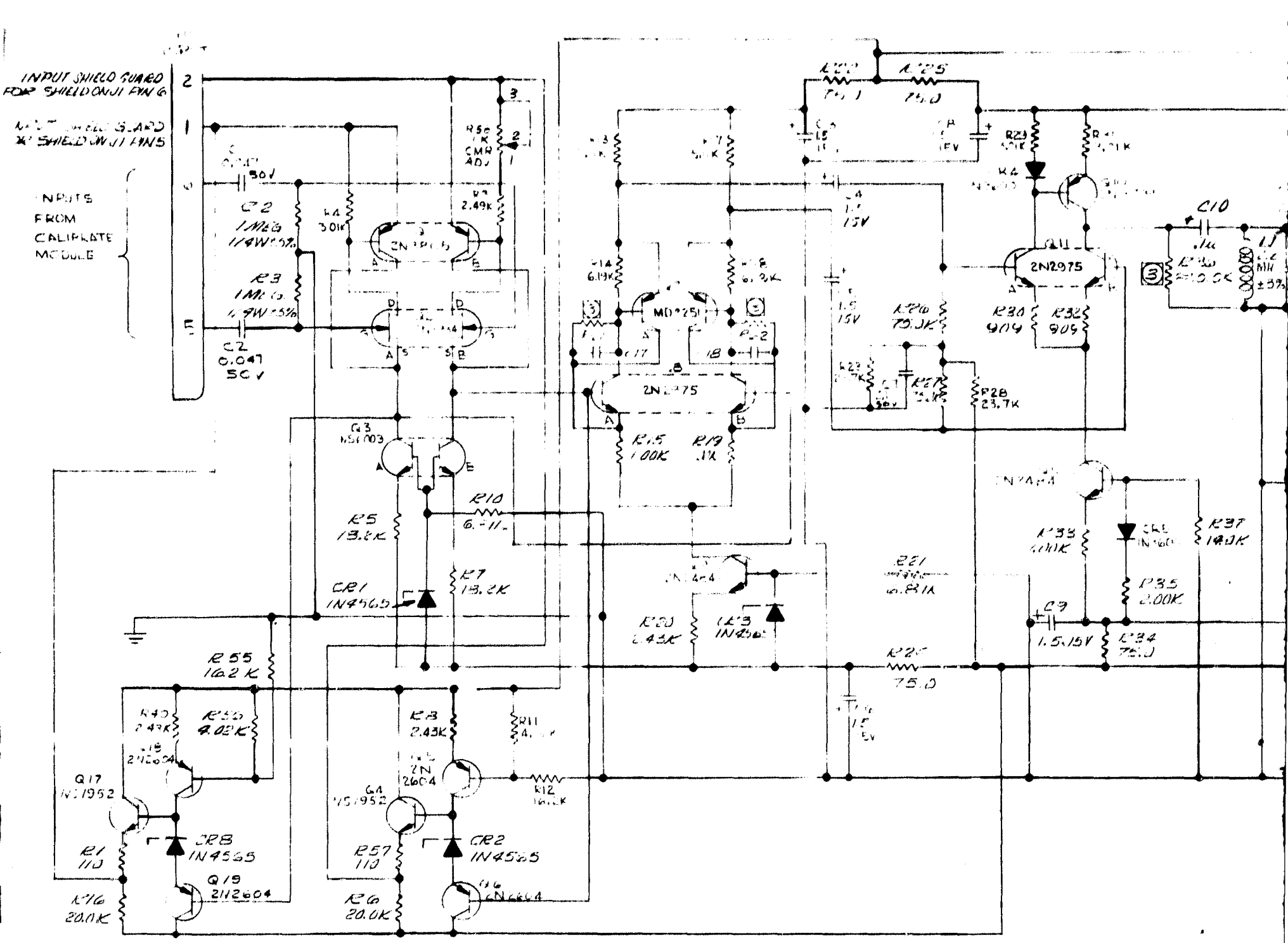
DRAFT	[illegible]	8/2/67
DESIGNER		
STRESS & WEIGHT		
CHECKER		
DESIGN ENG	[illegible]	9/1/67
MFG ENG	[illegible]	9/3/67
STDS ENG		
PROJ ENG	[illegible]	9/8/67

TITLE: SCHEMATIC DIAGRAM, △Z & △°Z OUTPUT AMPLIFIER-(ZCG)

LAYOUT: RELEASE DATE:
SCALE: NONE WT LB WT LB

Spacelabs, Inc.
18521 LANARK ST.
VAN NUYS, CALIFORNIA

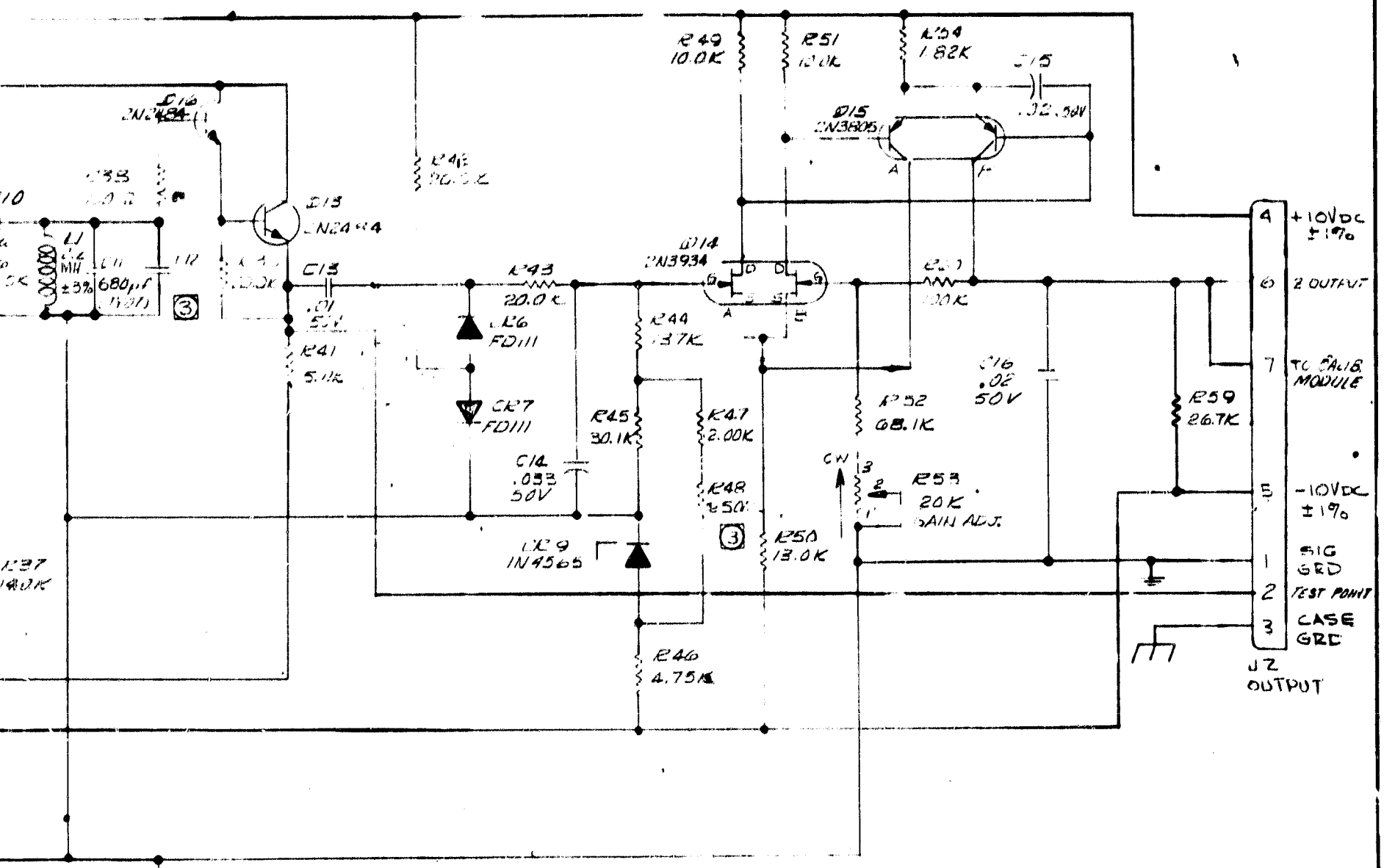
DWG NO 104413
REV C
SHEET 1 OF 1



10. FOR COMPONENT PARTS ASS'Y. SEE DWG NO. 104416.
9. FOR MYLAR ARTWORK PATTERN, COMPONENT PARTS BOARD SEE DWG. NO. 104417.
8. FOR FINAL ASSY SEE DWG NO. 104415.
7. FOR OUTLINE DWG. SEE DWG NO. 104414.
6. FOR ECG SYSTEM WIRING DIAGRAM SEE DWG. NO. 104409.
5. FOR PARTS LIST SEE DWG NO. PL 104419.
4. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR COMPLETE DESIGNATION PREFIX WITH ASSY & UNIT DESIGNATION.
(3.) VALUE TO BE DETERMINED AT ELECTRICAL TEST (C12 & R48) (RG1, RG2, C17 & C18 TO BE USED INDIVIDUALLY OR IN COMBINATION AS REQUIRED. (MAY NOT BE REQUIRED)
2. ALL CAPACITANCE VALUES IN MICROFARADS.
1. ALL RESISTANCE VALUES IN OHMS, ± 1%, RATED 1/10 W.

NOTES: UNLESS OTHERWISE SPECIFIED.

REVISIONS						
DISPOSITION CODE: 1 MAY BE REWORKED; 2 CANNOT BE REWORKED; 3 OBSOLETE CHANGE; 4 NEW SHOP PRACTICE; 5 PARTS MADE ON				DISP CODE		APPROVAL & DATE
REV LTR	VALUE CODE	DESCRIPTION	MFG EFF	PART	ASSY	
A		RELEASED PER ECO 00198				
B		REVISED PER ECO 00250				
C		REVISED PER ECO 00258				
D		REVISED PER ECO 00000				



REFERENCE DESIGNATIONS		
LAST USED	DELETED	REVISED SCHEMATIC NO SEQUENCE.
C 18	C	
CR 9	CR	
Q 16	Q	
R 62	R-10 PER	
J 2	—	

FIGURE 9

QTY PER ASSY	ITEM	PART NO	DESCRIPTION	MATL	MATL SPEC	ZONE

LIST OF MATERIAL

CALCULATED WT LB: 10418

PART NO

REFERENCE TO SIMILAR DWG

DWG SIZE: D

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
.XX = ± .02 | .XXX = ± .010 | ∠ = 0° ± 30'
WEIGHT IS IN LBS & TENTHS
ALL FINISHED SURFACES 125 PER MIL-STD-10
MFR PER SPEC
TOLERANCE SYMBOLS PER MIL-STD-8,
ELECTRICAL SYMBOLS PER MIL-STD-15
MECHANICAL SYMBOLS PER MIL-STD-17
WELDING SYMBOLS PER MIL-STD-19

DRAFT	R. MILLER	9/16/67
DESIGNER	C. HALEY	9/16/67
STRESS & WEIGHT		
CHECKED	R. HALEY	9/16/67
DESIGN ENG		
MFG ENG	Paul	9/24/67
SYS ENG		
PROJ ENG		

TITLE: SCHEMATIC DIAGRAM DIFF. AMPL. & DETECTOR (ZCG)

LAYOUT | RELEASE DATE

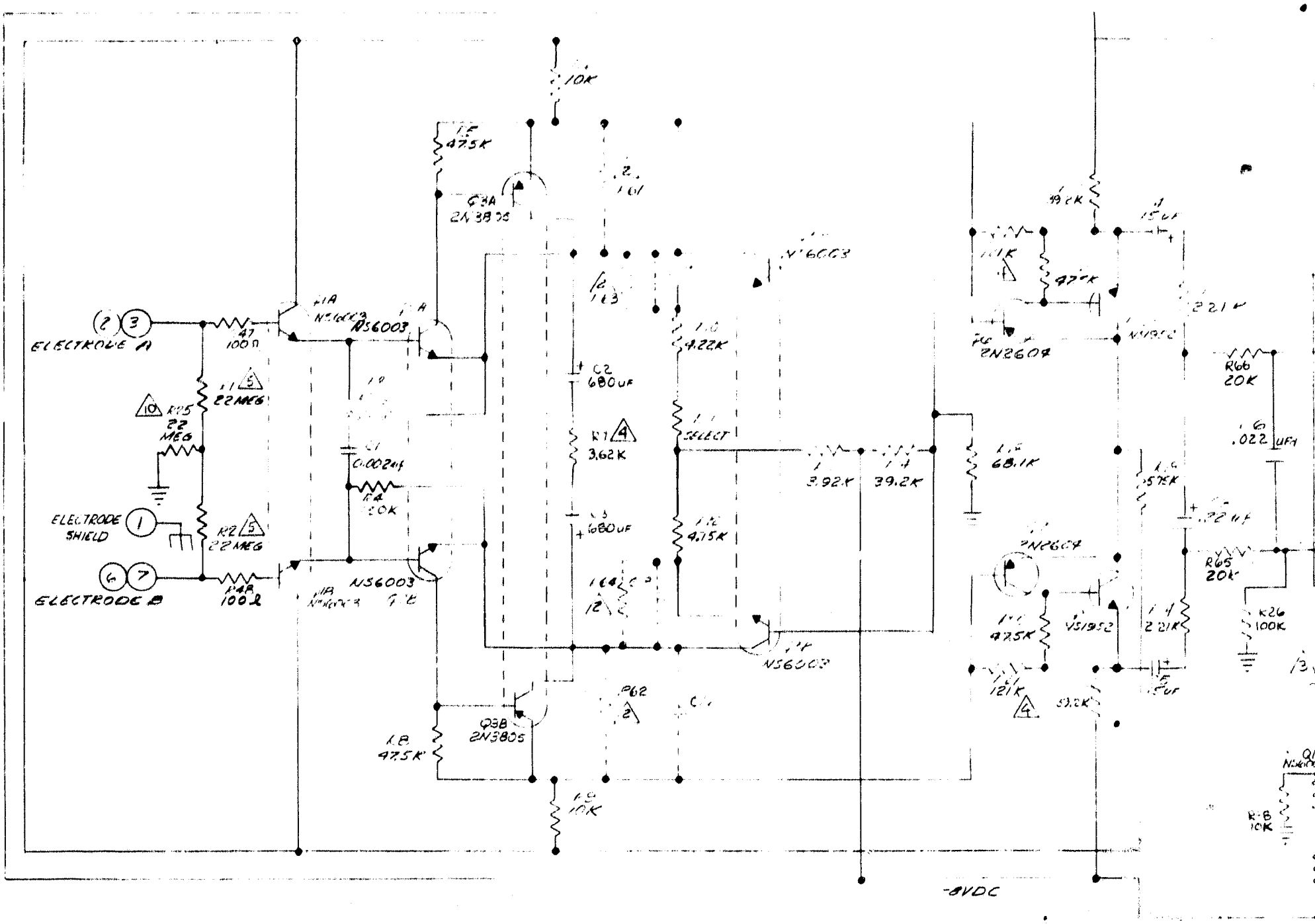
SCALE NONE | WT | WT SHEET | LB | SHEET | OF

Spacelabs, Inc.
(552) LANARK 8
VAN NUYS, CALIFORNIA

DWG NO 10418 | REV D

PART NO | QTY | DWG NO | ITEM | PART NO | APPLICATION | QTY REQ

10418



10. RESISTORS NOTED ARE 1/4 WATT, ±5% CARBON COMP
9. FOR FINAL ASSEMBLY SEE DWG 104225
8. ALL CAPACITANCE VALUES ARE ±10%
7. FOR ENGR. PARTS LIST SEE DWG 104221
6. FOR OUTLINE DRAWING SEE 104220
5. MATCHED PAIR PER SPEC. 601400
4. RESISTORS NOTED ARE ±50 PPM PER °C
3. RESISTORS NOTED ARE 1/10 W, ±1% METAL FILM SELECT VALUE PER 102844
2. DOTTED COMPONENTS ARE SELECTED PER 102844
1. RESISTORS ARE METAL FILM 1/10 WATT, ± 1.0%.

NOTES: UNLESS OTHERWISE SPECIFIED

LEGEND

INPUT CONNECTOR

OUTPUT CONNECTOR

CAST SYMBOL USED	SYMBOLS NOT USED
1.66	R27, R39
1.75	Q4
1.8	C7, C13
1.6	
5.N1	

3/65 DIETERICH-POST CLEARPRINT 1020-9

FOLDOUT FRAME 2

REVISIONS								
DISPOSITION CODE		1 MAY BE RE-WORKED		3 CANNOT BE REWORKED		RECORD CHANGE		
		4 NEW SHOP PRACTICE		5 PARTS MADE OBSOLETE		DISP CODE	APPROVAL & DATE	
DOV SYM	WORK CODE	DESCRIPTION		MFG ECP		PART	ASSY	

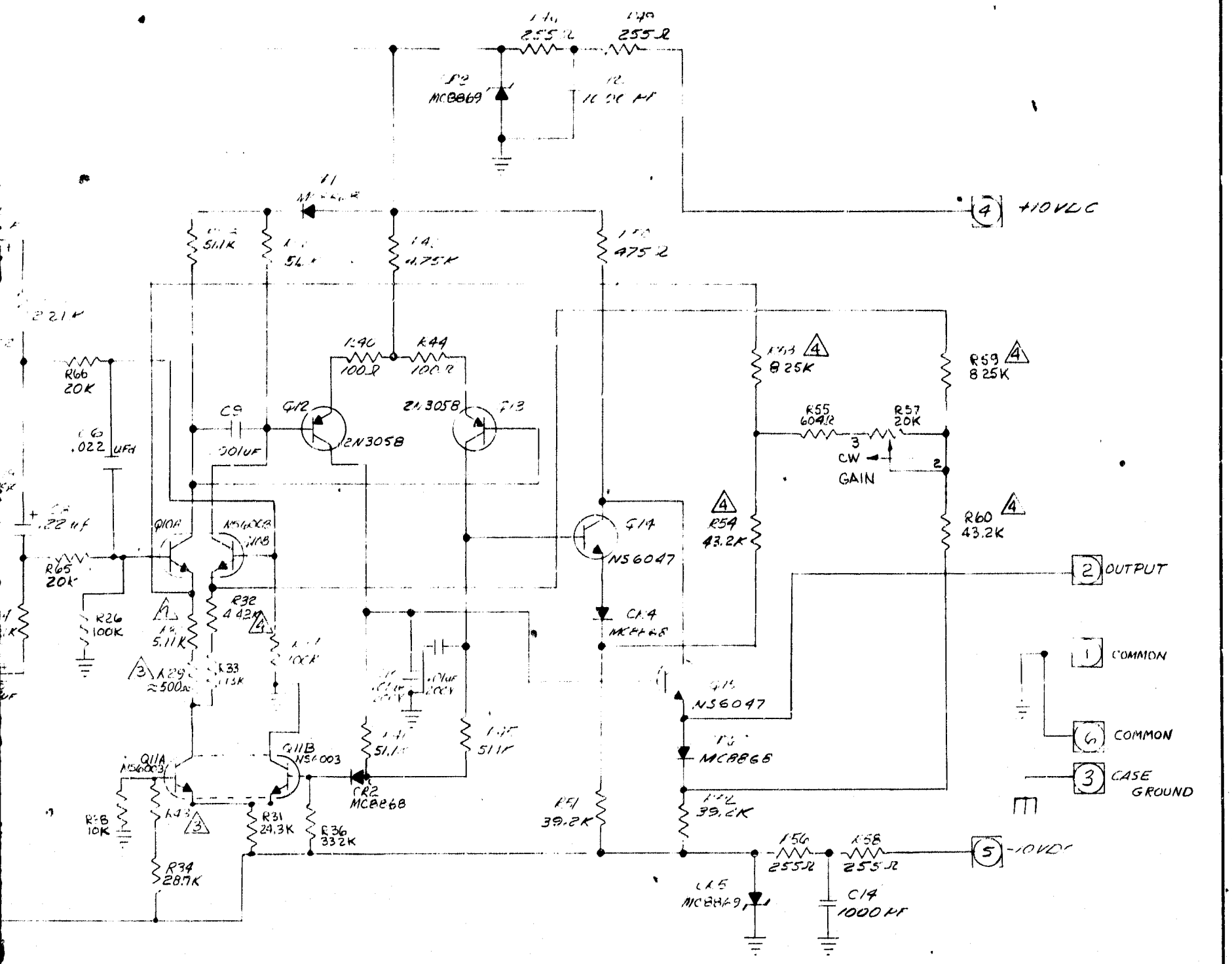


FIGURE 10

LAST SYMBOL USED	SYMBOLS NOT USED
1.66	R27, R39
D5	Q9
C8	C7, C13
K6	
SW1	

QTY PER ASSY	ITEM	PART NO	DESCRIPTION	MATL	MATL SPEC	ZONE

LIST OF MATERIAL

PART NO	ECP	MOD NO	NEXT ASSY	NEXT ASSY	FINAL ASSY	QTY REQ
APPLICATION						

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
.XX = ± .03 | .XXX = ± .010 | X° = 0° ± 30'
WEIGHT IS IN LBS & TENTHS
ALL FINISHED SURFACES = 125 √ PER MIL-STD-10

CALCULATED WT LB: 10423
PART NO
MFR PER SPEC
REFERENCE TO SIMILAR DWG
DWG SIZE D

TOLERANCE SYMBOLS PER MIL-STD-8
ELECTRICAL SYMBOLS PER MIL-STD-15
MECHANICAL SYMBOLS PER MIL-STD-17
WELDING SYMBOLS PER JAN-STD-19

DRAFT	[illegible]	9-9-66
DESIGNER		
STRESS & WEIGHT		
CHECKER		
DESIGN ENG	[illegible]	9-9-66
MFG ENG		
STDS ENG		
PROJ ENG	[illegible]	9-28-66

TITLE
SCHEMATIC DIAGRAM
ECG SIGNAL CONDITIONER
BLOCK II APOLLO

LAYOUT | RELEASE DATE
SCALE | WT ACT LB | WT CALC LB

Spacelabs, Inc.
15521 LANARK ST.,
VAN NUYS, CALIFORNIA

DWG NO 104223
REV —
SHEET 1 OF 1

APPENDIX D

COMMON-MODE-REJECTION ANALYSIS

FACTORS IN CMR RATIO DEGRADATION

VCG SUBSYSTEM

INTRODUCTION

This brief technical discussion of factors in CMR ratio is related to the VCG Subsystem performance, and represents the kind of analysis carried out in performance of the contract. Results are graphically presented in Figures 4, 5, and 6.

Figure 1 depicts a differential amplifier supplied by differential (e_d) and common mode (e_o) signal sources exhibiting output impedances, R_a and R_b. The input impedance of the amplifier is assumed balanced and has a value, each input to common, of R.

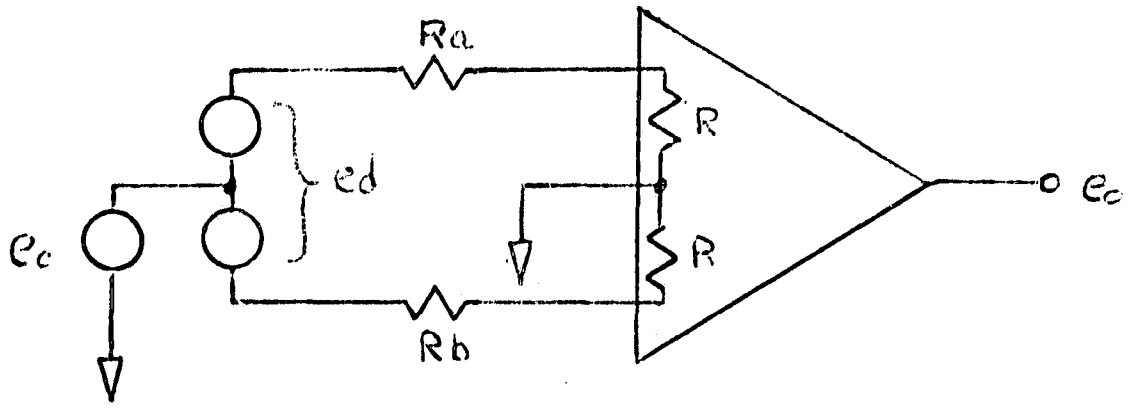


FIGURE 1

Since the common mode performance is the object of this discussion, assume that e_d is zero, as shown in Figure 2.

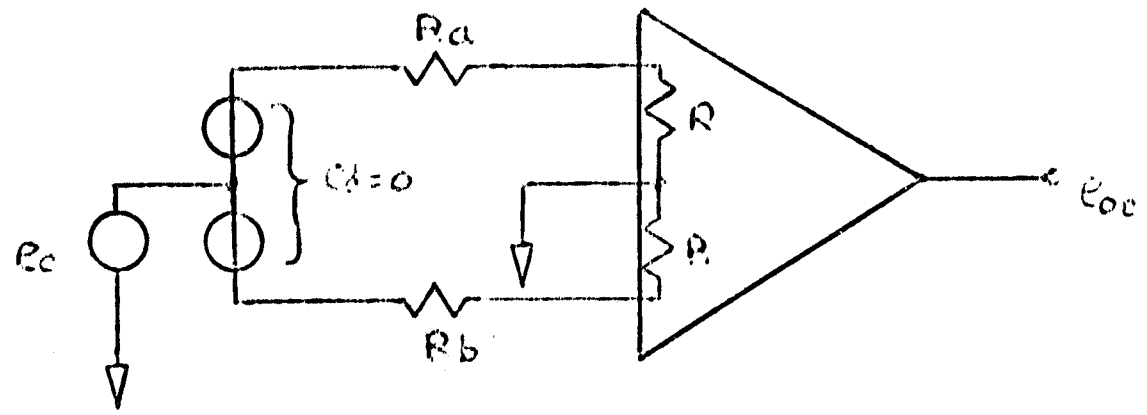


FIGURE 2

The common mode rejection ratio is defined as:

$$\frac{A_d}{A_c},$$

where:

A_d is the differential gain, and

A_c is the common mode gain.

Expressed in db,

$$db_{(CMR)} = 20 \log_{10} \frac{A_d}{A_c} \qquad (1)$$

If we assume an ideal differential amplifier with infinite common mode rejection, any output voltage resulting from the application of the common mode voltage, e_c, is due to the difference in the voltages appearing at the input terminals of the amplifier, multiplied by the differential gain, A_d. The difference in voltages is

the result of unbalanced voltage dividers $\frac{R}{R + R_a}$ and $\frac{R}{R + R_b}$.

The voltage at the input terminals then is the output voltage, e_{oc}, divided by the differential gain, A_d, or:

$$e_{in} = \frac{e_{oc}}{A_d} \tag{2}$$

The input voltage, e_{in}, as generated by unbalanced input voltage dividers is:

$$e_{in} = \frac{e_c R}{R + R_a} - \frac{e_c R}{R + R_b}$$

or:

$$e_{in} = \frac{e_c R (R_b - R_a)}{(R + R_a)(R + R_b)} = K e_c \tag{3}$$

where:

$$K = \frac{R (R_b - R_a)}{(R + R_a)(R + R_b)}$$

Equating (2) and (3),

$$K e_c = \frac{e_{oc}}{A_d} \tag{4}$$

The common mode gain for the system is the ratio of the common mode output voltage, e_{oc}, to the common mode input voltage, e_c.

That is:

$$A_c = \frac{e_{oc}}{e_c} \tag{5}$$

This ratio from Equation (4) is:

$$A_c = \frac{e_{oc}}{e_c} = KA_d \tag{6}$$

Substituting $A_c = KA_d$ in Equation (1), the definition of common mode rejection ratio,

$$db_{(CMR)} = 20 \log_{10} \frac{1}{K}$$

For convenience, let $\frac{1}{K}$ be expressed as a power (σ) of 10.

$$\frac{1}{K} = 10^{\sigma} \tag{7}$$

Then,

$$db_{(CMR)} = 20\,(\sigma)$$

For a given common mode rejection Q,

$$\sigma = \frac{Q}{20} \tag{8}$$

Substituting for K and σ in Equation (7),

$$\frac{1}{\frac{R\,(R_b - R_a)}{(R + R_a)\,(R + R_b)}} = 10^{Q/20}$$

or:

$$\frac{(R + R_a)\,(R + R_b)}{R\,(R_b - R_a)} = 10^{Q/20} \tag{9}$$

If we let $R_a = \gamma R_b$, where $0 \leq \gamma \leq 1$, then:

$$\frac{R_b \left(\frac{R}{R_b} = \gamma\right)\left(\frac{R}{R_b} + 1\right)}{R\,(1 - \gamma)} = 10^{Q/20}$$

Now assume that $\frac{R}{R_b} \geq\geq 1$, then:

$$\frac{R}{R_b\,(1 - \gamma)} = 10^{Q/20} \tag{10}$$

The percentage deviation of R_a from R_b is:

$$\rho = \frac{R_b - R_a}{R_b}\ (10^2)$$

Since $R_a = \gamma R_b$,

$$\rho = (1 - \gamma)\ 10^2 \tag{11}$$

Solving for $(1 - \gamma)$ in Equation (10),

$$1 - \gamma = \frac{R}{R_b}\ 10^{-Q/20}$$

$$\rho = (1 - \gamma)\ 10^2 = \frac{R}{R_b}\ 10^{-Q/20 + 2}$$

$$\rho = \frac{R}{R_b}\ 10^{-\left(\frac{Q - 40}{20}\right)} \tag{12}$$

A similar analysis of the general case shown in Figure 3 results in:

$$(1 - \gamma\beta) = \frac{(Z_b + Z_c + Z_d)}{Z'}\ 10^{-Q/20} \tag{13}$$

where:

$$Z' = \frac{1}{\frac{1}{Z_b} + \frac{1}{Z_c} + \frac{1}{Z_d}}$$

$$\gamma = \frac{Z_a}{Z_b}$$

$$\beta = \frac{Z_e}{Z_d}$$

Q = common mode rejection ratio in db

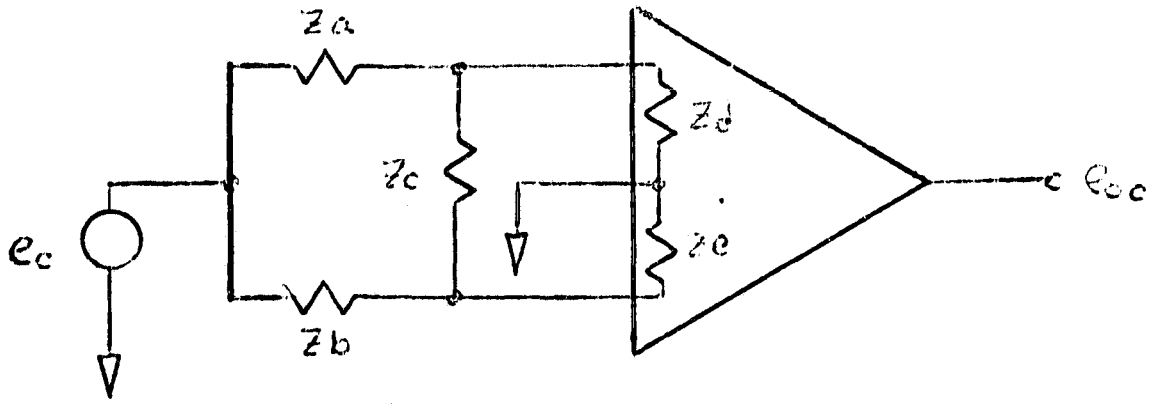


FIGURE 3

Figure 4 graphically illustrates the relationship between common mode rejection and percent unbalance in the series resistances R_a and R_b under the conditions

$$P = \frac{R}{R'} 10^{-\left(\frac{Q-40}{20}\right)}$$

where P = % difference in series resistances R_a & R_b

R = amplifier input resistance each lead to common

Q = CMR in db

$$R' = \frac{1}{\frac{1}{R} + \frac{1}{R_b} + \frac{1}{R_c}}$$

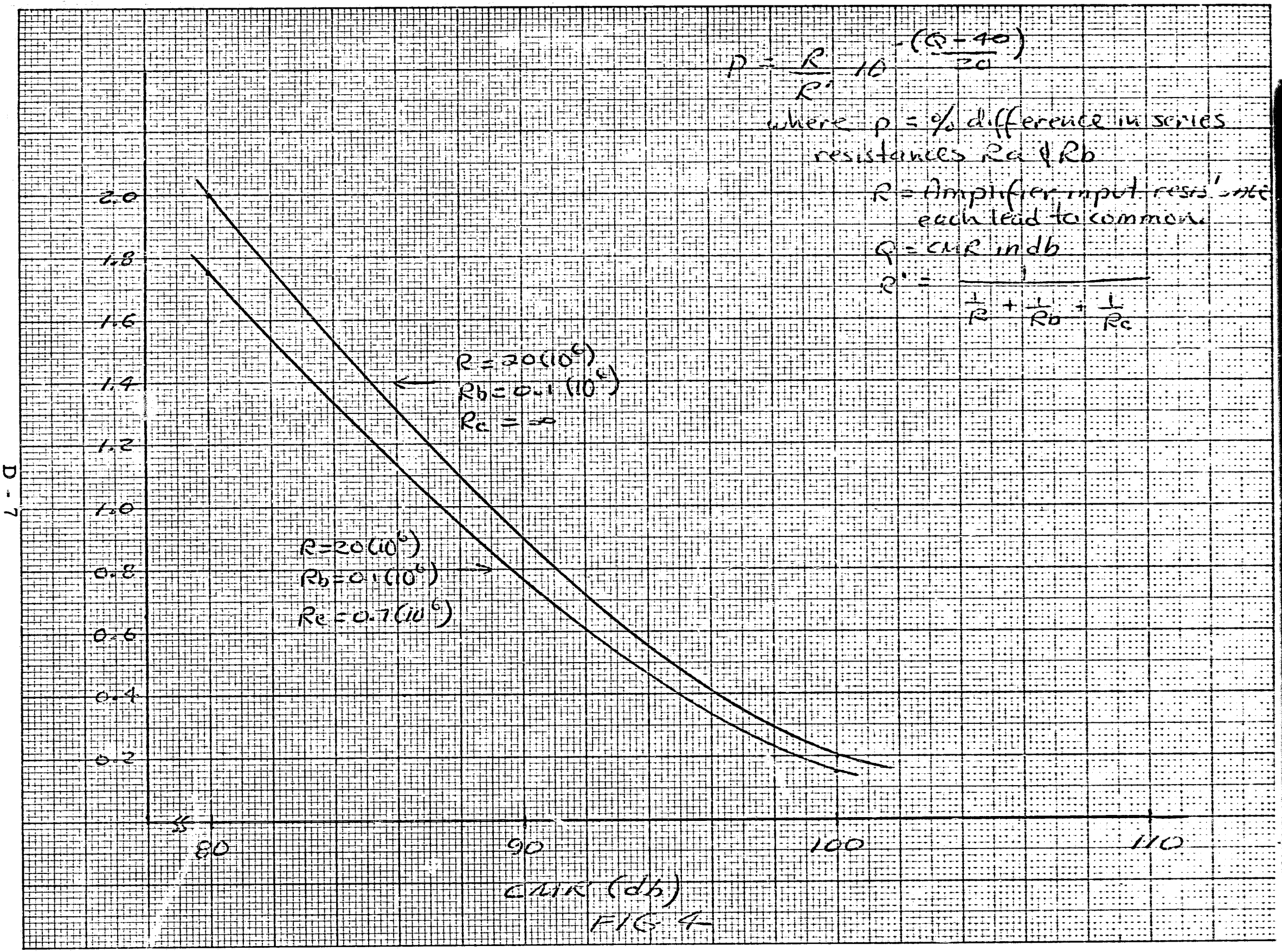


FIG 4

D - 7

indicated in Figure 2. The curve for finite R_c is derived from the general Equation (13).

The effect of stray capacitance in the Frank Lead Network can be simply shown by assuming that this stray capacitance is lumped and placed in parallel with the input resistance R. This input resistance then becomes Z_d and Z_e as shown in Figure 3. To avoid complication, assume that Z_c is infinite and that $Z_a = R_a$, $Z_b = R_b$.

From Equation (13),

$$\gamma\beta \approx 1 - \frac{Z_d}{R_b} \; 10^{-Q/20}$$

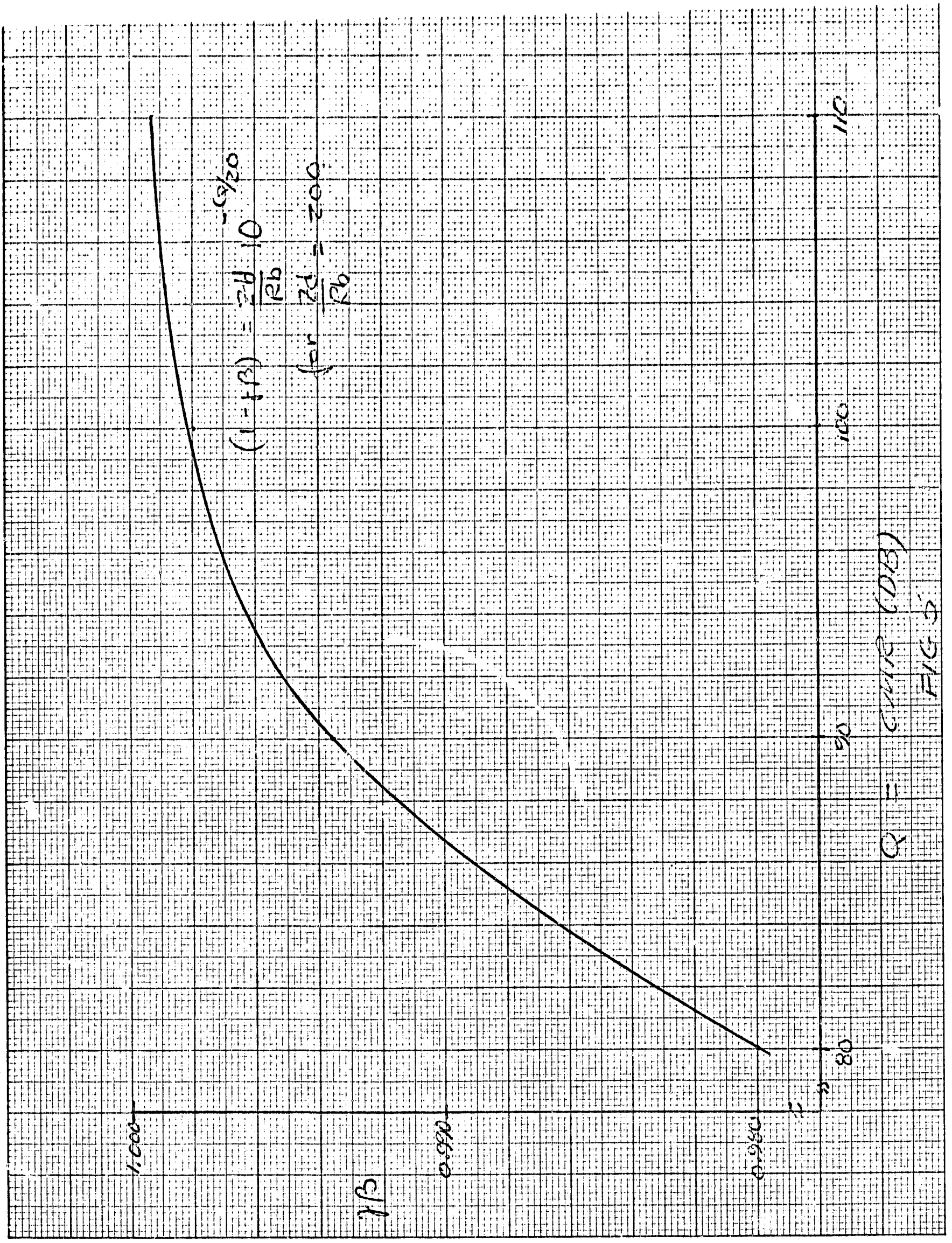
This equation is graphically presented in Figure 5 for various values of $\frac{Z_d}{R_b}$ and Q. If the amplifier is not ideal from the standpoint of CMR, additional system CMR degradation occurs.

This modifies Equation (13) to include the factor $10^{-A/20}$ as shown in Equation (17). The derivation consists of changing e_{oc} to e_{oc}':

$$e_{oc}' = \left[\left(\frac{e_{oc}}{A_d} \right) + K e_c \right] A_d \qquad (14)$$

where:

$\frac{e_{oc}}{A_d}$ represents the differential voltage appearing at the output as referred to the input, resulting from a non-ideal amplifier. This term is added to the term representing the differential voltage produced by the unbalanced input network.



Then:

$$e_{oc}' = e_c \left[\frac{A_c}{A_d} + K \right] A_d$$

$$e_{oc}' = A_c' e_c = e_c \left[\frac{A_c}{A_d} + K \right] A_d$$

from which:

$$A_c' = \left[\frac{A_c}{A_d} + K \right] A_d \qquad (15)$$

where:

A_c' represents the overall common mode gain.

Substitution into Equation (1) yields:

$$Q' = db_{(overall)} = 20 \log_{10} \frac{A_d}{A_c'}$$

From Equation (15),

$$Q' = 20 \log_{10} \frac{1}{\frac{A_c}{A_d} + K}$$

As in Equation (7), let

$$\frac{1}{\frac{A_c}{A_d} + K} = 10^{\sigma'} = 10^{Q'/20}$$

Then,

$$\frac{1}{\frac{A_c}{A_d} + K} = 10^{Q'/20}$$

$$\frac{A_c}{A_d} + K = 10^{=Q'/20}$$

$$K = 10^{-Q'/20} - \frac{A_c}{A_d} \qquad (16)$$

Since,

$$db_{(amp)} = 20 \log_{10} \frac{A_d}{A_c}$$

Let,

$$db_{(amp)} = A \quad \text{and} \quad \frac{A_d}{A_c} = 10^{\Delta}$$

Then,

$$A = 20\Delta$$

or,

$$\frac{A_d}{A_c} = 10^{-A/20}$$

Substituting into Equation (16),

$$K = 10^{-Q'/20} - 10^{A/20}$$

this reduces to,

$$(1 - \gamma\beta) = \frac{(Z_b + Z_c + Z_d)}{Z'} (10^{-Q'/20} - 10^{-A/20}) \qquad (17)$$

NO. 318. 20 DIVISIONS PER INCH BOTH WAYS. 150 BY 200 DIVISIONS.
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