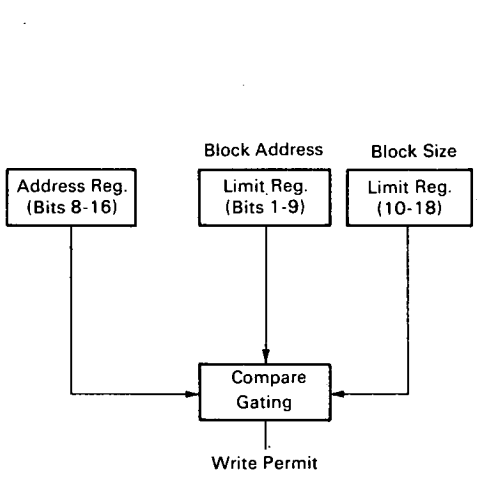
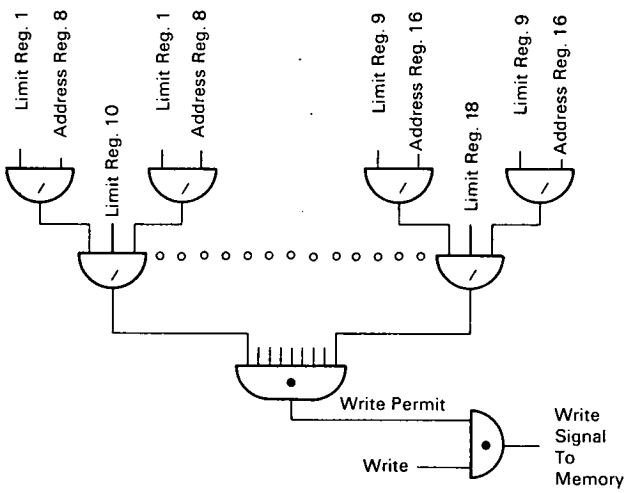
NASA TECH BRIEF

Circuitry Selectively Limits Data Storage in General Purpose Computer





Circuitry has been designed to implement the concept of limiting storage in the memory of a stored program general purpose digital computer. Although limiting storage is not new, the implementation and way the storage limit register is used are unique. The idea is to permit storage or writing to certain, specified areas of memory. The design has been incorporated into an 18-bit word length computer with a maximum of 64K storage; however, it would apply to any machine where limiting storage is necessary.

Since it is most efficient (from a hardware and programming standpoint) to use a register of the word length of the machine, this was the goal of this design. The register (here known as a limit register) is broken up into two nine-bit fields. The first field indicates the amount of memory (size of block) in which storage is permitted and the second field indicates specifically where in memory (which block) the storage is to be permitted. A block diagram of this circuitry is shown in the left figure.

The nine most significant bits of the address register are compared to limit register bits one to nine. If there is a compare, a write permit occurs and thus the computer is permitted to write in the location specified by the address register. Since bits one–seven of the address are not compared, then any memory location in a block of 128 words with the comparable nine bits can be written into. Any block of 128 may be specified and thus any word in the entire memory may be written or not written into by this means. The above description is true if the limit register, bits 10 to 18, contains all ones. If block size portion of the register does not contain all ones, the block in which writing is permitted becomes larger. For example, if the first bit is a zero, the block size is 256 bits and any such block in memory may be specified by the first nine bits of the limit register. A condition of all zeros in the second field permits storage in the entire 64K of memory.

The implementation of this is shown in the right

(continued overleaf)

figure. Three gates are required per bit of compare. The two gates compare the limit register to the address, a third gate enters the field size into the compare. If a zero exists in this second field, it forces the address to compare, and overrides the actual compare. If all nine of the compares are true, then the write is permitted. A nine-input AND gate combines each of the compare conditions and thus nine compares must exist to permit a write. The write permit signal is ANDed with a write signal to form the actual write initiate which goes to the memory.

Generally, this register would be used to specify one block and this is performed by successively adding zeros to the lower part of the register. This successively increases the block size. If, however, zeros are inserted in the middle of the field, this creates dual fields. For example, if just the second bit of field size is set to a zero (bit 11), then rather than one block of 512 words, the write specifies two 128-bit fields.

Notes:

1. In the computer the limit register may be easily set under program control and the memory block size and position may be readily changed to suit each specific problem (in the computer for which this was designed, the register is used to inhibit an experimenter's program from modifying his and other person's programs). It has the additional advantage that it is flexible yet it requires very little hardware for implementation. The design concept also has the flexibility that it may be adapted to nearly any size word length and memory.
2. Inquiries concerning this invention may be directed to:

   Technology Utilization Officer
   Goddard Space Flight Center
   Greenbelt, Maryland. 20771
   Reference: B69-10121

Patent status:

Inquiries about obtaining rights for the commercial use of this invention may be made to NASA, Code GP, Washington, D.C. 20546.

Source: David K. Sloper
of Westinghouse Electric Cooperation
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