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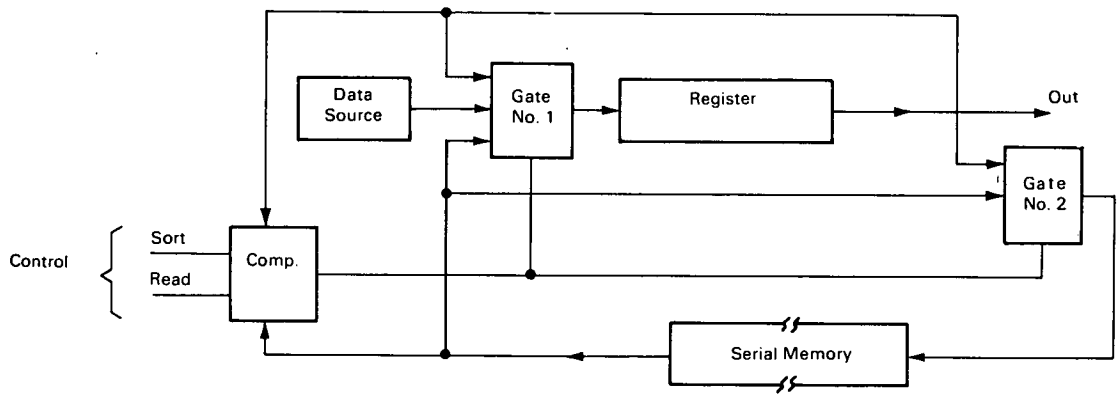
Simplified, Reliable Circuit Sorts Binary Numbers in Order of Magnitude



A relatively simple, highly reliable circuit has been designed to sort binary numbers in order of magnitude. This circuit operates at high speed and can be built at low cost. Although any computer is capable of sorting binary numbers utilizing well-known subroutines, and some special-purpose devices have been developed for this purpose, these are unduly complex and are, therefore, not suitable for applications in which small size and high reliability are essential.

The new circuit includes a single-word input/output register and a multiword serial memory which are circulated in synchronism. The outputs of the register and the memory are applied to a serial comparator which determines whether the register output word is larger than the memory output word. If it is, the memory output word is coupled to the register input, and the register output word is coupled to the memory input. Thus, each new word loaded into the register will be transferred into the proper position in the memory to maintain the words in order of magnitude.

A significant feature of the circuit is its ability to put out data at a rate compatible with relatively slow-speed electromechanical devices, such as line printers. The circuit can be switched from the high-speed sort mode to the low-speed output mode merely by changing the criteria of the comparator so that the memory output words are loaded into the register only when they exceed the register output word in magnitude. In this manner, N memory words can be read out in N full memory cycles, each word being held in the register for one full cycle.

The circuit, represented by the block diagram, functions to insert a binary word from the data source into its proper position (by magnitude) in the serial memory. The latter can be any one of such devices as a magnetic drum, a magnetic tape loop, or a delay line. The output of the data source is connected through gate no. 1 to the input of the single-word input/output register. From this register, the output is connected through gate no. 2 to the input of the

(continued overleaf)

serial memory. The outputs of both the register and the serial memory are connected to the inputs of both gates and also to the inputs of the comparator, whose output controls these gates.

To explain the operation of the circuit, assume that the serial memory contains several words arranged in order of decreasing magnitude, so that the largest word is put out first during each memory cycle. Prior to each memory cycle, a word to be inserted in the proper position in the memory is delivered by the data source through gate no. 1 to the register. During the memory cycle, each word put out by the memory is compared with the word in the register by the comparator. As long as the word from the memory exceeds the word stored in the register, the two gates will be controlled to recycle the contents of the register and the memory, respectively. On the other hand, when the comparator recognizes that the word in the register exceeds in magnitude a word output from the memory, it will switch the gates to couple the output of the memory to the input of the register and the output of the latter to the input of the memory. Accordingly, the world in the register will be inserted into its proper position in the memory, and all of the succeeding words in the memory will be passed through the register prior to returning to the memory, thereby being shifted one word time backward in the memory.

The comparator contains *sort* and *read* terminals. To define a *sort* mode, a logically true signal is applied to the *sort* terminal. The words in the memory can be read out at a relatively slow speed at the output terminal of the register by applying a logically true signal to the *read* terminal of the comparator. In the output mode, the criteria applied to the comparator is reversed, so that the output of the memory is coupled to the input of the register when the memory output word exceeds the register output word in magnitude. Therefore, if the words in the memory are arranged in order of decreasing magnitude, each word will remain stored in the register for a full memory cycle, thus enabling it to be easily coupled to slower-speed peripheral devices (e.g., electromechanical line printers).

Note:

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