NASA TECH BRIEF

Modification to Improve Self-Isolating Transistor Arrays

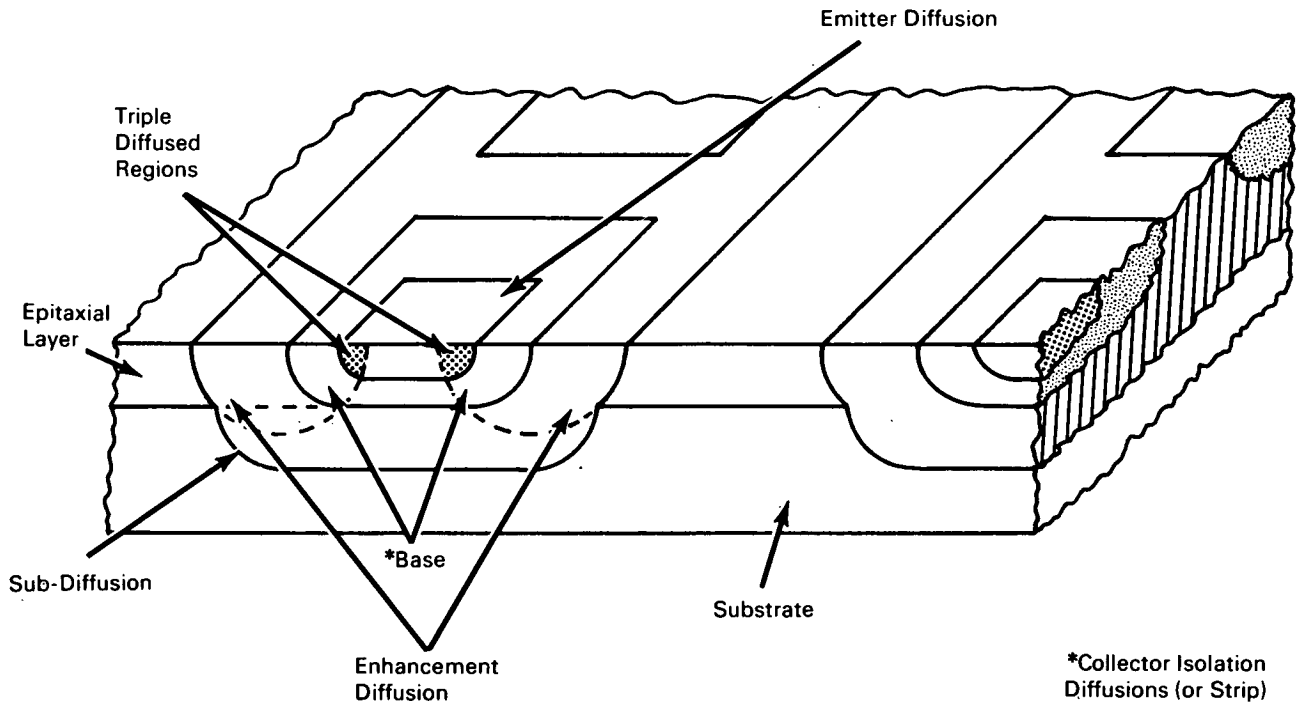

Figure 1. Modified Fabricating Method

A fabricating process to improve the size ratio and shape factor of the base region of self-isolating transistor arrays is being developed.

Figures 1 and 2 illustrate the primary distinctions between the standard and the modified processing methods. The fabricating technique shown in Figure 1 results in a larger base region, C_{bc} is increased, a graded base region becomes available, and the base region shape is more nearly optimum for vertical transistor action. The process also minimizes lateral transistor action, reduces surface recombination effects, and reduces the effects of up-diffusion of collector sub-diffusion.

The basic processing steps in the modified method are:

(1) Substrate preparation
(2) Collector sub-diffusion
(3) Epitaxial layer growth
(4) *Collector isolation-diffusions
(5) *Base enhancement diffusions

(continued overleaf)

(6) Emitter diffusion
(7) Aluminum interconnect deposition
(8) Testing and packaging

*Note: These two steps constitute the self-isolation process.

Notes:

1. This development has application to the transistor manufacturing industry.
2. This development is in the conceptual stage only, and as of date of publication of this Tech Brief, neither a model nor a prototype has been constructed.
3. Requests for further information may be directed to:

   Technology Utilization Officer
   Marshall Space Flight Center
   Huntsville, Alabama 35812
   Reference: B69-10678

Patent status:

Inquiries about obtaining rights for the commercial use of this invention may be made to NASA, Code GP, Washington, D.C. 20545.

Source: D. L. Farnsworth of
Westinghouse Electric Corp., Aerospace Division
under contract to
Marshall Space Flight Center
(MFS-20499)

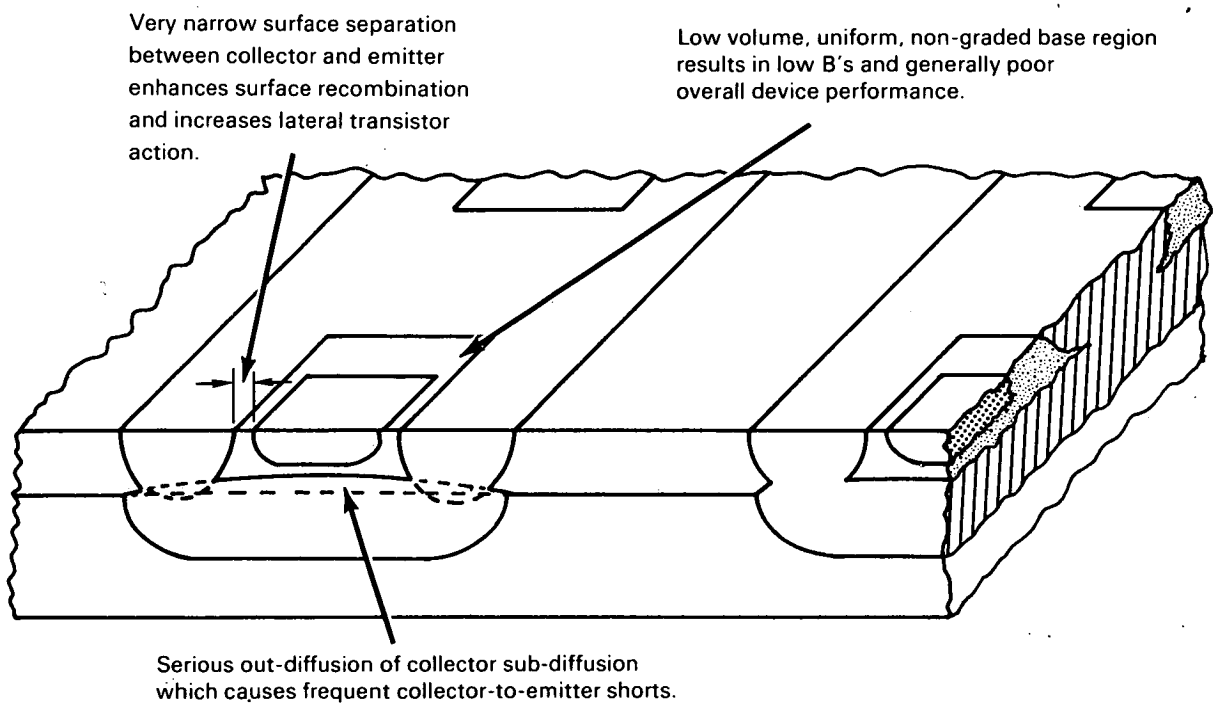

Figure 2. Standard Fabricating Method