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NASA TECH BRIEF

Pulse-Code-Modulation Baseline Correction for Low Signal-to-Noise Ratios

Transmitted binary data appear as a sequence of positive and negative pulses occurring in random order. Binary bit detectors differentiate between the positive and negative pulses by comparing them with a reference voltage. Ideally, this reference would lie at the midpoint between the plus and minus maxima, thus, in effect, establishing a baseline. In practice, however, extraneous voltages get superimposed on the binary data which cause a mislocation of the midpoint voltage. Therefore, if the data are to be read correctly, the bit detection system will have to include a means for reestablishing the baseline voltage to its correct value. Conventionally, a baseline reference is obtained by using a clamping circuit that detects a peak and arbitrarily assigns a bias to it that establishes the "zero" line for the positive and negative pulses. This technique, however, works best when the signal-to-noise ratio (S/N) is high.

In a newly developed system, time-shared integrate-hold-dump circuits are used to separate the dc level due to the signal (bit information) from the dc signal due to the baseline error. The system performs this function when the S/N is very low. The system detects the baseline error, filters it, and then algebraically adds enough voltage to a servo loop to reduce the error signal to zero. It works on the assumption that the beginning and end of each bit period are known. Further, the detection circuitry is sensitive only to adjacent "1" and "0" bits, responding only to the average dc over this interval and rejecting all other dc.

The input to the baseline correction circuitry is obtained from an automatic gain control output amplifier. The signal is applied to the input of three time-shared integrate-hold-and-dump circuits (IHD_1, IHD_2, and IHD_3). Each integrator circuit integrates for two bit times, then holds and dumps for one-half bit time each. The integration intervals overlap so that all pairs of adjacent bits form an integration interval. The integration intervals are controlled by the logic functions R_1, R_2, and R_3. Thus, when R_1 is low, IHD_1 integrates. When R_1 goes high, IHD_1 holds the voltage resulting from the previous integration. At the midpoint of the hold period, a dump pulse turns on the dump switch, discharging the integrating capacitor. When R_1 goes low, a new integration interval begins. The integration periods of the three circuits, IHD_1, IHD_2, and IHD_3 are staggered in time in order to average over all pairs of bits.

Interleave circuits (IL_1, IL_2, and IL_3) select each integrate output during the respective hold periods for routing to the baseline channel output. However, the interleave gate is held off if no data transition has occurred during the previous integration. R_1 and a data transition signal form an *and* gate function which controls IL_1 to route an associated integrator to the baseline channel output only during hold time and only if a data transition has occurred. In like manner, IHD_2 and IHD_3 contribute to the output through IL_2 and IL_3. The integrator waveforms show a net dc present as a result of integrating over periods of no data transition.

Note:

Requests for further information may be directed to:

Technology Utilization Officer
Manned Spacecraft Center, Code BM7
Houston, Texas 77058
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(continued overleaf)

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No patent action is contemplated by NASA.

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