STUDY OF SEMICONDUCTOR HETEROJUNCTIONS

OF ZnSe, GaAs and Ge

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Semiconductor heterojunction transistors of GaAs/Ge and ZnSe/Ge are being studied to determine the parameters controlling gain and frequency response. These parameters include the emitter and base doping levels, the device geometry and the device processing. The growth processes under study include HCl close-spaced transport of GaAs and ZnSe, iodine transport of Ge, and solution-growth of Ge from Zn.

The optical properties of ZnSe/Ge or GaAs/Ge photo-diodes and photo-transistors are to be examined and are expected to offer attractive features such as window effect. If the progress of the work allows, studies will also be made of nZnSe/pGaAs heterojunctions.
1. INTRODUCTION

1.1 Objectives

The research in process comprises a detailed study of several classes of semiconductor heterojunction structures. The studies are aimed at obtaining a better basic understanding of the conditions for minority carrier injection, the transport mechanism for carriers across the interface and the photo-voltage properties of n-p heterojunctions.

Experimental and analytical study is to be made of the factors controlling gain, frequency and temperature dependence in heterojunction transistors of GaAs/Ge and ZnSe/Ge, including the following:

a) Experimental study of the factors presently limiting performance in GaAs/Ge and ZnSe/Ge transistor structures by exploring effects of parameters such as doping levels, base thicknesses, capacitances. Some investigations of masking and contact problems.

b) Design studies for a small-signal medium-frequency (of the order of $100 \text{ MHz } f_T$) heterojunction transistor in which the base is doped at a level greater than or comparable to that of the emitter. Study of the extent to which the heavy base doping level should minimize the effects of emitter crowding and second breakdown in such a transistor.

c) Experimental study of the feasibility of growing device quality Ge base and collector regions on emitter substrate seeds of GaAs or ZnSe. Low temperature growth systems are under study including the solution growth of Ge from Zn and the iodine disproportionation reaction process.

It is hoped also, if progress permits, to make preliminary studies of the electrical and optical properties of ZnSe-GeAs heterojunction structures.

Semiconductor heterojunction structures offer many unusual and interesting device possibilities, including:

1. Wide-gap emitter transistors with a new degree of freedom in base doping levels. These should have reduced lateral bias effects, good high frequency performance and unusually high quantum-gain as photo-transistors.

2. Window-effect photo-junctions of low internal resistance, offering the possibility of high performance and good radiation resistance (see Section 9 of this report).

3. High-frequency rectification by N-N semiconductor heterojunctions, since minority carrier storage does not occur.
(4) N–N heterojunctions contain energy barriers in the range up to about 0.7 ev, and may be expected to be infra-red detectors with less free carrier absorption than metal-semiconductor junctions.

(5) Semiconductor heterojunctions in virtue of the band-gap differences offer the possibility of infra-red to visible light "up-conversion" for display purposes. In addition they represent the possibility of achieving injection and recombination radiation from semiconductors in which pn homojunctions can not be formed by doping.

(6) Space-charge-limited-flow emitter structures are possible with heterojunctions and these may be high frequency transistors.

The present study is mainly concerned with the investigation of items (1) and (2), although the results will have bearing on most of the other aspects.

1.2 General Comments

Although research on semiconductor heterojunctions has been in progress for a number of years the effort supported has been rather limited and progress has been slow. The need for great care in the choice of heterojunction pairs, and in fabrication and doping details, has been realized; and in the last year or so, the "wide-gap emitter" action postulated in 1951 by Dr. W. Shockley, has been shown to be a practical effect in semiconductor heterojunctions. Transistors of GaAs, Ge, Ge, and ZnSe, Ge, Ge (emitter, base and collector regions) with current gains (beta) of between 20 and 60 have been fabricated by the Carnegie-Mellon group. In these transistors the base doping (about $10^{19}$ cm$^{-3}$) is far larger than the emitter doping level ($10^{12} - 10^{16}$ cm$^{-3}$). These doping ratios would be quite impractical in a homojunction transistor, where the emitter doping must greatly exceed that of the base to prevent loss of gain by reverse injection from the base to the emitter. In a heterojunction this reverse injection is prevented by an extra barrier representing the energy gap difference of the semiconductors used for the emitter and base. This situation is shown in Fig. 1 (a) and (b) which illustrate the emitter-base conduction and valence band barriers for a homojunction and heterojunction respectively.

Three factors are necessary to produce semiconductor heterojunctions that exhibit good injection and collection instead of a variety of undesirable
FIG. 1 Transistor Energy Band Diagrams for Homojunction 1 (a) and Heterojunction Emitters 1 (b).
tunnelling and recombination mechanisms as previously seen. These three factors are:

1) The lattice match must be very close to reduce interface states. The most promising pairs are GaAs (5.654 Å) on Ge (5.658 Å) and ZnSe (5.667 Å) on Ge, since these are now known to form injecting junctions. ZnSe on GaAs, of course, is an equally promising pair, but has not yet been evaluated.

2) The conduction or valence band in which the injection is required should not contain a large energy spike caused by electron affinity differences, or interface state charge. Such spikes impede injection and allow interface recombination or tunnelling phenomena to dominate the current flow mechanisms. The valence band edge for a pGaAs-nGe junction is shown in Fig. 2 (a) and contains an energy discontinuity that is about 0.6 eV and impedes the injection of holes from GaAs into the Ge. On the other hand, the conduction band edge for a nGaAs-pGe junction, Fig. 2 (b), contains only a very minor energy spike which does not seem to impede the injection of electrons from the GaAs into the Ge.

3) Growth methods need to be very carefully chosen and carried out with attention to detail so that clean conditions are maintained. Seed preparation is important and so is leak-tightness and freedom from oxygen, vacuum grease and other sources of contamination. The growth temperature, times and chemical species in the growth system should be such that they minimize the possibilities of strain and cross-doping or abnormal grading between the semiconductors forming the two sides of the heterojunction. For example, the nGaAs-pGe growth system must not allow undesired Ga or As to be incorporated in the Ge layer or excessive amounts of Ge to be incorporated in the GaAs.

Failure to recognize these three factors (lattice match, interface band structure and suitable growth systems) have been the major reasons in the past for the slow progress towards the fabrication of useful and unique heterojunction semiconductor devices.

The objectives of the present research are to evaluate the factors controlling the gain, frequency and temperature dependence in heterojunction transistors of GaAs/Ge and ZnSe/Ge. Secondly to investigate the electrical and optical properties of heterojunctions of nZnSe-pGaAs and compare them with nZnSe-pGe junctions. Such junctions should have interesting device properties because ZnSe and GaAs are of good lattice match, high in energy
FIG. 2  Spike Barrier Impedes Injection in pGaAs-nGe Heterojunction but not in nGaAs-pGe junction
gap (2.6-1.4 eV) and direct recombination in energy band structure.

The key question to be answered from these studies is to what extent the performance (electrical or optical) is determined by interface recombination rather than by normal junction behavior and bulk properties of the base or emitter. The answer to this question will to some extent depend on process details but it is expected that the studies will indicate where improvements are needed in processing.

Design studies are in process for a small-signal medium-frequency (> 100 MHz f_T) heterojunction transistor in which the base is doped at a level greater than, or comparable to that of, the emitter. We hope to establish the degree to which the completely different emitter and base doping proportions of a heterojunction transistor may be expected to change frequency response characteristics, emitter crowding, second breakdown and related factors. For example the doping levels modify parameters such as resistances, capacitances, emitter base and collector transit times, and voltage and current ratings. Design studies will indicate how to proportion the transistor, within the limits imposed by the process technology, for good performance. Some investigation of masking and contact technology is involved, since the presence of heterogeneous materials affects the permitted processing.

Experimental studies are intended of the feasibility of epitaxial growth of the Ge base and collector regions on emitter substrate seeds of GaAs or ZnSe. This would be an inversion of the present practice of growing the emitter on a base-collector germanium substrate.

In favor of growing the emitter is the fact that imperfect structure, if present, is mainly in the emitter where it has presumably little effect on the device injection efficiency. On the other hand, during the emitter growth of GaAs free As is present and can diffuse into the p type Ge base layer. This is a major problem since As is an n type dopant and the p Ge base region has to be heavily doped (with consequent degradation of lifetime and mobility) to prevent the creation of an undesired n layer. If the Ge layers are grown by GeI₂ decomposition at about 400°C, it is possible that As from the GaAs seed will not be so readily incorporated into the Ge base layer region. On the other hand the mobility and lifetime in the grown pGe base layers may not be particularly good because of defects in the epitaxial layers.

In the growth of ZnSe emitters by the HCl process, the presence of free Zn is not an important problem since it is a p type dopant and has therefore little effect on the p type Ge base region. However the n type ZnSe layers
are not as heavily doped as we would like. Apparently n type dopants (Al, Ga, In) in ZnSe do not transport too well in the presence of HCl. For example, at present ZnSe layers of $10^2$-$10^3$ ohm-cm are about the best that can be obtained from source ZnSe in the 0.1-10 ohm cm range.

The germane decomposition process (700°C) does not seem very promising for the growth of germanium on ZnSe seeds, since the loss of Zn tends to become rapid at temperatures above 500°C. Examination of the junctions formed by the growth of Ge from the iodine-germanium disproportionation reaction however appears worthwhile, since the temperature involved is 400°C at the seed. The ZnSe seed may also be protected against Zn loss by coating of exposed surfaces with SiO$_2$ obtained from TEOS decomposition. We are also exploring the possibility of growing Ge on ZnSe by solution growth from Zn. The temperatures required are moderate, 400-500°C, and the presence of the Zn should suppress zinc vacancies.

2. ZnSe Epitaxy for Heterojunctions

ZnSe may be grown on p-type Ge substrates by an HCl close-spaced epitaxial process. This type of growth system was available and operating at the outset of this grant. It is described in detail in a previous report. In the close-spaced system ZnSe is separated from Ge by a 10-15 mil quartz spacer. The ZnSe, Ge, and spacer are in turn held rigidly between two oxidized Si blocks which are situated in a quartz growth tube where HCl and hydrogen gas can be admitted. The blocks are heated independently by two intense light sources (sun-guns) which produce upper (ZnSe) block temperatures from 650 to 800°C and lower (Ge) block temperatures of 500 to 680°C. During growth the higher ZnSe temperature causes ZnSe etching by the flowing HCl + H$_2$ gas. The etched material diffuses to the lower temperature Ge seed where it deposits epitaxially. Table I gives typical results on uniformly doped (0.1-30 ohm-cm) p-type Ge substrates.

<table>
<thead>
<tr>
<th>Table I</th>
<th>Growth of ZnSe On Ge By the Close-Spaced HCl Process*</th>
</tr>
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<tbody>
<tr>
<td>ZnSe Temp.</td>
<td>Ge Temp.</td>
</tr>
<tr>
<td>675°C</td>
<td>580°C</td>
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<td>675°C</td>
<td>580°C</td>
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<td>675°C</td>
<td>580°C</td>
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* The seed to source spacing was 12 mils and the total HCl plus H$_2$ flow rate was 200 cc/min. Low HCl concentrations are necessary to prevent Ge etching.
Grown layers are single crystal on (111) oriented Ge. Single crystal-
linity on (100) substrates has not been determined as yet. As-grown surfaces
on (111) substrates show a regular triangular pyramid pattern of
density $2 \times 10^5 - 4 \times 10^5 \text{ cm}^{-2}$. This does not correspond to the much lower
($5 \times 10^3 \text{ cm}^{-2}$) dislocation etch pit density of the Ge substrates measured
before and after growth. It is believed that ZnSe stacking faults originate
at the ZnSe-Ge interface due to the inclusion of strain from thermal ex-
pansion mismatch between ZnSe and Ge. Severe cracking of ZnSe occurs if it
is cooled from growth temperatures at more than 2°C/min. Layers thicker than
$1 \mu m$ also present a cracking problem. Slower cooling produces no cracks.
Growths on (100) p-type Ge do not produce stacking fault patterns but give an
almost matt surface. However this is no reason to believe that faults are
not present.

Grown ZnSe layer resistivities are typically $10^6 - 10^8 \text{ ohm-cm}$ when no
attempts are made to suppress Zn vacancy formation. At temperatures above
400°C Zn vacancies are created quite rapidly. Such vacancies are acceptors
and can almost completely compensate any existing or intentionally added
donor impurities. This study requires low resistivity n-type ZnSe, and con-
sequently the high resistivity grown material is quite useless. Several
ideas are under examination that are aimed at making the grown ZnSe low
resistivity n-type either during or after growth.

The first method (previously employed$^1$) uses Ga doped ($10^{17} \text{ cm}^{-3}$) ZnSe
as source material coupling it with a zinc vapor diffusion step while still
in the growth apparatus. This produces a lowest resistivity of $10^3 - 10^4
\text{ ohm-cm}$. Experiments indicated that the low dopant transfer ratio may be due
to poor dopant transfer factors, since Al doped ($10^{18} \text{ cm}^{-3}$) ZnSe yielded
$10^5 - 10^6 \text{ ohm-cm}$ material.

The second method involves evaporating Zn layers on grown ZnSe to re-
move Zn vacancies. In this method a thin (1000 Å) layer of Zn is evaporated
on the grown layer surface. A 1 μ layer of Al is deposited over the zinc. The Al-Zn coated ZnSe-Ge device is then heated slowly (2°C/min.)
to a temperature and for a time necessary for the zinc to diffuse completely
through the ZnSe. Then it is cooled at the same rate. Typical temperatures
and times are 450° - 500°C for 10 minutes to 2 hours. Results from growths
with undoped sources indicate that the resistivity can be reduced as low as
$5 \times 10^3 - 5 \times 10^4 \text{ ohm-cm}$. This is about an order of magnitude better than
the zinc vapor diffusion method can produce under similar conditions. Runs
with doped sources are now under way, and it is hoped that the evaporated Zn layer method can produce better doping than previously obtained.

3. GaAs EPITAXY FOR HETEROJUNCTIONS

During the first portion of this grant work on the growth of GaAs layers on Ge has been directed toward improving the properties of the GaAs layer and the GaAs-Ge heterojunction.

The first GaAs-Ge heterojunction transistors produced in this laboratory suffered from a low DC current gain and a high emitter resistance. Both of these problems have been attacked simultaneously. In an effort to lower the emitter resistance the effects of substrate orientation, substrate temperature, HCl concentration, and the method of initiating growth have been studied.

GaAs layers have been grown on substrates oriented in the (111), (100), and (311) directions as well as at 8° off (111) toward (100). It has been definitely established that substrates oriented accurately to the (111) direction produce layers with rough, grainy texture under growth conditions which produce mirror smooth layers with very few stacking faults on (311) and 8° off (111) substrates. These comparisons were made at a substrate temperature of 600°C. A study of GaAs layers grown at temperatures ranging from 450° to 650°C onto heavily doped p type substrates demonstrates that the best growth morphology is obtained at temperatures higher than 550°C.

The effect of introducing the HCl with a linear rise in concentration at the beginning of the growth was compared with an abrupt increase in concentration obtained by either doubling the total flow rate into the growth tube or by using ten times the final HCl concentration during the initial stages of growth. It was found that doubling the flow rate in order to raise the HCl concentration in the tube allowed growth without surface conversion due to arsenic for p-Ge substrates doped as low as $8 \times 10^{18}$ cm$^{-3}$. This procedure produced the best p-n heterodiodes so far obtained from this system.

Variation of the growth temperature when growing on p-Ge substrates showed that surface conversion was more pronounced at lower temperatures than at high temperatures. This result is being studied further to see what bearing it may have on transistor fabrication.

It has been shown that the resistivity of GaAs layers obtained from Hall measurements is inconsistent with the resistance measured between a contact on the layer and an n-type Ge surface. The n-type Ge may either be converted Ge surface or a p-type substrate or n-type bulk substrate material.
This observation prompted studies of the tin contacts reported in the next section. Improving the contacts did not change this result. In fact, it was shown that the lateral resistance of the layer is frequently less than the resistance through the layer to the Ge. In an attempt to determine the cause of this problem, profiles of the carrier concentration versus layer thickness are being made on past runs. So far, we have determined that in two cases the carrier concentration increases toward the heterojunction from the GaAs surface as might be expected from Ge autodoping.

By way of contrast, occasional runs have produced low mesa resistances of a few ohms. The reason for this is not clear but seems to be orientation dependent and is probably also connected with Ge autodoping. It is hoped that the present study will lead to a clarification of the above results and result in an optimization of layer resistivity and heterojunction properties.

4. CONTACTS TO ZnSe AND TO GaAs

Most work on ohmic contacts to bulk n-type ZnSe is contained in a previous report. The best contact found is pure In alloyed at 300°C for 10-20 sec. in an ambient gas consisting of Ar-15% H₂ plus 1-2% high purity HCl gas. Penetration depths are less than 1/2 micron. Results from potential probe experiments indicate that although the contacts are ohmic at 300°K and 77°K, there exists a sizable contact resistance which increases with decreasing temperature and decreases with decreasing resistivity. As an example a typical contact on 4 ohm-cm ZnSe shows less than 1 ohm contact resistance at 300°K but 20 ohms contact resistance at 77°K. The mechanism responsible for this contact resistance is not understood. Nickel plating ZnSe allows superior In wetting of the ZnSe but does not reduce the contact resistance. Similar contact studies have not been extensively pursued in grown material due to the fact that traps and injected space charge in such high resistivity material "mask out" the contacts. More work will be continued as soon as lower resistivity material can be obtained.

Work has begun on evaporated In-Zn contacts to bulk and grown ZnSe since this technology will be needed to create heterojunction transistors with well-defined emitter contact geometries, and photo-diodes with digitated contacts for low lateral resistance. A typical procedure is to sequentially evaporate a 1000 Å layer of Zn, a 5000 Å layer of In and a 1/4 layer of protective Al on a grown ZnSe layer and bulk high resistivity (no intentional doping) ZnSe. The idea here is to use the zinc to suppress Zn vacancies and
the In to form the contact. The material is doped and contacted simultaneously. The bulk ZnSe is used as a check on the effectiveness of the method since it usually contains more n-type impurities than the grown material and can therefore be driven lower resistivity to produce better contacts. Samples are heated to 450-500°C for 10 minutes to 2 hours depending on the thickness of ZnSe to be doped. Results obtained so far are promising. Bulk ZnSe shows 1-10 ohm-cm skins whose thickness corresponds to that obtained experimentally from the diffusion of Zn in ZnSe. Contacts are almost ohmic but show about 2-3 times the resistance of In dots alloyed to the same material. Contact resistance measurements over a temperature range have not been made. The same is true on grown material except the apparent resistivity is in the 5 x 10^3 - 5 x 10^4 ohm-cm range (for undoped sources). More work on ZnSe grown from doped sources should produce better results.

Considering now the question of contacts to GaAs, the practice in our laboratory has been to use alloyed tin contacts with HCl as the flux in an atmosphere of Ar-15% H₂. A re-examination of these contacts during this report period showed that when properly alloyed at a temperature of about 320°C onto 0.03 ohm-cm and 0.2 ohm-cm n-type GaAs the resistance is approximately the theoretical spreading resistance of the contact. It has been shown that remelting of contacts during subsequent fabrication steps and contacts to grainy surfaces frequently result in an inordinately high contact resistance. Some of the high resistance observed for many of the past devices can undoubtedly be attributed to remelting the contact in order to attach a lead wire.

Recently, contact resistance measurements were performed on a mirror smooth GaAs layer grown on (311) n-type Ge. The typical contact resistance leads to a value of 1.3 ohms which is consistent with the resistivity inferred from other resistance measurements.

5. FABRICATION TECHNOLOGY FOR HETEROJUNCTION TRANSISTORS

GaAs-Ge and ZnSe-Ge heterojunction transistors have been fabricated and studied by Jadus and Hovel. The emitter area (mesa) in these studies was defined by masking the contact area with apiezon wax and etching. The active areas obtained in this way are usually of irregular shape and an accurate control of the geometry is not easy since it may not be possible to obtain two devices having exactly the same geometry for parameter variation studies. Also with the wax technology there is no possibility of interdigitation of emitter and base contacts to minimize the base resistance. It therefore has
been decided to use photomasking techniques to obtain devices with accurately
controlled geometry that can be reproduced on a single wafer in steps. It is
expected that devices of improved and reproducible electrical characteristics
should be obtainable in this way.

The devices formed by photomasking and etching may be either of mesa
type or of planar type. In mesa type the successive masking and etching gives
a device as shown in Fig. (3). The geometry and the arrangement of a planar
type device is shown in Fig. (4). Each type has its own advantages and dis-
advantages. In the present studies the ZnSe grown wafers are 9 x 7 mm and
it is proposed to make 9 transistors on a single wafer in three rows each row
containing 3 devices.

The mesa type structure has the advantage that the number of steps in its
fabrication is minimum but the junctions are open to atmosphere and hence the
properties of the device will be influenced by the ambient. This possibility
is reduced in the planar structure by the deposited SiO₂ layer. However the
properties of this type will be influenced by the quality of SiO₂ and also by
the surface below SiO₂. Poor quality insulation sometimes gives excessive
high leakage current in planar type transistors. Whereas in some cases the
characteristics of mesa type devices can be improved by etching this is not
possible in planar type.

Fabrication of planar type device involves a considerably larger number
of steps than that of the mesa type. The number of steps can be reduced if
SiO₂ is deposited on pGe before ZnSe growth and emitter windows are etched in
the SiO₂. ZnSe or GaAs may now be grown selectively in the areas where
windows have been etched. However it is not clear if the growth condition
on the small window area will be the same as on the large area. It is
possible that the nucleation will first start at the edges of the grown
layers and may not be uniform and may not be of the same quality. This point
has to be investigated by a number of experiments. The merits of the three
methods can be decided only by experiment and hence all the three types of
structures should be fabricated and their relative performances compared.
Drawings corresponding to these structures have been prepared and masks have
been made by photographic reduction of these drawings. Studies for the
fabrication of mesa type structures have been started. It is hoped shortly
also to do some runs on the selective growth of ZnSe through small SiO₂
windows on Ge substrates.
ALL DIMENSIONS ARE IN MILS.

FIG. 3 Structure of Mesa type Heterojunction Transistor

- BASE PAD

- Evaporated Al emitter contact
- Zn, In evaporated layer
- Al base contact
- p-Ge (diffused)
- n-Ge (substrate)
- Collector contact

ZnSe GROWN LAYER
FIG. 4 Structure of a Planar Heterojunction Transistor.
The actual dimensions of the transistor are shown in Fig. (3). Magnified drawings (X80) of the masks were made on Stabilene Film and the areas to be masked were cut. These patterns were reduced to the required size by using two separate reduction steps of 4:1 and 20:1. The second camera (Burke & James, Inc. Chicago) had a resolution of 5 microns.

The next step toward transistor fabrication from these masks is etching of the emitter mesa. As a preliminary stage, the etching characteristics and pattern definition has been studied on wafers of polycrystalline ZnSe material. These bulk wafers were lapped with 3 µm Al₂O₃ and then etched for 10 minutes in methanol-bromine (100:0.5) solution. Agitation was provided by rotating the container. The etched surface revealed many twin planes. After usual cleaning in trichloroethylene, acetone and methanol, the photoresist KTFR was applied and the adhesion of the resist was found to be good. The sample was exposed through the mask and after developing was heat treated to harden the photoresist. The patterns were etched in 1% solution of bromine in methanol at room temperature. No agitation was provided during the etching. It was found that for etching times up to 10-15 minutes the masks were quite effective but this etching revealed many other twin planes. Hopefully the problem of difference in etching rates on different planes will not arise when we proceed to the etching of thin grown layers of ZnSe which are single crystal.

The use of methanol-bromine as the etching agent is desirable because it etches both ZnSe and GaAs, but does not attack the Ge base-collector region. Fig. 5 and 6 shows the etching rates observed for methanol-bromine on ZnSe or GaAs. Some studies were also made of the angle of etching since this can determine the pattern resolution. The results are shown in Fig. 7, from which it is seen that an etching depth of 5 microns is associated with an edge spread of 0.5 to 3 microns under the simple conditions tested. This is acceptable for the transistor patterns that we are presently interested in. It is somewhat unexpected that there is no sign of undercutting in these particular etching studies.

6. HETEROJUNCTION TRANSISTOR DESIGN STUDIES

A preliminary design study of the high frequency characteristics of heterojunction transistors was begun on this grant. This work has been further advanced as part of a U.S. Air Force contract 19628-68-C-0179. The results of these two studies are summarized in this section.
FIG. 5 The Etching Rate of ZnSe

Etchant: 200 cc Methanol + 2 cc bromine.
Room temperature, no agitation.
FIG. 6 The Etching Rate of GaAs

Etchant: 200 cc Methanol + 4 cc bromine
Room temperature, no agitation.
FIG. 7: Studies of Etching Angle for Methanol-Bromine Etch on ZnSe and GaAs.

The ZnSe specimens were polycrystalline and the GaAs specimens were etched on the (111) As face.
The frequency limitations of three transistor types were explored assuming identical geometries. The three types were a Ge homojunction device, and a space-charge-limited, semi-insulating GaAs on Ge device. The geometry chosen was an alloyed-emitter, diffused-base, epitaxial-collector type structure. Calculations were performed in which allowances were made for the transverse base resistance and the resistance of the metal contacts to the base. However calculations were also made in which these were assumed minimized to determine the inherent improvement possible.

The conclusions from the studies are as follows. The GaAs-Ge heterojunction transistors may be expected to be about equivalent in frequency performance whether the emitter is space-charge-limited or not (this assumes that the field in the GaAs n-emitter remains slightly below the critical value for the valley transfer effect of Gunn oscillation). If parasitic base contact resistances (typical of present contact technology) are included the heterojunction transistors may be expected to have a maximum frequency of oscillation 1.25 times that of the Ge homojunction transistor. However, if the parasitic base resistances could be largely eliminated, the $f_{\text{max}}$ of the heterojunction transistors would be over twice that of the comparable Ge homojunction transistor. (The calculations were made for a structure that should perform in the high GHz range). Most of the frequency-performance advantages of heterojunction transistors results from the low base resistance made possible by the permitted heavy doping of the base. Obviously this advantage is not realizable unless advanced contacting techniques are available to minimize parasitic base resistances.

7. **PREPARATION FOR TRANSISTOR FREQUENCY MEASUREMENTS**

When heterojunction transistors with well-defined geometries are available, it is proposed to study their amplitude and phase-response as a function of frequency. This should show whether traps or recombination states in the emitter, or the base, or at the interface, are playing a determining role in the frequency response. For this purpose, the Grant provided for the purchase of a Vector Voltmeter hp 8405A and this instrument was received about a month ago. The transistor fixtures are still on order.

We are now in process of setting-up the instrument in a measuring circuit. The circuit proposed is shown in Fig. 8. This circuit and its individual components are presently undergoing test and evaluation.
FIG. 8 Block Diagram for Measurement of Transistor Frequency Parameters.
8. LOW TEMPERATURE GROWTH OF Ge ON ZnSe OR GaAs

Bulk ZnSe can readily be doped n type to less than 1 ohm-cm resistivity, but layers of ZnSe grown by the HCl close-spaced transport process tend to be $10^3 - 10^4$ ohm-cm. This has prompted an investigation into the possibilities of growing suitably doped p-Ge on doped ZnSe substrates.

Although ZnSe has a very high melting point and n-type impurities in ZnSe (Ga and Al) also have fairly low diffusion coefficients, the problem of fast out-diffusion rates of Zn from ZnSe severely limits the processing temperatures to less than 400°C. Zn vacancies act like acceptors and thus compensate the n-material to high resistivity. A low temperature epitaxial growth system for Ge by disproportion of iodides was available and therefore tried.

Several runs were made in the iodine system, but all of them gave n-type Ge deposits even though Ga (a p-type dopant) was present in the system. Identical conditions with Ge seeds gave a very heavily doped p-type growth. It was concluded that the control of growth rates and doping levels was unsatisfactory in the system in its existing form, and it was decided to rebuild in a form that included the improvements reported by IBM workers recently.

8.1 Improved Iodide Disproportionation System

The previous germanium iodide disproportionation growth system has been modified to 1) permit controlled p and n type doping, 2) isolate the iodine source from the atmosphere between runs, and 3) reduce turn around time between runs. Fig. 9 shows the revised system as it is now constructed.

The growth process begins by metering a controlled mixture of hydrogen and helium and passing this mixture upwards through a column containing ultra high purity iodine crystals and glass beads. The beads act as inert material to prevent packing of the iodine crystals and to insure that the partial pressure of iodine in the existing gas mixture is at the equilibrium value for a given iodine temperature. The gas mixture containing iodine vapor next passes through a chamber containing fine platinum wool at 350 - 450°C. This heated platinum catalyzes the reaction between the hydrogen and iodine to form hydrogen iodide which is more stable in the vapor phase near room temperature than is iodine. As the figure indicates, both the iodine column and the platinum wool converter can be closed off from the atmosphere by teflon valves when the main growth tube is opened to the atmosphere for seed insertion and cleaning.
FIG. 9 Schematic Diagram of Germanium Iodide Growth System.

ARSENIC IN HELIUM

HYDROGEN + HELIUM SUPPLY

GROWTH TUBE

REMOVABLE LINER TUBE

REACTION PRODUCTS

TEFLON CONNECTOR

EXHAUST AND VACUUM

PLATINUM WOOL + GLASS BEADS

INCLUSION GERMANIUM

BAFFLES

SEED
The resultant HI-He mixture is next passed through a bed of intrinsic Ge which is maintained at 550-650°C. Here the HI reacts with the Ge to form GeI₂, and free H₂. The bed consists of several small chambers separated by baffles which force the gases to pass in contact with the Ge lumps, rather than by their surface, to promote reaction to equilibrium. After passing through a restriction, the transported GeI₂ enters the deposition region in which the seed is maintained at 350 - 450°C. Here the disproportionation takes place resulting in free Ge, which deposits out as a solid growth, and germanium iodides of higher iodine content. These remaining iodides deposit onto the final length of liner tube which is now the only system part which must be removed for cleaning between runs.

Doping will be accomplished by addition to the growth stream, just prior to the deposition region, of either arsine in helium for n-type or boron tri-iodide in a helium-hydrogen mixture for p-type layers. The flow of these gaseous dopants is metered through needle valves and may be changed during the course of a run to form a junction within the grown layer. At the output end of the growth tube provisions exist for exhausting the transport gases and for evacuating the entire system prior to growth runs. This system has just now been completed and leak tested. Initial runs to determine the quality of growths and conditions for controlled doping are being made.

8.2 Solution Growth of Ge from Zinc Alloys

Another low temperature epitaxial growth system under investigation is a solution growth system using Zn as a solvent for Ge. Here Zn serves three purposes. First, it acts as a vehicle (solvent) for transport of Ge. Second, it provides the p-type dopant impurity for the Ge grown layers and third, last but not the least, it prevents out-diffusion of Zn from ZnSe. Therefore, this process is not necessarily restricted to operation at low temperatures. However, in our experiments, low temperatures (<500°C) were used for the following reasons.

Application of the devices to be fabricated demands a low doping level and long diffusion length for minority carriers in the grown p-Ge layer. In the growth system, since the dopant (Zn) is present in large quantities, its incorporation in Ge is limited by its solid solubility limit only. Unfortunately, most of the dopants have rather high solid solubility limits (5 x 10¹⁷ to 5 x 10²⁰ range). Therefore, partial compensation by the inclusion in the Zn of an opposite type impurity is contemplated in the solution growth system to obtain a suitably low doping level. However, because of the second requirement
on minority carrier diffusion length, it is desirable to use as low a growth
temperature as possible in order to reduce the amount of compensation needed.

Experiments with the Zn solvent system soon indicated that the fluid
properties of Zn at temperatures below 500°C are not suitable for easy pour-
off of the solution after the growth is over. A mixture of 50% Zn and 50% In
was used in later experiments. Non-uniform features were found on the grown
layers. These and other observations, suggest the presence of a very thin
scum (oxides probably) over the solution, which breaks-up and covers small
patches of the interface between the ZnSe and the solution, when the solution
is rolled over to cover the seed. Therefore, extra care is now being taken
to repurify the starting materials. The graphite boat was also found to de-
gas during the runs in dry hydrogen and probably was a further source of
oxygen in the system. A sapphire boat is now ordered and is expected to be
available soon. Meanwhile, purification of Zn and In and the 50/50 Zn/In
alloy is being carried out. Bulk ZnSe material, which is to be used for seeds
in later runs is also being doped. Each doping run takes about a week.

9. OPTICAL MEASUREMENTS

The optical properties of heterojunctions are potentially interesting
for several reasons. One is the window effect in a pn heterojunction, in
which the wide-gap semiconductor acts as a window for light in the photon
energy range between that of the energy gaps of the two semiconductors forming
the junction. For example, in a ZnSe/Ge junction photons of energy between
2.6 and 0.7 eV are transmitted without absorption through the ZnSe to the
junction with the Ge where they create hole-electron pairs and photo-cell
action. In a GaAs-ZnSe junction photons of energy between 2.6 - 1.4 eV
will create hole-electron pairs.

In a homojunction photo-cell, where window action does not occur, the
light tends to be absorbed very close to the surface of the cell that is il-
luminated and the junction must be correspondingly close to the surface if
carriers are not to be lost by recombination while diffusing to the junction
or by surface recombination. The junction close to the surface tends to
create lateral bias effects and results in internal impedance in the cell.
In a heterojunction photocell, however, the junction is much deeper (Fig. 10
(a) (b)) and the lateral effects may be correspondingly less. Comparison
of this window effect in photocell designs of nZnSe-pGaAs, and nZnSe-pGe is
of interest because the output voltage of the GaAs cell should be greater
FIG. 10 Homojunction and Heterojunction Solar Cells.
The thick epitaxial ZnSe layer in the heterojunction cell produces window effect and low lateral resistance.
than that of the Ge cell and less sensitive to high temperatures. If the electrical properties are sufficiently interesting, neutron flux irradiation studies (in which our laboratory has some experience) may be attempted to assess radiation resistance effects.

The junctions of nZnSe-pGaAs may also be well worth examination for photon radiation emission (through the ZnSe window) resulting from direct gap recombination of injected carriers.

The photo-properties of heterojunction transistors should also be unusually interesting. For instance in an npn heterojunction transistor (biased between emitter and collector with the base floating) the quantum gain should be high, since the passage of holes from the base to the emitter will involve considerable forward bias of the emitter-base junction and therefore result in a heavy injection of electrons from the emitter into the base which will appear as collector current. In essence, therefore the Kroemer exponential factor \( \Delta E_g/(kT) \) should appear in the quantum gain. The window effect should further contribute to the effectiveness of the photo heterojunction transistor. We propose looking for these effects since relatively little is known at present about the optical properties of heterojunctions that have exhibited good electrical transistor characteristics.

The major hold-up in the determination of these optical properties is related to our need to have low resistivity in the high energy gap material and good contact technology. Both of these problems are being actively worked on as discussed earlier in this report.

For obtaining optimum performance from ZnSe-Ge or ZnSe-GaAs photo-diodes, a knowledge of the optical properties of doped ZnSe in the photon energy interval (2.7 eV to 0.6 eV) is also desirable. To date, this information is not available in the literature. Therefore, these measurements are being undertaken.

Transmission through a polished ZnSe sample is being measured for two different thicknesses. The results are analyzed to separate the reflection and absorption coefficients. In the photon energy interval for these measurements the absorption coefficient is small while reflection coefficient is relatively high and the samples available are quite thin, therefore extra care is needed for better accuracy of measurements. With the available system, only one optical detector can be used at a time with no arrangement for beam-splitting. This requires a long-term as well as short-term stability of the
light source. A constant voltage transformer is now used to power the lamp source.

At present some difficulties are also encountered in obtaining chemically polished (damage free) ZnSe with optical grade surfaces. This trouble is mainly because of the presence of twin-planes in the ZnSe crystals. However, preliminary investigations show that mechanical damage in a properly polished ZnSe sample does not alter the optical properties in the photon energy range 2.7 eV to 0.6 eV. Measurements are in progress and doped ZnSe samples are being polished.
10. REFERENCES


11. CONTRIBUTORS
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