FINAL REPORT

National Aeronautics and Space Administration
Electronics Research Center
Cambridge, Massachusetts

Research Grant NGR 36-003-067

IMPURITIES AND INTERFACE STATES IN THE SiO_2/Si SYSTEM

CASE WESTERN RESERVE UNIVERSITY

September 1, 1968

Final Report

"Impurities and Interface States in the SiO_2/Si System"

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Principal Investigator: Alan B. Kuper

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SUMMARY

Principle results in the year of grant research to September 1, 1968 are:

1. Hydration of thermal oxide on Si at moderate temperatures analyzed by tritium profiles as a function of time, temperature and pressure, suggests oxide porous structure.
2. Interface-states between oxide and Si controllably produced by dry nitrogen baking between 500 and 700°C. MOS capacitance characteristics at 77°K versus bias, time, and interface-state concentration studied.
3. MOS photocapacitors built and tested.
4. Combined electrical-radiochemical analysis of gold in Si near interface done including MOS C(V) shift and lifetime by diode storage-time and by MOS transient method.

"Impurities and Interface States in the SiO_2/Si System"

Purpose

(1) To understand factors contributing to instability in surface properties of silicon planar devices and (2) To provide information which silicon device engineers can use to improve reliability.

Introduction

Applied Research on this grant is related to current microcircuit technology. The purpose of the work is to improve device process yields and to increase reliability. Silicon surface controls device characteristics to a great extent. Present devices make use of thermally-oxidized Silicon. The Si surface and oxide is the area of our study. Impurities in the vicinity of the oxide/Si interface, and electronic levels in the interface are studied. Charge in the vicinity of the Si determines quiescent surface potential, that is device parameters such as offset-voltage and channel formation. Interface-states determine the ease with which surface potential can be changed, as well as surface lifetime.

This report covers work done in three main areas: oxide hydration, interface-states, and gold effects. The basic approach is to combine electrical MOS measurements with radiochemical impurity analysis. Process steps and hot-bias are the experimental parameters.

Results are:

1. Water-species distribution in oxide as a function of time, temperature, and pressure.
2. Redistribution of water-species in oxide during processing.
3. MOS C(V) transients at $77^{o}K$.
   a) for interface-state analysis, correlated with hydration
   b) for photodetection

4. Gold distribution in Si and oxide compared with electrical effects; MOS C(V), parallel conductance, and lifetime.

These experiments suggest factors which may be valuable to technologists in improving yield and reliability in this area. Our principal result is that water-species distributes anomalously at temperatures about 100°C above room temperature. The results suggest that conventional thermal oxide on Si is not uniform, as generally assumed. The porous structure suggested, may explain a number of observations of failure such as anomalous impurity penetration and breakdown of the oxide.

Oxide Hydration (G. Holmberg)

In these experiments, tritiated water vapor is maintained at constant pressure in a closed system over oxidized Si wafers at constant temperature.

Oxides are near 5400 A in thickness as indicated by interference color. Si is 1 or 10 ohm-cm n-type. Oxide is grown at 1200°C, baked at 1000°C for 1/2 hour. Cleaning just before hydration consists of degrease and deionized water rinsing.

Hydration cell is first evacuated. Samples are brought to temperature. 1 curie/gm radioactive water vapor from thermostated source is introduced. At end of run, sample chamber is cooled. Radioactive water is condensed back to source vial and sealed off. Tritium monitor is installed to detect malfunctions.

Hydrated samples are rinsed to remove detectable radioactivity from surfaces. Aluminum evaporated electrodes are deposited on Si back and on oxide for electrical measurements. Electrodes on oxide are etched off in aqua regia before sectioning.

Sectioning of oxides is done in a teflon holder which is used to minimize total volume of etch in order to maximize detection sensitivity. The holder forms a miniature beaker in which the sample is sealed in to form the bottom. Etch solution, dilute HF, only 0.5 cc.,

followed by water rinse of 1.0 cc. is adequate and can be controlled by this method.

Tritium activity is counted by liquid scintillation. In this method, the radioactive etch plus rinse is added to liquid scintillant with a solubilizer to keep the liquids from segregating. The technique developed in this work to give stable solutions, and therefore reproducible counting, is given in Appendix A.

One count/min. equals approximately 10^{12} hydrogen determined by counting a known quantity. Background is approximately 25 cpm. Thus, detection sensitivity is approximately $4 \cdot 10^{16}$ hydrogen/cm^3 for counting more than one hour. Counting is done in an automatic refrigerated system, Picker Ansitron II. Counting period is selected so that statistical uncertainty is generally less than 5%.

Results

Fig. 1 shows reproducibility of data from four different runs at the same p, T, t. Samples were from two different oxidation runs. Reproducibility is seen to be about ±10%, adequate for interpretation. Note, data is more than 2 times background.

Fig. 2 shows hydrogen penetration from hydration as a function of time at constant T and p. Note for a short time, penetration is anomalous, verified in other runs. Hydrogen concentration in the oxide near the surface is seen to increase with time although experimental conditions are steady-state.

Figure 3 shows penetration as a function of oxide temperature. For the lowest temperature, anomalous penetration is seen. Concentration near the surface increases with temperature.

Fig. 4 shows penetration as a function of water-vapor pressure in the system. The effect of pressure is principally to shift the entire curve. In Fig. 5 we plot average concentration and find it is approximately proportional to $p^{1/2}$. This is evidence that water molecules break into H and OH upon entering the oxide, as has been postulated for the hydration of silica.[1]

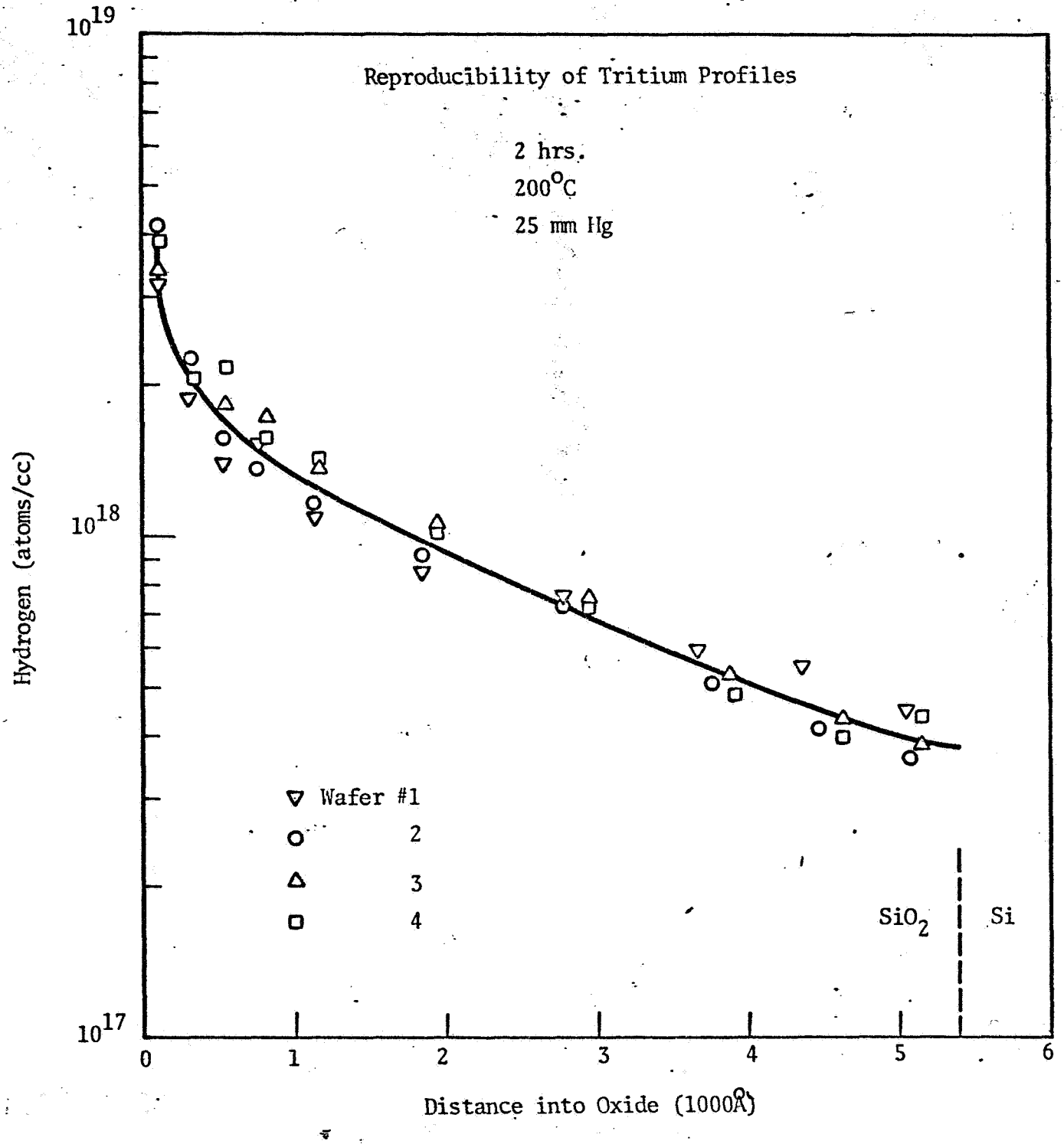

Reproducibility of Tritium Profiles
2 hrs.
200°C
25 mm Hg
Hydrogen (atoms/cc)
10^19
10^18
10^17
Wafer #1
2
3
4
SiO2
Si
0
1
2
3
4
5
6
Distance into Oxide (1000Å)

Fig. 1

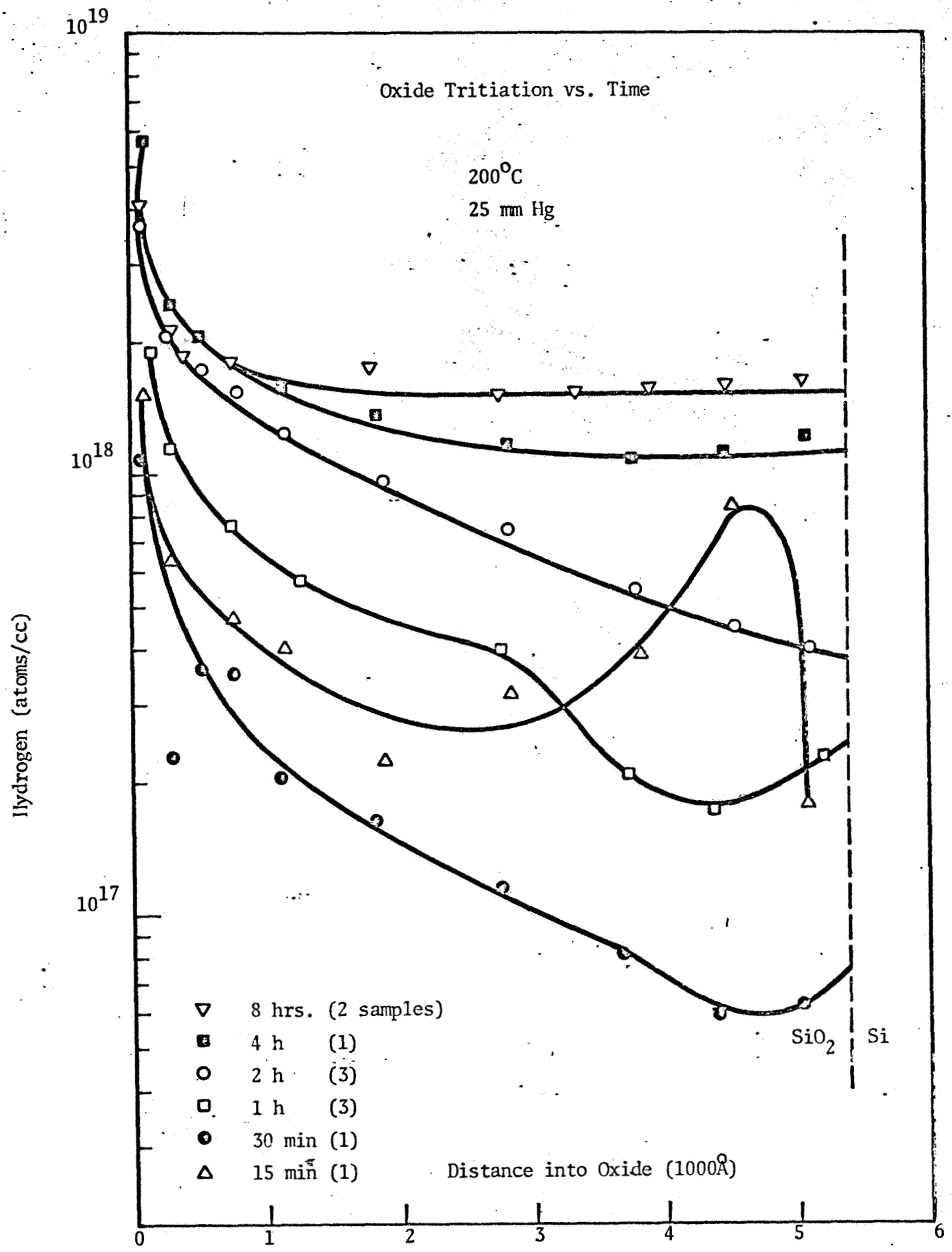

Oxide Tritiation vs. Time
200°C
25 mm Hg
Hydrogen (atoms/cc)
10^19
10^18
10^17
8 hrs. (2 samples)
4 h (1)
2 h (3)
1 h (3)
30 min (1)
15 min (1)
SiO2
Si
Distance into Oxide (1000Å)
0
1
2
3
4
5
6

Fig. 2

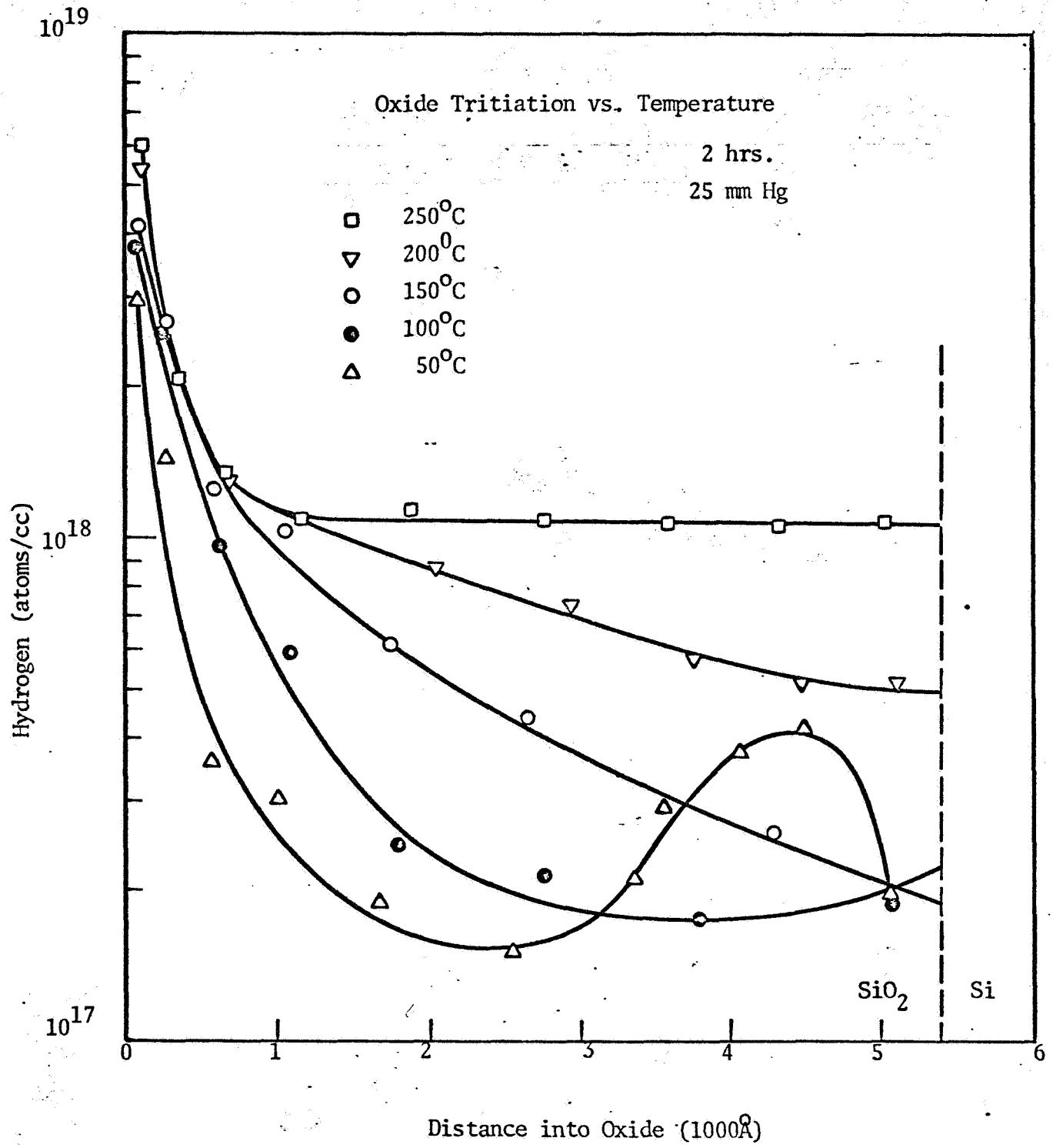

Oxide Tritiation vs. Temperature
2 hrs.
25 mm Hg
250°C
200°C
150°C
100°C
50°C
10^{19}
10^{18}
10^{17}
Hydrogen (atoms/cc)
SiO_2
Si
0
1
2
3
4
5
6
Distance into Oxide (1000Å)

Fig. 3

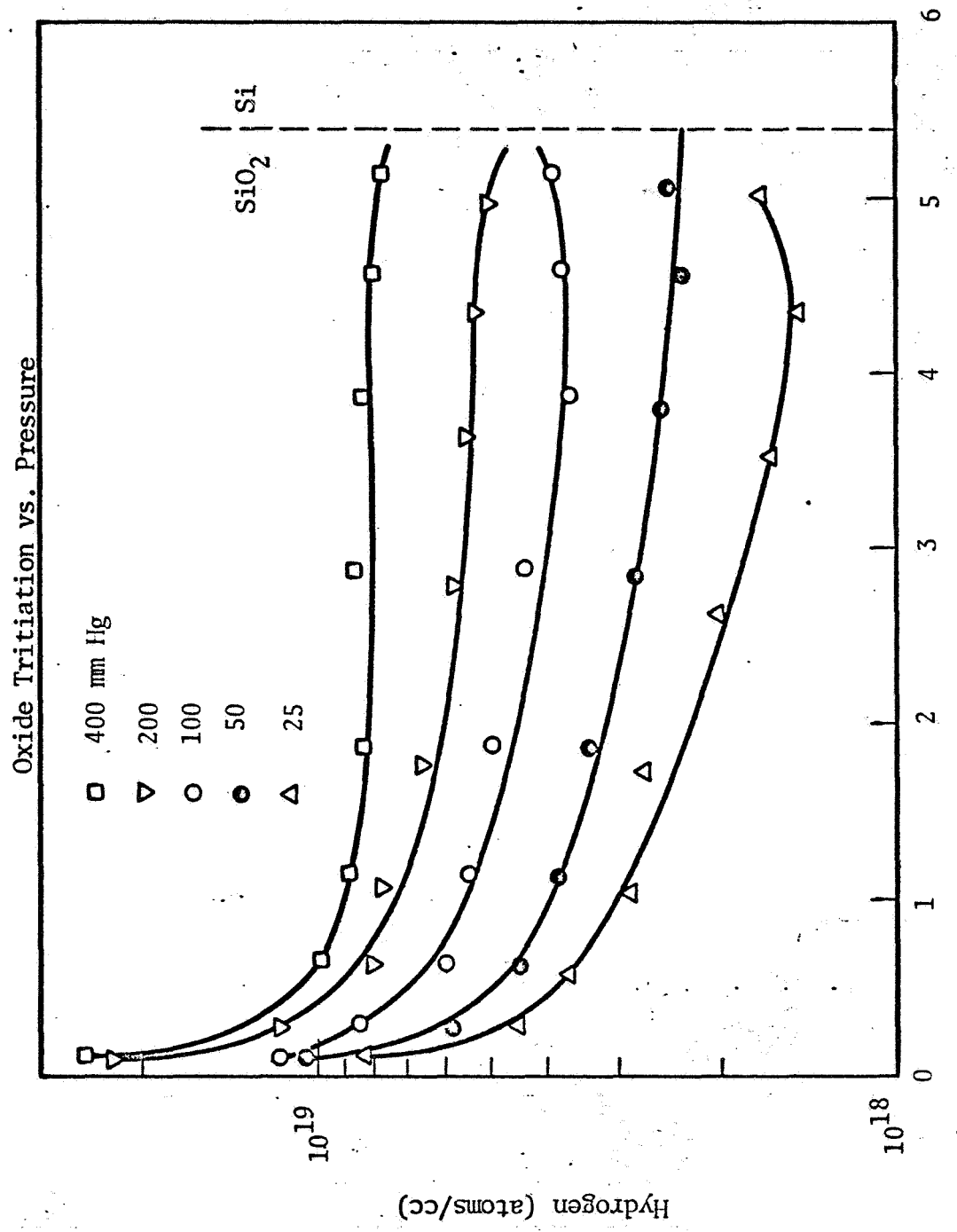

Oxide Tritiation vs. Pressure
400 mm Hg
200
100
50
25
Si
SiO_2
10^{19}
10^{18}
Hydrogen (atoms/cc)
0
1
2
3
4
5
6
Distance into Oxide (1000Å)

Fig. 4

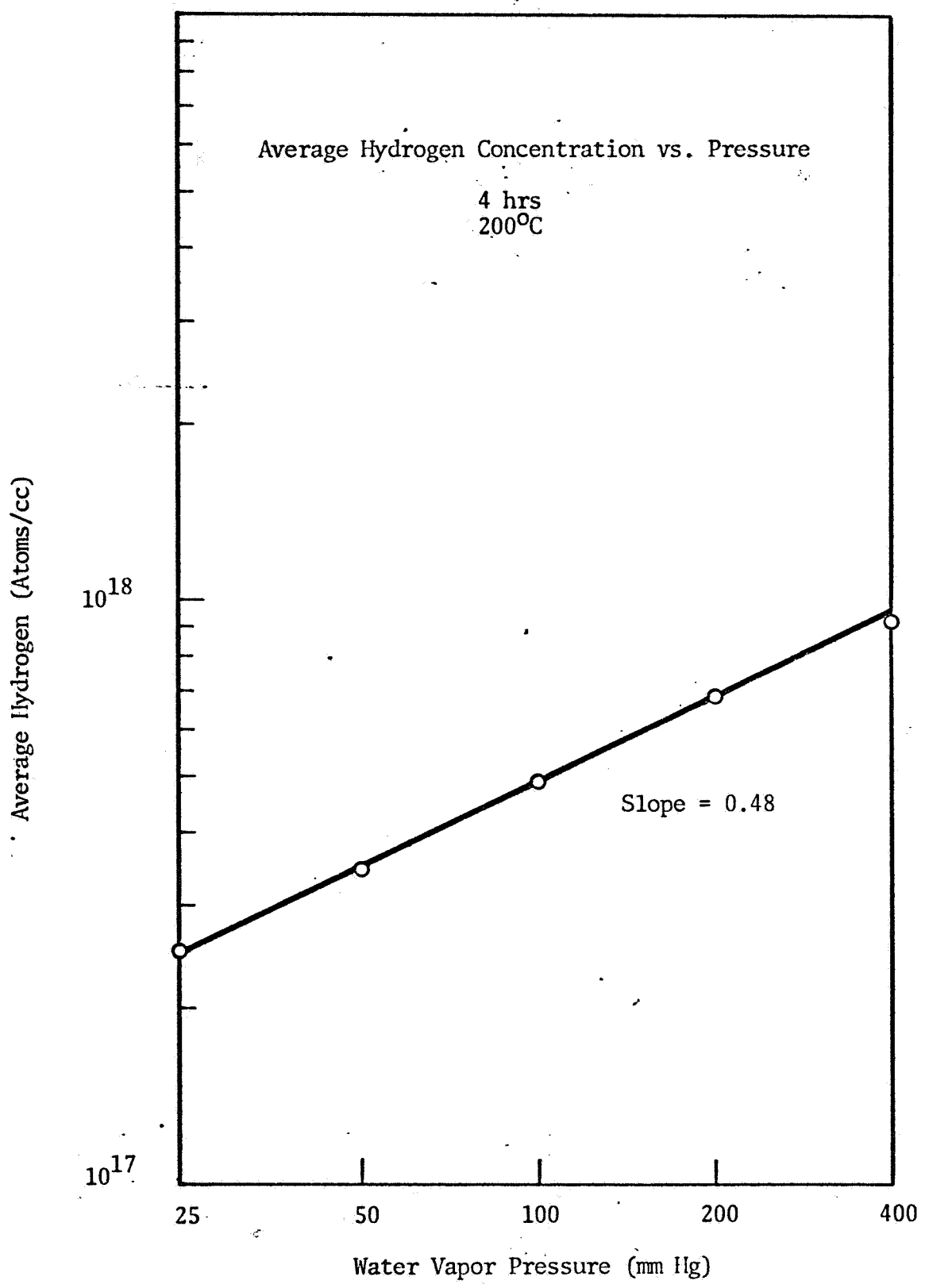

Average Hydrogen Concentration vs. Pressure
4 hrs
200°C
Average Hydrogen (Atoms/cc)
10^18
10^17
Slope = 0.48
25
50
100
200
400
Water Vapor Pressure (mm Hg)

Fig. 5

Interpretation

The most significant features of these results are:

1. Penetration is rapid compared to hydration of fused silica.
2. A spike of concentration exists near the air surface unlike ordinary diffusion.
3. Surface concentration is not a constant.

Penetration of fused silica in 1 hour at 200°C is $2\sqrt{Dt}$ = 1600A extrapolating higher temperature data[2] i.e. for $c_o = 10^{19}$ cm^{-3}, concentration of 10^{17} cm^{-3} would be at a depth of approximately 4500A after 8 hours diffusion into semi-infinite silica. Thus penetration we observe is much greater than expected. This is consistent with an oxide containing "pipes" within which water-species can diffuse rapidly. Experiments on oxide permeation[3] and dielectric breakdown[4] suggest this is the case.

The spike of concentration near the air surface increases with time but does not advance into the oxide with time. This suggests that the outer oxide surface contains a high density of "pipes" mostly extending less than 700A. The observed increase of near-surface concentration would be due, on this model, to bulk diffusion spreading from pipes, giving a weak t dependence as seen in Fig. 2.

Activation energy (Q) for diffusion may be obtained approximately by plotting penetration x at constant concentration, versus temperature, since

$$x \sim D^{1/2} \sim e^{-Q/2kT}$$

The data in Fig. 3 give $Q \cong 0.3$ev. For comparison, activation energy for diffusion of water species in fused silica is about 1ev.[2] Thus not only magnitude of penetration but temperature dependence is other than expected.

In an effort to test this model, the experiment shown in Fig. 6 was performed. One sample was baked in order to outdiffuse water

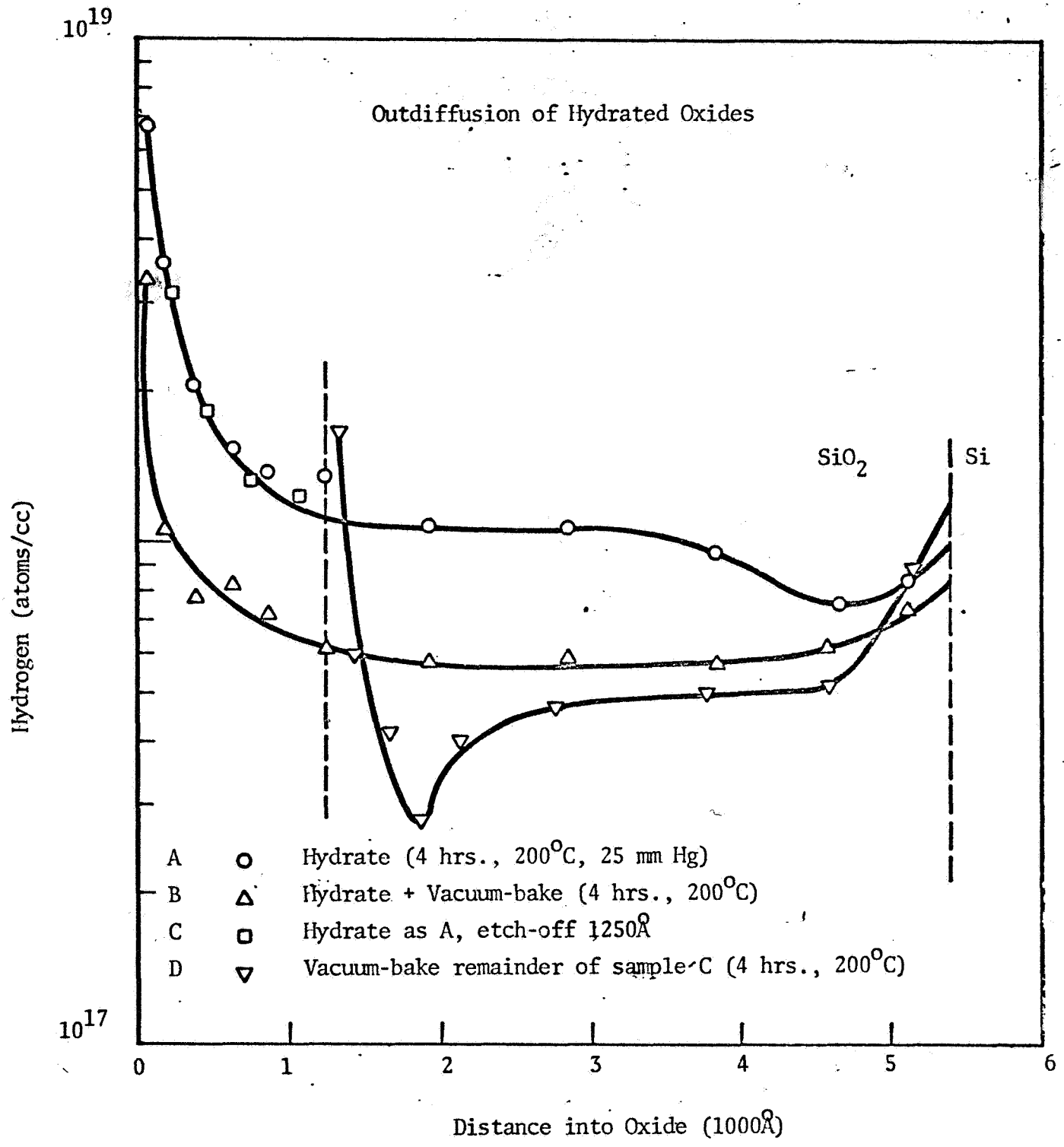

Outdiffusion of Hydrated Oxides
10^{19}
10^{17}
Hydrogen (atoms/cc)
SiO_2
Si
A Hydrate (4 hrs., 200°C, 25 mm Hg)
B Hydrate + Vacuum-bake (4 hrs., 200°C)
C Hydrate as A, etch-off 1250Å
D Vacuum-bake remainder of sample C (4 hrs., 200°C)
0
1
2
3
4
5
6
Distance into Oxide (1000Å)

Fig. 6

species. No outdiffusion profile was observed. Concentration dropped, but surface spike remained. To test whether an outer layer of oxide was responsible for the spike, it was removed before outdiffusion. The result, shown in Fig. 6, suggests that the outer porous layer is characteristic of the oxide, at least after heating to 200°C or more.

Thus the hydration data suggest a model for thermal oxide in which the oxide, due to thermal mismatch, is "piped", with the largest concentration of such pipes in a layer about 700A deep at the free surface where stress-relaxation is greatest.

This model may explain other data:

1. Anomalously rapid permeation reported for gases[3].
2. Selective etching of oxide[4].
3. Precipitates on surface, penetrating the oxide[5].

The model also suggests that improved passivation may be obtained by using a system which has less thermal mismatch than pure SiO_2 on Si.

Oxygen Tracing

This work has had to be postponed. Emphasis this year has been on tritium tracing. Time and budget have been limited for oxygen analysis. Meantime, the scattering chamber is being used by Professor Heuer of Ceramics Department in a Van de Graaff oxide analysis experiment patterned after ours. Detection and resolution determined in those experiments are pertinent to our work.

References

1. A. J. Moulson and J. P. Roberts, Trans. Faraday Soc. 57, 1208 (1961).
2. T. Drury and J. P. Roberts, Phys. Chem. Glasses 4, 79 (1963).
3. S. W. Ing, R. E. Morrison, and J. E. Sandor, J. Electrochem. Soc. 109, 221 (1962).
4. A. D. Lopez, J. Electrochem. Soc. 113, 89 (1966).
5. F. J. Cocca, Trans. IEEE on Electron Devices, to be published.

Interface States (H. P. Caban-Zeda)

Interface-states of interest in devices are electron energy levels located in the energy gap at the silicon surface which can change charge-state under operating conditions. Control of these states is as essential as control of impurities.

The effect of interface-states on the surface potential of n-type Si is shown in the room temperature C(V) of Figure 7. As dc voltage is reduced, Si depletes and C drops. The usual drop of C is distorted just before inversion, indicating interface-states which discharge electrons as the energy bands are bent upward.

Three basic purposes lie behind this study: (1) to observe the effects of processing (baking, hydration, etc.) on interface-state density, N_{ss}, as fundamental to their eventual prediction and control; (2) to study N_{ss} characteristics and analyze MOS C(V) transients at low temperature, particularly those aspects related to N_{ss} contributions; (3) to investigate the relationship between impurities (such as water or Na) and N_{ss}. Identification of avalanche-type processes in the MOS C(V) transients at low temperatures has also been contemplated.

Fundamental to this study is the method of Gray and Brown[1] for measuring N_{ss}. The method consists of obtaining MOS C(V) characteristics both at room temperature and at low temperature. The low temperature ($77^{o}K$) is such that the Fermi level in the bulk approaches the conduction band for n-type (valence band for p-type) material. For n-type material, for example, most of the surface states in the upper half of the band gap charge more negative. This, in turn, shifts flat-band voltage toward more positive (Fig. 7). The relationship between the flat-band voltage shift from low temperature to room temperature, $\Delta V_{fb} = V_{fb}(77^{o}K) - V_{fb}(\text{room temperature})$, and N_{ss} is given by :

$$|N_{ss}| = \frac{C_{ox}}{e} |\Delta V_{fb}| = \frac{\varepsilon_{ox}}{e x_o} |\Delta V_{fb}| \qquad (1)$$

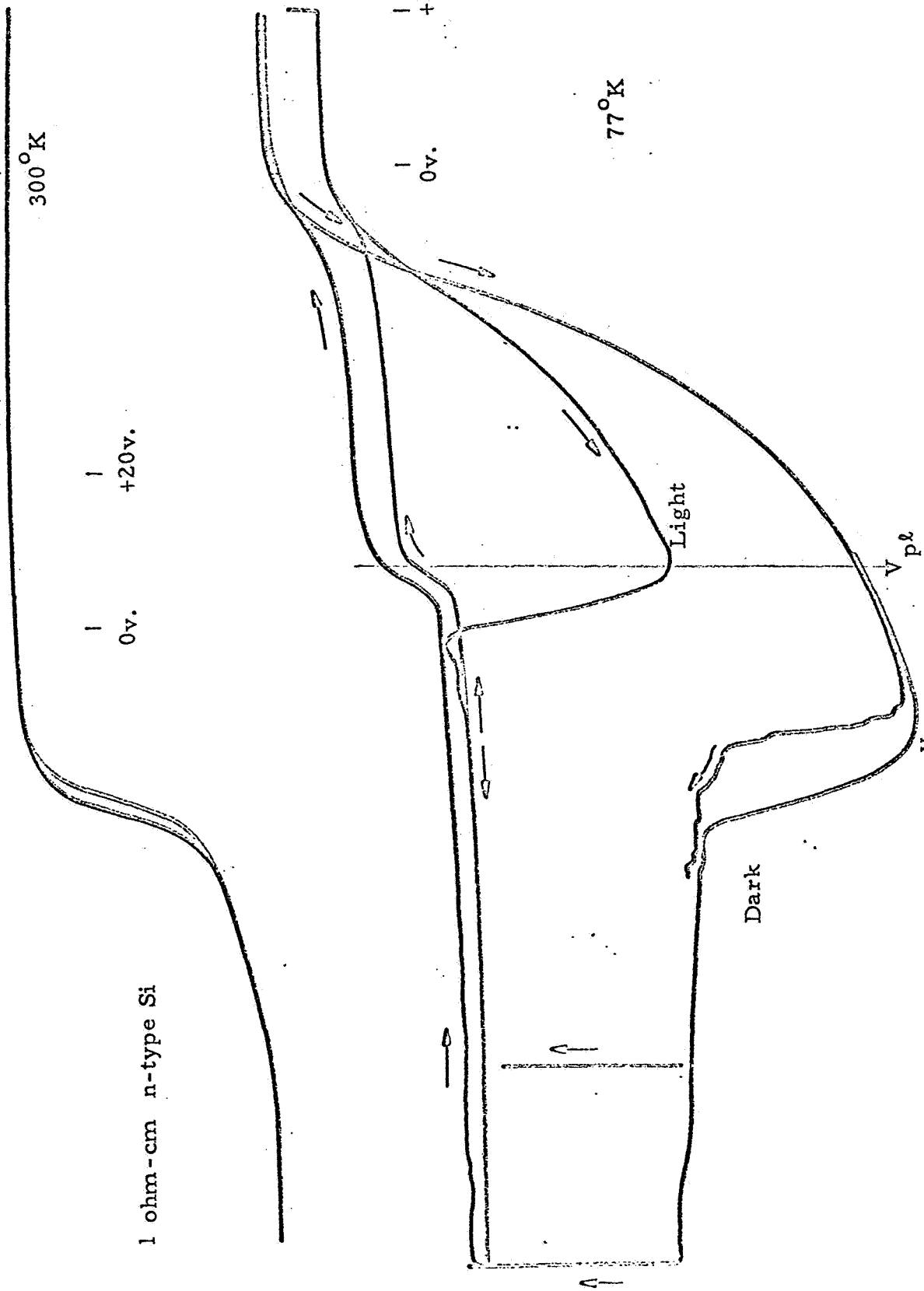

MOS C(V) at Room Temperature and at 77°K
1 ohm-cm n-type Si
300°K
0v.
+20v.
77°K
0v.
+20v.
Light
Dark
$V_{p\ell}$
V_{pd}

Figure 7

where C_{ox}, ε_{ox}, and x_o are the oxide capacitance, dielectric constant, and thickness, respectively, and e is the electronic charge. Measurement of surface states lying in the lower half of the energy gap requires the use of p-type material. Density of surface states as a function of energy within the band gap can be obtained by observing changes in V_{fb} as temperature is changed, and relating this to position of the Fermi level in the bulk of the substrate.

Oxides used in the MOS structures were grown at 1000°C in wet oxygen (T_{water} = 92 - 94°C, 1 lt./min.) to a thickness of either 2000 or 5400 Å. Aluminum contacts were evaporated on the Si wafers (dots on the top and a film covering all or most of the area on the back).

The relatively complex character of the low temperature MOS C(V) characteristic has spawned considerable interest in its analysis and understanding[2]. A description of its salient features as found for n-type material follows.

In dark at moderate scan from accumulation toward negative voltage we observe transient deep depletion of the Si (Fig. 7 and 8). This transient is due to the inability of the minority carriers (holes) to reach equilibrium. The field is then terminated by unshielded donors in a depletion region whose width increases approximately linearly with field. The variation of C with V, in this region, may be obtained as follows. We may relate dV to the corresponding change in the depletion region width, dx, by adding the changes in the potential drops across oxide and substrate

$$dV = e(N_D - N_A)\left(\frac{x}{\varepsilon_s} + \frac{x_{ox}}{\varepsilon_{ox}}\right) dx, \qquad (2)$$

where x_{ox} is the oxide thickness and ε_s and ε_{ox} are the substrate and oxide dielectric constants respectively. Other symbols have their usual meaning. The differential capacitance is given by

$$\frac{1}{C} = \frac{x_{ox}}{\varepsilon_{ox}} + \frac{x}{\varepsilon_s} \qquad (3)$$

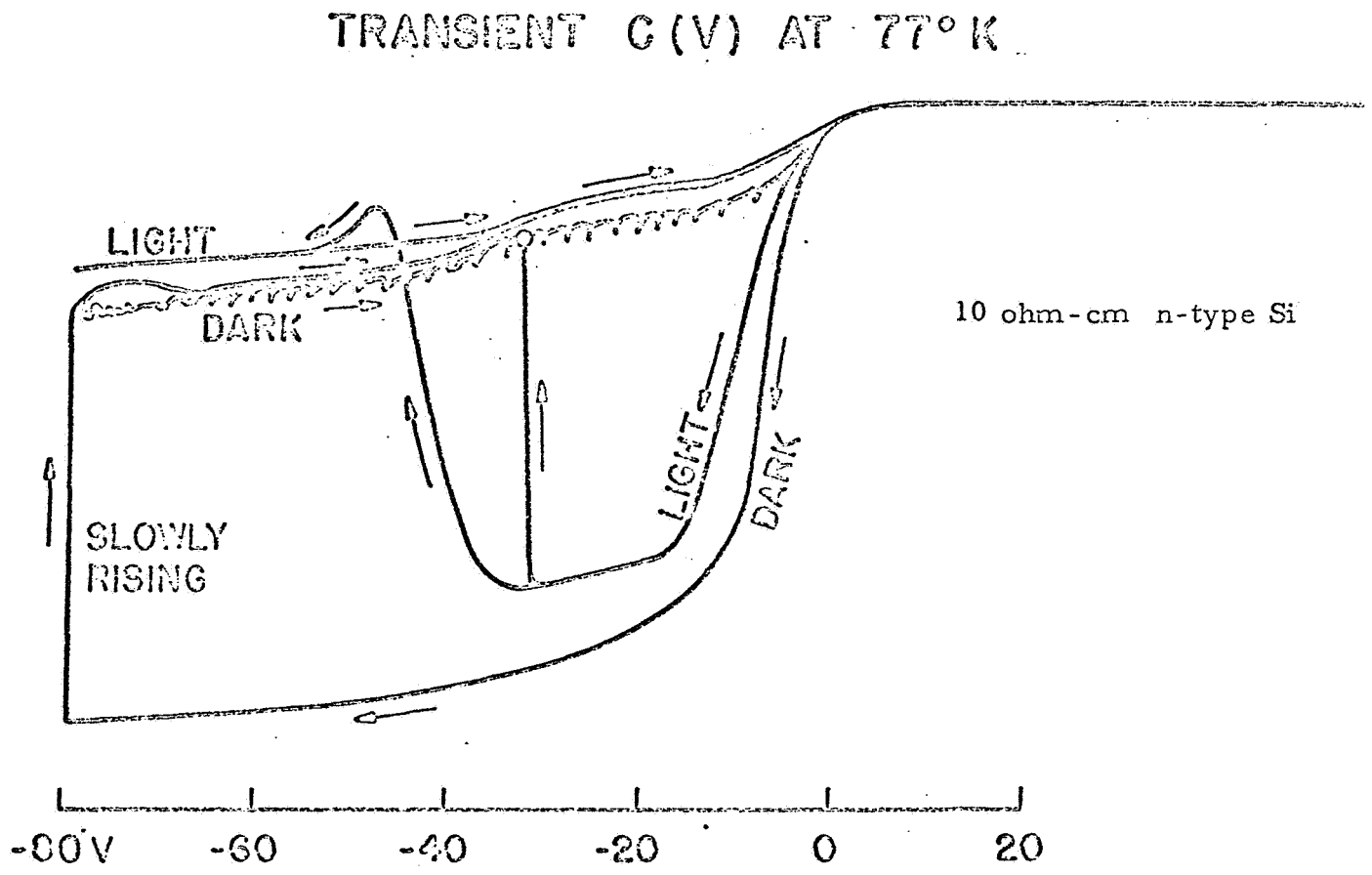

TRANSIENT C(V) AT 77° K
LIGHT
DARK
SLOWLY
RISING
LIGHT
DARK
10 ohm-cm n-type Si
-80V
-60
-40
-20
0
20

Figure 8

Integrating equation (2) between V and V_o, any two voltages lying within the deep depletion transient region, solving for W and substituting in (3) yields

$$\frac{1}{C^2} = \frac{1}{C_o^2} + \frac{2}{e\varepsilon_s(N_D-N_A)}(V - V_o), \qquad (4)$$

where $C_o = C(V_o)$.

Fig. 9 shows a plot of $1/C^2$ vs. V which agrees fairly well with a straight line. The slope of the line, however, does not agree with the theory. It gives an $|N_D-N_A|$ about half the measured doping. This is believed to be due to the fact that at 77°K considerable "freeze-in" of the donors is taking place and cannot be appropriately taken into consideration in a simplified approach such as that outlined above. Goetzberger and Nicollian[3] have studied the deep depletion transient by using a pulse technique at room temperature, avoiding therefore the "freeze-in" effect. They obtain good agreement with equation (3).

The rate at which the system tries to reach equilibrium, decreases as the applied bias becomes more negative and is very sensitive to light (increasing with light intensity), as would be expected from increased generation of holes by light. Further increase in negative bias usually results in a sudden increase in capacitance at a certain value of bias, V_{pd}, which depends, on substrate resistivity, density of surface states, and oxide thickness. The transient, however, does not end here, since the capacitance continues to rise slowly with time till a certain value is reached which is slightly lower than that in the light.

The possibility of avalanche processes giving rise to the abrupt termination of the deep depletion transient has been considered. For this to be the case, however, a definite relationship between V_{pd} and the substrate resistivity should be expected. Evidence for the effect can be seen in Fig. 7 compared to Fig. 8. However, experiments where substrate resistivity and oxide thickness were systematically varied failed to disclose definite correlation between V_{pd} and substrate

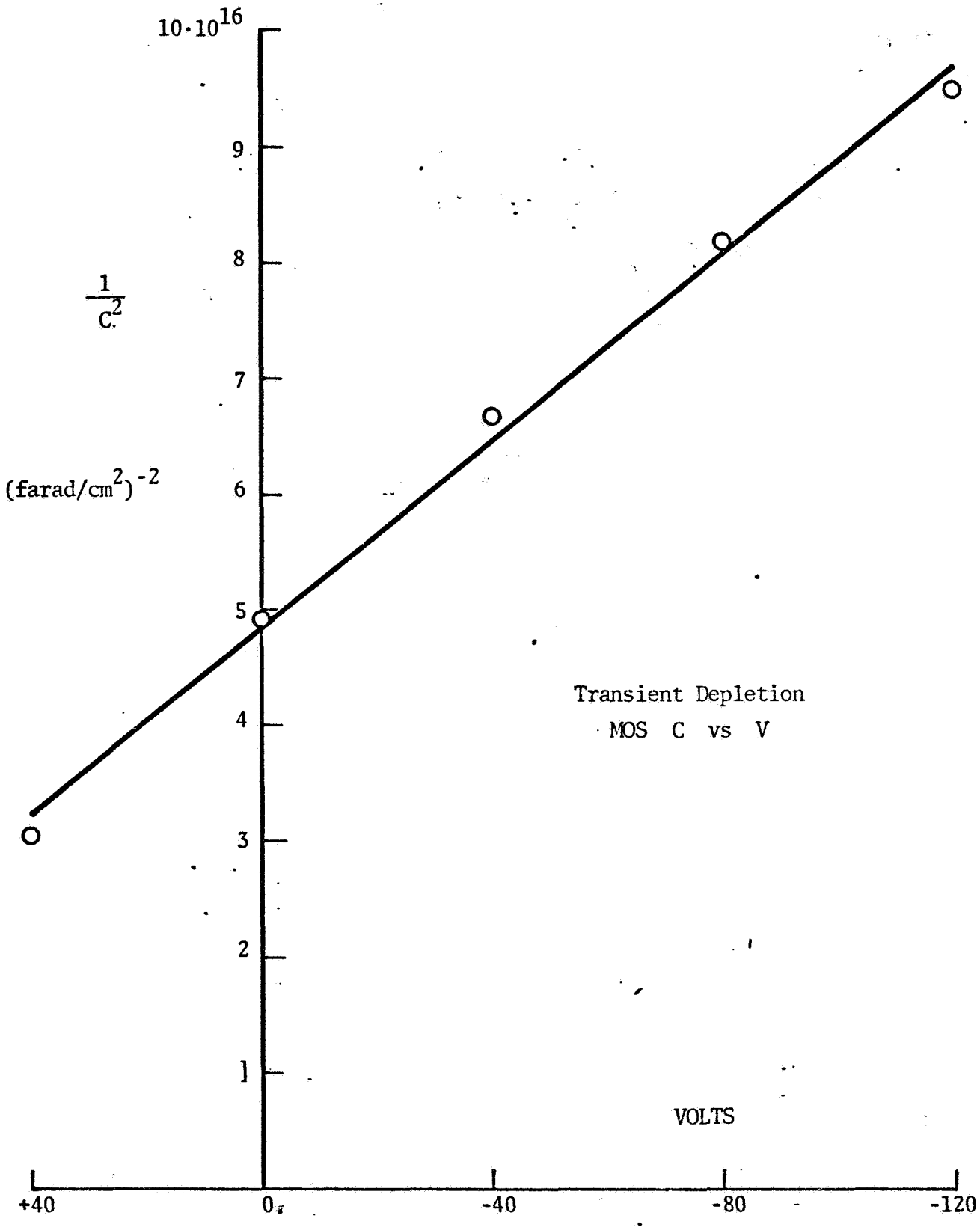

10·10^16
9
8
1/C^2
7
(farad/cm^2)^-2
6
5
4
3
2
1
Transient Depletion
MOS C vs V
VOLTS
+40
0
-40
-80
-120

Fig. 9

resistivity. Moreover, values of V_{pd} tend to be considerably higher than expected from pn junction measurements. V_{pd} increases with N_{ss}. This is shown in Table 1.

Scanning the bias toward the positive side, a "plateau" in the capacitance can be observed whose width (W) depends on density of surface states and oxide thickness.

In the light, the deep depletion transient is terminated at a bias, V_{pl}, smaller than V_{pd}, which coincides with the more negative edge of the "plateau". In contrast with the dark case, however, the capacitance now reaches a final steady-state value immediately after V_{pl} is reached. Scanning back toward accumulation, the "plateau" is still observed.

If we assume that the deep depletion transient corresponds to the Fermi level traversing the surface states, then we might expect electrons being discharged from the energy states (as the voltage is scanned toward inversion) to recombine with holes being generated by the light. The holes, then, are not able to reach their equilibrium concentration and a deep depletion transient ensues. Once the Fermi level has traversed all the surface states, then, minority carriers can accumulate and the transient ceases. Further evidence of this we have found is that W, and thus V_{pl}, is proportional to N_{ss}, as discussed later.

The evaporated aluminum contacts on top of the oxides were, usually, of sufficient thickness to be opaque to room light. Using very thin ($\lesssim$600 A in thickness) transparent aluminum contacts disclosed that, under moderate light, the deep depletion transient was absent. The C(V) curve would, under such circumstances, retrace itself as the bias was scanned back and forth.

It should be mentioned that, in the dark, the 77^{o}K C(V) curve obtained by scanning the voltage from depletion toward accumulation is always slightly higher than that obtained by holding bias constant, allowing the system to reach "equilibrium", and then joining the points thus obtained. However, this second curve also exhibits a "plateau". Figures 7 and 8 show these characteristics.

Table I

Table I shows typical values of V_{pd}, substrate resistivities, and N_{ss}.

Typical Values of V_{pd}

Substrate Resistivity (Ω-cm)	Oxide Thickness (Å)	V_{pd} (v)	$V_{pd} - V_{fb}$* (v)	N_{ss} (10^{11} cm^{-2})
0.41	5400	-47	-24	1.4
0.41	5400	-176	-216	35
1.38	2000	-16	-12	1.0
1.38	2000	-27	-24	4.3
1.38	5400	-34	-20	0.4
1.38	5400	-56	-43	3.2
2.73	5400	-37	-25	0.8
2.73	5400	-111	-125	15

*V_{fb} is approximate flat-band voltage at $77^{o}K$.

A definite correlation has been found between N_{ss} and the width of the "plateau", W. This is shown in Figures 10 and 11. From this figure it can be seen that

$$W/\Delta V_{fb} \cong 2 \qquad (5)$$

Gray and Brown have reported a distribution of surface states density characterized by a peak of donor-type energy states near the valence band and a peak of acceptor-type energy states near the conduction band, the total number of each being about the same. The result described by equation 5 suggests that the total excursion of the Fermi level across the surface band gap as the bias is scanned from inversion to accumulation is such that it traverses, not only the acceptor, but the donor-type energy states as well. The width of the "plateau", being proportional to N_{ss}, would then be twice ΔV_{fb}.

It is interesting to note that, whenever surface states are present in sufficient numbers ($\gtrsim 10^{11}$ cm^{-2}.), the room temperature C(V) characteristics do not level off in the inversion region till a certain bias is reached (see Fig. 7), this bias being roughly the same as V_{pl}. This, plus equation 5, facilitates prediction of W, V_{fb}, and thus N_{ss}. Care should be exercised in the use of room temperature curves for the prediction of N_{ss} however, since the results are only approximate.

The effects of baking and hydration on N_{ss} have been investigated. Temperature and duration of baking have been varied and correlated with the amount of N_{ss} introduced. It has been found that the "harder" the bake, the more N_{ss} will be created for temperatures up to about 800°C. Bakings at 1000°C, however, reverse the trend, since N_{ss} created under such conditions is lower than would be expected. This may be related to cooling procedure. Table II lists some representative values of N_{ss} and corresponding baking conditions. The results are reproducible and, therefore, we are in a position to create surface-states in predetermined numbers.

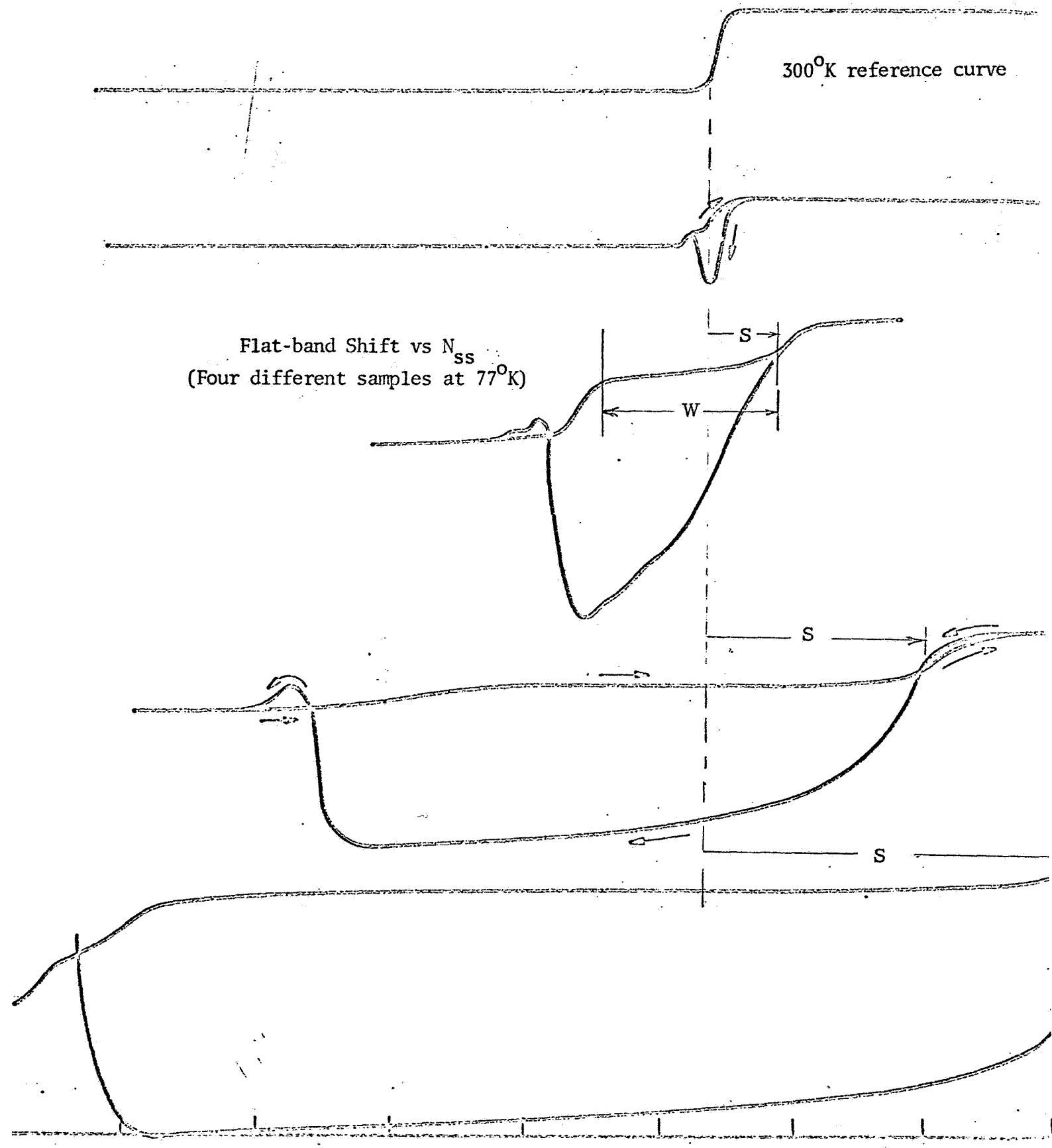

300°K reference curve
Flat-band Shift vs N_{ss}
(Four different samples at 77°K)
S
W
S
S

Figure 10

W vs. S

(Plateau Width vs. "Flat-band" shift)

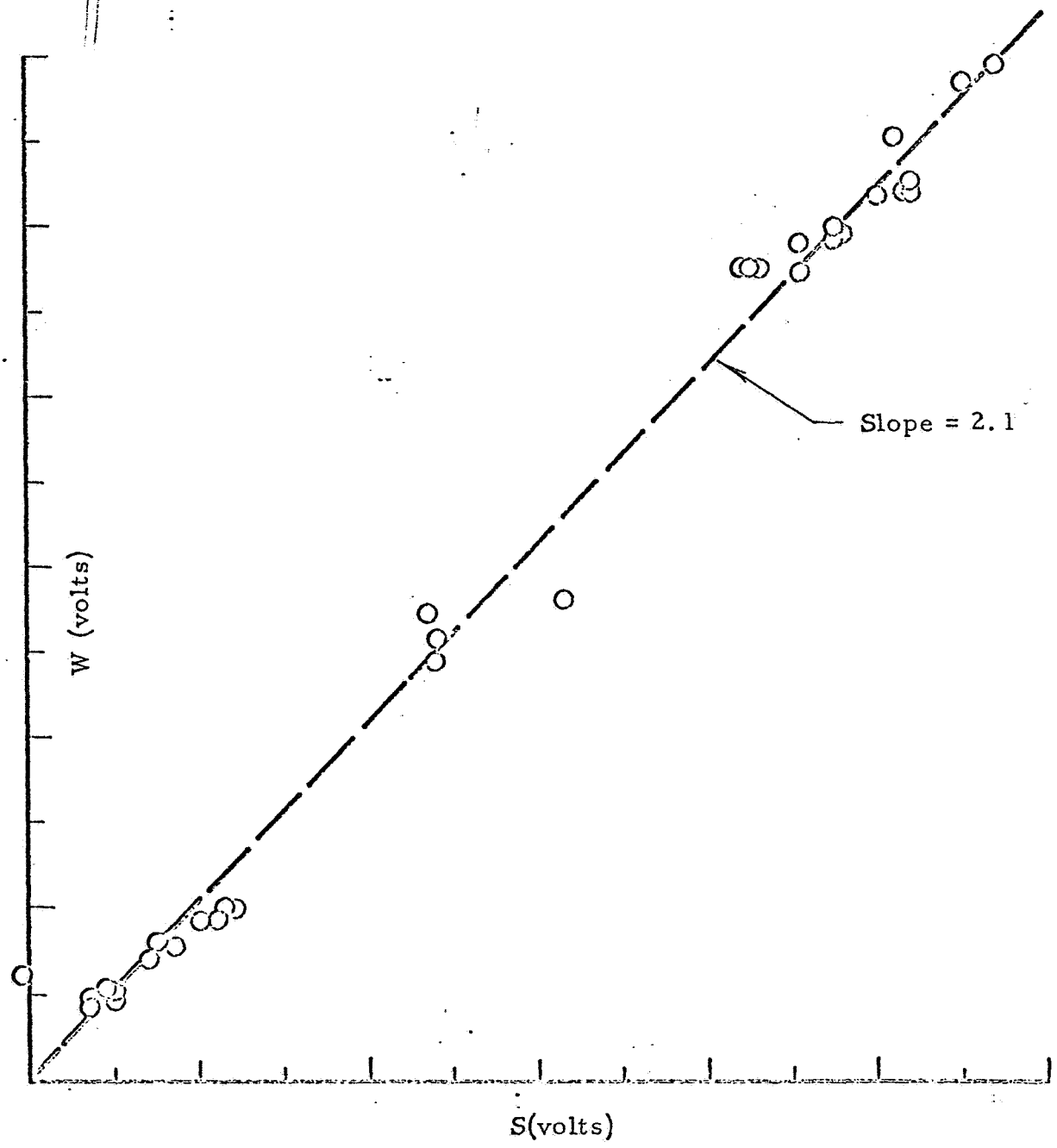


Figure 11

Table II

N_{ss} vs. Baking

Temp. (°C)	Time (min.)	Oxide Thickness (Å)	Substrate Resistivity (Ω-cm.)	V_{fb} (volts)	N_{ss} (cm^{-2})
700	10	5400	0.41	88	3.52×10^{12}
600* & 550	10* & 30	5400	2.73	37	1.48×10^{12}
500	60	2000	1.38	4	4.32×10^{11}
500	60	5400	1.38	8	3.2×10^{11}

*This sample was subjected to two bakings, one at 600°C for 10 min., and another at 550°C for 30 min.

The role of water in the control of N_{ss} has been analyzed by electrical and radiochemical measurements. After a known amount of N_{ss} was introduced (by baking) and measured, samples were hydrated under varying conditions with tritiated water and the N_{ss} remeasured. Then, water-species profile in the oxide was determined by radiochemical methods. These profiles are found elsewhere in this report.

It was found that no significant reduction of N_{ss} was achieved by hydrations at low temperatures (see Fig. 12), even though water content near the Si/SiO_2 interface, if each water-specie annihilated one interface state, was sufficient to produce an easily measured reduction in N_{ss}. A hydration at $800^{o}C$ for a short time, however, was effective in annihilating a large number of surface states.

Experiments to investigate the time dependence of Na drift showed that N_{ss} increased as Na pile-up at the Si/SiO_2 interface increased, as evidenced by both room temperature and $77^{o}K$ measurements. In particular, room temperatures disclosed that the distortion associated with surface states shifted its position in the inversion portion of the curve as the Na drift proceeded, as shown in Fig. 13. This suggests that contamination may be at least partly responsible for the number and character of surface-states. This result is being investigated further at present with combined electrical and radiochemical measurements after controlled contamination of samples.

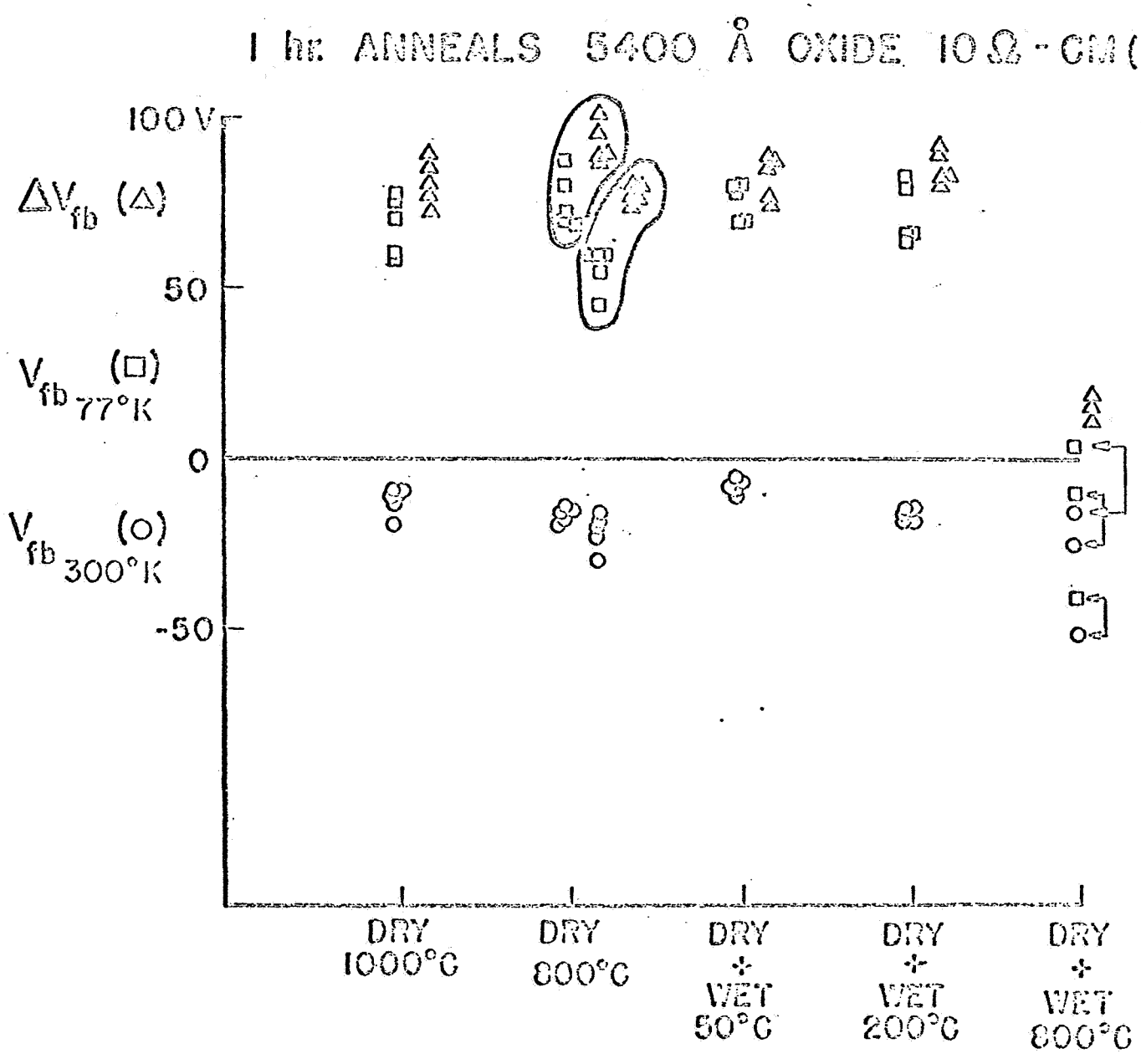

1 hr. ANNEALS 5400 Å OXIDE 10 Ω-CM
100 V
ΔV_fb (Δ)
50
V_fb 77°K (□)
0
V_fb 300°K (○)
-50
DRY 1000°C
DRY 800°C
DRY + WET 50°C
DRY + WET 200°C
DRY + WET 800°C

Figure 12

MOS C(V) Distortion vs. Na Drift
(NaOH contamination)

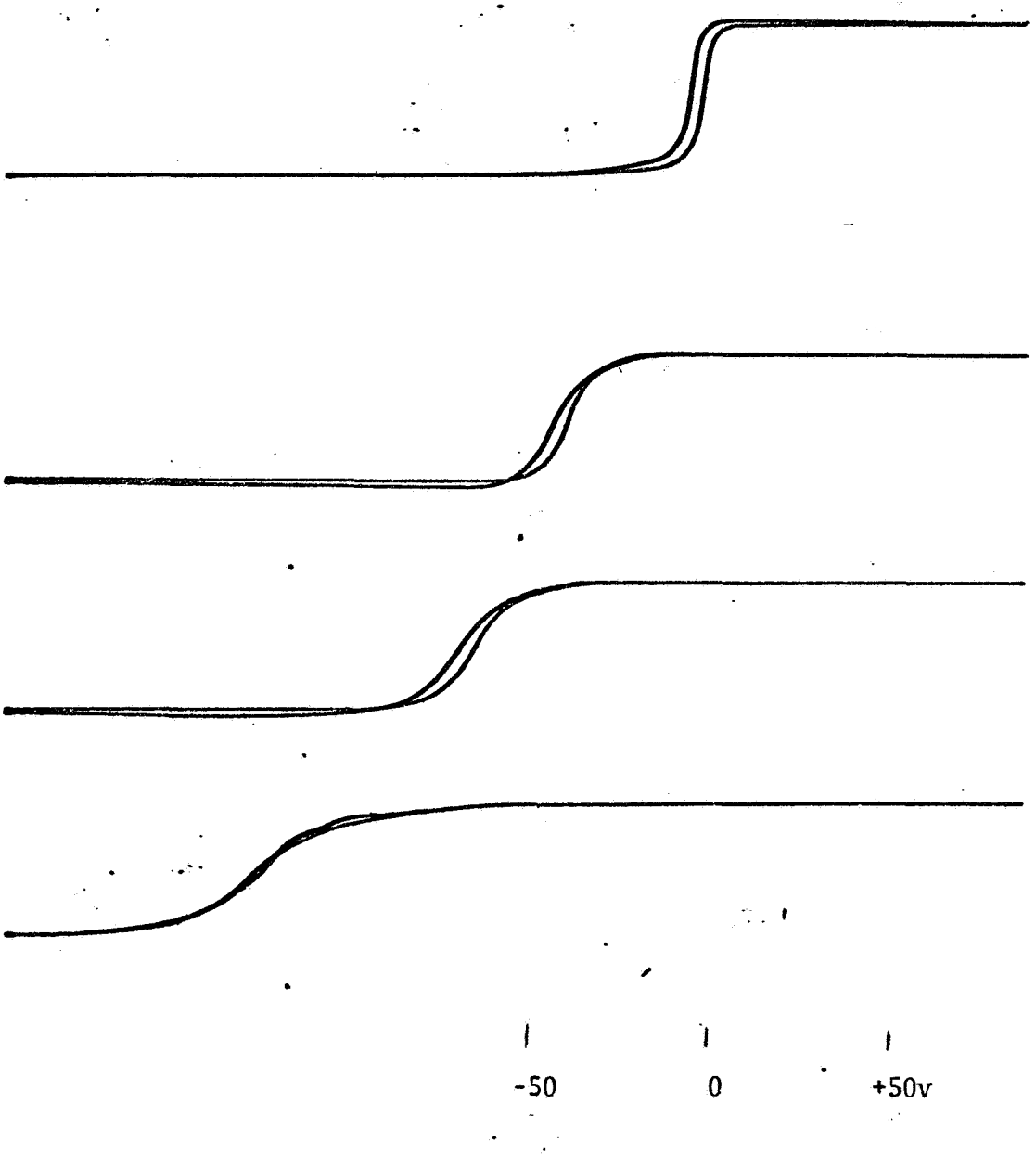


Fig. 13

Summary

1. Interface states (N_{ss}) are controllably introduced by baking in dry N_2.
2. Low temperature transient MOS characteristic is related to N_{ss}.
3. Room temperature characteristic is compared to low temperature.
4. "Plateau" width is studied.
5. Effect of light, resistivity, oxide thickness is studied.
6. Effect of hydration using tritium analysis is compared to N_{ss}.
7. N_{ss} is related to Na impurity in oxide.

References

1. Peter V. Gray and Dale M. Brown, Applied Physics Letters, 8 No. 2, 31-33 (1966).
2. D. M. Brown and P. V. Gray, J. Electrochem. Soc. 115, 760 (1968).
3. A. Goetzberger and E. H. Nicollian, Applied Physics Letters, 9 No. 12, 444-446 (1966).

MOS Photodevice (E. Greenstein)

During this grant period, initial experiments were done to explore the MOS as a photodevice. Such a device would have the advantage of fabrication simplicity, requiring no diffusion or alloying.

This work grew out of our observations of MOS photosensitivity at 77°K. Understanding of this device might show that room temperature operation would be possible with a similar approach.

Experiment

MOS photodevices were fabricated using transparent chromium evaporated field plates on 3000Å oxide. For bonding a lead, gold was evaporated over all, then selectively etched to leave a pad using photo-masking and Hope gold etch. Dice were mounted on TO-18 headers at approximately 400°C and leads thermal-compression bonded. (Figure 14)

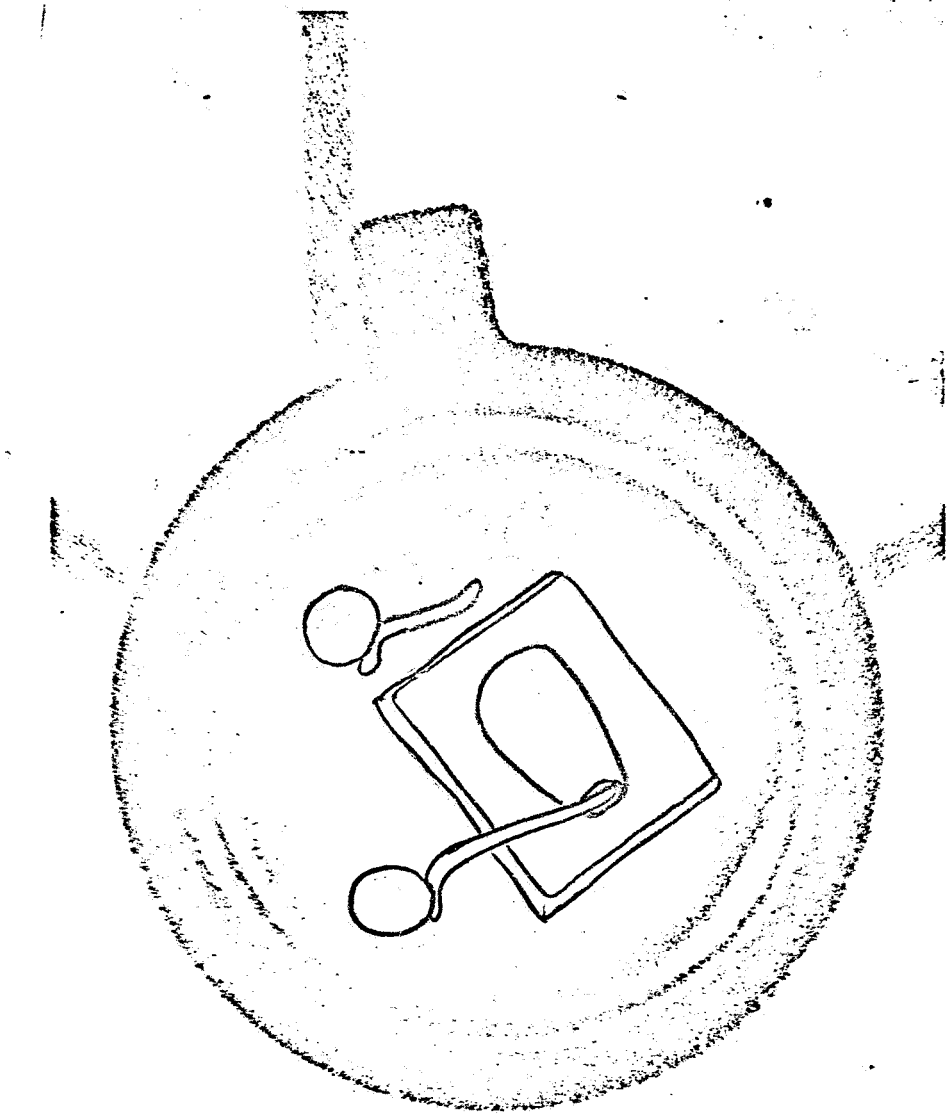
The open MOS device was immersed in liquid nitrogen. Signal leads were brought to the device socket and a light was placed near. A light-tight enclosure was secured around the apparatus.

The MOS was connected as shown in Figure 15. Typical test condition, as shown, was a 10ms. positive or negative 25v pulse in a 10% duty cycle.

Results

(1) As shown in Table III, response of typical pre-baked devices depends on polarity of input voltage. v_{in} is applied to the field-plate with respect to ground.

(2) Unbaked samples respond to light only for $-v_{in}$ not for $+v_{in}$.



MOS Photo-Capacitor

Fig. 14

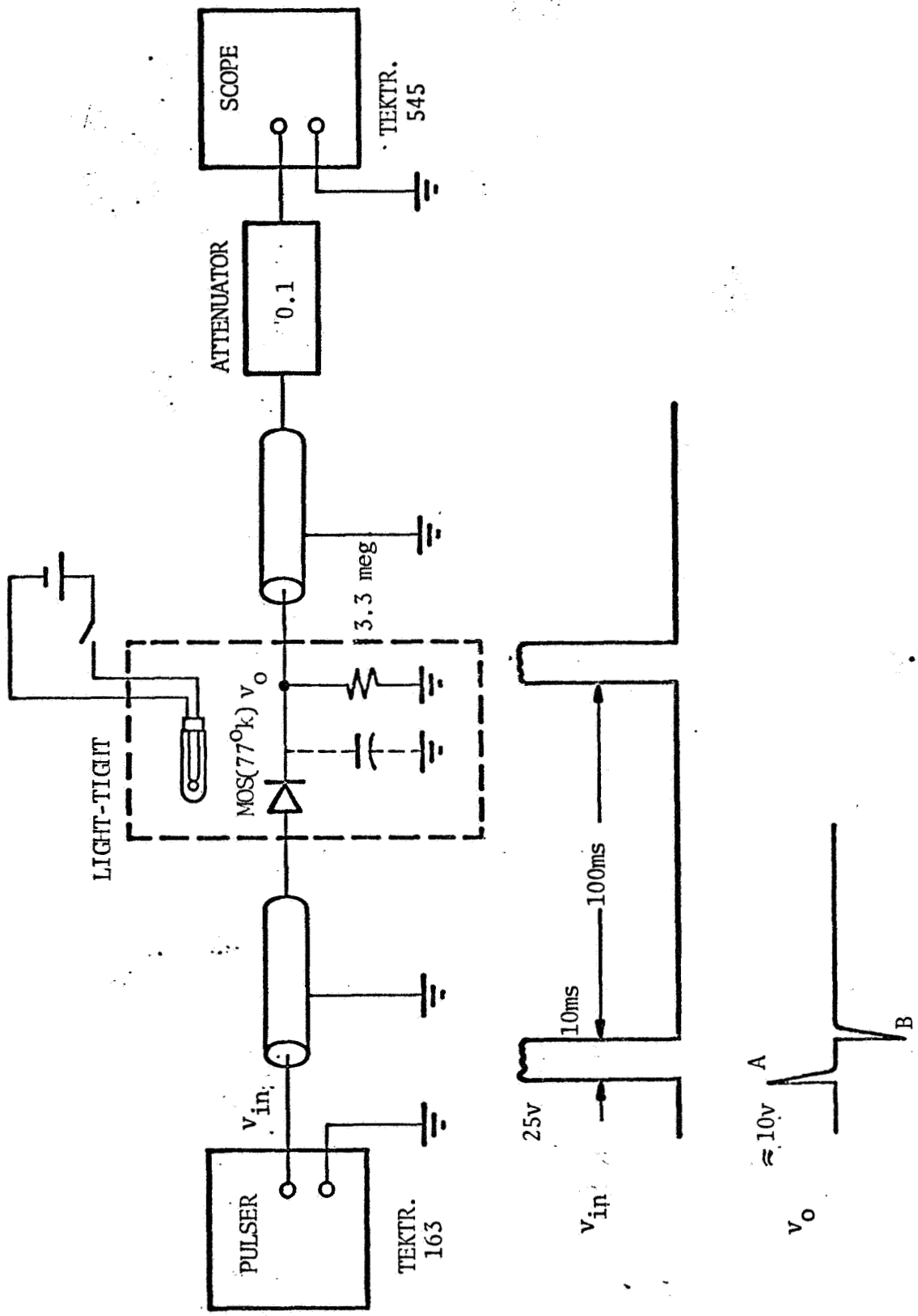

SCOPE
TEKTR. 545
ATTENUATOR
0.1
3.3 meg
LIGHT-TIGHT
MOS(77°k) v_o
v_{in}
PULSER
TEKTR. 163
25v
10ms
100ms
v_{in}
≈10v
A
B
v_o

Fig. 15

(3) Input pulse duration has an effect when $-v_{in}$, relatively little effect when $+v_{in}$. As pulse width is increased, response increases (lus. to 11ms).

(4) Most important, device responds at room temperature for $-v_{in}$. Response is about half that observed at 77^0K.

Interpretation

These results are tentatively understood by referring to C(V) characteristics like those in Fig. 8 with the difference that zero bias is located within the wide "plateau" after heavy pre-bake (30 min., 1200^{o}C). Integrated light intensity determines average capacitance, $\bar{C}$, under steady-state bias conditions. Stray capacitance, shown in Fig. 15, is responsible for making peak v_o less than v_{in} given by:

$$v_o = v_{in} \frac{C}{C + C_s} \exp\left(- \frac{t}{R(C + C_s)} \right) \qquad (6)$$

In dark, $\bar{C}$ is relatively low. Approximately same steady-state deep depletion is reached for either pulse polarity. In deep depletion C(V) is nearly flat, so $A \cong B$ (Fig. 15). In Table III, peak v_o is relatively small corresponding to small $\bar{C}$, small charging and discharging current.

In light, $\bar{C}$ increases resulting in larger peak v_o. Because of the C(V) hysteresis, $\bar{C}$ (and peak v_o) is larger when voltage is positive-going. In light for $+v_{in}$, $\bar{C}$ is larger relative to that for $-v_{in}$ because bias cycle is not driving toward deep depletion for $+v_{in}$.

This interpretation assumes that charging and discharging of interface-states is a second-order effect. Interface-states are important in that they shift the low temperature C(V) characteristic. Thus unbaked samples, pulsed from zero bias, do not show photocapacitive effect for positive gate voltage because the Si accumulates and is not appreciably photosensitive.

Table III

Peak v_{in}		Peak v_o Dark	Peak v_o Light
-25v	A	2v	2.4v
	B	2	8.
+25v	A	2	18.5
	B	2	10

10 ohm - cm n-type Si
Pre-Baked 30 min. at 1200°C

Gold Effects (C. J. Slabinski)

Grant research this year has been in two main areas of radiochemical gold measurements: (1) correlated with MOS capacitance and (2) correlated with minority carrier lifetime near the Si surface.

Gold compensates bulk Si, with the result that MOS capacitance minimum (C_{min}) decreases. This effect was calculated[1] and discussed in the grant report last year. Combined electrical/radiochemical analysis gives fraction of electrically-active gold contributing to $-\Delta C_{min}$.

Gold was vacuum-evaporated onto backs of oxidized Si wafers and diffused at 1000°C into Si. Fig. 16 shows gold concentration measured by neutron activation and gamma spectrometry vs that measured by $-\Delta C_{min}$. The two agree from about $1\text{-}5\cdot10^{15}$ cm^{-3}, with evidence of non-active excess gold at higher concentrations. Precipitation of excess gold near the interface during cool-down is the probable cause.

Additional evidence for excess gold is shown in Fig. 17 in which gold concentration, measured radiochemically, increases as diffusion proceeds, finally exceeding the limit of solid solubility in Si at 1000°C. (At lower temperatures, solubility limit is less.)

Main conclusion from this work is that the method of MOS $-\Delta C_{min}$ is probably a good measure of electrically active gold in Si near surface.

Electrical measurement of minority-carrier lifetime was by MOS transient technique[2]. This was checked by storage-time measurement of shallow junction alloyed aluminum diodes fabricated side-by-side with the MOS capacitors. Gold concentrations were obtained from $-\Delta C_{min}$ after the alloying cycle, a two-minute furnace heating to slightly above the Al-Si eutectic. Table IV shows results of diode

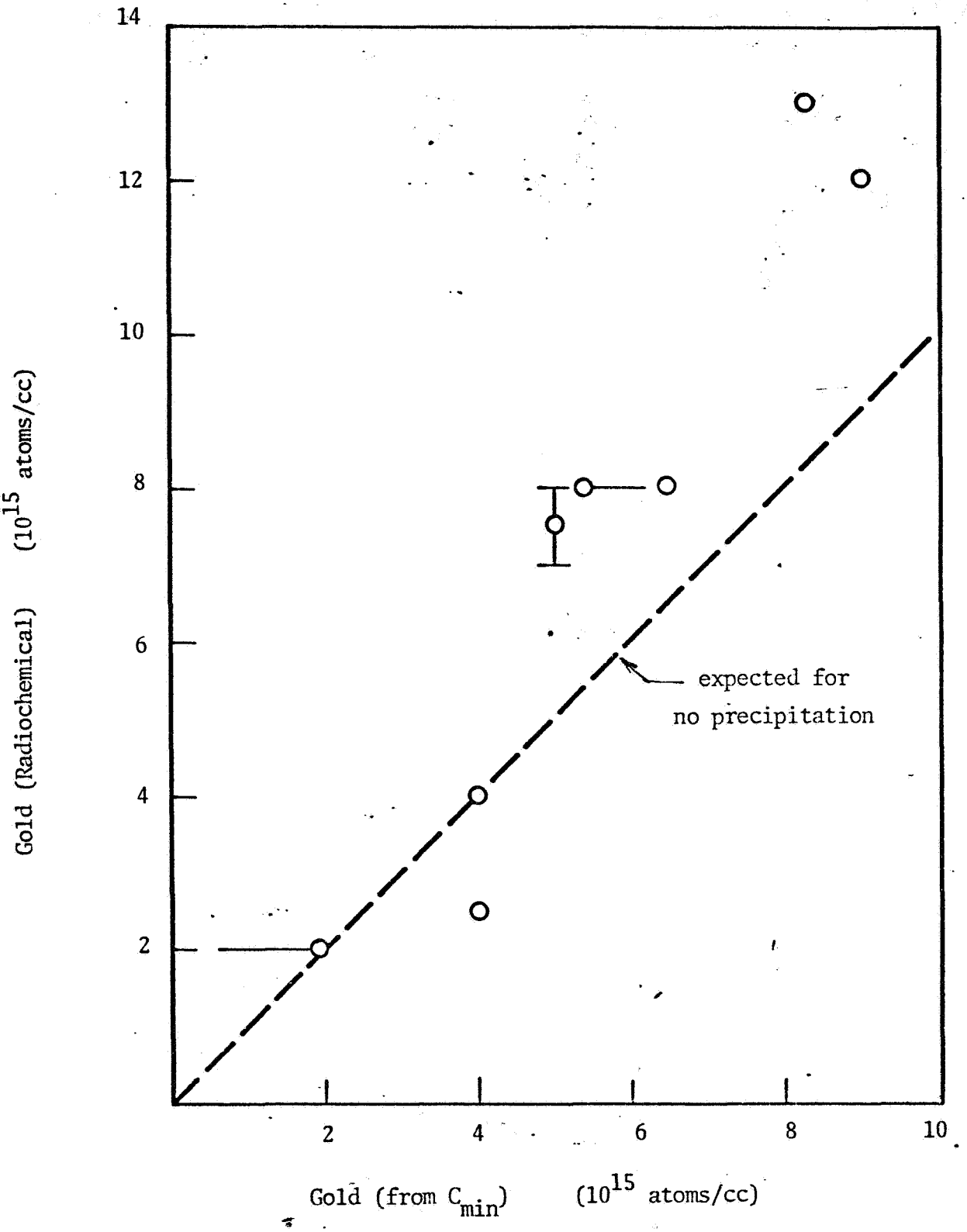

14
12
10
8
6
4
2
Gold (Radiochemical) (10^{15} atoms/cc)
expected for
no precipitation
2
4
6
8
10
Gold (from C_{min}) (10^{15} atoms/cc)

Fig. 16

Gold in Si Measured ~ 1 micron from Surface

1000°C diffusion

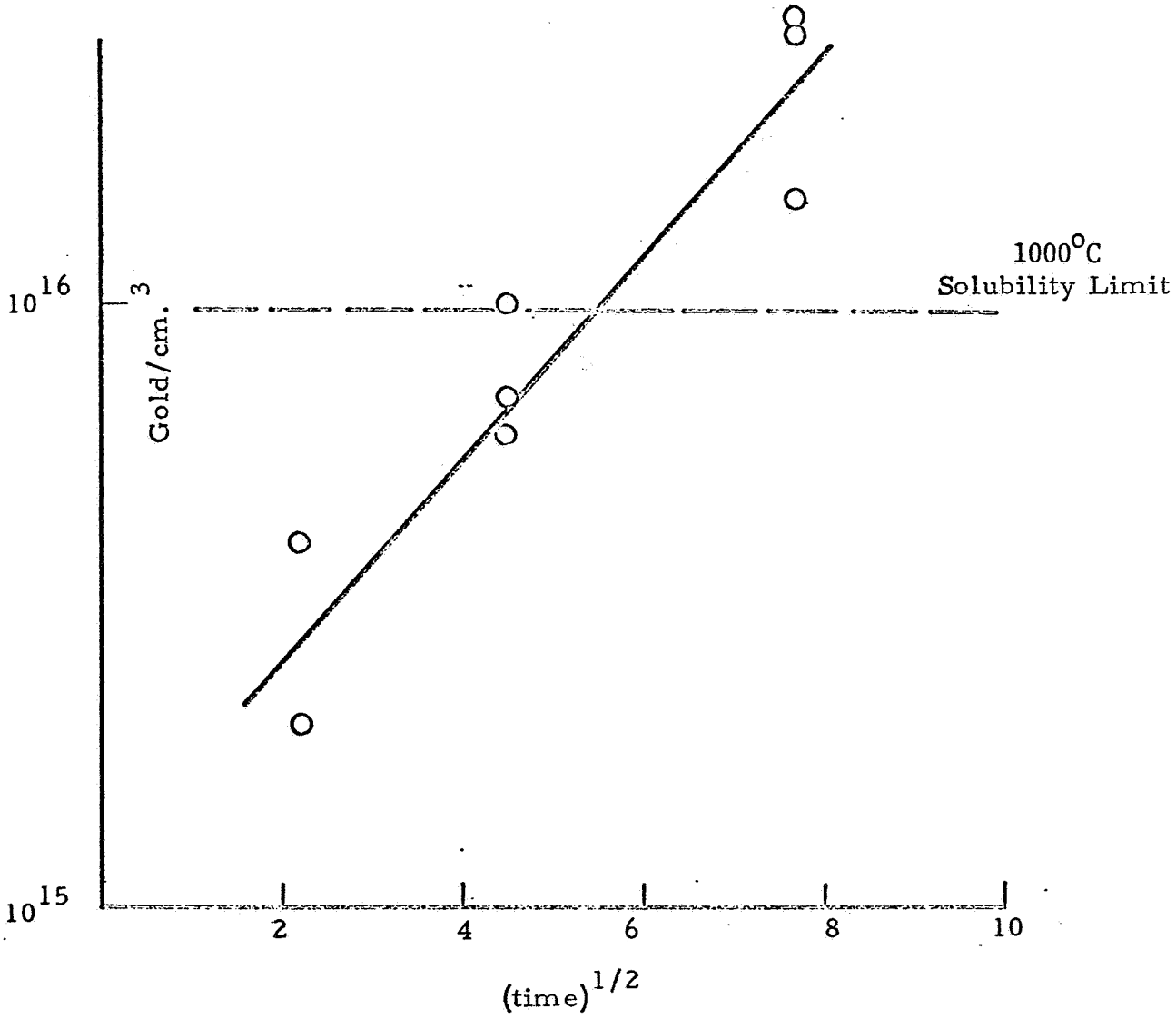


Fig. 17

lifetime vs. gold concentration. A monotonic relation is seen. Lifetimes are longer than expected for amount of gold.[3] This may imply that an excess of gold near the Si/SiO_2 interface affects $-\Delta C_{min}$ more than it affects diode storage-time, or that alloying reduces gold concentration in the vicinity of diode.

Table IV

Storage Time Lifetime	Gold from $-\Delta C_{min}$	Lifetime Expected[3]
520 ns	0	—
395	$0.45 \times 10^{16} cm^{-3}$	11.ns
208	1.2	4.2
43	1.4	3.6

Control samples containing only residual gold were neutron-activated, Si sectioned, and gold counted (Fig.18). One sees there is indeed a spike of gold at the Si/SiO_2 interface.

MOS transient technique uses an abrupt change in dc bias and continuous measurement of differential capacitance. Our circuit[4] is shown in block diagram in Fig. 19 and in detail in Fig. 20. Calibration was done using the Boonton capacitance meter. Output voltage was linearly proportional to capacitance to 75 pf., becoming non-linear due to amplifier saturation. Range was extended by inserting a switched attenuator between the 4.5 mc preamp and amplifier. Circuit was immune to spurious response caused by large pulses during bias switching.

Transient MOS lifetime results were scattered, independent of diffused gold concentrations. Lifetimes were generally an order of magnitude lower than those from diode storage. The explanation for this may be that transient response is controlled by carrier generation at the interface; either from the excess residual gold (Fig. 18) or from interface states.

To investigate interface states, MOS parallel conductance is being measured[5]. An experimental difficulty with conductance measurement of gold-doped samples is that gold compensates bulk Si, raising series resistance of the device. This effect can be corrected for. Measurements and calculations are being done to handle effect of series resistance and oxide capacitance, to obtain C_p and R_p (parallel capacitance and conductance) characteristic of only the interface region.

References

1. S. F. Cagnina and E. H. Snow, J. Electrochem. Soc. 114, 1165 (1967).
2. F. P. Heiman, Trans. IEEE, ED-14, 781 (1967).
3. A. E. Bakanowski and J. H. Forster, Bell Syst. Tech. J. 39, 87 (1960).
4. K. H. Zaininger, RCA Rev. 27, 341 (1966).
5, E. H. Nicollian and A. Goetzberger, Bell Syst. Tech. J. 46, 1055 (1967).

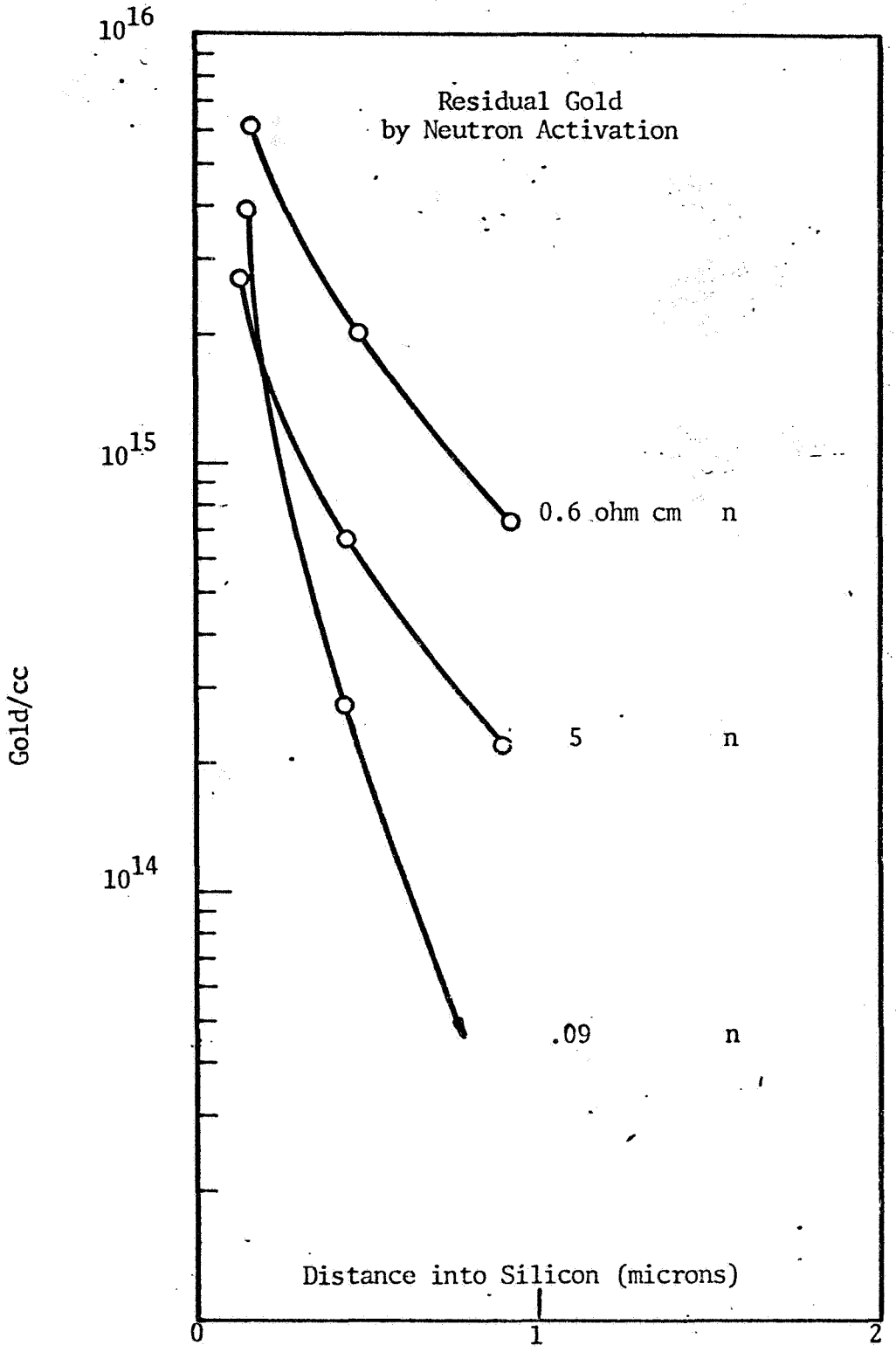
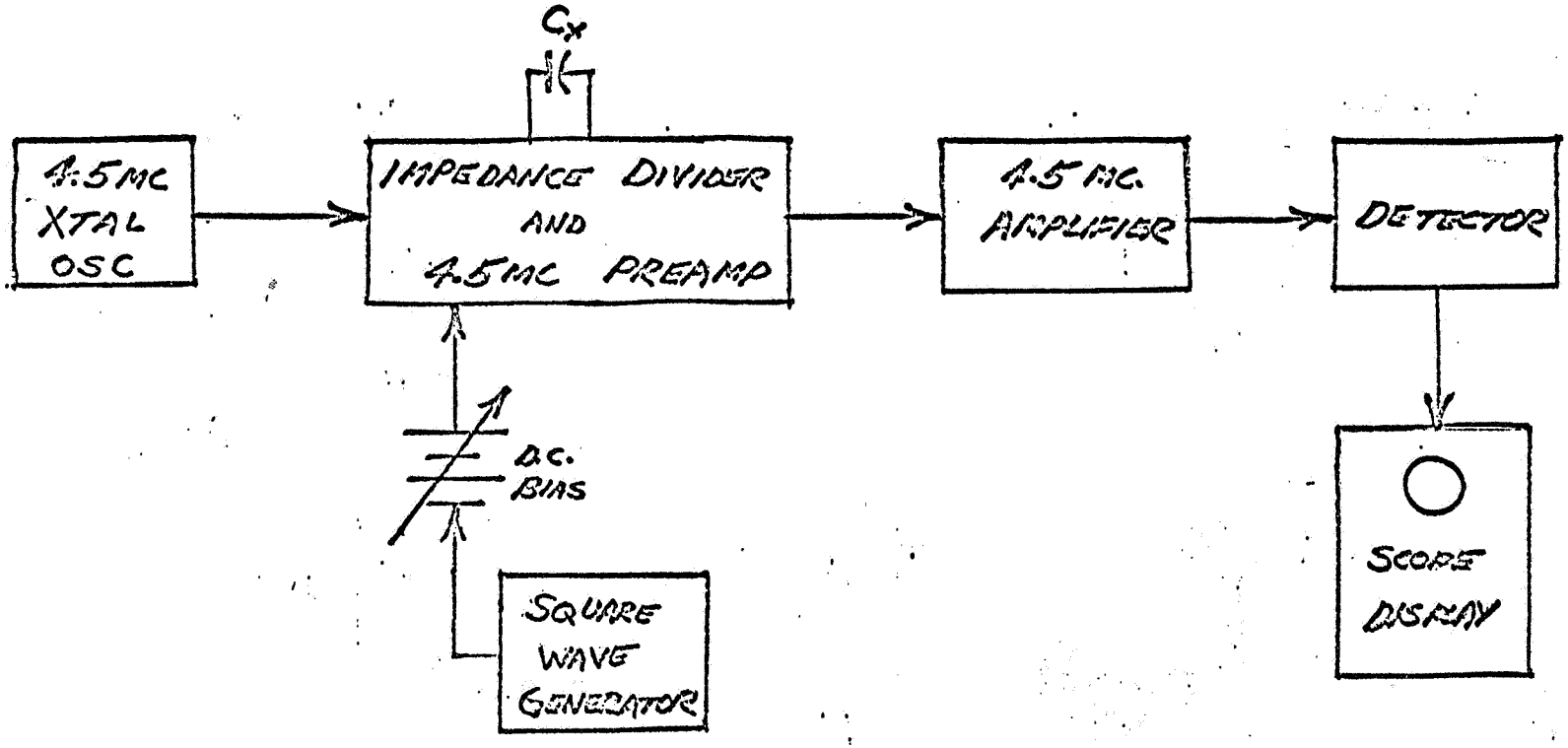
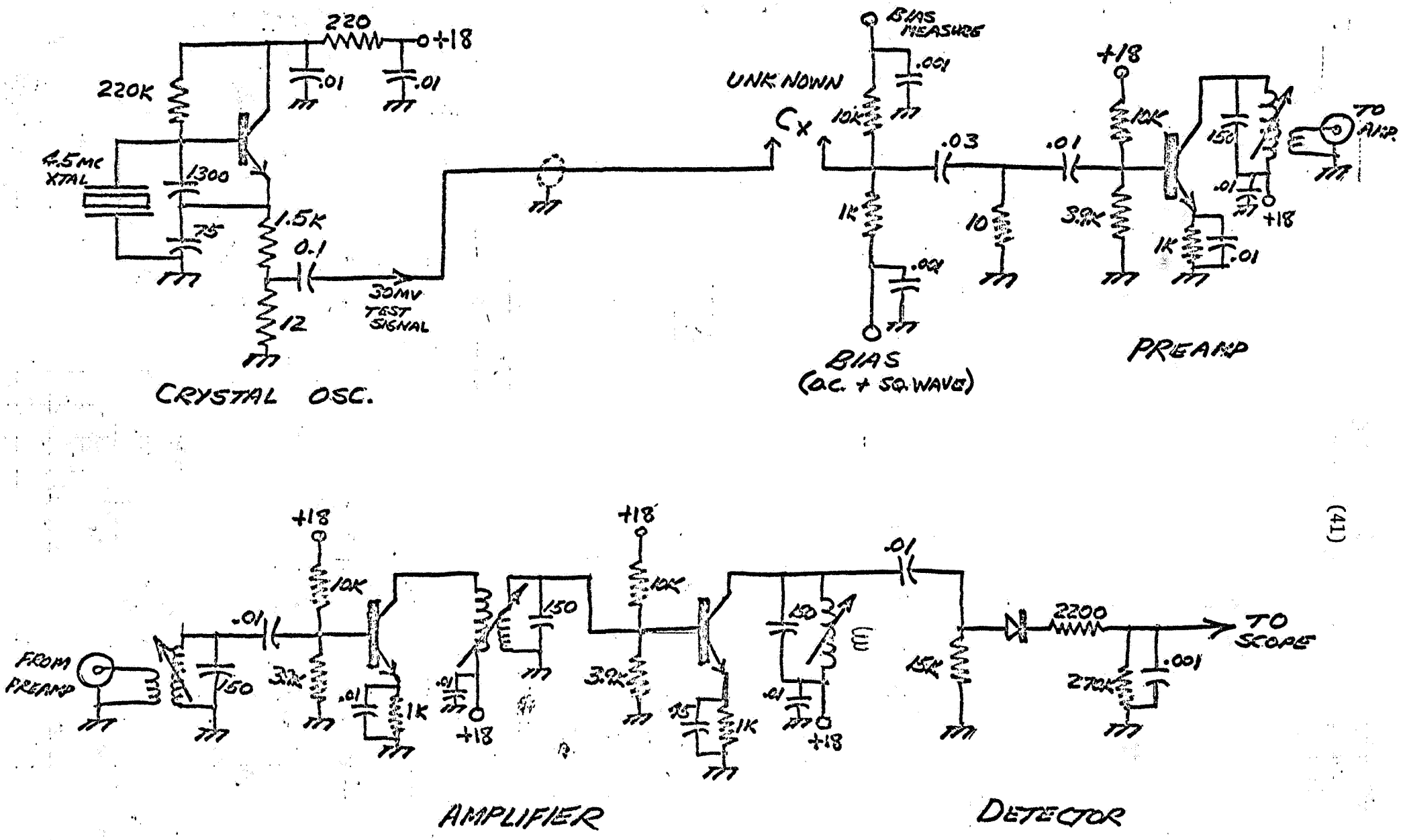

Residual Gold
by Neutron Activation
10^{16}
10^{15}
10^{14}
Gold/cc
0.6 ohm cm n
5 n
.09 n
Distance into Silicon (microns)
0
1
2

Fig. 18



BLOCKS FOR TRANSIENT C(V) MEASUREMENT

Fig. 19



(41)

CIRCUIT FOR TRANSIENT C(V) MEASUREMENT

Fig. 20

Publications and Talks

1. "Interface States in SiO_2/Si MOS at Low Temperature," A. B. Kuper, E. Greenstein, and H. P. Caban-Zeda, J. Electrochemical Soc. 114, 273C (Nov. 1967).

2. "Phosphosilicate Glass Passivation Against Sodium Impurity in Thermal Oxide on Si", W. W. Smith, Jr. and A. B. Kuper, Proc. IEEE Reliability Physics Sixth Annual Symposium, 1967.

3. "Analysis of MOS by Combined Electrical-Radiochemical Technique," A. B. Kuper, Georgia Institute of Technology, Electrical Engineering Seminar, December 4, 1967.

4. "Transient MOS C(V) Effects at 77 K," A. B. Kuper, IEEE-Semiconductor Interface Specialists Conference, Las Vegas, Nevada, March 4, 1968.

5. "Combined MOS and Radiochemical Analysis," A. B. Kuper invited paper, Semiconductor Surface Symposium, American Chemical Society, April 1968. (to be published in "Surface Science")

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	Chester J. Slabinski, M. S., E. E., Case 1968.
Summer Students:	Eugene Greenstein, B. S., E. E., Case 1968.
	James Spreen, Case Undergraduate.

APPENDIX A

PREPARATION OF COUNTING SOLUTION

Order of mixing the ingredients in a CS-3-stabilized solution is quite important, contrary to the statements of the manufacturer. If CS-3 solubilizer is mixed with the xylene-PBD scintillant before mixing with the aqueous component, the solution may develop a very intense and long-lasting phosphorescent background. The following order of preparation is therefore used:

1. Excess of calcium carbonate is measured into the radioactive HF solution to neutralize the acid. This gives stable count-rate later.
2. Three cc of CS-3 are added and vial swirled to mix CS-3 and aqueous component.
3. Xylene-PBD mixture is added to vial, and vial is shaken vigorously. This gives a solution with a good deal of suspended calcium carbonate and calcium chloride.
4. Vial is centrifuged for a few minutes. This settles the suspended material firmly onto the bottom of the counting vial and leaves a clear solution above the precipitate. Solution count-rate is now stable.
5. Background on the samples may go lower if vials are allowed to stand for a few hours between preparation and counting.