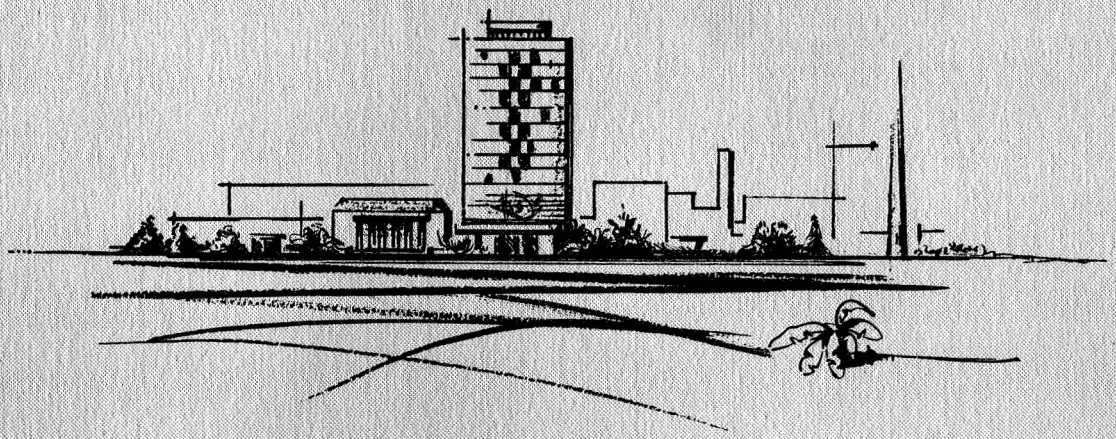
RESEARCH REPORT

A SURVEY OF SEMICONDUCTOR MATERIALS AND PROCESSES FOR THICK-FILM FIELD-EFFECT TRANSISTOR FABRICATION

by

F. W. Duncan, Y. F. Chang and H. C. Carton



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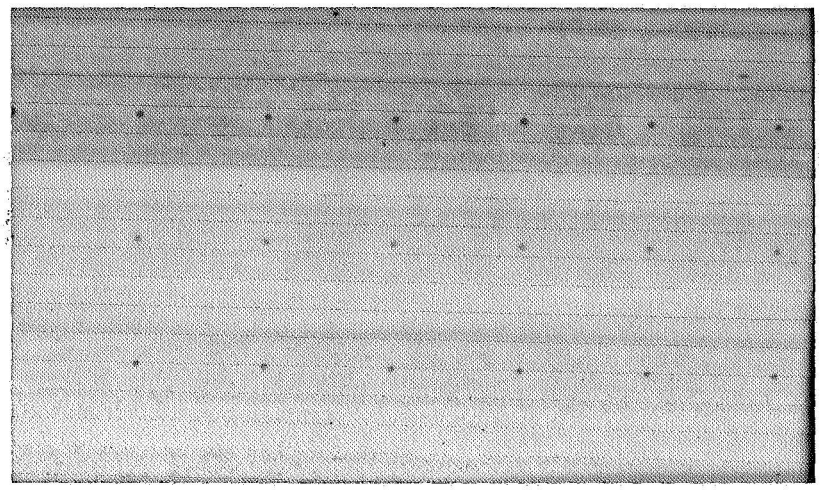

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By F. W. Duncan, Y. F. Chang, and
H. C. Gorton

ABSTRACT

The criteria described in the report were applied to a number of candidate materials (semiconductor, dielectric, and electrode), deposition processes, and device configurations obtained from the TFT literature and elsewhere. On the basis of this analysis, nine specific combinations of materials, processes and configurations appear to have some potential for use in the fabrication of thick-film insultated-gate FET's. These specific combinations or models include staggered, coplanar, and inverted-coplanar structures.

Semiconductor deposition processes include the wet chemical deposition of PbS at room temperature, the pyrolytic deposition of CdS at 210 C, the pyrolytic deposition of Si at 1000 - 1200 C, and the reduction of dielectric $BaTiO_3$ at 900 C to obtain semiconducting $BaTiO_{(3-x)}$. In the nine models SiO_2, $BaTiO_3$, or TiO_2 dielectrics and Au, or Ti electrodes are used with the above semiconductors.

The nine models have been divided into three groups according to their likelihood of successful implementation. The models in Group 1 represent minimal departure from standard thick film technology and are recommended as having reasonable potential for successful development. The models in Group 2 represent a significant but not incompatible departure from thick film technology and include process steps that may require considerable continued

development for successful implementation in a thick film device. Because of an unmodulated component in the source-to-drain resistance, the models in Group 3 are not recommended for implementation.

A SURVEY OF SEMICONDUCTOR MATERIALS AND PROCESSES FOR THICK-FILM FIELD-EFFECT TRANSISTOR FABRICATION

By F. W. Duncan, Jr., Y. F. Chang
and H. C. Gorton

SUMMARY

The purpose of this study is to assess the reasonably available and pertinent literature to determine insofar as practical those materials (semiconductor, dielectric, and electrode), deposition processes, and device configurations which possess the highest potential for the fabrication of thick-film field-effect transistors. All materials and processes selected for further consideration are believed to be identical to or compatible with those used in existing thick-film technology.

An historical sketch of the development of the thin-film field-effect transistor (FET) is presented and two recent attempts at making thick-film FET's are described.

Criteria are presented for the electrical, chemical, physical and mechanical, and metallurgical properties of the semiconductor, dielectric, and electrode materials. Additional criteria deal with the device configuration and thick-film-compatible processes of deposition. Frequent applications of these criteria occur throughout the report.

Equations are presented for the drain current I_D and the transconductance g_m as a function of semiconductor and dielectric properties, device geometry, and applied voltages. The expressions are developed for a thin-film insulated-gate FET and are assumed to apply to the corresponding thick-film device.

The thin-film insulated-gate FET configurations include the staggered, coplanar, inverted-staggered, and inverted-coplanar structures. The use of a polycrystalline semiconductor layer in these configurations makes them appropriate for consideration in the fabrication of thick-film FET's.

A number of semiconductor materials reported in the thin-film transistor (TFT) literature and elsewhere were evaluated on the basis of the materials criteria. The result of this evaluation was the selection

of the following 14 materials for consideration as semiconductor layers in this study:

Si	Ag_2Te	CdS	GaAs	PbS	$BaTiO_{3-x}$
Ge		CdSe	InAs	SnO_2	TiO_{2-x}
Te		CdTe	InSb		

In a similar evaluation of dielectric materials, SiO_2, $BaTiO_3$, TiO_2, and Ta_2O_5 were selected for further consideration as gate insulators. Gold and titanium were selected for further consideration as electrode materials.

A number of processes for the deposition of the semiconductor, dielectric, and electrode layers (excluding vacuum evaporation and sputtering) were evaluated on the basis of the process criteria. The subsequent application of the configuration criteria to the numerous combinations of specific materials, processes, and device configurations resulted in the selection of nine particular combinations (or models) which appear to have some potential for use in the fabrication of thick-film insulated-gate FET's. These nine models include the staggered, coplanar, and inverted-coplanar structures depicted in Figures 5 through 13 and in Table 7.

The semiconductor deposition processes employed in the models include the wet chemical deposition of PbS at room temperature, the pyrolytic deposition of CdS at 210 C, the pyrolytic deposition of silicon at 1000 to 1200 C, and the reduction of dielectric $BaTiO_3$ at 900 C (estimated) to obtain semiconducting $BaTiO_{3-x}$.

SiO_2, $BaTiO_3$, and TiO_2 are employed as dielectrics in the models. The SiO_2 is deposited by anodization at 20 C, pyrolytic decomposition at 850 C (estimated), or thermal oxidation at 900 to 1300 C. The $BaTiO_3$ layers are obtained by printing and firing a thick-film paste at 750 to 1000 C, reoxidation of semiconducting $BaTiO_{3-x}$, or utilization of a $BaTiO_3$ substrate as the dielectric layer. In addition, TiO_2 films are obtained by anodization or thermal oxidation.

One of the electrode materials used in the models is a thick-film gold paste, printed and fired at 750 to 1000 C. The other electrode material

is titanium, bonded to the substrate by the process described for titanium in Reference (51).

The nine models have been divided into three groups according to their likelihood of successful implementation. The models in Group 1 (Figures 9 and 10) represent minimal departure from standard thick film technology and are recommended as having reasonable potential for successful development. The models in Group 2 (Figures 11, 12 and 13) represent a significant but not incompatible departure from thick film technology and include process steps that may require considerable continued development for successful implementation in a thick film device. Because of their sizeable unmodulated component of source-to-drain resistance, the models in Group 3 (Figures 5, 6, 7, and 8) are not recommended for implementation.

INTRODUCTION

The first concept of a field-effect device was given by J. E. Lilienfeld and patents were granted in the years 1930 through 1933.[1] This early invention did not prove workable primarily due to the very low hole mobility in the Cu_2S semiconductor materials.[2]

The first modern-day field-effect device was invented by Shockley[3], who was granted a patent in 1956. The Shockley "unipolar field-effect transistor" is a workable device in which source and drain electrodes make ohmic contact to the ends of a bar of semiconductor material, and a p-n junction is formed on the surface of the bar between the source and drain electrodes. This p-n junction serves as the controlling gate of the device. As a reverse bias is applied to the gate junction, the space-charge region associated with the junction extends into the body of the semiconductor bar. The mode of operation is by depletion of charge carriers. Thus, the width of the conducting channel in the semiconductor bar can be controlled by the gate voltage. The basic principle of modulating the conductivity is also applicable to the newer versions of the field-effect device. The Shockley invention was reduced to practice by Dacey and Ross[4]. It is referred to as the junction- (or channel-) type FET.

The next development in the FET was the use of an insulated gate electrode. Atalla[5] and Kahng[6] were granted patents on the idea of a gate electrode separated from the semiconductor by a thin layer of insulator. The insulator was usually silicon dioxide of approximately 1000 Å thickness. The conductivity of the semiconductor directly beneath the gate electrode is modulated by a capacitive effect. As a voltage is applied across the metal-insulator-semiconductor capacitor, the appropriate charge carriers accumulate on the opposite plate of the capacitor. If the charge carriers accumulating at the semiconductor surface are the minority carriers, majority carriers will be repelled, and the conductivity of the semiconductor will be reduced. This is the same as the depletion mode of operation in the channel-type FET. In the enhancement mode of operation, the metal-insulator-semiconductor capacitor is charged such that majority carriers accumulate at the semiconductor surface. Thus, the conductivity of the semiconductor is increased.

With the advent of the insulated-gate version FET, the device has become much more versatile. The possibility of operation in the enhancement mode as well as in the depletion mode advanced the development of the field-effect device. It was soon discovered that there was not a necessity for using single-crystal semiconductor materials in the device. In 1962, Weimer[7] reported an FET made from a thin film of polycrystalline cadmium sulfide. All the components of the thin-film transistor (TFT) can be fabricated entirely by vacuum evaporation. Aside from the consideration of adherence between each adjacent layer, it is required that the source and drain electrodes form ohmic contacts to the semiconductor and that the insulator film does not contain pin holes.

The above thin-film work demonstrated the occurrence of a field effect in a polycrystalline semiconductor layer deposited by vacuum evaporation. Thus, the deposition of a polycrystalline semiconductor layer by a thick-film-compatible process might be expected to lead to the development of a thick-film insulated-gate FET.

Thick-film techniques for the deposition of passive components, such as thick-film resistors and capacitors, have been used for many years.

Passive networks prepared by screen printing and firing have been combined with prefabricated active components to produce microminiaturized hybrid circuits. Also, extensive research has been carried out on the deposition of semiconducting materials such as CdS by screen printing and firing for the purpose of fabricating CdS photocells. These CdS photocells have been developed to a high degree of perfection and are commercially available.[8]

Y. T. Sihvonen and his coworkers at Texas Instruments performed an exploratory investigation of materials, processes, and configurations suitable for a printable insulated-gate FET.[9] They produced a number of operational devices using a semiconductor layer of sintered CdS-CdSe in conjunction with various dielectrics. The better devices used dielectric films of nitrocellulose (Duco cement), silicate cement (Sauereisen), and glyceryl monostearate. In addition, devices of comparable quality employed a $BaTiO_3$ substrate as the dielectric "layer". The electrode materials were either metallic paints or low-melting alloys applied at or near room temperature.

Some of the devices had higher transconductance ($\leq$2000 μmho) coupled with poor frequency response ($<$100 Hz), while others had lower transconductance ($\leq$20 μmho) coupled with better frequency response ($>$100 Hz). Considerable development is still required, however, to improve stability and raise the performance level to that of the thin-film FET.

Witt, Huber, and Laznovsky at RCA have made operational insulated-gate FET's with a mixture of thick- and thin-film layers.[8] The thick-film (or thick-film-compatible) layers included a screen-printed and fired CdS semiconductor and pyrolytically deposited SiO_2 dielectric. Thin-film source, drain, and gate electrodes were deposited by vacuum evaporation. These devices had transconductance values on the order of 1000 μmho and exhibited drain current saturation.

Subsequent attempts by the same researchers to fabricate an all thick-film insulated-gate FET were not successful.[10] The following problems were revealed in this work:

(a) Damage to other FET layers by the corrosive chlorine vapors released from the CdS flux during firing.

(b) Degradation of the CdS semiconductor layer during firing by migrant impurities from other thick-film layers (such as the gold electrodes).

If thick-film FET's could be fabricated by processes compatible with the printing and firing process of thick-film technology, then thick-film integrated circuits could be realized. Such circuits, although larger in size than the silicon integrated circuits, have their own place in the total spectrum of electronic applications. The advantages of thick-film integrated circuits over silicon integrated circuits include lower unit cost for small production quantities, greater flexibility in accommodating design changes, and reduced parasitic coupling among active devices on the same substrate.

The purpose of this study is to establish the relative potential of candidate materials, processes, and configurations, reported in the TFT literature and elsewhere, for use in the fabrication of thick-film FET's.

DISCUSSION OF CRITERIA

A large amount of information on potential materials, processes, and configurations for the fabrication of thick-film field-effect transistors had to be evaluated in this study. A list of the criteria used in the evaluation is presented in the following sections. These criteria will be discussed as their application to the various materials, processes, and configurations arises throughout the body of the report.

The following notation is used in the listing of the criteria:

μ = charge carrier mobility

n = charge carrier density

E_g = bandgap energy

TFT = thin film transistor

g_m = FET transconductance

I_D = FET drain current

K = dielectric constant (relative permittivity)

t = thickness of dielectric layer

ρ = electrical resistivity

Materials Criteria

(I) Electrical Properties

(a) Semiconductor

(1) μ (field effect) > 0

(2) $10^{13} < n < 10^{18}/cm^3$*

(3) 0.18 (InSb) $\leq E_g \leq$ 2.4 eV (CdS)*

(4) Operation as a TFT with $g_m > 0$ and I_D saturation preferable**

(5) Sufficiently low density of traps associated with the semiconductor-dielectric interface to permit modulation of the source-to-drain conductivity by the transverse electric field imposed by a reasonable gate potential

(6) Low resistance ohmic contact of source and drain electrodes to the semiconductor

(b) Dielectric

(1) $K/t > 10^5$/cm (or 10/micron)

(2) E (breakdown) > 10^5 V/cm

(3) $\rho > 10^6$ Ω-cm

(4) Sufficiently low density of traps associated with the semiconductor-dielectric interface to permit modulation of the source-to-drain conductivity by the transverse electric field imposed by a reasonable gate potential

(c) Electrodes

(1) $\rho <$ (50-100) $\mu\Omega$-cm

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*These "criteria" are not rigid, but represent the ranges of values reported in the TFT literature.

**Not a rigid requirement.

(2) Low resistance ohmic contact of source and drain electrodes to the semiconductor

(II) Physical and Mechanical Properties

(a) Good adhesion of adjacent layers

(b) Reasonably matched linear expansivities

(c) Uniform thickness, free of pinholes and volds (primarily for the dielectric)

(III) Chemical and Metallurgical Properties

(a) Low reactivity with environmental water vapor and oxygen at operating temperatures ($\approx$ 0 - 100 C)

(b) Low chemical and metallurgical reactivity at the interfaces at operating temperatures ($\approx$ 0 - 100 C)

(c) Chemical and metallurgical compatibility of adjacent materials during processing

Processing Criteria

(I) Thick-film process, or a process compatible with thick-film technology

(II) No vacuum evaporation or sputtering (preferable)

(III) Chemical and metallurgical compatibility of adjacent materials during processing

Configuration Criteria

(I) An FET configuration for which a sequence of processing steps exists with:

(a) Low degradation of initial FET layers by deposition of subsequent FET layers

(b) Low degradation of other thick-film components on the same substrate by FET processing

(II) An FET configuration which will minimize the unmodulated component of source-to-drain resistance in the semiconductor layer

DISCUSSION OF DEVICE DESIGN AND OPERATION

Theory of FET Operation

The physical phenomenon governing the operation of an insulated-gate field-effect transistor is fundamental and relatively simple to analyze. Borkan and Weimer[11] and Sah[12] have written papers on this analysis. The major assumptions in the analysis are as follows. Only majority carriers are assumed to exist in the semiconductor. The semiconductor layer is assumed to be homogeneous and thin compared with the insulator layer. The carrier mobility in the semiconductor layer is constant, and the source and drain contacts are ohmic. There is also an implicit assumption that the electric field is perpendicular to the surface of the semiconductor. This is the "gradual approximation" introduced by Shockley[3]. The electric field can be perpendicular to the surface of the semiconductor only if the drain-to-source electric field is small. This condition is not satisfied under operating conditions particularly when the drain current has reached saturation.

The electrical characteristics of a typical FET are shown in Figure 1. The device is operating in the enhancement mode, where majority carriers are accumulated in the semiconductor by action of the gate voltage across the gate-semiconductor capacitor. In the simple theory, expressions are derived for the drain current and for the mutual transconductance.

Assuming that the "gradual approximation" is valid, the voltage across the gate-semiconductor capacitor is given by

$$V_{cap} = V_G - V(x), \tag{1}$$

where V_G is the gate voltage referred to the source contact, and $V(x)$ is the voltage on the semiconductor also referred to the source potential. A drawing of the device structure is shown in Figure 2.

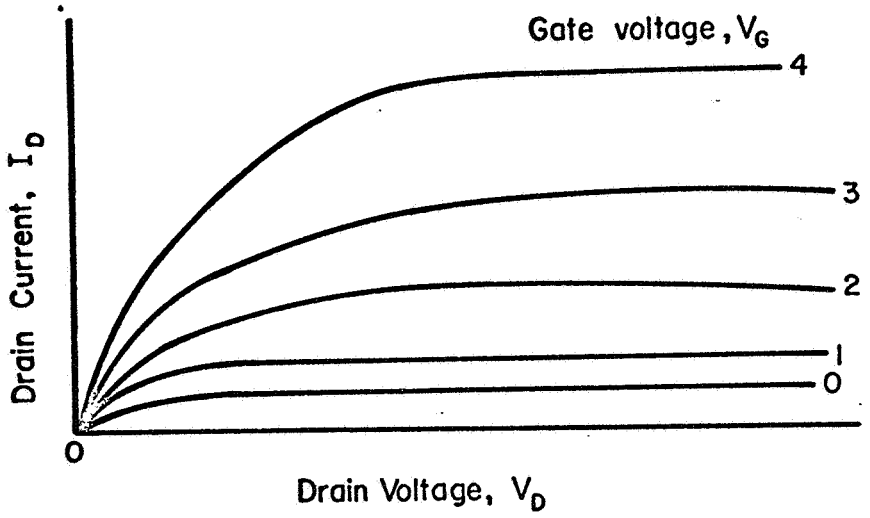


FIGURE 1. TYPICAL FIELD-EFFECT TRANSISTOR CHARACTERISTICS (ENHANCEMENT MODE)

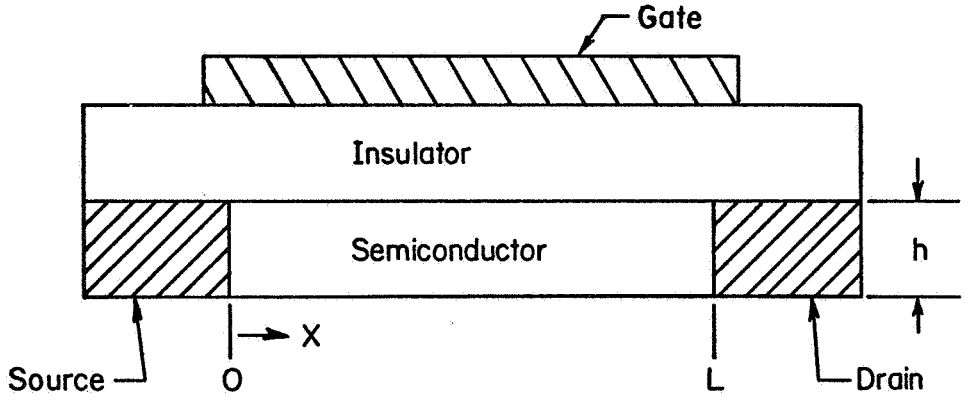


FIGURE 2. FET DEVICE STRUCTURE USED FOR ANALYSIS

The added charge accumulating on the plates of the capacitor per unit area will be

$$\Delta n(x) = \frac{C_G}{qWL}\left[V_G - V(x)\right], \tag{2}$$

where $\Delta n(x)$ is the charge per unit area, C_G is the capacitance of the gate-semiconductor capacitor, L is the source-to-drain spacing, W is the width of the device--i.e., the length of the source and drain contacts--, and q is the electronic charge.

The added charge carriers modulate the conductivity of the semiconductor, which becomes

$$\sigma(x) = q\mu \left[n_o + \frac{\Delta n(x)}{h} \right] , \tag{3}$$

where $\sigma(x)$ is the local conductivity, μ is the charge carrier mobility, n_o is the equilibrium carrier concentration, and h is the thickness of the semiconductor. The drain current is given by the product of the local conductivity and local electric field

$$I_D = hW\sigma(x)\ E(x) = hW\sigma(x)\ \frac{dV(x)}{dx} , \tag{4}$$

where $E(x)$ is the local electric field. After performing the appropriate substitutions, the following integral is obtained.

$$I_D \int^{L} dx = \frac{\mu C_G}{L} \int^{V_D} \left[\frac{qWLhn_o}{C_G} + V_G - V(x) \right] dV(x). \tag{5}$$

The quantity $qWLhn_o/C_G$ is a threshold voltage, the minimum voltage necessary on the gate to turn on the drain current. Therefore, it can be replaced by $-V_t$.

The simple integrations in Equation (5) yield the result

$$I_D = \frac{\mu C_G}{L^2} \left[(V_G - V_t)\ V_D - \frac{V_D^2}{2} \right] , \tag{6}$$

where V_D is the drain voltage. This is the simple theoretical expression for the drain current as a function of the gate-semiconductor capacitance, the threshold voltage V_t, and the gate and drain voltages. It will be used to derive an expression for the mutual transconductance of the device.

When the drain current is saturated at constant gate voltage, $(\partial I_D/\partial V_D)_{V_G} = 0$, or $V_G - V_t - V_D = 0$. Under this condition, a saturation drain voltage is defined as $V_D(sat) = V_G - V_t$. As a result, the saturation drain current is given by

$$I_D(sat) = \frac{\mu C_G V_D^2(sat)}{2L^2}, \text{ or } \frac{\mu C_G}{2L^2}(V_G - V_t)^2 \quad . \tag{7}$$

The mutual transconductance of the device at drain voltages above saturation is defined by the condition $g_m = (\partial I_D(sat)/\partial V_G)V_D$. The result is simply

$$g_m = \frac{\mu C_G}{L^2}(V_G - V_t) \quad . \tag{8}$$

It is evident from this expression that certain device design features should be considered. In order to obtain devices with high values of g_m, the carrier mobility and the gate-semiconductor capacitance should be large, and the Source-to-drain spacing and the threshold voltage should be small. A small threshold voltage can be obtained with small semiconductor volume and low equilibrium carrier density. Thus, the source-to-drain spacing and the carrier density are found to be most critical for an FET of high gain.

From the materials standpoint, the most desirable semiconductor is one with low equilibrium carrier concentration and high carrier mobility. From a fabrication standpoint, the device needs to be small, and of particular importance is the source-drain spacing.

Some modifications and additions have been made to the simple theory. The most important analysis is one made by Geurst[13], where the "gradual approximation" was not used. Among other things, he found that the saturation resistance of an FET, where the drain current does not saturate but increases slowly with drain voltage, is inversely proportional to the ratio h_{ins}/L. In this relation, h_{ins} is the thickness of the insulator layer (which has been defined in this report as t), and L is the source-to-drain spacing.

FET Configurations

The two basic types of field-effect transistors are the junction (or channel) FET and the insulated-gate FET. The junction FET uses single-crystalline bulk semiconductor material. One form of the insulated-gate FET (or IGFET) also uses single-crystalline bulk semiconductor material, while the other form of IGFET consists of a structure of thin film layers (usually polycrystalline).

The common configurations for the thin film IGFET or(TFT) are shown in Figure 3. They include the staggered, coplanar, inverted-staggered, and inverted-coplanar structures.

In identifying materials and processes suitable for the fabrication of a thick-film FET, attention will be focused on these four configurations. Related configurations in which the substrate contains the dielectric or semiconductor layer will also be investigated.

Thin Film Transistor Interfaces.-- The eight relevant interfaces arising in the basis TFT configurations are indicated in Table 1.

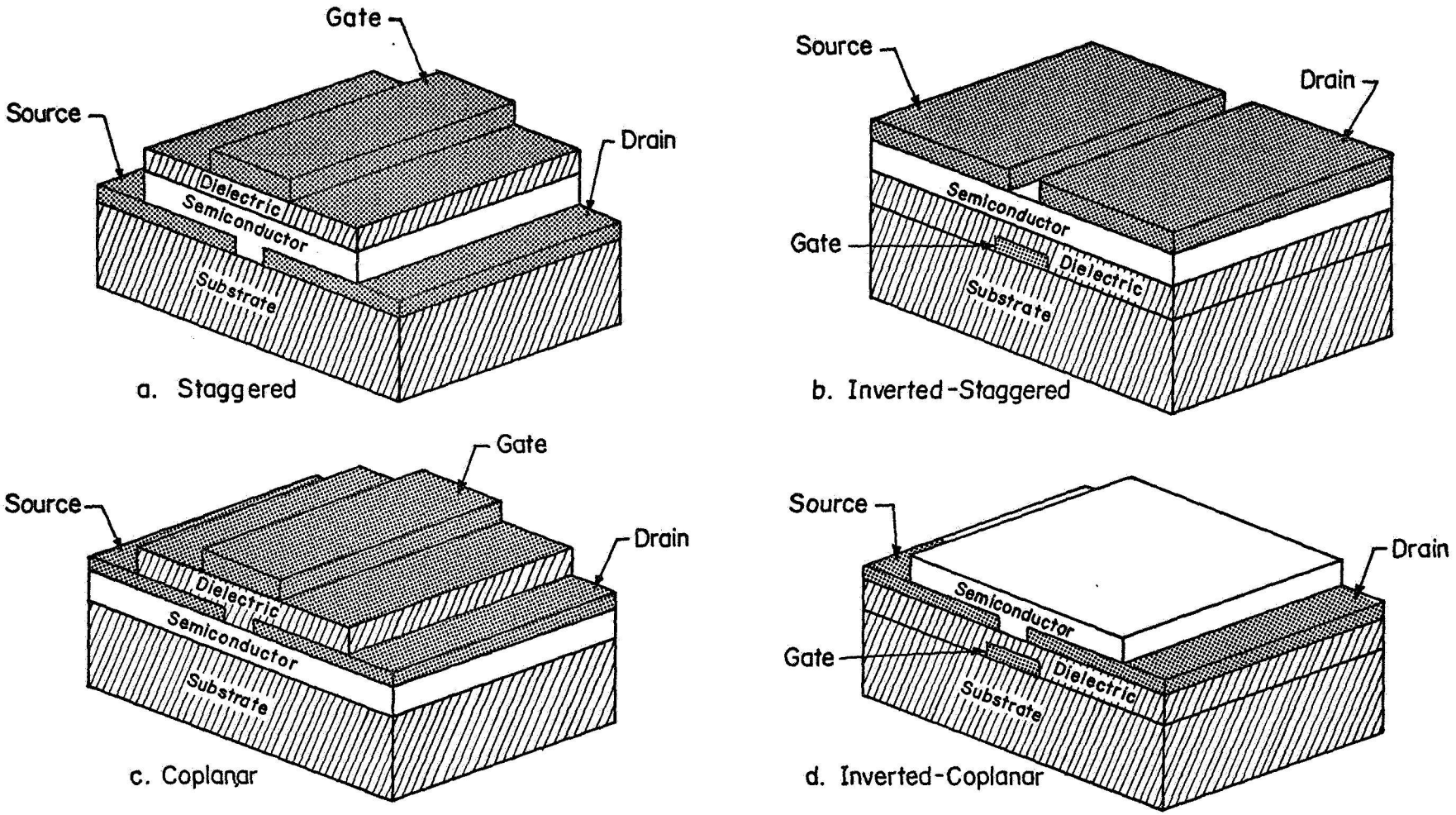
TABLE 1. THIN FILM TRANSISTOR INTERFACES

	Substrate	Source & Drain Electrodes	Semiconductor	Dielectric
Gate Electrode	S_I, C_I*			S, C
Dielectric	S_I, C_I	C	S, C	
Semiconductor	S, C	S, C		
Source & Drain Electrodes	S			

* S - staggered configuration

C - coplanar configuration

S_I, C_I - inverted configurations



Note: All layers are usually polycrystalline

FIGURE 3. COMMON THIN FILM TRANSISTOR CONFIGURATIONS

The following requirements apply to each of the above interfaces:

(1) Good adhesion

(2) Reasonably matched linear expansivities

(3) Chemical and metallurgical compatibility of adjacent materials during processing

  (a) For example, avoid doping semiconductor at semiconductor-substrate interface to obtain high-conductivity surface channel.

(4) Low chemical and metallurgical reactivity at operating temperature ($\approx$ 0-100 C).

In addition, the following electrical requirements apply at the semiconductor-dielectric interface and the semiconductor-electrode interfaces:

(1) Sufficiently low density of traps associated with the semiconductor-dielectric interface to permit modulation of the source-to-drain conductivity by the transverse electric field imposed by a reasonable gate potential

(2)

DISCUSSION OF DEVICE MATERIALS

Semiconductors

Semiconductors Selected for Study.-- Table 2 lists all the semiconductor materials that were considered in this study. The materials in the table are divided into two groups: the elemental semiconductors and the compound semiconductors. Within each group, the materials are ordered on the basis of their position in the periodic table. Attention is limited to semiconductors deposited as polycrystalline films.

TABLE 2. LIST OF SEMICONDUCTOR MATERIALS AND PERTINENT PROPERTIES

Thin Film Semiconductor Material	Group in Periodic Table	ρ, Ω-cm	n, cm^{-3}	μ,[a] cm^2/V-sec	Remarks[b] on performance in a thin-film IGFET	Reference
B	III				Amorphous semiconductor film[c]. Apparently no field effect.	(14)
Si	IV	500	$\approx 1.7 \times 10^{15}$ (calc.)[d]	5-10 (effective)	p-type film; field effect observed ($g_m > 0$), pinch-off occurred (not complete)	(15)
					$g_m \approx 100$ μmho, incomplete pinch-off	(16)
Ge	IV				p-type layer 300 Å thick, field effect ($g_m > 0$); pinch-off for lower magnitudes of gate voltage	(17)
Se	VI	10^3-10^{10} (questionable)		0.7	$25 < g_m < 200$ μmho, (p-type) no pinch-off	(18)

Notes: (a) The mobility values reported in the literature were usually referred to as effective mobilities, field effect mobilities, Hall mobilities, or film mobilities. The effective mobilities and the field-effect mobilities are believed to have been calculated by the various authors from equation (8), rearranged to give μ as a function of (measured values of) g_m, L, C_G, V_G, and V_t. The Hall mobilities and film mobilities are believed to be Hall effect values for thin films. Where reported, the type of mobility is indicated in parenthesis after each mobility value listed in the table.

(b) Semiconductor film prepared by vacuum evaporation unless otherwise specified. Films are all polycrystalline.

(c) Results of a short, initial investigation by Melpar. Most of these materials were studied for potential TFT operation at high temperatures (up to 500 C). Resistance to radiation damage was also a consideration.

(d) Calculated values of ρ, n, and μ assume $\rho = \frac{1}{ne\mu}$ for majority carriers.

Thin Film Semiconductor Material	Group in Periodic Table	ρ, Ω-cm	n, cm^{-3}	μ,[a] cm^2/V-sec	Remarks[b] on performance in a thin-film IGFET	Reference
Te	VI	few tenths	$\approx 3 \times 10^{17}$ (calc.)[d]	> 200 (effective)	Well saturated enhancement characteristics, g_m up to 40,000 μmho, p-type, 150 Å thick	(19)
					Possible Te health and contamination hazard	(20)
					200-300 Å thick, good g_m and pinch-off	(21)
					g_m >1000 μmho, V(pinch-off) >1 V on quartz substrate	(16)
					$g_m \approx$ 22,000 μmho on sapphire substrate	(22)
Ag_2Te	I-VI			$\leq$ 400 (film)	Field effect (for 500 Å film), some I_D saturation at lower V_G	(23)
BaO	II-VI				No acceptable film[c]	(14)
CdS	II-VI	100-7900 (questionable)		0.03-5.7 (effective)	Field effect (g_m >0), pinch-off (some units)	(24)
					g_m = 4000 μmho (typical) g_m up to 25,000 μmho, good pinch-off	(25)
				$\approx$ 5 (Hall)	g_m up to 25,000 μmho g_m > 10,000 μmho	(26)
					Screen-printed CdS about .001 inch thick, g_m = several hundred μmho, good I_D saturation	(27)

Thin Film Semiconductor Material	Group in Periodic Table	ρ, Ω-cm	n, cm^{-3}	μ,[a] cm^2/V-sec	Remarks[b] on performance in a thin-film IGFET	Reference
CdS (cont.)		10^4 - 10^5			Screen printed CdS about 3μ thick with pyrolytically deposited SiO_2 dielectric about 0.2μ thick, $g_m \leq 1000$ μmho, good I_D saturation.	(8)
				0.1 - 150 (effective)	IBM, commenting on work of others	(25)
		2.6×10^4	3×10^{13}	42.5 (film)	Film suitable for TFT	(28)
		10^5 (film) 10^5-10^2 (with SiO dielectric)			TFT[e]	(20)
					TFT[e]	(21)
					TFT[e]	(16)
					TFT[e]	(17)
CdSe	II-VI			4-30 (film)	TFT[e], g_m >10,000 μmho	(29)
		>20 (enhancement mode)			TFT[e] (improved stability with Al_2O_3)	(30)
					TFT[e]	(31)

(e) In this table, the term TFT implies both field effect ($g_m > 0$) and I_D saturation.

Thin Film Semiconductor Material	Group in Periodic Table	ρ, Ω-cm	n, cm^{-3}	μ,[a] cm^2/V-Sec	Remarks[b] on performance in a thin-film IGFET	Reference
CdSe (cont.)					TFT[e]	(32)
					TFT[e]	(33)
					TFT[e],	(20)
					TFT[e]	(23)
					TFT[e]	(16)
					TFT[e]	(17)
CdS-CdSe	II-VI				Electrodes and gate insulator applied at room temperature. Printed and fired semiconductor, field effect, no I_D saturation at higher frequencies. $g_m \leq 2000$ μmho.	(9)
					TFT[e], $g_m \approx 200$ μmho, I_D saturation	(20)
CdTe	II-VI				Field effect, less flat I_D saturation at higher V_G.	(17)
CoS	II-VI				Film, apparently no field effect[c]	(14)

Thin Film Semiconductor Material	Group in Periodic Table	ρ, Ω-cm	n, cm^{-3}	μ,[a] cm^2/V-sec	Remarks[b] on performance in a thin-film IGFET	Reference
PdO	II-VI	≈ 0.1		≈ 17	No thin film IGFET attempts reported. $E_g \approx 1.5$ eV, 3000 Å film grown on Pd surface in O_2 at 700 C for 24 hours	(34)
ZnO	II-VI				Film, no field effect[c]	(14)
ZnS	II-VI				No thin-film IGFET attempts reported	
ZnS-CdS	II-VI				TFT[e] (operation up to 350 C)	(16)
ZnTe	II-VI				Field effect; no I_D saturation	(16)
GaAs	III-V				TFT[e], polycrystalline p-type material, g_m = 5-20 μmho, I_D saturation	(35)
InAs	III-V	0.026 (calc.)[d]	8×10^{16}	3000 (field effect)	TFT[e] (depletion mode, V_G = 4.5 V for pinch-off)	(36)
				$\leq$ 1800 (field effect)	TFT[e], g_m = 10,000 μmho, I_D saturation at lower V_G	(37)
					TFT[e] (less flat I_D, saturation at higher $\lvert V_G \rvert$)	(17)
InSb	III-V	0.03	3.7×10^{17}	560 (film)	n-type (better than p-type), g_m = 2500 μmho, field effect, incomplete I_D saturation.	(38)
		≈ 0.06 (calc.)[d]	$10^{16} - 10^{17}$	$10^3 - 10^4$ (film)	Field effect observed	(39)
		0.03	5×10^{17}	≈ 600 (film)	g_m up to 3000 μmho, field effect, incomplete I_D saturation.	(32)

Thin Film Semiconductor Material	Group in Periodic Table	ρ, Ω-cm	n, cm^{-3}	μ,[a] cm^2/V-sec	Remarks[b] on performance in a thin-film IGFET	Reference
Gd_2Se_3	III-VI				No field effect in thin film[c]	(8)
SiC	IV-IV				Sensitivity very low but field effect evident (n-type)	(16)
PbS	IV-VI	$\geq$ 0.024 (questionable); (calc.)[d]	$\leq 10^{18}$ (questionable)	$\leq$ 260 (effective)	$g_m \approx$ 1500 μmho, incomplete I_D saturation, field effect (quite crude I_D vs V_D characteristic)	(40)
					Field effect, no I_D saturation (fair sensitivity)	(16)
PbTe	IV-VI				Field effect, no I_D saturation	(23)
SnO_2	IV-VI			$\leq$ 70 (film)	Field effect (g_m = 300 μmho)	(41)
					Time degradation, initial g_m = 3000 μmho, field effect, no I_D saturation	(16)
SnS	IV-VI			< 1 (film)	Very little field effect[c]	(23)
$TiO_{(2-x)}$	IV-VI				No thin film IGFET attempts reported. (TiO_2 dielectric can be reduced to obtain a semiconductor)	
Bi_2Se_3	V-VI				Field effect, no I_D saturation	(23)
Bi_2Te_3	V-VI				Some field effect (questionable)	(23)

Thin Film Semiconductor Material	Group in Periodic Table	ρ, Ω-cm	n, cm^{-3}	μ,[a] cm^2/V-sec	Remarks[b] on performance in a thin-film IGFET	Reference
$MoTe_3$	VI-VI				No field effect[c]	(20)
WS_3, WSe_3	VI-VI				Almost no field effect in thin films[c]	(20)
$MnSi_2$	VII-IV				Film, no field effect[c]	(14)
MnO_2	VII-VI				No thin film IGFET attempts reported. (Used as counterelectrode material in solid electrolytic Ta capacitors)	(42)
MnSe	VII-VI				Field effect, no I_D saturation	(23)
MnTe	VII-VI			≤ 40	Field effect, no I_D saturation	(23)
$BaTiO_{(3-x)}$					No thin film IGFET attempts reported. (Existence of reduced titanate technology in capacitor manufacturing)	(43)
Semiconductor Glasses					No thin film IGFET attempts reported. (Apparent compatibility with thick film technology)	

For each semiconductor material, the table indicates the electrical resistivity, carrier concentration, mobility and remarks on TFT performance, where reported.

Various terms have been used in the "Remarks" column of Table 2 to describe the degree of drain current I_D saturation. These terms are defined in Figure 4. In many of the TFT papers reviewed, the term "pinch-off" is used to mean drain current saturation.

No TFT's using a ZnS semiconductor layer (by itself) were reported in the literature reviewed for this report.

PdO was considered because of the possibility of its being grown on existing Pd-bearing, thick-film, conductive or resistive pastes in a firing operation.[34]

$BaTiO_{(3-x)}$ semiconductor was considered in view of the existence of the reduced titanate capacitor technology.[43] In this technology dielectric $BaTiO_3$ is reduced to obtain semiconducting $BaTiO_{(3-x)}$. The use of this procedure to obtain a semiconductor-dielectric interface might be applicable in the fabrication of a thick film IGFET. Similar processes exist for reducing the dielectric TiO_2 to obtain semiconducting $TiO_{(2-x)}$. The nonferroelectric nature of TiO_2 may make it preferable to $BaTiO_3$ in a thick-film TFT.[10]

MnO_2 is of interest because of its use as a counterelectrode in solid electrolytic tantalum capacitors.[42] The adjacent layers of tantalum, Ta_2O_5, and MnO_2 in these capacitors bear a close resemblance to the adjacent layers of gate electrode, gate insulator, and semiconductor in the inverted-staggered TFT configuration. Finally, semiconductor glasses are of interest because of their potential compatibility with thick-film processing.

Application of Semiconductor Material Criteria.-- The material criteria for the semiconductor layer are the following:

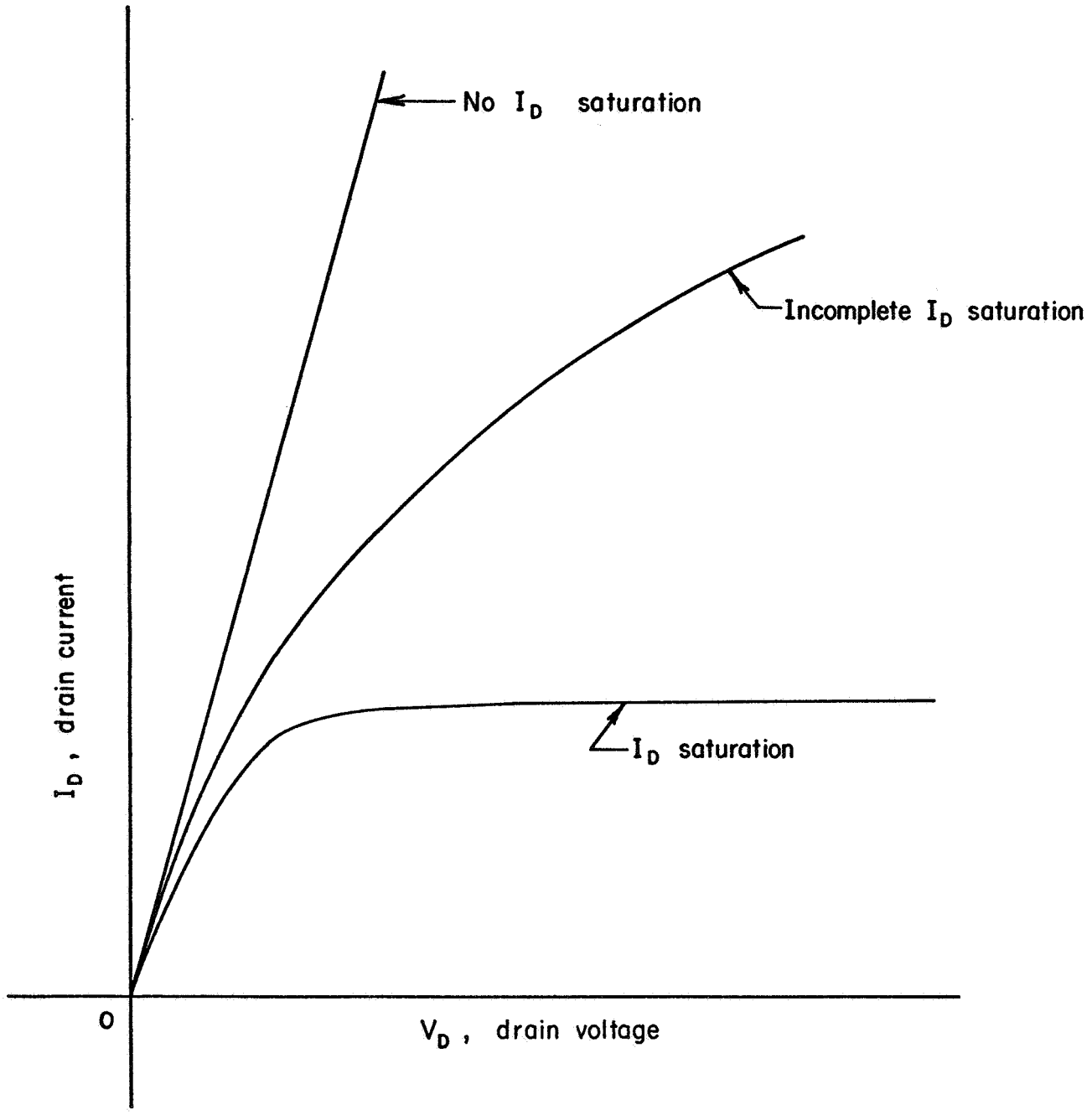


FIGURE 4. DEGREES OF DRAIN CURRENT SATURATION

(a) μ(field effect) > 0

(b) $10^{13} < n < 10^{18}$ cm^{-3}*

(c) 0.18 (InSb) $\leq E_g \leq$ 2.4 eV (CdS)*

(d) Operation as a TFT with $g_m > 0$ and I_D saturation preferable**

(e) Sufficiently low density of traps associated with the semiconductor-dielectric interface to permit modulation of the source-to-drain conductivity by the transverse electric field imposed by a reasonable gate potential

(f) Low resistance ohmic contact of source and drain electrodes to the semiconductor

(g) Good adhesion of adjacent layers

(h) Reasonably matched linear expansivities

(i) Low reactivity with environmental water vapor and oxygen at operating temperatures ($\approx$ 0 - 100 C)

(j) Low chemical and metallurgical reactivity at the interfaces at operating temperatures ($\approx$ 0-100 C)

(k) Chemical and metallurgical compatibility of adjacent materials during processing.

Table 3 embodies an attempt to apply criterion (d) to the semiconductor materials under consideration. In this table, the semiconductors for which TFT operating information was found in the literature were divided into groups. The groups reflect the existence or nonexistence of field effect and the degree of drain current I_D saturation when a field effect does exist. The groups are arranged in order of decreasing desirability. The semiconductors within a particular group are listed in order of decreasing TFT transconductance g_m, where values were reported.

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* These "criteria" are not rigid, but represent the ranges reported in the TFT literature.

** Not a rigid requirement.

TABLE 3. PERFORMANCE OF SOME SEMICONDUCTOR POLYCRYSTALLINE THIN FILMS IN IGFET'S

Semiconductor Material	g_m, μmho	ρ, Ω-cm	n, cm^{-3}	μ, cm^2/V-sec	E_g, eV
		Field Effect and I_D Saturation:			
Te	≤ 40,000	few tenths	≈ 3×10^{17} (calc.)	> 200 (effective)	0.32, 0.37
CdS	≤ 25,000	≈ 10^4	≈ 10^{13}	0.1-150 (effective)	2.4
CdSe	≤ 10,000	> 20	---	4-30	1.7
CdS-CdSe	≤ 2,000	---	---	---	---
GaAs	≤ 20	---	---	---	1.39
CdS-ZnS	> 0	---	---	---	
		Field Effect and Incomplete I_D Saturation:			
InAs	10,000	0.026 (calc.)	8×10^{16}	3000 (field effect)	0.36
InSb[a]	≤ 3,000	0.03	5×10^{17}	≈ 600 (film)	0.18
PbS	≤ 1,500	≥ 0.024[b] (calc.)	≤ 10^{18} (b)	≤ 260 (effective)	0.41
Si	≈ 100	500	≈ 1.7×10^{15} (calc.)	5-10 (effective)	1.10
Ag_2Te	> 0	---	---	≤ 400 (film)	0.17
Ge	> 0	---	---	---	0.66
CdTe	> 0	---	---	---	≈ 1.45
		Field Effect and No I_D Saturation:			
SnO_2	≤ 3,000 [c]				---

(a) I_D saturated in one reference.

(b) The meaning of the term "actual charge density" is not clear as reported in reference (40).

(c) Before degradation. (16)

TABLE 3. PERFORMANCE OF SOME SEMICONDUCTOR POLYCRYSTALLINE THIN FILMS IN IGFET'S (Continued)

Semiconductor Material	g_m, μmho	ρ, Ω-cm	n, cm^{-3}	μ, cm^2/V-sec	E_g, eV
Se	≤ 200				~ 2
ZnTe	> 0				2.2
PbTe	> 0				0.32
Bi_2Se_3	> 0				0.35
MnSe	> 0				---
MnTe	> 0				---
		Small Field Effect:			
SiC	~ 0				2.2(β), 3.12(α)
Bi_2Te_3	~ 0				0.15
		Very Little or No Field Effect:			
B	≈ 0				---
CoS	≈ 0				---
ZnO	≈ 0				3.2
Gd_2Se_3	≈ 0				---
SnS	≈ 0				≈ 1.26
$MoTe_3$	≈ 0				---
WS_3	≈ 0				---
WSe_3	≈ 0				---
$MnSi_2$	≈ 0				---
		No Aeeeptable Film:			
BaO					4.2

Several of the semiconductors in the latter part of Table 3 were examined only briefly in short-term investigations. It is quite possible that more extensive experimental development of such materials could improve their TFT performance levels above that indicated in Table 3. As it stands, however, Table 3 is representative of the TFT performance levels reported in the available literature for the indicated materials.

Examination of Table 3 suggests that TFT's using the following semiconductor materials more fully satisfy criterion (d):

Si	Ag_2Te	CdS	GaAs	PbS
Ge		CdSe	InAs	SnO_2
Se		CdTe	InSb	
Te				

The pseudo-binary alloys, CdS-CdSe and CdS-ZnS have not been included for two reasons. First, they do not appear to offer advantages over CdS and CdSe as semiconductors in a thin-film IGFET; and second, the fabrication of devices using these materials as semiconductors would be more complicated than using CdS or CdSe alone.

The semiconductor layer is polycrystalline both in the TFT's considered and in the thick film IGFET's envisioned. The extent to which a given semiconductor material satisfies criterion (d), however, is still dependent on the process of deposition. Thus the successful use of a semiconductor material in a TFT does not necessarily guarantee that the same material will work well in a thick film IGFET. Unfortunately, only limited information is available on the properties of these semiconductors deposited by thick-film-compatible processes. As a result, the successful use of a semiconductor in a TFT will be regarded as at least a rough indication of potential success in a thick film IGFET.

Values of resistivity ρ, carrier concentration n, mobility μ, and bandgap energy E_g were also listed in Table 3, where reported, in an attempt to determine the ranges of these parameters associated with successful TFT operation. It had been hoped that this procedure would yield a set of fairly narrow ranges of ρ, n, μ, and E_g which could then be used

to estimate the potential of other semiconductors for which no reports of TFT operation were available. The resulting ranges were too wide, however, to be sufficiently restrictive for the intended purpose.

The ability of the 13 materials listed above to more fully satisfy criterion (d) suggests that with one exception, they also satisfy criteria (a) through (c) and (e) through (h).

Se is the exception. The hexagonal allotrope, has a larger linear expansivity of 37 x 10^{-6} C^{-1} at 20C, compared with 5.9 x 10^{-6} C^{-1} for a 96% alumina substrate between 25 and 200 C. Thus Se must be rejected because of its failure to satisfy criterion (h).

$BaTiO_{(3-x)}$ was mentioned earlier as a candidate semiconductor in view of the existence of the reduced titanate capacitor technology.[43] Since no reports of TFT's using a $BaTiO_{(3-x)}$ semiconductor layer were found in the literature survey, it is difficult to determine if $BaTiO_{(3-x)}$ satisfies criteria (d) and (e). Further searching of the literature could be expected to verify that cirteria (a) and (f) are satisfied. The use of $BaTiO_3$ in thick film capacitors[49] may imply the satisfaction of criteria (g) and (h).

Thus reduced $BaTiO_3$ semiconductor appears to have potential for use in a thick film IGFET, pending more information on certain material properties indicated in the above discussion.

A similar evaluation applies to semiconducting $TiO_{(2-x)}$. The remaining materials are Si, Ge, Te, Ag_2Te, CdS, CdSe, CdTe, GaAs, InAs, InSb, PbS, SnO_2, $BaTiO_{(3-x)}$ and $TiO_{(2-x)}$. The satisfaction of criteria (i) and (j) by these 14 semiconductors is related to the long-term stability of the device. Although no major problems are expected, it is difficult to accurately predict the potential stability of a thick film IGFET using these materials.

Laznovsky has reported degradation of a CdS semiconductor film by migrant impurities from adjacent thick film layers of gold electrodes and $BaTiO_3$ dielectric.[10] He also reported damage to other layers by corrosive chlorine vapors released from the semiconductor flux during

firing. These results emphasize the necessity of selecting a device configuration and processes for deposition of the adjacent electrode and dielectric layers in an attempt to more nearly satisfy criterion (k).

The use of PdO semiconductor in a thick film IGFET was mentioned earlier because of the possibility of its being grown on existing Pd-bearing, thick-film, conductive or resistive pastes during firing. The incorporation of this processing technique into a thick-film IGFET, however, did not appear to be practical.

MnO_2 and the semiconductor glasses were also mentioned earlier as candidate semiconductors to be evaluated for use in a thick film IGFET. A more thorough review of the literature is required to determine the potential of these materials.

Preferred Semiconductor Materials.-- A number of semiconductor materials reported in the TFT literature and elsewhere have been evaluated on the basis of the listed material criteria. The result of this evaluation is the selection of the following 14 materials for consideration as semiconductor layers in this study:

Si	Ag_2Te	CdS	GaAs	PbS	$BaTiO_{(3-x)}$
Ge		CdSe	InAs	SnO_2	$TiO_{(2-x)}$
Te		CdTe	InSb		

Dielectrics

Review of TFT Materials.-- Table 4 lists the gate insulator materials noted in the survey of the TFT literature. The table includes information on the mating semiconductor, method of insulator deposition, insulator film thickness, dielectric constant and breakdown electric field, where reported.

SiO is probably the most commonly used dielectric in TFT's. It is also used in combination with other materials such as Dy_2O_3, Bi_2O_3, B_2O_3, and SiO_2.

TABLE 4. GATE INSULATOR MATERIALS USED IN TFT'S

Gate Insulator Material	Mating Semiconductor in TFT	Insulator Film Deposition	Insulator Film Thickness	Remarks	Reference
SiO	Te	Evaporation			(19)
SiO	CdS	Evaporation	1,000-10,000 Å	$E_{bkdn} > 10^6$ V/cm	(24)
SiO	CdS	Evaporation	< 500 Å	Depletion mode	(25)
SiO	CdS	Evaporation			(26)
SiO	CdS	Evaporation			(27)
SiO	CdS	Evaporation			(45)
SiO	CdS	Evaporation			(20)
SiO	CdS	Evaporation	≈ 800 Å	Post-deposition thermal stability is successful	(31, 47)
SiO	CdSe	Evaporation (50 Å/sec.)		ρ(CdSe) decreased 10,000/1; high sensitivity in depletion mode	(17)

TABLE 4. GATE INSULATOR MATERIALS USED IN TFT'S (Continued)

Gate Insulator Material	Mating Semiconductor in TFT	Insulator Film Deposition	Insulator Film Thickness	Remarks	Reference
SiO	CdSe	Evaporation (1 Å/sec.)		ρ(CdSe) decreased 10/1; medium sensitivity in enhancement mode.	(17)
SiO	CdSe	Evaporation			(16)
SiO	GaAs	Evaporation in O_2 at 10^{-4} mm Hg	2,500 Å		(35)
SiO	CdTe	Evaporation	1,500 Å		(23)
SiO	InAs	Reactive evaporation	1,500 Å		(37)
SiO	InSb	Evaporation			(38)
SiO	InSb	Evaporation	~ 2,000 Å		(39)
SiO	Ag_2Te	Evaporation	1,500 Å		(23)
SiO	PbTe	Evaporation	1,500 Å		(23)
SiO	Bi_2Se_3	Evaporation	1,500 Å		(23)

TABLE 4. GATE INSULATOR MATERIALS USED IN TFT'S (Continued)

Gate Insulator Material	Mating Semiconductor in TFT	Insulator Film Deposition	Insulator Film Thickness	Remarks	Reference
SiO	MnSe	Evaporation	1,500 Å		(23)
SiO	MnTe	Evaporation	1,500 Å		(23)
SiO	Bi_2Te_3	Evaporation	1,500 Å		(23)
SiO	SnS	Evaporation	1,500 Å		(23)
SiO	Semiconductor not specified	Evaporation			(47)
SiO-Dy_2O_3	Te	Evaporation	1,000 Å		(22)
SiO-Dy_2O_3	Te	Evaporation			(16)
SiO-Dy_2O_3	CdSe	Evaporation			(16)
SiO-Dy_2O_3	Si	Evaporation			(16)
SiO-Dy_2O_3 (two layers)	CdSe	Evaporation	SiO < 200 Å Dy_2O_3:800-900 Å	SiO drops CdSe resistance, Dy_2O_3 is more stable	(17)

TABLE 4. GATE INSULATOR MATERIALS USED IN TFT'S (Continued)

Gate Insulator Material	Mating Semiconductor in TFT	Insulator Film Deposition	Insulator Film Thickness	Remarks	Reference
$SiO-Bi_2O_3$	CdSe	Evaporation			(16)
$SiO-B_2O_3$	Semiconductor not specified	Evaporation			(20)
$SiO-SiO_2$	InAs	Evaporation	3,000 Å	Dielectric constant = 8	(36)
SiO_x	Si	Evaporation			(15)
SiO_2	PbS	Slow evaporation SiO in H_2O vapor or O_2 ambient			(40)
SiO_2	Not clear	Evaporation	300-2,000 Å		(32)
SiO_2	Not clear	Evaporation			(21)
SiO_2	Not clear	Evaporation	3,000 Å	Dielectric constant depends on thickness	(47)
SiO_2	CdSe	Evaporation (50 Å/sec.)		$K_{max} = 4.3$ ρ(CdSe) decreased 10/1; poor sensitivity-enhancement mode.	(17)

TABLE 4. GATE INSULATOR MATERIALS USED IN TFT'S (Continued)

Gate Insulator Material	Mating Semiconductor in TFT	Insulator Film Deposition	Insulator Film Thickness	Remarks	Reference
Quartz	Not clear	Evaporation		Improved characteristics; no improvement in stability	(46)
SiO_2-B_2O_3-Dy_2O_3	Not clear	Evaporation			(20)
SiO-B_2O_3	Not clear	Evaporation			(20)
Silicate cement	CdS-CdSe	Apply at room temp., optional 200 C for 4 hrs.			(9)
Al_2O_3	SnO_2	Anodized	~ 250 Å		(41)
Al_2O_3	CdSe	Evaporation			(29)
Al_2O_3	Not clear	Evaporation		Dielectric constant = 6.4	(47)
Al_2O_3	CdSe	Evaporation (50 Å/sec.)		ρ(CdSe) decreased 10/1; poor sensitivity-enhancement mode.	(17)
Al_2O_3	CdSe	Wet anodized		Only unstable in the enhancement mode.	(17)

TABLE 4. GATE INSULATOR MATERIALS USED IN TFT'S (Continued)

Gate Insulator Material	Mating Semiconductor in TFT	Insulator Film Deposition	Insulator Film Thickness	Remarks	Reference
Al_2O_3	CdSe	Dry plasma anodization in O_2 gas discharge	500 Å (typical)	Much improved stability E_{bkdn}=5-8x10^6 V/cm, dielectric constant = 7.5	(44)
Al_2O_3	CdSe			Better stability with Al_2O_3	(33)
Al_2O_3	Te			Better stability with Al_2O_3	(33)
CaF_2	CdS	Evaporation	< 500 Å	Enhancement mode	(25)
CaF_2	Not clear	Evaporation	300-2,000 Å		(31)
CaF_2	CdSe	Evaporation		ρ(CdSe) decreased 100/1; high sensitivity-enhancement mode.	(17)
CaF_2	CdS	Evaporation			(32)
CaF_2	Te	Evaporation			(19)
MgF_2	InSb	Evaporation	~ 2,000 Å		(39)

TABLE 4. GATE INSULATOR MATERIALS USED IN TFT'S (Continued)

Gate Insulator Material	Mating Semiconductor in TFT	Insulator Film Deposition	Insulator Film Thickness	Remarks	Reference
MgF_2	Not clear	Evaporation	300-2,000 Å		(31)
MgF_2	CdSe	Evaporation		ρ(CdSe) decreased 1000/1; medium sensitivity-depletion mode.	(17)
AlF_3	Not clear	Evaporation	300-2,000 Å		(31)
AlF_3	CdSe	Evaporation		ρ(CdSe) decreased 10/1; medium sensitivity-enhancement mode.	(17)
$BaTiO_3$	CdS:CdSe	$BaTiO_3$ subtrate			(9)
B_2O_3	Not clear	Evaporation	300-2,000 Å	$E_{bkdn} > 2 \times 10^6$ V/cm	(31)
B_2O_3	Not clear	Evaporation		Mixing B_2O_3 with SiO increases breakdown strength.	(21)
ZnS	Not clear	Evaporation	900 Å	Dielectric constant depends on thickness $K_{max} = 34.7$	(48)
ZnS	CdSe	Evaporation		Extremely poor sensitivity-enhancement mode.	(17)

TABLE 4. GATE INSULATOR MATERIALS USED IN TFT'S (Continued)

Gate Insulator Material	Mating Semiconductor in TFT	Insulator Film Deposition	Insulator Film Thickness	Remarks	Reference
Se	CdSe	Evaporation		Extremely poor sensitivity-enhancement mode.	(17)
Si_3N_4	Not clear	Evaporation		Si_3N_4 "complex"	(48)
Si_3N_4	CdSe	Evaporation		Poor sensitivity-enhancement mode.	(17)
Nitrocellulose (Duco cement)	CdS:CdSe	Apply at room temperature		Dielectric constant $> 10^5$ for $f < 1$ Hz	(9)
Glyceryl monostearate	CdS:CdSe	$T \leq 60$ C		Less decrease in K with increasing f than for nitrocellulose	(9)
Dy_2O_3	CdSe	Evaporation	300-2,000 Å		(31)
Dy_2O_3	Not clear	Evaporation			(21)
Dy_2O_3	CdSe, Te	Evaporation		Excellent pinch-off	(16)
Dy_2O_3	CdSe	Evaporation (8 A/sec.)		ρ(CdSe) decreased 100/1; high sensitivity-enhancement mode.	(17)

TABLE 4. GATE INSULATOR MATERIALS USED IN TFT'S (Continued)

Gate Insulator Material	Mating Semiconductor in TFT	Insulator Film Deposition	Insulator Film Thickness	Remarks	Reference
La_2O_3	Not clear	Evaporation	300-2,000 Å		(31)
La_2O_3	Not clear	Evaporation			(21)
La_2O_3	Not clear	Evaporation	< 125 Å	Very thin	(48)
La_2O_3	CdSe	Evaporation	≈ 1,000 Å		(17)
Yb_2O_3	Not clear	Evaporation	300-2,000 Å		(31)
Yb_2O_3	Not clear	Evaporation			(21)
Yb_2O_3	Not clear	Evaporation	< 125 Å	Very thin	(48)
Yb_2O_3	CdSe	Evaporation			(16)
Yb_2O_3	CdSe	Evaporation	≈ 1,000 Å		(17)
Nd_2O_3	Not clear	Evaporation	300-2,000 Å		(31)
Nd_2O_3	Not clear	Evaporation			(21)

TABLE 4. GATE INSULATOR MATERIALS USED IN TFT'S (Continued)

Gate Insulator Material	Mating Semiconductor in TFT	Insulator Film Deposition	Insulator Film Thickness	Remarks	Reference
Nd_2O_3	CdSe	Evaporation	≈ 1000 Å		(17)
CeO_2	Not clear	Evaporation			(48)
CeF_3	CdSe	Evaporation			(16)
Eu_2O_3	CdSe	Evaporation		More expensive than Dy_2O_3 & no better	(16)
Eu_2O_3	CdSe	Evaporation	≈ 1000 Å		(17)
Y_2O_3	CdSe	Evaporation			(16)
Y_2O_3	CdSe	Evaporation	≈ 1000 Å		(17)
Sm_2O_3	CdSe	Evaporation	≈ 1000 Å		(17)
Ho_2O_3	CdSe	Evaporation	≈ 1000 Å		(17)
Er_2O_3	CdSe	Evaporation	≈ 1000 Å		(17)
Lu_2O_3	CdSe	Evaporation	≈ 1000 Å		(17)

Al_2O_3 has been used as a TFT gate insulator. This material can be grown on an aluminum gate electrode in an inverted configuration. Waxman obtained a significant improvement in the stability of CdSe TFT's by using dry plasma anodized Al_2O_3 in place of SiO.[44]

Other inorganic dielectrics used in TFT's include the fluorides of calcium, magnesium and aluminum.

Sihvonen reported the use of a $BaTiO_3$ substrate as the gate insulator in a TFT.[9] He also tried some organic dielectrics deposited at or near room temperature.

Si_3N_4 is the only nitride dielectric reported.

The Melpar investigation of rare-earth oxides as dielectrics was motivated by an interest in operating TFT's at temperatures up to 500 C and possibly in a radiation environment.

Consideration of current capacitor manufacturing technologies suggests the addition of at least two materials to the list of dielectrics obtained from the TFT literature survey. They are TiO_2 and Ta_2O_5. A number of other refractory metals form stable thermal and anodic oxide films, but TiO_2 and Ta_2O_5 were selected because of the considerable experience in their use.

Application of Dielectric Material Criteria.-- The material criteria for the gate insulator dielectric are the following:

(a) $K/t > 10^5$/cm (10/micron)

(b) $E_{breakdown} > 10^5$ V/cm

(c) $\rho > 10^6$ Ω-cm

(d) Sufficiently low density of traps associated with the semiconductor-dielectric interface to permit modulation of the source-to-drain conductivity by the transverse electric field imposed by a reasonable gate potential

(e) Good adhesion of adjacent layers

(f) Reasonably matched linear expansivities

(g) Uniform thickness

(h) Freedom from pinholes and voids

(i) Low reactivity with environmental water vapor and oxygen at operating temperatures ($\approx$ 0-100 C)

(j) Low chemical and metallurgical reactivity at the interfaces at operating temperatures ($\approx$ 0-100C)

(k) Chemical and metallurgical compatibility of adjacent materials during processing.

The dielectric material criteria will be applied to SiO_2, $BaTiO_3$, TiO_2 and Ta_2O_5 for which well known thick-film-compatible processes of deposition exist. The details of these processes are discussed in a subsequent section of this report.

SiO_2: The successful operation of a TFT using a pyrolytically deposited SiO_2 gate insulator[8] implies the satisfaction of criteria (a) through (h). The satisfaction of criteria (i) and (j) is related to the long-term stability of the device. It is difficult to predict the potential stability of a thick film IGFET using an SiO_2 dielectric. The satisfaction of criterion (h) depends on the configuration, and on the materials and deposition processes used in the adjacent layers.

$BaTiO_3$: Commercially available thick film pastes containing $BaTiO_3$ can be printed and fired to obtain films with a dielectric constant of 600 at room temperature. Application of criterion (a) to such a dielectric film, implies a maximum thickness of 60 microns. A thickness of 50 to 60 microns is typical for printed and fired thick film layers of this type.

A $BaTiO_3$ substrate could be expected to have a dielectric constant on the order of 2000 at room temperature. The application of criterion (a) to such a substrate implies a maximum substrate thickness of 200 microns (approximately 8 mils). Thus the use of a 10 mil thick $BaTiO_3$ substrate as a gate insulator comes reasonably close to satisfying criterion (a).

$BaTiO_3$ may fall somewhat short of satisfying criterion (b), but this apparent shortcoming is probably acceptable in view of the greater thickness of the $BaTiO_3$ layers.

Hamer reported a resistivity of approximately 10^{13} Ω-cm for $BaTiO_3$.[43] This value easily satisfies criterion (c).

The use of a $BaTiO_3$ substrate in an experimental thick film IGFET by Sihvonen[9] suggests that criterion (d) is satisfied with a CdS-CdSe semiconductor layer.

Hoffman reported the use of printed and fired $BaTiO_3$ in thick film capacitors.[49] His results indicate that criteria (e) through (h) are satisfied.

The satisfaction of criteria (i) and (j) is related to the long-term stability of the device. Although no major problems are expected, it is difficult to predict the potential stability of a thick film IGFET using a $BaTiO_3$ dielectric.

Laznovsky reported degradation of a CdS semiconductor layer by migrant impurities from a thick film $BaTiO_3$ dielectric layer.[10] This result points out the need to select configurations and processes for deposition of the adjacent semiconductor and electrode layers in order to satisfy criterion (k).

Ta_2O_5: Application of criterion (a) to Ta_2O_5, suggests a maximum thickness of 2.6 microns for a dielectric constant of 26.[42] Ta_2O_5 layers of less than 2.6 micron thickness are easily obtainable using anodization.[42]

With a breakdown electrical field of 2×10^6 V/cm[42], Ta_2O_5 easily satisfied criterion (b).

The extensive use of Ta_2O_5 in solid electrolytic tantalum capacitors suggests that criteria (c), (e), (f), (g), and (h) are satisfied.

Whether or not criterion (d) is satisfied cannot be predicted on the basis of the information available for this report. An experimental effort would be required to resolve this question.

The satisfaction of criteria (i) and (j) is related to the long-term stability of the device. Although no problems are expected, it is difficult to predict the potential stability of a thick film IGFET using Ta_2O_5.

The satisfaction of criterion (k) depends on the device configuration, and the materials and deposition processes used in the adjacent layers.

TiO_2: Application of the dielectric material criteria to TiO_2 suggests its potential for use as a gate insulator in a thick film IGFET.

Preferred Dielectric Materials.-- A number of dielectric materials reported in the TFT literature and elsewhere have been evaluated on the basis of the listed material criteria and the existence of thick-film-compatible processes for their deposition. The result of this evaluation is the selection of SiO_2, $BaTiO_3$, Ta_2O_5, and TiO_2 for further consideration as gate insulator materials in this study.

Electrodes

Source and Drain Electrodes.-- Table 5 lists the source and drain electrode materials noted in the survey of the TFT literature. For each source and drain electrode material, the table indicates the mating semiconductor, electrode deposition process, and literature reference information. The listed source and drain electrode materials include Au, In-Au, In, Al, Nichrome, Co, Kovar, Cr, Sb, Bi, Te, Hg-In, and Sn-Ga. Ag is excluded from the list because of problems with Ag migration in Ag-bearing pastes used in passive thick film technology.

The material criteria for source and drain electrodes are the following:

(a) $\rho < (50\text{-}100)\ \mu\Omega\text{-cm}$.
(b) Low resistance ohmic contact to semiconductor
(c) Good adhesion to adjacent layers
(d) Reasonably matched linear expansivities
(e) Low reactivity with environmental water vapor and oxygen at operating temperatures ($\approx$ 0 - 100 C)
(f) Low chemical and metallurgical reactivity at the interfaces at operating temperatures ($\approx$ 0 - 100 C)
(g) Chemical and metallurgical compatibility of adjacent materials during processing.

TABLE 5. SOURCE AND DRAIN ELECTRODES USED IN TFT'S (cont.)

Source & Drain Material	Mating Semiconductor	Remarks	Reference
Al	Si		(15)
Al	CdS	Source & drain above CdS	(25)
Al	CdS (printed & fired)		(27)
Al	InAs		(36)
Al	InSb	n-type operation	(38)
Nichrome	Te	Co & Kovar better than Nichrome in Te TFT's	(16)
Nichrome	CdSe		(17)
Nichrome	CdS, CdSe, Te	Low work function conductor for n-type semiconductor; high work function conductor for p-type semiconductor	(21)
Nichrome	CdS, CdSe, CdTe		(31)
Co	Te		(22)
Co	Te	Co & Kovar better than Nichrome in Te TFT's	(16)
Co	Te		(27)

TABLE 5. SOURCE AND DRAIN ELECTRODES USED IN TFT'S (cont.)

Source & Drain Material	Mating Semiconductor	Remarks	Reference
Kovar	Te	Co & Kovar better than Nichrome in Te TFT's	(16)
Cr	CdSe	Cr source electrode yields high contact resistance to CdSe	(44)
Cr	CdS, CdSe, Te	Low work function conductor for n-type semiconductor; high work function conductor for p-type semiconductor	(21)
Sb	InSb	n-type operation	(38)
Bi	Se		(18)
Te	Se		(18)
90% Hg-10% In	CdS-CdSe (printed & fired)	Print conductor paste & heat to 120 C in vacuum	(9)
Sn-Ga (5-10% Sn)	CdS-CdSe (printed & fired)	Wet film; does not flow	(9)
Au resinate solution: Hanovia Liquid Brite Gold 7621	CdS-CdSe (printed & fired)	Au predeposited & fired before CdS-CdSe	(9)

TABLE 5. SOURCE AND DRAIN ELECTRODES USED IN TFT'S

Source & Drain Material	Mating Semiconductor	Remarks	Reference
Au	Te		(19)
Au	CdS		(50)
Au	CdS		(44)
Au	CdS	Source & drain under CdS	(26)
Au	CdS, CdSe	Source & drain under CdS & CdSe	(25)
Au	CdSe		(44)
Au	CdSe		(29)
Au	GaAs		(35)
Au	InAs		(36)
Au	InSb	p-type operation	(38)
Au	PbS		(40)
In-Au	CdSe		(30)
In-Au	CdSe		(44)
In (source only)	CdS		(44)

The source and drain electrode material criteria will be applied to gold for which a well known thick-film-compatible process of deposition exists.

The use of Hg-In or Sn-Ga source and drain electrodes in an inverted-staggered configuration might be of interest, except for the possibility of exceeding the conductor melting points at the modestly elevated temperature associated with device operation.

Gold, Pd-Au, and Pt-Au source and drain electrodes can be deposited by printing and firing commercially available thick film conductor pastes. These gold electrodes could be expected to satisfy all of the criteria listed above, with the possible exception of criterion (g).

Laznovsky reported degradation of a CdS semiconductor layer by migrant impurities from a gold thick film electrode layer.[10] This result points out the need to select configurations and processes for deposition of the semiconductor and dielectric layers so as to minimize the migration of impurities from the gold thick film source and drain electrodes.

Gate Electrodes.-- Table 6 lists the gate electrode materials noted in our review of the TFT literature. For each gate electrode material, the table indicates the mating gate insulator and the literature reference information. The listed gate electrode materials include aluminum, gold, titanium, molybdenum, and silver. Each of the materials was deposited by vacuum evaporation, except for the silver which was a paint (duPont no. 5584).

The material criteria for the gate electrode are the same as those listed in the previous section for source and drain electrodes, except that criterion (b) does not apply.

The gate electrode material criteria will be applied to gold, titanium and possibly silver for which well known thick-film-compatible processes of deposition exist.

The silver paint is not expected to satisfy criteria (f) and (g) because of silver migration and other problems contributing to poor stability.

TABLE 6. GATE ELECTRODES USED IN TFT'S

Gate Electrode* Material	Mating Gate Insulator	Remarks	Reference
Al	SiO		(35)
Al	SiO		(38)
Al	SiO		(21)
Al	SiO		(45)
Al	SiO		(27)
Al	SiO, others	Al gate electrode gives better stability than Au.	(31)
Al	SiO-SiO_2		(36)
Al	SiO-Dy_2O_3		(31)
Al	SiO_2		(50)
Al	Al_2O_3		(29)
Al	Al_2O_3	Al_2O_3 is dry plasma anodized on Al gate.	(44)
Al	Al_2O_3	Al_2O_3 is dry plasma anodized on Al gate.	(30)
Al	Al_2O_3 (anodized)		(41)
Al	Not clear	Ti & Mo appear no better than Al for gate electrode.	(17)
Au	SiO		(26)
Au	SiO-SiO_2		(36)
Au	SiO_2	SiO formed too highly conducting surface channel on PbS semiconductor.	(40)

TABLE 6. GATE ELECTRODES USED IN TFT'S
(Continued)

Gate Electrode * Material	Mating Gate Insulator	Remarks	Reference
Au	Al_2O_3		(29)
Ti	Not clear	Ti appears no better than Al for gate electrode.	(17)
Mo	Not clear	Mo appears no better than Al for gate electrode.	(17)
Aqueous Ag ink	Organic dielectric		(9)
duPont Ag paint No. 5584	Cement, ceramic, inorganics		(9)

* Note: All gate electrode materials were deposited by vacuum evaporation unless otherwise specified.

The gold thick film conductor is expected to be suitable for use as a gate electrode, subject to the same precautions discussed previously in connection with source and drain electrode materials.

A thick-film-compatible process exists for the application of titanium films to a ceramic substrate.[51] With an electrical resistivity of 42 $\mu\Omega$-cm and a linear expansivity of 8.4 x $10^{-6}C^{-1}$ (both at 20 C), titanium satisfies criteria (a) and (d). Criterion (c) is satisfied in an inverted configuration where the titanium layer is bonded to the ceramic substrate at one interface and has its own thermal oxide for a gate insulator at the other interface. Titanium is also expected to satisfy criteria (e), (f) and (g).

A similar application of material criteria to tantalum suggests its use as a gate electrode material, providing a suitable process of deposition exists (such as that for titanium).

Preferred Electrode Materials.-- A number of electrode materials reported in the TFT literature and elsewhere have been evaluated on the basis of the listed material criteria and the existence of thick-film-compatible processes for their deposition. The results of this evaluation are the selection of gold source and drain electrodes and gold, titanium and tantalum gate electrodes for consideration in this study.

DISCUSSION OF DEVICE FABRICATION

Thick-Film-Compatible Fabrication Processes

Semiconductor Deposition Processes.-- The following processes were considered for deposition of the polycrystalline semiconductor layer:

(1) Sintering (CdS, CdSe)

(2) Pyrolytic decomposition (Si, Ge, CdS, SnO_2)

(3) Rapid pressing of molten material between flat quartz plates (InSb)

(4) Wet Chemical desposition (PbS)

(5) Vapor transport (GaAs, InAs)

(6) Reduction of a dielectric material at elevated temperature [$TiO_{(2-x)}$, $BaTiO_{(3-x)}$].

The following process criteria were listed in a previous section of this report:

(a) Thick film process or a process compatible with thick film technology

(b) No vacuum evaporation or sputtering (preferable)

(c) Chemical and metallurgical compatibility of adjacent materials during processing.

A brief description of the specific semiconductor deposition processes indicated above is now presented. Criterion (b) is satisfied by each of the processes. An evaluation of each process [based on consideration of criteria (a) and (c)] is included in the following discussion.

Silicon: Silicon films can be prepared by the hydrogen reduction of $SiCl_4$ or $SiHCl_3$. In these pyrolytic decomposition processes, a mixture of the halide vapor and hydrogen is passed over a heated substrate. The silicon halides are reduced to silicon at substrate temperatures above 1000 C, with 1200 C being a typical deposition temperature. A similar process employs hydrogen-diluted silane (SiH_4).[52] Film thicknesses of a few microns have been obtained.[53]

The 1000 to 1200 C processing temperature range suggests that this step should precede the deposition of other FET layers. This ordering of the process steps is required in order to avoid the risk of degrading other thick film layers by a 1000 to 1200 C reducing atmosphere. The possibility of damaging the silicon film during processing of subsequent electrode and dielectric layers could present a problem in satisfying criterion (a).

Germanium: Germanium films of controlled thickness and resistivity have been grown by means of the hydrogen reduction of $GeCl_4$ and $GeBr_4$.[54,55] The reactions will proceed at temperatures in excess of

600 C for $GeBr_4$ and 615 C for $GeCl_4$. Doping of the films is accomplished by including in the germanium-containing gas controlled amounds of phosphorus halides for n-type conductivity or boron halides for p-type conductivity.

Cadmium Sulphide and Cadmium Selenide: A process for printing and firing CdS has been developed in connection with the fabrication of photocells. The paste is prepared by mixing CdS power and ethyl cellulose powder with a solvent solution of dibutyl carbotol. The paste is screen printed on the substrate and sintered at about 500 C in air for 30 minutes.(8)

Another process for depositing a polycrystalline layer of CdS was developed by the National Cash Register Company for the fabrication of thin-film photovoltaic cells.(56) It offers the advantage of lower processing temperatures ($\approx$ 200 C). The technique involves a chemical spray deposition depending on the pyrolytic decomposition of an organic complex to yield CdS. Either cadmium thio-cyanate $[Cd(SCN)_2]$ or a combination of cadmium chloride and thiourea $\{Cd[(NH_2)_2CS]_2Cl_2\}$ serves as the organic complex. Films of less than one micron thickness have been obtained at a substrate temperature of 210 C.

CdSe layers can be printed and fired in a manner similar to that described for CdS. In addition, researchers at Texas Instruments have developed a CdS-CdSe paste for use in thick film insulated-gate FET's.(9) Reference (9) contains a detailed step-by-step description of the preparation of the CdS-CdSe powder, the mixture of the paste, screen printing, sintering, and the application of surface activating agents.

The sintering processes for CdS and CdSe may fail to satisfy criteria (a) and (c) in two respects. First, the release of corrosive Cl vapors from the semiconductor flux during firing could damage other thick film layers.(10) Second, the migration of impurities from the electrode and dielectric layers into the CdS or CdSe during firing (at 500 C) could substantially alter the electrical properties of the semiconductor layer.(10) The lower processing temperature (210 C) for the pyrolytic deposition of

CdS is expected to help overcome these two problems. It is probable that this process could be adapted for deposition of CdSe.

Indium Arsenide: RCA has developed a process for the preparation of polycrystalline films of InAs for use in photovoltaic solar energy cells.[57] The InAs film is grown by vapor transport from n-type polycrystalline source wafers in a flow of hydrogen gas. The InAs source temperature is estimated to be 725 C and the substrate temperature is approximately 650 C. Films approximately four microns thick were obtained in two hours and it is assumed that thinner layers could be deposited in shorter times.

The 650 C substrate temperature for this process makes it awkward for incorporation into the sequence of process steps required in FET fabrication. This raises some problems in connection with criterion (a). First, it is not clear whether or not the deposition of subsequent electrode and dielectric layers will damage the InAs semiconductor layer. Second, if the semiconductor layer is deposited last, it may be degraded by migration of impurities from adjacent layers. In addition, previously deposited thick film layers might be altered by the hot hydrogen reducing atmosphere.

Gallium Arsenide: Thin polycrystalline layers of GaAs have been deposited by a vapor transport process similar to that described for InAs.[55]

Indium Antimonide: Bate and Taylor prepared thin films of InSb by a "squashing" technique where molten material is physically squashed between two parallel optically flat surfaces (preferably quartz).[58] InSb melts at 530 C. The thin layer prepared in this way is always polycrystalline. The relatively short time required in the molten state during the "squashing" operation reduces the probability of degrading the InSb by migration of impurities from adjacent layers. This process has the disadvantage that it would require some development for its adaptation to use in the fabrication of a thick-film IGFET.

Lead Sulfide: Thin polycrystalline films of PbS are deposited by a wet chemical process in the fabrication of infrared detectors.[59] The substrate is placed in an aqueous solution of lead acetate and thiourea.

Sodium Hydroxide is added and a mirror-like coating of PbS precipitates over the substrate. The polycrystalline films are about one micron thick with crystallite dimensions on the order of 0.1 micron. The PbS layer can be protected from atmospheric effects by overcoating with a thin film of butyl methacrylate.

Since the entire process is performed at room temperature, it is suitable as the final processing step in the fabrication of an inverted coplanar IGFET. This process appears to satisfy all three process criteria. If the PbS source-to-drain resistance is too low, the use of a thinner film and post-deposition heat treatment in air could be used to increase the resistance. An oxidation treatment to increase sensitivity is a commonly-used step in lead sulphide infrared detector fabrication. It increases film resistance markedly.

Stannic Oxide: SnO_2 films are currently produced by pyrolytic decomposition for use in discreet resistors.[42] They are deposited by spraying aqueous organic $SnCl_4$ solutions on a glass or ceramic substrate heated to 500 to 800 C. Hydrolysis of the $SnCl_4$ produces SnO_2 films. Due to the reducing atmosphere caused by the organics, the film is highly oxygen deficient resulting in an n-type semiconductor. The addition of donors such as Sb, As, Te, W, P, or F lowers the resistivity and yields a more positive temperature coefficient. Acceptors such as Fe, B, Cd, In, or Al have the opposite effect. These additives are incorporated into the original solution. Sb doping provides the greatest environmental stability.

The problems associated with this process are similar to those previously discussed in connection with the deposition of InAs by vapor transport.

Reduced Barium Titanate: A reduced, or semiconducting $BaTiO_3$ ceramic capacitor is used in thick film hybrid integrated circuits.[43] The reducing step changes the ceramic from an insulator to a semiconductor. The reaction is carried out above 900 C in a strong reducing atmosphere such as hydrogen. The $BaTiO_3$ insulator has a high dielectric constant and a resistivity on the order of 10^{13} Ω-cm, while the reduced titanate is a semiconductor with a resistivity in the range from 1 to 10 Ω-cm.

The 900 C reducing temperature places the semiconductor deposition at or near the beginning of the sequence of processing steps in the fabrication of a thick film IGFET. The $BaTiO_3$ to be reduced could be a screen-printed layer of commercial paste or a portion of a $BaTiO_3$ substrate. Satisfaction of criteria (a) and (c) might be impaired by migration of electrode impurities into the semiconductor during its firing or during the firing of subsequent electrode layers.

Reduced Titanium Dioxide: A similar reducing process can be employed to obtain semiconducting $TiO_{(2-x)}$ from dielectric TiO_2.

Dielectric Deposition Processes.-- The following processes were considered for deposition of the polycrystalline dielectric layer:

(a) Print and fire a thick film paste ($BaTiO_3$)
(b) Pyrolytic decomposition (SiO_2)
(c) Thermal oxidation (SiO_2 , TiO_2, Ta_2O_5)
(d) Anodization (SiO_2, TiO_2, Ta_2O_5)
(e) Oxidation of a thin layer on the surface of a reduced semiconductor ($BaTiO_3$, TiO_2)
(f) Use of the substrate as dielectric ($BaTiO_3$)

SiO_2, $BaTiO_3$, TiO_2 (rutile), and Ta_2O_5 dielectrics have been selected for consideration in this study. The applicability of the above processes to these dielectrics is indicated above in parenthesis and below in the following table.

Dielectric	Process of Deposition
SiO_2	(b) (c) (d)
$BaTiO_3$	(a) (e) (f)
TiO_2	(c) (d) (e)
Ta_2O_5	(c) (d)

A brief description of the specific dielectric deposition processes indicated in the table is now presented. Criterion (b) is satisfied by each of the processes. An evaluation of each process [based on consideration of criteria (a) and (c)] is included in the following discussion.

Silicon Dioxide: RCA has deposited thin films of SiO_2 dielectric by the pyrolytic decomposition of silane (SiH_4).[8] In this process, a gas comprised of 3% SiH_4 and 97% N_2 flows over a heated substrate. The substrate temperature was not reported but it is estimated to be 850 C.

The growth of a thermal oxide on Si is a well known facet of Si processing technology. Using dry O_2, temperatures of 900-1300 C are required.

SiO_2 can also be grown on Si by an anodization process.[60] In this process, a solution of oxalic acid and ethylene glycol is used with an anodizing potential of 20-30 volts.

The pyrolytic deposition of SiO_2 has been used in IGFET's with printed and fired CdS. The high deposition temperature (850 C, estimated) is somewhat of a disadvantage.

The thermal growth of SiO_2 on a Si surface has the advantage that the process can probably be performed in a standard tunnel kiln available at every thick film facility.

The wet anodization of SiO_2 on a Si surface has the advantage of being a room temperature process.

All three of these processes have strong potential for use in the fabrication of a thick film IGFET.

Barium Titanate: Hoffman has reported the recent development of a $BaTiO_3$ thick film dielectric paste.[49] The screen-printed dielectric is fired at 750-1050 C, over which range the dielectric constant increases from 400 to 800.

The preparation of $BaTiO_{(3-x)}$ semiconductor by a high-temperature reducing process was described in a previous section of this report. It is possible to reoxidize a $BaTiO_{(3-x)}$ surface to obtain a thin layer of $BaTiO_3$ dielectric.

When a $BaTiO_3$ substrate is used, the substrate itself can serve as the dielectric layer. Texas Instruments has made some experimental IGFET's using this approach.[33]

Difficulties in the use of the printed and fired $BaTiO_3$ dielectric paste in a thick film FET were revealed in the recent work at RCA.[10] These difficulties may be attributable to degradation of the semiconductor electrical properties by the migration of impurities from the $BaTiO_3$ into the semiconductor, the roughness of the $BaTiO_3$-semiconductor interface and the possible effect of the domain structure of a ferroelectric material at the interface with the semiconductor material.

The use of a $BaTiO_{(3-x)}$ semiconducting substrate with a thin layer of reoxidized $BaTiO_3$ as a dielectric might be expected to reduce the severity of the above difficulties.

Titanium Dioxide: TiO_2 dielectric can be grown on a titanium surface using a thermal oxidation process.[61] Oxidation temperatures range from 700 to 875 C, above which nonadherence of the oxide becomes prevalent.

An anodization process can be used to grow TiO_2 on a titanium surface, or to increase the thickness of thermally grown TiO_2. Such an anodization process is described in reference (61).

In addition, TiO_2 dielectric can be prepared by reoxidizing a thin surface layer of $TiO_{(2-x)}$ semiconductor. This process is similar to that already described for $BaTiO_3$.

If the ferroelectric nature of $BaTiO_3$ is a significant problem in its use as a dielectric layer in a thick film IGFET, the use of reoxidized TiO_2 dielectric in conjunction with $TiO_{(2-x)}$ semiconductor would overcome this problem.

The thermal oxidation of TiO_2 has the advantage that it could be performed in a standard tunnel kiln available at every thick film facility. The anodization of TiO_2 has the advantage of being a room temperature process. All three of these processes have high potential for the intended application.

Tantalum Oxide: The preparation of anodic Ta_2O_5 has received extensive attention in connection with the fabrication of tantalum oxide electrolytic capacitors.[42] A typical Ta_2O_5 capacitor dielectric process

yields 0.2 micron layers obtained with a 130 volt anodization potential in a room temperature electrolyte. Preparation of Ta_2O_5 by anodization has high potential for the intended application.

Electrode Deposition Processes.-- On the basis of the previous application of material criteria to a number of candidate electrode materials, gold, titanium and tantalum were selected for further consideration in this study.

Gold, Pt-Au, and Pd-Au electrodes can be deposited on an alumina substrate by screen printing and firing a commercially available thick film paste. The firing temperature can be anywhere in the range from 760 to 1000 C. Gold electrodes are used routinely in the manufacture of thick film capacitors. (The same cannot be said for thick film Pd-Ag electrodes, however, because of silver migration problems.) The use of gold electrodes in thick film capacitors suggests a sufficiently low reactivity during processing at the dielectric-to-electrode interfaces. The greater sensitivity of the semiconductor layer to possible doping by the constituents of the electrode and dielectric pastes is expected to present a more serious problem.[10]

In the case of titanium, the complete substrate could be coated with a thin film of the conductor by the process conceived by R. A. Quinn and R. F. Karlak.[51] The desired conductor pattern could then be obtained by the application of an etch resist and the subsequent etching away of the unwanted conductor areas.

Tantalum will be removed from further consideration in this study because a well-known thick-film-compatible process is not available for its deposition.

Thick-Film IGFET Configurations

Specific combinations of the selected semiconductor, dielectric, and electrode materials in the four major configurations will now be described. The staggered, coplanar, inverted-staggered, and inverted-coplanar configurations were described in a previous section of this report.

The following notation will be used in describing the various IGFET layers:

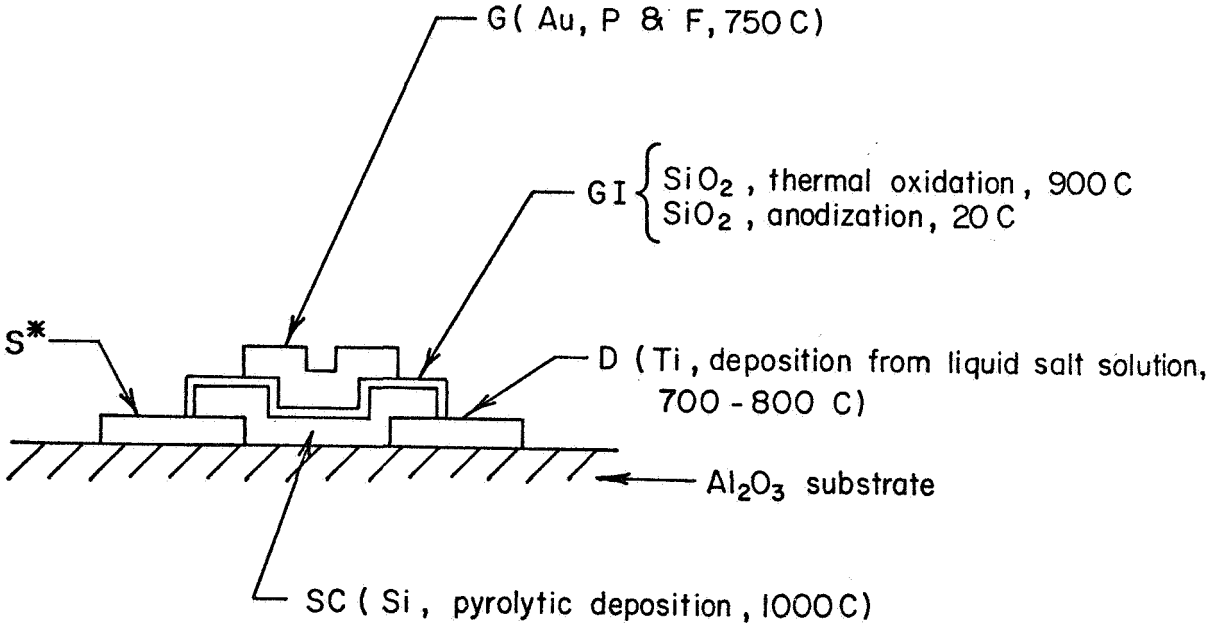
Symbol	Meaning
G	Gate electrode
GI	Gate insulator (or dielectric)
SC	Semiconductor
S	Source electrode
D	Drain Electrode
///////	Substrate
P&F	Screen print and fire

Configurations Using Al_2O_3 Substrate.

Staggered Configuration: In the staggered configuration, the source and drain electrodes are the first layers deposited on the substrate. This step can be accomplished by the printing and firing of a gold conductor paste at 1000 C. It follows that the semiconductor layer must be deposited at a process temperature in a suitable range below 1000 C. Such processes have been described for the deposition of Ge, InAs, GaAs, $BaTiO_{(3-x)}$ and $TiO_{(2-x)}$ at temperatures in the range from 500-900 C. Consideration of the pyrolytic deposition of an SiO_2 dielectric layer at 850 C (estimated) or the printing and firing of $BaTiO_3$ at 750 C reveals an important disadvantage inherent to the staggered configuration.

The disadvantage arises from the need for semiconductor and dielectric processing temperatures to fall in the range from 1000 to 750 C, the processing temperatures of the source and drain electrodes, and the gate electrode, respectively. The narrowness of this 250 C temperature range leads to a high probability of semiconductor degradation by migrant impurities from adjacent layers during three processing steps, each performed at over 500 C.

Two staggered configurations are shown in Figures 5 and 6, however, which tend to overcome the disadvantages just described.



* Note: The processing of source electrodes will be the same as that for drain electrodes unless otherwise specified.

FIGURE 5. STAGGERED CONFIGURATION - MODEL 1
Source and Drain Electrodes - Titanium; Semiconductor - Silicon; Gate Insulator - Silicon Dioxide; Gate Electrode - Gold

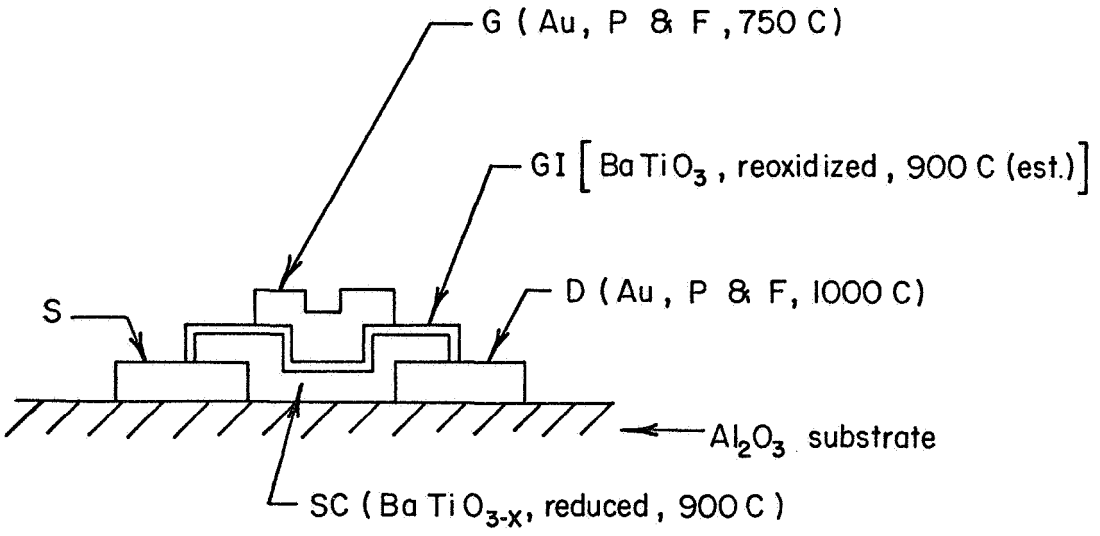


FIGURE 6. STAGGERED CONFIGURATION - MODEL 2
Source and Drain Electrodes - Gold; Semiconductor - Reduced Barium Titanate; Gate Insulator - Barium Titanate; Gate Electrode - Gold

Coplanar Configurations: The deposition of source, drain, and gate electrodes by screen printing and firing in a coplanar configuration where a thin dielectric layer is grown on the semiconductor surface reveals important difficulties. The location of the gate electrode between the source and drain requires a larger source-to-drain spacing L thus significantly reducing the device transconductance g_m, since $g_m \propto 1/L^2$. Also, since the gate electrode does not extend beyond the ends of the source and drain electrodes, as is the case in staggered configurations, that part of the semiconductor between the gate electrode and the source and drain electrodes will remain unmodulated by the gate potential. Thus, in the enchancement mode, the unmodulated portion of the semiconductor will represent a large unmodulated component of the source-to-drain resistance. Complete

coverage of the source-to-drain spacing by the gate electrode is not required, however, for operation in the depletion mode, since depletion of the current carriers at one point only between the source and drain electrodes is sufficient to "pinch off" the device. The above difficulties associated with the coplanar configuration could be minimized by making the source-to-gate and drain-to-gate spacings as small as possible. This might be accomplished using photolithographic techniques to form the electrode configurations from a screen printed and fired conductive film, such as is depicted in Figure 7. In this Figure, a silicon semiconductor layer is used in conjunction with a SiO_2 gate insulator.

Figure 8 shows essentially the same configuration but with a $BaTiO_{(3-x)}$ semiconductor layer and a reoxidized $BaTiO_3$ gate insulator.

Inverted-Staggered Configuration: The inverted-staggered configuration has the disadvantage that the deposition of the semiconductor layer is followed by the 750 C firing of the gold source and drain electrodes. This arrangement gives rise to semiconductor degradation by migrant impurities from the source and drain electrode layers. Also, with the gate electrode on the opposite side of the semiconductor film from the source and drain electrodes, a large unmodulated component to the source-to-drain resistance will be associated with the film thickness.

Inverted-Coplanar Configuration: The above disadvantages of the inverted-staggered configuration are essentially overcome in the inverted-coplanar configuration. Three specific forms of the inverted coplanar configuration are illustrated in Figures 9, 10 and 11.

Configurations Using $BaTiO_3$ Substrates.-- The use of $BaTiO_3$ as a substrate material leads to the simple configuration shown in Figure 12. The use of reduced titanate processing on a $BaTiO_2$ substrate is shown in Figure 13.

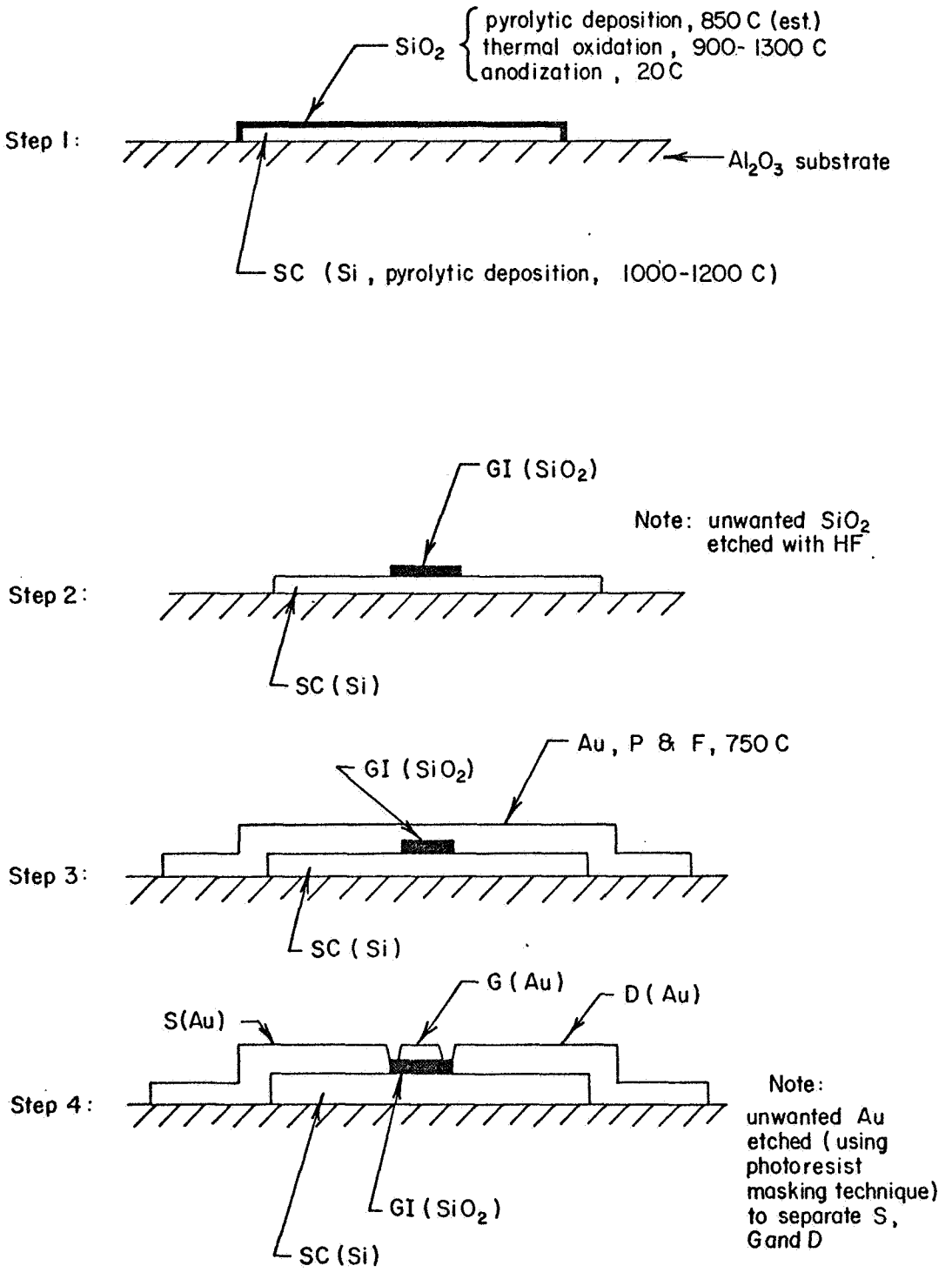


FIGURE 7. COPLANAR CONFIGURATION - MODEL 3
Semiconductor - Silicon; Gate Insulator - Silicon Dioxide; Source, Drain and Gate Electrodes - Gold

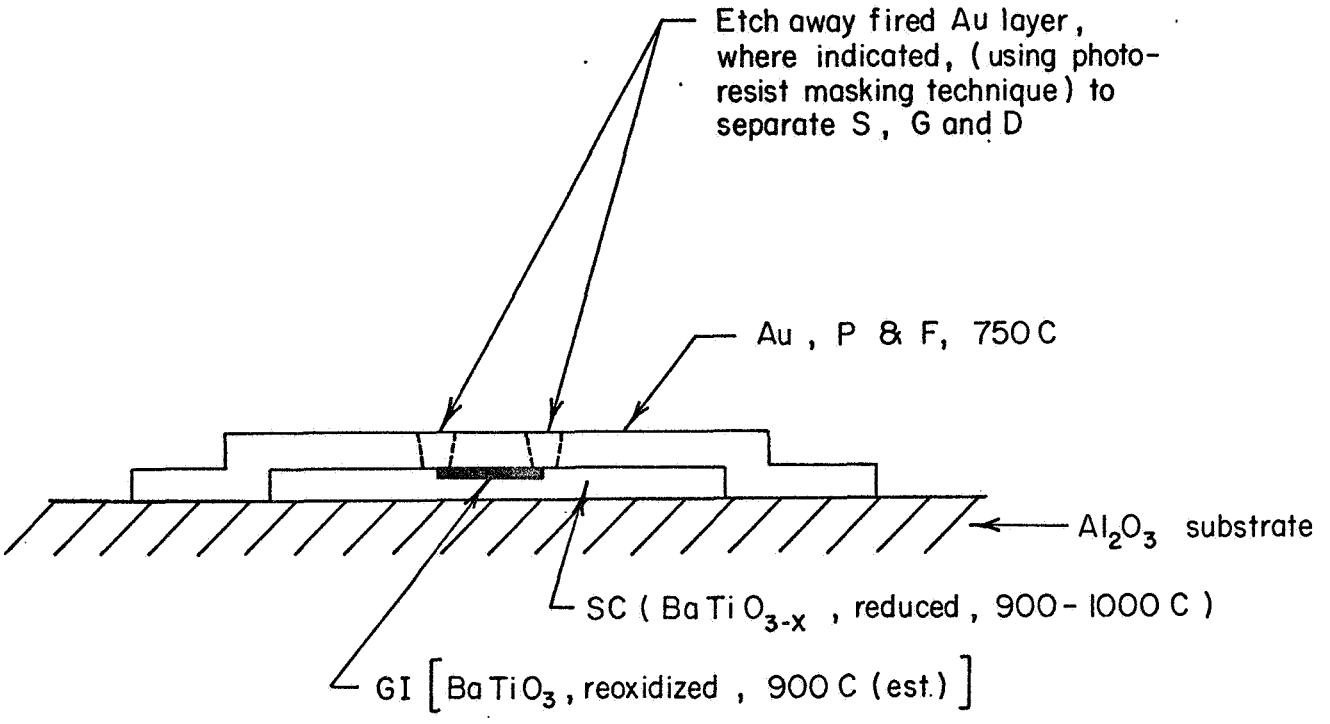


FIGURE 8. COPLANAR CONFIGURATION - MODEL 4
Semiconductor - Reduced Barium Titanate; Gate Insulator - Barium Titanate; Source, Drain and Gate Electrodes - Gold

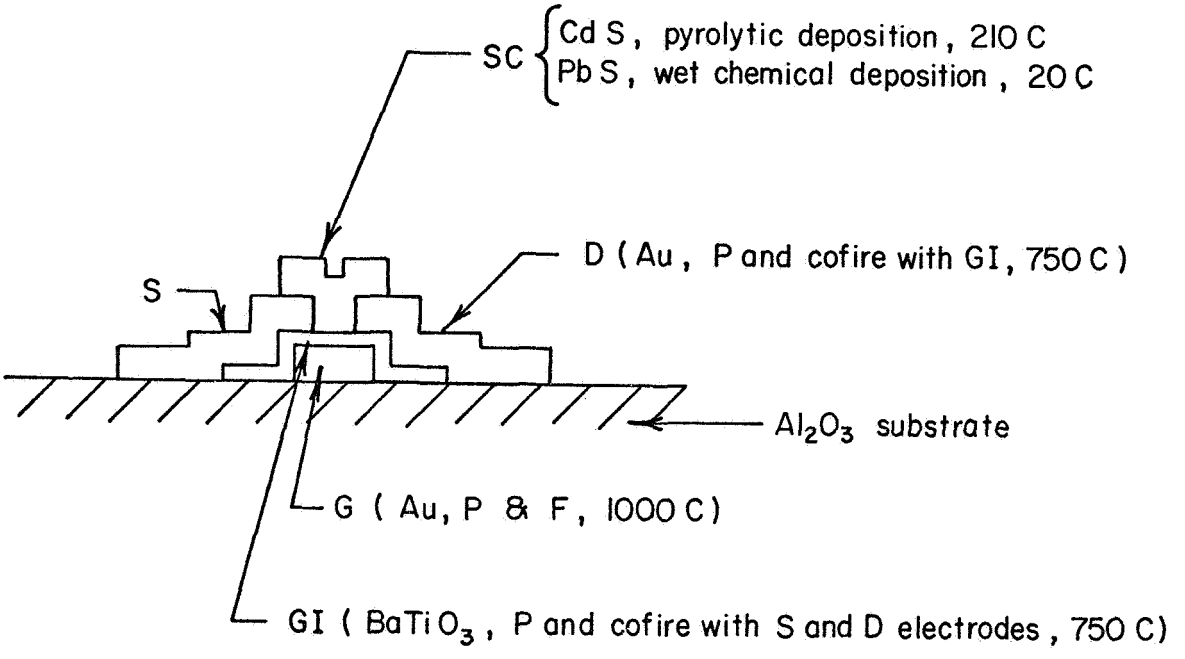


FIGURE 9. INVERTED-COPLANAR CONFIGURATION - MODEL 5
Gate Electrode - Gold; Gate Insulator - Barium Titanate; Source and Drain Electrodes - Gold; Semiconductor - Cadmium Sulfide or Lead Sulfide

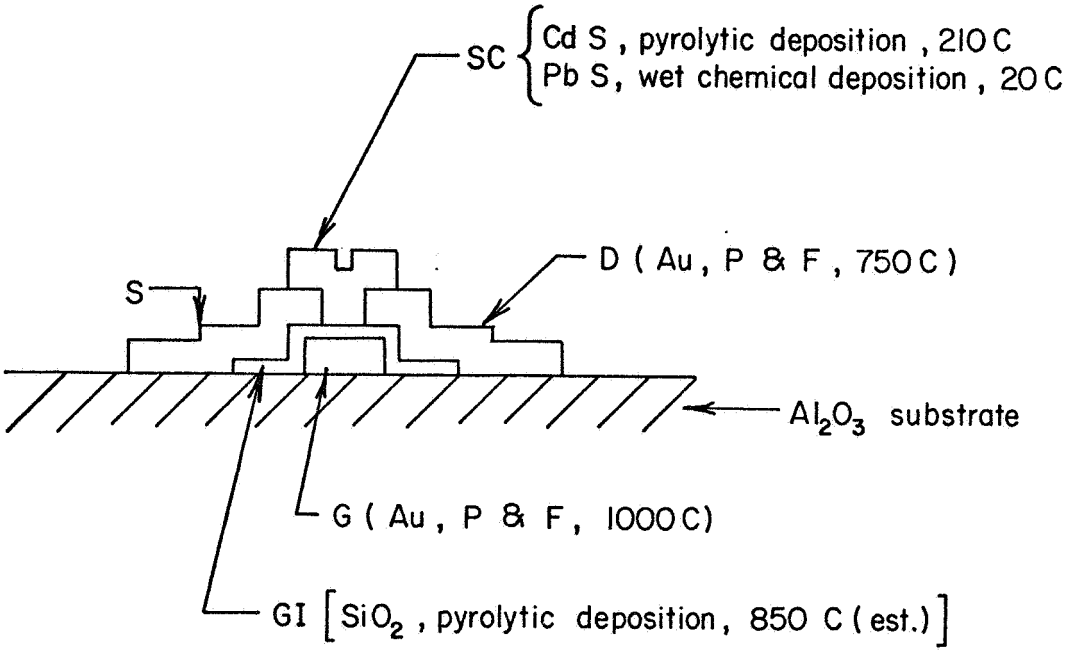


FIGURE 10. INVERTED-COPLANAR CONFIGURATION - MODEL 6
Gate Electrode - Gold; Gate Insulator - Silicon Dioxide; Source and Drain Electrodes - Gold; Semiconductor - Cadmium Sulfide or Lead Sulfide

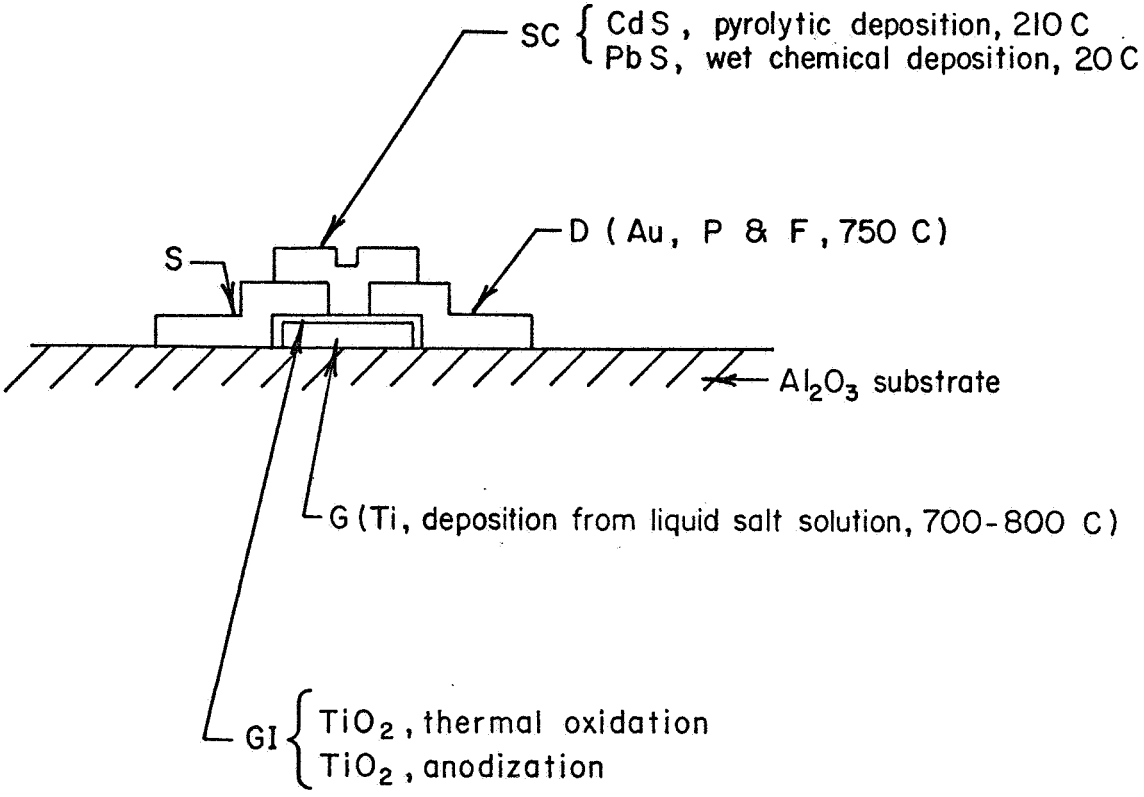


FIGURE 11. INVERTED-COPLANAR CONFIGURATION - MODEL 7
Gate Electrode - Titanium; Gate Insulator - Titanium Dioxide; Source and Drain Electrodes - Gold; Semiconductor - Cadmium Sulfide or Lead Sulfide

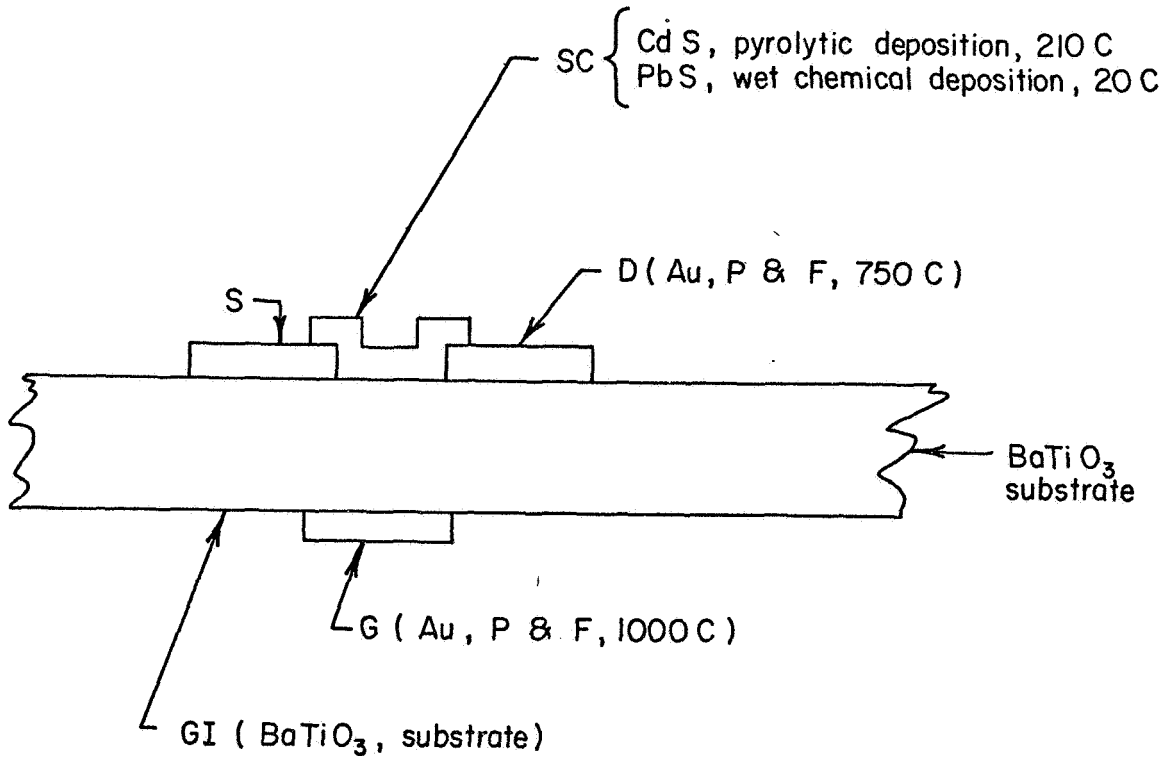


FIGURE 12. COPLANAR CONFIGURATION - MODEL 8
Gate Electrode - Gold; Gate Insulator - Barium Titanate; Source and Drain Electrodes - Gold; Semiconductor - Cadmium Sulfide or Lead Sulfide

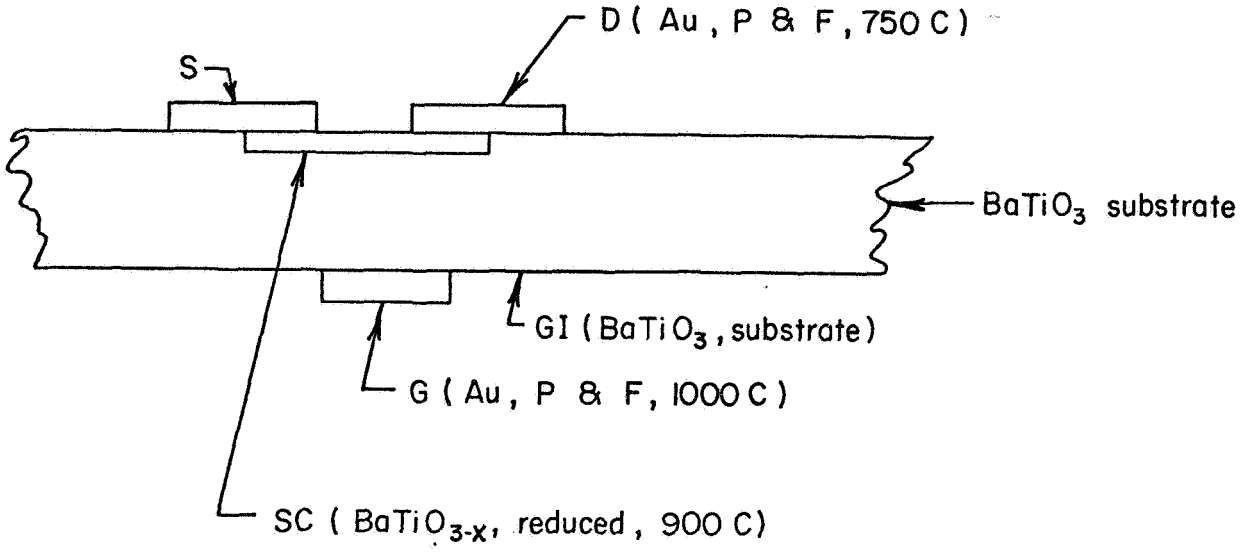


FIGURE 13. STAGGERED CONFIGURATION - MODEL 9
Gate Electrode - Gold; Gate Insulator - Barium Titanate; Semiconductor - Reduced Barium Titanate; Source and Drain Electrodes - Gold

DISCUSSION AND CONCLUSIONS

The criteria for application of solid state electronic technology to thick film compatible FET's described earlier in the report have been applied to various combinations of constituent materials, fabrication processes and device configurations. Those combinations (or models) which appear to have some potential for successful application were shown in Figures 5 through 13 and are listed again in Table 7. The nine models have been divided into three groups according to their likelihood of successful implementation.

The first group, comprising Models 5 and 6 (Figures 9 and 10), contain materials and processes representing the least deviation from standard thick film technology, and are deemed to have the highest potential for successful development. The second group, comprising Models 7, 8 and 9 (Figures 11, 12 and 13), contain either unconventional materials or configurations which increase the complexity of the processing procedure or introduce process steps that may require additional development for successful implementation. Associated with the third group, comprising Models 1, 2, 3, and 4, (Figures 5, 6, 7, and 8), are problems inherent in the device design that would severely limit the quality of their operation. Following is a discussion of the particular advantages and problem areas related to the models in each of the three groups.

Group 1

Model 5.-- The gate electrode, dielectric film, and source and drain electrodes are all deposited by standard thick film techniques. The semiconductor material - either CdS or PbS - is deposited by a low temperature process which should preclude the possibility of contamination from adjacent layers, which has been a problem in some of the higher temperature processes. A conventional substrate is used in this model and all materials are commercially available.

TABLE 7. COMBINATIONS OF MATERIALS, PROCESSES AND CONFIGURATIONS FOR THICK FILM IGFET'S

Model No.	Configuration	Semiconductor	Dielectric	Source & Drain Electrodes	Gate Electrode	Substrate	Reference Figure
1	Staggered	Si (pyrolytic deposition)	SiO_2 {pyrolytic deposition, thermal oxidation, anodization}	Ti (deposition from liquid salt solution)	Au (print & fire)	Al_2O_3	5
2	Staggered	$BaTiO_{3-x}$ (reduction)	$BaTiO_3$ (reoxidation)	Au (print & fire)	Au (print & fire)	Al_2O_3	6
3	Coplanar	Si (pyrolytic deposition)	SiO_2 {pyrolytic deposition, thermal oxidation, anodization}	Au (print & fire)	Au (print & fire & etch)	Al_2O_3	7
4	Coplanar	$BaTiO_{3-x}$ (reduction)	$BaTiO_3$ (reoxidation)	Au (print & fire)	Au (print & fire & etch)	Al_2O_3	8
5	Inverted-Coplanar	CdS (pyrolytic deposition) or PbS (wet chem. deposition)	$BaTiO_3$ (print and cofire)	Au (print & cofire)	Au (print & fire)	Al_2O_3	9
6	Inverted-Coplanar	CdS (pyrolytic deposition) or PbS (wet chem. deposition)	SiO_2 (pyrolytic deposition)	Au (print & fire)	Au (print & fire)	Al_2O_3	10
7	Inverted-Coplanar	CdS (pyrolytic deposition) or PbS (wet chem. deposition)	TiO_2 {thermal oxidation, anodization}	Au (print & fire)	Ti (Lockheed process)	Al_2O_3	11
8	Coplanar	CdS (pyrolytic deposition) or PbS (wet chem. deposition)	$BaTiO_3$ (substrate)	Au (print & fire)	Au (print & fire)	$BaTiO_3$	12
9	Staggered	$BaTiO_{3-x}$ (reduction)	$BaTiO_3$ (substrate)	Au (print & fire)	Au (print & fire)	$BaTiO_3$	13

Among the limitations or problems to be resolved concerning Model 5 are the following:

(1) Definition of the area of the semiconductor material bridging the source and drain electrodes would be required either by some scheme of selective application of the semiconductor or by applying the semiconductor over the entire surface and selectively etching the material from the unwanted areas.

(2) Limitations on the thickness tolerance of the $BaTiO_3$ gate insulator applied by thick film techniques may be sufficiently severe to result in appreciable variability of the gate capacitance for a given gate voltage from device to device.

(3) The width and uniformity of the source-to-drain spacing will be limited by the state of the art of thick film technology.

(4) Applying both the gate electrode and gate insulator by screen printing and firing may result in a semiconductor-dielectric interface of sufficient roughness to cause appreciable local variations in the field strength.

(5) Contact resistance between the gold source and drain electrodes and the semiconductor could be a problem requiring some experimentation.

(6) As hypothesized in reference (10), the ferroelectric nature of $BaTiO_3$ might present a problem.

Model 6.-- Model 6 is the same as Model 5 with the exception of the gate insulator, which in this case is a pyrolytically deposited film of SiO_2. Although the pyrolytic deposition step represents an added complexity to the processing procedure, Model 6 would be recommended if problems such as the ferroelectric nature of the $BaTiO_3$ layer precluded its use. It would be anticipated that the SiO_2 would be deposited over the entire substrate containing the gate electrodes and would be selectively removed with photolithographic masking and etching. The rate of deposition and hence the film thickness could be closely controlled.

Group 2

Model 7.-- Model 7 consists of a titanium gate electrode applied to an alumina substrate by a deposition process such as that described in reference (51); a gate insulator formed by anodization or thermal oxidation of the gate metal; and the same arrangement for source and drain electrodes and semiconductor as in Models 5 and 6. Model 7 has the advantage of providing a thin dielectric layer of controlled thickness. The smoothness of the dielectric layer in this case would be expected to be limited by the smoothness of the substrate. The referenced deposition technique, however, is relatively untried, and a number of potential problems associated with it would need to be resolved. As in the case of the pyrolytic deposition of SiO_2, it would be required either to apply the material to the entire surface of the substrate and selectively remove the unwanted regions, or to develop masking procedures for depositing the extremely small geometries required for the gate electrodes. If etching were required for film removal, the problems of compatibility of the masking material with the etchant and of undercutting the narrow gate regions would need to be considered. If the insulating oxide is grown anodically, the compatibility of the interfacial bond with the electrolyte would be of concern; and if the oxide were grown thermally, the integrity of the bond at the oxidation temperature would need to be verified.

Model 8.-- Model 8 utilizes the substrate material as the gate insulator. The source, drain and gate electrodes are applied by conventional screen printing and firing and the semiconductor is the same as described in the previous models. While this model represents a simpler processing procedure in that the separate application of a gate insulator is not required, additional complications are associated with the necessity of applying the gate electrode on the opposite side of the substrate from the source and drain electrodes. Specifically, the advantage of a visual check on alignment is lost; and because of tolerance limits on substrate size and shape, separate sets of registration pins would probably be required so that the same sides and angles of the substrate could be used for alignment when printing on each side. The requirement for the gate electrode to be on the opposite side of the substrate from the source and drain electrodes

could be an advantage or a disadvantage depending on circuit design. If all the circuit were designed for one side of the substrate, feed-throughs or other means would be needed to provide contact to the gate electrode. Because of tolerance limits on substrate thickness, appreciable variation from device to device might be expected to occur in the field strength at the semiconductor-dielectric interface for a given gate voltage. To maintain the gate capacitance in the range of that required for successful TFT operation, a dielectric constant K of 2500 would be required for a 10 mil thick substrate. Values of $K > 2000$ at room temperature have been reported for polycrystalline $BaTiO_3$ formulations.[62] Both the availability and cost of such materials would represent disadvantages over the more conventional substrate materials. Additional disadvantages of the $BiTiO_3$ substrate material might include the possible nonuniformity of the dielectric constant and the ferroelectric nature of the material.

Model 9.-- Model 9 is a variation of Model 8, both incorporating the substrate as the gate insulator, and requiring the gate electrode to be on the opposite side from the source and drain electrodes. In Model 9, however, the semiconductor film is formed by reducing selected areas of the insulating $BaTiO_3$ substrate to form semiconducting $BaTiO_{(3-x)}$. To form semiconductor areas in the substrate, it would be required either to develop a mask that could withstand the high temperature reducing environment or to reduce the entire surface of the substrate and remove material from the unwanted areas by etching.

Group 3

Models 1 and 2.-- The unique aspect of the fabrication of Models 1 and 2 is associated with the semiconductor and gate insulator. In Model 1, the semiconductor is a pyrolytically-deposited layer of polycrystalline silicon and the gate insulator is either a thermally or anodically grown layer of SiO_2. Thin layers of silicon and SiO_2 with closely controlled thicknesses could be produced by this method. However, a considerable amount of silicon technology would be required in order to grow silicon films with

controlled physical and electrical properties. Applied to ceramic substrates, the smoothness of the films would be limited by the smoothness of the substrates. Also, the contact resistance between the silicon and the titanium electrodes would be a matter of concern.

In Model 2, the semiconducting $BaTiO_{(3-x)}$ layer is to be formed by printing a $BaTiO_3$ thick film paste and firing it in a reducing atmosphere at about 900 C. The gate insulator would be formed by reoxidizing the surface region of the reduced barium titanate layer. Although the forming of semiconducting barium titanate from the insulating material by hydrogen reduction and the forming of insulating barium titanate from the semiconducting material by oxidation are well-known processes, such modifications have not been carried out, to our knowledge, with barium titanate thick film pastes. The feasibility of the oxidation and reduction processes in thick films of barium titanate, therefore, is in question; and it is to be expected that some research would be required to develop appropriate oxidation and reduction procedures for the material in paste form. Assuming the reduction of a $BaTiO_3$ thick film paste and the subsequent oxidation of its surface region is feasible, the achievable thicknesses and thickness control of the dielectric layer are more in question than in the case of Model 1, since less is known about the oxidation process for reduced barium titanate than about the oxidation process for silicon. Also, as in the case of Model 1, the contact resistance between the semiconductor and the source and drain electrodes might prove to be a problem.

Common to Models 1 and 2 is the staggered configuration in which the current carriers are required to pass through the thickness of the semiconductor layer in their transit between the enhanced region of the semiconductor-dielectric interface and the source and drain electrodes. The associated high series resistance would be expected to limit the performance of a device designed to operate in the enhancement mode, particularly in Model 2 where a thicker semiconductor layer is used.

Models 3 and 4.-- Models 3 and 4 incorporate no new material combinations, but are characterized by a coplanar arrangement for the source, drain and gate electrodes in which the electrode layer is laid down as a

single film and separation of the electrodes is achieved by etching. A screen printing and firing technique is envisioned for electrode deposition, and etching of the film would be accomplished utilizing photolithographic masking procedures. It is anticipated that work would be required to develop appropriate etchants and etching procedures for the thick film conductor materials. Inherent in the design of Models 3 and 4 is a coplanar gap between the gate and the source and drain electrodes under which the semiconductor would not be modulated by the gate electrode. This unmodulated region would represent a high series resistance to the modulated semiconductor under the gate electrode and would be expected to severely limit the performance of a device designed for operation in the enhancement mode.

In conclusion, the models in Group 1 represent minimal departure from standard thick film technology and are recommended as having reasonable potential for successful development. The models in Group 2 represent a significant but not incompatible departure from thick film technology and include process steps that may require considerable continued development for successful implementation in a thick film device. The models in Group 3 represent configurations incorporating an unmodulated component of the semiconductor material between the source and drain electrodes which would comprise a high series resistance and thus seriously limit the performance of a device designed for operation in the enhancement mode. The models in Group 3, therefore, are not recommended for implementation.

APPENDIX I. RECOMMENDATIONS FOR FUTURE RESEARCH

As indicated in the Discussion and Conclusions section, transistor Model 5 represents an all thick-film process with the exception of the last step which is the application of the semiconductor film. The recommended semiconductors are either cadmium sulfide, applied by a low temperature pyrolytic deposition process or lead sulfide applied by a room temperature, wet chemical deposition process. Thin film FET's have been operated using each of these semiconductors. (Cadmium sulfide, of course, has been far more intensively exploited.) Of those approaches to the design of a thick film FET conceived in this study, the procedures relating to the fabrication of Model 5 digress the least from conventional thick film electronic technology. It would thus appear that if a satisfactory device could be developed on the basis of the general concepts of that model, existing thick film technology would be perturbed the least. It is concluded that the chances for successful development of a device on that basis are sufficiently high to warrant consideration of exploratory experimental work. In pursuing such a program, it may be expected that several problem areas will require investigation. Among them are the following:

(1) It would be required to develop a means for appropriately positioning the semiconductor over the source and drain electrodes. This might be accomplished by a masking procedure during film deposition to apply the film only in the appropriate areas, or by depositing the film over the entire surface and removing it from the unwanted areas by a masking and etching procedure.

(2) The compatibility of the semiconductor and contact materials would have to be determined. Because of the low-temperature deposition process for the CdS, it is not envisioned that contamination from the thick film gold electrodes would be a problem. However, experimental verification would be

required. The problem of contact resistance between the electrodes and semiconductor may be of concern also. If contact resistance did prove to be a problem, either replacement of or modification to the electrode materials would be required.

(3) Apart from possible problems arising from the ferroelectric properties of barium titanate, it is possible that limitations on thickness control of the barium titanate gate insulator as well as surface roughness problems on the gate electrode and the gate insulator will prove important. Depending upon their severity, they may lead to appreciable variability in operating characteristics from device to device. The dimensions and significance of this problem must be clarified by experimentation.

(4) Also significant in the uniformity or reproducability of device characteristics will be the precision with which the source-drain spacing can be reproduced using thick film techniques. Here again, experimentation will be required. The degree to which this matter is a problem will be dependent, in part, upon the quality of transistor characteristics being sought. For example, if a given transconductance can be achieved with a source-drain spacing of ten mils, then a given limit on the achievable precision in source-drain spacing will be less significant than if the required transconductance demanded a source-drain spacing of three mils.

(5) A further consideration relating to reproducibility of devices will be the need for and ability to

reproduce critical electrical properties of the deposited semiconductor layer. Properties of primary concern here will be conductivity type, free charge carrier density, effective mobility and the electronic properties of the surface. It is known, of course, that the properties of both CdS and PbS films can be intentionally varied. It is also known that unintentional variation in properties can occur. The degree to which a necessary level of control can be maintained in the structure of Model 5 and the associated fabrication processes must also be evaluated experimentally in the light of transistor requirements.

At some stage, most of these individual areas of investigation can profitably be pursued on a somewhat isolated basis. It seems evident, however, that individual experimentation with specific aspects of the overall problem should be preceded by some exploratory work involving fabrication of complete transistors. It would appear that only in this way can those problems which represent the most fundamental limitations to ultimate success be identified both in nature and in severity.

With respect to the other transistor models discussed, particularly those in groups 2 and 3, a number of problems peculiar in some way to a particular model or to a particular process called for in the model have been called out in the Discussion and Conclusion section. Apart from those special considerations, it is reasonable to expect that details of the sort mentioned above in connection with transistor Model 5 will be of equal significance in the development of a device based on any one of the other models. If there is any problem area common and unique to the concept of a thick film transistor, that problem is the one associated with the possible roughness of various surfaces and the effect of that roughness on the uniformity and quality of performance of the gate insulator function. Should that problem prove insurmountable by any adaptation of conventional practices, then consideration could be given to the utilization of glazed substrates or other such modifications. Their use could be evaluated in

relation to need and to their possible perturbations on established thick film fabrication technology.

The possibility of developing a practical thick film transistor would be an interesting and a challenging undertaking. A technical evaluation of concepts upon which to base such a transistor leads to the conclusion that the pursuit of such a development is justified. An evaluation of the matter from an economic point of view is more difficult to make. It probably cannot be made validly without some information to be obtained from experimental investigation as well as from considerations of the breadth of application of the desired transistor. By way of simple example, initial experimental work for one reason or another might lead to the conclusion that a major development program would be required in order to achieve a satisfactory device. The wisdom of such a long-range development would have to be judged in the light of the needs for that transistor and the benefits which would accrue from it in contrast to using silicon chip devices in a hybrid thick film circuit configuration. Full consideration of these aspects of the desirability of thick film transistor development are beyond the scope of the present study and as indicated above depend upon some information not presently at hand with respect to the utilization and control of various fabrication procedures.

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