N69-13087

NASA CR-72455
WAED 68.37E

PARALLEL OPERATION OF STATIC INVERTERS AND CONVERTERS AND EVALUATION OF MAGNETIC MATERIALS

by

C. L. DOUGHMAN

prepared for

NATIONAL AERONAUTICS AND SPACE ADMINISTRATION

CONTRACT NAS3-2792

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SUMMARY REPORT

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AUGUST 1968

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PREFACE

Technical Manager of this program for the NASA Lewis Research Center was Mr. Francis Gourash.

The entire program "Parallel Operation of Static Inverters and Converters and Evaluation of Magnetic Materials" is reported in four reports and a summary report.

"Inverter-Converter Parallel Operation" (ref. 1) defines and experimentally verifies the circuit conditions that must exist for operating static inverters and static converters in parallel.

"Inverter-Converter Automatic Paralleling and Protection" (ref. 2) defines and experimentally verifies the electrical control and protection circuits necessary for isolating faulted inverters and converters from a parallel system while maintaining continuity of high-quality electric power to load equipment.

"Evaluation of Magnetic Materials for Static Inverters and Converters" (ref. 3) defines the magnetic characteristics of improved materials for magnetic components as applied in advanced static inverters or static converters.

"Load Programmer, Static Switches and Annunciator for Inverters and Converters" (ref. 4) assesses the characteristics of static electrical switches for both ac and dc systems; defines the characteristics of a load programmer for maintaining power to the critical system loads, and provides an annunciator function for displaying inverter and/or converter operating conditions.

"Parallel Operation of Static Inverters and Converters and Evaluation of Magnetic Materials," summarizes the four reports of this program (NASA CR-1224, 1225, 1226, and 72454).

PARALLEL OPERATION OF STATIC INVERTERS AND CONVERTERS AND EVALUATION OF MAGNETIC MATERIALS

By C. L. Doughman

ABSTRACT

This report summarizes the design, analysis, and development work of four other reports relating to the ability to operate static inverters or converters as parallel electric power systems. In addition, data on several magnetic materials are generated for square-wave excitation at frequencies ranging from 400- to 3200-Hz. Areas described are the analysis and design of load-division circuits for inverters and converters, the establishment of automatic control and protection philosophy and circuits, the development of static-power contactors, and the initial study of load programming as a means of improving load capacity of parallel electric power systems.

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PARALLEL OPERATION OF STATIC INVERTERS AND CONVERTERS AND EVALUATION OF MAGNETIC MATERIALS

By C. L. Doughman

SUMMARY

The results of this program may be separated into two general categories. The first category is the establishment of design information on various magnetic materials as they are applied to circuits in static conversion equipment. Materials evaluated were: 4%Mo-79%Ni-17%Fe, 50%Fe-50%Ni, magnetically annealed 49%Co-2%V-49%Fe, singly and doubly oriented silicon steel. These materials were tested under dc excitation and 400- to 3200-Hz square-wave excitation. The data presented include hystersis loops, core loss, apparent power, and magnetization curves, at temperatures ranging from -55° C to +250° C. Constant-current flux reset data were obtained at room ambient. In addition to these data, the effects of vacuum exposure at 250° C and the effects of several conventional processing steps on magnetic properties are evaluated. These data represent the first comprehensive compilation of data on magnetic materials operating under the above conditions.

The second category is the development of complete static ac and dc parallel electric power systems. The development included the following system components: automatic control and protection circuits, visual annunciators, load programmers, and static circuit breakers. In addition to these system components, circuits for paralleling and load division among paralleled conversion equipment were developed for previously developed inverters and converters. The results of the paralleling and load division circuits include the methodology of determining both analytically and experimentally the internal impedance of a static inverter, the necessary conditions to establish parallel operation, and the actual circuits required to force division of load among paralleled inverters and converters. These concepts were tested on two 750-volt-ampere inverters and two 750-watt converters. The results of the test program verified the analytical work.

Using the characteristics of the conversion equipment, additional system components were developed. These components included automatic paralleling, contactor control, visual annunication, and protection features. The protection circuits included frequency reference protection, over- and underfrequency (for ac systems only), over- and undervoltage, load-division protection, overcurrent, and differential-current protection. In addition, two new control features were developed. One was a zero-impedance, static switch and the other was an automatic synchronizer. The zero-impedance

switch was developed for the very low differential voltages in the load-division control circuits of paralleled converters. The switch performs the function of disabling the load-division circuit when converters are not operating in parallel. The automatic synchronizer forces an on-coming inverter into phase with the parallel system so that no frequency transients are introduced when the inverter is paralleled to the system. All these systems components were tested in a two-channel parallel system. All functions operated satisfactorily. A load-programming concept is developed to work in conjunction with the developed control and protection circuits. The concepts developed appear feasible with either relay or solid-state control; however, no hardware was built and tested.

Characteristics and experimental test results of a three-phase static switch and a dc switch are analyzed. Circuit interruption times of less than three milliseconds are obtained for current loads up to 250 percent of rated value. The results of the development program showed the static switch exhibited faster response, repeated cycling, no arcing, longer life, and higher reliability than an equivalent electro-mechanical relay. However, the static switch is heavier, larger, and less efficient.

INTRODUCTION

This report summarizes the four reports which describe the development of a parallel ac and a parallel dc static electric power system and the evaluation of magnetic materials for static inverters and converters. The need for parallel systems is the consequence of larger power demands due to more complex and longer-duration space missions. The longer duration of space missions also demands a more reliable source of power for critical spacecraft loads. Rather than meet these demands with static power conditioning equipment of ever-increasing capacity and complexity, methods of paralleling already-developed conversion equipment were developed.

Because it was not known whether the present technology of paralleling electromechanical generators applied directly to static inverters, it was first necessary to determine that static inverters and converters could be reliably paralleled. The results of this investigation are described in report NASA CR-1224, "Inverter-Converter Parallel Operation" (ref. 1).

In order to eliminate the need for continuous manual surveillance and control of the power system, a means of automatically controlling and protecting the parallel system was needed. Circuit concepts developed and tested to accomplish this end are described in report NASA CR-1225, "Inverter-Converter Automatic Paralleling and Protection" (ref. 2). A further extension of system control and monitoring is provided with concepts of load programming, static power switches, and visual annuciation. These concepts are described in report NASA CR-72454, "Load Programmer, Static Switches, and Annunciator for Inverters and Converters" (ref. 4).

Because magnetic components substantially contribute to the size, weight, and losses of static conversion systems, the magnetic materials of these components were intensively investigated to determine the possible means for improving performance. The investigation included the effects of waveform, frequency, temperature, vacuum, and fabrication variables on the performance characteristics of five ferro-magnetic alloys. The results of this investigation are described in report NASA CR-1226, "Evaluation of Magnetic Materials for Static Inverters and Converters"(ref. 3).

These investigations have advanced the state of the art of spacecraft electric power systems. Of especial significance is the parallel operation of static converters and inverters, the obtaining of data on ferro-magnetic materials at high frequencies, and the development of methodology for the analysis of this type system.

INVERTER-CONVERTER PARALLEL OPERATION

The objective of this program (ref. 1) were to mathematically develop the means and criteria for paralleling static inverters and converters with equal load division among the paralleled units. And to prove the concept by operating two inverters and two converters in two separate parallel systems.

The static inverters can be paralleled if the following four criteria are met:

1) all inverters must operate at the same frequency;
2) the internal voltages must be in phase;
3) the nominal regulated voltages must be equal;
4) a means of ensuring proper load division must be available.

To determine the circuits necessary for dividing load among paralleled inverters, the characteristics of the internal impedances of the inverter must be defined. Therefore, several approaches to describing these impedances are presented in reference 2. The following two equations show how the unbalanced real and reactive currents are affected by the internal impedance of the inverter.

$$R(\dot{I}_1 - \dot{I}_0) \doteq \frac{\Delta E}{Z_1} \cos (\theta_0 - \theta_1) - \frac{E_0 \Delta \theta}{Z_1} \sin (\theta_0 - \theta_1) \qquad (1)$$

$$Q(\dot{I}_1 - \dot{I}_0) \doteq \frac{\Delta E}{Z_1} \sin (\theta_0 - \theta_1) - \frac{E_0 \Delta \theta}{Z_1} \cos (\theta_0 - \theta_1) \qquad (2)$$

where

$R(\dot{I}_1 - \dot{I}_0)$ is the component of unbalanced current among paralleled inverters that is in phase with the bus voltage.

$Q(\dot{I}_1 - \dot{I}_0)$ is the component of unbalanced current among paralleled inverters that is in quadrature with the bus voltage.

E_0 is the magnitude (rms) of internal voltage of an inverter adjusted so that differential current is zero.

θ_0 is the angle between a referenced terminal voltage and the internal voltage, E_0.

$\dot{Z}_1 = Z_1 \underline{|\theta_1}$ is the magnitude and phase angle of inverter internal impedance.

ΔE and $\Delta \theta$ are incremental quantities.

If the difference angle $(\theta_0 - \theta_1)$ were zero degrees, the phase angle of E_0 would control the reactive component of the load current. If $(\theta_0 - \theta_1)$ were 90 degrees, the magnitude of E_0 would control the reactive component of load current. However, in the general case of static inverters, neither condition exists. In order to compensate for this, a reference phasor was developed to force a 90 degree relationship. The angle of the reference vector, θ_2, is approximately equal to $90 + \theta_0 - \theta_1$ degrees. Since 90 degrees was chosen, the phase angle of E_0 determines the division of real load (equation 1), and the magnitude of E_0 determines the division of reactive load (equation 2).

Figure 1 shows the internal impedance, $\dot{Z}_1$, of the test inverters. Figure 2 shows the complete reactive-load-division circuits for two paralleled inverters. The transformers T27 and T28 and impedances R64, R65, R66, and C21 provide the reference vector angle, θ_2.

Because the frequency of inverters is usually determined by reference oscillators, it is an easy matter to operate several inverters from a single oscillator. Hence, all inverters would operate at the same frequency, eliminating the need for feedback circuits among several oscillators. Since the phase of the internal voltage controls the real portion of the load, a means of assuring phase relationship of the paralleled inverters must be incorporated. The reference oscillator and countdown circuit

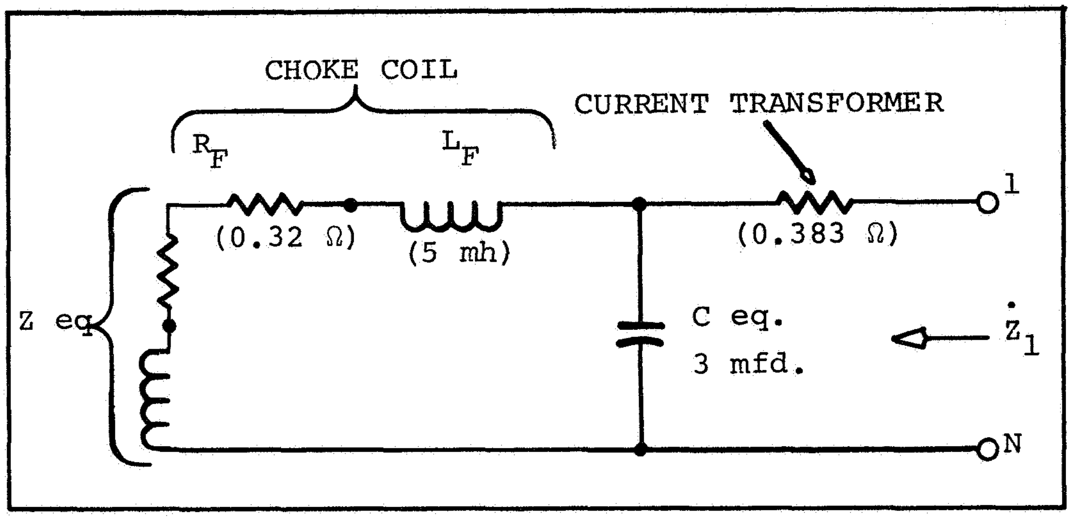


Figure 1. - The Equivalent Circuit for Internal Impedance of a Static Inverter Under Balanced Load Conditions

determines the phase within a single inverter, so a synchronizing signal was established to force or lock the paralleled inverters in phase. This removed the need for analog feedback signals to establish real load division.

The static converters can be paralleled if the following two criteria are met:

1) the nominal regulated voltages must be equal;

2) a means of ensuring proper load division must be available.

Paralleling static converters is somewhat simpler than paralleling static inverters because no frequency or phase relationships must be established. The sharing of load among paralleled converters is accomplished by sensing the bus voltage and the current from each converter. The unbalanced current is determined and the unbalance information controls the magnitude of internal voltage to restore balance. The converter load-division circuit is, therefore, very similar to the reactive-load-division circuit of the inverter. Figure 3 shows the load-division circuits for two parallel converters.

The load-division circuits developed are applicable to any number of paralleled units, and any reasonable load-division requirement can be met. The results of the developed technology provide a framework for applying any configuration of static inverter or converter to a parallel system. The technology either will be directly applicable to specific types or will provide a good basis for whatever variations in converters or inverters occur.

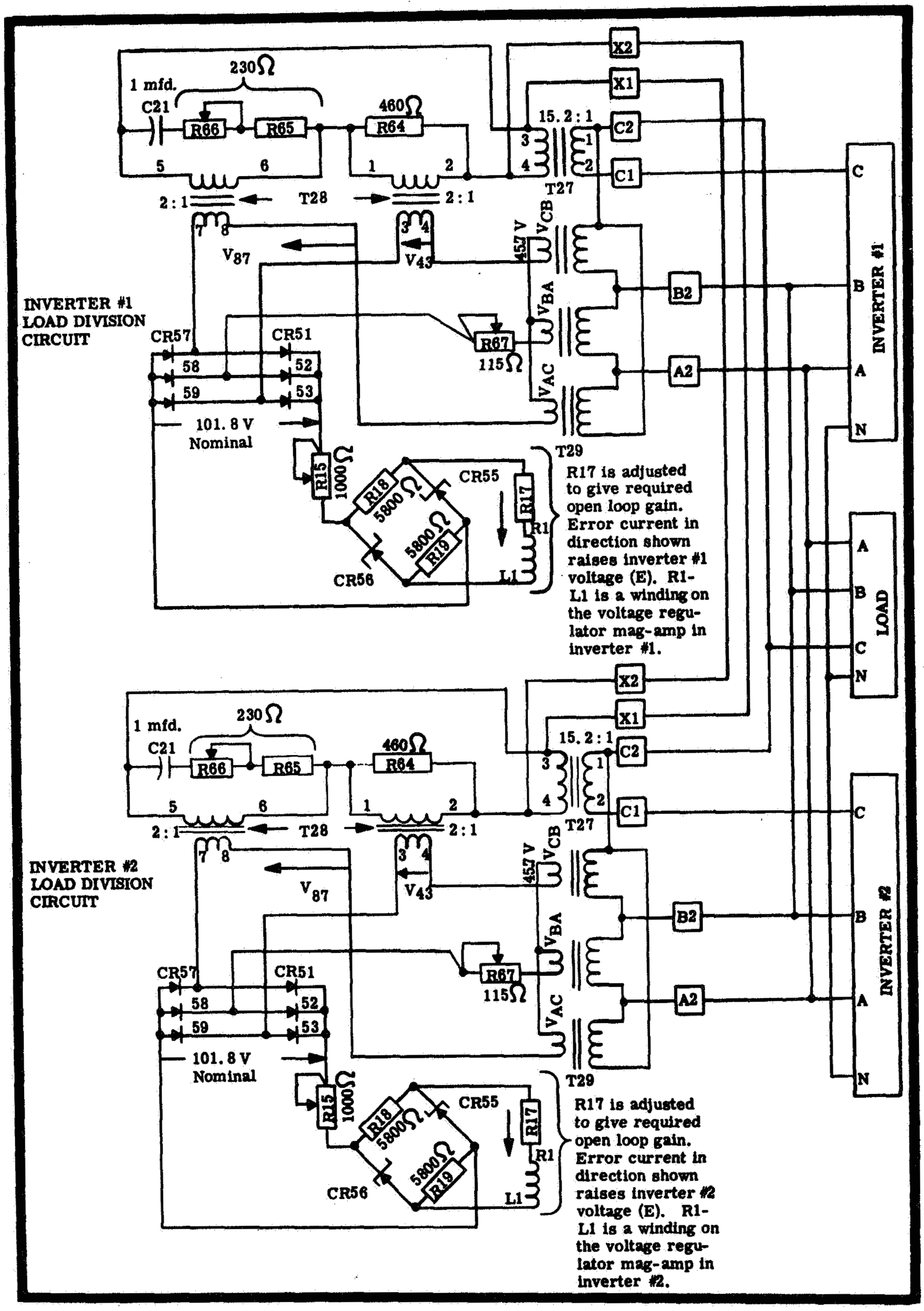


Figure 2. - Two Inverter Block Diagrams Connected in Parallel with AC Load Division Circuits Shown

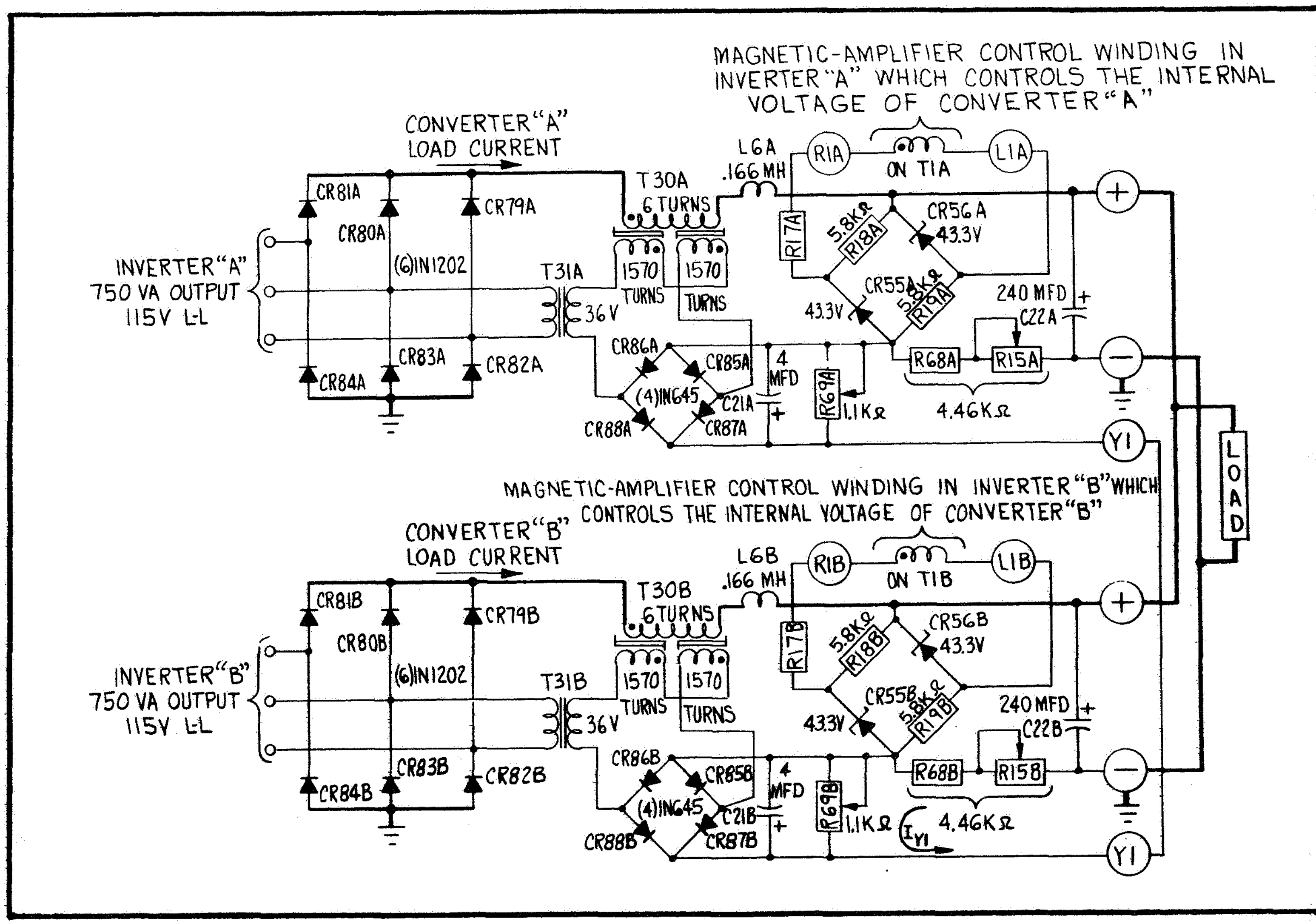


Figure 3. - Schematic Diagram of the Converter Load-Division Circuit

Both paralleled converters and inverters were tested using two 750-VA units. Each system was tested under balanced and unbalanced loading, motor starting, and load-bus faults. The systems operated within specifications. The paralleled units divided load well within the 10 percent initially specified. The good correlation between the experimental data and calculated values indicates that the analytical techniques developed during this study are valid.

INVERTER-CONVERTER AUTOMATIC PARALLELING AND PROTECTION

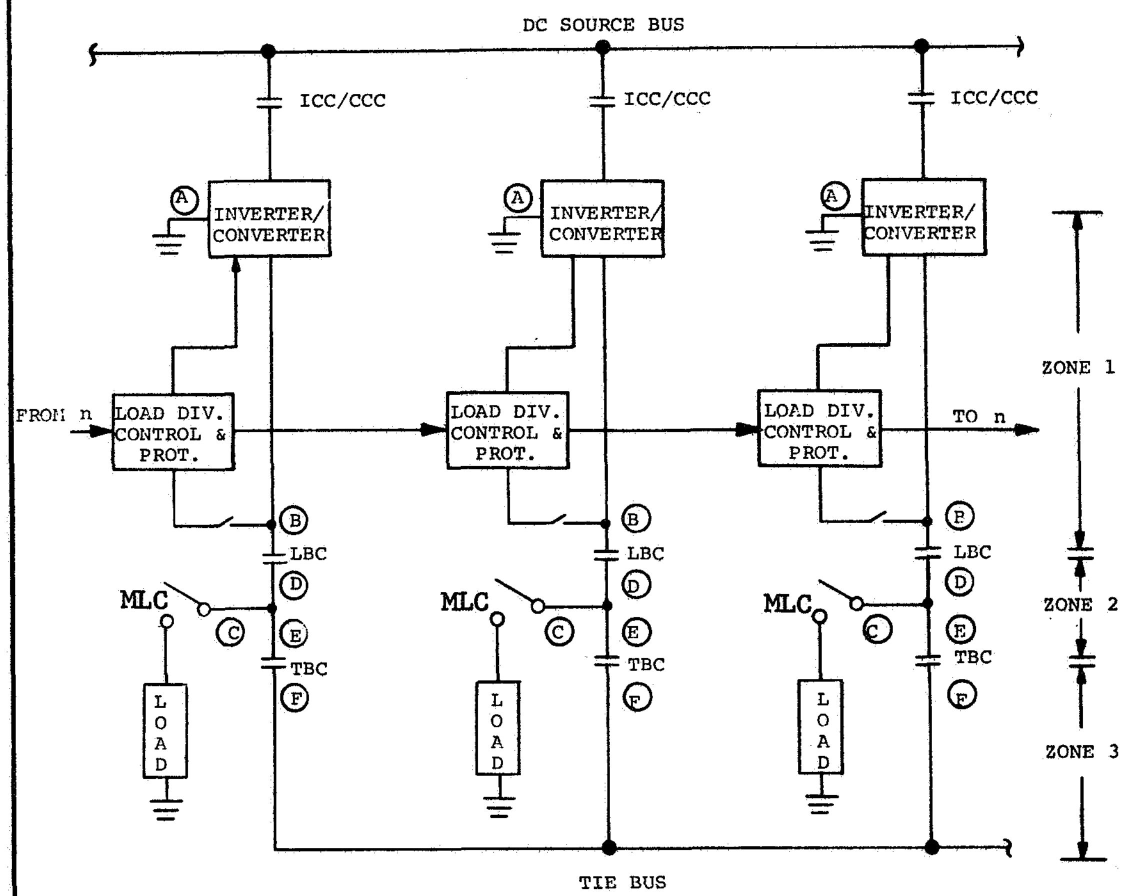
The objective of this program was the development of practical circuits for controlling and protecting inverters and converters in a paralleled electrical system (ref. 2).

If reliable parallel operation of a multi-channel electric power system is to be achieved, a means must be realized for interconnecting these channels so that channels can be added or removed with minimum disruption to the system loads. Figure 4 shows the interconnection scheme chosen.

The control and protection circuits are automatic, thus minimizing human error in the operation of the system. The control and protection circuits are arranged so that each channel has its own control and protection circuits. Sequencing circuits within each channel provides the means to operate in unison. This feature also allows each channel to operate in either an isolated or a paralleled mode of operation. Provisions are also included to allow a system operator to operate the parallel system independent of the control and protection circuits.

Control features included in the control and protection circuits are automatic paralleling and closure of the contractors shown in figure 4. For the inverter system, automatic paralleling includes the assurance that system frequency is proper, that the voltages are in phase, and that the magnitude of the voltages is within nominal limits. For the converter system, automatic paralleling includes the assurance that the magnitude of the voltages is within nominal limits as well as provisions to connect the initial converter to the system tie bus.

The basic function of the protection circuits is not to correct a faulty condition, but to isolate the fault from the rest of the system. Because such transient disturbances as load switching, system startup, and operation of secondary protection (fuses and thermal circuit breakers) result in temporary abnormal conditions, the protection circuits are designed to override them. Hence, action is taken only on faults persisting beyond normal system transients.



Symbols

ICC/CCC - DC Input Contactor
LBC - Load Bus Contactor
TBC - Tie Bus Contactor
MLC - Manual Load-Control Switch

Figure 4. - Parallel System Line Diagrams

Faults occuring within the inverter or converter affect the quality of power delivered to the loads. These faults include: over- and undervoltage and, for the inverter, over- and underfrequency. Faults occuring on the interconnecting system are caused by short circuits, ground faults, or severe overloads on the load busses. These abnormal current faults include differential-current faults, load-bus overcurrent, and tie-bus overcurrent. The current-sensing and logic circuits within the protection circuits monitor currents in each of three zones (see figure 4) to determine the location of an abnormal current. Zone 1 is monitored by differential-current protection, zone 2 by load-bus overcurrent protection, and zone 3 by a combination of inverter/converter overcurrent protection and load-bus overcurrent protection. A third class of fault is the load-division fault. This fault occurs when the regulation or load-division control circuits within the unit fail to maintain load division within a specified limit. A fourth type fault for inverter systems is the failure of the reference oscillator circuits. Since the reference oscillator affects the frequency of all inverters, it is monitored in addition to the output frequency of each inverter. The action when a failure occurs is to transfer immediately to a standby reference oscillator.

To determine when one of the above fault conditions exists, the system voltages, currents, and frequency are converted to sensed voltages by various circuits which include current transformers, voltage dividers, potential transformers, magnetic-amplifier circuits, and resistor-capacitor charging circuits. The output of these circuits provide a voltage signal proportional to the sensed parameter. These analog signals are converted to digital signals by comparing the sensed voltage to a reference voltage. These digital signals are then processed by the logic circuit.

The logic functions include combinational logic (AND's and OR's), sequential logic (time delays), and memory function (circuits capable of a sustained signal when the setting signal is removed, such as a flip-flop). The proper arrangement of these logic functions was determined by analyzing the types of system faults and the prescribed action. This information was tabulated in the form of a truth table which resulted in the final logic circuits. Tables 1 and 2 are the truth tables used to develop the complete control and protection circuits for the parallel inverter and parallel converter systems.

Two models of each control and protection circuit, fabricated to test the theory, were installed in the parallel converter and parallel inverter systems described in NASA CR-1224 (ref. 1). Each circuit function was tested by actual faults applied to the parallel system. The control and protection circuits generally met the requirements set forth.

Table 1. - Truth Table for Inverter Control and Protection

Symbol	Independent Variable	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19
A	MOS-AUTO	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	
B	ICS-CLOSE	1																		
C	ICS-TRIP		0	0	0	0														
D	OV		1				0			1								1		
E	UV Protection			1			0				1									
F	OF				1		0					1								
G	UF					1							1							
H	TD1 (no power ready)		1	1	1	1														
I	LBC-CLOSE (memory)							1	1	1	1	1	1					1		
J	TD7 - initiated by I							1												
K	TBC-CLOSE (memory)								1									1		
L	ICC & LBC-TRIP (memory)						0													
M	TBC-TRIP (memory)		0	0	0	0		0		0	0	0	0				0			
N	TD2									1	1	1	1							
O	LDP																	1		
P	TD6 - initiated by 0																	1		
Q	DP																1			
R	LOAD OCP														1					
S	TD5* - initiated by R														1					
U	INV OCP													1		1				
V	TD4* initiated by U													1		Ø				
W	TD3*															1				
X	Tuning Fork Failure																			1
Y	LBC-TRIP (memory)						0													
Z	Reset Trip Memories		0	0	0	0				0	0	0	0	0	0	0	0	0	Ø	
	* TDS < TD4 < TD3	Initiate System Startup	Startup Fault				Normal Start			OV Fault	UV Fault	OF Fault	UF Fault	Zone 3 Fault	Zone 2 Fault		Zone 1 Fault	Load Division Fault	Manual Shutdown	Freq. Ref. Failure

Symbol	Dependent Variable	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19
T1	ICC-CLOSE	1																		
T2	LBC-CLOSE & set memory						1													
T3	TBC-CLOSE & set memory		1	1	1	1		1		1	1	1	1				1			
T4	ICC-TRIP & set memory		1	1	1	1				1	1	1	1			Ø	1		1	
T5	LBC-TRIP & set memory		Ø	Ø	Ø	Ø				1	1	1	1			1	1		1	
T6	TBC-TRIP & set memory													1	1			1	1	
T7	Load Division Control								1											
T8	Sync Bus Signal connected to Sync Bus								1											
T9	To H Bus								1											
T10	Switch to Tuning Fork No. 2																			1
		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19

LEGEND

1 - indicates that the condition must exist to perform the function.

0 - indicates that the condition must exist to perform the function.

Ø - indicates that either 1 or 0 may exist (don't care condition).

(a)-T number is TRANSMISSION or action resulting from a specific combination of Independent Variables.

NOTES

1 - System Control and Protection is accomplished on a subsystem basis. Subsystem is considered paralleled when both LBC and TBC are closed.

2 - All functions reading horizontally are OR functions, while all functions reading vertically are AND functions.

3 - See figure 4, in reference 2, for definition of other terms.

Table 2. - Truth Table for Converter Automatic Control and Protection

Independent Variable		Column Number															
Symbol	Variable	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
A	MOS-AUTO	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
B	CCS-CLOSE	1	1														
C	CCS-TRIP																1
D	OV				0					1							
E	UV				0						1						
F	TD1		1														
G	No Power Ready-Memory			1	0												
H	TD2				1												
I	CC-TRIP (memory)	0															
J	LBC-CLOSE (memory)		0			1		1		1	1						
K	LBC-TRIP (memory)				0												
L	DTB (no voltage on tie bus)					1		1									
M	AP						1		1								
N	TD7 - initiated by M						1		1								
O	TBC-TRIP (memory)			0		0	0			0	0						
P	LDC & LDP-TRIP (memory)							0	0							0	
Q	TD3									1	1						
R	DP														1		
S	COCP											1		1			
T	TD4 - initiated by S											1		Ø			
U	TD5 - initiated by T													1			
V	TB OC												1				
W	TD6 - initiated by V												1				
X	LDP															1	
Y	TD8 - initiated by X															1	
Z	TRIP Memory Circuit — Reset		0	0						0	0	0	0	0	0	0	Ø
			Startup Fault				Normal Startup			OV Fault	UV Fault	Zone 3 Fault	Zone 2 Fault		Zone 1 Fault	Load Division Fault	Manual Shutdown

Dependent Variable		Column Number															
Symbol	Variable	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
T1	CC-CLOSE	1															
T2	No Power Ready Memory		1														
T3	LBC-CLOSE & set memory				1												
T4	TBC-CLOSE			1		1	1			1	1						
T5	CCC-TRIP & set memory			1						1	1			Ø	1		1
T6	LBC-TRIP & set memory			Ø						1	1			1	1		1
T7	TBC-TRIP & set memory											1	1			1	1
T8	LDP & LDC-CLOSE & set memory							1	1								
T9	LDP & LDC-TRIP & set memory									1	1	1	1	1	1	1	1

LEGEND

1 - indicates that the condition must exist to perform the function

0 - indicates that the condition must not exist to perform the function

Ø - indicates that either a 1 or 0 may exist (don't care)

(a)-T(n) is transmission or action resulting from a specific combination of independent variables.

NOTES

1 - System Control and Protection is accomplished on a subsystem basis. A subsystem is considered paralleled when both LBC and TBC are closed.

2 - All functions reading horizontally are OR functions, while all functions reading vertically are AND functions.

3 - See figure 6, in reference 2, for definition of other terms.

The circuits developed may be applied to any parallel inverter or converter system by simply matching each sensing circuit to the actual rating of the system. This would include such items as turns ratios for transformers, wattage values for resistors, timing for changes in frequency, rating of power contactors and the like.

EVALUATION OF MAGNETIC MATERIALS FOR STATIC INVERTERS AND CONVERTERS

The objective of this study was to obtain design information and test data to improve the performance of magnetic components as they are applied in static inverters and converters (ref 3). Little or no information was previously available to adequately evaluate materials for high-frequency, square-wave excitation. The following is a list of materials investigated and test parameters.

Frequencies: 400, 800, 1600 and 3200 Hz (Square Wave)

Temperatures: -55° C, +25° C, and +250° C at sea level, and 1000 hours in vacuum at 250° C

Materials:

Code	Description
A	2 and 4 mil, Square Hysteresis Loop 4%Mo-79%Ni-17%Fe
B	2 and 4 mil, Grain Oriented 50%Ni-50%Fe
C	2 and 4 mil, Magnetic Field Annealed 49%Co-2%V-49%Fe
D	2 and 6 mil, Singly Grain Oriented Silicon Steel
E	2 and 6 mil, Doubly Grain Oriented Silicon Steel

The following tests were run:

Core loss and apparent power measurement per ASTM A343-60T.

Major ac hysteresis loop determination per ASTM A343-60T.

Direct Current magnetization and hysteresis loop determination per ASTM A341-64.

Constant Current Flux Reset (CCFR) tests were performed per AIEE Bulletin No. 432, Jan. 1959 except that square-wave excitation was used at the above test frequencies.

In addition to the above tests, degradation due to manufacturing processes was evaluated. The effect of these processes on the dc magnetization properties and core loss with 400- and 3200-Hz square-wave excitation was evaluated. Manufacturing processes included coil winding with and without core boxes, core cutting, dip and baking, fluidizing, and various core bonding procedures.

The results of the tests showed the following general characteristics:

1) In CCFR tests, the best gain values at 400 Hz were exhibited by toroids of materials A, E, and B (see materials list above). The best squareness ratio was shown by B. There appears to be no general change in squareness with increasing frequency. Toroids of material A are best suited for applications requiring a high gain. Toroids of material C are best suited for those requiring a high value of saturation. For an optimum combination of properties, material B (grain oriented 50%Ni-50%Fe) appears best followed by material E (doubly grain oriented silicon steel) when higher saturation values are desired.

2) For low core loss requirements using square-wave excitation, toroids of materials C and E display optimum capabilities at high inductions; whereas, materials A and E are best suited for low inductions.

3) Materials C, D, and E of the ferro-magnetic alloys tested are the least affected by temperature.

4) Except for core cutting, core processing procedures have only minor effects on magnetic properties.

5) The magnetic properties and interlamination resistance of the materials are not affected by vacuum at 250° C.

6) This magnetic materials study further substantiates the work of others by showing that square-wave excitation results in lower core loss than sine-wave excitation. At 3200 Hz, a 15-percent reduction in core loss was realized for materials A and E.

7) Singly and doubly grain oriented silicon steels (materials D and E) are compared for 750-VA power transformer cores in a harmonic-neutralized inverter. Significant reduction in core loss or transformer weight can be realized if doubly grain oriented silicon steel is used for the transformer cores.

LOAD PROGRAMMER, STATIC SWITCHES, AND ANNUNCIATOR FOR INVERTERS AND CONVERTERS

The objective of this program (ref. 4) was to investigate the following system components:

1) A load programmer to fully utilize the available capacity of the power system by automatically adding and removing loads on a priority basis;

2) Ac and dc static switches to eliminate electromechanical contactors; and

3) An annunciator to provide visual information as to the state of each channel of a parallel system.

The following summarizes the results of these individual development areas.

Load Programmer

A design concept is defined for a load programmer which monitors system capacity relative to load power demands and automatically adds or removes lower priority loads whenever higher priority loads or changes in system capacity warrant. The programmer concept is applicable to either ac systems or dc systems consisting of multiple static inverters or converters operating electrically in parallel. Mathematical equations and circuit concepts are presented for both isolated and parallel systems. Four levels or priorities of loads are used in the development of the load programmer concept.

Static Switches

Ac and dc static power switches are developed and tested. Each type is rated for a two-channel, 1500-VA or 1500-watt parallel power system of the type described in reference 1. Figures 5 and 6 are schematic diagrams of each type of switch. The rating of the dc switch is single-pole, 28 volts, 40 amperes continuous with a 250 percent current-interrupting capability. The full-load efficiency is 96.9 percent. The rating of the ac switch is three-pole, 115/200-volt, 2.2 amperes continuous with a 250 percent interrupting capability. The full-load efficiency is 95.9 percent.

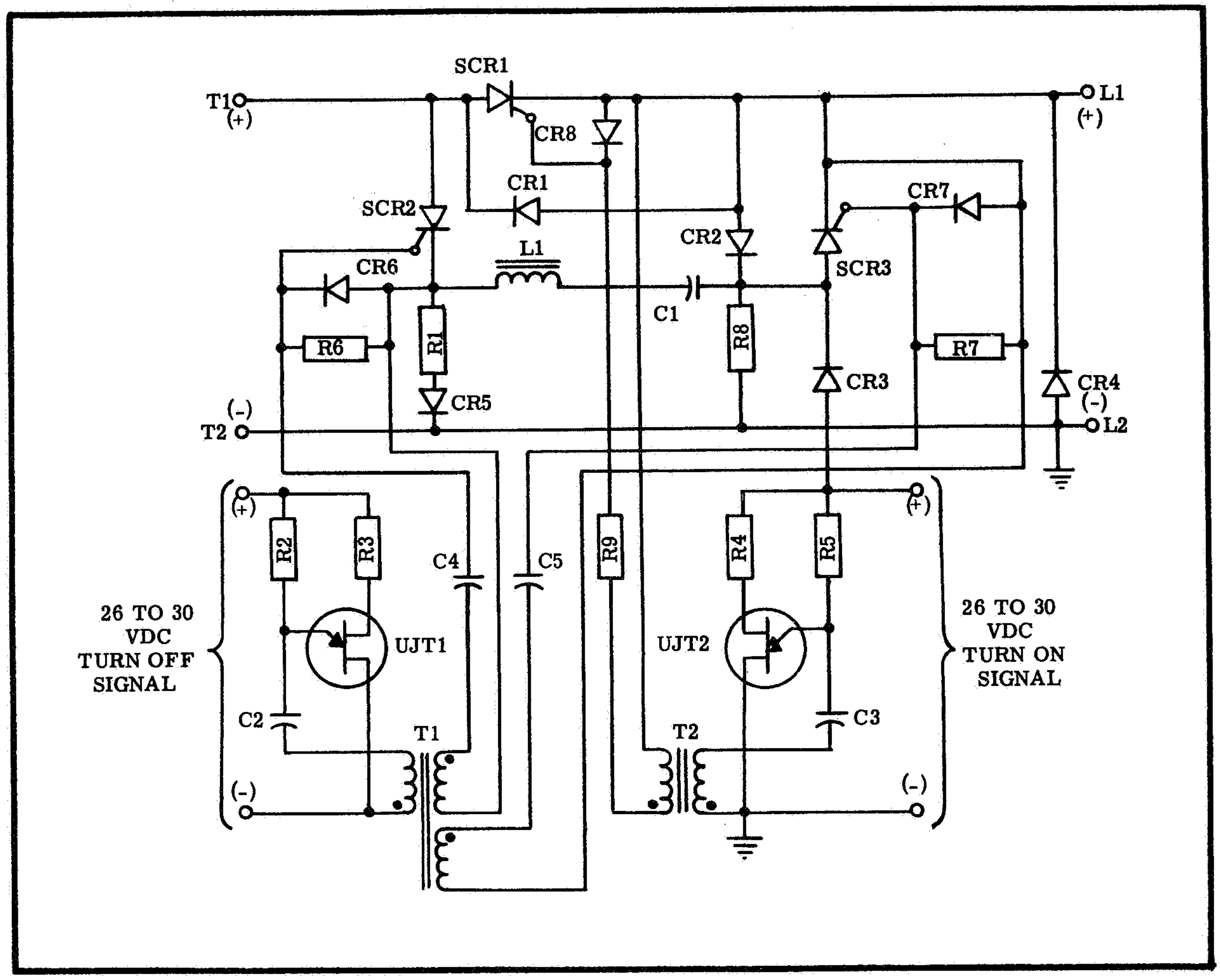


Figure 5. - Static Inverter Control Contactor/Converter Control Contactor Circuit

Static switches exhibit such advantages as faster response, repeated cycling, no arcing, long life and higher reliability. However, the static switch is heavier, larger, and less efficient than its electromechanical counterpart.

Annunciator

The annunciator provides a visual indication of the state of the electric power system. Figure 7 shows a typical layout of an annunciator for one channel of a parallel system. Lamps provide an indication as to the type of fault, the conditions of the various contacts and the operating mode (isolated or parallel) of the channel. The lamps are controlled either by

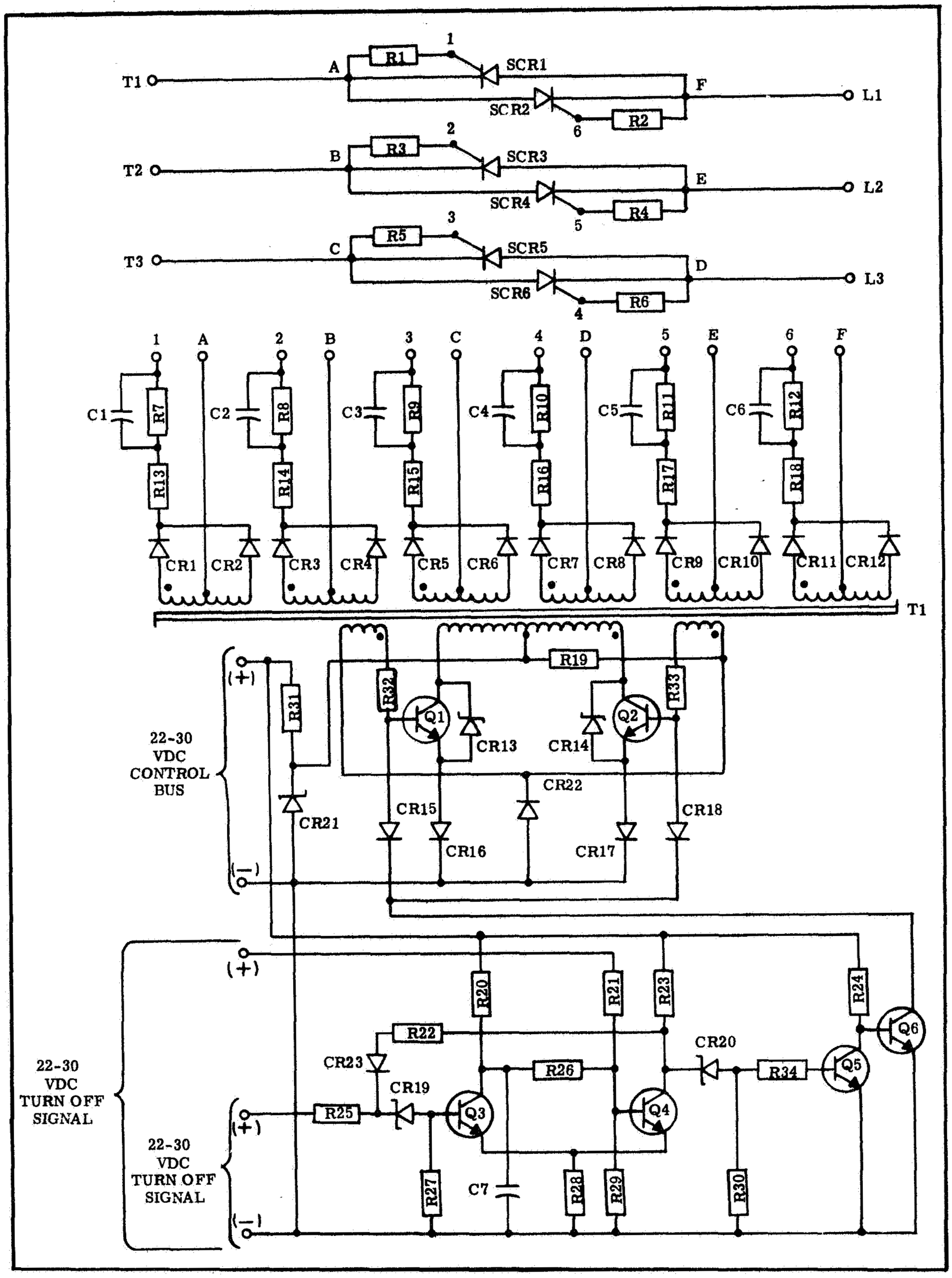


Figure 6. - Inverter System Static Load Bus, Load Control, and Tie-Bus Contactor Circuit

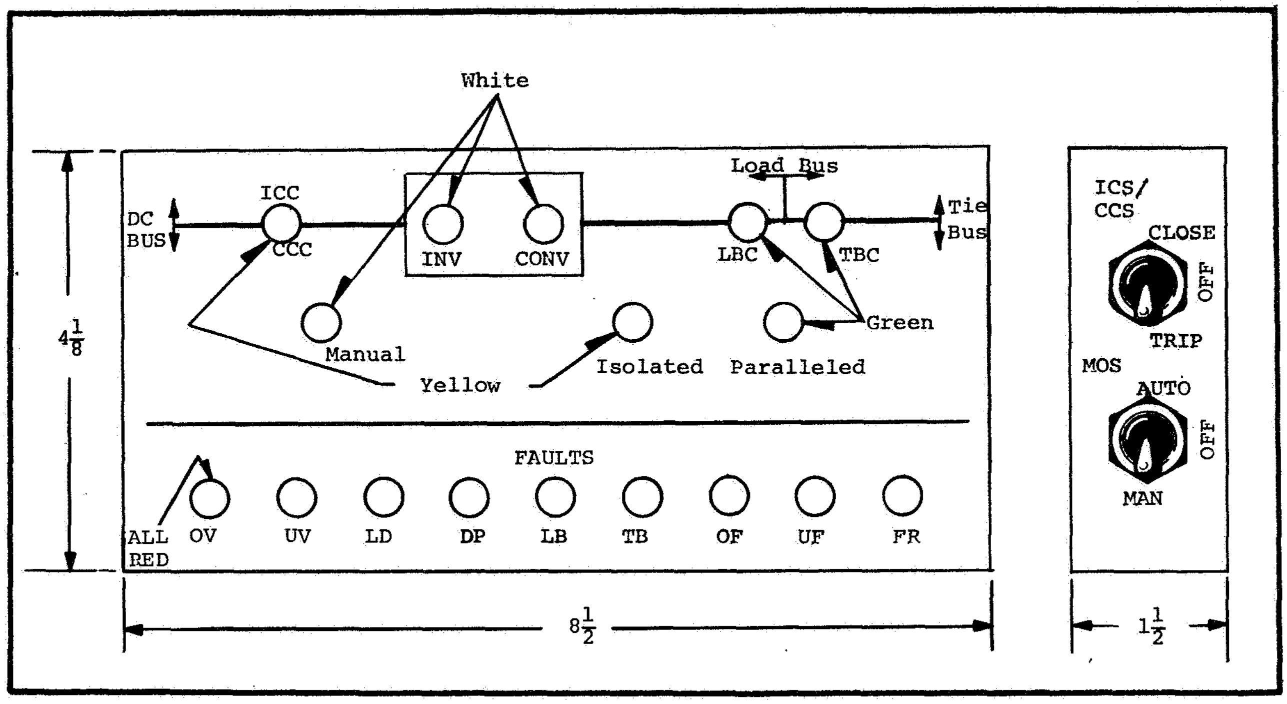


Figure 7. - Annunciator Front Panel

auxiliary contacts of the contactors or by silicon controlled rectifiers (SCRs) as in the case of fault indicator lamps. Figure 8 is a schematic of an SCR lamp driver. The diodes connected to the gate of the SCR provide an AND logic function such that the lamp is turned on only when all signals from the control and protection circuit (NASA CR-1225, ref. 2) are present. The SCR is used to maintain the lamp on until the series switch (MOS of figure 8) is opened which also serves to restart the channel. The annunciator circuit developed is compatible with both ac and dc control and protection circuits described in NASA CR-1225 (ref. 2). The annunciator circuits were verified by operating two units (one for each channel) in a two-channel ac parallel system and in a two-channel dc system.

CONCLUDING REMARKS

In developing methods to improve the performance of static inverters and converters of higher power ratings (1 kW), two general paths were followed. One was the evaluation of a complete parallel system from the power source to the load busses. The evaluation

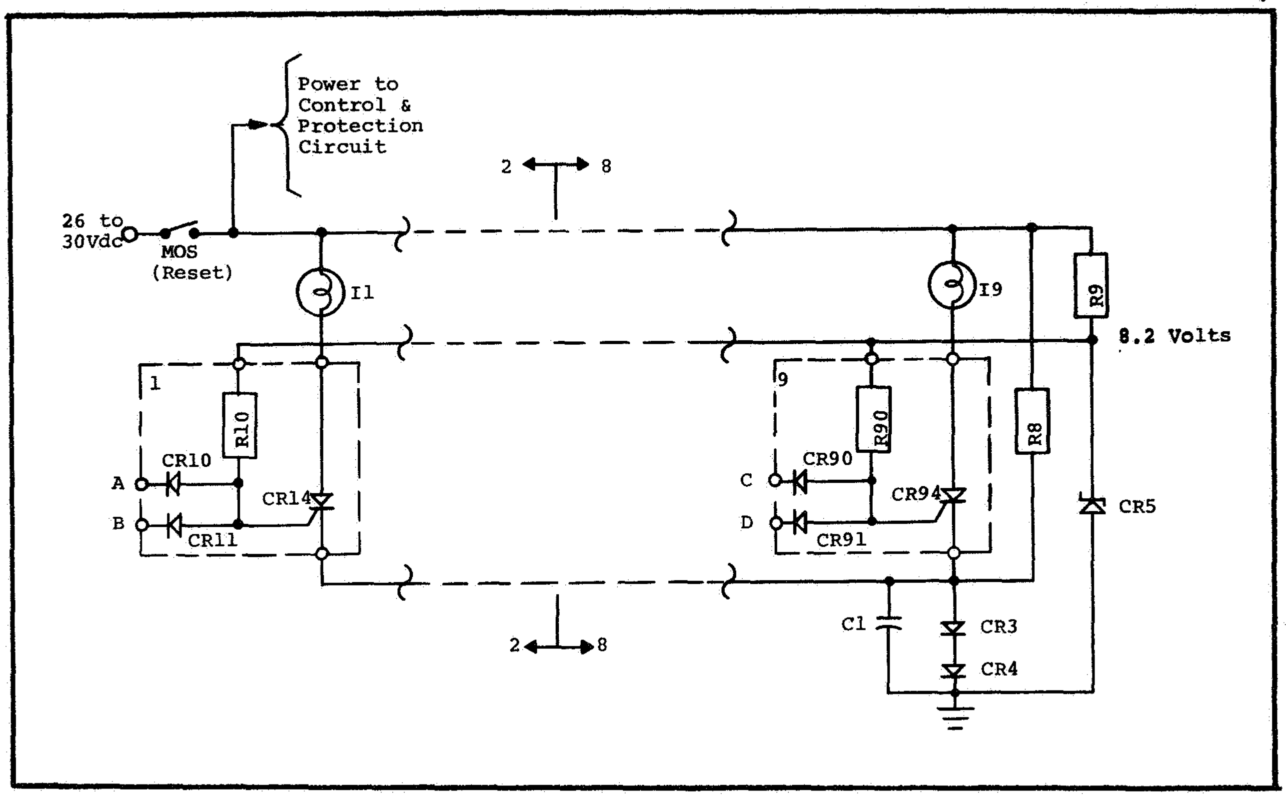


Figure 8. - SCR Lamp-Drive Circuit

included static inverters; static converters; ac and dc system control, protection, and visual annunciators; load programming; and static power switches (ac and dc). The second path was to improve the performance of static conversion systems by evaluating several ferro-magnetic alloys as they are applied to static conversion equipment. The most significant result of this portion of the study is that this represents the first comprehensive analysis of magnetic alloys operated with high-frequency, square-wave voltages.

While a specific type of inverter was used for the development testing, the circuits developed for control, protection, annunciation, load programming and static power switches are directly applicable to any ac or dc parallel electric power system. The load-division control circuits developed for the harmonic neutralized inverter are also directly applicable to static inverters having complex internal impedance and utilizing a central frequency reference and countdown circuits capable of being synchronized. For other types of inverters, the information and methodology provided in the detailed analysis of NASA CR-1224 (ref. 1) may be used to develop similar circuits for the specific case. For inverters not using central references and synchronizible countdown circuits, an additional feedback circuit would be necessary to adjust the phase relationship of the internal voltage of the paralleled inverters in accordance with the real-load-division error. The circuit would be quite similar to the reactive-load-division circuit except the error signal would be added in phase rather than in quadature with the sensed voltage across the system loads.

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