RESEARCH TO DEVELOP MASS DATA STORAGE (U)

BY

A. D. ROBBI
S. KATZ
C. WENTWORTH

AUGUST 1968

Prepared under
CONTRACT NO. NAS12-574

by

RCA LABORATORIES
PRINCETON, NJ 08540

ELECTRONICS RESEARCH CENTER
NATIONAL AERONAUTICS AND SPACE ADMINISTRATION

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RESEARCH TO DEVELOP MASS DATA STORAGE

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SUMMARY

The laminated ferrite technology, combined with integrated MOS-bipolar circuitry, has the potential to realize a low-power, mass random-access memory operating at a 2.5-μsec cycle time. The fabrication of the ferrite planes by pressure-sintering yields storage planes with protruding conductors on regular center spacings. The pressure-sintering was developed sufficiently to produce planes with acceptable mechanical and magnetic properties if the conductors are platinum (maximum processing temperature of 1230°C). Further development is required to lower the processing temperature to accommodate gold conductors (melting temperatures of 1063°C). The combination of p-channel MOS devices and n-p-n bipolar transistors in the integrated address selection, current drive, and sense circuitry results in optimum performance consistent with low power drain. A 13-million-bit module, 65,536 words x 200 bits, consuming 20 to 25 watts is estimated to occupy 4 to 6 cubic feet. The electronics complement of the module includes 65,536 integrated bipolar drivers, a 1024-output binary-tree address decoder, 200 sense amplifiers, 200 dual unipolar digit drivers, and a 200 x 16 digit-sense multiplex circuit. These circuits were designed and evaluated in breadboard form. Further developments in the areas of large-scale integration of the electronic circuitry and mass interconnection techniques are required to fabricate this type of mass memory.

I. INTRODUCTION

Laminated ferrite and integrated semiconductor are appealing technologies to combine for the realization of a medium-speed, mass random-access memory. The high bit-packing density and low-power operating capability of laminated ferrite arrays are a natural match for the high-density and relatively low-power handling characteristic of large-scale integrated semiconductors. The system goals are a capacity of 10^8 bits at a cycle time on the order of 2 μsec with the constraints of minimum power, volume, and weight to make such a memory practical for application to on-board data processing in spacecraft.

The work described here is a culmination of previous RCA activity with the general goal of a mass random-access memory (Refs. 1-5). The experience of those programs and the background of rapidly changing technology led to a modification in approach in two important areas: the laminated ferrites were to be fabricated utilizing pressure-sintering (Ref. 6), and the building blocks of the integrated electronics were to be p-channel MOS transistors combined with n-p-n bipolar transistors. Pressure-sintering was found to be a means of forming a laminate with suitable magnetic properties while holding a tolerance in lateral dimensions sufficient to permit automated interconnection. The MOS transistor itself is not as capable a device for high-current or high-gain-bandwidth applications as the bipolar transistor. The combination of MOS and bipolar devices, called BIMOS, is extremely attractive for laminated ferrite electronics. The BIMOS integrated arrays are circuits with low power drain because of their complementary nature but with the high performance necessary for signal amplification and current driving.

The work described in this report was pursued at RCA Laboratories, Princeton, New Jersey and at RCA Electronic Components, Somerville, New Jersey. The Laboratories effort was in the Data Processing Applied Research Laboratory, Dr. W. M. Webster, Acting Director. The work was under the supervision of Dr. R. Shahbender. Dr. Anthony D. Robbi was the Project Engineer. Technical Staff Members Mr. C. Wentworth, Dr. J. T. Wallmark, and Mr. J. W. Tuska contributed to the program. The Electronic Components effort was in the Technical Programs Laboratory, Dr. Robert B. Janes, Manager. The program was supervised by Dr. Richard W. Ahrons, Manager of Advanced Devices and Applications. The Staff Members contributing to the program were Mr. Stanley Katz and Mr. Norman Ditrick.

II. SYSTEM DESIGN

A. Partitioning

For reasons of reliability, stack bulk, and interconnection complexity, the 10^8-bit memory is formed from eight modules each containing 65,536 words by 200 bits deep or 13,107,200 bits in all. Thus, the complete system would contain approximately 1.05×10^8 bits with all modules "up", and 0.92×10^8 bits with one module "down".

The 200-bit word depth is chosen to keep the voltages associated with word currents moderate. To achieve wide operating margins and a high yield on laminate fabrication, it is required to use two crossovers (digit-sense and word conductor intersections) to store a "bit" of information (Ref. 3). At an estimated peak back voltage of 20 mV per crossover the word back voltage is 8 V.

Low system noise and a simplicity in interconnection pattern are obtained in a word-address decoding scheme incorporating word lines grounded at one end. A one-out-of-1024 binary tree decoder is a reasonable compromise between decoder complexity and the driving capability at the decoder input. In a module each decoder output must drive the inputs of 64-word drivers ($1024 \times 64 = 65,536$ words), one of which is selected by clocked power. The unselected drivers present a capacitive loading. A block diagram of word partitioning of the 10^8-bit system is shown in Figure 1. The design of the word driver and the 1024-output decoder are detailed in Section IV. The other decoders shown in Figure 1

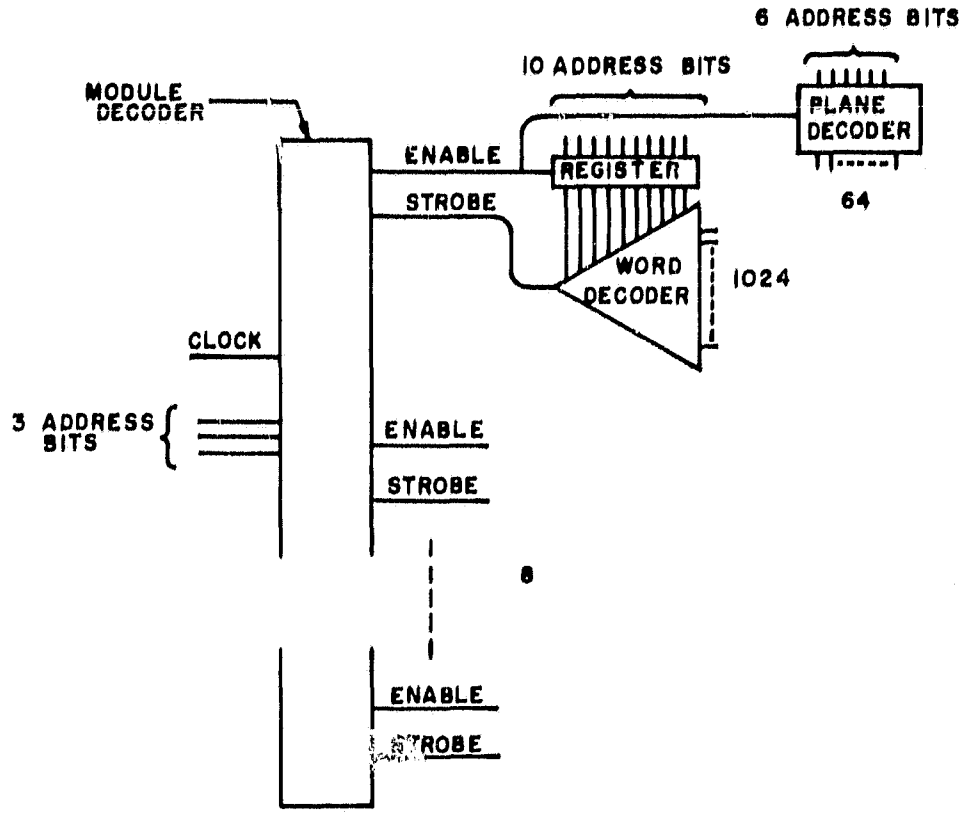


Figure 1. Block diagram of word-decoding subsystem.

have not been designed; they are assumed to be integrated logic gates. The address registers are complementary flip-flops of the type described in Section V as data registers.

If the 200 digit/sense lines are series-connected throughout the 64 x 1024 word stack the total time delay from end to end would be roughly 2 μsec (Ref. 5). Since the digit noise requires several delay times to attenuate sufficiently to detect a 1-mV signal, a segmenting of the digit/sense line is necessary. On the other hand, high-gain sense amplifiers and detectors are by nature consumers of power (on the order of 100 mW each). A multiplex strategy has been conceived and designed to realize reasonably short digit/sense lines and the minimum of 200 sense amplifiers per module, as indicated in Figure 2. The digit/sense lines are partitioned into sixteen 4096-bit segments, serviced at their centers. This cuts the amplifier-to-termination delay from 1 μsec to 65 nsec, but maintains the desired low power dissipation in the amplifier-detectors. Section V details the design and breadboard results on the digit/sense regeneration loop.

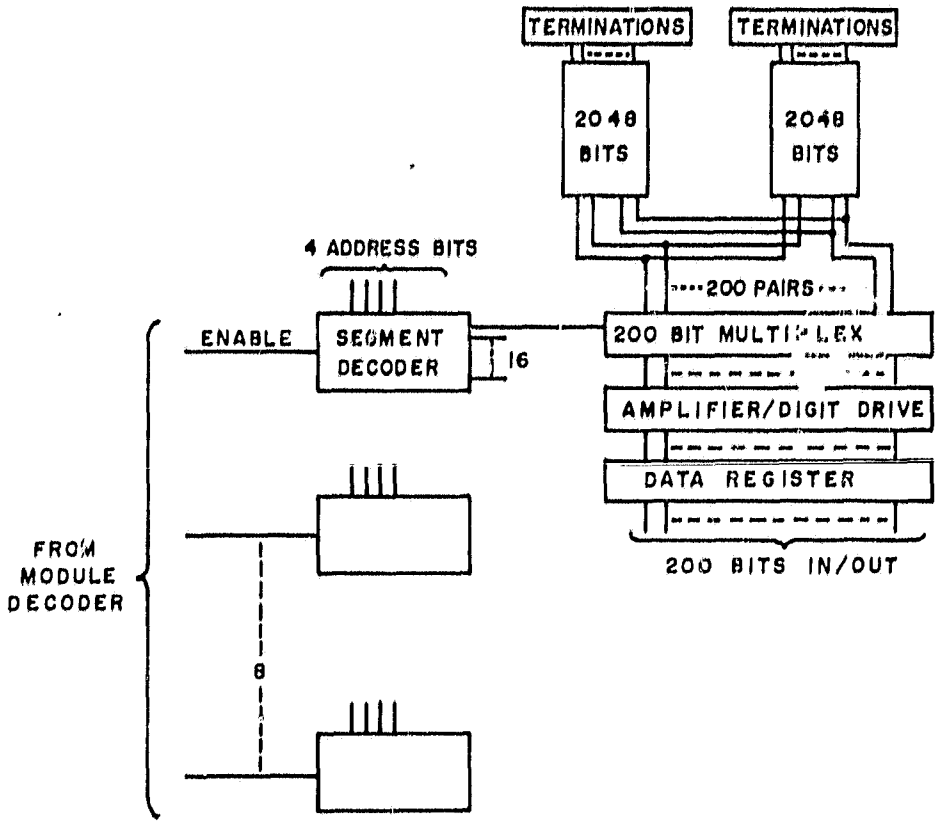


Figure 2. Block diagram of digit/sense multiplex subsystem.

B. Systems Packaging and Interconnection

The systems packaging and interconnection method is illustrated by the exploded view of one module shown in Figure 3. The module consists of 13,107,200 bits; i.e., 26,214,400 crossovers, arranged in a stack of 64 planes, each containing 1024 words by 400 crossovers (200 bits).

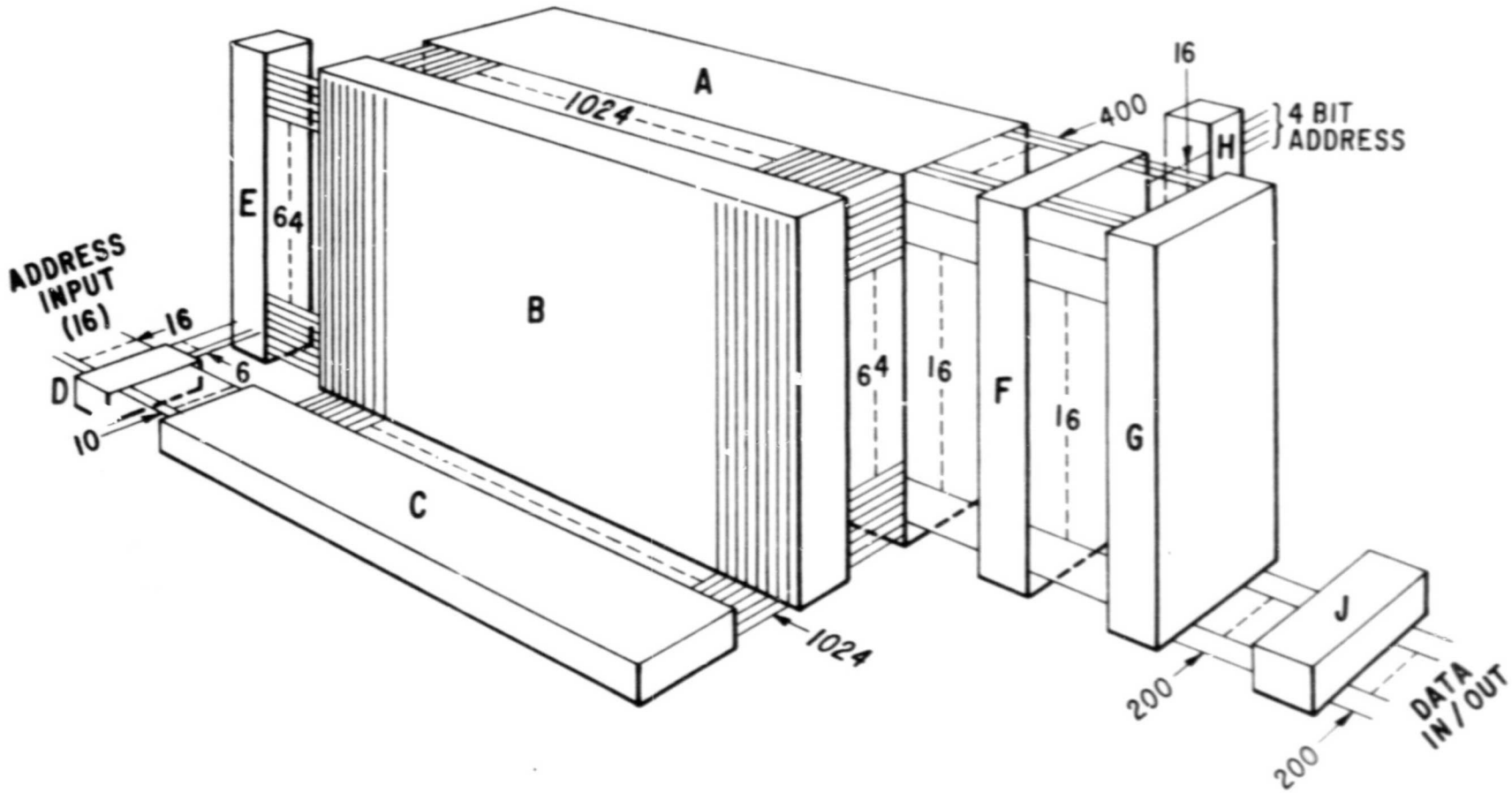


Figure 3. Memory module - exploded view. A. ferrite stack, B. word drivers, C. word decoder (selects 1 word of 1024), D. address register, E. clocked supply decoder (selects 1 plane of 64), F. multiplex devices, G. amplifier/detector assembly, H. digit control (selects 1 segment of 16), and J. data register.

Each of the 64 planes containing eight ferrite arrays, 1024 word driver circuits, and a part of the word driver clock circuit constitutes a replaceable plane which is mounted on a separate circuit board (Figure 4). This circuit board is tested independently of the others and then stacked and connected to the rest of the system. Replacement of the board is possible by cutting its connections, removing it, sliding in a fresh board, and patching up the connections.

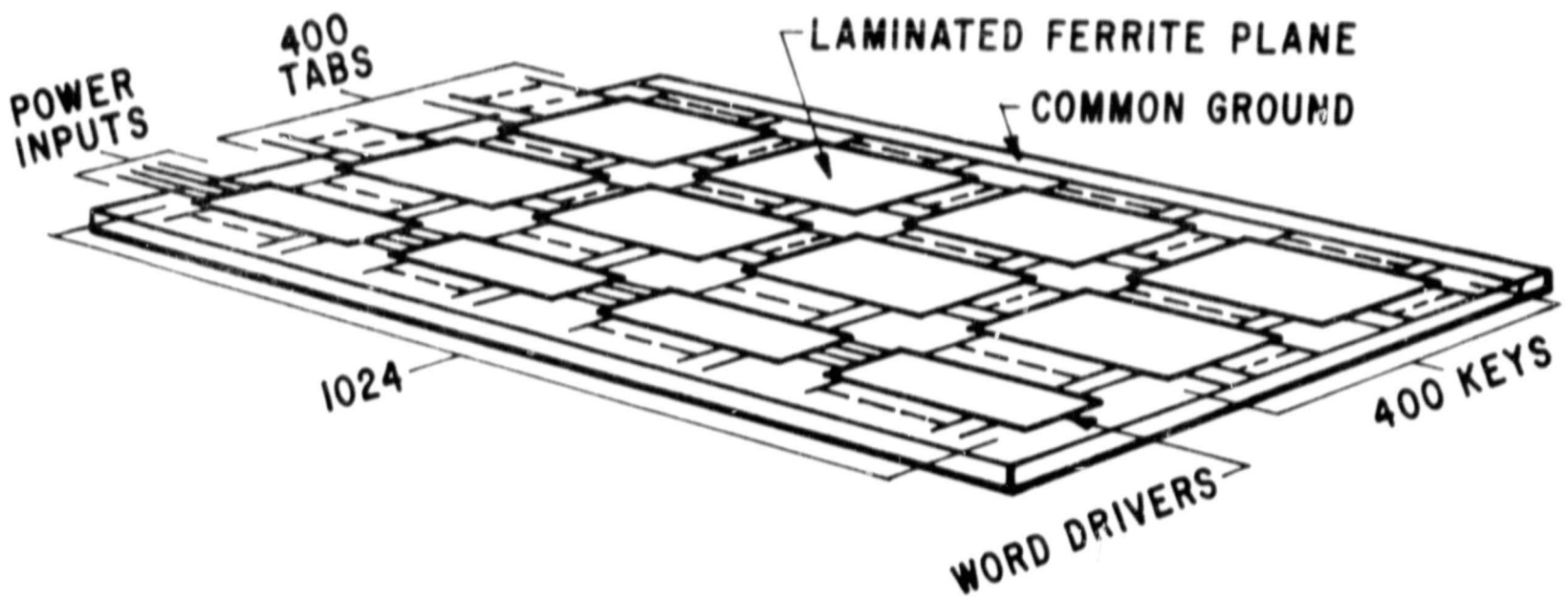


Figure 4. Stack plane layout.

Each ferrite array, consisting of 256 x 200 crossovers, is encapsulated in a semihermetic metal-glass epoxy enclosure using solder and epoxy for sealing (see Figure 5). This package has been developed and tested at 100% relative humidity and 100°C temperature for several months with voltage applied between lines (Ref. 7). No change was observed in the isolation resistance between lines, which is a sensitive detection method for the deleterious effect of water vapor.

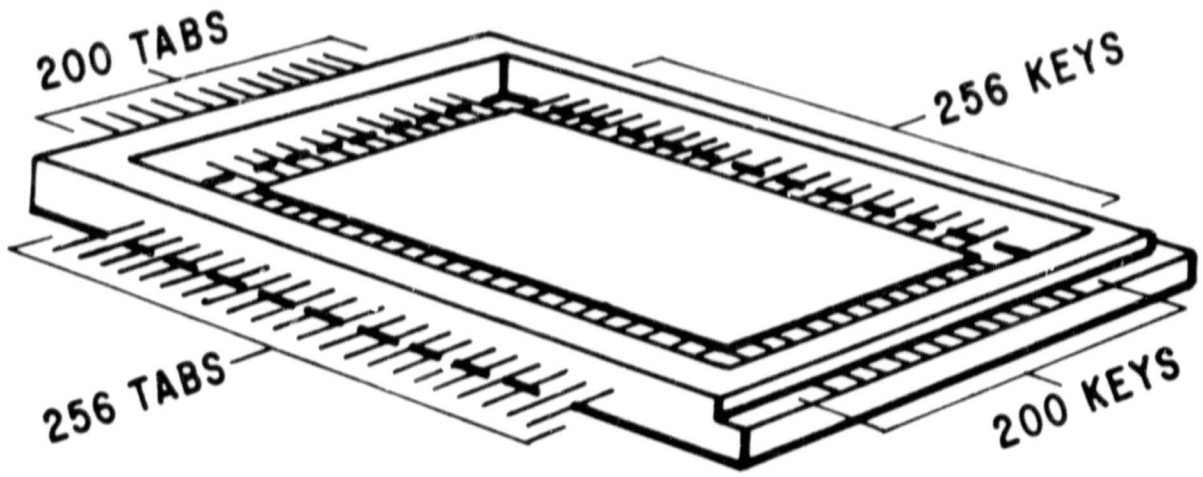


Figure 5. Laminate assembly (cover removed).

The contacts for interconnection to this package are made using a "piano keyboard" construction along two edges, and a protruding tab construction at the other two edges. The connections could be on 10- or 15-mil centers and are joined by a solder reflow technique using a point welder with two coplanar electrodes for supplying the heat pulse. Replacement of a faulty array may be made by cutting the leads, removing the serially connected arrays, placing new arrays in their place, and reconnecting.

The semiconductor devices are hermetically encapsulated using a beam-lead technique in which the semiconductor is covered by a layer of silicon nitride or aluminum oxide with the leads of plated gold or nickel protruding from the strips on 10- or 15-mil centers. These tabs are directly connected to the ferrite array package keyboards and to the vertical intraconnecting bars on the outside of the stack.

Connections from the word-driver strips to the word-decoder circuit are made via vertical intraconnection bars which join directly to the tabs of the word-driver strips by the solder reflow technique. The same is true for the word-driver clock lines.

On the opposite side of the stack the word lines are joined by a ground connection which runs vertically between the planes.

The digit lines on the digit side of the stack are connected in series through four planes, resulting in 4096 bits per multiplex circuit. Thus, the terminations and the multiplex circuits repeat in 16 segments which are controlled by a digit decoder selecting 1 of 16 four-plane segments. Every fourth word plane consequently contains part of the digit multiplex circuit and terminations, in addition to the ferrite planes and word drivers. The multiplex circuit is interconnected by vertical bars leading to the digit-decoder circuit which connects the main sense amplifier and the current source to the selected digit segment. From the multiplex circuit 400 lines go to the sense/regeneration circuitry.

The estimated dimensions of the ferrite array package of Figure 5 are 3 in. x 3-1/2 in. x 1/4 in. for the case of 10-mil centers. The board of Figure 4 containing one plane has the dimensions 16 in. x 11 in. x 1/4 in. The stack in Figure 3, assuming that the connections can be made as planned, occupies a space of about 20 in. x 16 in. x 20 in., or 3.7 cubic feet. With spacings of 15-mil centers the volume per module is approximately 6 cubic feet.

III. LAMINATE FABRICATION BY PRESSURE-SINTERING

A. Introduction

The firing of a laminated ferrite plane causes it to shrink approximately 17% in all dimensions; the shrinkage, however, is not precisely reproducible and may, in fact, be nonuniform throughout a laminate. In order that interconnections be made rapidly and accurately the laminate conductors must be precisely spaced. A possible solution to this problem is to employ a procedure called pressure-sintering. Here the unfired laminate is placed between two flat punches, or plates, and pressed during firing. The application of pressure in this way can reduce the lateral firing shrinkage to less than 1%, thus providing the desired dimensional uniformity. The required volume shrinkage is obtained by a decrease in thickness.

The electrical resistance of the conductors, particularly in large arrays, should be very low. Gold, silver, and copper, then, would be the most obvious candidates for conductor material. Gold is the most suitable material because silver and copper enter the spinel structure, adversely altering the magnetic properties. The use of pressure-sintering offers the best possibility of obtaining satisfactory laminates using gold conductors because processing temperatures below the melting point of gold can be used with this method.

B. Description of Apparatus

Photographs of the apparatus are shown in Figures 6 and 7. In Figure 6 the pressing chamber is open for loading; in Figure 7 the chamber is assembled for pressing. Power is obtained from a 208-V, 30-A line through a 6-kVA powerstat driving a 25-kVA transformer with a stepped 208-V primary providing secondary voltages of 4 to 14 V. Normal power consumption is 3 to 4 kW. The 12-ton hydraulic press is placed on the 25-kVA transformer. The powerstat is shown mounted on the side of the transformer. It is driven by an electric motor to provide a controlled rate of temperature rise for the sample. The pressure chamber is gas-tight, enabling the use of vacuum or any gas as atmosphere; usually vacuum or N_2 is used.

Figure 8 is an exploded view of the pressure-sintering furnace. The pressing stack is identical on both sides of the sample. The cooling plate is aluminum with 1/4-in. copper tubing brazed to it. A 5/8-in.-thick backup plate of cold-rolled steel (not shown) is placed between the cooling plate and the thermal barrier plate. The thermal barrier plate consists of two 1/4-in.-thick plates of -100 mesh GGB zirconium oxide grog. The nonsticking electrical insulating plates are 10-mil-thick phlogopite. The pressure plate is 1/2 to 1-in.-thick TZM metal. The heater is 27-mil-thick Inconel. The contact material (if any) is placed between the pressure plate and the sample. All plates, except the phlogopite, are fine-ground flat and parallel. The movable seal plate is the top of the chamber and is a piston with the seal being effected by an O-ring.

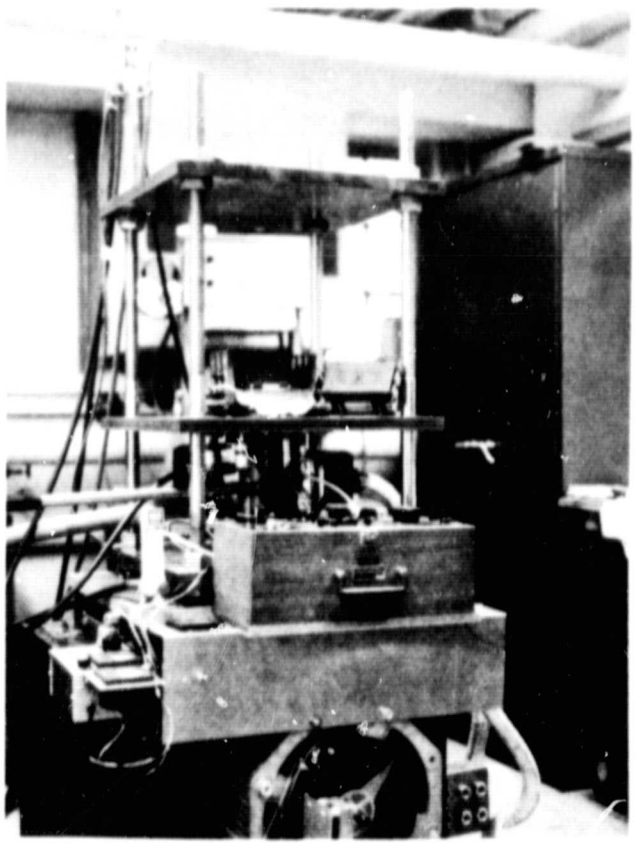


Figure 6. Pressure-sintering apparatus - chamber open.

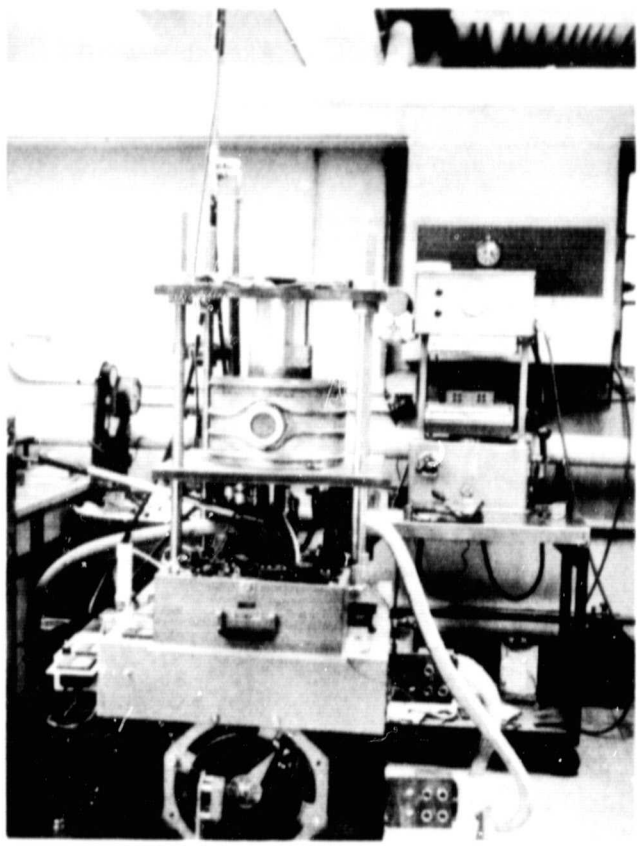


Figure 7. Pressure-sintering apparatus - chamber assembled.

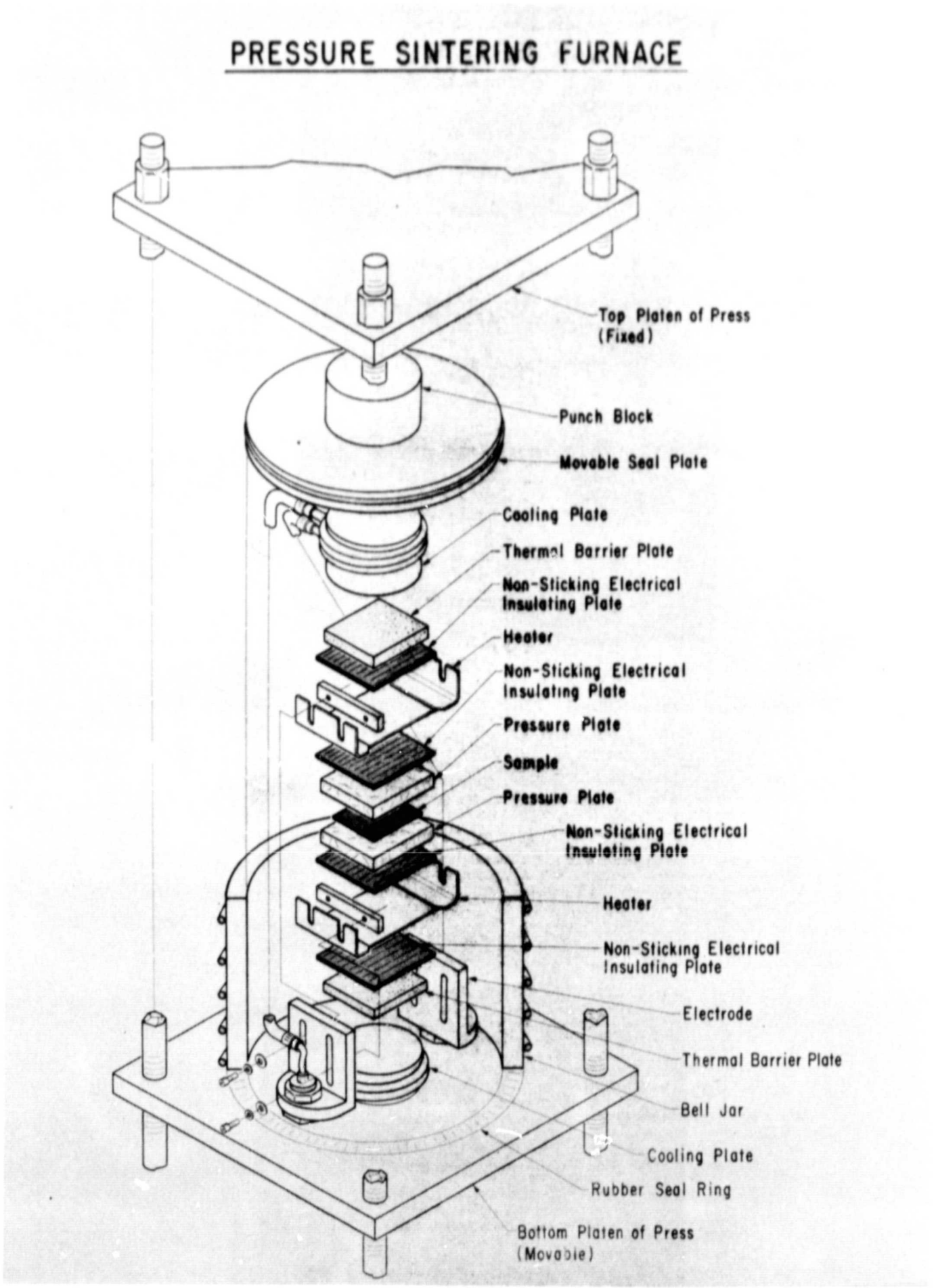


Figure 8. Pressure-sintering apparatus - exploded view.

The two halves of the stack between the sample and the cooling plate are clamped together to form an integral block. This is shown in Figure 9. The top block is held to the piston by a bolt through the piston into the top backup plate. The threaded hole in the top backup plate can be seen in Figure 9. The two block assemblies can be separated slightly by moving the piston up. This removes all pressure from the sample.

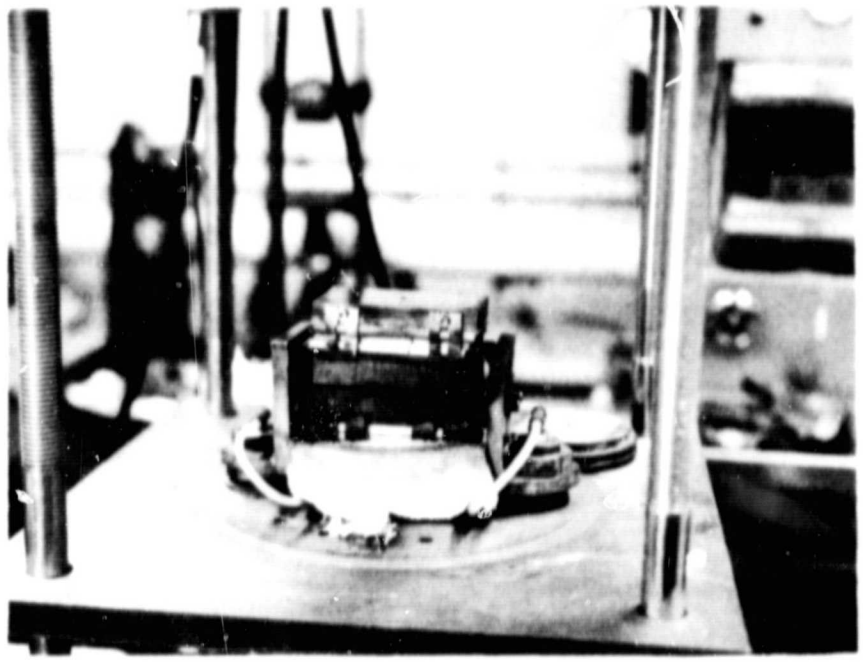


Figure 9. Assembled pressing stack.

C. Ferrite Materials

Two compositions have been used: No. 3515 and No. 47 (Ref. 2). Composition 47 (38% Fe_2O_3, 38% MgO, 19% MnO and 5% ZnO) was used for most of the work because it has better temperature stability and higher pulse outputs at low driving currents. A high-temperature anneal is required to develop usable magnetic characteristics in No. 47.

While best results with No. 3515 have been obtained using a high-temperature anneal, work with this material has indicated a fair possibility of obtaining satisfactory results after an anneal at temperatures below the melting point of gold. The hysteresis loops of cores ultrasonically cut from hot-pressed conductorless sheets of this material are shown in Figure 10.

D. Contact Materials

The best material used in contact with ferrite is 1/2- to 1-mil-thick phlogopite sheets. Under many firing conditions this material does not stick at all to the ferrite; when it does stick it can be easily abraded. If abrading is required, it should be done before annealing. No sticking of the phlogopite

(a) (b)

Figure 10. (a) Hysteresis loop of a torid of 3515 material ultrasonically cut from a laminated sheet hot-pressed at 4000 lb/in.^{2} in N_2 at 1050°C for 30 minutes. H_c = 1.83 Oe. (b) Hysteresis loop of the same toroid after an anneal in air at 1040°C for 24 hours followed by 9 hours in N_2 at the same temperature. H_c = 1.35 Oe.

to the TZM was experienced. See Table I for results obtained with various contact materials.

E. Pressure Plates

A good pressure plate should deform as little as possible at sintering temperatures under the pressure used. The best materials for these plates are tungsten carbide or TZM. The best thickness is 1/2 to 1 inch, which is a compromise between the temperature gradient across it and its rigidity.

F. Effect of Pressure, Temperature, and Time

The effects of pressure, temperature, and time on the magnetic and mechanical properties of composition 3515 have been studied in detail elsewhere (Ref. 6). The work described here has been done with relatively large-area, thin samples of both compositions 3515 and 47. Practical engineering considerations limit the range of parameter variation. Sintering above 1100°C causes too much sticking and reaction with the contact material as well as softening of the pressure blocks. Soft pressure blocks always result in extensive cracking. Proper sintering below 1000°C requires a considerable increase in pressure and/or time. The energy required to attain the density and proper spinel structure is much more easily obtained through thermal than mechanical work. The best results have been obtained by sintering at 1000°C to 1060°C for 30 to 360 minutes at 4000 lb/in.^{2} (see Figures 10 and 12).

G. Atmosphere

Nitrogen has been found to be the most suitable atmosphere; it provides reasonable protection for the heaters and the pressure plates and uniformly controls the oxidation state of the Mn and Fe. A vacuum environment leads to a nonuniform diffusion of oxygen from the laminate resulting in density variations.

TABLE I

SUMMARY OF EXPERIMENTS WITH DIFFERENT CONTACT MATERIALS

CONTACT MATERIAL	COMMENTS
Dense MgO	Severe reaction under sintering conditions required for laminates with sufficiently high densities to give usable magnetic properties.
Graphite	No sticking or cracking; however, considerable chemical reduction of the ferrite. Low ferrite resistivity and extensive surface fracturing developed during a subsequent oxygen anneal.
Tungsten carbide	Reaction is a problem. No reaction was observed in a few cases. This indicates that the problem could be solved.
Silicon carbide	This material is extremely brittle and is prone to crack. Difficulty has been experienced in obtaining a sufficiently smooth and dense surface to prevent mechanical sticking but it has been done.
Molybdenum	Too much reaction with ferrite, even in vacuum or N_2 atmosphere.
Tungsten	Possibly usable; cannot be used in oxidizing atmosphere. Some reaction with the ferrite was observed, but insufficient work has been done to determine its limitations.
Tantalum	Severe reaction with the ferrite.
Stainless Steel	Too soft at temperatures above 900°C. Flows under pressure and breaks ferrite.
Iridium	Some sticking. Probably good at thicknesses of 1/4 in. to 1/2 in., but expense excessive.
Muscovite	Decomposes and reacts with ferrite at temperatures below the ferrite sintering temperature.
Phlogopite	Usable and relatively satisfactory. Thicknesses less than 1/2 mil generally unsatisfactory because of through-reaction between backup plate and ferrite. Thicknesses above 5 mils avoided because of difficulty in obtaining sufficient uniformity in thickness over the entire area. A thickness of 1 mil seems a good compromise.

H. Anneal

An anneal is usually required to attain good hysteresis squareness. Composition 47 requires an anneal at temperatures above the melting point of gold. Figure 11 shows the hysteresis loop of a toroid of pressure-sintered No. 47 material annealed in CO_2 at 1260°C. No loop was evident prior to the anneal.

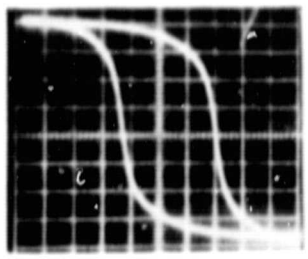
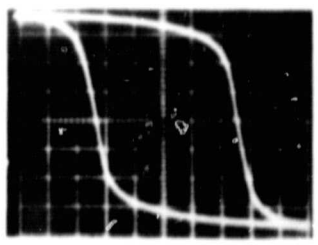
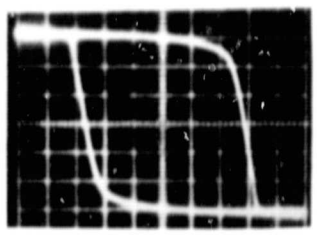


Figure 11. Hysteresis loop of a toroid of 47 material pressed at 4000 lb/in.^{2} for 2 hours in N_2 at 1000°C, annealed in CO_2 at 1260°C for 10-1/2 hours, cooled in H_2 from 1150°C to room temperature. H_c = 1.25 Oe.

Good loops have been obtained from Composition 3515 annealed at 1040°C for 24 hours in N_2, then followed by a 9-hour soak in N_2 and cooled in N_2. See Figure 10(b). Composition 3515 shows some promise of providing a usable laminate even when no anneal is used, as seen in the hysteresis loop of Figure 12(a). There is a possibility of attaining suitable pulse performance. As shown in Figure 12(b), the anneal caused a substantial improvement in performance. Composition 3515, then, offers the possibility of obtaining magnetically good laminates using solid gold conductors, thus substantially reducing the conductor resistance and achieving a transmission line closer to an ideal distortionless line.



(a)



(b)

Figure 12. (a) Hysteresis loop of a toroid of 3515 material ultrasonically cut from a laminated sheet hot-pressed at 4000 lb/in.^{2} at 1060°C in N_2 for 3 hours. H_c = 1.87 Oe. (b) Hysteresis loop of the same toroid after an anneal in air air at 1150°C for 24 hours followed by 9 hours in N_2 at the same temperature. H_c = 1.03 Oe.

I. Conductors

Most of the conductor-containing laminates have been made by filling grooves in the ferrite with platinum powder; some palladium powder has also been used.

Sufficient work has been done on the use of solid conductors to show that this would be a feasible process. Arrays of 64 x 64 solid gold conductors have been embedded into a ferrite memory plane, which was pressure-sintered. A radiograph of such an array is shown in Figure 13. The areas of different contrast are due to multiple exposure of the x rays necessitated by the sample-handling capabilities of the x-ray machine. The conductors were not stretched during the embedding process, resulting in the nonuniform spacing evident in Figure 13. Several of these planes have been made and pressure-sintered but all had back-to-front short circuits; so they were not magnetically tested. A 256 x 100 plane has been fabricated using 1-mil x 6-mil beryllium-copper conductors formed as an integral part of a heavy frame of the same material. The beryllium-copper conductors would not stand the firing temperatures, but handling techniques such as stretching during the conductor-embedding and ferrite-launching process have been worked out successfully using these arrays.

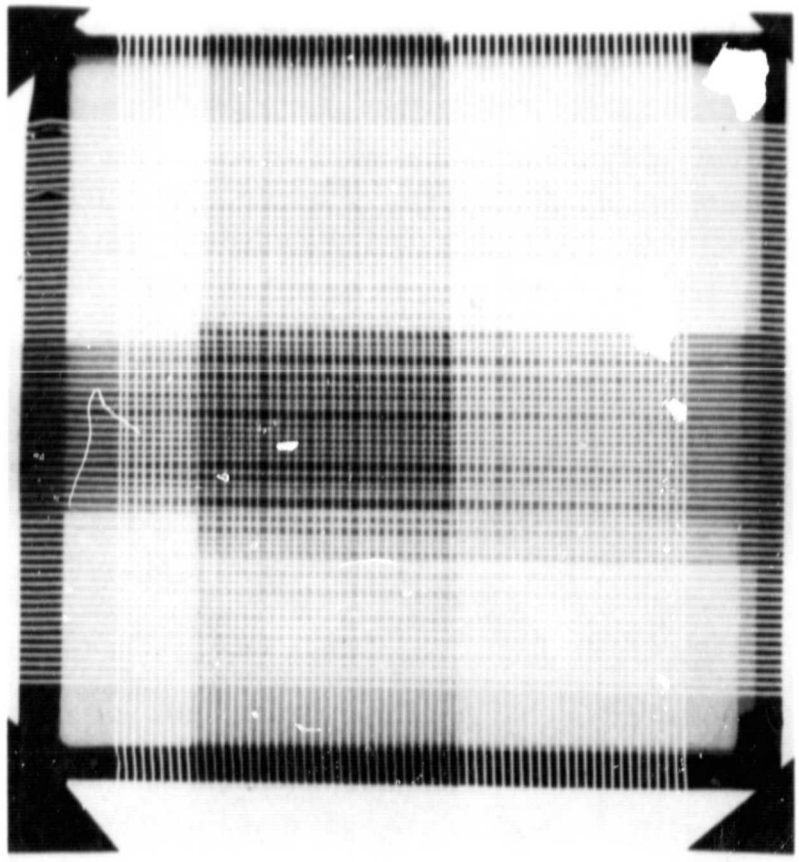


Figure 13. Radiograph of pressed laminate containing solid gold conductors on 15-mil centers.

J. Pulse Test Results

The pulse program used in testing the laminates is of a two crossovers-per-bit, unipolar digit type (Refs. 4, 5). The number of disturb pulses, both before and after writing, is 50. The digit/sense pairs and the word lines are far-end grounded. The drive current characteristics are given in Table II.

TABLE II

DRIVE CURRENT CHARACTERISTICS

Current	Amplitude (mA)	Pulse Width (nsec)	Rise Time (nsec)
I_{read}	100	400	120
I_{write}	50	400	120
I_{digit}	18	500	50

The samples listed in Table III all were driven by the above pulse program. The average signal output of each sample is given. Good results were obtained with Composition 47, which at best duplicated signal amplitudes obtained from a conventionally fired laminate.

TABLE III

OUTPUT SIGNAL FROM DIFFERENT SAMPLES

Sample Number	Signal (mV)	Comments	
7-64 (conventional)	2.9	Reference	
42-61-47 (hot press)	2.7 ± 10%	Best hot press	No. 47 Material
42-73-47-1	1.9	Fair	
42-81-47-1	2.3	Fair	
42-84-47-1	0.3	Bad	
42-83-47-1	2.5	Good	
42-88-47-1	1.2	Poor	
42-86-47-1	0.7	Bad	
42-89-47-1	1.25	Poor	
42-100-47-1	0.3	Bad	
42-92-15-1	0.5	Bad	No. 3515 Material
42-97-15-1	0.3	Bad	
All samples were tested under identical drive conditions.			

K. Details of Pressure-Sintered Laminates

The above results and conclusions are abstracted from a large body of experimental work. The scope of that work is indicated in Table IV, which summarizes the data for all the pressure-sintered samples.

TABLE IV

SUMMARY OF MATERIALS AND CONDITIONS

No.	Contact Material	Sample Size (in.)	Conductor	Pressure ($lb/in.^2$)	Temp. (°C)	Time (min.)	Atmosphere	Magnetic Property	Anneal	Pressure Applied	Comments
				A. Type 11 Material Calcined @870°C for 2 hr in Air							
1.	Dense MgO	1.7x4.2	none	5000	1180	5	air	not measured	none	total cycle	Everything stuck together.
2.	Dense MgO	1.7x4.2	none	1000	1090	5	air	not measured	none	total cycle	No sticking - Ferrite not dense.
3.	Dense MgO	1.7x4.2	none	4000	1050	65	air	not measured	none	total cycle	Everything stuck together.
4.	0.002" SnO_2	1.7x4.2	none	6000	1180	5	air	not measured	none	total cycle	Everything stuck together.
				B. Type 47 Material Calcined @900°C for 2 hr in Air							
5.	0.0027" SnO_2	1.7x4.2	none	4000	1090	10	air	not measured	none	total cycle	Sticking - badly cracked.
6.	1/8" MgO	1.7x4.2	none	5000	1180	5	air	not measured	none	total cycle	Some sticking - badly cracked.
7.	1/8" MgO	1.7x4.2	none	4000	1050	65	air	not measured	none	total cycle	Some sticking - badly cracked.
8.	Graphite	1.7x4.2	none	4000	1205	10	air	not measured	1260°C O_2	total cycle	No sticking. Mechanically perfect. Cracked badly during anneal.
9.	Tungsten carbide	1.7x4.2	Pt Embossed	3300	1000	45	vac.	poor on pulse test	Air 1205°C N_2 1120°C	total cycle	Slight sticking. Broke.
10.	Silicon carbide	1.7x4.2	Pt Embossed	3300	1000	45	air	not measured	none	total cycle	No sticking. Badly cracked.
11.	Stainless steel	1.7x4.2	Pt Embossed	3300	1000	45	vac.	not measured	none	total cycle	No sticking. Few cracks. Delaminated.
12.	Stainless steel	1.7x4.2	Pt Embossed	3300	1000	45	N_2	not measured	none	total cycle	No sticking. Few cracks. Delaminated.
13.	Silicon carbide	1.7x4.2	Pt Embossed	3300	1000	60	air	not measured	none	hold	Stuck somewhat around edge.
14.	Stainless steel	1.7x4.2	Pt Embossed	3480	1000	60	N_2	not measured	none	total cycle	Stuck badly. Separated at center layer.
15.	0.002" tungsten	1.7x4.2	Pt Embossed	3680	1000	75	N_2	not measured	none	total cycle	Some sticking.
16.	Phlogopite	1.7x4.2	none	3600	1000	300	N_2	H_c=1.23 Oe Fair squareness	1260°C 10 hr CO_2	hold	Phlogopite removed in anneal.
17.	Phlogopite	1.7x4.2	none	3600	1000	360	N_2	Good loop	1260°C 10 hr CO_2	hold	Phlogopite abraded before anneal.
18.	Phlogopite	1.7x4.2	none	3300	1100	300	N_2	Poor loop	none	hold	Some reaction with phlogopite.
19.	Phlogopite	1.7x4.2	none	3300	1000	240	N_2	not measured	none	hold	Cracked. Center 0.020" narrower than ends.
20.	Phlogopite	1.7x4.2	none	3300	1000	240	N_2	good loop	1260°C 10 hr CO_2	hold	Broken in handling.
21.	Phlogopite	1.7x4.2	none	3400	1000	300	N_2	fair loop	1260°C 10 hr CO_2	hold	Mechanically perfect. Phlogopite not removed.

TABLE IV (Continued)

Type 47 Material Calcined @900°C for 2 hr in Air											
No.	Contact Material	Sample Size (in.)	Conductor	Pressure (lb/in.^{2})	Temp. (°C)	Time (min.)	Atmos-phere	Magnetic Property	Anneal	Pressure Applied	Comments
22.	Phlogopite	1.570 x 3.515	Pt Embossed	4350	1000	240	N_2	not measured	1230°C 10 hr CO_2, cool N_2	hold	Shrinkage cracks during anneal. Phlogopite reaction.
23.	Phlogopite	1.555 x 3.520	Pt Embossed	4350	1000	180	N_2	not measured	1230°C 10 hr CO_2, cool N_2	hold	Shrinkage cracks during anneal. Phlogopite reaction.
24.	Phlogopite	1.555 x 3.520	Pt Embossed	4350	970	300	N_2	Excellent on pulse test	1230°C 10 hr CO_2, cool N_2	hold	Freshly ground TZM pressure plates.
25.	Phlogopite	1.555 x 3.520	Pt Embossed	4350	1002 1036	180 90	N_2	not tested	none	hold	Phlogopite reacted - thrown out.
26.	Yttralox	0.530 x 0.850	none	5000	1000 to 1060	120	N_2	not tested	none	hold	Ferrite and Yttralox reacted and bonded together.
27.	Phlogopite	3.505 x 1.560	Pt Embossed	4400	1025	240	N_2	not tested	none	hold	Iridium sheets 0.002" placed between phlogopite and TZM. No reaction. Sample cracked.
28.	Phlogopite	3.505 x 1.560	Pt Embossed	4400	1025	240	N_2	not tested	none	hold	Tungsten sheets 0.002" placed between phlogopite and TZM. Bad reaction between all.
29.	Phlogopite	3.505 x 1.560	Pt Embossed	4400	1000	60	N_2	Fair on pulse test	1230°C 16 hr CO_2, cool N_2	hold	Pt sheets 0.002" placed between phlogopite and TZM. No reaction. No cracks.
30.	Phlogopite	3.505 x 1.560	Pt Embossed	4400	1040	300	N_2	not tested	none	hold	Same except many cracks.
31.	Phlogopite	3.440 x 1.545	Pt Embossed	4500	1050	240	N_2	not tested	none	hold	Severe reaction with phlogopite.
32.	Phlogopite	3.440 x 1.545	Pt Embossed	4500	1000	60	N_2	Fair on pulse test	1230°C 10 hr CO_2, cool N_2	hold	No reaction.
33.	Phlogopite	3.440 x 1.545	Pt Embossed	4500	1062	30	N_2	Good on pulse	1230°C 10 hr CO_2, cool N_2	hold	No sticking. No reaction.
34.	Phlogopite	3.560 x 1.505	Pt Embossed	4500	1080	30	N_2	Bad on pulse	1230°C 10 hr CO_2, cool N_2	hold	No sticking. No reaction. New batch of ferrite.
35.	Phlogopite	3.453 x 1.468	Pt Embossed	4730	1060	30	N_2	Bad on pulse	1230°C 10 hr CO_2, cool N_2	see comments	Pressure applied at 980°C. No cracks. No reaction. Phlogopite had to be abraded.
36.	Phlogopite	3.550 x 1.500	Pt Embossed	4500	1060	30	N_2	Poor on pulse	1230°C 10 hr CO_2, cool N_2	see comments	Pressure applied at 980°C. One shrinkage crack after anneal.
37.	Phlogopite	3.415 x 1.420	Pd Embossed	4950	1060	30	N_2	Poor on pulse	1230°C 10 hr CO_2, cool N_2	see comments	Pressure applied at 980°C. Distorted in anneal.
38.	Phlogopite	3.440 x 1.455	Pd Embossed	4800	1060	30	N_2	not tested	1230°C 10 hr CO_2, cool N_2	see comments	Pressure applied at 980°C. Shrunk and cracked badly in anneal.
39.	Phlogopite	0.560 x 0.560	none	2000	1048	30	N_2	not tested	none	hold	Spreading crack. Looked as though pressure was higher than thought.
40.	Phlogopite	3.412 x 1.425	Pd Embossed	4900	1048	30	N_2	Bad on pulse	1230°C 12 hr CO_2, cool N_2	900°C	0.025" more shrinkage on one end than on the other. No reaction.
41.	Phlogopite	3.598 x 1.462	Pt Embossed	4600	1000	90	N_2	not tested	1230°C 10 hr CO_2, cool N_2	hold	Cracked along one edge. Otherwise good.

TABLE IV (Continued)

No.	Contact Material	Sample Size (in.)	Conductor	Pressure (lb/in.^{2})	Temp. (°C)	Time (min.)	Atmos-phere	Magnetic Property	Anneal	Pressure Applied	Comments
				Type 47 Material Calcined @1040°C for 2 hr							
42.	Phlogopite	1.7x4.2	Pt Embossed	4200	1000	300	N_2	not measured	none	hold	Phlogopite reacted badly.
43.	Phlogopite	1.7x4.2	Pt Embossed	4200	1000	300	N_2	not measured	none	hold	Phlogopite reacted badly.
				Type 47 Material Calcined @1040°C for 2 hr in Air							
44.	Phlogopite	1.600 x 3.555	Pt Embossed	4300	1000	240	N_2	not measured	none	hold	Badly pitted due to phlogopite reaction.
45.	Phlogopite	1.600 x 3.555	Pt Embossed	4300	1000	240	N_2	not measured	none	hold	WC backup plated used instead of TZM. Reaction was extremely bad.
				Type 47 Material Calcined @1150°C for 2 hr							
46.	Phlogopite	1.7x4.2	Pt Embossed	3150	1100	60	vac.	not measured	1205°C air 1190°C N_2	total cycle	Tiny cracks all over.
47.	Phlogopite	1.7x4.2	Pt Embossed	3150	1100	60	vac.	not measured	1205°C air 1190°C N_2	total cycle	Tiny cracks all over.
48.	Phlogopite	1.7x4.2	Pt Embossed	4400	1000	120	vac.	not measured	none	hold cool	Some cracks.
				Type 47 Material Calcined @1150°C for 2 hr in Air							
49.	Phlogopite	1.7x4.2	Pt Embossed	4200	1000	240	N_2	Pulse tested unusable	1260°C 10 hr CO_2, N_2 cool	hold	Shrinkage cracks developed during anneal.
50.	Phlogopite	3.535 x 1.555	Pt Embossed	4300	1000	240	N_2	not tested	1260°C 10 hr CO_2, N_2 cool	hold	Bowed during anneal. No cracks.
				Type 47 Material Calcined @1175°C for 2 hr							
51.	Iridium	1.7x4.2	Pt Embossed	4400	1000	60	N_2	not measured	none	total cycle	Mostly whole. Stuck in few small spots.
52.	Iridium	1x1	Electro-formed gold	5000	1000	60	N_2	not measured	none	hold	Ferrite released. Gold stuck badly.
				Type 47 Material Calcined @1260°C for 10 hr in CO_2							
53.	Silicon carbide	1.7x4.2	Pt Embossed	3680	1000	30	air	not measured	none	total cycle	No cracking. Some sticking.
54.	Silicon carbide, high polish	1.7x4.2	Pt Embossed	4120	1000	60	air	not measured	none	total cycle	Stuck on bottom only. Broke.
55.	Phlogopite	1.7x4.2	Pt Embossed	4570	1000	60	N_2	not measured	none	total cycle	Looked good. Underfired. Soft.
56.	Phlogopite	1.7x4.2	Pt Embossed	4570	1100	60	N_2	not measured	none	total cycle	Badly cracked. Hard.

TABLE IV (Continued)

No.	Contact Material	Sample Size (in.)	Conductor	Pressure (lb/in.^{2})	Temp. (°C)	Time (min.)	Atmos-phere	Magnetic Property	Anneal	Pressure Applied	Comments
Type 47 Material Calcined @1260°C for 10 hr in CO_2 (Cont'd.)											
57.	Iridium	1.7x4.2	Pt Embossed	4380	1000	35	air	not measured	none	total cycle	Stuck. Broke.
58.	Iridium	1.7x4.2	Pt Embossed	2920	1000	65	N_2	not measured	none	total cycle	Stuck. Cracked.
59.	Phlogopite	1.7x4.2	Pt Embossed	4400	1000	180	N_2	not measured	none	hold	Many microscopic cracks.
60.	Phlogopite	0.25x4	none	12,000	1000	300	N_2	no loop	1200°C CO_2 10 hr	hold	No cracks.
61.	Phlogopite	1.7x4.2	none	3300	1000	180	N_2	no loop	1200°C CO_2 10 hr	hold	No cracks.
62.	Phlogopite	1.7x4.2	none	3300	1000	180	N_2	no loop	1260°C CO_2 10 hr	hold	No cracks.
63.	Phlogopite	1.7x4.2	none	3400	930	300	N_2	fair loop only after anneal	1260°C CO_2 10 hr	hold	No cracks.
64.	Phlogopite	6 pieces 0.25x1.1	none	13,700	1000	240	N_2	no loop before anneal	1260°C CO_2 10 hr	hold	No cracks.
65.	Phlogopite	4 pieces 0.25 x 0.875	none	14,000	1000	300	N_2	poor loop after no loop before	1260°C CO_2 10 hr	hold	No cracks.
66.	Phlogopite	1.7x4.2	none	3300	1000	120	N_2	very poor loop after fair loop after anneal	1260°C CO_2 10 hr	hold	No cracks.
67.	Phlogopite	4 pieces 0.5x1	none	14,000	1000	240	N_2	not measured	none	hold	Phlogopite reacted with ferrite.
Type 47 Material Calcined @1340°C for 1/2 hr in Air											
68.	Phlogopite	1x1	Au Electro-formed	5000	1000	15	N_2	not measured	none	hold	No cracks. Soft. Back to front short.
69.	Phlogopite	1.125 x 1.125	none	6000	1000	15	N_2	not measured	none	hold	Looked fired. No cracks. Broke easily.
70.	Phlogopite	1.125 x 1.125	none	7900	1000	15	N_2	not measured	none	total cycle	Looked fired. Broken in few places.
71.	Phlogopite	1.125 x 1.125	none	5000	1000	15	N_2	not measured	none	hold	Two cracks.

TABLE IV (Continued)

No.	Contact Material	Sample Size (in.)	Conductor	Pressure (lb/in.^{2})	Temp. (°C)	Time (min.)	Atmos-phere	Magnetic Property	Anneal	Pressure Applied	Comments
				C. Type 3515 Material Calcined @1040°C for 1 hr							
72.	Silicon carbide	1x1	Au Electro-formed	4000	1000	35	air	not measured	none	total cycle	Stuck.
73.	Phlogopite	1.7x4.2	none	4800	1060	180	N_2	H_c=1.87 loop fair H_c=1.03 loop good anneal	1150°C N_2 9 hr	hold	Phlogopite not removed. Badly cracked.
				Type 3515 Material Calcined @1040°C for 2 hr in Air							
74.	Phlogopite	3.585 x 1.460	Pt Embossed	4600	1048	60	N_2	not tested	none	900°C hold	Ferrite No. 010668-1. Considerable ferrite flow. Blisters, reaction, warped.
75.	Phlogopite	3.580 x 1.455	Pt Embossed	4800	1048	60	N_2	not tested	none	1100°C hold	No phlogopite reaction. Some blistering. Some flow.
76.	Phlogopite	4.180 x 1.695	none	3500	1048	60	N_2	not tested	none	900°C hold	Phlogopite stuck. After phlogopite was removed by abrading, sample broke very easily.
77.	Phlogopite	3.575 x 1.455	none	4800	1000	300	N_2	not tested	none	hold	Several reaction spots. Blisters along one side.
				Type 3515 Material Calcined @1150°C for 9 hr in Air							
78.	Phlogopite	1.7x4.2	Pt Embossed	3200	1100	60	N_2	not measured	none	hold cool	Badly broken.
79.	Phlogopite	1.7x4.2	Pt Embossed	3000	1100	60	N_2	not measured	none	hold	Badly broken.
80.	Phlogopite	1.7x4.2	Pt Embossed	3100	1100	60	N_2	not measured	none	total cycle	Many tiny cracks.
81.	Phlogopite	1.7x4.2	Pt Embossed	3150	1040	60	N_2	no good on pulse	none	total cycle	Looked good.
82.	Phlogopite	1.7x4.2	Pt Embossed	3150	1100	60	vac.	not measured	1205°C 9 hr air, N_2 cool	total cycle	Many cracks.
83.	Phlogopite	1.7x4.2	Pt Embossed	3150	1100	60	vac.	not measured	none	total cycle	Many cracks.
84.	Phlogopite	1.7x4.2	Pt Embossed	4400	1000	120	vac.	not measured	none	hold cool	Few cracks.
				Type 3515 Material Calcined @1150°C for 2 hr in Air							
85.	Phlogopite	3.500 x 1.535	Pt Embossed	4470	1080	35	N_2	bad on pulse	none	see comments	Pressure applied at 980°C. Few cracks before anneal.
86.	Phlogopite	3.475 x 1.512	Pt Embossed	4600	1048	30	N_2	bad on pulse	2100°F 10 hr air, N_2 cool	hold	Looked good but ferrite soft.
87.	Phlogopite	3.515 x 1.535	Pt Embossed	4400	1048	60	N_2	not tested		900°C hold	Ferrite soft.

TABLE IV (Continued)

No.	Contact Material	Sample Size (in.)	Conductor	Pressure (lb/in.^{2})	Temp. (°C)	Time (min.)	Atmos-phere	Magnetic Property	Anneal	Pressure Applied	Comments
Type 3515 Material Calcined @1150°C for 2 hr in Air (Cont'd.)											
88.	Phlogopite	3.683 x 1.685	none	3800	1048	30	N_2	fair loop good loop	none 1040°C 12 hr air, N_2 cool	900°C hold	Ferrite No. 050867-1.
89.	Phlogopite	3.655 x 1.670	none	3900	1048	120	N_2	fair loop good loop	none 1040°C 12 hr air, N_2 cool	900°C hold	Ferrite No. 050867-1.
Type 3515 Material Calcined @1205°C for 2 hr											
90.	Iridium	1.7x4.2	Pt Embossed	3150	1000	60	N_2	not measured	none	total cycle	Stuck, many cracks.
91.	Polished silicon carbide	1.7x4.2	Pt Embossed	3150	1000	60	air	not measured	none	total cycle	No sticking, soft, no cracks.
92.	Silicon carbide	1.7x4.2	Pt Embossed	3090	1000	60	air	not measured	none	total cycle	Stuck and broke.
93.	Silicon carbide	1.7x4.2	Pt Embossed	3240	1000	60	air	not measured	none	total cycle	Stuck very badly.
94.	Phlogopite	1.7x4.2	Pt Embossed	3000	1000	60	N_2	not measured	none	total cycle	Very slight sticking. Many tiny cracks. Held together by phlogopite and conductors.
95.	Phlogopite	1.7x4.2	Pt Embossed	4400	1000	60	vac.	not measured	none	total cycle	Broken in few places.
96.	Phlogopite	1.7x4.2	none	2000	1050	60	air	Good squareness H_c=1.33 Oe	1120°C 9 hr N_2	hold and cool	Broken in several pieces.
Type 3515 Material Calcined @1260°C for 2 hr in Air											
97.	Tungsten carbide	1.7x4.2	Pt Embossed	3300	1000	15	N_2	not measured	none	hold	Stuck badly, cracked.
98.	Tungsten carbide	1.7x4.2	Pt Embossed	3480	1000	15	vac.	not measured	none	total cycle	Stuck badly; no visible cracks.
99.	Iridium	1.7x4.2	Pt Embossed	3480	1000	15	vac.	not measured	none	total cycle	Stuck slightly.
100.	Iridium	1.7x4.2	Pt Embossed	3480	1090	15	vac.	usable on pulse	1000°C air 1 hr	total cycle	Stuck slightly.
101.	Silicon carbide	1.7x4.2	Pt Embossed	3840	1000	60	air	not measured	none	total cycle	Stuck. No visible cracks.
102.	Molybdenum	1.7x4.2	Pt Embossed	3300	1000	60	vac.	not measured	none	total cycle	Ferrite reacted.
103.	Molybdenum	1.7x4.2	Pt Embossed	3680	1000	60	N_2	not measured	none	total cycle	Ferrite reacted.
104.	Tungsten	1.7x4.2	Pt Embossed	3680	1000	30	vac.	not measured	none	total cycle	Some sticking.
105.	Tantalum	1.7x4.2	Pt Embossed	3680	1000	60	vac.	not measured	none	total cycle	Ferrite reacted.

IV. WORD SELECTION DRIVE CIRCUITRY

A. Introduction

The basic requirements of the integrated word selection-drive circuitry are to select and to drive one of 65,536 laminated ferrite memory word lines, 64 planes of 1024 words, with bi-directional read and write current pulses. The drive circuitry must be capable of generating a 150- to 200-mA peak read current, followed by a 75- to 100-mA write current of the opposite polarity, with both rise-times and pulse widths of approximately 200 nsec. The words are 400 crossovers long. The selection of a particular word within a given memory module is accomplished through two levels of decoding. One of 64 individual planes and one of 1024 lines are simultaneously selected by their associated address decoders. To meet the system requirements for a 2- to 3-μsec cycle time, word decoding should not exceed 0.5 μsec. The main emphasis in the design of the integrated-circuit selection-drive system was to minimize power consumption. The system has been designed, breadboarded, partially integrated, and evaluated.

In commercial practice, circuits incorporating n-p-n bipolar transistors and transformers have been used to generate bi-directional current pulses. The quiescent power dissipation exhibited by such circuits is generally negligible. Since no transformer-coupled drive scheme lends itself to integrated-circuit (I-C) fabrication, other techniques were investigated. Circuits incorporating only n-p-n bipolar transistors as active components consume an excessive amount of power. Strips of MOS switches for driving laminated ferrites have been previously fabricated (Refs. 4, 5). However, the factory yield for these structures that operate at relatively high current levels was expected to be poor. Although complementary bipolar circuits have been designed to provide bi-directional word drive current pulses, there is still some difficulty in fabricating both high-quality n-p-n and p-n-p devices on a common substrate. The approach pursued for meeting the requirements of this program incorporates n-p-n bipolar transistors and p-channel MOS enhancement devices (BIMOS). This technique is compatible with present I-C technology.

B. Design and Breadboard Results of Word-Drive Circuit

The BIMOS word driver, shown in Figure 14, has been designed and fabricated in I-C form. A driver consists of three n-p-n bipolar transistors (Q_1, Q_2, and Q_3), one MOS device (Q_4), and three diffused resistors (R_1, R_2, and R_3). The bases of transistors Q_1 and Q_2 are connected together at point V_{IN} and driven, along with 63 identical circuits in unselected planes, by the output of the 1024-address decoder. A write line (V_W), read line (V_R), positive supply line (V_S), and a line which carries the write current, are all common to a given plane. The lines V_R and V_W are pulsed sequentially to effect plane selection. The output of the circuit, V_o, taken at the connection of the emitter of Q_3 and the collector of Q_2, drives the 400-crossover-long word line. Two precision resistors, R_R and R_W, external to the circuit and shared by a multiplicity of drivers, are used for setting the magnitude and rise-time of the read and write current pulses, respectively. The values for the supply voltages and current-setting resistors, given in the schematic, correspond to a read and write pulse of 150 and 75 mA, respectively.

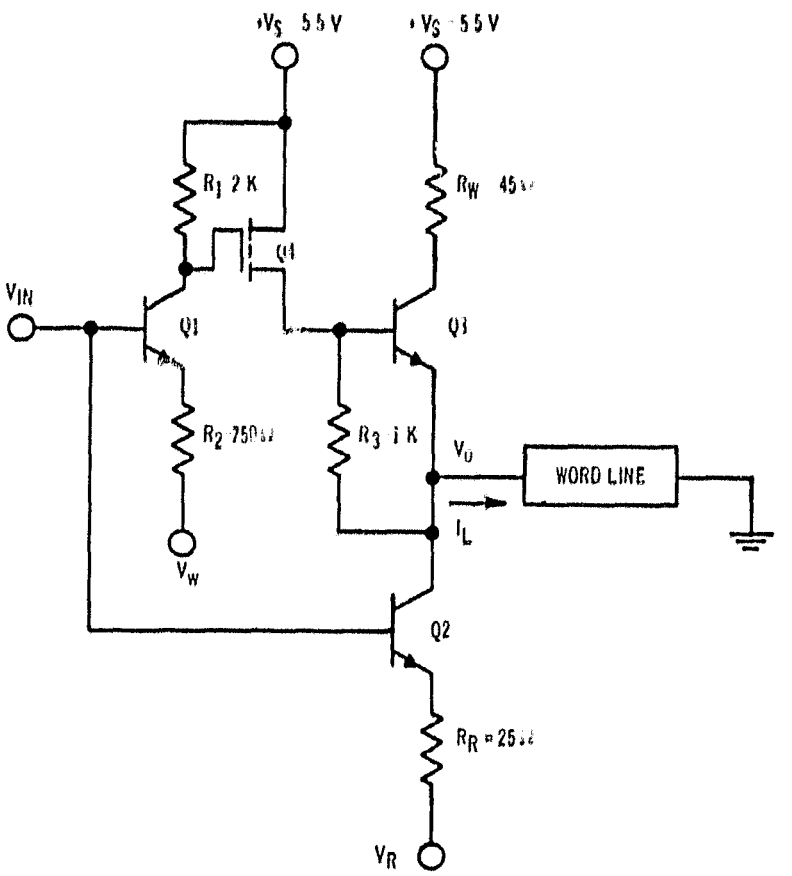


Figure 14. Schematic of BIMOS word-drive circuit (MOS substrate assumed at V_S).

The operation of the circuit is as follows. In the quiescent state, V_{IN} = -10 V and $V_W = V_R$ = -5.5 V. Under these conditions, the emitter-base junctions of transistors Q_1 and Q_2 are reverse-biased, and the devices are nonconducting. Since no current flows through Q_1, the p-channel enhancement MOS device Q_4 is also biased in the off state, i.e., there is zero gate-to-source potential. In addition, because of the zero base current, transistor Q_3 is nonconducting. Therefore, no current flows into the word line and the output voltage is at ground. The standby power consumed in the driver, dependent upon transistor leakage currents, is estimated at 1 to 10 μW. For a selected address, the input V_{IN} is pulsed from -10 to -5.5 V. For nonselected planes, V_W and V_R remain at -5.5 V, all transistors are biased in the off state, and there is still zero current in the word line. A read cycle is begun by pulsing V_R to -10 V for a selected plane, thus forward-biasing transistor Q_2, which produces a negative current in the word line. Initially, transistor Q_2 saturates because of the inductive load. The steady-state read current, determined by the emitter current of Q_2, is given by

$$I_L = -I_C = -\frac{V_{IN} - V_{be} - V_R}{R_R} = -\frac{-5.5 - 0.75 - (-10)}{25} = -150 \text{ mA} \qquad (1)$$

where V_{be} = 0.75 V is assumed (for transistor Q_2). The current is thus not a function of the beta of Q_2. The pulse rise-time is a function of the magnitude of V_R. The read cycle is terminated by returning V_R to -5.5 V.

Correspondingly, for the write cycle V_W is pulsed to -10 V, thus forward-biasing transistor Q_1. MOS transistor Q_4 also conducts because of the 10-V gate-to-source voltage developed. It supplies base current to transistor Q_3, which acts as a saturated switch, and a positive current flows in the word line. The fact that Q_3 saturates makes the magnitude of the write current insensitive to device parameter variations. The 10-V gate-to-source voltage, V_{GS}, of unit Q_4 is independent of the absolute values of R_1 and R_2, and is a function only of their relative values as seen in the following expression.

$$V_{GS} = \frac{-R_1}{R_2} \quad (V_{IN} - 0.75 - V_W) \tag{2}$$

For R_1 = 2 kΩ, R_2 = 750 Ω, V_{IN} = -5.5 V, and V_W = 10 V, V_{GS} = -10 V. In I-C form, the ratio R_1/R_2 can be held to approximately ± 3%. The steady-state write current is given by

$$I_L = \frac{V_S - V_{ce}}{R_W + R_L} \approx \frac{5.5 - 0.5}{45 + 20} \approx 75 \text{ mA} \tag{3}$$

where V_{ce} is the collector-to-emitter voltage of transistor Q_3 and R_L is the assumed equivalent load resistance. The write pulse rise-time is given by

$$t_r \approx 2.3 \quad \frac{L}{R_W + R_L} \tag{4}$$

where L is the effective load inductance. The write cycle is completed by V_W returning to -5.5 V. Resistor R_3 allows transistor Q_3 to discharge at the end of the write cycle so that the load current can return to zero. A system timing diagram appears in Figure 15.

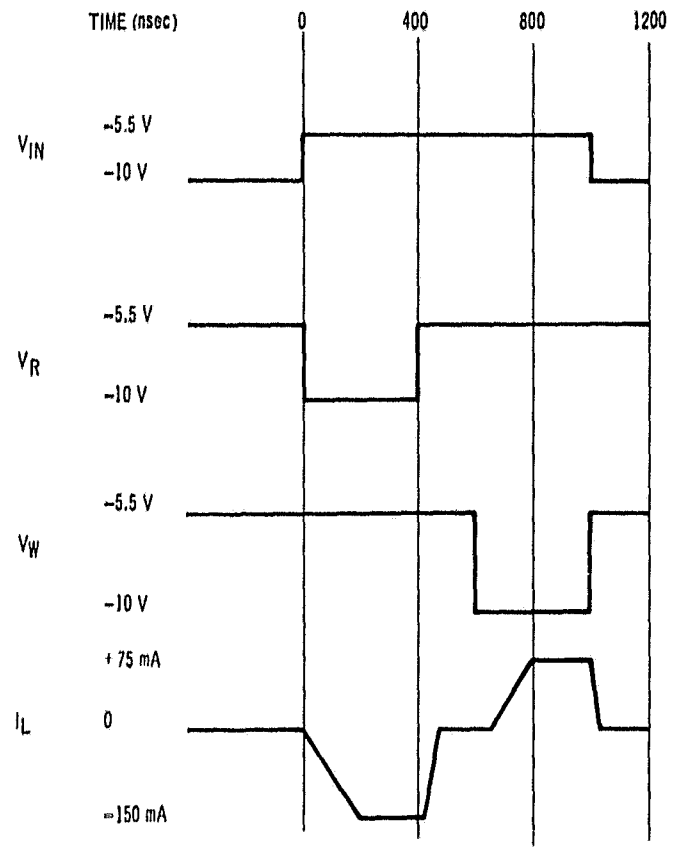


Figure 15. Word system timing diagram.

The three bipolar transistors used for the breadboard evaluation of the drive circuit were obtained from an experimental RCA integrated-circuit, which was not gold-doped. The channel dimensions for the p-channel MOS device are 10 mils in width and 0.3 mil in length. The load was a laminated ferrite memory of 400 crossovers. Figures 16(a) and (b) show waveforms for the word currents and some pertinent voltages, respectively. The resistors R_W and R_R were capacitively loaded with 3000 pF and 1000 pF, respectively, to simulate the unselected word lines of the same plane. The estimates are that a total of five R_W resistors and twenty R_R resistors will be required per plane. The magnitudes of both the read and write currents are close to the predicted values. Pulse rise-times and durations (at peak current) are approximately 200 nsec each. The 200-nsec rise-time for the write cycle indicates an effective load inductance of nearly 6 μH [from Eq. (4)]. The voltage waveforms indicate that bipolar transistors with collector-to-emitter breakdown voltages in excess of 15 V will operate reliably.

C. Fabrication of Integrated BIMOS Word Driver

The BIMOS technology combines the p-channel MOS with the n-p-n bipolar transistor on one substrate. Figure 17 shows the common silicon substrate compatibility of the BIMOS process. The compatibility is further emphasized by the fact that the critical diffusion steps for the bipolar do not appreciably interact with the critical oxide steps of the MOS.

Artwork was generated and the photomasks were produced for processing the integrated BIMOS word-driver pellet, consisting of a strip of eight individual word-drive circuits on a single substrate. The input-output leads are on 15-mil centers. The pellet was designed to have bonding pads large enough to permit soldering of leads or beam leading. Each individual driver circuit requires a 48-mil by 15-mil silicon area. The overall pellet size for the eight drivers, including all bonding pads, is 160 mils by 70 mils. A photomicrograph of the chip is shown in Figure 18.

The integrated BIMOS driver was fabricated with standard bipolar integrated-circuit techniques and processes wherever possible. A total of eight photomasks were used, one more than required for the bipolar circuit alone. The additional mask provided the channel oxide for the MOS transistor. The silicon wafer was a standard 25 to 50 Ω-cm p-type substrate, cut on [100]-axis and one face polished with HCl gas. The basic processing sequence is given in Table V. Although the table gives the standard sequence, in some cases, the base diffusion (step 5) was done before the base contact diffusion (step 4). The reversal in the sequence was due to mask alignment difficulties when the normal sequence was used. The source and drain of the MOS transistor were diffused concurrently with the bipolar base diffusion, and the MOS contacts with the base contact diffusion.

Several groups of wafers have been processed. In one group, the bipolar transistors exhibited low collector-to-base breakdown voltages. A second batch yielded devices with poor betas at the high current levels of interest,

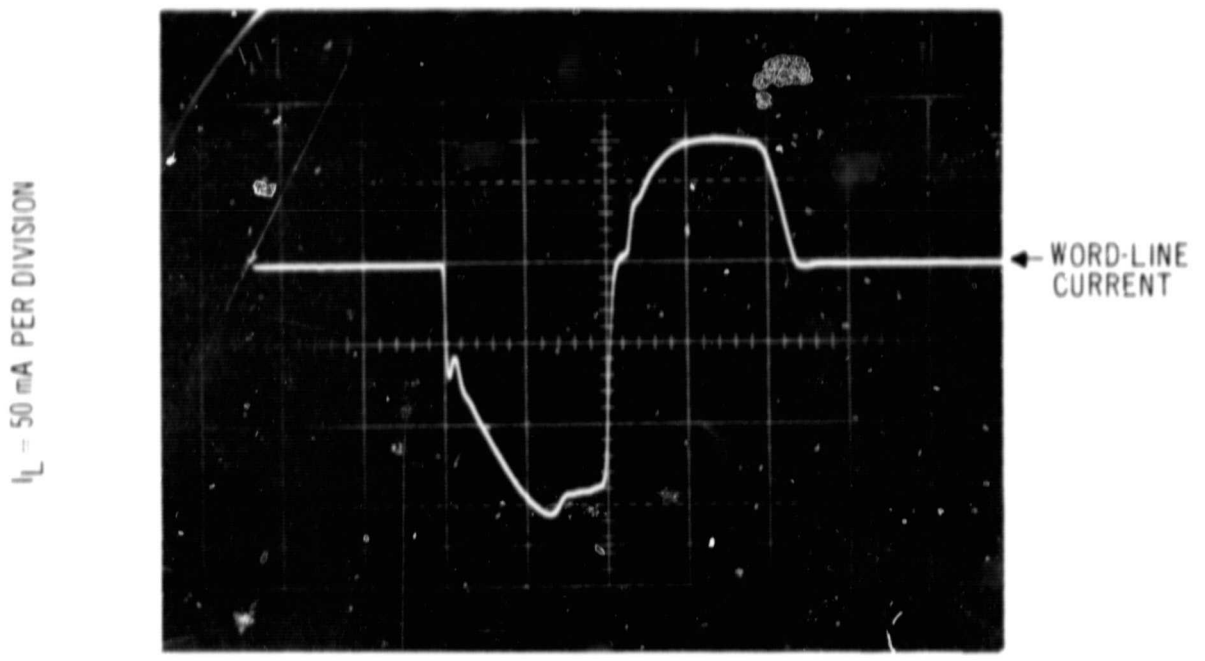


Figure 16. Oscillograms of word-line current and voltage waveforms.

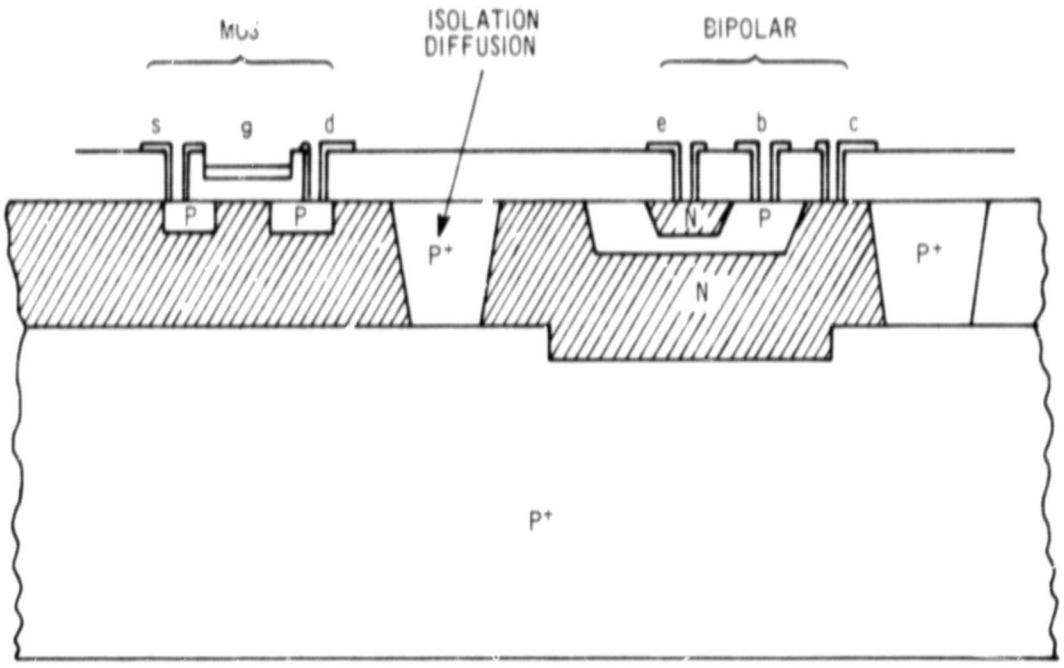


Figure 17. BIMOS cross-sectional view.

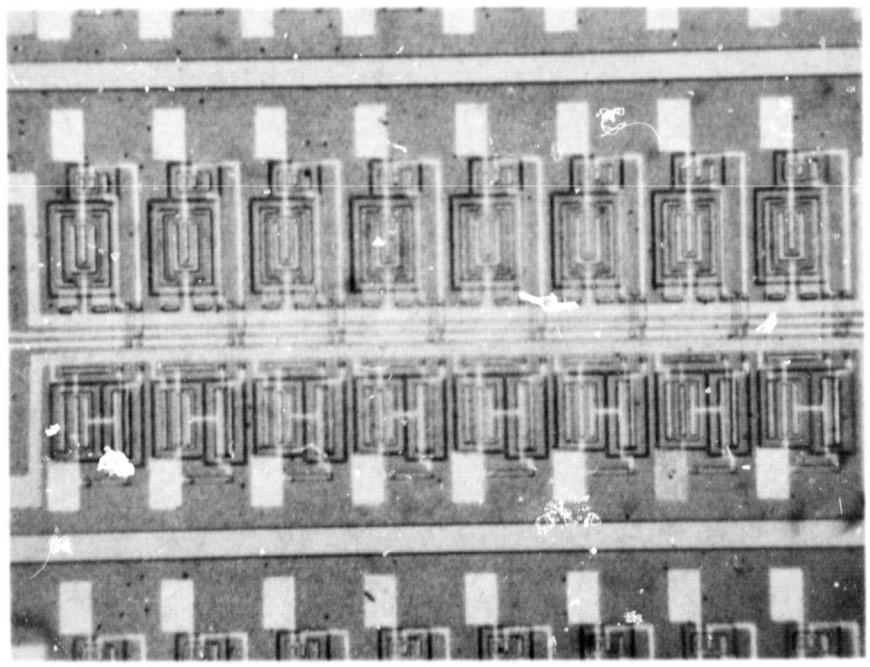


Figure 18. Photomicrograph of BIMOS word-drive pellet.

TABLE V

BIMOS PROCESS SEQUENCE

1.	n^+ pocket diffusion (antimony)
2.	epitaxial growth n^- 1 Ω-cm, 0.4 mil thick
3.	isolation diffusion p^+ (boron nitride)
4.	contact and tunnel diffusion, p^+ (boron nitride)
5.	base and resistor diffusion p (boron nitride)
6.	emitter diffusion n^+ (phosphorus oxychloride)
7.	MOS channel oxide
8.	open contact areas
9.	metallization (aluminum)

i.e., I_C = 150 mA. Bipolar devices from a third group exhibited betas of 100 at I_C = 100 mA. However, these devices appear to function as silicon-controlled rectifiers (or thyristors), breaking down into a low-voltage mode, as shown in Figure 19. This behavior is being investigated.

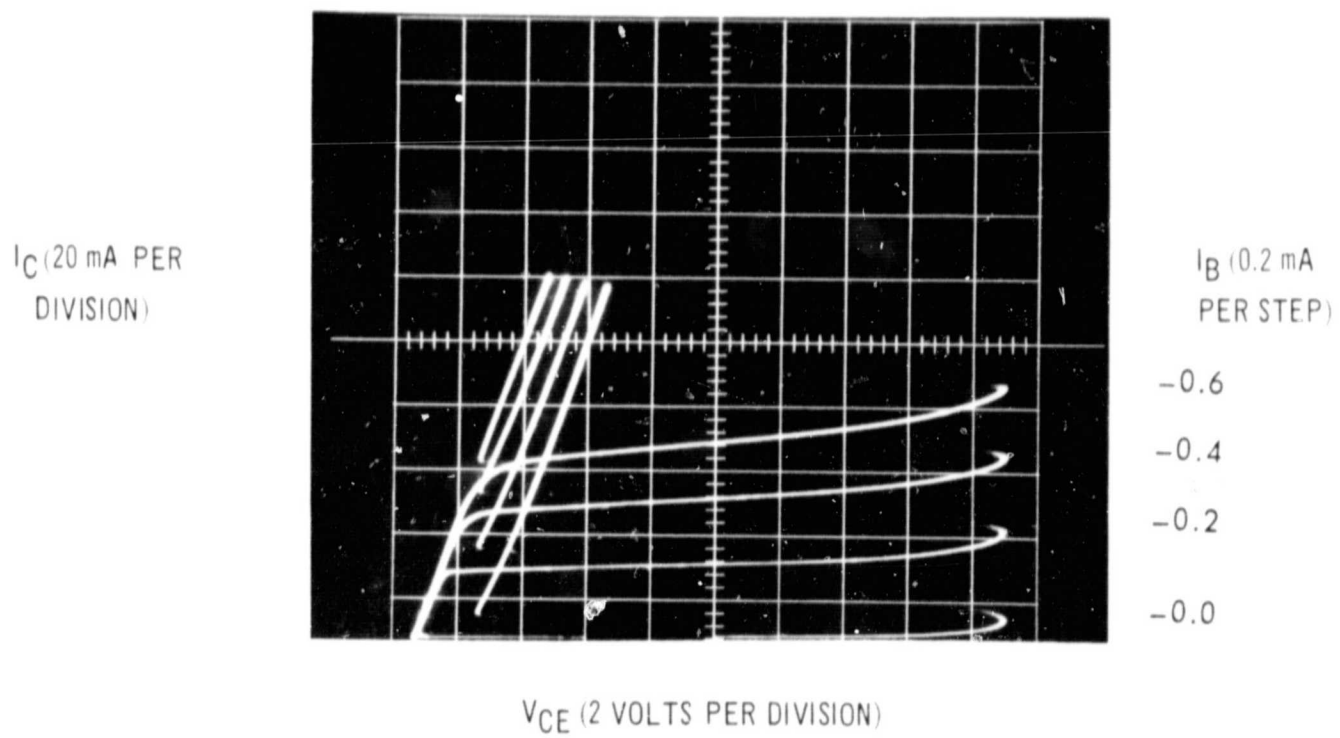


Figure 19. Output characteristics of a typical bipolar device from BIMOS word-drive pellet (Q_2 of Figure 14).

Strips of 64 MOS transistors, each with a separate input (gate) and output (drain) and with a common ground (source) were previously fabricated for driving ferrite memories (Refs. 4, 5). For this application the transistors are large, high-performance, n-channel depletion units with a channel length of 0.2 mil, a channel width of 100 mils, and a channel oxide thickness of 600 to 750 Å. The processing requires a double metallization scheme to provide crossovers for the common source connection. The process leveled off at a yield of 55 to 62 good MOS transistors per strip; one perfect strip was made. The low yield on perfect strips is mainly attributable to two causes: the large number of devices per strip and the problem of random imperfections in the critical MOS oxide. The BIMOS word driver has an MOS channel width of only 10 mils and should thus be capable of being produced at high yields, once the processing is under control.

D. Design and Breadboard Results of 1024-Output Decoder

A 1024-output decoder to mate with the word-drive circuit was designed, breadboarded, and evaluated. Besides selecting one of 1024 possible word lines, the decoder must have a low output impedance. This makes the read current supplied to the ferrite load insensitive to device parameters, i.e., transistor Q_2 (of Figure 14) operates as a grounded-base amplifier. In addition, a low impedance is necessary to drive the capacitance associated with the parallel inputs of 64 word-drivers. To satisfy these conditions, an emitter-follower output stage was designed. To minimize power dissipation, a complementary-symmetry circuit configuration is needed. Complementary MOS circuitry was considered since it is generally ideal for low-power digital applications. However, substantial technology development would have to be made to fabricate both p-channel and n-channel MOS devices, along with bipolar emitter-follower outputs, on a monolithic substrate. By substituting n-p-n bipolar devices for the n-channel MOS units, at some sacrifice in chip size and power dissipation, a decoder was designed which could be built in monolithic form using the BIMOS process.

The strobe-activated BIMOS decoder consists of 33 binary decision trees, of 32 outputs each. The 1024-output decoder, with a 10-bit binary address, is partitioned into 33 individual packages because of external pin limitations. The block diagram of the decoder, shown in Figure 20, illustrates how the 32 outputs of the first tree serve as the activating strobes for the 32 remaining packages. The basic 32-output decoder, depicted in Figure 21, is incorporated in each package. The circuit shows the five-bit binary input with corresponding address complements, which would be obtained from BIMOS inverters on the same pellet. When a given address signal is applied to lines A, B, C, D, and E, a unique path of five conducting p-channel transistors is established. Because the strobe signal is at ground potential during the quiescent state, the n-p-n bipolar devices are biased in the ON state, and all output devices are forced to the negative supply voltage, $-V_S$. Upon command, the common p-channel strobe-controlled transistor activates the selected address line and switches the output of that address line to ground. The other 31 unselected outputs remain at the negative supply voltage. When the strobe signal returns to ground, the selected output voltage reverts to $-V_S$. The complementary structure gives circuit operation that is essentially independent of device parameters. Because of the common source-drain connections inherent in MOS I-C's, the silicon area is

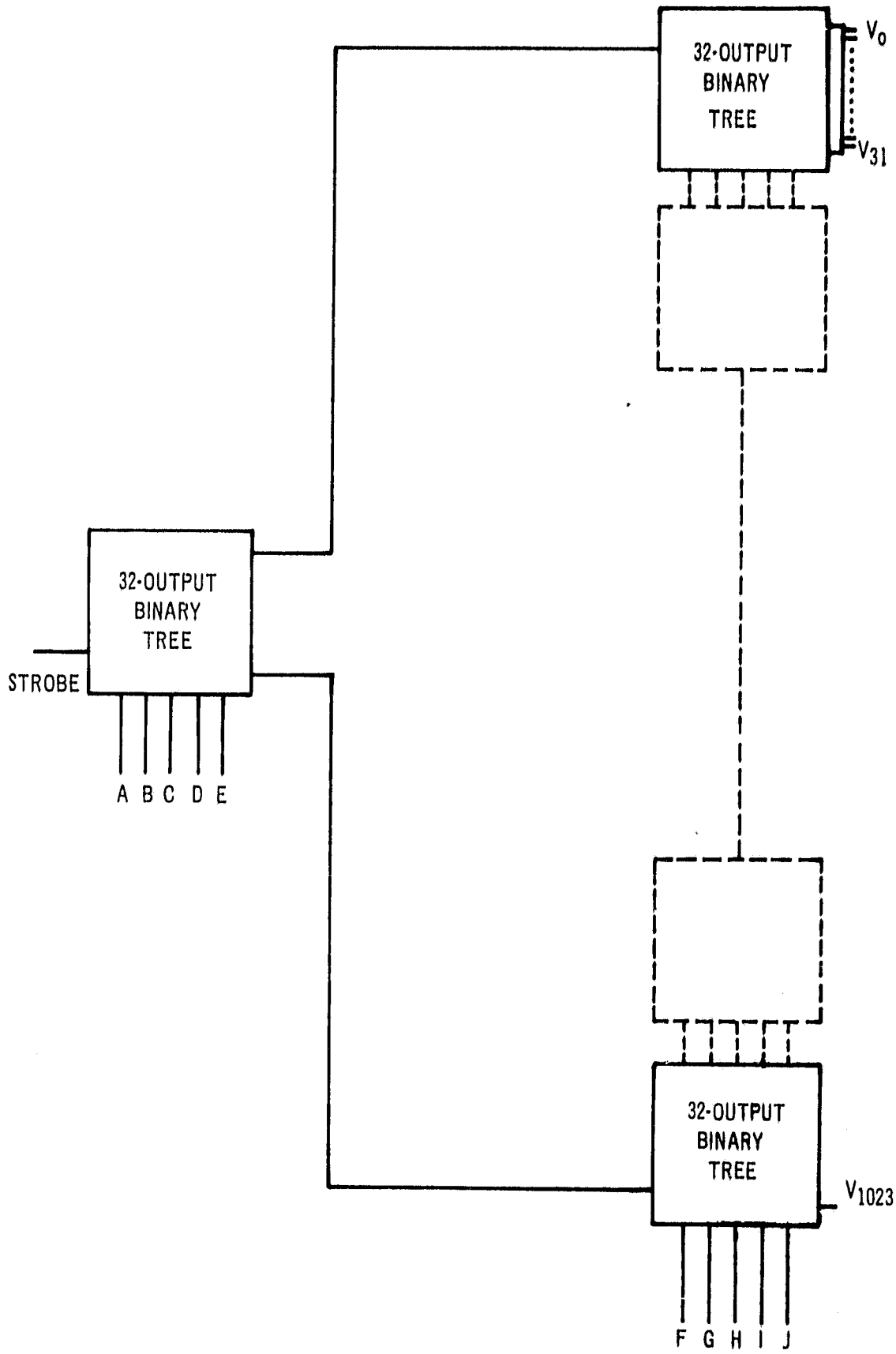


Figure 20. Block diagram of 1024-output decoder.

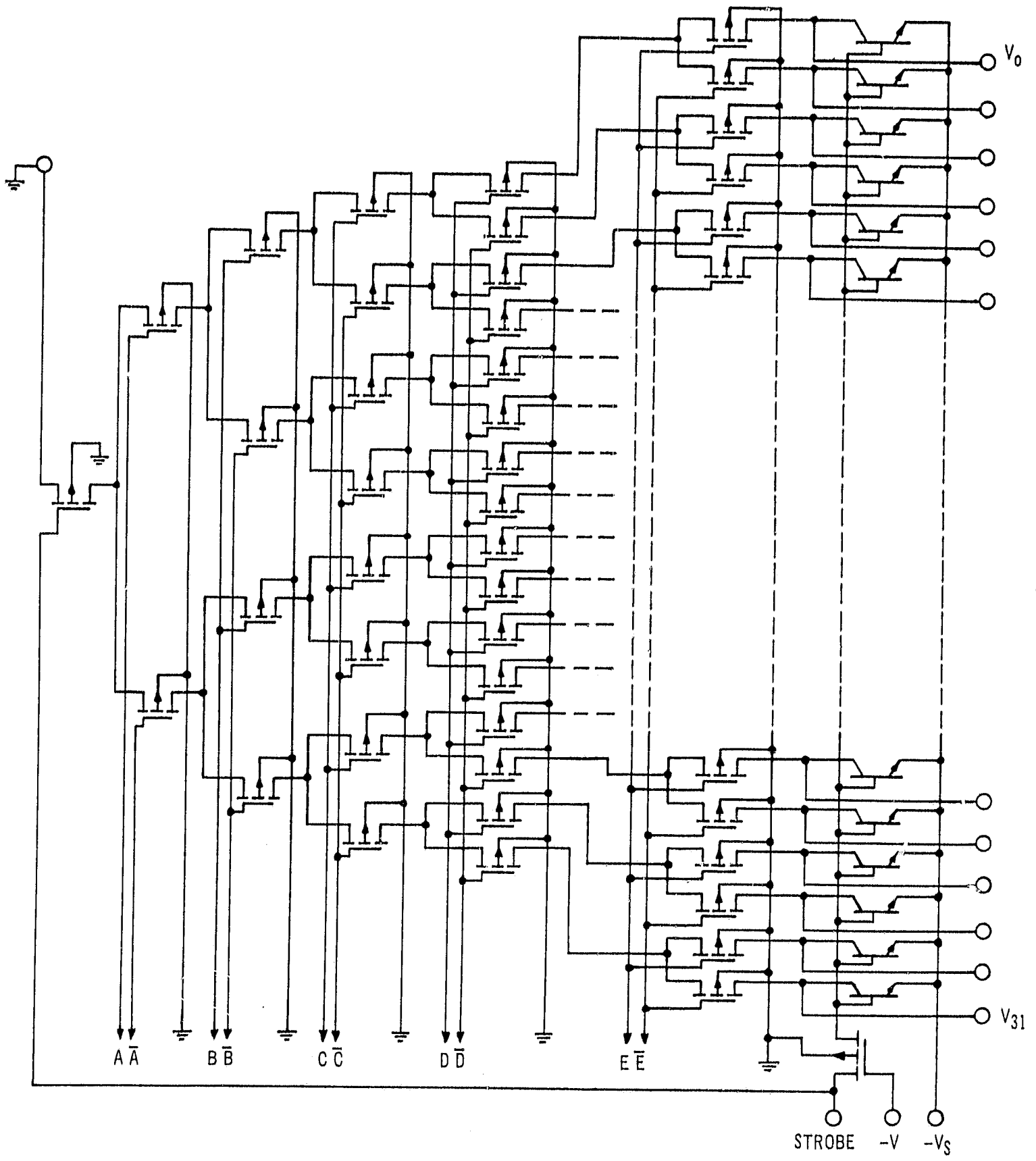
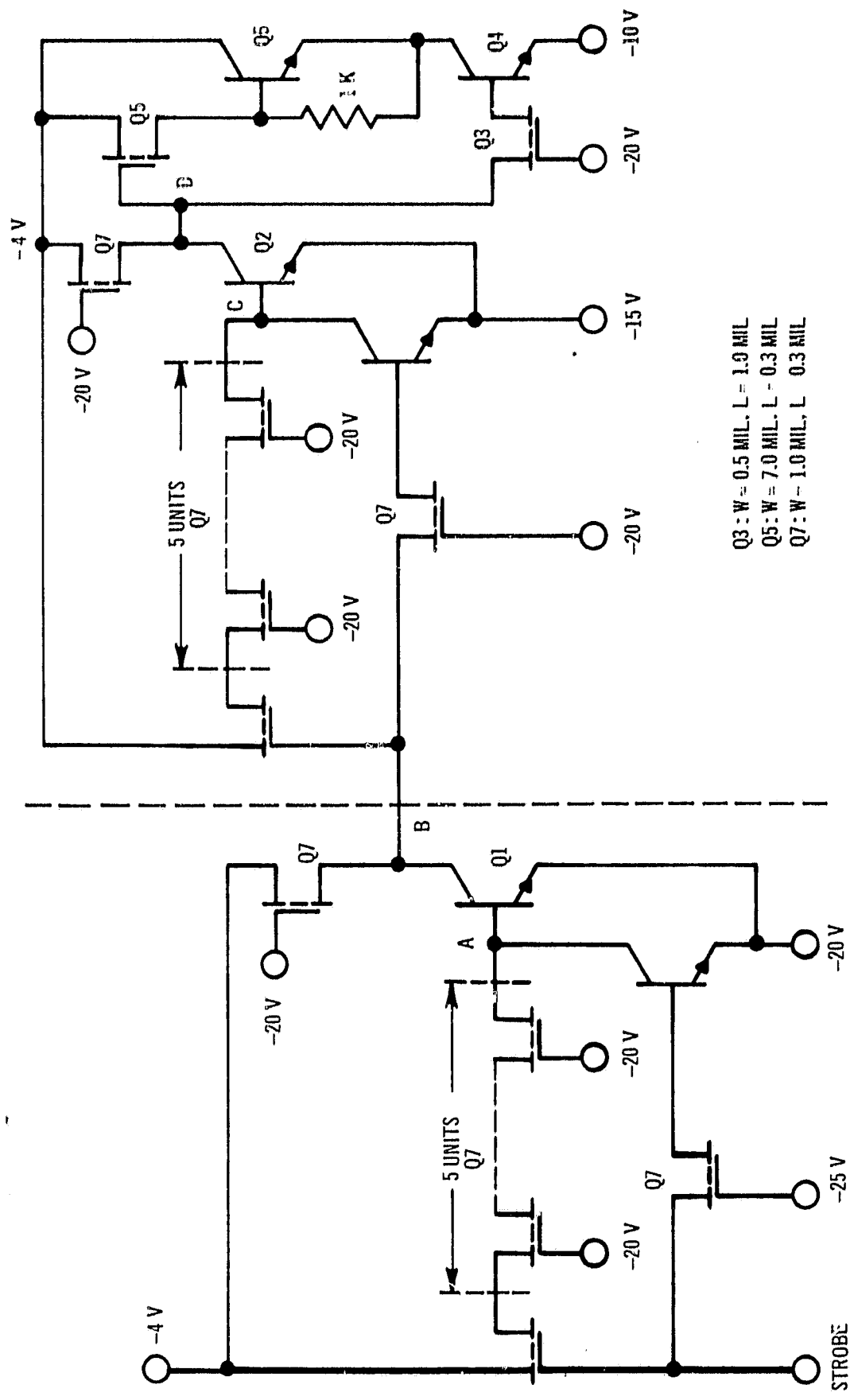


Figure 21. Schematic of basic 32-output BIMOS decoder (complement inputs to be obtained internally from inverters).



Q3 : W = 0.5 MIL, L = 1.0 MIL
Q5 : W = 7.0 MIL, L - 0.3 MIL
Q7 : W - 1.0 MIL, L 0.3 MIL

Figure 22. Schematic showing selected path of 1024-output decoder (MOS substrates assumed at -4 V).

minimized by using the bipolar devices as the output units. In addition, silicon area is conserved by incorporating an MOS device, in place of a diffused resistor, to strobe the bases of bipolar transistors.

The schematic diagram of Figure 22 shows the complete selected path of one of 1024 possible word lines through the decoder. In the quiescent state, the strobe is at -4.0 V and the potential at point A is at -20 V. Since transistor Q_1 of the following inverter, which uses an MOS load resistor to minimize space, is biased off, point B is at -4 V. Correspondingly, the potential at point C is at -15 V, transistor Q_2 is nonconducting, and point D is at -4 V. The MOS device Q_3 conducts, supplying base current to the output bipolar transistor Q_4. Since transistor Q_5 is biased off, no base current is supplied to Q_6 and the output potential is at -10 V, which is the quiescent input voltage for the BIMOS word-driver. When the strobe is activated to -20 V, the output is brought to approximately -5.5 V (as required to select the word driver). The capacitance of the output line discharges to -10 V, through transistor Q_4, when the strobe signal returns to -4 V. The total quiescent power dissipation for the 1024-output decoder is 1 to 1.2 W.

The circuit of Figure 22, which simulates the selected path of a word line, was breadboarded and tested using discrete nongold-doped bipolar transistors and semi-integrated MOS devices, i.e., p-channel transistors — four to a package. The output was loaded with nearly 1000 pF to simulate the capacitance of the 64 paralleled word-driver inputs which must be charged. The actual breadboard waveforms of the combined decoder-driver circuit appear in Figure 23. The decoding time is approximately 500 nsec. Even faster operation would result from the I-C version. In the full system, this delay coincides with the decay of the digit transient and thus does not add directly to read-write cycle time.

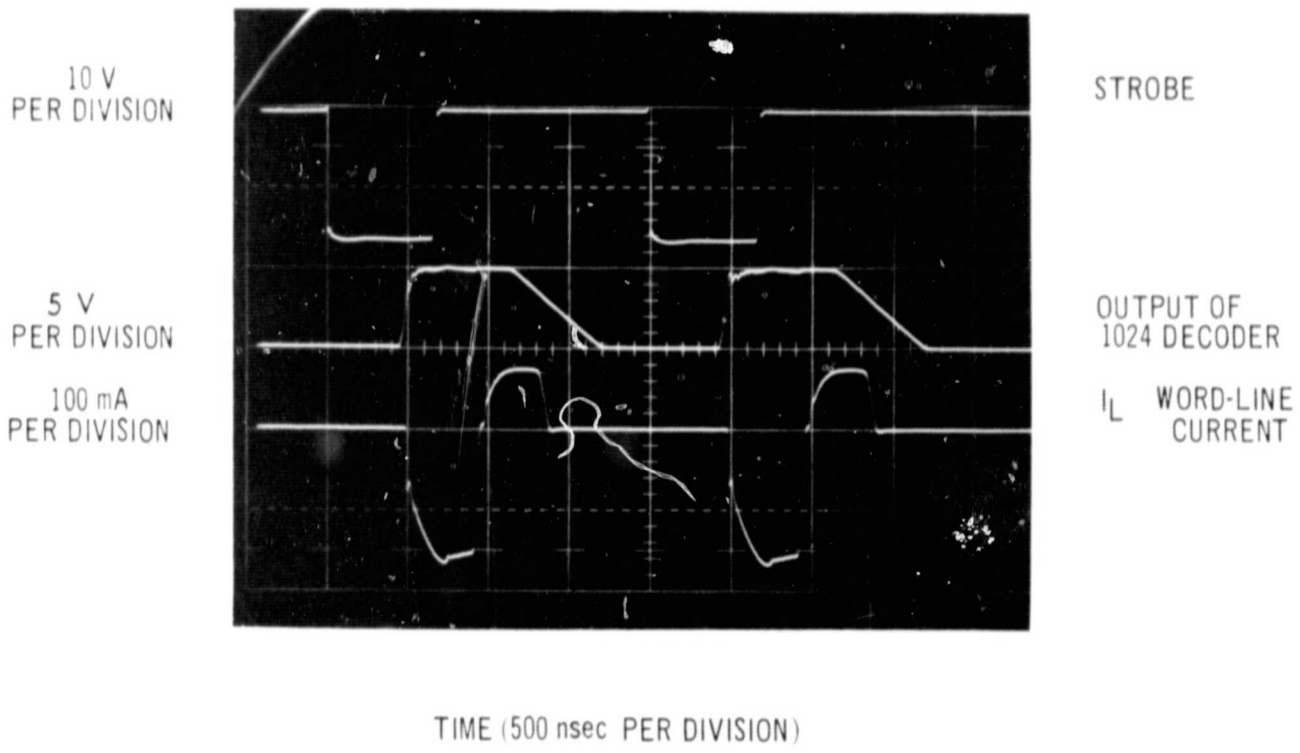


Figure 23. Breadboard waveforms of decoder-drive circuit.

V. SENSE-DIGIT REGENERATION LOOP

A. Introduction

A sense-digit regeneration loop was designed, and portions of the system were breadboarded and tested. The functions of the regeneration loop are to detect and write, or regenerate, information into each of the 200 bits of a selected word. Information is detected by an ac-coupled, differential-input, sense amplifier. During the write time, the digit driver feeds a current pulse to one of two digit lines, coinciding with the write pulse at one of the two crossovers of a memory bit. The digit driver consists of two identical current drivers under the control of the timing generator and a flip-flop in the memory data register.

Ideally in a system, there would be a single sense amplifier, digit driver, and flip-flop for each bit of the word line. This would require the digit driver to feed 65,536 bits; the line delay time would be excessive at that length, as described in Section II. A digit/sense segment of 4096 bits, or four of the 64 planes, is a reasonable compromise between circuit complexity and cycle time. A multiplex arrangement of n-p-n bipolar transistors is used to connect various lines to a single digit driver. In addition, MOS devices are incorporated to multiplex the low level signals into a single sense amplifier. To minimize digit line delay time, the multiplex transistors are connected to the midpoints of the digit lines. A block diagram of the sense-digit regeneration loop is shown in Figure 24. Since it is generally true that standby power in sense amplifier circuits is a major factor in magnetic memories, the regeneration system is designed to minimize power dissipation, within the constraints of the word length and memory cycle time.

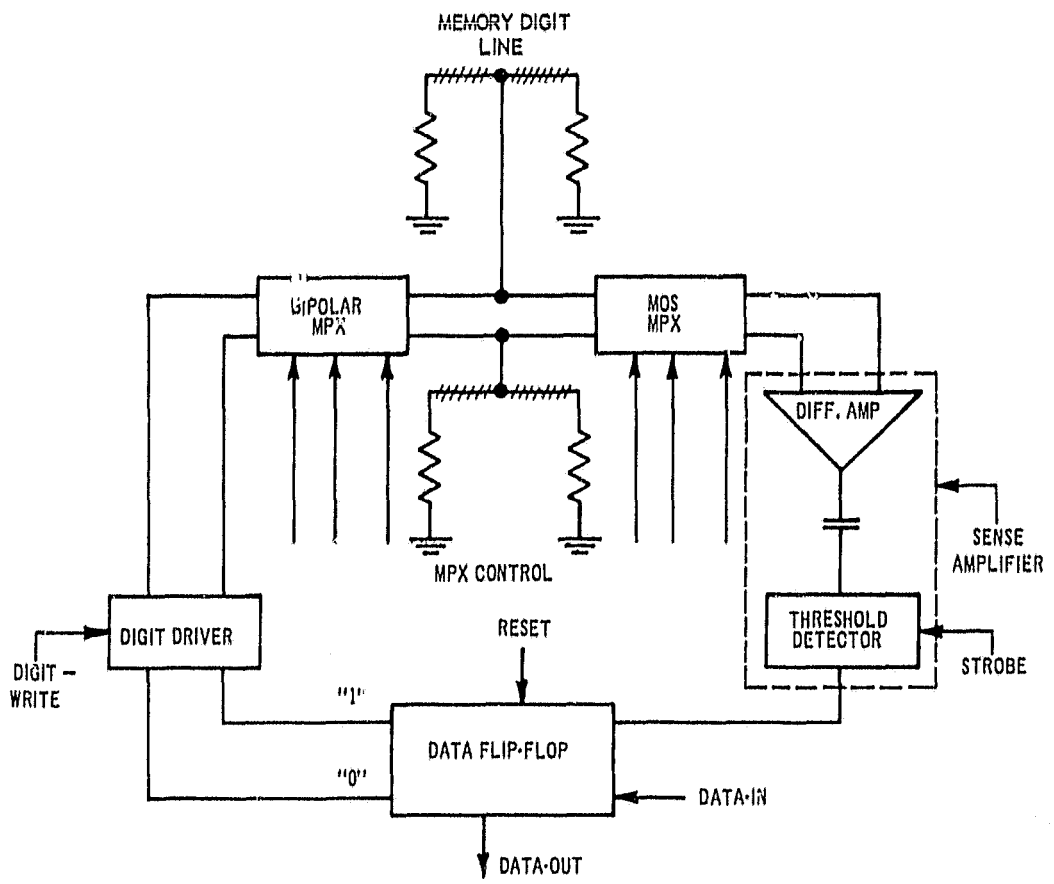


Figure 24. Block diagram of regeneration loop.

B. Description of Bipolar-MOS Multiplexer

The schematic of the bipolar-MOS multiplex arrangement for a memory module appears in Figure 25. The two crossovers of a bit are in corresponding positions in the upper and lower halves of the figure. Since each pair of devices drives

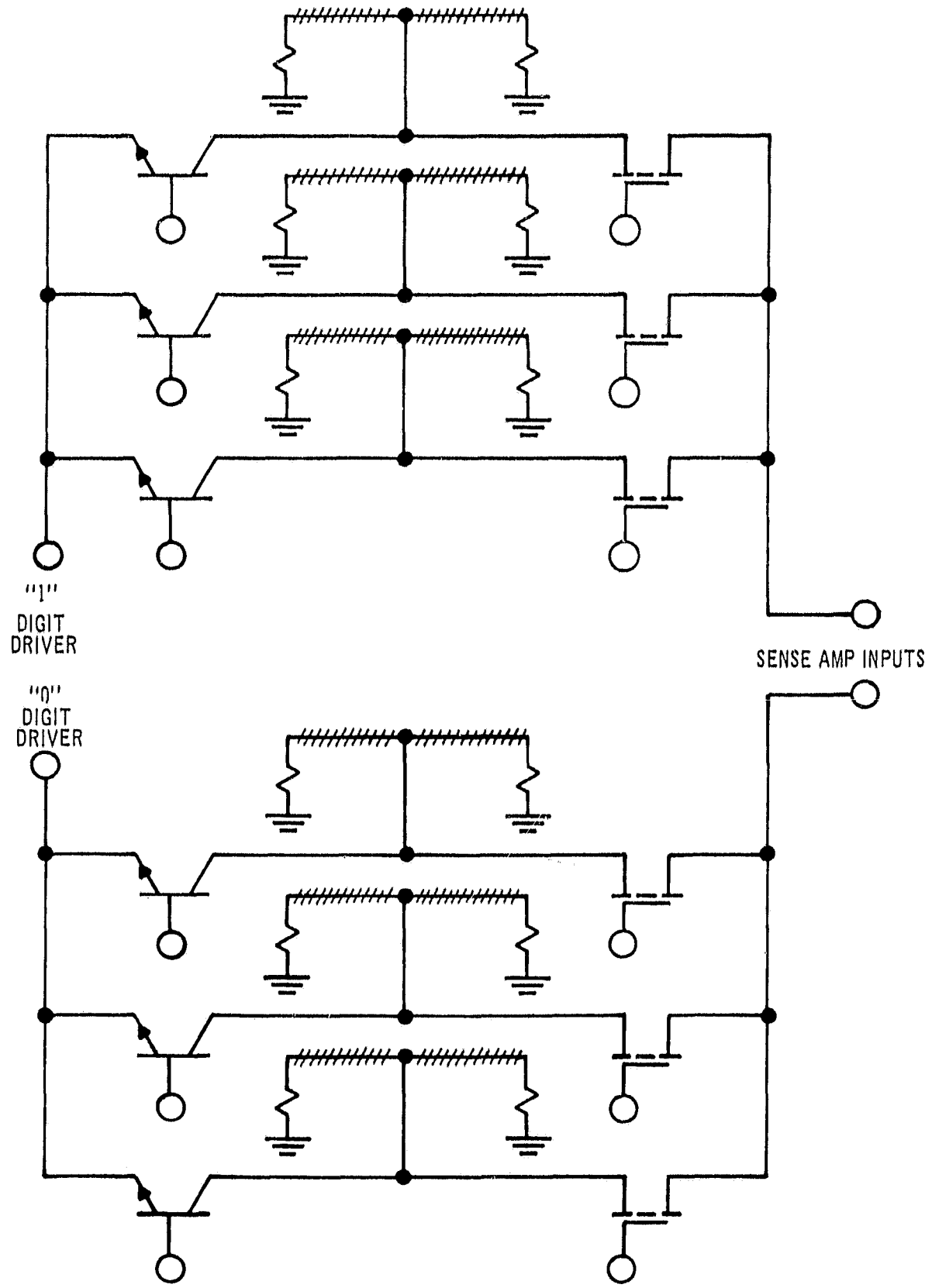


Figure 25. Schematic of bipolar-MOS multiplex circuit for 3 of the 16 segments per module (MOS substrates assumed grounded).

four planes, a total of 32 transistor pairs per sense-digit loop are needed. In other words, 32 n-p-n bipolar devices, and 32 p-channel enhancement MOS units are incorporated in the multiplex circuit for each of the 200 bits. The digit lines are tapped at the midpoints. The total digit current passed by the n-p-n transistor is approximately 40 mA, since each half of the digit line requires as much as 20 mA. The MOS devices are ideal for switching low-level signals into a sense amplifier because they exhibit a very low drain-to-source offset voltage at low current and do not require a transformer-coupled control drive (as bipolars do) because of their high input impedance. The bipolar-MOS multiplex circuit is designed to be fabricated on a common substrate (using the BIMOS process).

Circuit operation is as follows. In standby, all bipolar and MOS devices are biased in the nonconducting state; i.e., all emitter-base junctions are reverse-biased and the gate-to-source potential of all MOS transistors is zero. Prior to read, the two MOS devices associated with the appropriate segment of 4096 bits are selected by pulsing their gates negative. This connects the appropriate digit lines to the sense amplifier. After the information is sensed, the MOS transistor is disengaged from the digit line to reduce the effect of the digit voltage on the amplifier. Although the MOS unit is non-conducting, small voltage spikes are capacitively coupled to the sense input during the digit current rise and fall times.

The appropriate bipolar transistor base is pulsed positive to steer the digit current, and it remains conducting until the termination of the digit current. In Figure 26 the n-p-n multiplex transistors are shown as selected at the beginning of the memory cycle. This is convenient in simplifying timing, but system noise considerations may delay the n-p-n turn-on until after the read portion of the cycle.

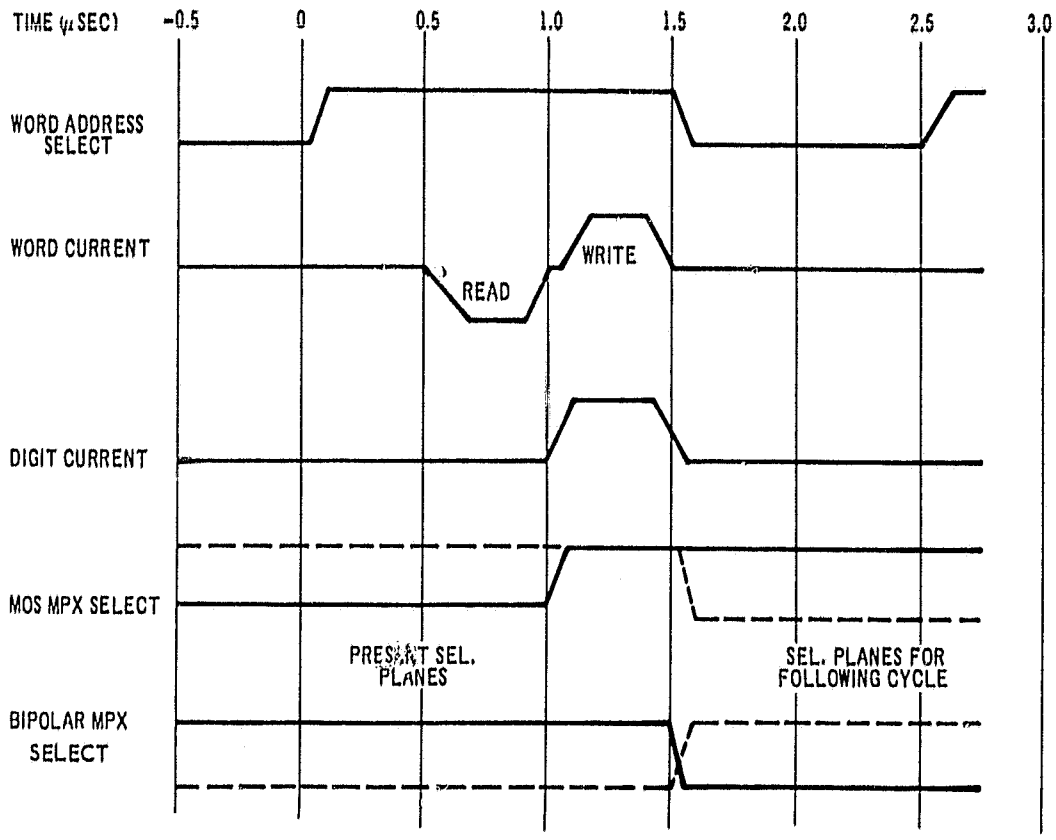


Figure 26. Timing diagram of 2.5-μsec system.

C. Design and Breadboard Results of Linear Portion of Sense Amplifier

The linear bipolar portion of the ac-coupled sense amplifier was designed, breadboarded, and tested. The amplifier should have a single-ended output to differential input gain of 500 to 600, enough to trigger a bipolar transistor in the threshold detector with a 1-mV sense signal. The amplifier bandwidth required, for the cycle times involved, is approximately 5 MHz. The sense amplifier is ac-coupled to the detector since it must detect signals in the 1-mV range. In an all ac-coupled differential sense amplifier, the sense signal must be larger than the inherent dc offset uncertainty. Since the principal offset is due to the V_{be} mismatch of the input transistors, typically 3 to 5 mV, only signals somewhat greater than 3 to 5 mV can be discriminated. An MOS linear amplifier was not used because an even larger offset voltage can result from the mismatch of device threshold voltages.

The circuit designed, shown in Figure 27, is a two-stage differential amplifier with emitter degeneration in each stage, buffering between stages, over-all common-mode feedback, and an emitter-follower output. The emitter degeneration provides gain stability with temperature variations. The emitter-follower buffering between stages makes the amplifier gain independent of device beta, by preventing the input impedance of the second stage from loading the first, in case of low transistor beta. The single-ended output to differential input gain is given by

$$A_V \approx \frac{R_L^2}{(R_E+r_{e_1})2(R_E+r_{e_2})} \approx \frac{(6250)^2}{(162.5)2(190)} \approx 630 \qquad (5)$$

where R_L is the collector load resistor, R_E the emitter degeneration resistor, and r_e is approximately equal to K_T/qI_e, for each stage. In addition, the buffering also increases the amplifier bandwidth Without the emitter-follower, the dominant circuit time constant would be the load resistance of the first stage times the input Miller effect capacitance of the second stage. Buffering reduces that resistance by the beta of the emitter-follower transistor. The common-mode feedback, obtained by biasing the first-stage current source from the second stage, also minimizes components and power dissipation. The emitter-follower output ensures that the input impedance of the threshold detector does not load the second stage, reducing its gain.

The circuit breadboard, incorporating RCA nongold-doped bipolar I-C transistors along with a pair of MOS multiplex devices at their inputs, exhibited a gain of 580 which compares favorably with the predicted value. The small-signal pulse performance of the amplifier is shown in the oscillogram of Figure 28. Quiescent power dissipation of approximately 35 mW was measured. The low-frequency common mode rejection ratio, defined as the ratio of differential gain to common mode gain, was found to be greater than 8000.

D. Design of Threshold Detector, Data Flip-Flop, and Digit Driver

A sense-amplifier threshold detector, data flip-flop, and digit driver were designed. The circuit, which uses n-p-n bipolar and p-channel MOS transistors, is shown in Figure 29. The detector has a strobed input allowing

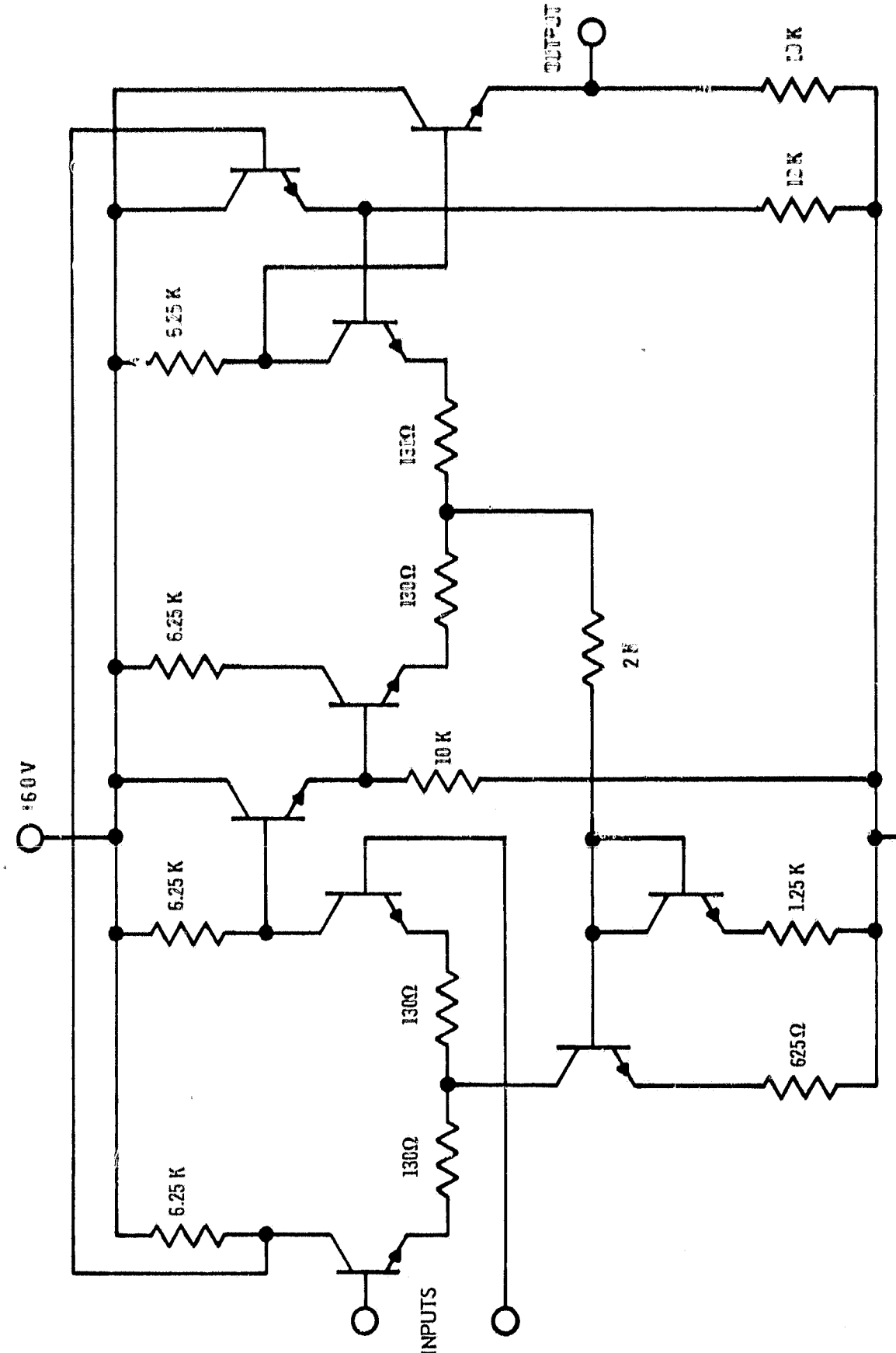
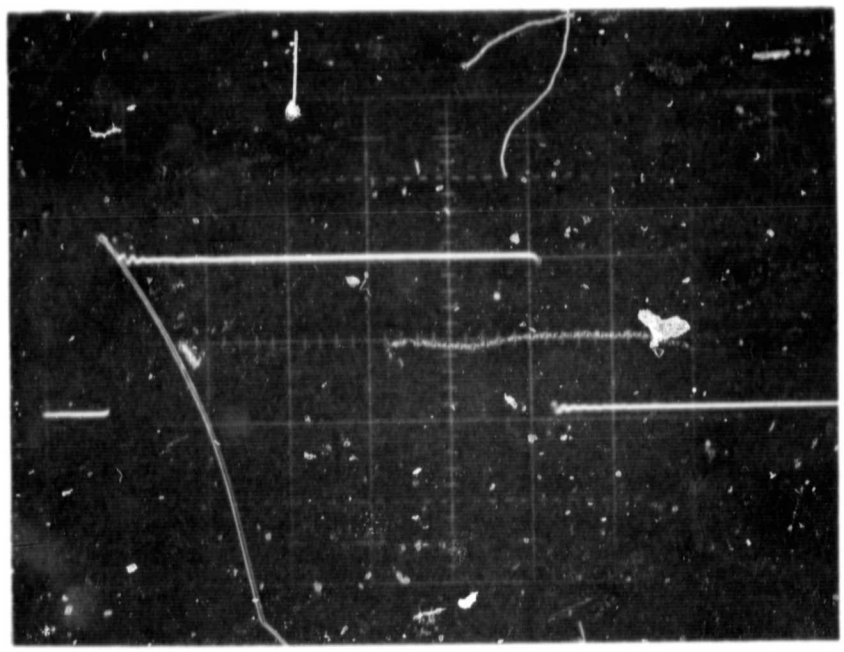


Figure 27. Schematic of two-stage differential amplifier.

0.5 mV
PER DIVISION

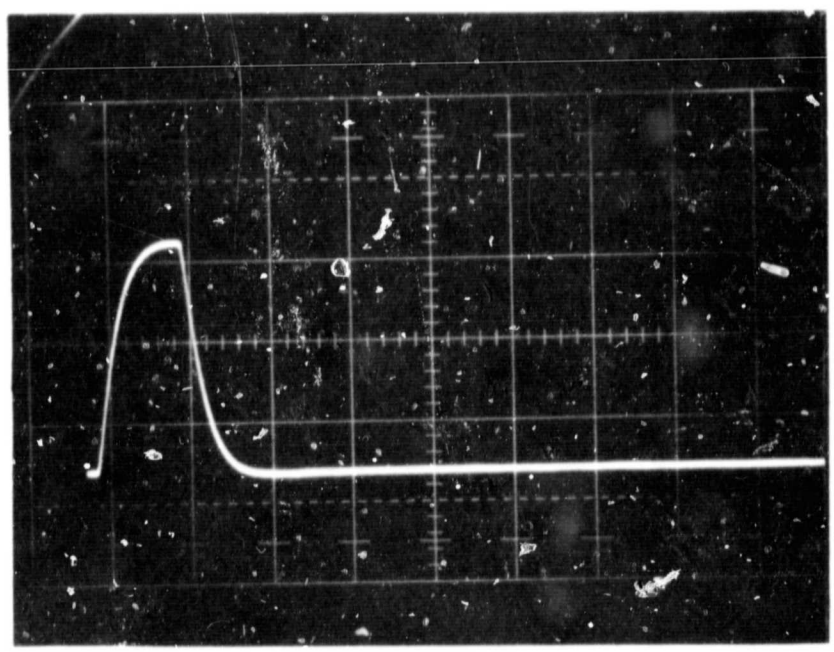


INPUT PULSE

TIME (100 nsec PER DIVISION)

(a) INPUT TO TWO-STAGE AMPLIFIER

200 mV
PER DIVISION



OUTPUT
VOLTAGE

TIME (500 nsec PER DIVISION)

(b) FOSITIVE OUTPUT OF TWO-STAGE AMPLIFIER

Figure 28. Oscillograms of pulse performance of two-stage amplifier.

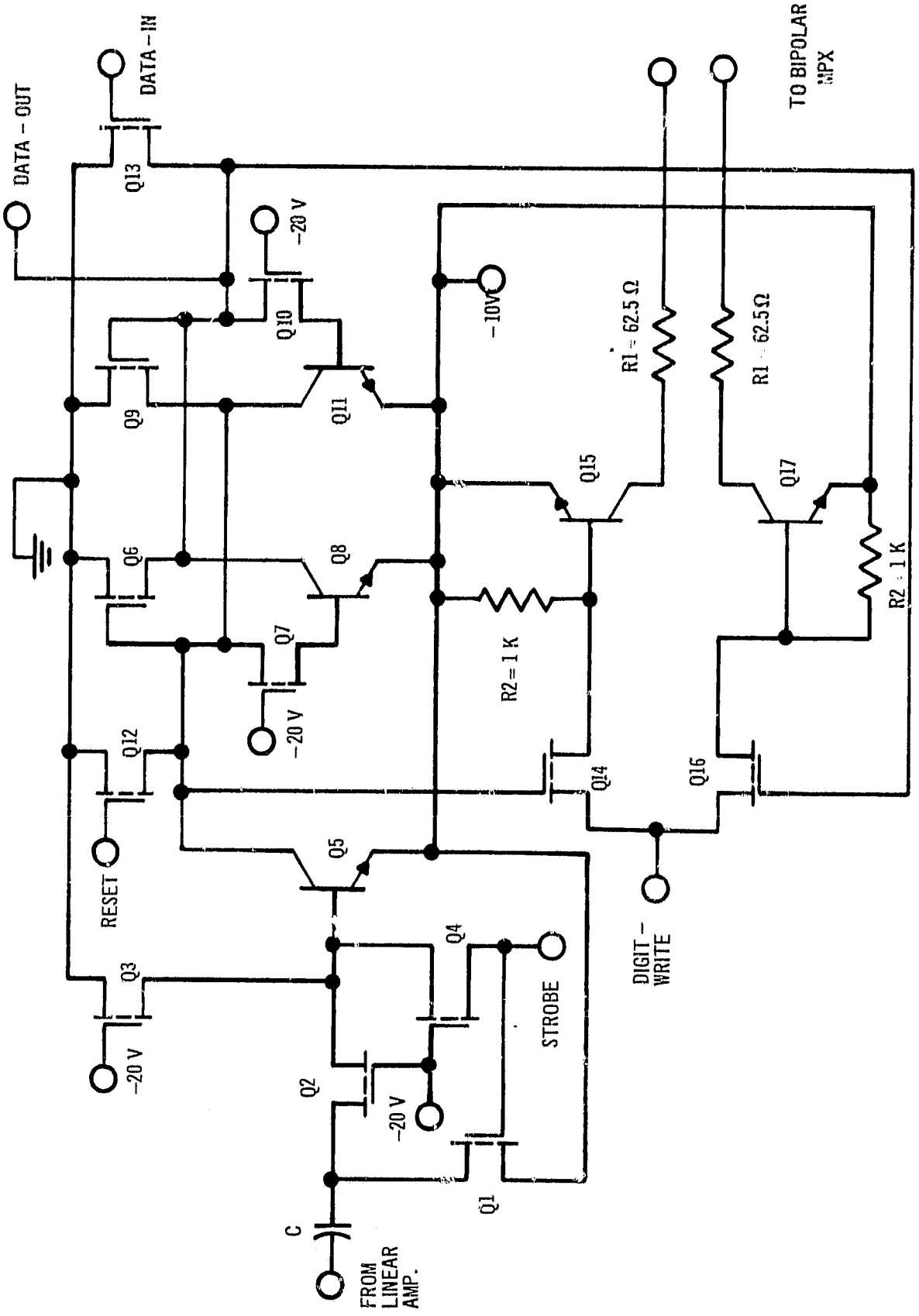


Figure 29. Schematic of BIMOS threshold detector, data flip-flop, and digit-drive circuit (MOS substrates assumed grounded).

the sense system to perform discrimination at read time only. The dc restoration is employed to eliminate variations in threshold with changes in duty cycle, i.e., information or address pattern.

Transistors Q_6, Q_7, Q_8, Q_9, Q_{10}, and Q_{11} (of Figure 29) compromise the complementary-symmetry BIMOS data flip-flop. MOS units Q_7 and Q_{10} function as base resistors for bipolars Q_8 and Q_{11}. This complementary-symmetry arrangement results in negligible power dissipation when storing information in either state. At the start of a read-write cycle, point '0' is at ground potential and point '1' is at -10 V. The RESET and DATA-IN lines are normally at ground potential. Transistors Q_1, Q_2, Q_3, Q_4, and Q_5 comprise the threshold-strobe portion of the circuit. The STROBE signal is set at -20 V, except during read, biasing transistor Q_1 in the on-condition. In addition, transistor Q_5 is reverse-biased by about 4 V, determined by the voltage division between MOS devices Q_3 and Q_4. The STROBE signal is pulsed to -10 V just prior to read, reducing the reverse-bias for transistor Q_5 to about 0.5 V. In this two-crossover-per-bit memory system, bi-directional signals, corresponding to a binary "1" or "0", appear at the input to the sense amplifier. The detector is set to trigger on a positive 0.5-V pulse, since device Q_5 would be forward-biased. A negative signal would keep transistor Q_5 in its nonconducting state. Upon triggering, the impedance of device Q_5 is low enough so that point "0" is "dragged" to the -10-V supply, as "1" changes to ground potential.

Besides extracting the stored information appearing on the DATA-OUT line, this information must also be regenerated, upon command. The DIGIT-WRITE signal, which was at -10 V in its quiescent state, is pulsed to ground during the write-in time. Depending on the state of the flip-flop, either device Q_{14} or Q_{16} will be conducting, saturating transistor Q_{15} or Q_{17}, respectively. Therefore, a current pulse is fed into either of two digit lines. Figure 30 shows the current path through the digit driver and the selected bipolar matrix switch, transistor Q_3, which is operated unsaturated so that the digit current is its emitter current. One of 15 unselected multiplex devices is represented by transistor Q_4, whose base is biased at -10 V. The magnitude of the current is given by

$$I \approx \frac{V_b - V_{be} - V_{ce} - V_S}{R_1} \approx \frac{-6.5 - 0.75 - 0.25 - (-10)}{62.5} \approx 40 \text{ mA} \qquad (6)$$

where V_b is the input base voltage and V_{be} is the base-to-emitter voltage of transistor Q_3, V_{ce} is the collector-to-emitter saturation voltage of transistor Q_2 (assumed to be 0.25 V), V_S is the -10-V supply, and R_1 is a precision current-setting resistor. As in the word driver, the current is insensitive to the betas of Q_2 and Q_3. Values of digit current other than 20 mA are achieved by changing the value of R_1. Resistors R_2 of Figures 29 and 30 allow either transistor Q_{15} or Q_{17} to discharge at the end of the write cycle, returning the digit-drive current to zero. After the completion of the cycle, the RESET line is pulsed to -10 V and point "0" reverts back to ground potential. Instead of regeneration, entry of new information may be desired. It is placed in the flip-flop by pulsing the DATA-IN line to the -10-V supply. A split read-write cycle is achieved by injecting a RESET and pulsing DATA-IN after the read portion of the cycle.

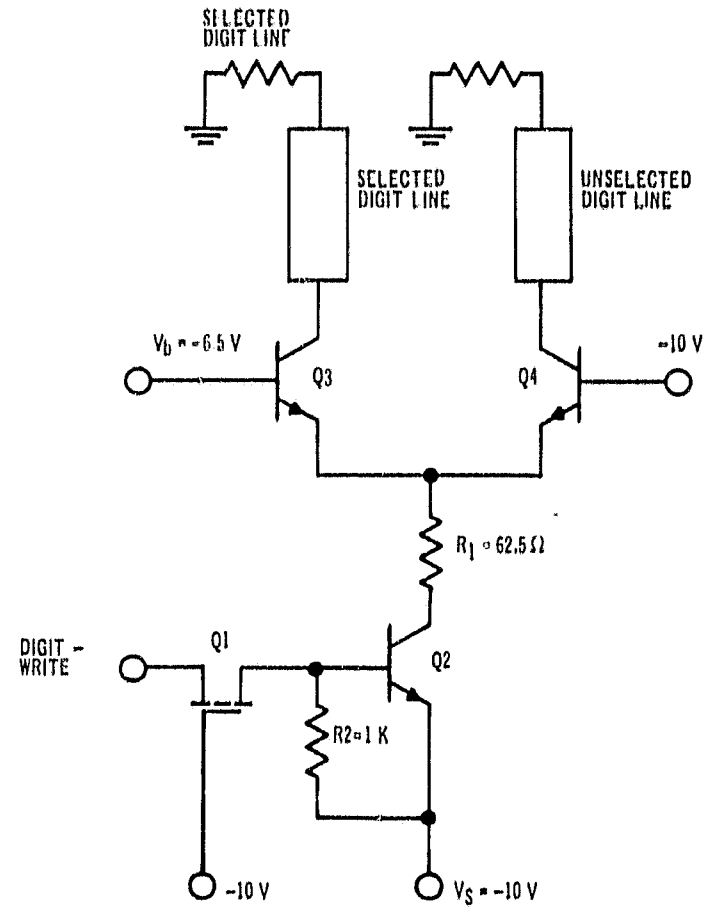
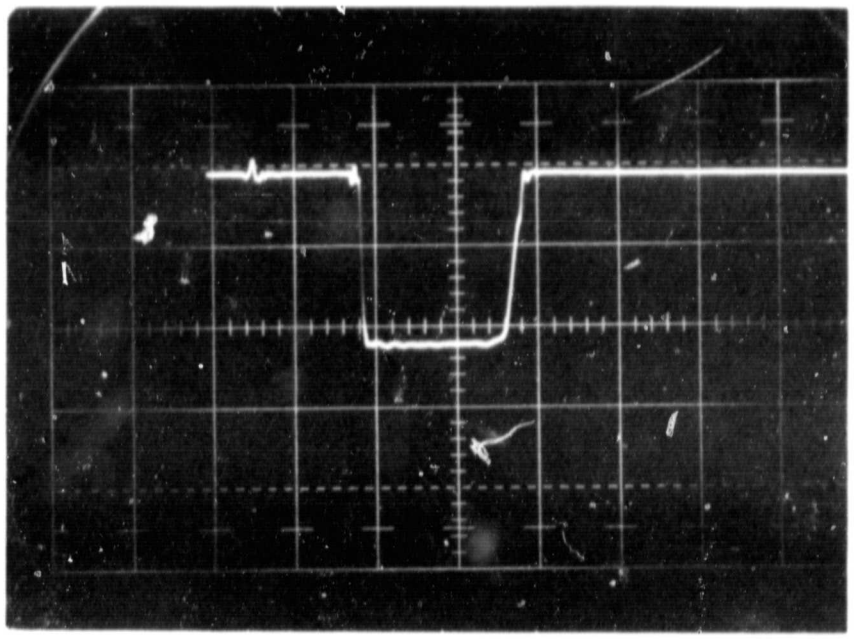


Figure 30. Schematic of digit-drive system (MOS substrates assumed grounded).

The digit drive system of Figure 30 was breadboarded and tested with non-gold-doped n-p-n bipolar and the semi-integrated p-channel MOS transistors. For test purposes each half of the digit line was approximated by a 200-Ω equivalent resistance (a single 100-Ω resistor). The voltages at the collectors of transistors Q_3 and Q_4 (of Figure 30) are shown, for a pulsing DIGIT-WRITE signal, in the oscillogram of Figure 31. A 4-V pulse, corresponding to 40 mA through a 100-Ω resistor, appears at the collector of device Q_3. As expected, there is zero current flowing through the unselected Q_4 device.

Except for the coupling capacitor, C, and the two precision current-setting resistors, R_1, the entire circuit can be fabricated in monolithic form (using the BIMOS process). It is estimated that the total power consumption in standby, for the circuit of Figure 29 will be 20 to 30 mW. A complementary-symmetry data flip-flop could be used to lower the quiescent power dissipation still further and reduce the pellet size. However, the standby power consumed by the flip-flop and digit driver is already relatively low compared with that of the detector.

One approach to integrating the sense-digit regeneration loop would be to fabricate a circuit containing the sense amplifier, digit driver, and data register for a single bit or multiple bits, e.g., four or eight bits. However, the work performed in this program indicates that there is a more efficient way to partition the regeneration loops, namely by circuit function. The approach would be to integrate arrays of bipolar linear amplifiers on one common substrate,



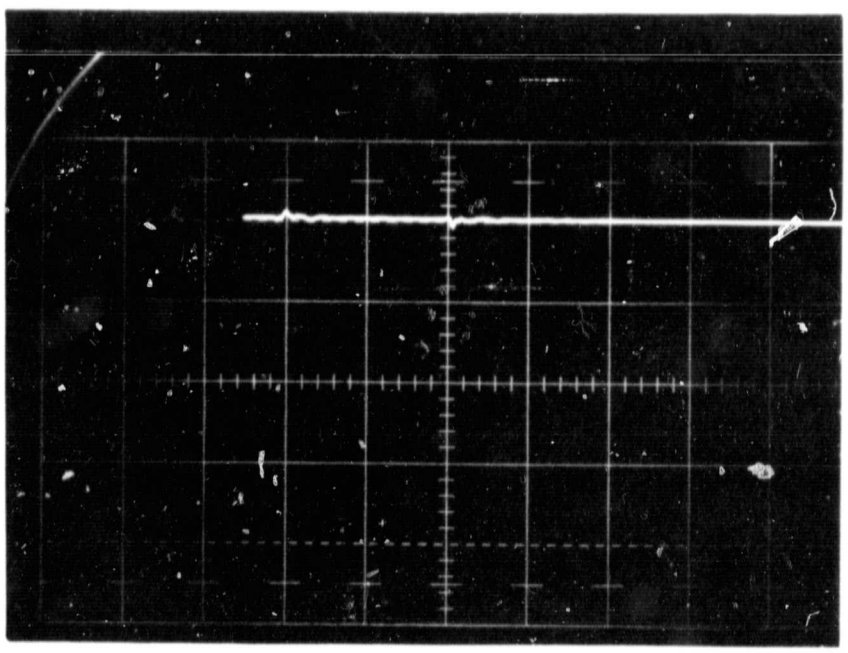


Figure 31. Oscillograms of collector voltages as a function of DIGIT-WRITE signal. (a) Selected transistor (Q_3 of Figure 30). (b) Unselected transistor (Q_4 of Figure 30).

and BIMOS arrays of detectors, flip-flops, and digit drivers on another substrate. The BIMOS multiplex devices would also be integrated in strips on a common substrate so that they can become part of every fourth stack plane, as described in Section II.

VI. CONCLUSIONS AND RECOMMENDATIONS

The feasibility of producing a usable ferrite laminate with reproducible mechanical dimensions has been demonstrated. The overall shrinkage, from completely green through anneal, of all samples that could be measured varied between 0.1% and 4%; most of this variation occurred in binder burnout. The ability to use solid conductors attached to a frame so as to maintain fixed spacing compensates for small variations in sample dimensions. This can be accomplished by pressure-sintering.

For both compositions 3515 and 47, pressure-sintering temperatures and/or annealing temperatures required to produce acceptable magnetic characteristics are in excess of the melting point of gold. This precludes the possibility of using solid gold conductors for the laminate at the present stage.

The packaging and interconnection techniques described in the report are promising but need to be further developed to permit their successful use in the construction of a reliable memory system with the capability of being repairable. This is true for both the magnetic stack and associated integrated electronics.

Breadboard tests of critical circuit functions indicate that the circuits synthesized are capable of interfacing with a laminated ferrite stack. Power dissipation is reasonably low: less than 25 W for a 1.3×10^7 bit module at 2.5-μsec read-regenerate cycle time.

The operating word selection drive system that was designed looks very attractive. The driver and decoder circuits incorporate both n-p-n bipolar and p-channel enhancement MOS devices; the combination is compatible with present I-C technology. The breadboarded word driver that simulates the integrated version delivers a read pulse as high as 150 to 200 mA, followed by a write pulse as high as 75 to 100 mA. The pulse rise-times and widths can be as low as 200 nsec. The 1024-output decoder, consisting of 33 binary decision trees, exhibits a 500-nsec decoding time. The breadboard employed integrated arrays of n-p-n transistors that were junction-isolated demonstrating the capability of the n-p-n I-C process.

The level of BIMOS word-driver integration comprises strips of eight individual word-drive circuits on a 160-mil by 70-mil silicon pellet. Several groups of wafers have been processed with partial success. The problems which occurred do not appear serious.

The sense-digit regeneration loop was designed with emphasis on reducing power dissipation. In addition to sense amplifiers, digit drivers, and data registers, the system uses a BIMOS multiplex arrangement to limit the length of digit lines without requiring additional sense amplifiers or digit drivers. The ac-coupled sense amplifier consists of a two-stage bipolar differential amplifier with a gain of nearly 600 at a standby power drain of 35 mW, feeding a BIMOS strobed detector which would consume 20 to 30 mW. For a 2.5-μsec cycle time the assumed 20-mA digit current generates 31 mW of average power in the terminating resistors. Thus, an energized digit-sense system dissipates on the order of

100 mW per bit depth or 20 watts for the 13-million bit module. This type of integrated sense-digit electronics appears promising for a variety of applications.

Considerable testing of laminated ferrite memory cross sections has been undertaken to determine system performance. The test data, part of which appears in the literature (Refs. 3, 5), supports the memory characteristics outlined in Section II.

To give a 10^8-bit, medium-speed, low-power, laminated ferrite/BIMOS electronics memory a firmer technical foundation will require effort as follows:

(1) Reduction of pressure-sintering to a practical, low-cost process for magnetic memory fabrication.

(2) Investigation of other ferrite compositions which sinter at lower temperatures, having the desired magnetic properties, to permit the use of solid gold conductors.

(3) Development of beam lead-solder reflow, mass interconnection techniques.

(4) Achievement of BIMOS word-driver processing at economic yields.

(5) Integration of BIMOS word-decoder trees.

(6) Integration of BIMOS sense-digit regeneration loop.

(7) Systems testing, incorporating integrated-circuit cross sections with magnetic stack cross sections.

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