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SYSTEM DEVELOPMENT
COMMUNICATIONS
DATA LINK
DATA PROCESSING
ANTENNAS
MULTIPLEXERS

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NASA MICROMIN COMPUTER

CONTRACT NO. NAS8-20643

MONTHLY PROGRESS LETTER NO. 8 - JANUARY 1967

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OBJECTIVE:

The objectives of this contract are: (1) the fabrication and evaluation of two sets of ten discrete vector breadboard circuits of the micromin design for the flight control computer; (2) the fabrication and evaluation of a discrete system breadboard (epoxy p. c. modules) using the micromin circuit designs; and (3) preparation of circuit schematics, system block diagram, and system reliability estimate.

SUMMARY:

Approximately half of the p. c. assemblies for the system breadboard have been completed. A phasing problem has been discovered with the Scott magnetic amplifiers and is being followed up by Scott. The system breadboard chassis assembly has been initiated and wiring interconnections will begin with the completion of the run wire list. Documentation is proceeding on the individual circuit schematics and the system block diagram. The reliability estimate will be completed when the circuit failure mode analysis is available. The report contains detailed descriptions of all micromin circuit designs.

PROGRESS:

Assembly of approximately 50% of the seventy-eight p. c. modules (with the exception of magnetics) has been completed for the system breadboard. The only p. c. boards not available at this time are the switching logic cards and the solid state C. A. T. cards. Switching logic boards will be available by mid-February and the solid state C. A. T. layout will be completed when final evaluation of the vector breadboard circuits

has been finished. Inverter transformers have been received from Raytheon and are being installed in the p.c. assemblies.

A problem has occurred with Scott magnetic amplifiers. Units which have been received and tested were determined to be phased improperly indicating that during fabrication the top core was not flipped prior to applying the signal windings. Scott has been notified and the remaining units in fabrication are being checked to determine the extent of the problem.

The system breadboard external connectors have been wired and the run wire list is being completed for interconnection designations. The entire chassis has been laid out and is available for wiring as soon as the run wire list is completed. Minor differences in the wiring between the system breadboard and the AS 205 configuration will be the deletion of redundant interconnections and the "simulate" inputs.

The finalized circuit schematics (with the exception of the solid state C. A. T. and switching logic) on MSFC format have been completed in preliminary form and are being checked by Engineering. The system block diagram is being evolved as the run wire list is being generated. The failure mode analysis on all circuits is nearing completion and will enable Reliability to complete the system reliability estimate.

The remaining portion of this report contains detailed circuit descriptions of all circuits including separate descriptions of the power supplies and the magnetic amplifier.

Inverter Circuits

Those inverter circuits which provide magnetic amplifier excitation operate at 25 kHz. All others operate at 75 kHz and are relatively conventional in design except for the feedback circuit for the transistor switches.

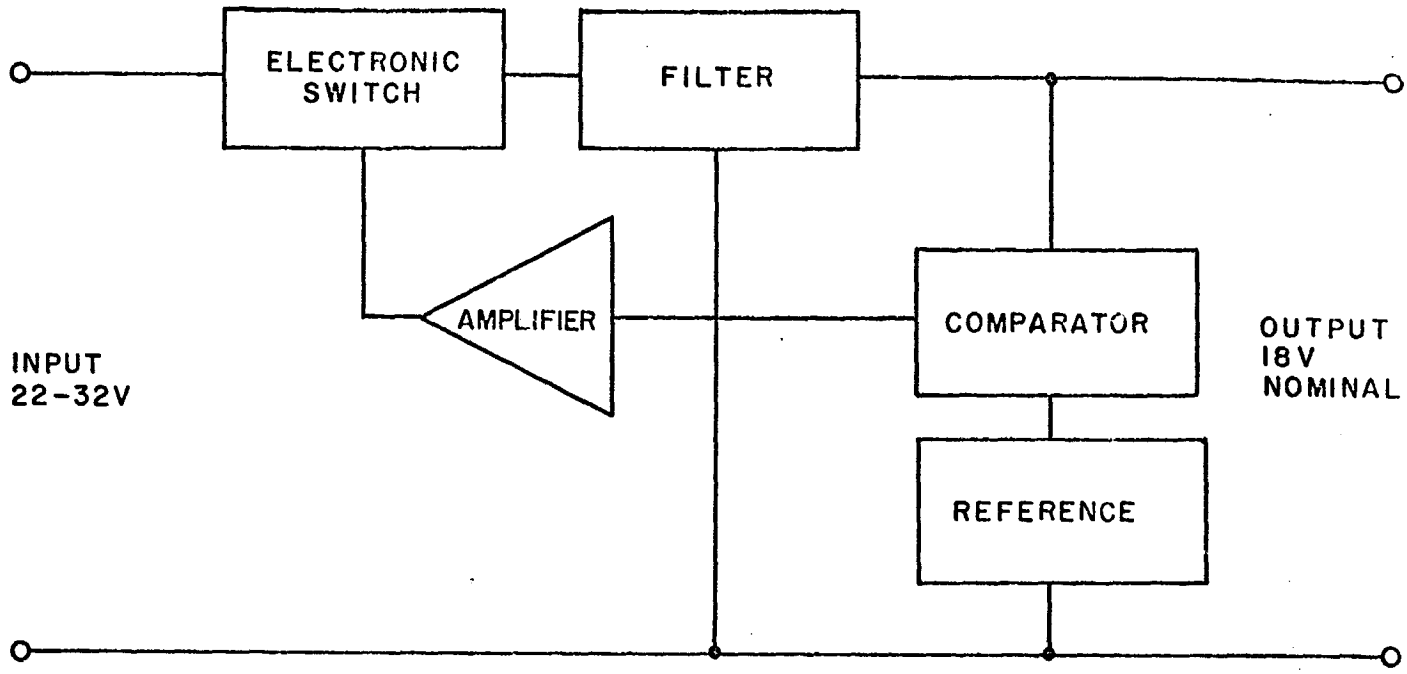
Constant current diodes are used to establish the desired level of base drive and offer two distinct advantages. The feedback current becomes relatively independent of voltage levels and the constant current diodes have a temperature coefficient which is used to offset the beta and base-to-emitter voltage change of the transistor switches with temperature.

In the region of core saturation, the current drawn by the inverter tends to rise abruptly. The regulators, which power the inverters, have been designed to have relatively high output impedances to these high frequency currents. Therefore, the supply voltage to the inverter drops abruptly at the time of core saturation. This voltage change is coupled via a capacitor to the inverter base drive circuit. The effect is to allow the inverter to commutate more easily due to a reduction in available inverter base drive at the time of core saturation.

Switching Regulator

Switching regulators are used in applications where the output current will exceed approximately 25 ma. The regulator input voltage is 22 to 32 volts and in most applications delivers a nominal 18 volts with a small negative temperature coefficient. The switching regulator, with minor differences to meet special requirements, is used in the 12 and 50 ma servo amplifiers, digital spatial amplifier, control attenuator timer, and signal switching circuit.

By designing the switching circuit to operate at comparatively high frequencies, the size of the inductor and capacitor used in the filter can be made relatively small, thus achieving a savings in size and weight. The use of relatively small filter capacitors permits the output voltage to significantly drop when the core of the inverter circuit saturates, which allows the inverter to commutate at much lower levels of peak current.



The electronic switch consists of either a single bipolar transistor, or two transistors in a modified Darlington circuit operating in a common emitter configuration. When the comparator determines that the output is low, the electronic switch closes. The current then rises in a linear manner at a rate determined by the inductance of the inductor in the filter and the differential voltage between the input and output of the regulator. When the current has increased to a value equal to the load current, the output voltage will stop decreasing. As the current continues to increase, the output voltage will rise to a point where the comparator turns the electronic switch off. The current supplied by the inductor will then begin to decline. However, only when the inductor current has decreased to a value equal to the load current will the output voltage begin to decrease. It should be noted that no other feedback is required other than that obtained from the comparator.

The combined temperature coefficient of the reference and comparator is intentionally made negative. The negative coefficient offsets the positive temperature coefficient of the inverter and rectifier circuits.

The reference voltage is established by a 6.2 volt zener diode located in the emitter of the high gain PNP stage used as the comparator. The current through the reference diode and the comparator is approximately 5×10^{-4} amperes and is established by a constant current diode.

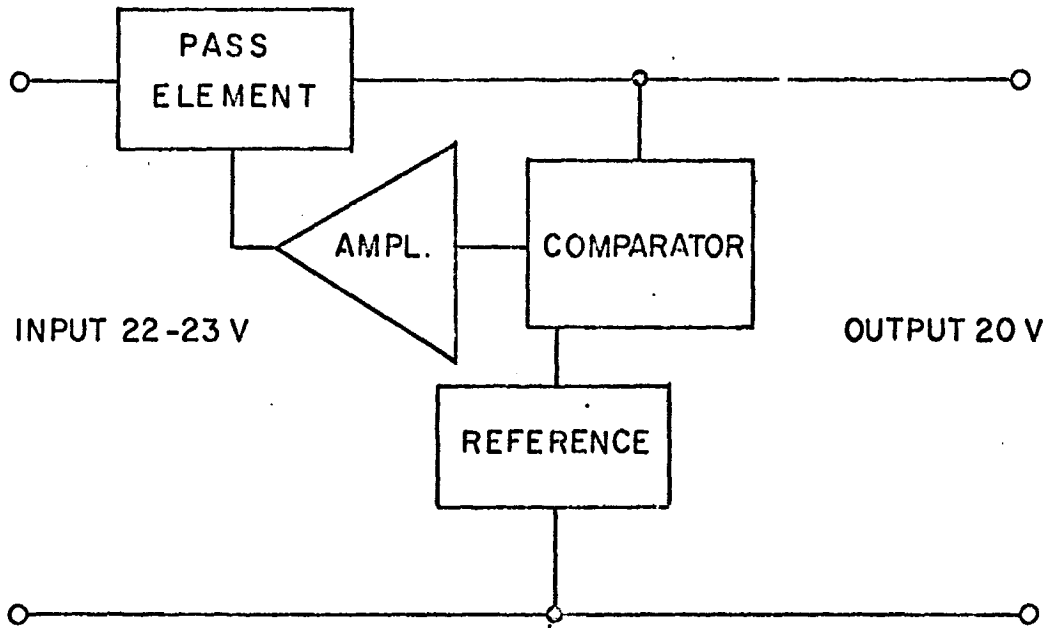
Circuit Specifications

Input Voltage Range	22 to 32 volts
Temperature Range	-55 to +125°C
Output Impedance (low freq.)	One ohm nominal
Maximum average output current	
Servo amplifier regulator	60 ma
CAT & Switching circuits regulator	150 ma
Output Voltage	18 volts nominal
Temperature Coefficient	-2 mv/°C nominal

Series Regulator

The 20 volt series regulator is intended for applications when a nominal 20 volts is required at currents approximately in the range of 10 to 25 milliamperes and is designed to function from an input voltage of 22 to 32 volts. It is used with minor modifications in the beta command, active filter, spatial telemetry, servo comparator, and spatial comparator circuits.

The pass element consists of an N-channel FET transistor with a minimum saturated current rating of 50 ma. The fact that this device is inherently "on" eliminates the possibility of starting problems in the regulator section. The pass element is shunted by a resistor to reduce its thermal stress level.



The reference consists of a zener diode operating essentially at a constant current of approximately 5×10^{-4} amperes established by a constant current diode. Most applications require that the output voltage of the regulator have a small negative temperature coefficient. This T. C. requirement is achieved by offsetting the negative characteristic of the comparator with the smaller positive T. C. of the reference diode.

The excellent performance achieved from this relatively simple circuit results from the large voltage gain obtained from the NPN transistor which functions as comparator and amplifier. The collector load for this stage is a constant current diode which represents a very high impedance. Therefore, a relatively large voltage change is obtained for small changes in collector current. The high gain (about 4, 000) obtained from this stage results in a circuit output impedance of less than one ohm at low frequencies. The gain at high frequencies has been rolled off to ensure stability and to increase the output impedance thus allowing the inverter to commutate easily.

CIRCUIT SPECIFICATIONS

Input Voltage Range	22 to 32 volts
Output Impedance (low frequency)	Less than one ohm
Temperature Range	-55 to +125°C
Maximum Average Output Current	30 ma
Output Voltage	20 volts nominal
Temperature Coefficient	-3 mv/°C nominal

ELECTRICAL DESIGN OF SPECIAL MICROMIN CIRCUITS

12 MA Servo Amplifier

The purpose of this circuit is to furnish a differential output current in proportion to the weighted sum of several isolated input signals. The amplifier drives a servo actuator solenoid which has 1000 ohm differentially wound coils and requires a full scale current of ±12 ma. The amplifier output impedance should be high compared to 1000 ohms because the solenoid is current-actuated. Gain stability and linearity should be better than one percent. The required gain is dictated by other loop parameters and is typically 24 amp/amp.

A block diagram of the 12 ma servo amplifier circuit developed for the micromin flight control computer is shown in Figure 1. This is identical to the 50 ma servo amplifier block diagram and much of the circuitry used is the same. Voltage regulation and isolation from the system 28 volt supply is provided by the circuit power supply which is described previously.

A two-core magnetic amplifier which is described previously is used to sum and amplify the several input signals. A high degree of isolation between inputs is maintained since a separate signal winding is provided for each input signal. The gain of the magnetic amplifier is nominally 15 volts/ampere-turn.

Further amplification occurs in the transistor preamplifier which is an emitter-coupled differential stage having a voltage gain of approximately 35 db. This stage uses a matched pair of high gain transistors for low null drift.

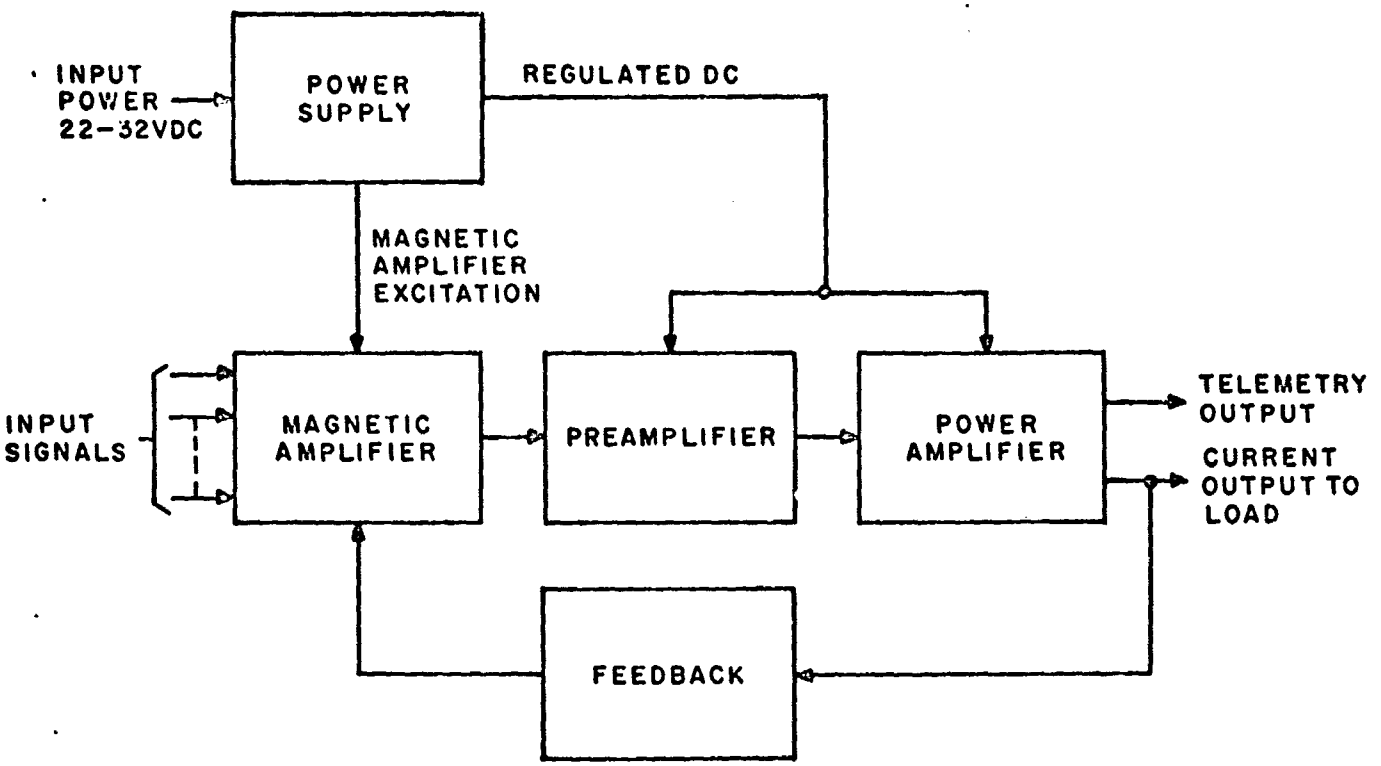


FIGURE 1. SERVO AMPLIFIER BLOCK DIAGRAM

The power amplifier consists of an emitter-follower buffer stage and a high-level emitter-coupled differential stage which directly drives the solenoid load. Biasing of the output stage is simplified by the use of complementary transistors which also provide temperature compensation and a stable quiescent current level which is necessary for maximum output current swing.

The circuit will tolerate an open-circuit load with no damage and will operate normally with a short-circuit load.

Precision current sampling resistors are connected in series with each side of the load to provide a telemetry voltage proportional to the differential load current. A telemetry voltage of 1.2 volts corresponds to a load current of 12 ma. The roll-off in frequency response of the entire amplifier is accomplished by capacitive feedback from the telemetry output to the transistor preamplifier. This method allows the use of small capacitors and also makes the amplifier bandwidth insensitive to changes in the transistor amplifier gain. Approximately 50 db of negative feedback is used to stabilize the over-all gain of the amplifier, improve linearity, and increase the output impedance.

A summary of the pertinent characteristics of the circuit which have been experimentally confirmed is given below:

TABLE 3-1

SUMMARY OF 12 MA SERVO AMPLIFIER SPECIFICATIONS

Operating Temperature Range	$-55^{\circ}C$ to $+125^{\circ}C$
Input Power	22-32 VDC
Gain (100 turn signal winding)	24 amp/amp nominal
Gain stability	±1%
Null drift	±0.2 ma
Bandwidth (-3 db)	70 Hz, min. 130 Hz, max.
Maximum output (1000 ohm load)	±16 ma min.

50 MA Servo Amplifier

The 50 ma servo amplifier is required to amplify several isolated input signals and provide an output current in proportion to the weighted sum of the inputs. The servo amp drives a servo actuator which has an input impedance having a resistive component of nominally 100 ohms. Since the servo actuator is a current-operated device, the output impedance of the amplifier should be very high in comparison to the load impedance. A full scale output current of 50 ma is required. The amplifier gain stability and linearity should be better than one percent. The gain required is typically 100 amp/amp; however, the exact value is determined by other loop parameters.

A block diagram of the 50 ma servo amp circuit developed for the micromin flight control computer is shown in Figure 1. The power supply block consists of a switching regulator and inverter which provides the required bias voltages for the transistor amplifier and the gating voltage for the magnetic amplifier, all of which are isolated from the system 28 volt supply. A description of the operation of the power supply is given previously.

A two-core magnetic amplifier is used as the input stage of the servo amplifier because it provides a high degree of isolation between the multiple input signals and is also an excellent summing device. The gain of the magnetic amplifier used in this design is the same as that of the 12 ma servo amplifier.

The magnetic amplifier is followed by a transistor preamplifier and power amplifier to provide additional gain and the necessary impedance level. The preamplifier consists of two differential stages using complementary transistors to simplify the biasing. Differential amplifier stages are used to minimize null drift and provide high gain. The over-all gain of the two preamplifier stages is approximately 80 db. The frequency response of the amplifier is determined by a feedback capacitor across the two preamplifer stages which results in a capacitance multiplication effect in proportion to the voltage gain of the preamplifier and thereby allows the use of a smaller capacitor.

The power amplifier stage can be classified as a transconductance amplifier in that it produces an output current in proportion to an input voltage. Because of the moderate power level involved, the output stage should have a high efficiency to minimize heat dissipation problems in the micromin circuit. For this reason, a Class B output stage is used. Crossover distortion inherent in the Class B connection is reduced to a negligible level by the application of approximately 40 db of degenerative current feedback around the entire power amplifier stage. In addition, the local negative feedback stabilizes the gain and increases the output impedance of the circuit. The emitter follower output transistors are driven from a high impedance as provided by the collector impedance of the driver transistor and a field-effect constant current diode. This has the advantage of increasing the output impedance and minimizing crossover distortion. The use of a constant current diode also permits a large dynamic swing without requiring excessive biasing power.

A portion of the output load current is returned to the magnetic amplifier in a degenerative fashion which further increases the output impedance and stabilizes the over-all gain of the complete amplifier. A telemetry output voltage is also provided which is related to the load current by the factor of 20 volts/amp.

Since this circuit is essentially a current amplifier, it is inherently short-circuit proof. An open circuit load will not damage the amplifier; however, the load voltage must be limited to approximately ±11 volts for linear operation.

SUMMARY OF 50 MA SERVO AMPLIFIER SPECIFICATIONS

Operating Temperature Range	$-55^{\circ}C$ to $+125^{\circ}C$
Input Power	22-32 VDC
Gain (100 turn signal winding)	100 amp/amp nominal
Gain stability	±1%
Null drift	± 1 ma
Bandwidth (-3 db)	70 Hz min. 130 Hz max.
Maximum output (100 ohm load)	±70 ma min.
Output impedance (-f ≤1 kHz)	50 K ohms min.

BETA Command Power Supply

The beta command power supply is designed to provide a stable supply voltage to power a hydraulic actuator potentiometer of approximately 5,000 ohms. Since the potentiometer is located at a considerable distance from the computer, thus increasing the possibility of accidental shorts, overload protection is provided. The 30 volt output of the regulator is isolated from the 28 volt power system. A block diagram of the power supply is shown in Figure 2.

The series regulator consists of a PNP transistor as the pass element which is driven by one side of an NPN differential amplifier and an N channel field effect transistor. The field effect transistor is used to establish the required operating current level for the differential amplifier and also provides a nominal gain of four. For load currents in the range of 4 to 8 ma, the regulator will function as a constant voltage source. If the load current increases beyond approximately 8 ma, the regulator will function as a constant current source. If the overload is removed, the circuit will return to normal constant voltage operation. A 5,000 ohm potentiometer is the normal load for this circuit. A resistive voltage divider is provided to develop a one volt telemetry signal for 30 volts out of the regulator.

The overload protection circuit monitors the voltage drop across a 100 ohm resistor placed in series with the regulator circuit. The collector current of the monitoring transistor will be approximately one ma per ten ma of regulator current. This collector current flows through a 10,000 ohm resistor which produces a voltage drop which is compared against the voltage of the regulator reference diode. If the voltage is greater than that of the reference diode, the current through the comparator transistor will be reduced which reduces the output of the regulator and prevents damage due to an accidental overload.

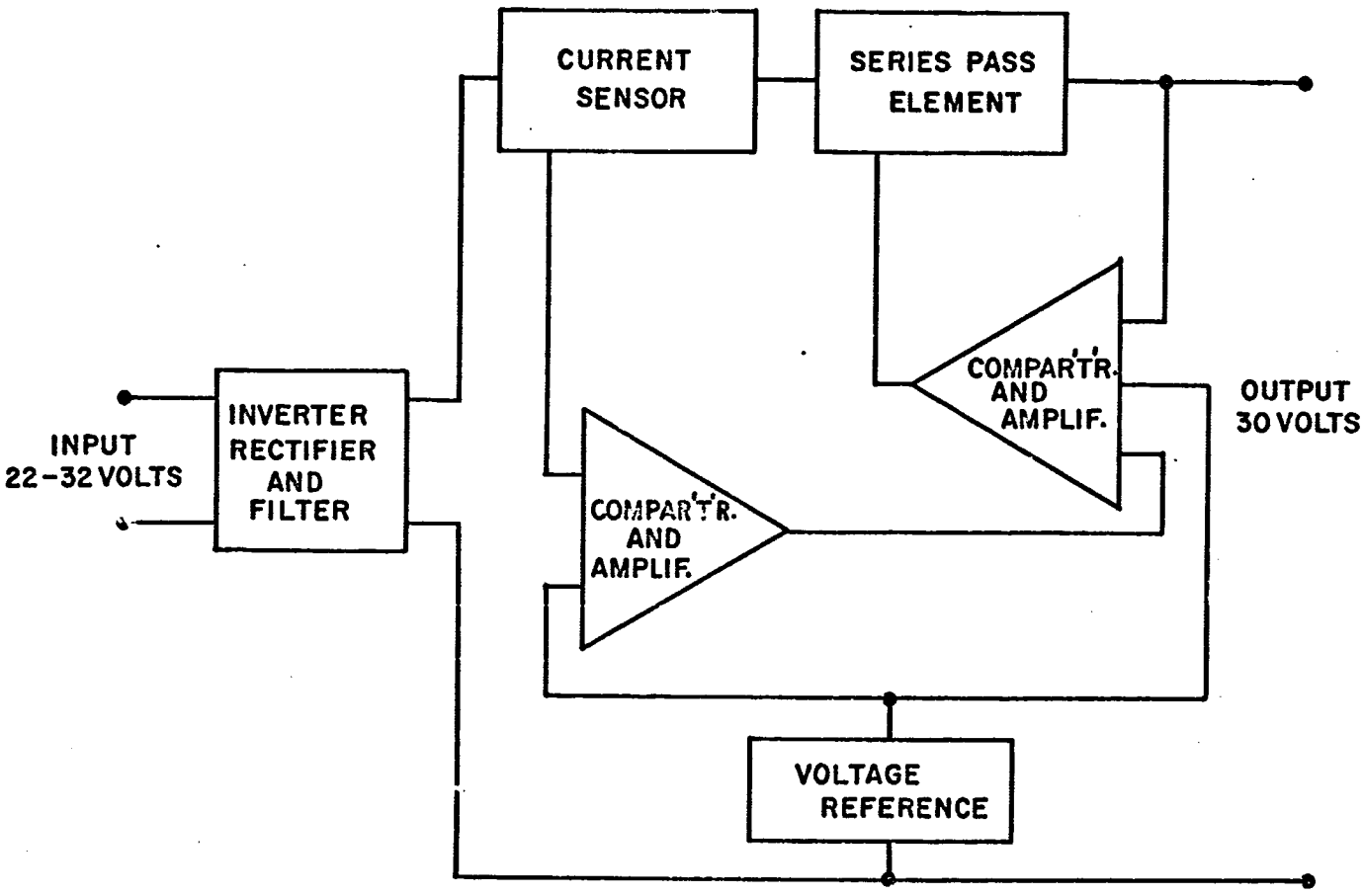
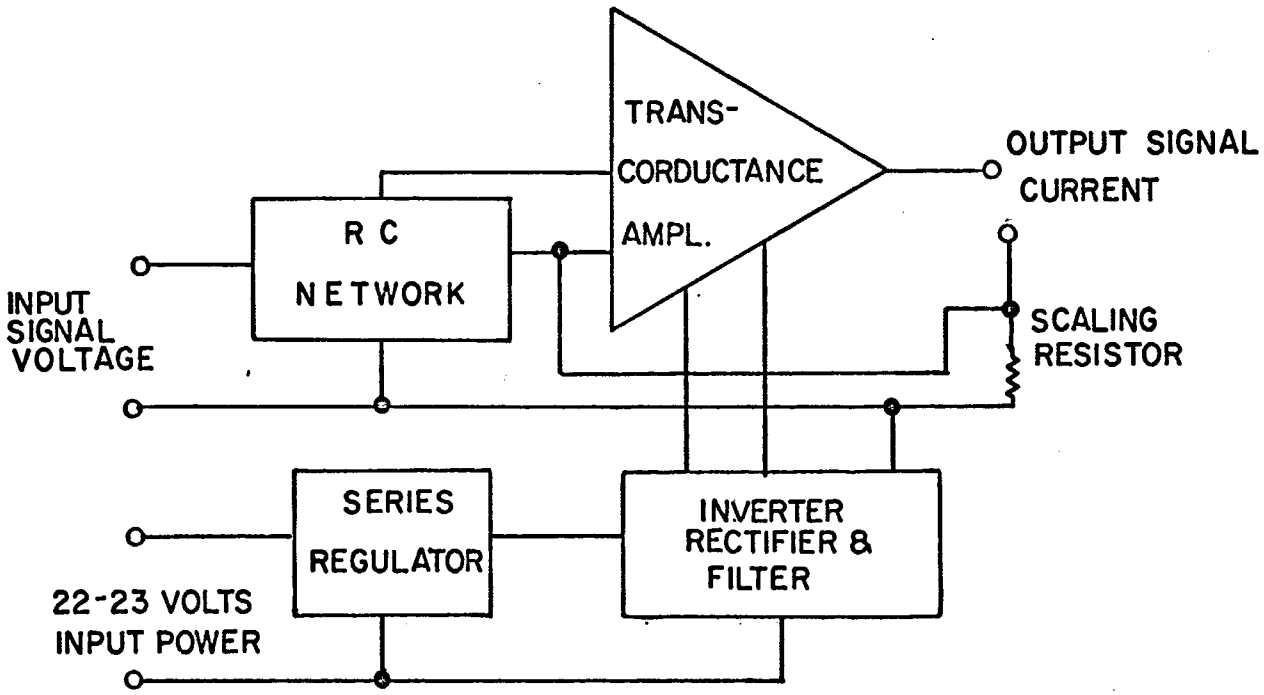


FIGURE 2. BETA COMMAND POWER SUPPLY BLOCK DIAGRAM

Active Filter

The active filter is designed to accept a low frequency analog signal, shape its amplitude and phase characteristics in a prescribed manner, and provide at its output terminals a current at a high impedance level proportional to the input signal voltage. The circuit is capable of driving as many series-connected magnetic amplifier signal windings as required by the system. Both the input and output are isolated from the 28 volt input power lines.

The R-C network used for a particular application will depend upon the amplitude and phase characteristics required. The resistors will, in general, be less than one megohm and the capacitors less than one microfarad.



The high impedance levels utilized in the R-C network require that the transconductance amplifier exhibit an extremely high input impedance characteristic. A junction N channel field effect transistor was selected for the amplifier first stage because of its high input impedance and good stability as a function of time and temperature. The bias level for this stage is established by another field effect transistor operating at a constant current.

The feedback scheme used within the amplifier was selected to produce a high impedance at the output of the amplifier. The high output impedance is achieved by making the feedback voltage proportional to the output current instead of the output voltage. The high output impedance is required to minimize the coupling between signal windings of different magnetic amplifiers and to minimize the loss in magnetic amplifier gain due to loading effects.

The gain scale factor for the transconductance amplifier is established by the value of the scaling resistor. The resistance value required can be calculated by taking the ratio of the full scale input voltage to the value of full scale output current required.

CIRCUIT SPECIFICATIONS

Input Voltage Range	22 to 32 volts minimum
Temperature Range	-55 to $+125^{o}$C minimum
Input Signal Voltage	30 volts p-p maximum
Output Current	5×10^{-3} ma maximum
Null Drift	$\pm 10^{-2}$ volts maximum referred to $+25^{o}$C

R-C Network Design

An optimum R-C network configuration would be one which contained the fewest number of elements and which is general enough to satisfy all of the requirements of the various filter types. The active filter is to replace one or two pole low pass filters, two pole notch sections, and a notch low pass combination. (See Figure 3.)

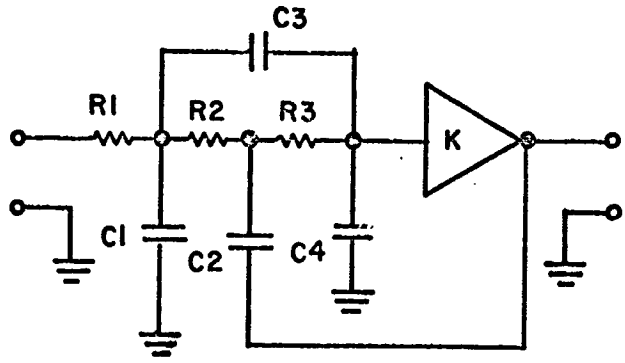


FIGURE 3. ACTIVE FILTER

The combination of R_2, R_3, C_2 and C_3 comprise the symmetrical notch filter. Capacitor C_4 gives the notch an unsymmetrical shape. R_1 and C_1 add an additional pole which makes the complete configuration have a two zero, three pole nature. If a two pole low pass section is needed, C_1 and C_3 are eliminated. If a one pole network is needed, C_1, C_2 and C_3 are eliminated. The feedback to capacitor C_2 gives use to the pass of complex poles of the notch section if C_3 is used or to the lowpass filter if $C_3 = 0$.

This entire concept was developed on an in-house, company funded study program just recently concluded. It involved analyzing all known filter requirements of the Saturn/ Apollo vehicles. The purpose of the study was to determine if any similarity existed between filters of a given channel for the various missions; or if any similarity existed between filters of the various channels for a given mission. Sufficient similarity was found to make a "building block" approach feasible, whereby various low-pass sections could be combined with various notch sections to obtain the desired response characteristics.

Method of Analysis

A comprehensive study of all filters used in the Saturn I, IB, and V computers, for which information was available, was made. The following list includes all the missions analyzed:

a. SA 5
b. SA 5 Mod 2 Rev I
c. SA 6
d. SA 6 Mod 2 Rev 2A
e. SA 7
f. Prod 1 Environmental
g. Mod 3
h. Mod 3, Rev I
i. AS 201, Production 2-5
j. AS 202, Production 6-7
k. AS 203, Production 8-9
l. AS 204, Production 10
m. AS 205
n. AS 201
o. AS 502

Transfer functions for most of these filters were not available, and therefore were derived by analysis of the schematic diagrams. Amplitude and phase data was then obtained by computation through the use of a digital computer. The missions prior to the AS 201 had very complicated filters and fairly elaborate responses. It was thought that particular care may have been taken with these designs because they were for the first missions. These elaborate filters were replaced in the latter missions by much simpler ones. It is thought, therefore, that active filter replacements need not be found for these early filters. Some of the later filters were designed completely of R-C sections with no inductors. Here again, these were not included as active filter equivalents because they could be used as is, or could be rescaled in impedance level and used in conjunction with a buffer amplifier. The remaining filters were of one of the following forms:

a. $$F_1(s) = \frac{S^2 + a_1 S + a_0}{C_4 S^4 + C_3 S^3 + C_2 S^2 + C_1 S + C_0}$$ (Equation 1)

b. $$F_2(s) = \frac{S^2 + a_1 S + a_0}{b_3 S^3 + b_2 S^2 + b_1 S + b_0}$$ (Equation 2)

c. $$F_3(s) = \frac{S^2 + a_1S + a_0}{b_3S^3 + b_2S^2 + b_1S + b^0} \times \frac{S^2 + b_1S + b_0}{d_3S^3 + d_2S^2 + d_1S + d_0}$$ (Equation 3)

$F_1(s)$ is composed of a pair of complex conjugate zeroes, a pair of complex conjugate poles, and two real poles. It is evident from the circuits and analysis that one of the real poles is far removed from all other poles (15-20 times the sigma of the other real pole) and so has negligible effect until quite high frequencies are considered. This pole appears to be a parasitic pole caused by the finite driving source impedance. The driving source impedance is not a parameter specified by NASA in each filter configuration and varies from one driver to the next. This pole is therefore uncontrolled and its synthesis would appear to yield no real benefit. This assumption will be adopted in the remainder of the proposal, but with the understanding that synthesis could be performed if such a pole were really desired. If this pole is removed from $F_1(s)$, then, the transfer function is of the form $F_2(s)$.

$F_3(s)$ is a cascade of two filters having the transfer function of $F_2(s)$ and can be of the same design except for part values.

Building Block Approach

Transfer functions of the form of $F_2(s)$ can be synthesized as the following schematic.

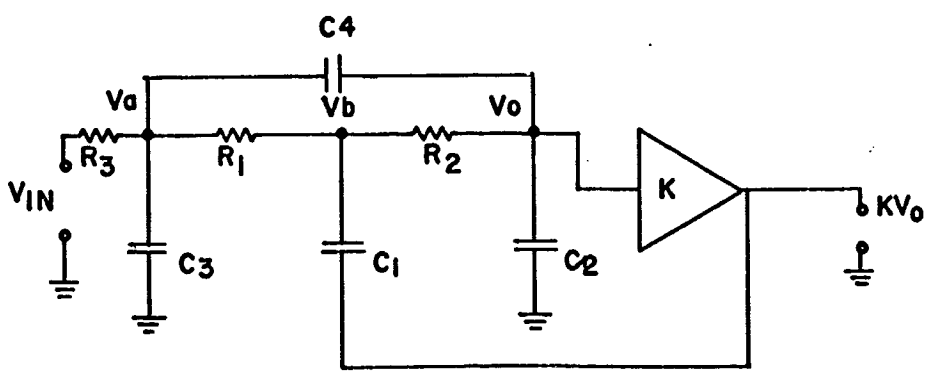


FIGURE 4. ACTIVE FILTER SCHEMATIC BLOCK DIAGRAM

The following analysis refers to this schematic

$$\begin{bmatrix} V_a \\ V_b \\ V_o \end{bmatrix} = \begin{bmatrix} 1 + \frac{R_3}{R_1} + S(C_3 + C_4) R_3 & -\frac{R_3}{R_1} - SC_4R_3 & \\ & & \\ -\frac{1}{R_1}\frac{1}{R_1} + \frac{1}{R2} + SC_1 & -(\frac{1}{R_2} + KC_1) & \\ & & \\ -SC_4 & -\frac{1}{R_2} + \frac{1}{R_2} + S(C_2 + C_4) & \end{bmatrix} \times \begin{bmatrix} V_1 \\ \\ 0 \\ \\ 0 \end{bmatrix}$$

(Equation 4)

After manipulation

$$\frac{V_0}{V_1} = \frac{R_1R_2C_1C_4S^2 + (R_1 + R_2) C_4S + 1}{a\,S^3 + bS^2 + C\,S + 1} \qquad \text{(Equation 5)}$$

where $a = R_1 R_2 R_3 C_1 (C_2 C_3 + C_2 C_4 + C_3 C_4)$

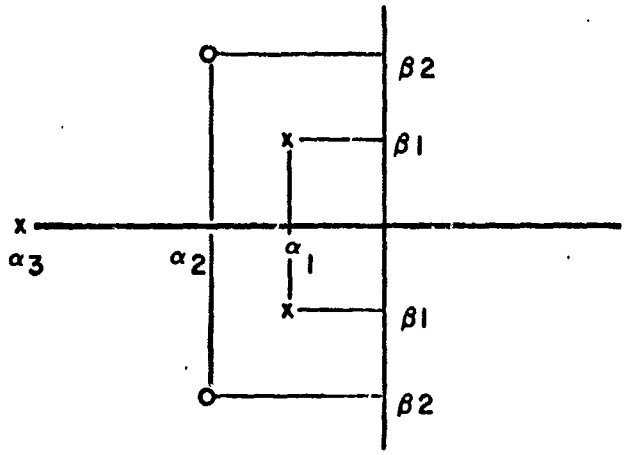
$$b = R_1 R_3 \left[(C_2C_3 + C_2C_4 + C_3C_4) + C_1 (C_3 + C_4) (1 - K)\right] +$$

$$R_2R_3 \left[(C_2C_3 + C_2C_4 + C_3C_4) + C_1 (C_2 + (1 - K) C_4)\right] +$$

$$R_1R_3 \left[C_1 (C_2 + C_4)\right]$$

$$c = R_1 \left[C_2 + C_4 + C_1 (1 - K)\right] + R_2 (C_2 + C_4) + R_3 (C_2 + C_3 + C_1 (1 - K))$$

A similar expression (Equation 7) can be formed from the pole-zero plot as follows:



$$\frac{V_0}{V_1} = \frac{(S + \alpha_2 + j\beta_2)(S + \alpha_2 - j\beta_2)}{(S + \alpha_3)(S + \alpha_1 + j\beta_1)(S + \alpha_1 - j\beta_1)} \qquad \text{(Equation 6)}$$

By combining and rearranging terms in Equation 6 the following equation results:

$$= \frac{\left(\alpha_2^2 + \beta_2^2\right)\left[\frac{1}{\alpha_2^2 + \beta_2^2} S^2 + \frac{2\alpha_2}{\alpha_2^2 + \beta_2^2} S + 1\right]}{\alpha_3\left(\alpha_1^2 + \beta_1^2\right)\left[\frac{1}{\alpha_3(\alpha_1^2 + \beta_1^2)} S^3 + \frac{1 + \frac{2\alpha_1}{\alpha_3}}{\alpha_1^2 + \beta_1^2} S^2 + \frac{1}{\alpha_3} + \left(\frac{2\alpha_1}{\alpha_1^2 + \beta_1^2}\right) S + 1\right]} \qquad \text{(Equation 7)}$$

By equating coefficients of identical terms in Equation 5 and Equation 7, the following equations result:

$$\frac{1}{\alpha_2^2 + \beta_2^2} = R_1 R_2 C_1 C_4 \qquad \text{(Equation 8)}$$

$$\frac{2\alpha_2}{\alpha_2^2 + \beta_2^2} = (R_1 + R_2)\, C_4 \qquad \text{(Equation 9)}$$

$$\frac{1}{\alpha_3 (\alpha_1^2 + \beta_1^2)} = R_1 R_2 R_3 C_1 \left[C_2 C_3 + C_2 C_4 + C_3 C_4\right] \qquad \text{(Equation 10)}$$

$$\frac{1 + \frac{2\alpha_1}{\alpha_3}\ R_1 R_3 \left[C_2 C_3 + C_2 C_4 + C_3 C_4 + C_1 (1-K)(C_3 + C_4)\right] + R_1 R_2 C_1 (C_2 + C_4)}{\alpha_1^2 + \beta_1^2} = + R_2 R_3 \left[C_2 C_3 + C_2 C_4 + C_3 C_4 + C_1 (C_2 + C_4 (1-K))\right] \qquad \text{(Equation 11)}$$

$$\frac{1}{\alpha_3} + \frac{2\alpha_1}{\alpha_1^2 + \beta_1^2} = R_1 \left[C_2 + C_4 + C_1 (1-K)\right] + R_2 (C_2 + C_4) + R_3 \left[C_2 + C_3 + C_1 (1-K)\right] \qquad \text{(Equation 12)}$$

Since there are five equations which must be solved simultaneously while there are eight unknowns, three of the unknowns can be chosen somewhat arbitrarily. Choosing $R_1 = R_2$ makes the spread of resistors as small as possible. Choosing $C_1 = 1.0$ ufd fixes the impedance level of the filter and also makes the largest capacitor = 1.0 ufd. (To eliminate adjustments of the gain (feedback factor), K is chosen to be the closed loop gain of amplifier. It will be kept as K in the equations, but no longer is an unknown.) It is assumed to be 0.995.

$$\frac{\text{Eq (9)}}{\text{Eq (8)}} = 2\alpha_2 = \frac{(R_1 + R_2)}{R_1 R_2 C_1}$$

Since $C_1 = 1$ and $R_1 = R_2 = R = \frac{1}{\alpha_2}$

Using this value for R in Equation 9 yields $C_4 = \frac{\alpha_2^2}{\alpha_2^2 + \beta_2^2}$ (Equation 13)

Define $g = \dfrac{\alpha_1^2 + \beta_1^2 + 2\alpha_1\alpha_3}{\alpha_2^2}$ (Equation 14)

and $h = \dfrac{\alpha_3 + 2(\alpha_1 - \alpha_2)}{\alpha_2}$ (Equation 15)

Using these definitions along with the expressions for R_1, R_2, C_1, C_4 and after lengthy simplification where

$$C_3' = \left[1 + \frac{R_3}{R_1}\left(1 - gC_4\left(1-3\left(1-K\right)\right)\right) - h\left(1-K\right)\left(1 + \frac{R_3}{R_1}\right) - \left(1-K\right)\left(2 + \frac{R_3}{R_1}\right)\right] \Big/ 2\frac{R_3}{R_1}\left(h - g\left(1-K\right)\right) \quad \text{(Equation 16)}$$

$$C_3 = C_3' + \sqrt{\left(C_3'\right)^2 + \left[\frac{C_4^2 R_3}{R_1}\left[g\left(1-2\left(\frac{R_3}{R_1}\right)\left(1-K\right)\right) - 2h\right] + \frac{C_4 R_3}{R_1}\left(1-h\left(1-K\right)\left(1+\frac{R_2}{R_1}\right) - 2\left(1-K\right)\left(2+\frac{R_3}{R_1}\right)\right) + \left(1-K\right)\left(1+2\left(\frac{R_3}{R_1}\right) + \left(\frac{R_3}{R_1}\right)^2\right)\right] \Big/ \left(\frac{R_3}{R_1}\right)^2\left(h - g\left(1-K\right)\right)} \quad \text{(Equation 17)}$$

$$C_2 = \frac{C_4\left(1 - hC_3\frac{R_3}{R_1}\right) + \frac{R_3}{R_1}\left(1-K\right)\left(C_3 + 2C_4\right)}{\frac{hR_3}{R_1}\left(C_3 + C_4\right) - \left(1 + \frac{R_3}{R_1}\right)} \quad \text{(Equation 18)}$$

Equations 16-18 would be solved for C_3', C_3, and C_2 if R_3 were known. R_3 is assumed and equations 16-18 are solved. The resultant C_2 C_3 and assumed R_3 are used in Equation 10 along with the known values for R_1, R_2, C_1, and C_4. If the right hand expression in the equation does not equal the left hand expression, R_3 is incremented until there is a compatible solution. At this point all the values are solved and the design is complete.

The building block approach originally had five basic units. Since the missions prior to the AS201 mission were omitted there remains only one building block.

The trimming technique described in ECI's Technical Proposal N-50364 "Study of Active Filter Building Blocks for Saturn IB and Saturn V Computers" will be used. Resistors will be comprised of a fixed resistor in series with a thin film resistor. The capacitors will be the parallel combination of a fixed capacitor and small-value capacitor chips which are a small percentage of the total value. The major benefit of this type of trimming capability is the quick turn-around time assuming last minute changes become necessary. No large stock-piles of many different values of components are necessary.

Computer Program

A computer program was written to solve for the components of the filter. Basically, it evaluated the expression in the previous section. It is completely automated. Inputs are the complex pole and zero frequencies of the transfer function and the gain of the amplifier. The outputs are the component values. The amplitude and phase response of the filter is then computed. The inputs are initial frequency, final frequency and increment. The output is amplitude as a numeral, amplitude in db and phase in degrees.

Results

Twenty-one filter transfer functions taken from actual S1, SIB and SV filter requirements have been synthesized using this one building block. The following tabulation gives the component values for the filter and their missions.

Filter No.	Channel	Mission	Stage	Switch Point
1	$\dot{\phi}R$	SA202	SI	Open
2	$\dot{\phi}R$	SA202	SI	Closed
3	$\dot{\phi}R$	SA201	SI	Open
4	$\dot{\phi}R$	SA201	SI	Closed
5	ϕR	Mod 3 Rev. 1, Prod. 1	SI	Open

Filter No.	Channel	Mission	Stage	Switch Point
6	$\dot{\phi}$R	Mod 3 Rev. 1, Prod. 1	SI	Closed
7	$\dot{\phi}$Y & P	SA203 Mod. 0 Rev. 1B	SIV	Open
8	$\dot{\phi}$Y & P	SA203 Mod. 0 Rev. IB	SIV	Closed
9	$\dot{\phi}$Y & P		SIV	Open
11	$\dot{\phi}$Y & P	SA201	SIV	Open
12	$\dot{\phi}$Y & P	SA201	SIV	Closed
13	$\dot{\phi}$Roll	SA203	SI	Open
14	$\dot{\phi}$Roll	SA203	SI	Closed
15	$\dot{\phi}$Y & P	SA203 Mod. 0 Rev. IB	SI	Closed
16	$\dot{\phi}$Y & P	SA203 Mod. 0 Rev. IB	SI	Open
17	$\dot{\phi}$Y & P	SA201, SA 203, Mod. 0 Rev. IB	SI	Open
18	$\dot{\phi}$Y & P	AS502	SIV	
19	$\dot{\phi}$R	AS205	SI	
20	$\dot{\phi}$Y & P	AS205	SIV	
21	$\dot{\phi}$Y & P	AS205	SI	

Study Areas

For some of these filters, the value of R_3 is appreciably greater than R_1 and R_2. Its value could be reduced if the proportion of amplifier output voltage fed back through C_1 is reduced a few percent. This would have the advantage that the null offset versus temperature would decrease. Also, the physical size of resistor R_3 would decrease.

It has been determined that the frequency of the notch in the circuit (Figure 5) can be electronically controlled by the use of two inputs having the same frequency and phase and differ only in amplitude. By changing the relative amplitudes the zeroes will move up or down the imaginary frequency axis. This feature deserves more investigation. The effective R-C product can be multiplied by the ratio of the inputs, hence the notch frequencies can be made lower without increasing the R-C product. It is likely that the same approach could be applied to the circuit of Figure 4.

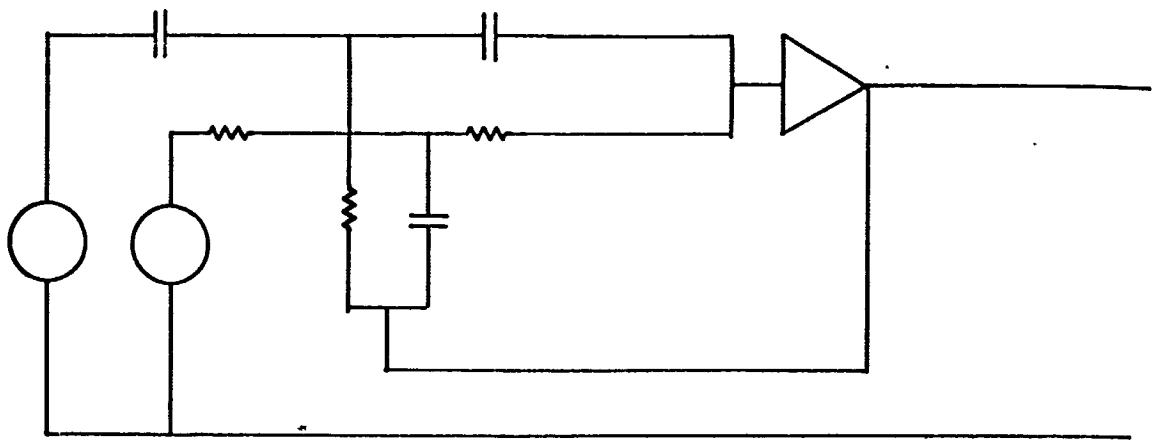


FIGURE 5. SPLIT INPUT SCHEME

Summary:

This overall approach will result in an optimized active filter application which not only meets requirements of functions which have been reviewed, but also will provide guide lines for analyzing and anticipating future functions which may be encountered. In this manner a "tool" similar to the "stocking" technique used on Saturn IB/V flight control computer filters will be made available to the NASA micromin computer program. It is anticipated that in using this technique the response time to filter changes at ECI can be reduced to days rather than weeks presently experienced on the Saturn IB/V Programs. Also, a close coordination of the program with the Flight Dynamics Group of NASA can well result in reduced response time to requirements by that group.

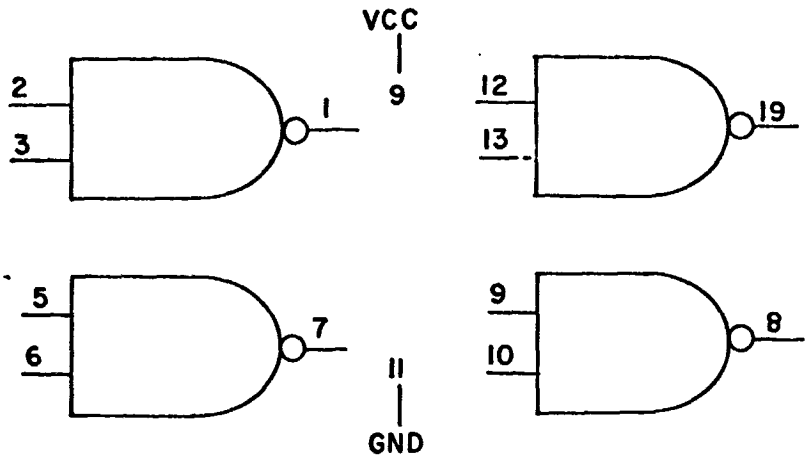
PART VALUES

	C_1	C_2	C_3	C_4	R_1	R_2	R_3	K
1	.1000000E+01	.1257487E-1	.5161463E0	.1000300E-1	.4000000E0	.4000000E0	.1474700E0	.995
2	.1000000E+01	.122988E-1	.4577896E0	.1000000E-1	.4000000E0	.4000000E0	.1657600E0	.995
3	.1000000E+01	.2989426E-1	.4029298E0	.1340000E-1	.4000000E0	.4000000E0	.3358700E0	.995
4	.1000000E+01	.2895998E-1	.3764210E0	.1340000E-1	.4000000E0	.4000000E0	.3549200E0	.995
5	.1000000E+01	.2024095E-1	.2687879E0	.1000000E-1	.4000000E0	.4000000E0	.3035600E0	.995
6	.1000000E+01	.1971166E-1	.2546048E0	.1000000E-1	.4000000E0	.4000000E0	.3199200E0	.995
7	.1000000E+01	.2104735E-1	.3415484E0	.1750000E-1	.4000000E0	.4000000E0	.2801900E0	.995
8	.1000000E+01	.2063730E-1	.3263154E0	.1750000E-1	.4000000E0	.4000000E0	.2922000E0	.995
9	.1000000E+01	.7128760E-2	.9708101E-1	.8571428E-2	.7000000E0	.7000000E0	.4308500E0	.995
10	.1000000E+01	.6834671E-2	.8813064E-1	.9685713E-2	.7000000E0	.7000000E0	.4713100E0	.995
11	.1000000E+01	.2104735E-1	.3415484E0	.1750000E-1	.4000000E0	.4000000E0	.2801900E0	.995
12	.1000000E+01	.2063730E-1	.3263154E0	.1750000E-1	.4000000E0	.4000000E0	.2822000E0	.995
13	.1000000E+01	.1248330E-1	.5351922E0	.1250000E-1	.4000000E0	.4000000E0	.1413400E0	.995
14	.1000000E+01	.1209779E-1	.4679414E0	.1250000E-1	.4000000E0	.4000000E0	.1611700E0	.995
15	.1000000E+01	.3434088E-1	.4388500E0	.1410000E-1	.4000000E0	.4000000E0	.4437800E0	.995
16	.1000000E+01	.3136151E-1	.4473793E0	.1410000E-1	.4000000E0	.4000000E0	.4328700E0	.995
17	.1000000E+01	.3349564E-1	.5246781E0	.1410000E-1	.4000000E0	.4000000E0	.3842000E0	.995
18	.1000000E+01	.4585808E-2	.3444858E-1	.5000000E-2	.4000000E0	.4000000E0	.2044119E+1	.995
19	.1000000E+01	.1189385E-1	.3272559E0	.9999750E-2	.4000000E0	.4000000E0	.2364600E0	.995
20	.1000000E+01	.3236922E-2	.5898734E-1	.8571370E-2	.7000000E0	.7000000E0	.1253300E+1	.995
21	.1000000E+01	.1500109E-1	.1223602E0	.8639080E-2	.6365372E0	.6365372E0	.1797269E+1	.995

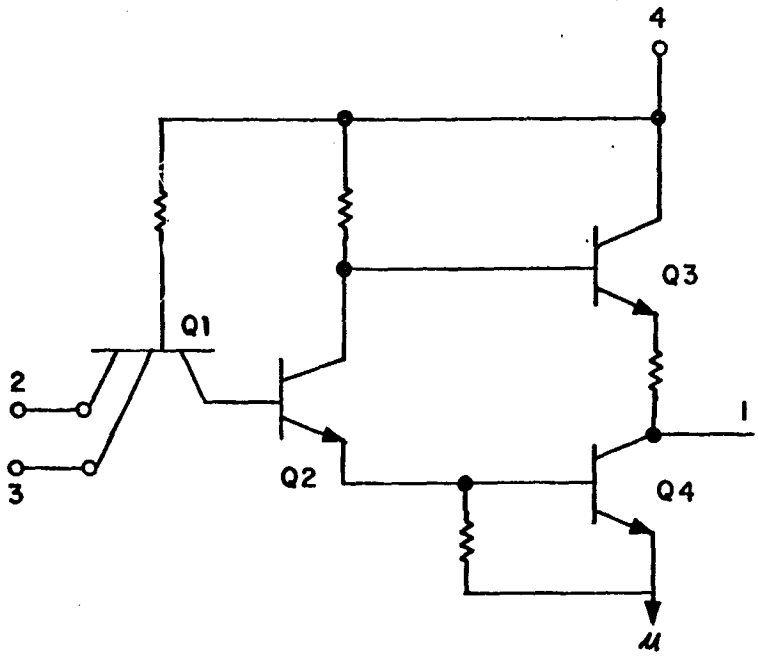
Digital Circuits

Operation

In discussing the operation of the digital circuits, the operation of the basic gate and flip-flop functions should be understood. The simplest gate in use is the SE 480J (a quad-two input NAND-NOR circuit in a 14 pin 1/4 in. x 3/8 in. ceramic flat pack). A block digram is shown.



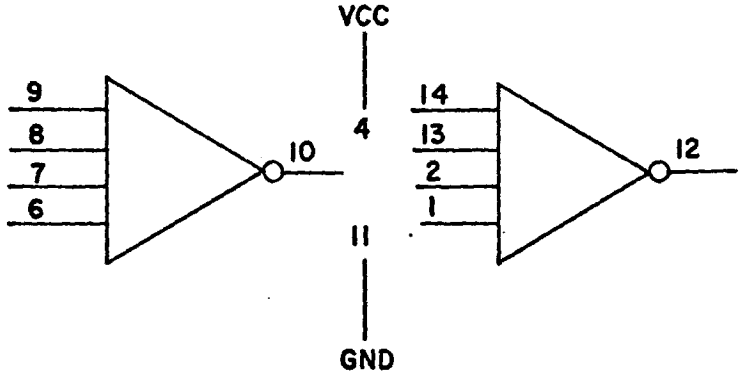
Each of the four blocks represent an independent two-input gate. The circuit represented by each gate is as follows:



By using a dual emitter T. T. L. input, the controlling input assumes a low condition. That is, when either input is below 0.5 V DC the output of the circuit will be high (4.0 V DC approximately). This is caused by all the base drive current for Q_4 being shunted through the emitter circuit of Q_1. If the other emitter circuit is in the high state, then this emitter is reverse biased with respect to the base. When both emitters are "high," current flows in the base of Q_1 to the collector in a normally reverse direction because of the forward biasing of the P-N junction between Q_1 base and Q_1 Collector. This results in the output transistor Q_4 being biased on, resulting in a saturated output of about 0.2 V DC (a low state).

In order to AND two inputs it can now be seen that two high inputs have to be present to produce a "low" output; hence, a negative "AND" or a "NAND" function. That is, if the inputs at pins #2 and #3 are high, the output at pin #1 will be "low." No other input combination will result in a low output state; hence, high pin #2 AND high pin #3 produce a low at pin #1. Likewise, a low input state can be used to produce a "NOR" function. That is, either pin #2 "OR" pin #3 low will produce a "high" output on pin #1. Since there is an output inversion, the "NOR" is generated.

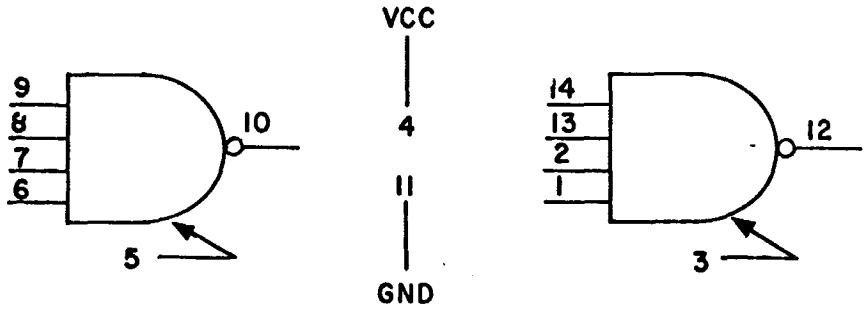
The next simplest gate is the SE 455J dual-four input driver buffer gate (in a 14 lead, 1/4 in. x 3/8 in. flat pack). The buffer-driver block diagram is shown below.



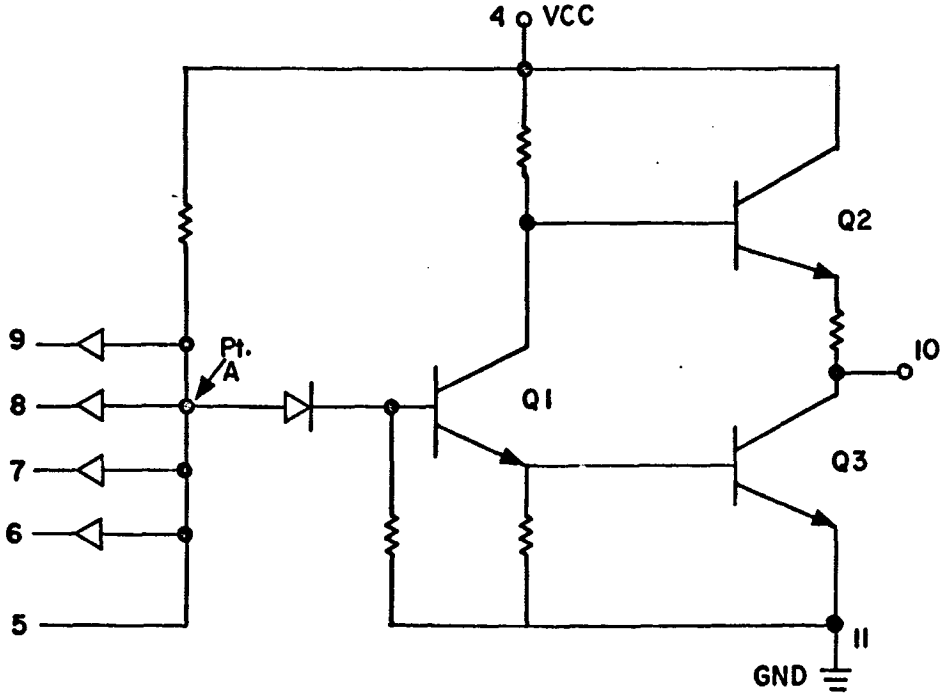
The schematic diagram for each gate is similar to that of the SE 480J as shown, with more drive capability and more inputs.

The main differences between this gate and the SE 480J are the quad emitter on Q_1, lower values of resistance in all resistors and the diode by-pass of the output resistor. The same conditions that apply for the SE 480J inputs apply for the SE 455J inputs except that four inputs can be "NANDed" or NORed." This circuit will drive 20 other low powered gates where the SE 480J will drive only 7. It also uses more power; 16 mw/gate as opposed to 4.5 mw/gate for the SE 480J.

Another gate is the SE 416J dual-four input expandable "NAND" gate. The block diagram is shown below.



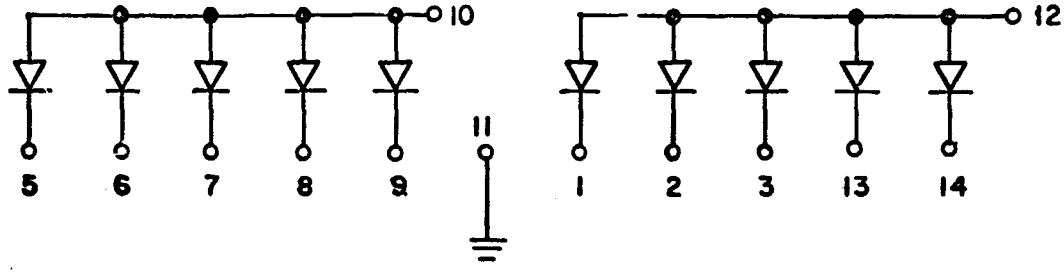
The schematic for this circuit is also shown.



This gate is used for multiple input "NANDing" functions or "NORing" functions.

In this case, the output at the SE 416J gate will be low only if all the inputs are high. This can be seen by the fact that if any of the inputs are low, Point A will be clamped one diode drop above the low value, cutting off all base current to Q_1. This results in Q_2 being "on," Q_3 being "off," and the output being "high." This gate is also capable of being expanded to allow for more than four inputs to be "ANDed." The inputs used for this purpose are pins #3 and #5. The device used for expanding this device is the SE 106J.

The SE 106J is a ten diode array arranged as shown below:



By connecting pin #10 or pin #12 to the expander input on the SE 416J (pins #3 or #5), the input diodes on this gate are paralleled by those in the diode array. This results in the gate being expanded from four inputs to nine inputs. This array is packaged in a fourteen pin 1/4" x 3/8" flat pack and requires no power input.

The most used device, and perhaps the most important device, in the digital C. A. T. and spatial amplifier circuits is the SE 424J-dual R-S flip-flop. Using the same 1/4" x 3/8" fourteen pin flat pack the circuit configuration for this device is shown in Figure 6.

There are two of these circuits in each flat pack and since this is a high usage device, the package reduces the individual parts count considerably.

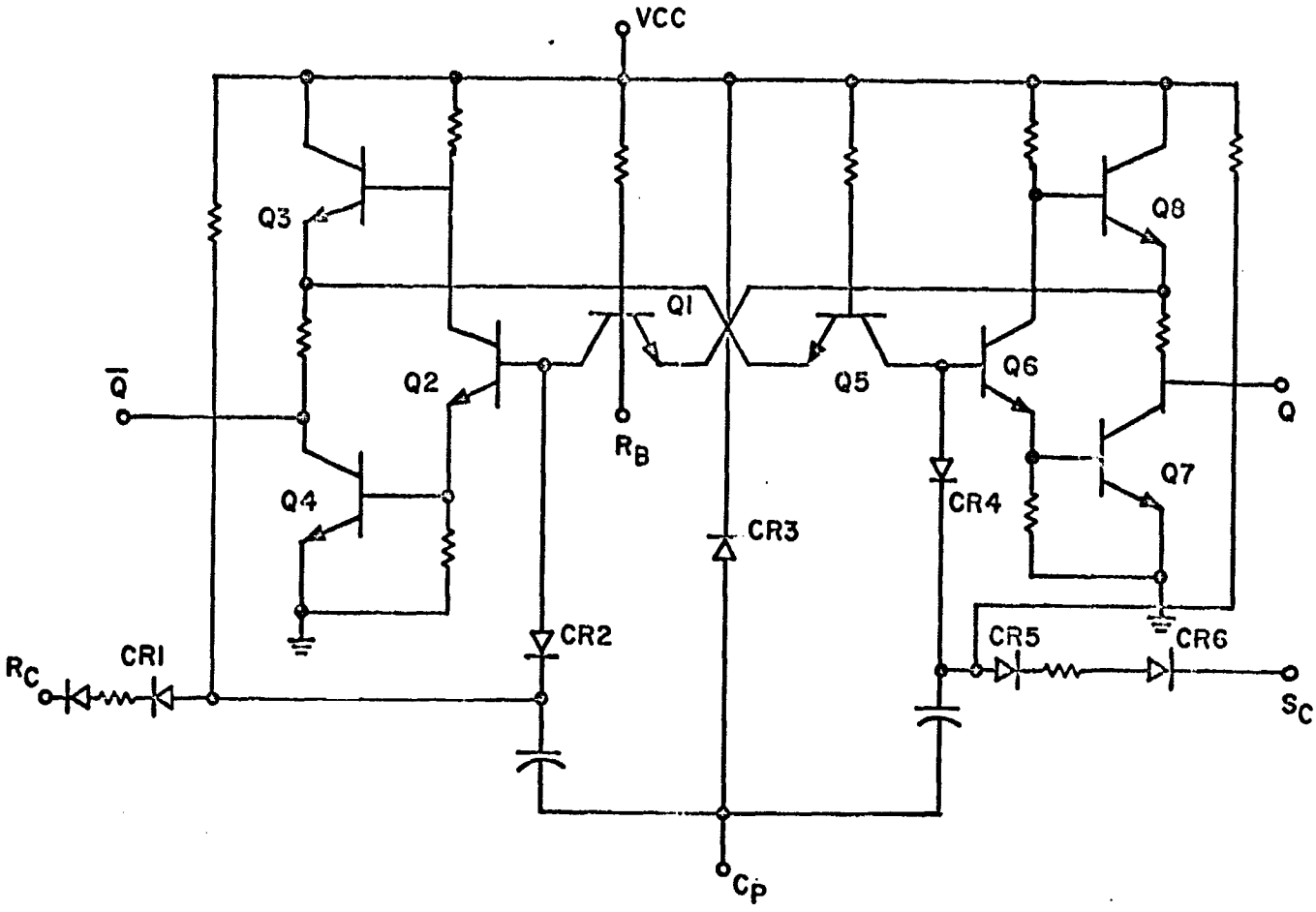


FIGURE 6. SCHEMATIC OF FLIP-FLOP

A truth table depicting the resulting outputs at Q and $\bar{Q}$ from the different set and reset conditions present at the time when the clock input is pulled from a "high" to a "low" state is as follows.

Cond #	Sc	Rc	Q	$\bar{Q}$
1	1	0	0	1
2	0	1	1	0
3	1	1	No Change	
4	0	0	Output Indeterminate	

Note that in condition #4 the resulting output state is indeterminate hence this set of set-reset conditions is a forbidden state condition. Number 3 results in no change in the output state. This condition is used to inhibit output change from undesired clocks or noise pulses.

The Rc input on this device is used to clear the flip-flop back to the zero state (that is Q "Lo" and $\bar{Q}$ "Hi"). When this input is pulled "Low," the base drive for Q_2 is shunted to ground and results in Q_2 and Q_4 being turned off and Q_3 being turned "On"; hence, $\bar{Q}$ output will be high and Q output will be low through the cross coupling.

The four previously described circuits constitute the majority of the logic devices used. The "Fan-Out" capabilities of each of these devices in terms of numbers of SE 480J inputs that can be driven (approximately 0.6 ma sinking current) is listed below.

		DC	AC
SE 480J	=	8	2
SE 455J	=	22	8
SE 416J	=	7	2
SE 424J	=	7	2

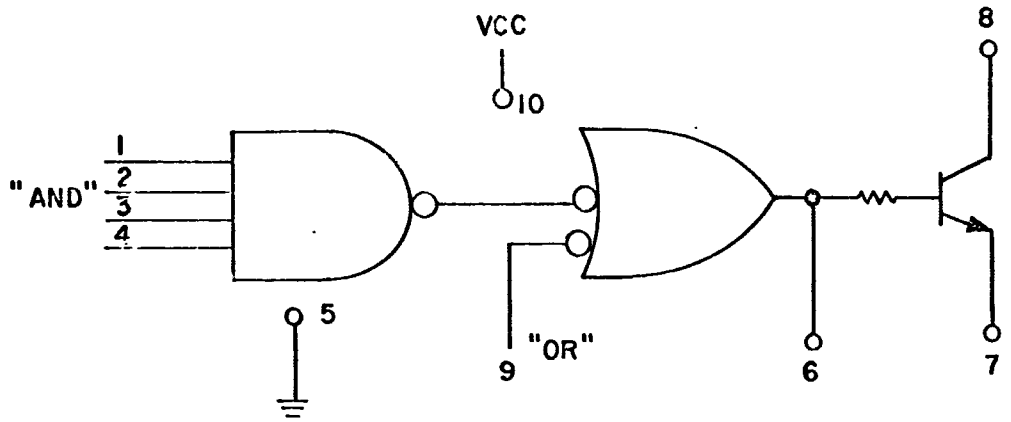
The AC Fan-Out refers to the number of SE 424J clock inputs that can be driven (unit load = 50 pf).

This series of devices was also selected because of the high noise immunity specification of 1.0 V over the full temperature range.

Other logic devices being used are the Fairchild μL951 Single Shot, the SH 2001 Relay Driver (Fairchild), the MWμL 909 RTL Buffer Driver (Fairchild), and the TIXD22 Eight Diode Array (common cathode-Texas Instruments).

The μL951 single shot is a D. T. L. type circuit with a two input OR capability which is expandable. Complementary outputs are available and the timing range is expandable with outside resistors or capacitors.

The SH 2001 consists of two cascaded μL932 gates in a package with a thin film resistor chip and an output transistor chip (2N3108). This device is capable of sinking 250 ma. A block diagram of the device is given below.



This is packaged in a 1/4" x 1/4" flat pack and has a four input AND gate input and a single OR input. Pin #6 can be used for latching functions by tying it back to an AND input and using the OR input as the latch input.

The MWμL909 is a two input NAND/NOR gate using the R. T. L. type input. It is used in the switching logic to discern between a +28 volt input and an open contact.

Digital Spatial Amplifier

Since the output of the spatial amplifier is a series of pulses of variable width, the circuit for the micromin version was redesigned using a digital format in place of the analog circuit used in the present computer. A block diagram of the digital spatial amplifier is shown in Figure 7.

The magnetic amplifier is similar to that used in the 50 ma servo amplifier design, and is described in detail previously. This device is used to isolate the input signals from each other and -28 V DC, while providing a nominal transconductance and a stable feedback approach.

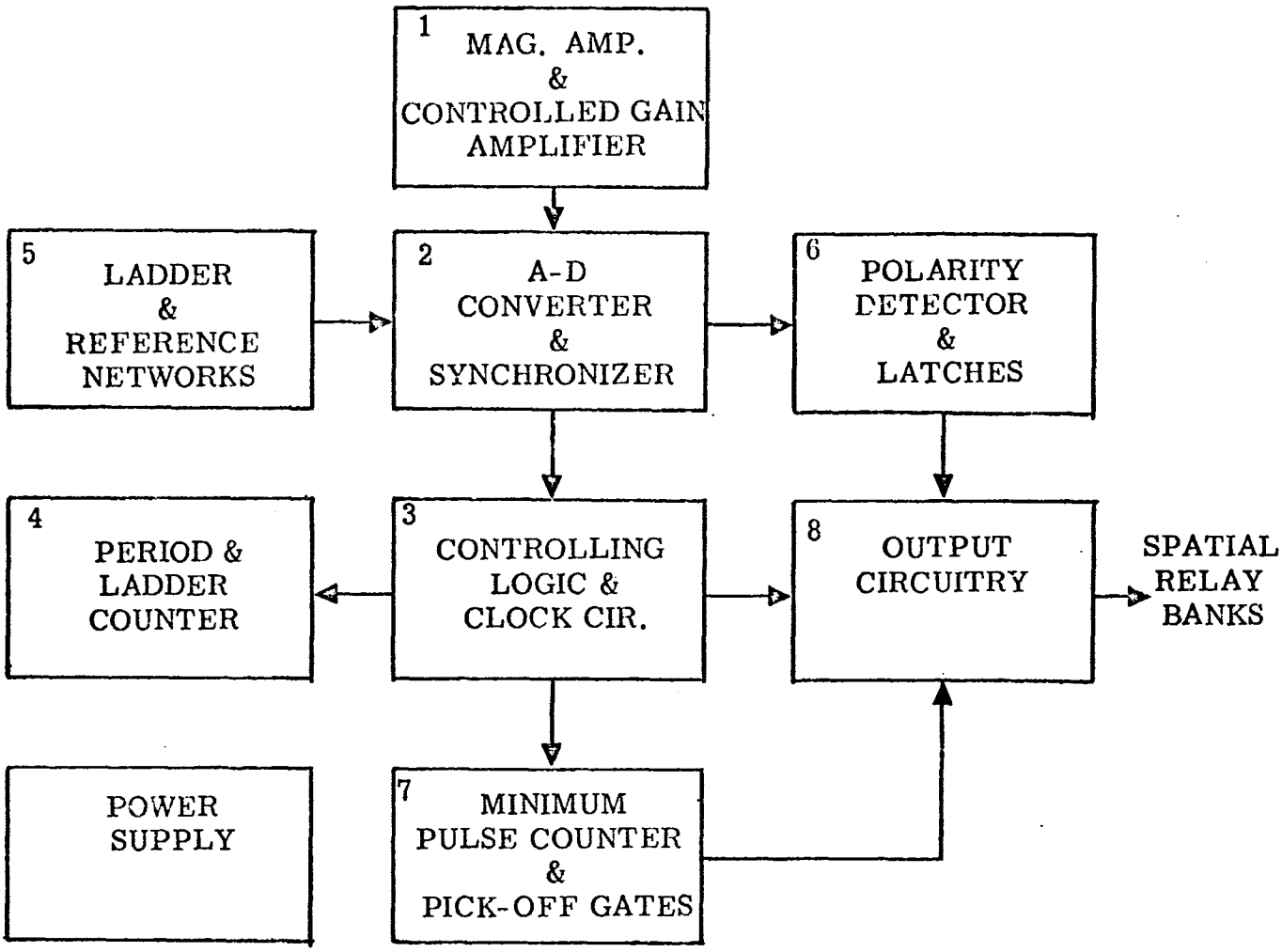


FIGURE 7. DIGITAL SPATIAL AMPLIFIER BLOCK DIAGRAM

The solid state amplifier consists of two cascaded differential amplifier stages employing two-stage Miller feedback for noise suppression and stability. Matched transistors on a common chip are used in each stage to minimize initial offsets and drift over the temperature range. The gain of both the magnetic amplifier and transistor amplifier is set at approximately $\frac{2.1\ V}{200\ \mu a}$ or 10.5 mv/μa which is adjustable to allow for initial variation of the voltage reference circuit. Common mode filtering capacitors are placed from the output collectors of the second stage to ground to reduce the effects of common mode signals.

The analog to digital section can be divided into the differertial-to-single ended converter, the ladder-analog output comparator stage and the current sensing, temperature compensated, synchronizing switch.

The differential-to-single ended converter is composed of matched emitter-follower circuits in cascade as shown in Figure 8.

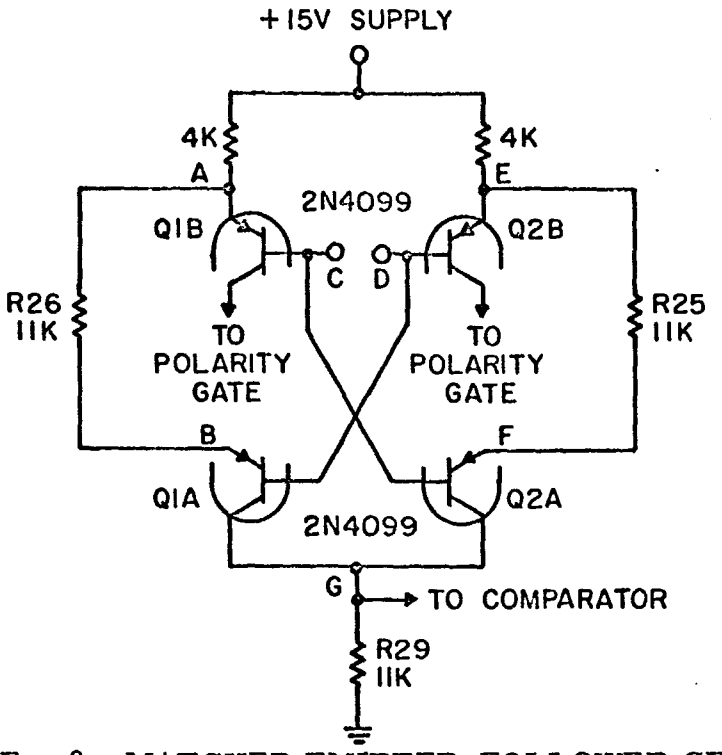


FIGURE 8. MATCHED EMITTER-FOLLOWER CIRCUITS

A differential voltage appearing at points C and D (V_{C-D}), assuming C more positive than D) results in point A being at $V_C + V_{be\ (Q1B)}$ and the voltage at point B being $V_D + V_{be(Q_1A)}$. If the two sides of Q_1 are V_{be} matched, then V_{A-B} is equal to $V_C + V_{be\ (Q_1B)} - V_D + V_{be\ (Q_1A)}$ and since $V_{be(Q_1A)} \approx V_{be(Q_1B)}$, $V_{A-B} = (V_C - V_D)$ or $V_{(C-D)}$. Hence the differential voltage V_{C-D} is developed across the 11 K (R26) resistor. Since the 2N4099 is a high gain transistor, then the current in Q_1A collector is approximately the same as the R26 current. By following the same logic it can be shown that Q_2A is cut off due to V_B being more positive than V_E (hence V_F). This then results in all the current in R29 being $I_{(R26)}$ hence V_{C-D} is developed across R29. When the polarity between C and D is reversed Q_2 is used and Q_1A is cut off.

The ladder-analog output comparator circuit is a simple comparator stage using matched transistors to minimize offsets. The schematic is shown in Figure 9.

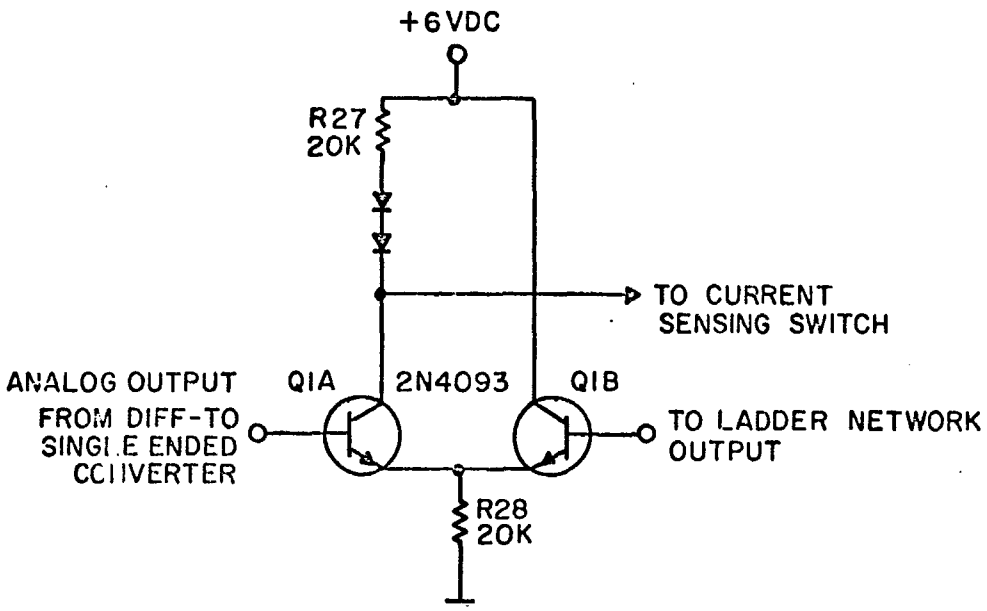


FIGURE 9. COMPARATOR OUTPUT CIRCUIT SCHEMATIC DIAGRAM

The analog output is continually compared to the output of the ladder network (the voltage of which is determined by the count in the ladder counter). When the analog output voltage exceeds the ladder network output, Q_1A conducts and the current sensing switch senses the collector current and when "ANDed" with the clock circuit to synchronize the digital output, turns on the output switch. The diodes in the collector of the comparator are used for temperature compensating the current sensing switch and output switch.

When the ladder output exceeds the analog output, Q_1B turns on and Q_1A turns off, resulting in the turn-off of the output switches.

The schematic of the current sensing and output switches and the synchronizing circuit is shown in Figure 10.

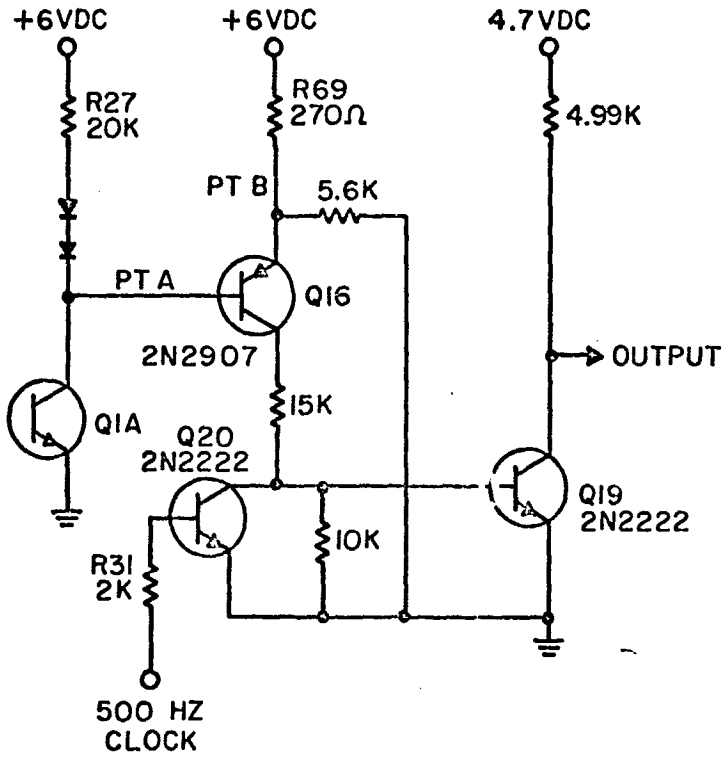


FIGURE 10. CURRENT SENSING SCHEMATIC DIAGRAM

When current flows in Q_1A collector, and the voltage at Point A drops below that at Point B, Q_{16} provides base drive to Q_{19}. Note that the collector of Q_{20} is tied to the base of Q_{19}. With this connection the clock is ANDed with the output of the comparator such that Q_{19} can only be switched on when the clock input is low. This synchronizes the output with the remaining digital circuitry to prevent logic race conditions and allows proper control and ease of logic implementation.

The controlling logic section consists of the logic necessary to interconnect the other sections and set up the necessary timing. Starting with A3A and A3B, these two input gates are cross coupled to provide a latching function as shown in Figure 11.

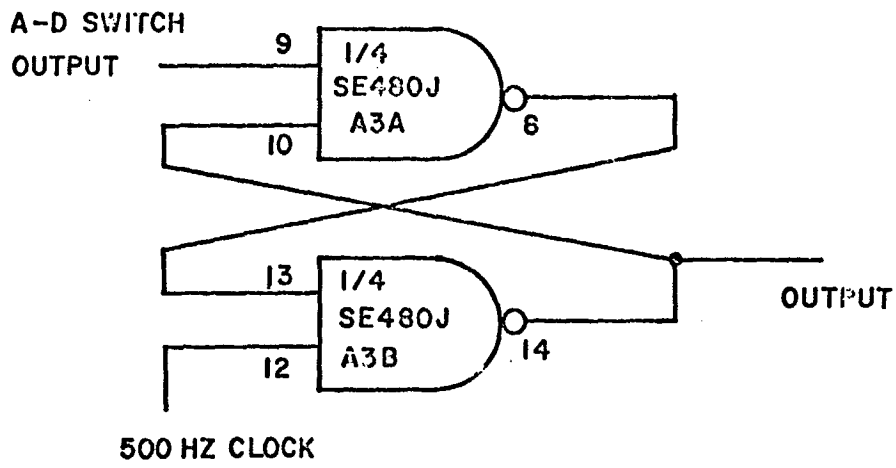


FIGURE 11. LATCHING FUNCTION

When output transistor Q_{19} of Figure 10 is just at threshold, the output state may oscillate between a "high" and "low" state and since this circuit is the decision-making circuitry, this has an undersirable effect on the output stability. The latch circuit provides that once Q_{19} is turned "on" during any clock period the output of the latch will stay "low" for that whole clock period.

The "latch" operates, assuming pin #8 (A3A) is LOW and inputs 9 and 10 of A3A are initially HIGH. Once a low state appears at pin #9 (A3A) pin #8 is forced HIGH. Using the timing diagram in Figure 12, pin #12 (A3B) is HIGH and pin #13 goes HIGH producing an "AND" condition on A3B which results in pir #14 A3B going LOW. This is fed back to pin #10 A3A holding the output of A3A HIGH. Now the output of A3A is latched HIGH by the LOW input on pin #10 regardless of the state of pin #9. Likewise, the output of A3B is latched low until the input of pin #12 switches to a LOW state and we return to the original state via the same process.

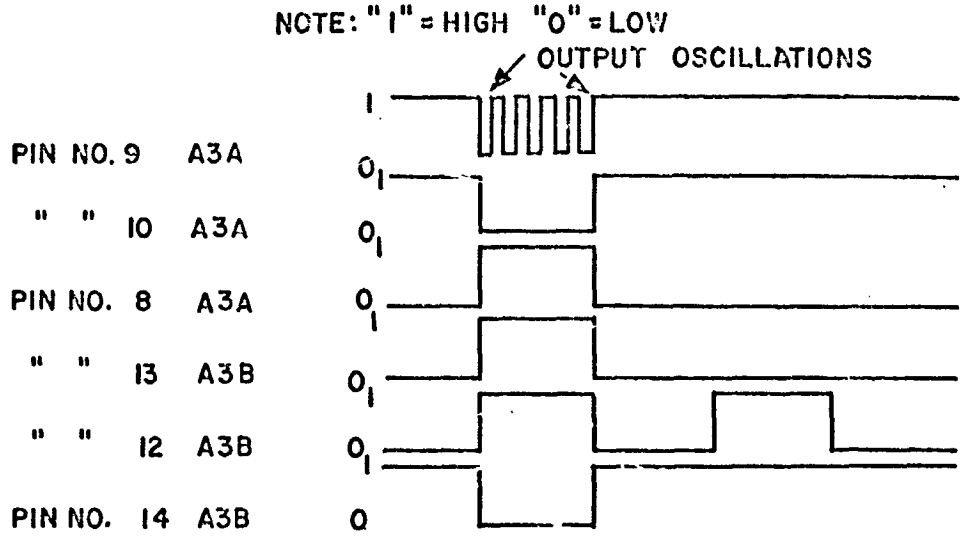


FIGURE 12. TIMING DIAGRAM

The output of A3B is fed to another latch A3C and A3D. Since the operation of the latch was described previously, only the function of this latch will be discussed. A timing diagram is shown in Figure 13.

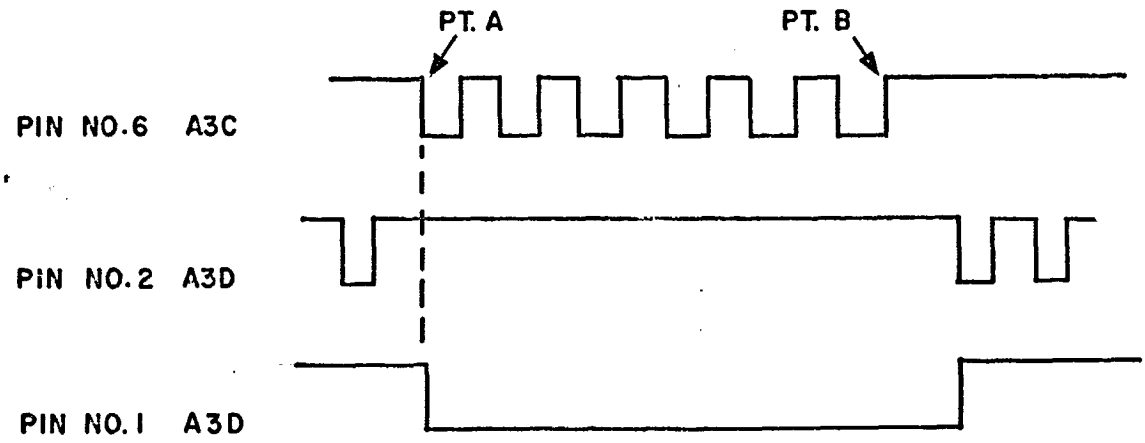


FIGURE 13. TIMING DIAGRAM

The latch block diagram is shown in Figure 14.

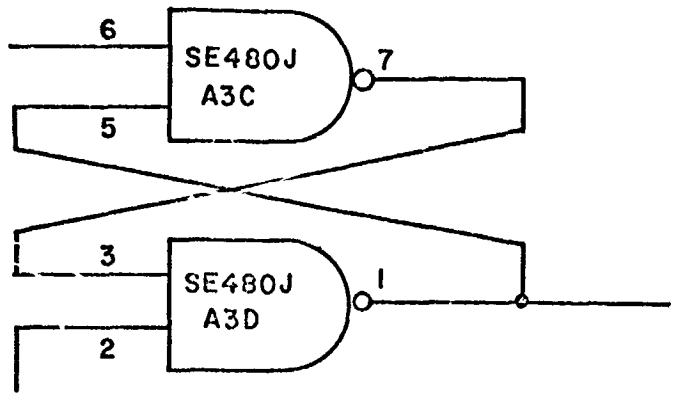
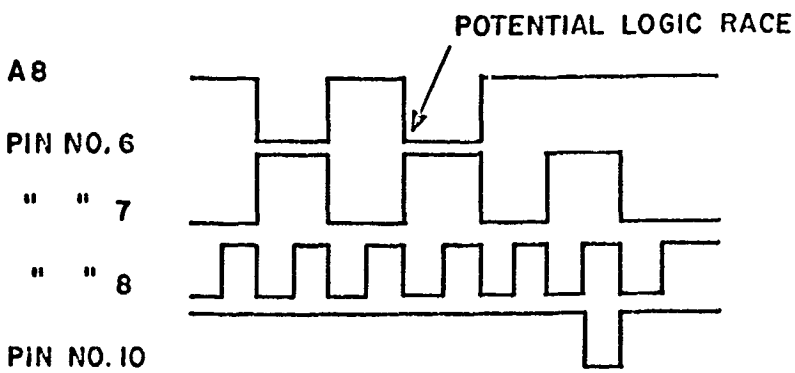


FIGURE 14. LATCH BLOCK DIAGRAM

Point A (Timing Diagram) occurs when the input to the comparator exceeds the ladder network output. Point B occurs when the ladder network output reaches and exceeds the output of the analog input circuit.

Prior to Point A the input to pin #2 (A3D) had been LOW, consequently pin #1 is HIGH. At Point A this output is forced LOW.

Gate A8B is used to reset the A3C-A3D latch when the A-D output latch (A3A-A3B) returns to the high state for more than a half clock period. Capacitor C_{19} is used to slow the rise of the input voltage on A8B to prevent a logic "race" between pin #6 and pin #7 on this gate as shown in the timing diagram below:



It can be seen that pin #10 will go LOW only if pin #6 stays HIGH for a full clock period which is the only case where all inputs are HIGH simultaneously.

The clock circuit is a temperature stabilized, self-starting multivibrator designed to operate at 1000 Hz ±3%. The timing equation for the clock circuit on one side is:

$$Z_{OFF} = R_c \left(\ln \left[\frac{2\,Vcc + Vf - Vbe - Vce}{Vcc + Vf - Vbe} \right] \right)$$

On the side with the diode in the opposite collector, the timing equation is:

$$Z_{OFF} = R_c \left(\ln \left[\frac{2\,Vcc + Vf - Vbe - Vce - Vf\,(CR19)}{Vcc + Vf - Vbe} \right] \right)$$

It can be seen from these equations that temperature variation of Vbe of the transistors is compensated by the diode drop (CR20) which is approximately equal to the Vbe variation. Vf(CR 9) is used to compensate the difference between Vbe and Vf variation and the variation of Vce. This latter diode also provides squaring of the output. Using NPO type capacitors, the variation due to capacity is limited to $\leq \pm 1\%$ from $-55^{\circ}C$ to $+125^{\circ}C$. The results thus far have been a variation of less than ±1% of the output frequency from $-55^{\circ}C$ to $+125^{\circ}C$.

The output frequency of the clock is divided by two by flip-flop A14A to obtain the system clock frequency of 500 Hz. This flip-flop also provides two phases (complementary output) for logic implementation. The general operation of the flip-flop is discussed in the logic section; therefore, only information added is that when the "Q" and "$\bar{Q}$" outputs are tied back to the "Sc" and "Rc" input, the output will change with each clock pulse.

A15A is used to buffer the clock flip-flop output to drive the synchronizer input and the clock output to the spatial comparator circuit.

The output of A3D (pin #1) is used to drive another latch A5B-A5C and to control the input gate to the minimum pulse counter. Clock pulses are enabled in the ladder counter through A1A when the pin #8 output of A5B-A5C latch is HIGH. Simultaneously, the pin #4 output provides a negative edge to "clock" the output flip-flop A14B to a "one" state. The Sc

input has been placed in the LOW state just prior to this "clock" by the output of the A3A-A3B latch. The A5B-A5C output will stay latched until the end of the period when it is reset at pin #13 A5C by the program reset pulse. The output of this latch (pin #8-A5B) also enables the polarity switch latches A6A-A6B discussed in the next section.

The input to the minimum pulse counter is inhibited when pin #1 A3D goes low. When the ladder network exceeds the analog input pin #1 A3D goes high allowing the clock to feed the minimum pulse counter through gate A5A.

The Initial Set Circuit assures that the system starts in the proper state. By driving Q_{27} through R_{17} when the first output pulse comes out of A8B, a capacitive spike is produced at A1B pin #6. This negative going spike produces a simulated reset pulse on the output of A15B pin #12 which resets the entire circuit. When Q_{27} is turned on its LOW output latches A5D in the one state until power is removed.

The ladder and period counter is a series of flip-flops connected as described previously. The counter is preset to 2 counts of 135 for threshold condition. A schematic is shown in Figure 15.

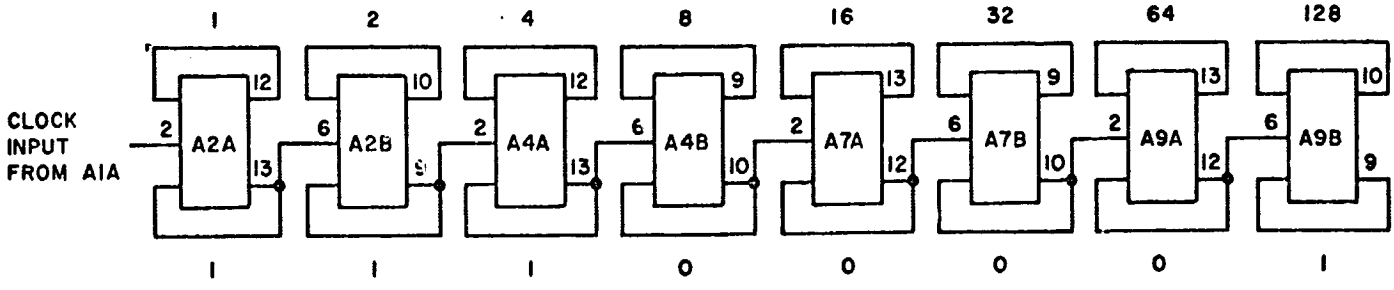


FIGURE 15. COUNTER SCHEMATIC DIAGRAM

The number shown above each flip-flop indicates the number of clock pulses necessary to bring that flip-flop to a "1" state if the counter had all been "0" to start with. By switching the normally "1" and "0" output at selected points, a reset pulse will place each flip-flop in the state indicated below it. Adding up the counts of the flip-flops in the "1" state shows that the counter is designed to be reset into a count of 135.

By "ANDing" the "1" sides of A2A, A2B, A7A, A7B, A9A and A9B through the normal inputs of A10A and the expander A18A, a count of 243 is picked off to produce a reset pulse through a latching gate arrangement of A1B and A15B which is assured of being a half clock period wide. The latch is reset by the clock pulse on A15B pin #2. The circuit reset pulse (output of A15B pin #12) resets the period counter, the minimum pulse counter and the A5B-A5C latch which disables the clock from being fed to the period counter until the circuit resets.

This counter also provides the digital count and the power to produce the output voltage of the ladder network. The ladder network produces a voltage which is linearly proportional to the count in the ladder counter. By scaling the values of the resistors in the ladder network such that the least significant bit is 400 K ohms, the resistor values are reduced by a succeeding factor of 0.5 until the eighth bit drives a 3.125 K ohm resistor. The four most significant resistor value must be accurate within 0.3%. The 26.7 K ohms is used to scale the full-on output to 4.0 V DC.

The voltage reference circuit shown in Figure 16 is used to provide a stable HIGH state voltage that the outputs of the flip-flops are clamped to in the one state to minimize errors due to voltage offsets between bits.

The voltage developed at Point A is determined by Vz(CR 28) which is set at 10 V DC ±1% by using the 1N4104. The voltage at Point B is then a result of $V_A - Vbe_{(Q25)}$ or $V_{z(CR28)} - V_{z(CR24)} + Vbe_{(Q25)}$. The input pins to the T1XD22 diode array pins #2-#9 since they are on a monolithic chip and the Vf are fairly well matched result in a voltage of $V_{z(CR28)} - V_{z(CR29)} + Vbe_{(Q25)} + V_f$ or

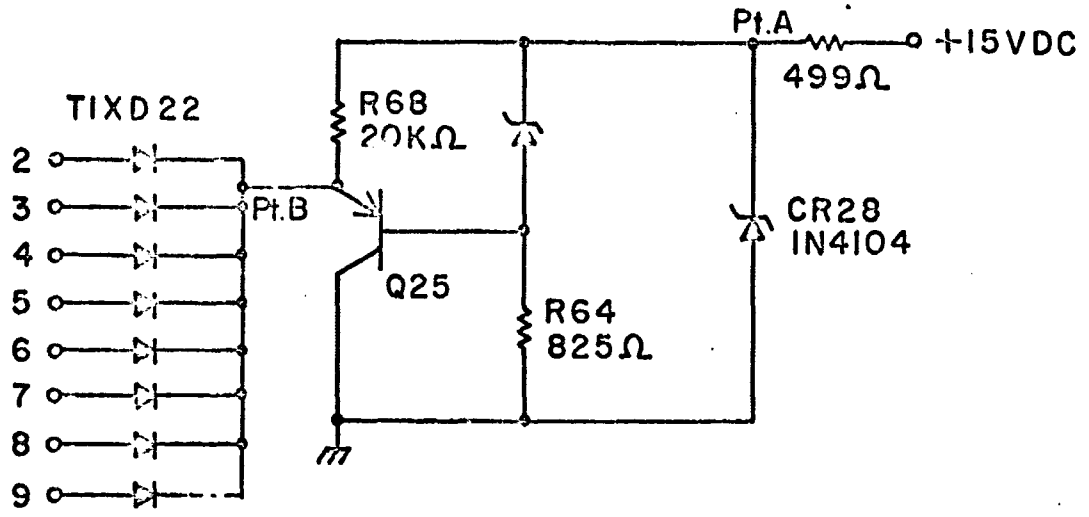


FIGURE 16. VOLTAGE REFERENCE CIRCUIT

10 V - 6.8 + 0.6 + 0.6 = 4.4 V DC when their connecting flip-flop is in the high state. The variation over temperature of V_0 points is 25 follows

$$V_{z(CR28)} - V_{z(CR24)} + V_{be(Q25)} + V_f$$

$$+.0006\,(10.0)/^{o}C - .00035(6.8)/^{o}C + (-2.2\ MV/^{o}C) + (-1.8\ MV/^{o}C)$$

$$+6.0\ MV/^{o}C - 2.38(6.8)/^{o}C - 2.2\ MV/^{o}C - 1.8\ MV/^{o}C = 3.8\ MV/^{o}C$$

The resulting temperature variation should then be -38 MV to +30 MV from +125°C to -55°C. The effect of even this small variation is further reduced by scaling by voltage division.

The Minimum Pulse Counter is a ripple type counter of the same type as the ladder counter. The Q outputs on this counter, however, are used as the one output such that when the Rd input on each bit is brought low, each bit in the counter is pulled to a "0" state. The clock to this counter is driven by A5A gate which is enabled when the ladder

voltage exceeds the analog output voltage. This gate is enabled when A3D pin #14 returns to the HIGH state. An "AND" gate A8A expanded by A18B is used to pick off a count of 32 which with a 500 Hz clock is being used results in a delay of 2 msec times 32 counts or 64 msec. The output of A8A (pin #12) is used to reset the output flip-flop A14B to the "0" state. Since this is the only way to reset A14B the 64 msec is always interposed in turning the output off. By changing the ANDing count in A8A-A18A different minimum pulse widths can be set.

The Polarity Selection Gates and latches are shown schematically in Figure 17.

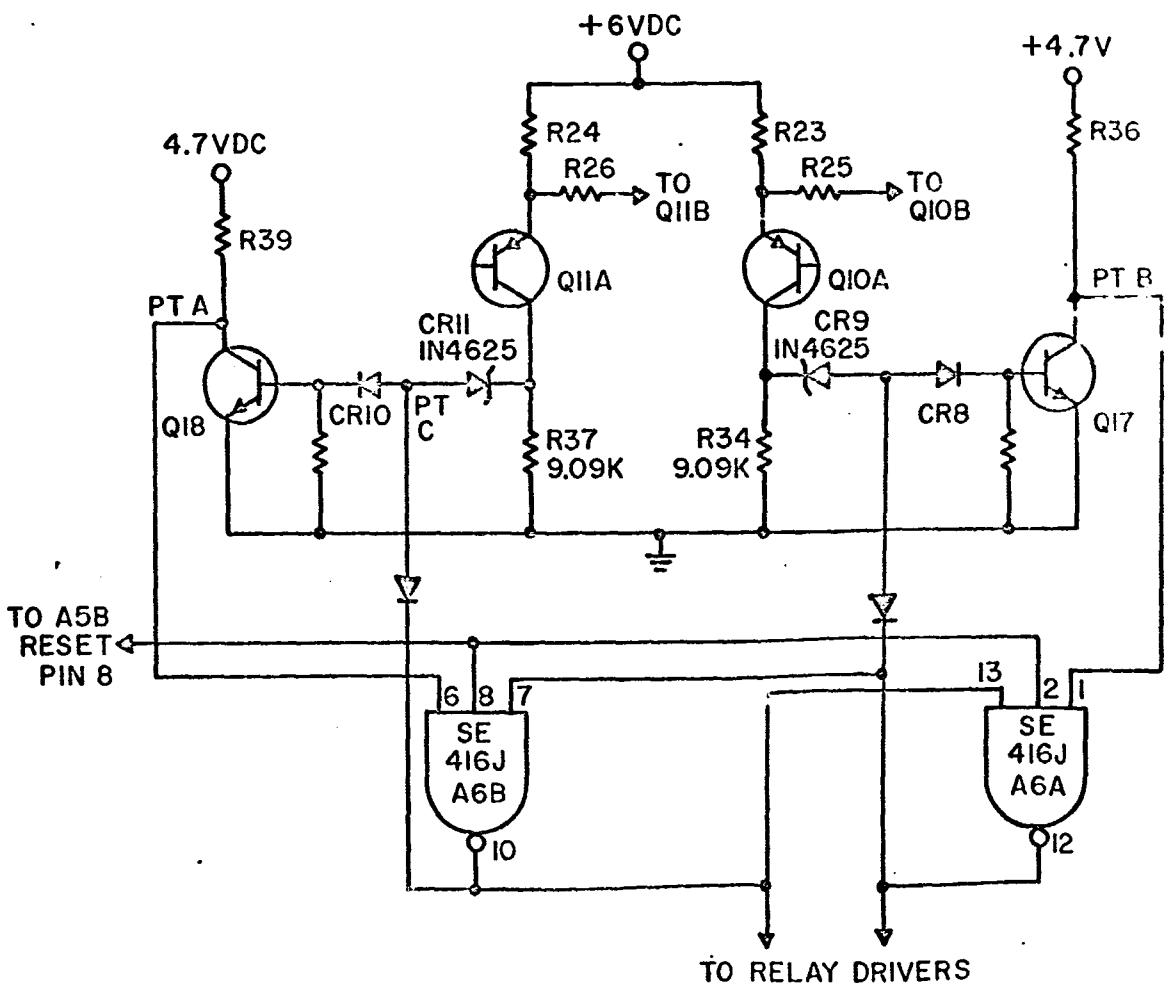


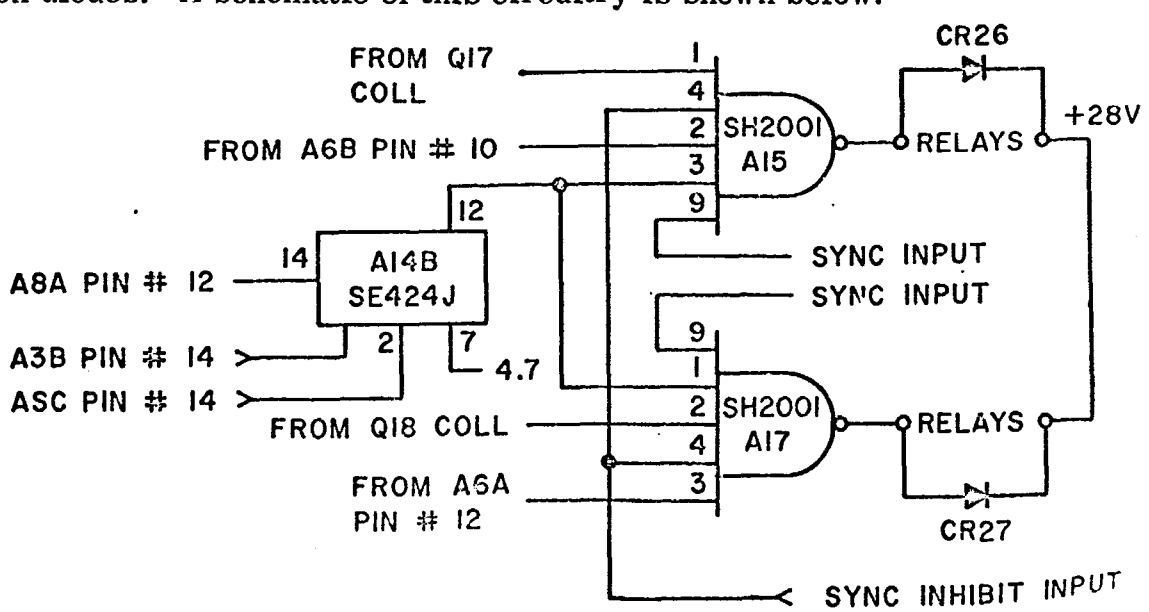
FIGURE 17. GATES AND LATCHES SCHEMATIC DIAGRAM

The current in the collectors of Q_{11A} and Q_{10A} which are part of the differential-to-single-ended converter determines which polarity gate will switch. When the voltage on Q_{11A} emitter is greater than that on the emitter of Q_{10A}, the current in R_{24} is reduced because of less voltage drop. The current in Q_{11} collector is further reduced by the current drain in R_{25}. In the quiescent state the collector current in Q_{11A} is sufficient to develop enough voltage across R_{37} to forward bias CR_{11} and turn on Q_{18}. The same holds true for CR_9 and Q_{17}. When the collector current in Q_{11A} is reduced, the voltage across R_{37} drops and reverse biases CR_{11}. As a result Q_{18} is turned off and Pt A rises to 4.7 V DC. Q_{17} is still biased on since I_c Q_{10A} has increased.

When the output from A5B is high, A6B pin #10 is "low." This pulls Pt C low and holds it until the reset pulse on A5B pin #8 releases it. This is to assure the output will not be pulled down during the cycle by a change in input polarity. The output of A6B (pin #10) is also connected to an input on A6A which holds this gate output high until the end of the period. The output of A6B is also fed to the opposite polarity relay driver to prevent it from coming on during the cycle and having both polarity outputs on simultaneously.

The same logic applies to the opposite polarity on Q_{11A} and Q_{18} with regard to the other polarity gate Q_{17} and A6A.

The Output Circuitry consists of the relay drivers, the output flip-flop and the relay suppression diodes. A schematic of this circuitry is shown below:



The output flip-flop controls the state of the output of the spatial amplifier. The operation of this device was discussed previously. If the output pin #12 is in the high state either A16 or A17 will be enabled, depending on whether the output of Q_{17} or Q_{18} is HIGH. When all the inputs to A_{16} or A_{17} are HIGH, the output at pin #8 will go LOW pulling currents through the relays in that bank from the +28 volt source. When any one of the inputs goes LOW, the output turns off and the reverse inductive current is shunted through the suppression diode CR_{26} or CR_{27}. When the polarity gate input to one of these drivers is high, the polarity latch input to the other is low preventing both from being "on" simultaneously.

The Sync Inputs and the Sync Inhibit Inputs are used only when the spatial sync circuit is being used. A low input is put on the Sync Inhibit input and the Sync Input is then controlled by the spatial sync circuit. The output of the relay driver will turn "on" when the sync input is pulled LOW.

The Synchrogram is shown in Figure 18. A list of the points shown and their schematic counterpart is given below.

Point A	A15A Pin #10
Point B	Base Q14B
Point C	A15B Pin #12
Point D	Any mag amp input
Point E	A16 Pin #1
Point F	A3D Pin #1
Point G	A5A Pin #1
Point H	A5B Pin #8
Point I	A8A Pin #12
Point J	A14B Pin #12
Point K	A17 Pin #2
Point L	A16 Pin #8

An input of median range of 265 μA is shown and can be followed to show how the output width is produced.

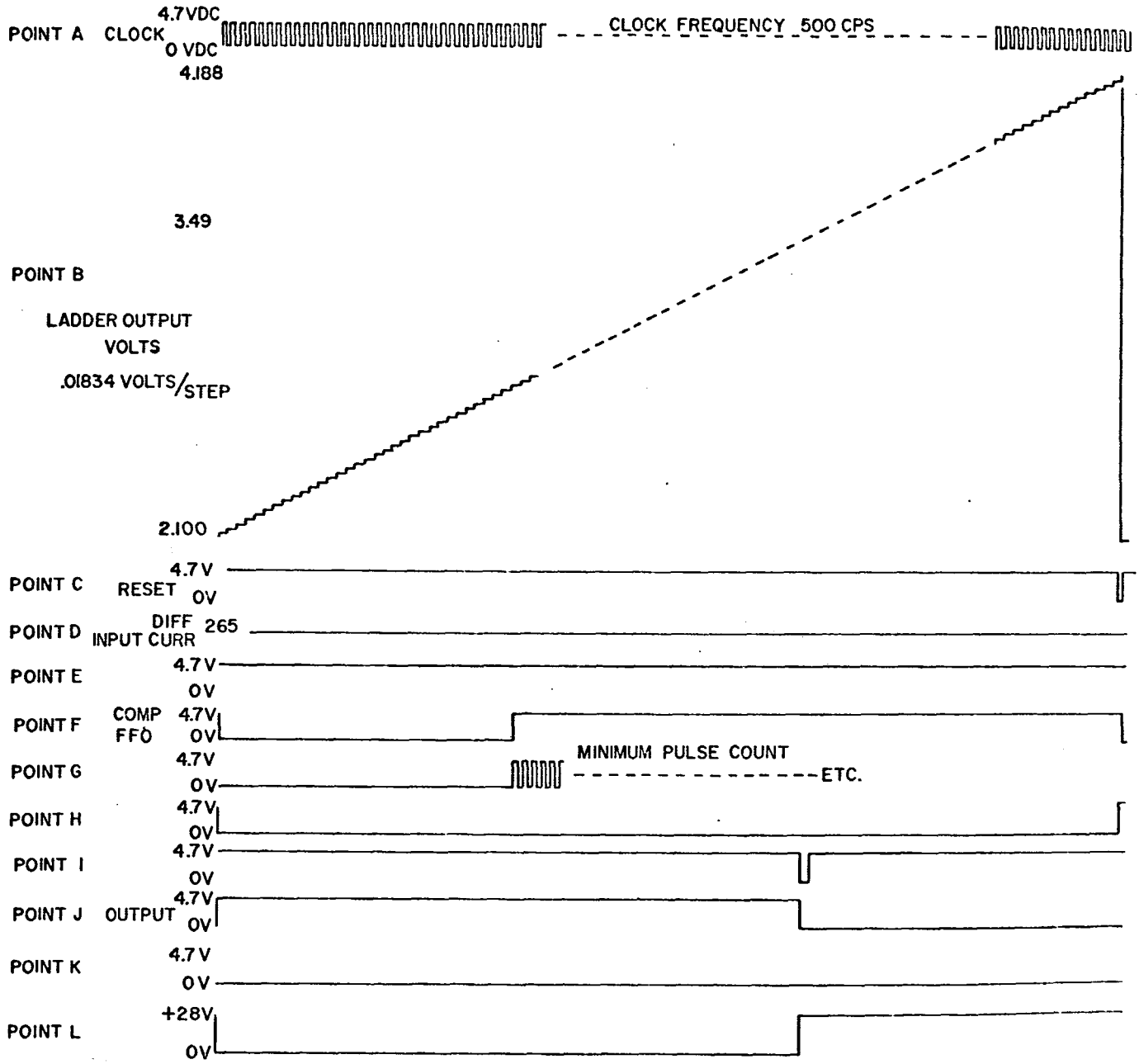


FIGURE 18. SYNCHROGRAM

SWITCHING LOGIC

The switching logic is the controlling circuitry for all relay switching in the computer. The logic can be separated into four sections as shown in Figure 3-19.

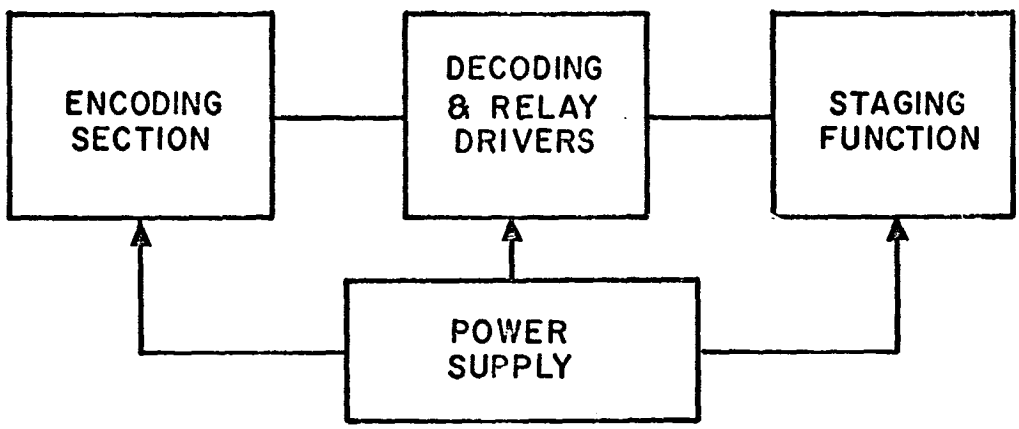


FIGURE 19. SWITCHING LOGIC

The encoding section is made up of four identical circuits. A typical encoding circuit is shown in Figure 20.

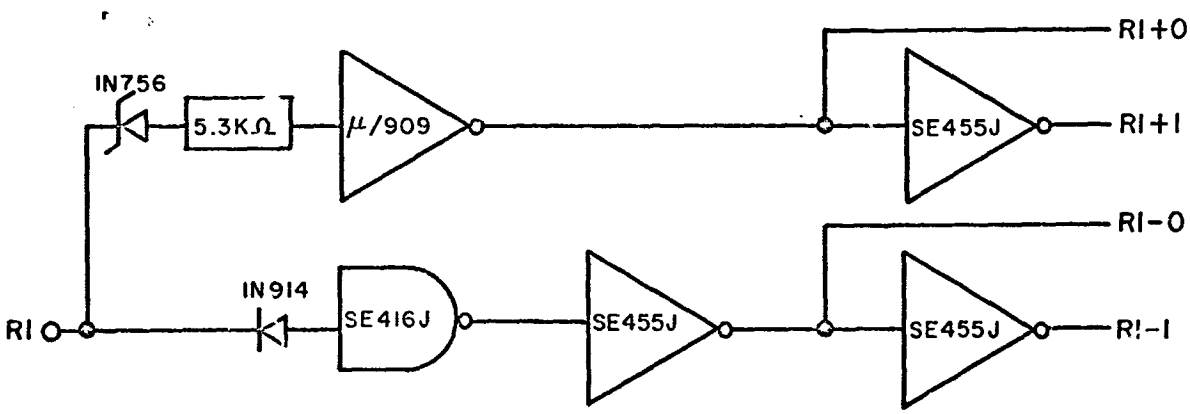


FIGURE 20. ENCODING CIRCUIT

The significant feature of this circuit is its ability to discriminate between a +28 V DC, 0 V DC and an open input condition. The two gates that perform this function are the SE 416J and the μL 909.

Since the SE 416J dual four input expandable gate was discussed in detail in the basic logic section just a few significant facts will be mentioned about its application here. Due to the expandable input an external higher voltage diode can be placed in series with the expandable input to boost the input maximum voltage rating on the gate from +8 V DC to +50 V DC. A truth table for the SE 416J is shown below, along with that of the μL909.

		Outputs	
State	Symbol	SE416J	μL909
+28 V DC	+	Low	Low
0 V DC	-	High	High
Open	0	Low	High

Note that the outputs of the two gates are opposite with an open input state. The μL 909 functions in the dual role of decoding the difference between a +28 V DC and an open input and being a buffer driver circuit. The schematic of this circuit shows an RTL type input using a leakage resistor to turn the input stage off when drive current is removed from the input. The resulting output states for the various inputs is shown in the truth table above.

Since the truth table above shows the transfer function of the input section the full transfer characteristics of this circuit are shown in the truth table below:

Inputs	Outputs			
R1	R1+1	R1+0	R1-1	R1-0
+28 V DC	High	Low	Low	High
Open	Low	High	Low	High
0 V DC	Low	High	High	Low

The circuit was designed in this manner to allow the use of codes used in previous computers and still gain the advantage of using off-the-shelf type monolithic integrated circuits that are commercially readily available.

The other three encoding section inputs and respective outputs are listed below:

Inputs	Outputs
R2	R2+0, R2+1, R2-0, R2-1
R3	R3+0, R3+1, R3-0, R3-1
R4	R4+0, R4+1, R4-0, R4-1

The codes are used with either the +28 V DC inputs and the open inputs or the 0 V DC inputs and the open inputs. When it is desired to use a +28 V DC input to decode a relay bank an encoding output such as R1+1 would be used. An open input to the encoding section used with other inputs involving +28 V DC inputs would be decoded with an output such as R1+0. If it is then desired to enable a companion code the previously "open" encoding inputs could be switched to 0 V DC to encode the second relay bank while maintaining the enable on the initial code. Examples of companion codes are shown in the following list.

1st Code	2nd Code	Dual Code
+0+0	0-0-	+-+-
+000	0---	+---
0++0	-00-	-++-

The result would be that one relay bank would be decoded for the first code, a second for the second code, and both banks would decode the dual code.

The second section is the decoding and relay drivers. The decoding is accomplished using four input "AND" gates type SH 2001, previously discussed in the basic logic section. A typical pair of relay banks and associated drivers are shown in Figure 21.

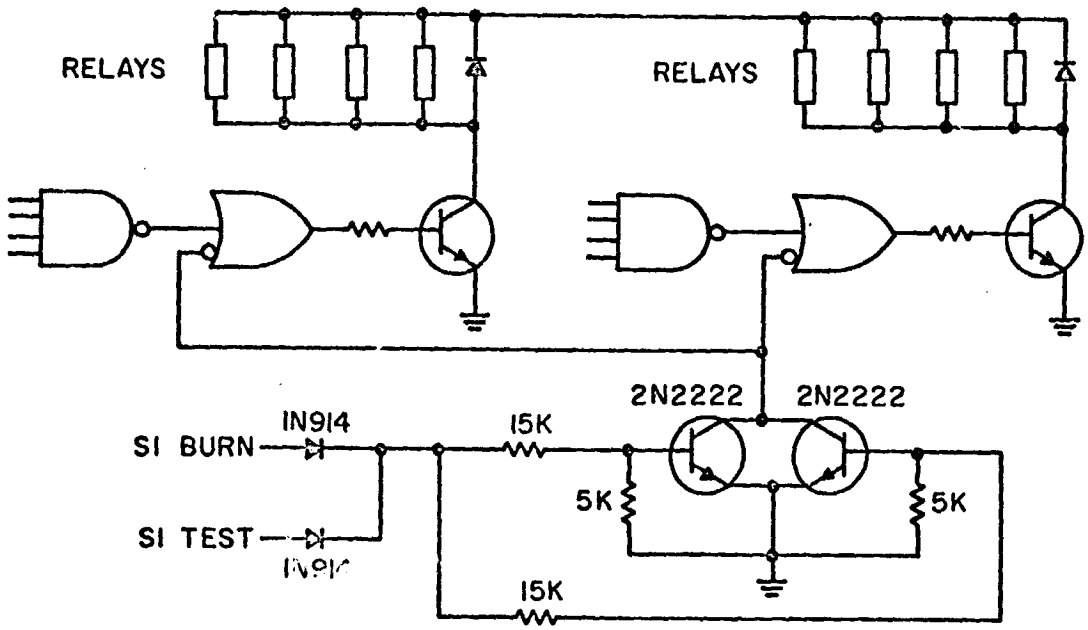


FIGURE 21. RELAY BANKS AND ASSOCIATED DRIVERS

In order to decode all possible functions it is necessary to bring a sixteen encoding output on any board and it is therefore most efficient to place a large number of relay drivers on a single board. A potential of 32 separate codes are available. Since this allows only 8 potential SH 2001 fan-out boards on any driver a single SE 455J is sufficient for each encoding output.

The staging functions are accomplished by connecting the output of a RTL type transistor pulse inverter type circuit (shown in Figure 22) to all relay driver "OR" inputs that require switching at a particular staging time.

The power supply section actually represents two redundant regulated inverter power supplies. The operational details of this type power supply is discussed in the power supply section. The power supplies are used according to the relay contact redundancy scheme (i.e., when contacts are redundant the relay drivers operating these contacts are powered by separate supplies). The voltage available on the output of the supplies is +4.7 V DC ±10%.

Several alternate approaches to the mechanical relay switching are available. The most feasible of the approaches studied are solid state relays developed at ECI for this purpose. The schematic for a single-pole-double-throw solid state relay is shown in Figure 22.

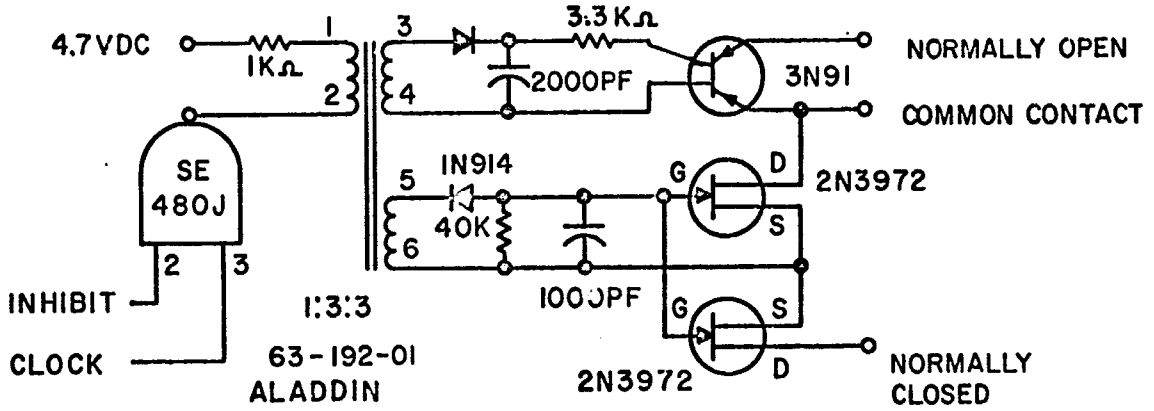


FIGURE 22. PULSE INVERTER CIRCUIT

This relay operates without mechanical movement and at extremely low power levels. It is designed to switch signal currents of 1 ma or less with the maximum channel voltage gradient of 30 volts. Applications in excess of either of the requirements would be switched using the mechanical relay-integrated circuit driver previously discussed.

When the inhibit input shown is placed in the high state the clock input controls the SE 480J gate output. The 155 kHz rectangular wave appears on the primary of the pulse transformer with an amplitude of approximately 2.0 volts. A DC level of $\geq$3.3 volts is generated after half wave rectification, on the secondary windings of the pulse transformer. This output provides turn-on bias for the dual-emitter chopper (3N91) and pinch-off voltage for the FET's (2N3972). When this clock signal is inhibited by a low state on the inhibit inputs the drive for the 3N91 is removed, hence the output circuit switches to the open mode. Since without power being applied the gate to source voltage on the FET's is reduced to zero volts the drain to drain circuit is "closed." The "on" resistance of the FET's is spec-

ified at 100 ohms maximum and is typically found to be approximately 60 ohms. The dual emitter chopper "on" resistance is specified at 100 ohms maximum and is typically found to be approximately 75 ohms.

The current in the primary winding is found to be 2.5 ma ±.5 ma in the "on" state with a 50% duty cycle. The primary power can then be shown to be 3.0×10^{-3} (.5) (4.7) w or 7.05 mw. Add to this the maximum power developed by the SE 480J gate which is 7 mw and the total power per single pole double throw function is shown to be 14 mw. Some additional power must be added to account for the power consumed in providing a clock output and logic power levels, but when this amortized over all the switching functions it is nearly negligible. Comparatively to provide a double pole double throw switching function using the low current GE grid 150 relay the following list indicates the power consumed in this switching approach.

	Type	Power	
Relay	GE Grid 150	22 ma at 28 V DC	= 617 mw
Driver	SH 2001	Assuming an average of three relays per driver	= 40 mw
		TOTAL	657 mw

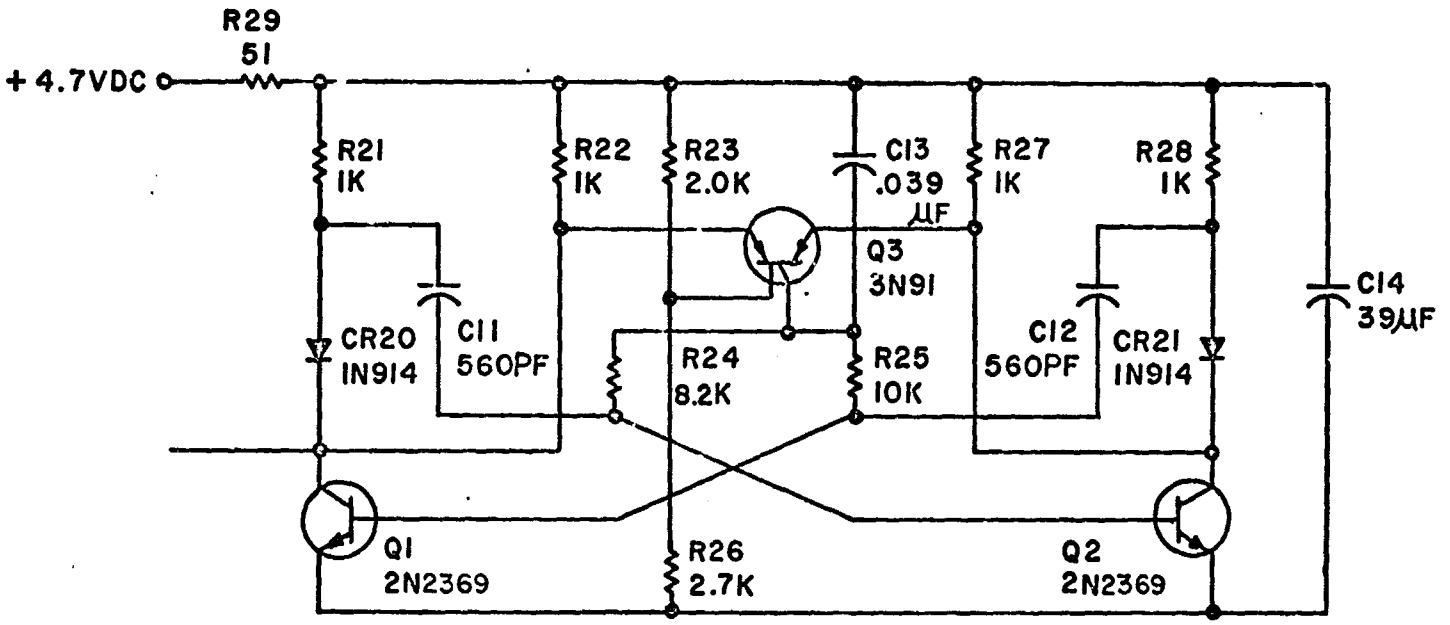
Reducing this to a single pole double throw configuration the power per function becomes 328 mw per function which is a conservative estimate since maximum values are not used for the relay current. The solid state relay shows a 42.8 to 1 power advantage over mechanical switching.

Due to the need for a pulse transformer the physical size of the solid state relay will be slightly larger than that of the mechanical relay.

The reliability advantage is inherently better with the solid state device due to the lack of necessity for mechanical movement. The solid state approach also eliminates contact bounce and RFI generated inductively by opening of the relay coils.

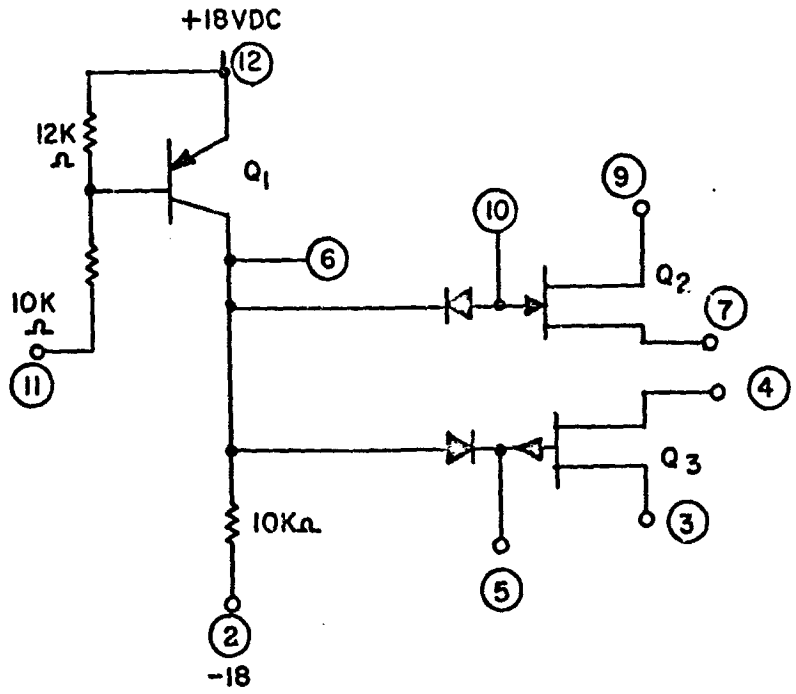
Some disadvantages are that some digital noise is generated in the channel being switched through the inter-electrode capacity by the transformer driving signal. This is in the form of spikes with very fast edges ($t_r \approx 10$ ns) which due to the low frequency nature of the computer signals is generally reduced to negligible levels by filtering.

The clock circuit needed to develop the 155 kHz driving frequency for the solid state relay is shown below.

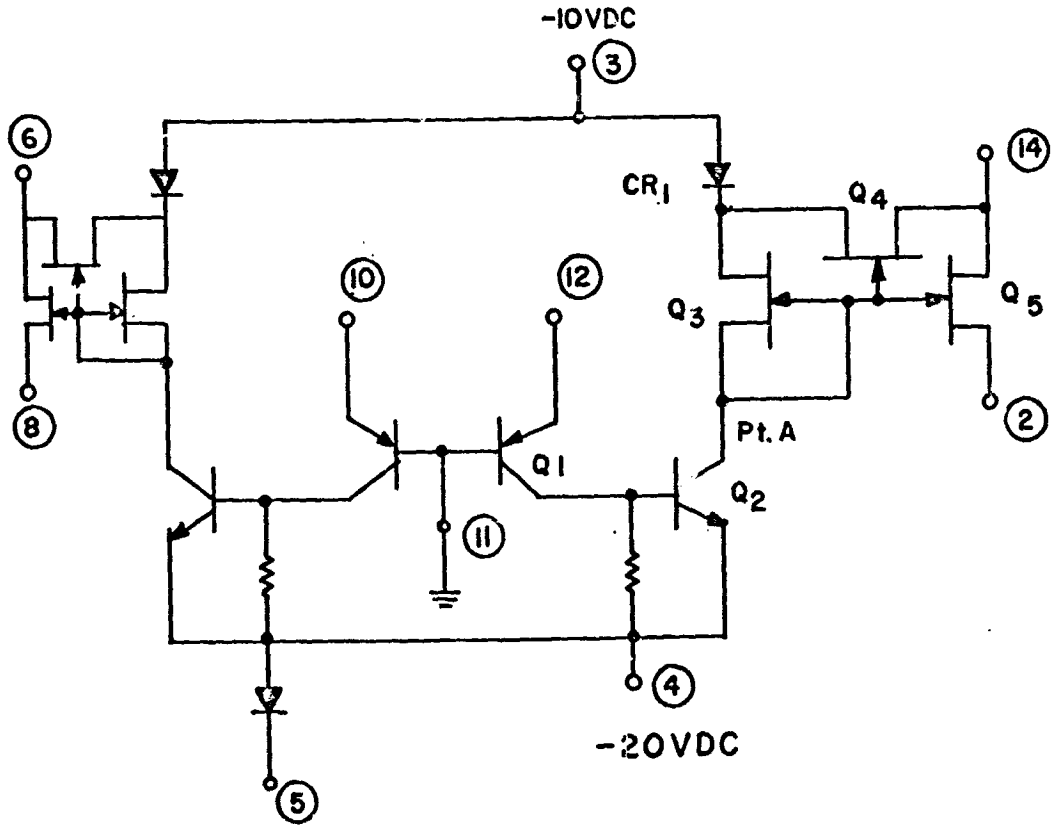


The clock circuit is a self starting temperature compensated multivibrator. Since most of the circuit is typical of multivibrator design only the unique self-starting feature will be discussed. By referencing the base of the dual emitter transistor to a voltage division of 0.575 V DC and supplying the base current for the switching transistor through the collector circuit a "lock up" condition is prevented. This is due to the fact that if both switching transistors turn on simultaneously both emitters of Q3 will be reversed biased shutting off collector current. Since this is also base current for the switching transistors both devices will turn off removing the locked-up state.

Two commercially produced analog gates were investigated for application here. These are the Siliconix DG104F and the Amelco E16-518A. Schematics of both are shown below.



AMELCO E16-518A



SILICONIX DG104F

The Amelco E16-518A operates by providing pinch-off voltage to one of the two FET's in each state. When the input switch is turned on the FET common point (pin #6) is connected to +18 volts through the saturated transistor. The P channel FET Q3 is therefore pinched-off. The FET pinch-off voltage for both transistors is specified at 7 volts. When Q1 is turned off pin #6 is pulled to -18 V DC through the 10 K ohm and Q2 is pinched-off. By connecting the two sources together a single pole double throw capability is developed. The diodes in the gate circuits of the FET's are used to isolate the channel when the polarity would be such to forward bias the gate to drain or gate to source junction.

Several problems and limitations of this design come to light upon applying it. First, isolation of the channel from the logic levels is poor. In order to pinch off the FET transistors it is necessary to externally reference the channel to logic ground. If this is done through very high impedances noise greatly affects the operation of the device. Furthermore, the channel level must stay within a very limited voltage range of the logic ground in order to assure proper pinch-off conditions. Since the voltage supply range is limited to ±20 V DC and the specified pinch-off of the devices is + or -7 volts the maximum channel swing is limited to + or -13 volts around logic ground. This is compounded by the first limitation discussed such that application of greater than ±10 volts would be foolish.

The power consumption of this device in the "on" condition (Q1 on) is 200 mw which is 14 times as great as that of the ECI version. The TO-8 can it is packaged in makes slightly smaller than the ECI device but larger than the GO Gnd 150.

Another limitation is that when Q1 is turned off pin #6 is pulled down through a 10K ohm resistor, hence the fall time is slow. Consequently, the gate diode in the Q3 circuit blocks most of the charge from being removed from the gate input of Q3 and the turn-on delay of the transistor is in the order of several tenths of a second.

The Siliconix DG 104F requires a complementary input to provide a single pole double throw configuration. Since both sides are identical only one will be discussed. When Q1 is turned on, providing base current for Q2, Point A is pulled to -20 VDC, pinching off Q5. (Pinch-off voltage specified at -3 volts.) Pin #14 is referenced to -10 V DC through Q4 which acts as a variable impedance. The current in Q2 is limited through the constant current source Q3. When Q2 is switched off Point A rises to -10 V DC and Q5 is turned on by V_{GS} being returned to zero. By connecting opposite sides together source to drain and providing complementary inputs a SPDT function is generated. Another Siliconix gate is being produced which will eliminate the need for the complementary input.

This device exhibits a lot of advantages: small size (1/4" x 1/8" flat pack); low power (approximately 60 mw); fast switching speeds (<1 μs); low "on" resistance (<100 ohm) and no need for external biasing.

The disadvantages are: the device is still in the early stages of development and little data is available and the channel voltage swing is limited to ±7 volts around the -10 V DC logic level. This last limitation is due to the fact that the output channel is referenced to -10 V DC through Q4 or its complement.

The ECI version is therefore considered a better choice at this time, because it does not require the output channel to stay within the limited voltage range of the logic levels due to the fact that it is self-biasing through the pulse transformer. The power consumed is also the lowest of all considered. The only areas where the Siliconix gate is superior are the smaller packaging, and faster switching capabilities. The Siliconix and Amelco gates both require voltage levels other than the normal logic level of 4.7 V DC while the ECI relay does not.

A typical relay bank using the ECI solid state relay is shown in Figure 23. This configuration represents a four-pole-double-throw relay.

Using two identical clock circuits a redundancy scheme similar to that of the power supplies is employed.

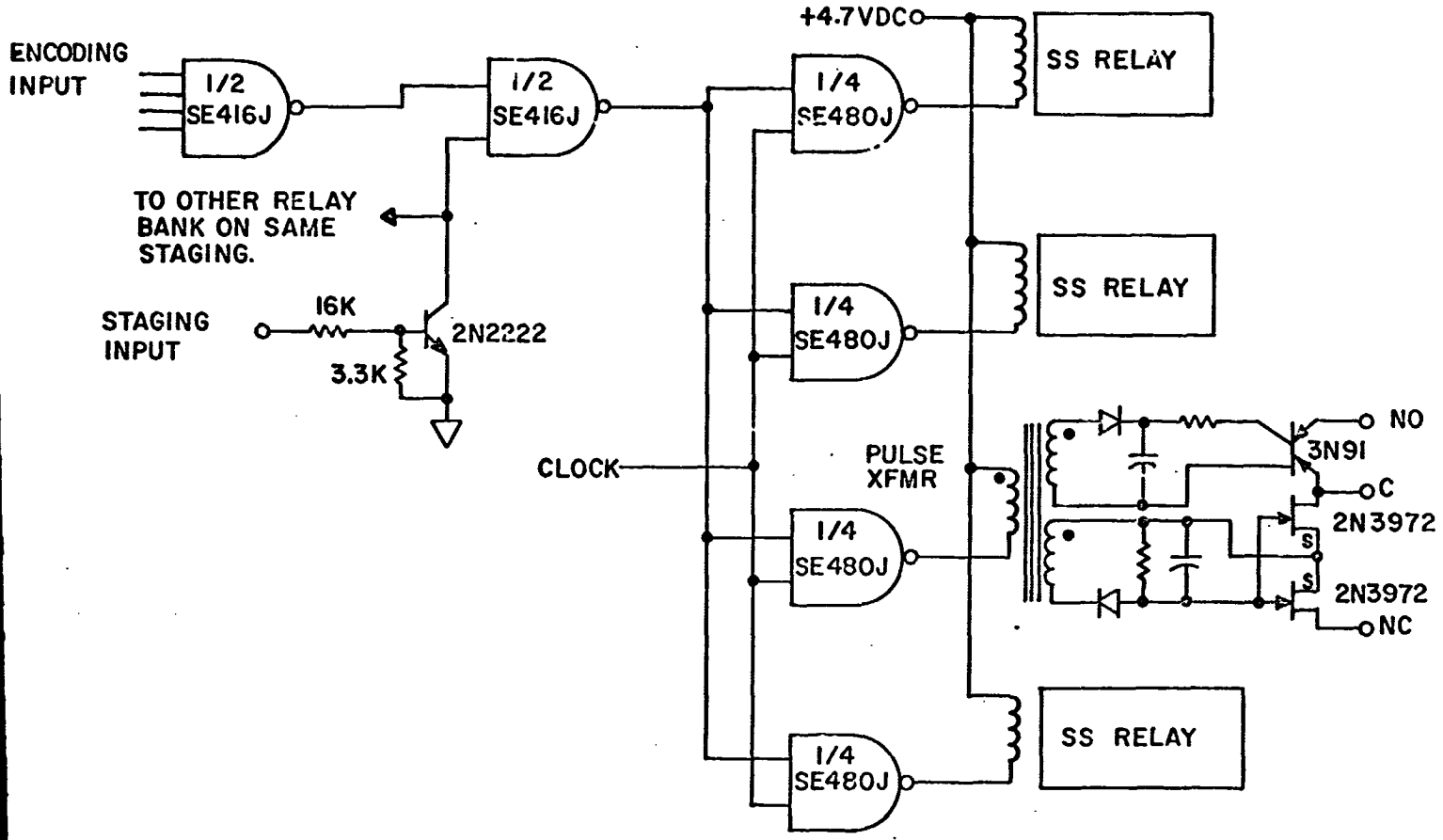
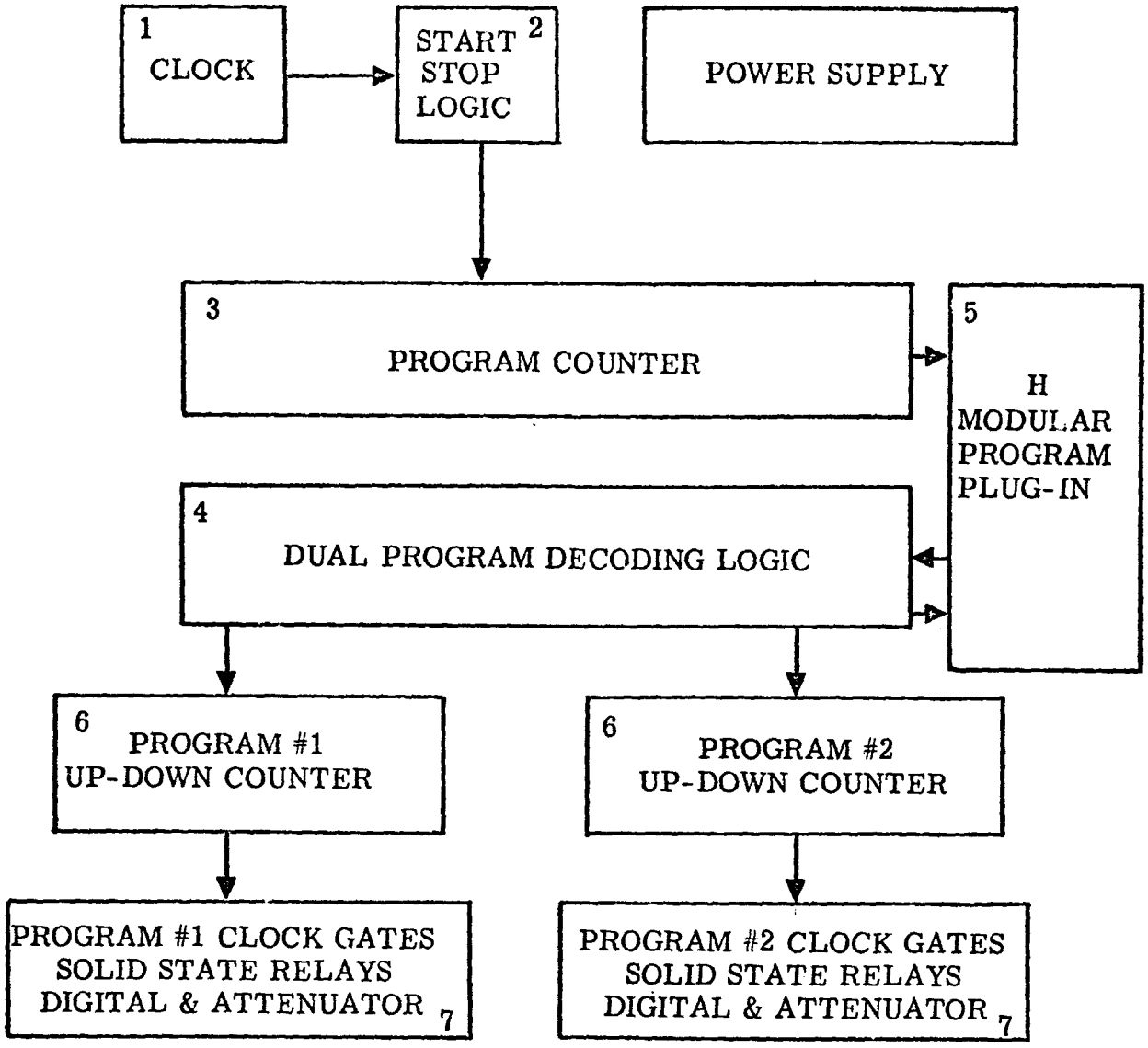


FIGURE 23. TYPICAL RELAY BANK

Solid State C.A.T.

The solid state control attenuator timer is composed almost entirely of digital flat packs. (See block diagram on following page.) The first section is the clock circuit (Figure 24) and is the same circuit that is used in the digital spatial amplifier, with minor modifications.



An analysis of the temperature compensation features of the circuit were discussed in detail in that section. The self-starting feature will be discussed here.

In some multivibrator designs a lock-up condition occurs when both transistors go into the "on" condition at the same time. This circuit prevents this condition because when both the collectors of Q31 and Q32 are low the base current for Q29 is cut off due to CR34 and CR35 both being in the "on" condition. This results in the current in R54 being

cut off and therefore, the base current for Q31 and Q32 is shut off. Both collectors are released and the "lock-up" condition is removed. The only differences between this circuit and that of the one in the spatial amplifier are that 2N930 transistors are used instead of 2N2222's and the R-C values for timing are different to generate the 128 Hz ±3% frequency.

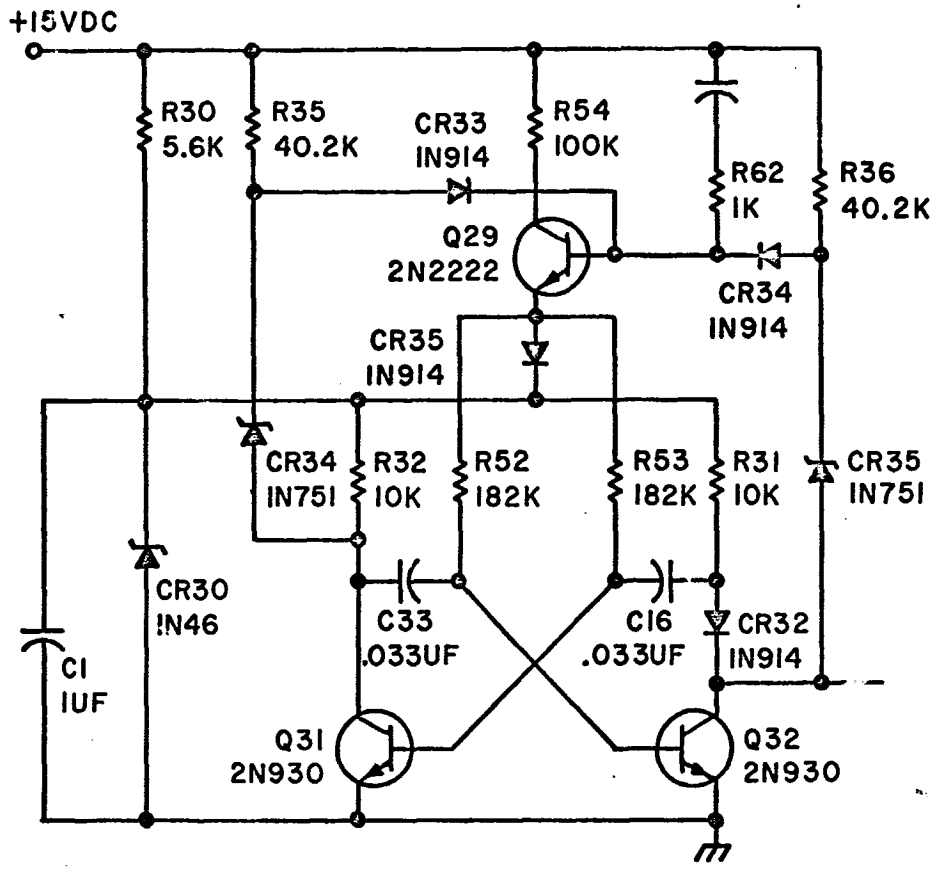


FIGURE 24. CLOCK CIRCUITS

The start-stop logic consists of the first motion input circuit, the interrupt input, the CAT zero circuit and the initial set circuit. The schematic for the first motion circuit is shown in Figure 25.

When a +28 V DC input is applied to the input, Q33 is turned "on." K1 relay turns "on" and the latch contact K1B closes. The first motion input can now be removed and the circuit will hold "on." K1A contact opens when K1 relay turns on. This releases pin #8, A1A which is pulled high by R66. Since LPFO is HIGH, the clock is enabled through A allowing it to be fed to the program counter.

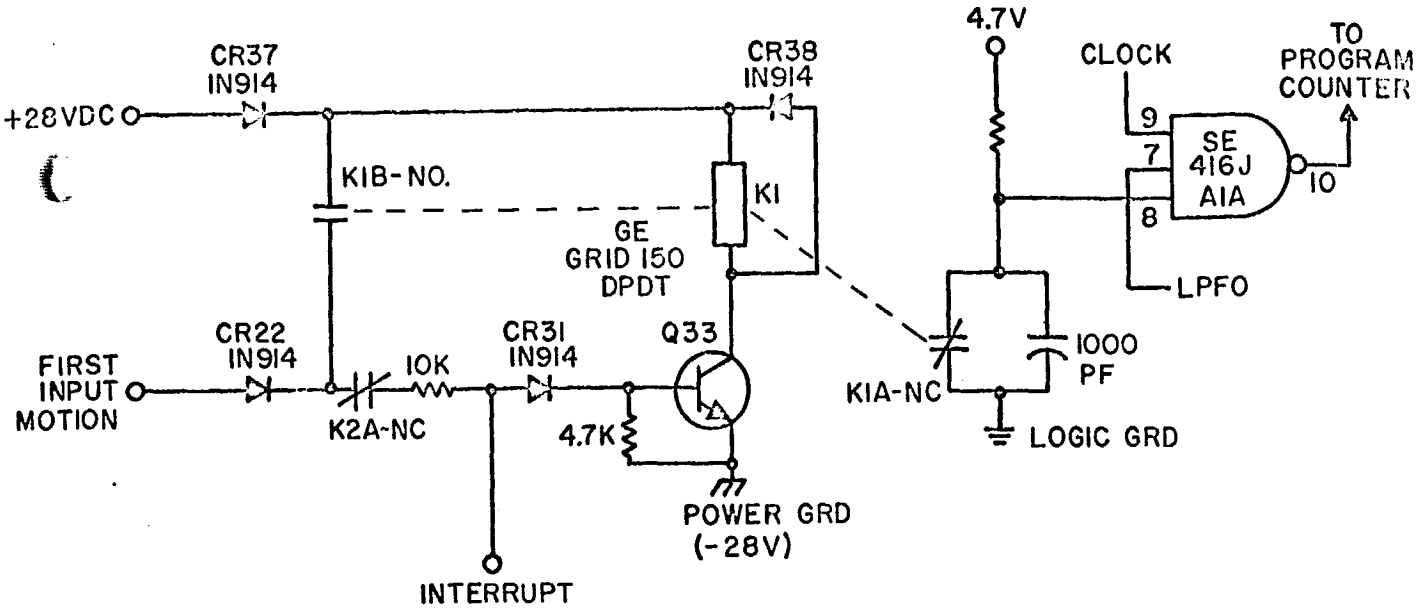


FIGURE 25. FIRST MOTION CIRCUIT

The interrupt input when brought to ground interrupts the base current in Q33 which turns off K1. K1A then closes and inhibits A1A, thus shutting off the clock pulses to the program counter. When the program counter stops counting, both programs will hold indefinitely in the state at which they were interrupted, as long as power is present.

The initial set circuit is designed to produce a system reset pulse when power is turned on regardless of the speed with which power is applied. The schematic is shown in Figure 26.

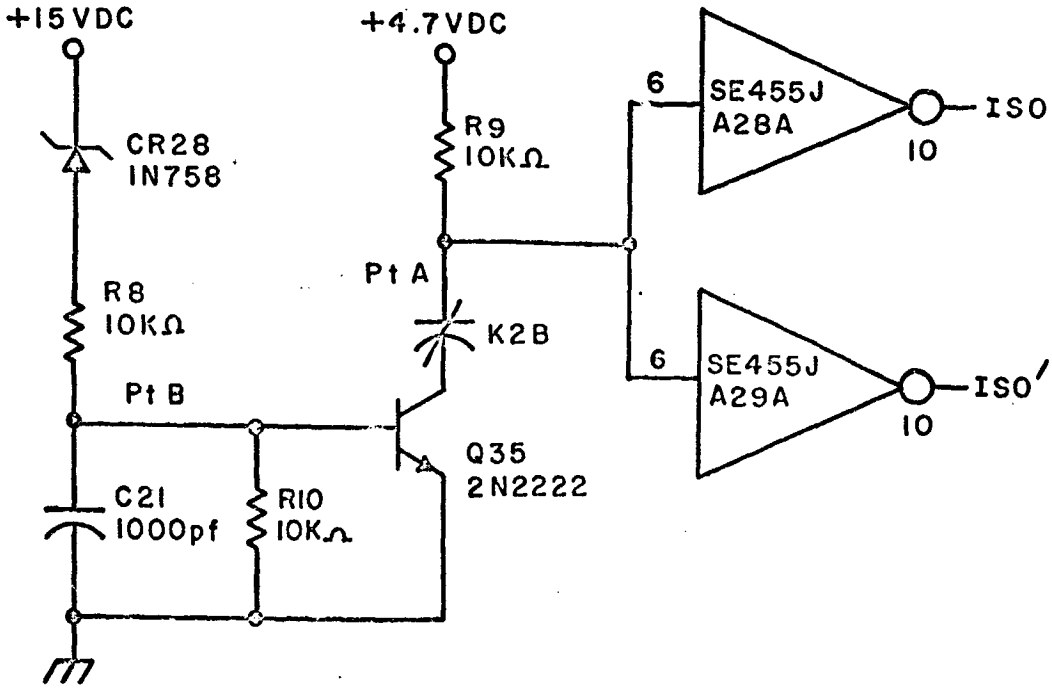


FIGURE 26. INITIAL SET CIRCUIT

When power is applied, both the +15 V DC and +4.7 V DC supplies start rising. If the rise is slow, the voltage at Point A will rise sooner than that at Point B because the CR28 zener diode will not be forward biased until nearly +15V DC is reached. Consequently, the outputs A29A - pin #10 (ISO) and A29A - pin #10 (ISO') are forced "low." This resets the entire circuit. When the voltage at Point B rises and turns "on" Q35, Point A is pulled "low" and the outputs ISO and ISO' are forced "high", which removes the reset condition allowing the circuits to function. This state will hold as long as power is present and this circuit is essentially not used again unless the C. A. T. zero input is activated.

If the power rises rapidly, Point B will still rise more slowly than Point A due to the time constant imposed on the voltage rise at Point B by R8 and C21.

The C. A. T. zero circuit consists of relay K2 with one side of the coil tied to -28 V, and the other side of the coil used as a +28 V DC input. The coil is by-passed by a suppression diode. One contact, K1A-NC (normally closed), opens when C. A. T. zero is activated and interrupts the base current in Q33 both from the first motion input and the latching contact (K1B) as shown in Figure 25. The other contact, K2B, opens the collector circuit of Q35 as shown in Figure 26, when the C. A. T. zero input is energized. This allows Point A to rise, forcing the ISO and ISO' outputs "low" and resets the entire circuit. Before the circuit will start again, the first motion input must be energized.

The program counter is the basic source of timing and frequencies for both programs. It consists of a series of fifteen flip-flops (SE 424's) connected in a ripple counter arrangement similar to that of the minimum pulse counter used in the spatial amplifier. The counter can sum a total count of 32,768 which represents 256 seconds using the 128 Hz clock. The time it takes when the clock initially is fed to the counter for the last eight bits to reach the "1" state is as follows.

PC 071	1 second
PC 081	2 seconds
PC 091	4 seconds
PC 101	8 seconds
PC 111	16 seconds
PC 121	32 seconds
PC 131	64 seconds
PC 141	128 seconds

By "ANDing" any of these outputs together, program transitions can be made to occur at any preselected time. For instance, if it is desired that a logic function occur 30 seconds after the program starts, PC 081 (2 seconds), PC 091 (4 seconds), PC 101 (8 seconds), and PC 111 (16 seconds) can be "ANDed" to produce a cumulative total of 30 seconds. When the outputs are fed through a multiple input "NAND" gate (SE 416J), a LOW condition will occur on the output of the device which can be used to initiate a desired logic operation.

Since each flip-flop divides its input frequency by two, any frequency which is a binary division of 128 Hz down to 0.003945 Hz can be obtained. If other frequencies are necessary, use of a divide-by-three or divide-by-five counter placed on the modular program plug-in board can be employed to further divide any of the available frequencies.

The program counter outputs are arranged so that the reset pulse places all bits in the counter in the "0" state.

The dual program decoding logic is the means by which the transition points and frequencies picked off the program counter are converted to the proper signals to be fed to the program up-down counters. The three basic logic arrangements in this section are the frequency transition gate, the hold gate and the program finish gate. The frequency transition gate is shown schematically in Figure 27.

By "ANDing" PC 081, PC 091, PC 101 and PC 111 into the inputs on A61A the output at pin #12 will go to the LOW state 30 seconds after the program starts, and A21A pin #14 will go HIGH. This forces A21C, pin #7 LOW, which in turn is fed back to pin #13 of A21A. This LOW input latches A21A's output HIGH even if the input on pin #12 changes. The result is that A21A, pin #14 is latched high and enables A61B and A21D. Since the input from the succeeding stage is high at this time, the clock frequency that appears on A61B (pin #6) also appears on the output of A61B (pin #10), but inverted in phase. This output is connected to one of the "OR" inputs on the output counter single shot (A27) of Figure 27 which produces a clock pulse on the output of the clock driver (A28B). The output of A21D, pin #1 is forced LOW by the "ANDing" of its two inputs with HIGH states. This output is connected to a count-up gate input (A26B) of Figure 28, if it is desired that the output counter count up, or, if it is connected to the countdown gate input (A25B) if the output counter is desired to count down.

When the next transition is reached, the previous state must be stopped. This is accomplished by feeding a LOW state into the inputs of A61B, pin #7 and A21D, pin #2. This results in outputs A61B, pin #10 and A21D, pin #1 being latched in the HIGH state

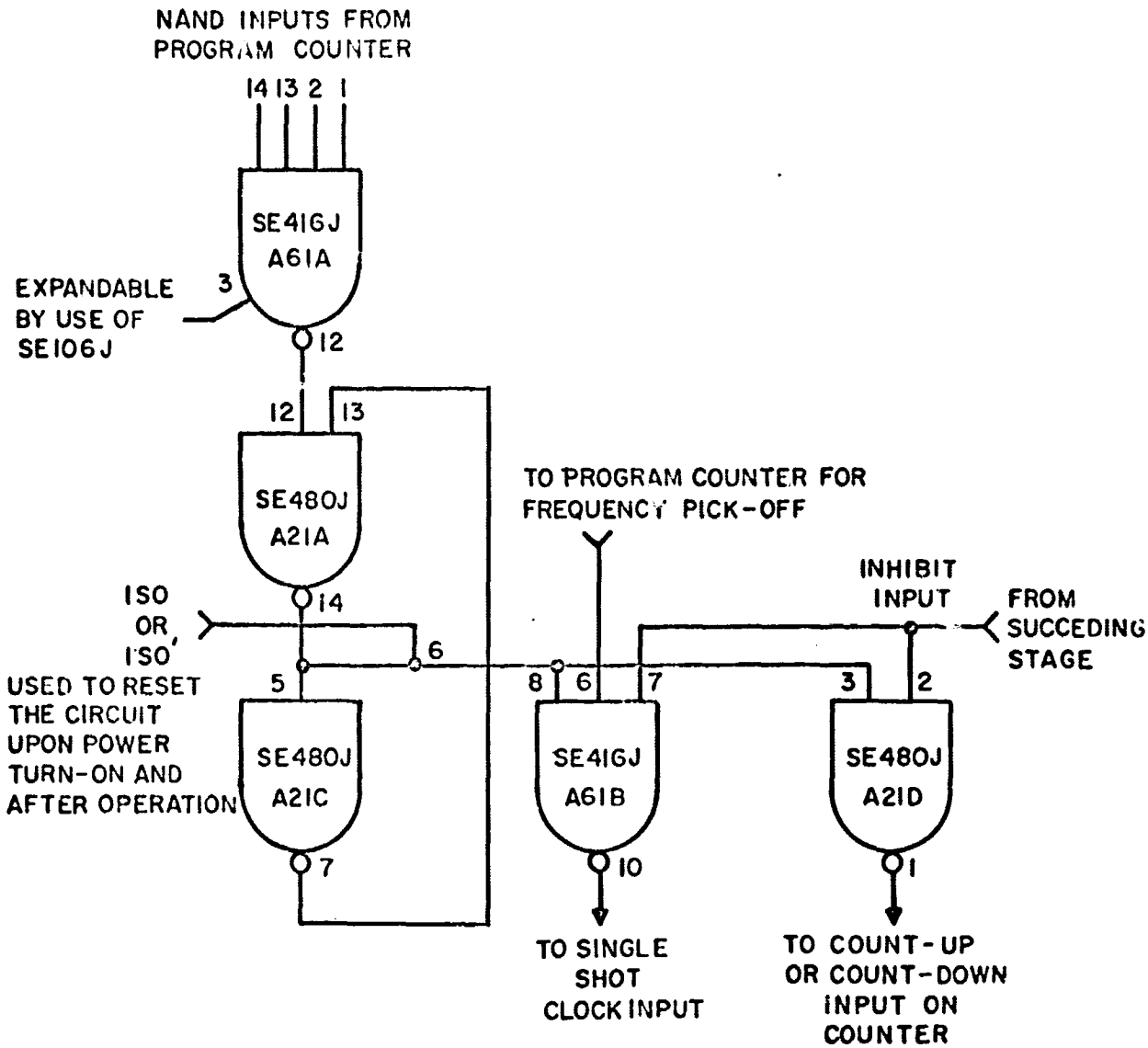
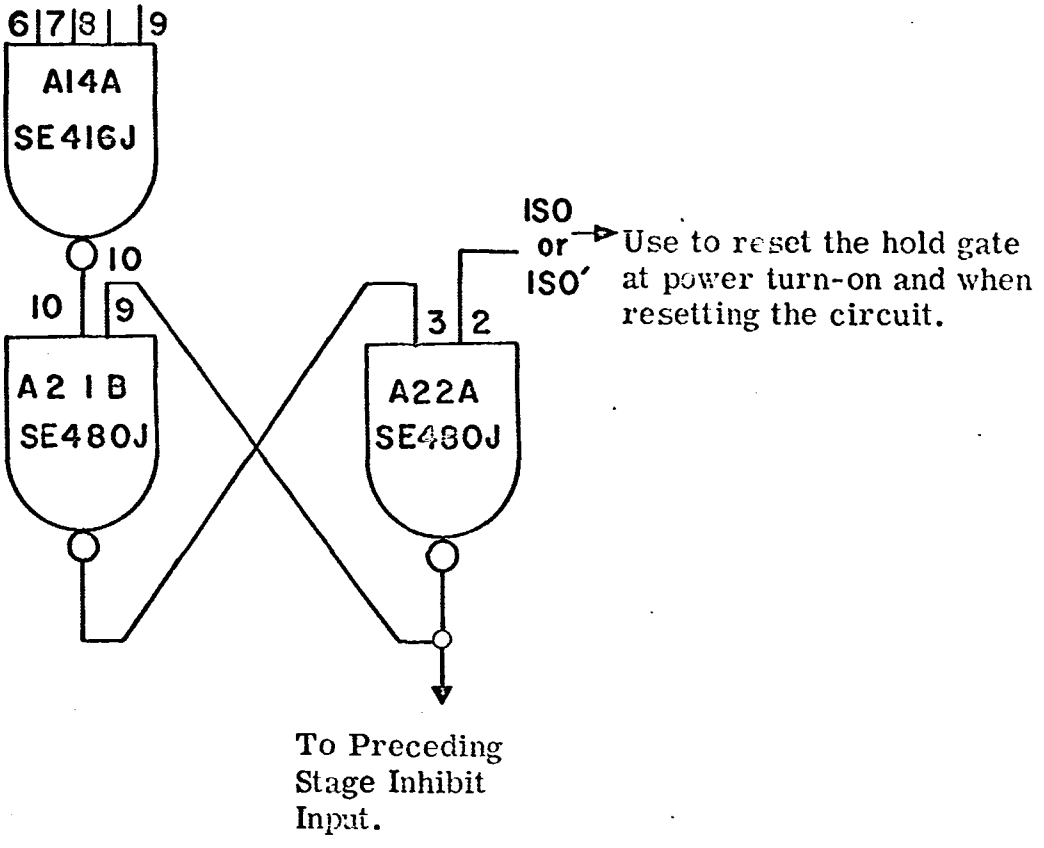


FIGURE 27. FREQUENCY TRANSITION GATE

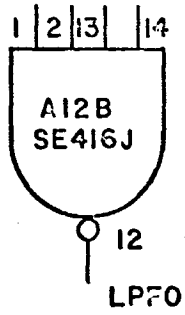
allowing the succeeding transition to control. This inhibit input is driven from either an output similar to A21C, pin #7 or from the output of either a hold gate or a program finish gate.

The hold gate consists of two SE 480J - two input gates and one SE 416J four input gate as shown below.



The "NAND" gate (A14A) input is similar to that of the frequency transition gate. When the output of this gate goes low the latch gate arrangement (A21B and A22A) is activated holding A22A, pin #1 in the LOW state. When this is connected to the inhibit input of a frequency transition gate, the frequency gate and count-up or -down outputs are inhibited, stopping the clocks from being fed to the output counters and pulling the counter out of both the count-up and count-down modes. The output counter controlled by these outputs, consequently, holds whatever state it was in prior to the hold.

The last of these three gates is the program finish gate, as shown schematically below.



It can be seen that the long program finish output is a multiple input NAND gate (SE 416J). The output of this circuit is connected to the gate that controls the clock input to the program counter (A1A). When this output (A12B, pin #12) goes low the clock is inhibited from being fed to the program counter and both programs are locked up since no clocks are fed to either output counter. The LPFO output is also connected to the inhibit input of the previous frequency transition to inhibit the count-up or -down output and provide better noise protection for the counter.

If two programs are required, the shorter of the two programs uses a program hold gate as a program finish gate and the output is called SPFO. The output of this gate is connected to the inhibit input of the last frequency transition gate used in that program.

Since the program up-down synchronous counters for both programs are exactly alike, only one will be discussed. The schematic of the up-down counter is shown in Figure 28.

The difference between a synchronous counter and a ripple counter is that in a synchronous counter all bits receive the clock input simultaneously, with the proper steering logic being set up prior to the arrival of the clock pulse. In the ripple counter, each succeeding stage receives its clock from the preceding stage, hence a clock pulse ripples down the counter for as many bits as change during that clock period. In the synchronous counter, the logic for selection of which bit is to change when the clock pulse comes, is determined by all the preceding stages. By "ANDing" the count-up signal with logic derived from the "1" side of each flip-flop, the counter can be made to increment. By "ANDing" the count-down signal with logic derived from the zero side of each flip-flop, the counter can be made to decrement.

The count-up gate (A26B) employs an SE 416J so that multiple count-up signals can be "ORed" together. The same is true of the count-down gate (A25B).

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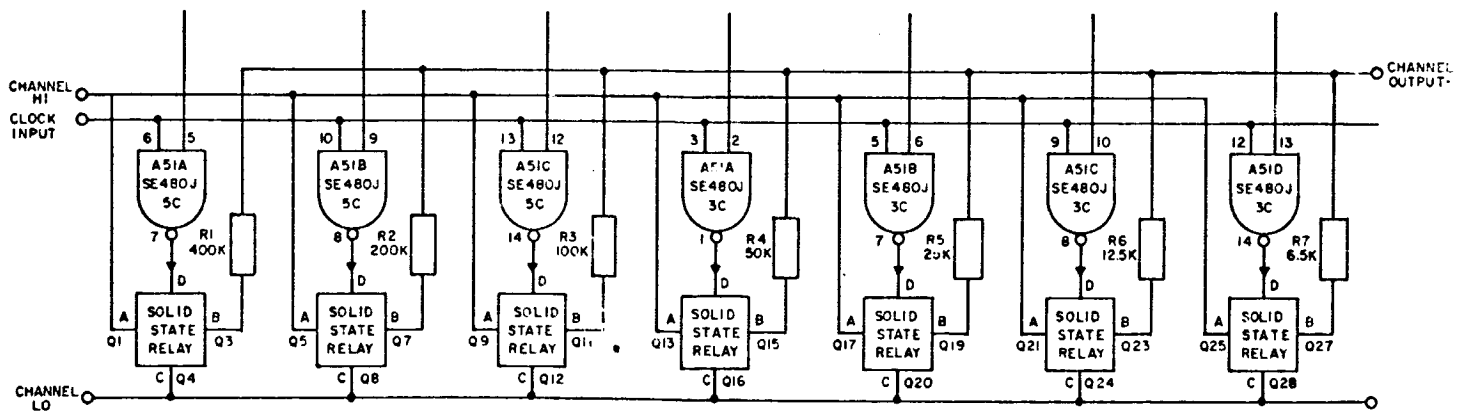
A single shot with multiple "OR" inputs was used to assure placement of the negative going edge to the clock line after all the logic operation in the program decoding was completed. The normally HIGH output was selected to assure that the clock line in the counter was in the LOW state when clock signals were not present as an added noise protection feature. The single shot drives a buffer driver circuit in order to be able to drive seven clock inputs.

The flip-flop outputs are initially arranged such that a reset input will set all bits in the "0" state. Four wires from each of the four most significant bits and brought out to the modular program plug-in so that the counter can be initially set into any count. A typical set of four wires per bit would be A32C, pin #5; A32A, pin #3; A39A, pins #12 and 13.

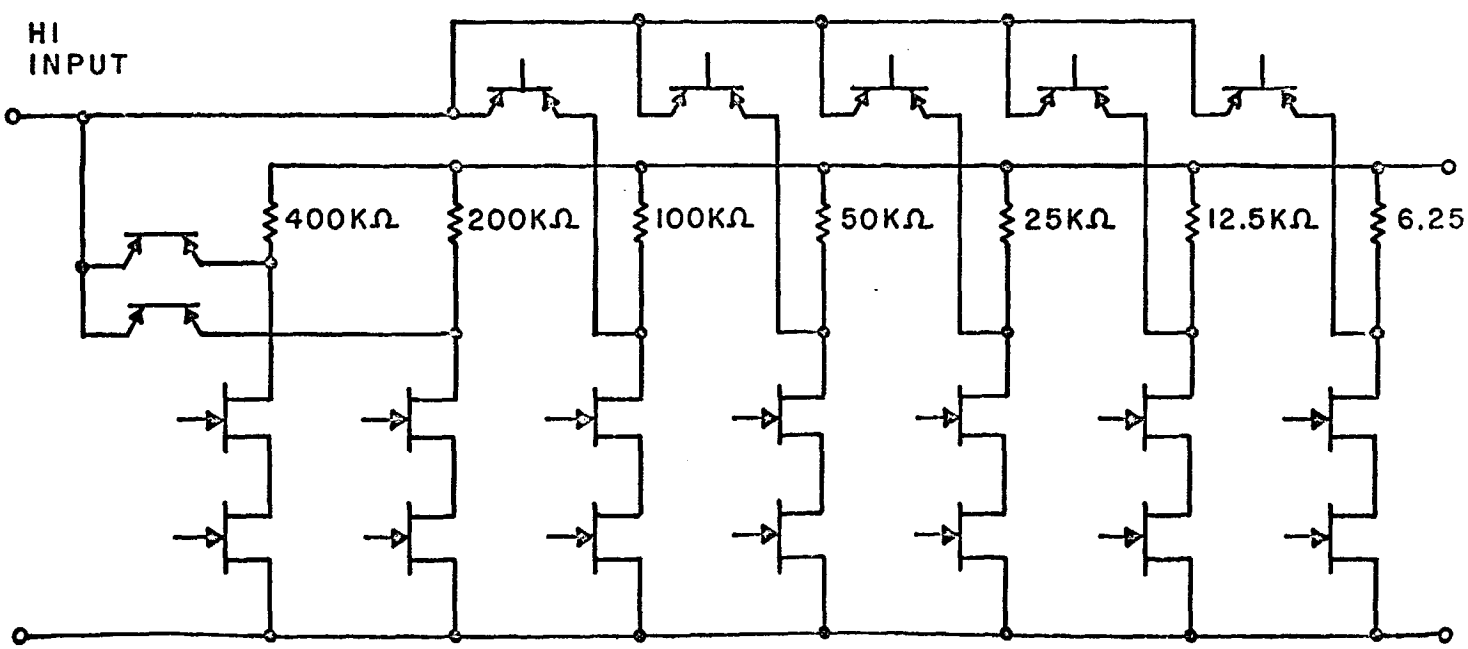
The output sections of both programs are identical, therefore, only one will be discussed. Each output section consists of seven two-input "NAND" gates, seven solid state relays, a resistor ladder network, a clock circuit and a "NAND" gate used as a buffer circuit. The schematic shown below depicts an entire output section.



Since the clock circuit and the solid state relay circuit are identical with those in the switching logic section, they will not be discussed further.

The "NAND" gates are connected to the outputs of successive flip-flops, the state which controls whether or not the relay clock signal is fed to the primaries of the solid state relay pulse transformers. These "NAND" gates drive the solid state relays.

The ladder network is the same as that used in the spatial amplifier with two resistors not being used (the 3.125 K and the 26.7 K). By connecting the resistor common point to the output of the channel and each of the weighted resistors to the relay corresponding to its weight (400 K to the solid state relay driven by the first bit in the counter, A37A, etc.) a linear attenuation variation relationship is set up between the count in the output counter and the attenuation with respect to the output of the channel. Since the "on" resistance of the FET is less than 100 ohms each and the "on" resistance of the dual emitter chopper is less than 100 ohms and since 70 ohms for each bit is designed into the ladder network, the switch resistance is negligible. The channel digital attenuator abbreviated is shown below.



The complete solid state relays are not shown. Prior to the first count in the counter all FET's shown are in the "on" state. With the assumption that the "on" resistances of the devices are negligible, the equivalent circuit is shown in Figure 29.

Successive steps from the "0" bit position to the fifth bit position are shown, and the attenuation on the output is shown. The digital attenuation steps are in 0.72% increments. The last "NAND" gate is used to drive the second channel clock inputs to minimize loading effects on the clock circuit.

The modular plug-in section consists of all wires necessary to maintain flexibility to change programs. The connectors needed here will require 125 pins and a mating connector with a plug-in patch board.

There are four levels of grounds in this circuit. They are the two channel low inputs which are isolated from each other and all other grounds by the pulse transformers and the dual emitter chopper and FET isolation. The logic ground is interposed between the channel low sides and -28 V by the isolated inverter transformer winding.

Buffer amplifiers of the type used in the active filter are used on the input of each channel to present a constant impedance to the incoming channel.

A diode and capacitor is used on the input to the power supply to insure against affecting the circuit in case of short power interruptions.

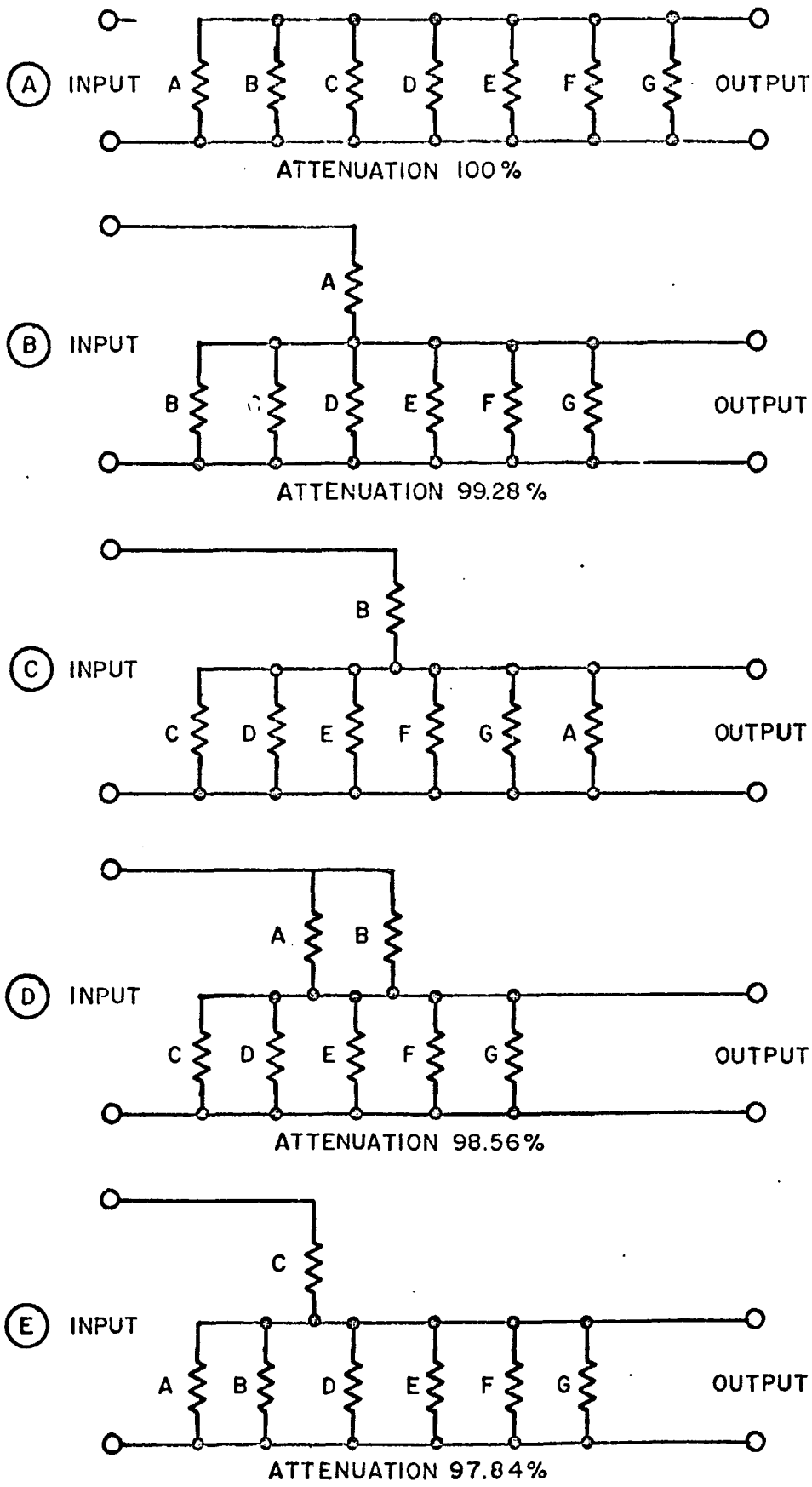


FIGURE 29. LADDER EQUIVALENT CIRCUIT

Spatial Amplifier Comparator

The redundancy scheme employed in the spatial amplifier system is similar to that used for the 50 ma servo amplifiers. Each spatial channel consists of a group of three identical amplifiers designated as A, B, and C. The A amplifier serves as a reference, the B amplifier is on-line, and C serves as a back-up or standby amplifier. The purpose of the comparator circuit is to compare the outputs of the A and B amplifiers and to switch the output loads to the C amplifier if A and B are sufficiently different.

The circuit developed to accomplish the desired comparison is shown in block diagram form in Figure 30. The output of the spatial amplifier is basically a train of pulses and the comparator is designed to compare the duty ratios of the output pulse trains from the A and B amplifiers. The output pulses from each amplifier are clipped at fixed voltage levels and the resultant is averaged by an RC integrator to provide a DC voltage proportional to the duty ratio. The difference in the two voltages thus derived is rectified to provide a unidirectional voltage proportional to the absolute difference in duty ratios as the input to the level detector. Full-wave rectification is accomplished by a four-transistor circuit which compensates for thermal drift and undesired nonlinearities and the output of which is referenced to the power supply.

The duty ratio check, as described, does not convey any information regarding the repetition rate of the spatial amplifier output pulses. In the digital spatial amplifier, the time base of the output is established by a circuit clock, the frequency of which is directly related to the repetition rate of the spatial output. In order to provide a more complete check on the operation of the spatial amplifier, the clock frequency is also monitored by the comparator.

The on-line spatial amplifier clock signal is a nominal 500 Hz symmetrical square wave. The delay time of a precision monostable multivibrator is compared with the half-period of the clock signal by an exclusive OR gate which produces a rectangular pulse having a width equal to the absolute difference between the monostable delay time and the half-period of the spatial amplifier clock signal. To facilitate comparison with a reference

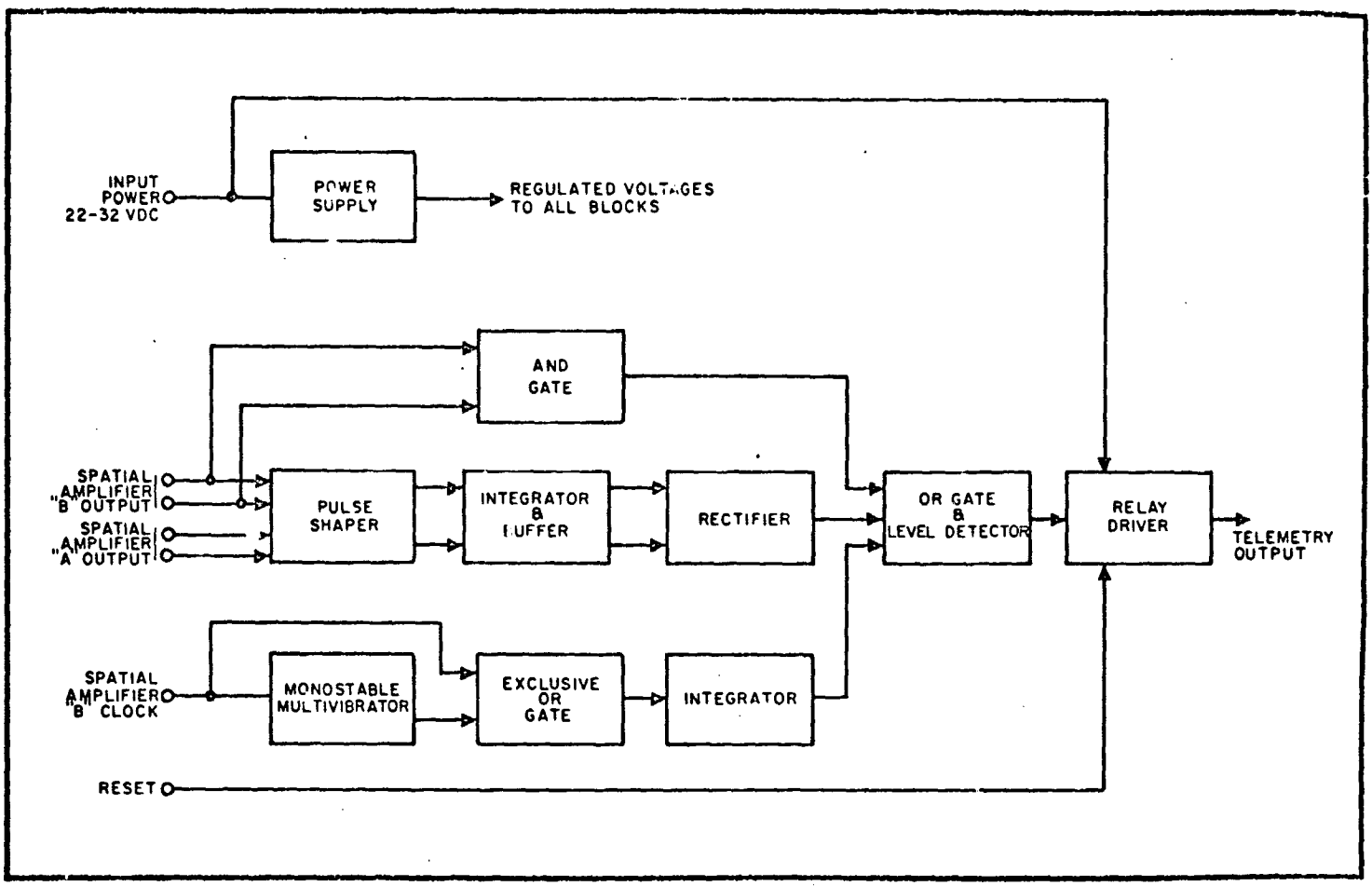


FIGURE 30. SPATIAL COMPARATOR BLOCK DIAGRAM

voltage, a simple RC integrator converts the output of the exclusive OR gate to a ramp voltage having a peak value approximately proportional to the pulse width. In this manner, the comparator is tripped when the clock period deviates excessively from the nominal value.

This method of monitoring the time base of the spatial amplifier output permits the use of smaller components than would be possible if the actual output pulses were used. The monostable multivibrator which provides the time reference against which the spatial clock frequency is compared uses a single 0.01 uf precision capacitor and provides a delay time stable to 0.5% over the entire temperature range.

Each spatial amplifier has two outputs, only one of which is activated at a given time depending on the polarity of the input to the spatial amplifier. The two output lines of the on-line spatial amplifier are monitored by an AND gate which trips the comparator if both outputs are activated simultaneously.

When the comparator is tripped by any of the three conditions previously described, the output loads are switched to the standby amplifier. The relay driver circuit latches after switching has occurred and must be manually reset. A telemetry output is provided to indicate the state of the comparator. Regulated voltages are provided by the power supply which is described previously.

A summary of the performance specifications of the comparator circuit is given below.

SPATIAL COMPARATOR SPECIFICATIONS	
Operating Temperature Range	$-55^{\circ}C$ to $+125^{\circ}C$
Power Requirements	22 - 32 V DC
Duty Ratio Trip Point	50 ±10% duty ratio
Clock Frequency Trip Point	7.5 ±2.5% from nominal

50 MA Servo Amplifier Comparator

The function of the servo amplifier comparator circuit is to compare the output current of the on-line amplifier with the output of a second similar amplifier used as a reference. If the two currents are sufficiently different, the comparator switches the servo actuator load to a third stand-by amplifier. The trip point is presently set at 8 ma ±3%.

The circuit developed to accomplish the desired function is shown in block diagram form in Figure 31. The power supply is described in detail previously, and provides regulated voltages for the transistor amplifier which are isolated from the 28 volt system power line. The output currents of both the "A" and "B" amplifiers are passed through bifilar-wound signal windings on the magnetic amplifier which produces an output voltage proportional to the difference in currents. This method of deriving the error signal for the comparator produces a large input signal at the trip point compared to thermally-induced drift signals. This permits the use of relatively simple, low-gain circuitry to achieve a temperature-stable trip point. Each of the bifilar signal windings is shunted by a pair of parallel diodes connected as shunt clippers. The voltage developed across the signal windings under normal conditions is insufficient to turn on the diodes, however, the diodes provide a current path in the event of an open winding.

The output of the magnetic amplifier is amplified further by a transistor amplifier utilizing two emitter-coupled differential stages for high gain and low drift. Capacitive feedback around the transistor amplifier is used to control the over-all frequency response of the comparator.

The output of the transistor amplifier is rectified by a full-wave diode bridge to produce an output voltage proportional to the absolute difference in the input currents such that the comparator responds identically to input signals of either polarity. As shown in Figure 31, the current through the diode bridge is injected as a feedback signal to the magnetic amplifier. This results in a stable over-all gain and near-perfect rectification by the diode bridge since nonlinearities and thermal drift introduced by the diodes are reduced by a factor equal to the gain of the preceding amplifier stages. The output voltage of the

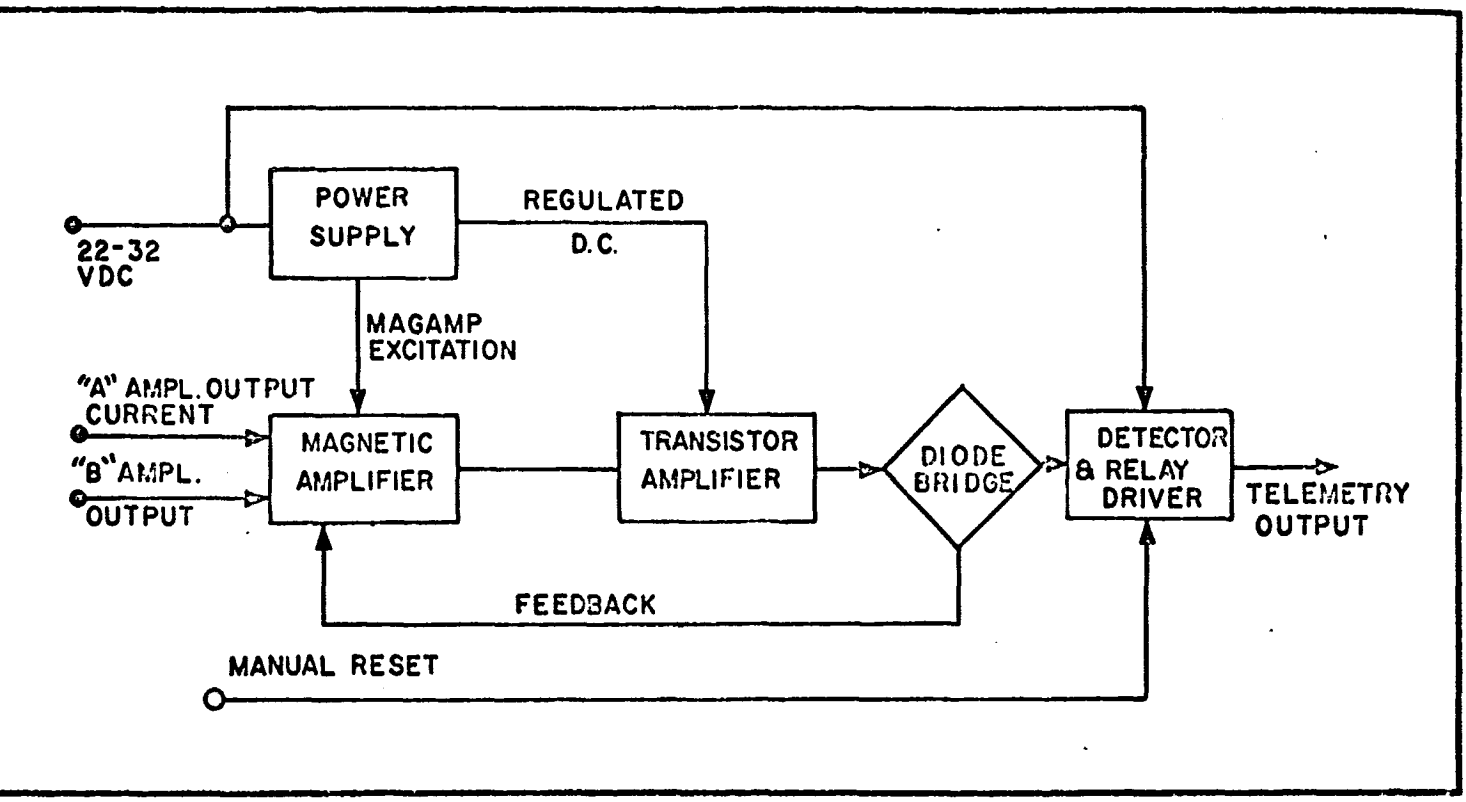


FIGURE 31. SERVO COMPARATOR BLOCK DIAGRAM

bridge is controlled by the value of a resistor connected across it. One side of this resistor is returned to the negative side of the 28 volt supply so that the output of the bridge can be compared with a zener-derived reference voltage. When the input current difference is ±8 ma, the bridge output voltage equals the reference voltage and the comparator trips. The relay driver circuitry incorporates a latching feature so that the circuit will remain in the tripped condition after switching has occurred. A manual reset capability is provided for testing purposes.

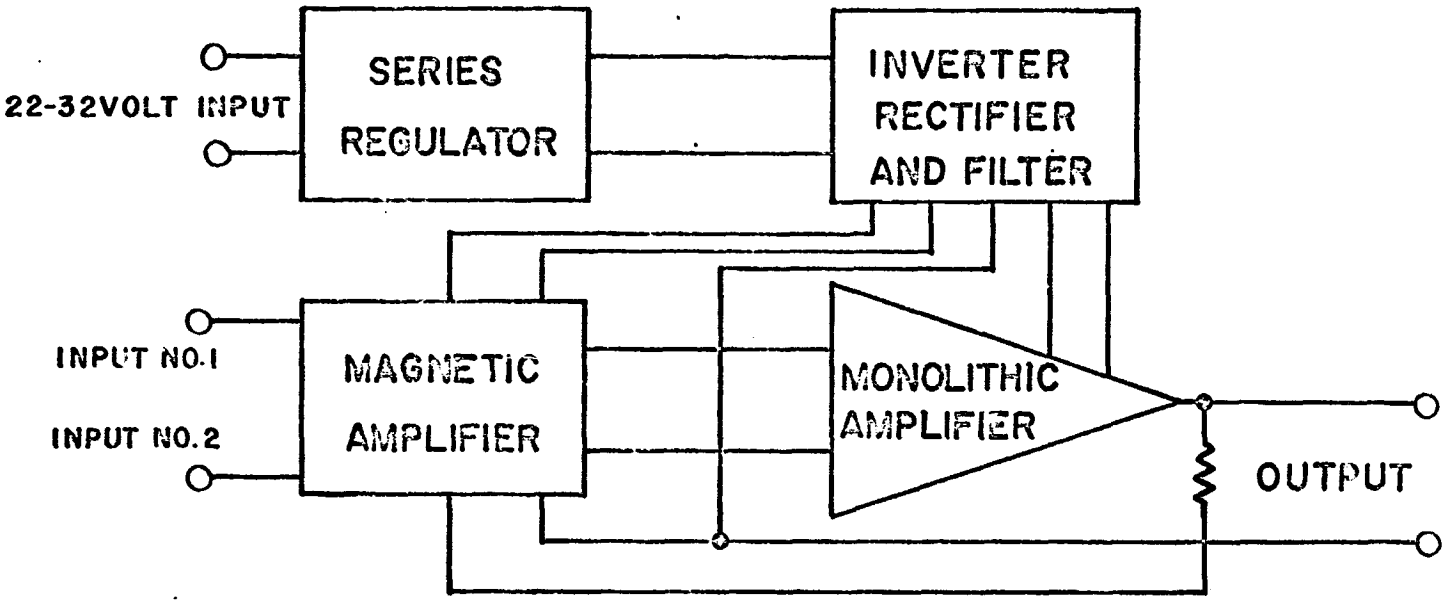
A total of three DPDT relays are used to switch the servo actuator load to the standby amplifier "C" and also switch the servo amp telemetry output lines to the "C" amplifier. Dummy loads for the "A" and "C" amplifiers are provided to minimize the transient introduced when the comparator is tripped. A comparator telemetry output is provided to indicate the state of the comparator.

A summary of the comparator specifications is given below. These characteristics have been confirmed by extensive testing.

SERVO AMP COMPARATOR SPECIFICATIONS	
Operating Temperature Range	$-55^{o}C$ to $+125^{o}C$
Power Requirements	22 - 32 V DC
Bandwidth (-3 db)	70 Hz min. 120 Hz max.
Trip Point	±8 ma ±3%

Spatial Telemetry Amplifier

The spatial telemetry amplifier is used to monitor the output current of the spatial amplifier and provide a proportional zero to ±2 volt telemetry signal at its output. The input and output are isolated from each other as well as from the 28 volt input power. A block diagram of the amplifier is shown below.



The magnetic amplifier used on the spatial telemetry amplifier is of the ultra low drift type initially developed for the 12 and 50 ma servo amplifiers as described previously.

The two input currents are derived from the voltage drops across two paralleled ten ohm resistors placed in series with the outputs from the spatial amplifier. With this arrangement the opening of a ten ohm resistor or a magnetic amplifier signal winding would not affect the operation of the spatial channel.

The output of the magnetic amplifier is connected to the differential input circuitry of a monolithic operational amplifier. The output of the monolithic amplifier provides a degenerate feedback current to a signal winding of the magnetic amplifier. The entire amplifier is therefore inclosed in a feedback loop. The closed loop bandwidth of approximately 200 Hz is established by the Miller feedback capacitor connected between input and output of the monolithic amplifier.

A summary of the spatial telemetry amplifier is given below.

SPATIAL TELEMETRY AMPLIFIER SPECIFICATIONS	
Input Voltage Range	22 to 32 Volts minimum
Input Current	12 ma nominal
Temperature Range	$-55^{o}C$ to $+125^{o}C$ minimum
Gain	2 Volts out for 210 ma in
Output Voltage	±2 Volts minimum
Bandwidth	150 Hz nominal
Null Drift	$\pm 10^{-2}$ Volts maximum referred to $+25^{o}C$

Spatial Limiter Circuit

The schematic in Figure 32 is the proposed limiter circuit for use in the spatial channels of the micromin computer. The limiter circuit will be used with an active filter amplifier for buffering purposes. The limiter, although simple in design, contains temperature compensation by means of the input steering diodes. The power supply for the limiter will be that of the active filter amplifier. With the use of low current (less than $250\mu a I_Z$) zener diodes, the circuit will require minimum power consumption.

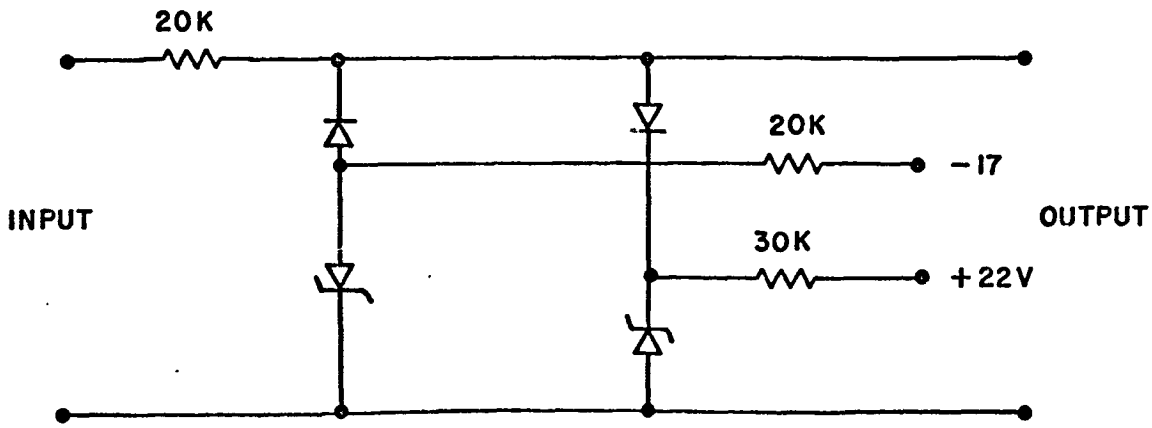


FIGURE 32. SPATIAL LIMITER SCHEMATIC