for "NASA ONLY"

SRRC-CR-67-65

AN INVESTIGATION OF THE EFFECTS OF RADIATION ON SILICON NITRIDE INSULATED GATE (MNS) TRANSISTORS

by

H A R Wegener, R. Frank and F Sewell

FINAL REPORT

Contract No. NAS5-10223

MAY 1968

Prepared for

NATIONAL AERONAUTICS AND SPACE ADMINISTRATION
GODDARD SPACE FLIGHT CENTER
GREENBELT, MARYLAND 20771

SPERRY RAND RESEARCH CENTER
SUDBURY MASSACHUSETTS 01776

SQ1-50296K

AN INVESTIGATION OF THE EFFECTS OF RADIATION ON SILICON NITRIDE INSULATED GATE (MNS) TRANSISTORS

by

H A R Wegener, R Frank and F. Sewell

FINAL REPORT

Contract No NAS5-10223

MAY 1968

Prepared for

NATIONAL AERONAUTICS AND SPACE ADMINISTRATION
GODDARD SPACE FLIGHT CENTER
GREENBELT, MARYLAND 20771

SPERRY RAND RESEARCH CENTER
SUDBURY MASSACHUSETTS 01776

SUMMARY

Early data taken at the Goddard Space Flight Center indicated IGFETs using silicon nitride as the gate dielectric were more radiation resistant than IGFETs using silicon dioxide as the gate dielectric. This added resistance manifested itself in a smaller change in threshold voltage for the same dose and in the absence of degradation of transconductance and drain junction reverse leakage currents

Since no theory exists that permits detailed prediction of the effects of radiation on IGFETs, a program was initiated to study empirically the effects of various processing steps on the changes in device parameters brought about by irradiation with 1 MeV electrons.

Under this program, several slices of silicon were fabricated for each processing variant. Ten mounted, bonded, and encapsulated devices representative of these slices were then delivered to GSFC for irradiation.

In all, eight variants were introduced in the processing of the devices. Four of these resulted in large thermal instabilities. The stable device series incorporated a 200 Å thick oxide layer between silicon and silicon nitride. The variants in these slices were the manner for formation of this oxide layer, the effect of heat treatment, the effect of in situ etching before oxidation and the effect of vacuum baking before encapsulation

The most clear-cut result was the beneficial effect of vacuum baking. The in situ etching also resulted in greater radiation resistance. However, some of the most radiation resistant devices were the result of unknown factors.

All devices fabricated were significantly more radiation resistant than commercial MOS transistors. It is recommended that future work be concentrated on structuring the gate and modifying its properties in such a way that more rapid leakage of charge accumulated during radiation is possible.

TABLE OF CONTENTS

LIST OF TABLES (cont.)

I INTRODUCTION

The use of insulated-gate field-effect transistors and integrated circuits consisting of these devices is very attractive for space technology applications. This is because the devices consume less power than bipolar transistors and because integrated circuits consisting of these devices have a very high function density per unit weight. However, when such devices have a silicon oxide dielectric they exhibit a progressive deterioration of electrical characteristics under electron irradiation such as generated in the Van Allen belt. This deterioration basically affects two electrical parameters, the threshold voltage and the source-drain leakage current. Under electron irradiation the threshold voltage for p-channel devices increases from values near -5 V to values beyond -30 V, depending on operating bias and radiation flux. These high values of threshold voltage may be beyond the voltage that the power supply can furnish. In some cases, the threshold voltage may even increase beyond the drain junction breakdown voltage. Under either condition the transistor cannot be turned on. The source-to-drain leakage current also deteriorates when silicon oxide insulated (MOS) transistors are subjected to electron irradiation It has been observed that under operating conditions electron radiation causes the leakage current to increase from near 10^{-10} ampere to 10^{-5} ampere.

Insulated-gate field-effect transistors that do not depend on silicon oxide have recently been made. Instead, silicon nitride has been used as the gate dielectric.[1] These MNS transistors have characteristics very much like those of MOS transistors, except that they confer the advantageous properties of silicon nitride on these devices.[2] F Gordon, Jr. and H E. Wannemacher, Jr. first found that MNS transistors were more resistant to 1 MeV electron radiation than MOS transistors.[3] They found that even under an operating gate bias of -20 V the change in threshold voltage was at most 17%.[4] Later, Stanley[5,6] and Wegener[5] indicated that even the maximum threshold voltages were significantly small in MNS transistors, although they were at gate voltages that were much higher than normal operating voltages. In addition, there was

LIST OF ILLUSTRATIONS

LIST OF TABLES

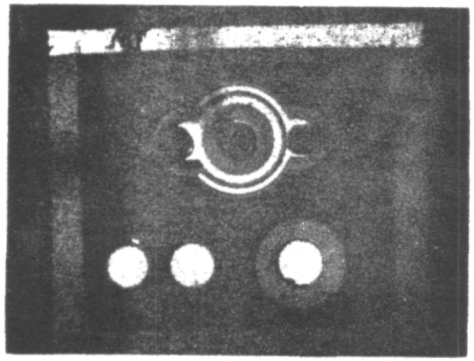
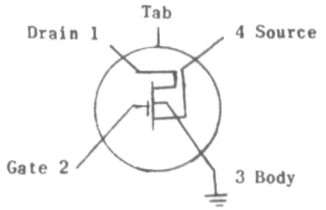


FIG. 1 Transistor geometry used for initial test vehicle.

TABLE 1. General Specifications of p-channel Enhancement Mode MNS Field Transistor.

Electrical Characteristics

Symbol	Characteristic	Value Min.	Typical	Max.	Units	Conditions
V_T	Turn-on voltage	-3	-4	-5	V	$V_{DS} = V_{GS}, I_D = 10\ \mu A$
G_m	Transconductance	1300	1500	1800	μmhos	$V_{DS} = V_{GS}, I_D = 10$ mA
BV_{DSS}	Breakdown voltage	70	72	75	V	$V_{GS} = 0, I_D = 10\ \mu A$
I_{GSO}	Gate leakage			100	nA	$V_{DS} = 0, V_{GS} = -20$ V
I_{GDO}	Gate leakage			100	nA	$V_{GS} = 0, V_{DS} = -20$ V
I_{DSS}	Junction leakage			100	nA	$V_{GS} = 0, V_{DS} = -20$ V
V_{on}	Gate voltage	15	17	20	V	$V_{DS} = V_{GS}, I_D = 10$ mA



TOP VIEW

no increase in source-drain leakage current All these results give promise that silicon nitride insulated-gate field-effect transistors will be essentially unaffected by the radiation normally encountered by space vehicles Electrically MNS transistors perform as well as MOS transistors Further there are indications that improvements in performance and reliability may be achieved with MNS transistors because their surface charge densities can be better controlled and because they are less susceptible to contamination.

These studies have led to the present program which was to be conducted as follows:

(1) A minimum of 10 silicon wafers would be processed for the fabrication of enhancement mode MNS transistors.

(2) The process steps for each wafer would be determined by initial information and by the information developed from NASA radiation studies The process variables to be considered were the silicon nitride deposition conditions, the silicon resistivity type and surface state conditions, the metallization procedure, the encapsulation

(3) A minimum of 10 device chips from each wafer would be mounted and contacted These chips would include both transistor and Hall-effect structures.

(4) These mounted devices would be evaluated at SRRC and then would be furnished to NASA for initial evaluation for irradiation and for post-irradiation measurement If desired a similar post-irradiation study would be conducted at SRRC

(5) Consultation between NASA and SRRC would determine the sequence of experiments to be performed

(6) A minimum of 100 evaluation samples would be furnished to NASA.

II. DISCUSSION

A. GENERAL PROCEDURES

1 Purpose. In this chapter all the aspects common to the more detailed experiments discussed later on are brought together These features are the structure of the IGFET used as a test vehicle the form of packaging

employed for this transistor, and the overall plan of fabrication of the transistor. It is clear that acceptance testing techniques at the Sperry Rand Research Center and the Goddard Space Flight Center also require description in separate sections. The actual irradiation procedures and the measurement of radiation effects are discussed next. This chapter concludes with a general plan for the reporting of the experimental series undertaken.

2 Design of the MNS Transistor Used as a Test Vehicle. A constant factor in all the process variations to be tried in the fabrication of the MNS transistor is its geometrical design. Figure 1, a photograph of a completed device structure, illustrates its features. A circular drain is completely surrounded by an annular channel which, in turn, has a source encircling it on all sides. Space for the gate is provided by a nearly circular enlargement of a small section of the gate. This contact is surrounded by only a narrow strip of the diffused source; the contact metallization of the source is not carried around it because the large width of the gate in that section reduces the channel current to insignificance. Parameters important to the device characteristics are the average gate diameter of 0.007 inches, a gate width of 0.0005 inches, a junction depth of 2.5 μ and a gate dielectric thickness of 1000 - 1200 Å. The angle subtended by the gate contact with respect to the center of the drain is 80^{0}, so that 2/9 of the gate circumference is inactive electrically. If permanent inversion occurred as a result of electron irradiation, the enclosed drain would permit the measurement of channel parameters. The electrical specifications of this design are given in Table 1.

3. Packaging of Devices. In order to obtain meaningful data, as large a number of devices as possible should be exposed to radiation under various conditions of gate and drain bias. One approach would be to keep all devices together on a slice after the processing had been completed. In order to permit putting a bias on the gates of all devices during irradiation, all gates must be connected by strips of metallization to a large region on the slice, to which the leads of a power supply can then be clipped. This approach involves only the modification of the final metallization mask. Thin strips of aluminum connect each gate to wider trunklines running in parallel across the whole slice. A ring of aluminum left around the edge of the slice connects

all trunklines together This mask was designed and made However this approach was not used in practice since testing required the individual probing of devices It developed that this was incompatible with the existing automatic test equipment at the Goddard Space Flight Center

Another approach considered was the mounting of nine devices on a twelve-lead TO-5 header All sources substrates and gates would go to common posts, respectively, while the drains of each device would have individual connections. This approach was rejected because the twelve-lead sockets and the necessary wiring would have made testing too complex. In addition, there might have been the problem of locating blocks of nine contiguous devices on a slice and separating these blocks from the rest of the slice. Another approach could have been to mount several chips on one header, which again would have entailed practical problems

We finally decided to mount each device separately on four-lead TO-5 headers The lead connection scheme is shown in Table 1. All were packaged in this way, making both mounting and testing routine The caps were spotwelded to the headers for easy removal in case the effect of secondary electrons from the cap required investigation.

4 Processing For the first quarter of the contract period a processing procedure was used for making MNS transistors that had become a standard over the year preceding the contract This procedure is outlined in the following paragraphs.

The substrate for the device is a 10 Ω-cm n-type slice of silicon 0.10 ± 0.001 inches thick and mechanically polished on one side - This slice is cleaned etched, and rinsed in deionized water Then a layer of silicon nitride is deposited on it at 900°C by the vapor phase pyrolysis of ammonia and silane The thickness of the deposited layer is 1900 Å.

The windows for source and drain diffusion are cut into the silicon nitride layer by standard photoresist etching procedures Boron oxide is then deposited on the slice in a platinum box arrangement Next the thickness of the silicon nitride in the gate region is reduced to about

500 Å. A layer of silicon nitride 500-700 Å thick is then deposited over the whole slice. After this, the boron deposited into the source and drain windows is driven into a junction depth of 2 5 μ. Contact windows are then opened over source and drain by photoresist methods Next, aluminum is evaporated over the whole slice to a thickness of 3000 Å. The contact pattern is defined using Shipley photoresist. A heat treatment to alloy the aluminum completes the processing sequence.

5. Characterization of Transistors at SRRC. As Table 1 indicates, there are many characteristics that describe an IGFET. Based on references 5 and 6, the most likely changes in electrical performance of IGFETS after electron irradiation are the reverse junction characteristics, the transdonductance of the device, and most important, the threshold voltage. In order to simplify the measurement of a large number of devices, we have chosen to describe these three in terms of a voltage taken at a constant current. This becomes particularly simple when a Tektronix 575 curve tracer is employed.

The reverse characteristics of the drain junction are thus defined by the voltage V_{BD} at the drain when 10 μA are flowing in the reverse direction. Source and gate are held at zero volts. A deterioration of the characteristic is indicated by a drastic decrease of this voltage.

The transconductance is characterized by the "on-voltage", V_{on}. This is the voltage at the drain, with gate and drain connected to each other, when a current of 10 mA is flowing between source and drain. Substrate and source are also connected to each other. The transconductance at 10 mA, can be, if desired, calculated by multiplying 10 mA by two, and dividing that value by the difference between V_{on} and the threshold voltage V_T

$$gm = \frac{2I_{DS}}{V_{on}-V_T}$$

A deterioration in transconductance is indicated by an increase in V_{on}.

The threshold voltage V_T is defined by the voltage on the gate, with the drain connected to the gate and source and substrate connected to each other, at which the current between source and drain is 10 μA. Any major change in the threshold voltage is deleterious, and much attention will be focused on this value.

6. Characterization of Transistors at GSFC. The most important pre-irradiation measurement at GSFC was a determination of the thermal stability of the contract samples. As each lot of 10 devices was submitted, two were subjected to a standardized temperature-bias stress, one with a +20 V gate voltage and the other with a -20 V bias. The standard test consisted of heating the device to 175°C for 0.5 hour under appropriate bias, maintaining the bias until the devices returned to room temperature. Lots with gate threshold shifts greater than an arbitrary amount, nominally ± 2 V, were not irradiated. Gate threshold voltage shifts as large as 2 V, whether due to radiation-bias or temperature-bias instability, would render contemplated circuits inoperable.

The gate threshold voltage was determined from a plot of the drain current vs gate voltage, as shown in Fig 2. The drain voltage was set at -10 V and the gate voltage was swept negatively from zero until a full scale current deflection was obtained on the X-Y recorder at a sensitivity of 20 μA/in The gate threshold voltage was defined and read off at the 10 μA point. This curve also shows up any unusual device characteristics such as soft source and drain diodes, leaky gate insulator, and changes in transconductance after irradiation

As a check on this measurement and to observe other device characteristics, the gate capacitance vs gate voltage was measured. A simple 1 MHz admittance measurement, Fig 2, is used where it is assumed that the real part of the complex current is negligible. This assumption has been checked and found to be reasonable for most cases. The gate voltage can be swept in either direction in this measurement. Besides verifying the gate threshold voltage, one can easily determine the extent of fast interface states, and the existence of states that follow the high frequency but not the slowly swept dc bias. Certain geometrical effects can also be seen Various conclusions with

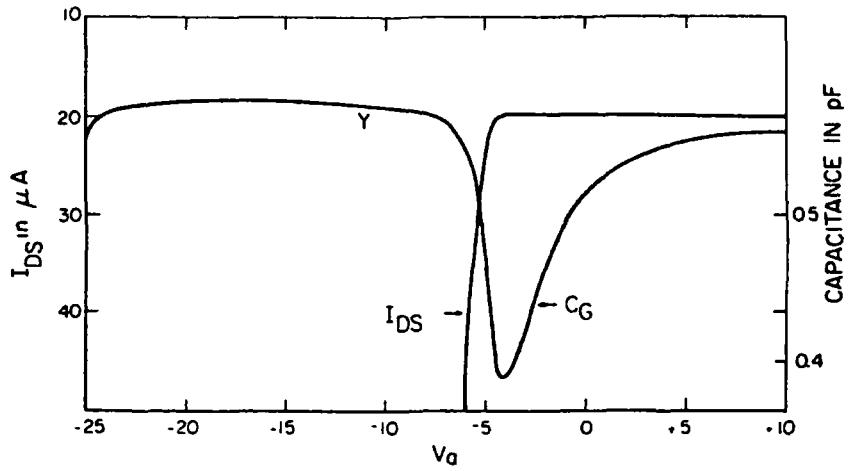


FIG. 2 Plot of gate capacitance C_g and saturation drain current I_{DS} vs applied bias V_G .

respect to these properties and the variations in fabrication procedures have been drawn at the close of each section.

In general, these two measurements have been made at three points in the experiment. First, after the devices have been received; second, after the thermal stability test; and last, after the irradiation. Occasionally these measurements were made at various intermediate fluence points, but usually this was handled in a different way, as is described below.

7. Irradiation Procedures and In Situ Measurements. The devices that were sufficiently stable under the temperature-bias stress were irradiated using the GSFC Van de Graaff. Devices were in all cases irradiated with 1.5 MeV electrons at rates of 1×10^{10} e/cm^2/sec. The devices were mounted on a printed circuit card and placed at the end of the scanning horn of the accelerator The beam was scanned so that all devices were covered. A Faraday cup was placed with its aperture in the same plane as the devices to measure the dose rate and dose.

The gate threshold voltages were continually monitored during irradiation by means of an automatic data acquisition system. The devices from each lot were irradiated under various negative biases The bias was removed at various intervals by the data system, and the device was switched to the gate threshold measurement mode. In this configuration, the gate was tied to the drain, while a constant current supply set to 10 μA was used as the drain supply The gate voltage was then recorded for this condition. The switching of the device to the measurement configuration, the actual measurement, and the switching back took less than 500 msec per device. The data is punched onto paper tape for later use.

In later experiments a gate voltage for a 1 mA drain current was also recorded This measurement gives a rough indication of any changes in the transconductance during irradiation This measurement permits large quantities of data to be accumulated in a relatively short time.

Due to tight scheduling of accelerator time, device lots were not studied any further where just two or three irradiated samples showed large shifts in gate threshold voltage.

8. Plan of Experiments. The experiments reported in the following sections will all be reported in a standard pattern. A paragraph entitled "Purpose" will detail the reasons for this experiment. The paragraph "Variants" will describe the experimental modifications in processing, device structure, and measurements, by which this purpose was accomplished. This paragraph is followed by that entitled "Electrical Results", which will report data obtained both at SRRC and GSFC. The final paragraph entitled "Interpretation" of an experimental result will generally lead into the "Purpose" of the following series.

B. INITIAL EXPERIMENTS

1. Purpose. The first program included the study of p-channel MNS transistors fabricated with variations in deposition temperature, post-deposition heat treatment, surface treatment before deposition, and the type of metallization. It was expected that the deposition temperature would affect both the interface between the nitride and the silicon and the structural details of the nitride proper. For this reason, the practical range of deposition was to be explored by runs done at 700°C, 900°C, and 1100°C. Post-deposition heat treatments were expected to have an effect similar to that of the deposition temperature. The effect of post-deposition heat treatments was to be explored by storage at temperatures of 300°C, 700°C, and 1000°C. Surface treatments before deposition should generally affect only the interface properties of the structure. They were to be investigated by the comparison of wet chemical processes with in situ etching runs. The effect of metallization on the device behavior under irradiation would probably be dependent on the production of secondary electrons in the metal For this reason a light metal, aluminum, and a heavy metal, gold, were to be used in a comparative study

2. Variants. In order to establish a basis of comparison, the first slice under this contract was fabricated by the "standard" process detailed in the preceding section. Twenty devices were mounted, bonded, and tested. The results are shown in Table 2.

TABLE 2

Device Characteristics of Initial "Standard" Devices

	V_T	V_{on}	BV_{DSS}
1	3.6	16	70
2	4.2	17.5	73
3	4.1	16	72
4	3.4	15	72
5	3.5	16	70
6	4.1	17	72
7	3.7	15	74
8	4.0	16	70
9	3.9	17	70
10	3.8	17.5	72
11	3.7	17	73
12	3.8	16	72
13	4.9	19	73
14	4.5	19	72
15	4.3	16	72
16	4.6	17	70
17	4.3	15.5	73
18	4.2	20	70
19	4.4	16.5	70
20	4.1	19	71

Post-deposition heat treatments can be inserted in the standard processing sequence immediately before the evaporation of the aluminum without affecting any other detail of fabrication. This is important, especially for heat treatments at higher temperatures, since the eutectic point of silicon with aluminum lies at 577°C. Temperatures in exesss of this value can cause the destruction of the devices due to uncontrolled alloying.

The first heat treatment was given at 300°C in dry nitrogen for a period of sixty-four hours.

The second slice in this series was subjected to a two-hour treatment at 700°C in dry nitrogen in the appropriate place in the processing sequence.

3. Electrical Results. The data in Table 2 were obtained from devices made by the standard process sequence. In Table 3 are data for the slice that received the 64 hour heat treatment at 300°C, and Table 4 gives the data for the slice that was subjected to a two hour heat treatment at 700°C.

One device each of the 300°C and 700°C heat-treated transistors was subjected to thermal cycling at +175°C. Device #1 of the 300°C series shifted from a threshold voltage of -1.4 V to -8 V under positive bias, and from the latter voltage to +5.1 V under negative bias. Device #1 of the 700°C series shifted from -8.7 V to -10.1 V under positive bias, and from there to -6 7 V under negative bias.

The thermal instability that was exhibited by the above devices made a radiation experiment appear superfluous.

4 Interpretation. The thermal instability was a complete surprise.

Transistors fabricated until this time had been subjected to a thermal stability test at 150°C at a positive bias of +15 V, and had been found to vary by less than 0.5 V. Since this result had become routine, testing for it had been suspended.

TABLE 3

Device Characteristics of MNS Transistors Heat Treated at 300°C

	V_T	V_{on}	BV_{DSS}
1	1.4	12.5	72
2	2.1	14.0	73
3	2.3	16.0	64
4	1.7	12.0	68
5	2.2	12.5	68
6	1.4	11.5	65
7	2.4	13.0	68
8	1.7	13.5	69
9	1.3	12.0	66
10	1.6	13.0	68

TABLE 4

Device Characteristics of MNS Transistors Heat Treated at 700°C

	V_T	V_{on}	BV_{DSS}
1	8.5	27	103
2	7.3	27	110
3	5.9	24	103
4	6.1	24	106
5	6.0	24	108
6	6.4	23	105
7	8.3	26	108
8	5.3	23	100
9	8.0	26	110
10	7.5	25	104

The cause of this change in stability behavior was undoubtedly connected with a change in procedure that was instituted to improve the reproducibility of the deposition of silicon nitride. Until that time, a relatively constant background of oxidizing impurities in the gases used for nitride deposition had resulted in silicon nitride layers of reproducible quality. Then a much higher purity gas was specified, and oxidizing agents were added deliberately to yield the same properties that had been obtained previously with the less pure gases. The oxidizing agent used ultimately was N_2O. It was with these more highly controlled gases that the first transistors had been made under this contract.

The different behavior of the transistors undoubtedly arose from some change at the interface between the silicon and the silicon nitride under the gate electrode. Therefore, something before or at the beginning of the actual nitride deposit, was involved. It was surmised that the oxygen-bearing gases present in the older reactant gases formed a thin oxide layer on bare silicon nitride during the time necessary to bring the slice to the temperature required for nitride deposition. In order to reproduce the older process, then, it would be necessary to form the oxide layer deliberately.

C. THERMAL OXIDE INTERLAYER

1. Purpose. The unexpected instabilities found in the transistors forced a reappraisal of our processing techniques.

It was hoped that a thin oxide layer would cure the instabilities, and otherwise would still permit the good radiation resistance of the MNS transistors to prevail.

This resulted in two changes in procedure. First, the deposition of silicon nitride was modified to include the formation of a 200 Å oxide layer between the bare silicon and the silicon nitride. Second, temperature-bias testing was instituted to monitor the effect of process changes on the thermal instability of the threshold voltage.

2. Variants. In general, the process remained the same as described before. Also, the device structure and the masks leading to it were not changed. The one important modification occurred right after the deposition of the boron dopant in the source and drain windows. At that point in the process, the silicon nitride was removed completely in the region under the gate. A 200 Å oxide layer was then formed by thermal oxidation in a diffusion furnace at 1200°C in dry oxygen. The slice was then transferred to the reactor, and 1000 Å of silicon nitride were deposited over the whole slice. Drive-in diffusion and all other steps remained the same as described previously.

The device characterization was expanded to include storage of the devices at 150°C, with positive and negative biases of 15 V on the gate alternated every 24 hours. This test extended over a week. Once every day, except on weekends, V_T, V_{BD}, and V_{on} were recorded. Only after this test was satisfactory would devices be subjected to irradiation.

3. Electrical Results. In Table 5, the voltage characterization of the test transistors made with a furnace-grown thermal oxide interlayer are shown. Table 6 shows the thermal stability of the threshold voltage of the same transistors, as measured at SRRC, Table 7 shows thermal stability data taken at GSFC. In spite of the large shifts observed in the latter tests, two devices were irradiated and the results given in Table 8.

4. Interpretation. There were two unexpected results associated with this series. The first one was that the stability measurements conducted at SRRC resulted in much smaller changes in V_T than those found at GSFC. A detailed comparison of procedures indicated that the devices were brought from high temperature to room temperature under different conditions. At SRRC, all biases were removed, while at GSFC the bias was left on the gate until the device had reached room temperature.

The second result of this run was the fact that although the extreme variations in V_T recorded with the previous transistors had been eliminated, there was still a large amount of variation This could be attributed either to a cleanliness problem in the oxidation furnace, or to contamination of the surface during transit between furnace and silicon nitride

TABLE 5

Characteristics of Furnace Grown Thermal Oxide Interlayer Devices

No.	V_T	V_{on}	BV_{DSS}
52	4 4	14 2	52
53	8.5	20 2	50
58	9.6	22.0	50
60	9.6	20.4	50
70	4.4	17.0	55
72	6.1	17.0	50
75	8.2	21.2	55
87	5.8	17.2	50
88	6.8	18.8	50
89	9.2	20 0	50

TABLE 6

Temperature-Bias Test of V_T of Furnace Grown Thermal Oxide Interlayer Devices

No.	Bias Date	Initial 12/12	-15 V 12/13	+15 V 12/14	-15 V 12/15	+15 V 12/16
52		4 4	No test	4.6	4.4	4.4
53		10	9 5	9.7	9.4	8.5
58		10	10	11	10	9.6
60		13	10	11	10	9.6
70		3.9	4.7	4 8	4.6	4.4
72		5.5	6.3	6 3	5.5	6.1
75		8 2	No test	8.9	8 8	8.2
87		5 0	"	5.8	5.2	5 8
88		6.6	"	7.2	7.3	6.8
89		9.0	"	9 6	9.6	9.2

TABLE 7

Temperature-Bias Test of V_T at +175°C

Device No.	Initial V_T	+20 V Bias	-20 V Bias
52	-4.4 V	+1.6 V	-1.5 V
75	-8.3 V	-1.0 V	-12.7 V

TABLE 8

Post-Irradiation Results of Furnace Grown Thermal Oxide Interlayer Devices

Device No.	Initial V_T	Gate Bias During Irradiation	Total Dose	Final V_T
88	-7.0 V	0 V	2×10^{14}	-10.2
70	-4.8 V	-35 V	2×10^{14}	- 2.2

reactor. However, in spite of the variations of the threshold voltage under temperature-bias conditions, the effect of radiation on the threshold voltage of the two units tested was small

D. EFFECT OF PACKAGING

1. Purpose. It will be recalled that all devices were packaged by mounting them on TO-5 headers, and then tacking on the caps to the headers by spot welding No particular bake-out procedure was employed, since the devices were open to the atmosphere anyway. At any rate, in the course of a test series at SRRC, it was found that devices originating from the same slice showed a different spread of electrical parameters before and after temperature-bias testing, depending on whether they had been packaged here at SRRC, or at the Sperry Semiconductor Division (SSD) in Norwalk. The latter packaging involved a vacuum bake-out and a hermetic seal between cap and header.

2. Variants. In order to assess the effect of packaging procedures on radiation resistance, devices from the same slice (#1051) were mounted, bonded and capped both at SRRC and at SSD

In addition, cooling under bias was instituted as a standard procedure during temperature-bias measurements

3. Electrical Results. The electrical parameters of devices from slice 1051 that were packaged at SRRC are shown in Table 9 Devices from the same slice, but packaged at SSD are also shown in that table. In addition, transistors from slice 34, also packaged at SSD, are characterized.

Both slices had been prepared by the process variant described under the heading "Thermal Oxide Interlayer". In addition, units from slice 23, prepared by the process described under "Initial Experiments", were submitted to electron radiation These data are also given in Table 9. The temperature-bias results for all these variants are given in Table 10. Table 11 details the radiation effects.

Figures 3 and 4 are typical plots of the threshold voltage at 10 μA (V_T) and at 1 mA (V_{on}) as a function of radiation dose. The constant distance between the two is equivalent to a transconductance unchanged by the radiation

TABLE 9

Characteristics of MNS Transistors

No.	V_T	V_{on}	BV_{DSS}
	(Slice 1051 packaged at SRRC)		
1	6.3	18	60
3	6.4	16	60
4	6.7	17	60
5	6.6	16	60
6	5.5	15	60
7	4.0	19	60
8	6.5	18	60
9	6.3	20	60
11	6.7	16	45
13	5.9	16	60
	(Slice 1051 packaged at SSD)		
R911	7.1	25	73
R912	7.2	18	55
R913	6.8	17	55
R914	7.6	18	55
R916	7.0	17	53

TABLE 9 (cont.)

No.	V_T	V_{on}	BV_{DSS}
	(Slice 34 packaged at SSD)		
2	6.5	22	52
3	6.2	17	50
4	6.1	23	50
5	6.0	24	55
8	5.5	24	52
14	5.9	24	50
15	5.5	21	48
18	6.3	24	52
20	6.1	24	52
28	6.0	19	55
	(Slice 23 packaged at SSD)		
10	6.5	15	22
11	7.1	19	25
12	7.1	25	22
13	6.4	17	21
14	6.5	17	22
15	7.1	16	22
16	6.9	17	20
18	7.0	16	20
19	6.8	17	23
20	6.5	16	18

TABLE 9

Characteristics of MNS Transistors

No.	V_T	V_{on}	BV_{DSS}
	(Slice 1051 packaged at SRRC)		
1	6.3	18	60
3	6.4	16	60
4	6.7	17	60
5	6.6	16	60
6	5.5	15	60
7	4.0	19	60
8	6.5	18	60
9	6.3	20	60
11	6.7	16	45
13	5.9	16	60
	(Slice 1051 packaged at SSD)		
R911	7.1	25	73
R912	7.2	18	55
R913	6.8	17	55
R914	7.6	18	55
R916	7.0	17	53

TABLE 10

Temperature-Bias Tests at 175°C

No.	Initial V_T	-20 V Bias	+20 V Bias
	(Slice 1051 capped at SRRC)		
4	-6.4	-5.2	-5.2
3	-3.2	—	-4.8
13	-5.75	—	-6.05
	(Slice 1051 capped at SSD)		
911	-7.1	-9.7	-6.6
912	-7 48	—	-7.2
	(Slice 34 capped at SSD)		
4	-6.25	-6.0	-6.0
5	-6.1	-5.8	-6.0

(Slice 23)

These devices exhibited hysteresis at room temperature and were therefore rejected from further investigation.

TABLE 9 (cont.)

No.	V_T	V_{on}	BV_{DSS}
	(Slice 34 packaged at SSD)		
2	6.5	22	52
3	6.2	17	50
4	6.1	23	50
5	6.0	24	55
8	5.5	24	52
14	5.9	24	50
15	5 5	21	48
18	6 3	24	52
20	6.1	24	52
28	6 0	19	55
	(Slice 23 packaged at SSD)		
10	6.5	15	22
11	7.1	19	25
12	7.1	25	22
13	6.4	17	21
14	6.5	17	22
15	7.1	16	22
16	6.9	17	20
18	7.0	16	20
19	6.8	17	23
20	6.5	16	18

TABLE 11

Post-Irradiation Results Obtained at Dose Rate of 10^{10} e/cm^2-sec

No.	Initial V_T (V)	Bias During Irradiation (V)	V_T at Dose of 1×10^{13} e/cm^2	Total Dose	Final V_T
		(Slice 1051 capped at SRRC)			
3	-4.8	0	-32	2×10^{13}	-33
13	-5.1	-35	-13	2×10^{14}	-35
		(Slice 1051 capped at SSD)			
R911	-6.8	0	-9.6	1×10^{13}	-9.6
R912	-7.5	-35	-11.9	1×10^{13}	-11.9
R913	-7.7	-35	-12.8	5×10^{13}	-17 7
R916	-7.0	-20	- 9 6	1×10^{13}	- 9 6
		(Slice 34 capped at SSD)			
4	-6.0	-35	-12 3	1×10^{13}	-12.3
5	-6.1	0	- 9.7	1×10^{13}	- 9 7

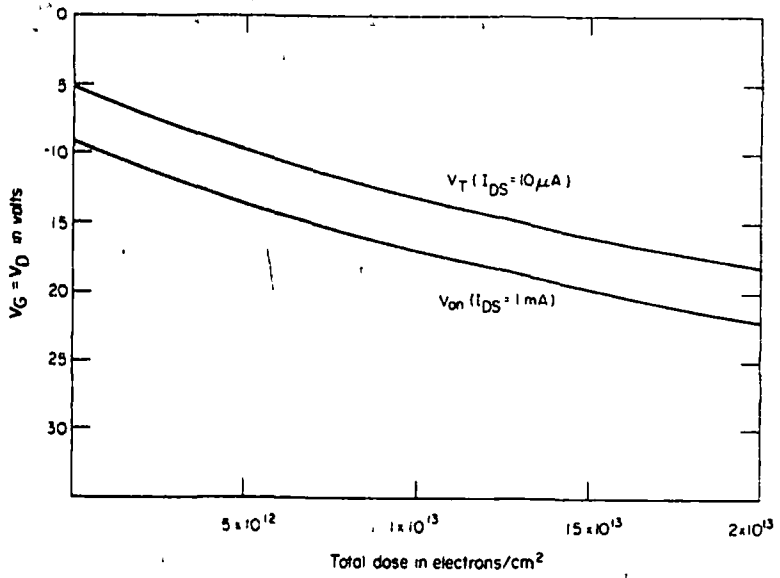


FIG. 3 Plot of V_T and V_{on} as a function of total dose at a dose rate of 1 x 10^{10} electrons/cm^2-sec for MNS transistor 1051-13. The gate bias during irradiation was zero

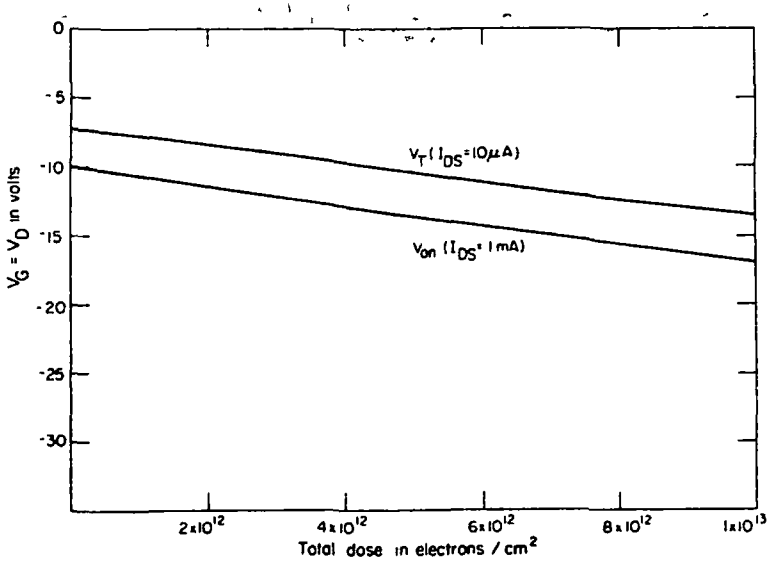


FIG 4 Plot of V_T and V_{on} as a function of total dose at a dose rate of 1 x 10^{10} electrons/cm^2-sec for MNS transistor 1051-R916. The gate bias during irradiation was -20 V.

4. Interpretation The results of this slice are quite remarkable. The devices from slices having an oxide interlayer (#34 and #1051) showed a narrower spread of threshold voltages and a smaller amount of change with radiation when they had been packaged at SSD. Apparently, the vacuum bake and the hermetic sealing associated with their encapsulation procedure made a strong difference. It was decided to incorporate vacuum baking and hermetic sealing into the standard process The improved packaging, unfortunately, did not improve the stability characteristics of slice 23, which had no oxide interlayer.

E IN SITU OXIDATION

1. Purpose The formation of the 200 Å oxide interlayer in a furnace gave stability results that were improved over those devices without it. But there was always the chance of contamination during the transfer of the slice from the furnace to the reactor. In order to eliminate this potential source of trouble, it was decided to form the oxide layer in the silicon nitride reactor.

2 Variant. For simplicity, the N_2O gas mixture used to dope the silicon nitride was also used as the oxidant. The oxidation was carried out at 1200°C. It required 10 minutes for the formation of a 200 Å oxide layer The susceptor was then cooled from 1200°C to 900°C, and the deposition of 1000 Å of silicon nitride was carried through. The process was the same as that described under "Thermal Oxide Interlayer" in all respects.

3 Electrical results. A batch of transistors from slice 1073, which was made by using in situ oxidation, is characterized in Tables 12 and 13. Temperature-bias tests done at GSFC confirmed the stability of these devices. The results of irradiation are given in Table 14. A plot of V_T and V_{on} vs dose is given in Fig 5.

4. Interpretation. This series of devices certainly exhibited a better thermal stability than previous devices Therefore, it is certain that contamination picked up in the oxidation furnace and during transfer has been eliminated. However, the radiation resistance does not appear improved. Perhaps even better contamination control is necessary.

TABLE 12

Characteristics of MNS Transistors from Slice 1073
(with in situ thermal oxide interlayer)

No.	V_T	V_{on}	BV_{DSS}
2	5.3	15	60
3	5.3	15	60
6	5.9	16	55
10	5.7	16	55
85	6.4	16	53
86	6.4	16	60
87	6.6	17	61
90	4.5	15	60
91	5.6	15	57
92	6.8	19	30

TABLE 13

Temperature-Bias Test of V_T for Devices from Slice 1073
(with in situ thermal oxide interlayer)

No.	Bias Date.	Initial 2/1	-15 V 2/2	+15 V 2/3	-15 V 2/6	+15 V 2/7	-15 V 2/8	+15 V 2/9	-15 V 2/10
85		6.3	6.2	6.4	6.3	6.4	6.5	6.4	6.4
86		6.3	6.2	6.4	6 3	6.4	6.4	6.4	6.3
87		6.7	6.5	6.7	6.5	6.6	6.8	6.6	6.6
90		4.6	4.5	4.5	4.5	4.6	4.7	4.5	4.6
91		5 7	5.5	5.5	5.6	5 6	5.7	5.6	5.7

TABLE 14

Post-Irradiation Results from Slice 1073

No.	Initial V_T (V)	Bias During Irradiation (V)	Dose Rate (e/cm^2-sec)	Total Dose e/cm^2	Final V_T (V)
87	-6 5	-35	1×10^{10}	1×10^{13}	-18
90	-4.5	-35	1×10^{10}	1×10^{13}	-17 2

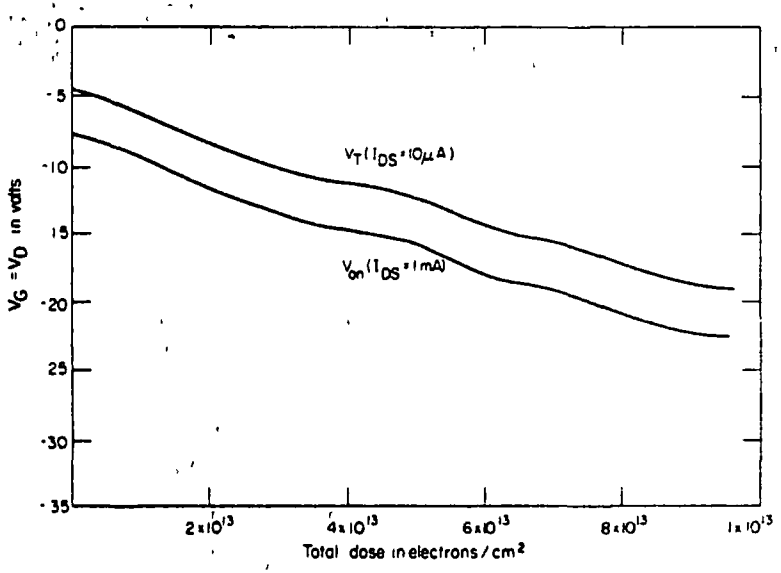


FIG. 5 Plot of V_T and V_{on} as a function of total dose at a dose rate of 1×10^{10} electrons/cm²-sec for MNS transistor 1073-90. The gate bias during irradiation was -35 V

F. IN SITU ETCHING

1. Purpose A further refinement in the control of the interface between the channel and the gate dielectric of the IGFET. Until now, an acid etch followed by quenching and rinsing in water caused the properties of the interface to be set before the in situ oxidation in the reactor, which was then followed by the deposition of the bulk of the gate dielectric in the form of silicon nitride It is clear that these properties depended on the details of the wet chemical reactions and quenching, on the time of storage, and on the cleanliness with which the slice was handled between its rinse and its introduction into the nitride reactor.

These uncertainties could be eliminated if the slice would experience its final surface preparation in the silicon nitride reactor immediately before the formation of oxide and nitride.

For this purpose, a hydrobromic acid gaseous etching technique was developed. It would be applied instead of wet chemical etch used heretofore, and it would be immediately followed by the established gate formation processes, without an exposure of the surface to the outside between process steps.

2. Variants. It was soon appreciated that this refinement could not simply be included as another step without affecting other process parameters. This problem resulted from the following circumstances In the present process, the gate dielectric is deposited over the whole region of the diffused source and drain and the channel area between them. This approach requires only loose control of the source and drain diffusion depth, since the gate metallization is designed to provide a sufficiently wide margin of overlap at both junctions to eliminate transconductance problems arising from lack of register between channel and gate electrodes When in situ etching is used to precede the deposition of the gate dielectric, the control of the etching rate of the silicon is insufficient. It was therefore decided to go back to an older processing sequence to permit the incorporation of the benefits of in situ etching into the device

The main feature of the approach is that the gate dielectric is not completely removed after source and drain junction formation. This means that the interface properties are determined when the first nitride layer is deposited. The control of the depth of the in situ etching is then not as critical, since the whole slice is affected uniformly and the diffusion occurs only afterwards. Unfortunately, this approach complicates device processing in other ways. The margin of overlap between gate electrode and channel region is now determined by the diffusion depth. To be sufficient, the diffused depth must be of the order of 8-10 μ. This requires a redesign of the source and drain masks to accommodate the added lateral distances of diffusion. In addition, the operation of the pilot line has to be modified to produce the altered depths of diffusion and gate etchback.

The benefits of in situ etching appeared well worth this complication. However, the only set of masks available that could be used for deep diffusion had a nonstandard geometry. It was decided to go ahead and establish the process modifications with this set of masks while the modified form of the standard set was being made.

The different geometry, and somewhat altered processing conditions, made a comparison of the in situ etching technique with previous variants difficult. In order to permit evaluation of the effect of in situ etching against wet chemical surface preparation, two series of slices were fabricated. They had identical processing parameters except at the very beginning.

One series was subjected to the wet chemical surface treatment before the in situ oxidation and silicon nitride deposition. The other series was cleaned by in situ HBr etching before oxidation and silicon nitride deposition. From then on, both series had identical processing.

The geometry of the IGFET used in the in situ etching experiments is shown in Fig. 6. Instead of a concentric circular geometry, source, gate and drain form parallel strips. The width of the gate is 0.0007 inches, its length 0.010 inches. The thickness of the gate dielectric is 1000 - 1200 Å, as in the circular device.

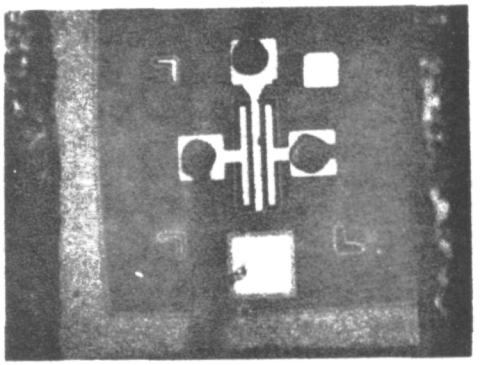


FIG. 6 Stripe geometry transistor.

3. Electrical results. Initial data from slice 10-102 are given in Table 15. This slice had a wet chemically prepared surface. The electrical data for slices 10-113 and 10-116, prepared by in situ etching, are given in the same table. The temperature-bias tests at GSFC confirmed the thermal stability of the devices, indicated in Table 16 Their behavior under irradiation is summarized in Table 17 The two different types of response to radiation of transistors from slice 10-102 are exemplified in Figs. 7 and 8. Figure 9 shows the behavior under irradiation of a transistor from slice 10-113.

4. Interpretation. Examination of Table 17 reveals a surprising fact: The transistors from slice 10-102 behaved in two distinctly different ways under irradiation. In order to bring this out, the data from the slice have been arranged so that devices of similar behavior are grouped together. During the actual data taking, the behavior was random, so that there was no correlation between date of packaging, or in the manner of testing, and the specific device behavior could be found. At this point, there are no indications how the difference in behavior should have arisen The reason for our interest is, of course, that one of the two groups exhibited some of the smallest changes in threshold voltage under irradiation that was found during the whole course of the contract. The group described first in Table 17 exhibited behavior that was quite similar to that found in previous devices. It was somewhat better than that exhibited by the "In situ oxidation" series, and not quite as good as some devices in the "packaging" series. The threshold voltages changed by about 6 6 V after a 10^{13} e/cm^2 dose, and by about -16 V after a 5 x 10^{13} e/cm^2 dose.

The second group, instead, had threshold voltage changes between +0.1 and -2.8 after 10^{13} e/cm^2, and on the average of -4 V after a 5 x 10^{13} e/cm^2 dose.

The devices from slice 10-102 represented an unetched control on the efficacy of the in situ etching on devices made later.

TABLE 15

Characteristics of MNS Transistors from Slices 10-102, 10-113, and 10-116

No.	V_T	V_{on}	BV_{DSS}
	(Slice 10-102 control for etch)		
86	7.5	22	60
88	7.8	20	65
92	7 5	20	82
94	8.2	25	86
2	6.9	20	58
3	7.5	22	70
5	9.3	25	85
6	9.0	26	85
7	8.3	24	82
8	6.0	22	75
	(Slice 10-113 in situ etched interface)		
18	6.3	20	88
19	6.7	25	87
22	7.9	24	94
24	6.4	22	92
25	6.2	25	86
71	8.1	32	94
73	7.5	23	80
	(Slice 10-116 in situ etched interface)		
18	8.4	22	100
19	8.9	24	95
20	8.6	23	92
23	8.7	25	86
25	9.0	24	70
68	9.0	24	90
70	8.9	24	94
72	8.8	28	88
73	8.9	24	65
74	8.8	23	85

TABLE 16

Temperature-Bias Test Data
(Slice 10-102 control for in situ etching)

No.	Bias Date	Initial 3/31	-15V 4/3	+15V 4/4	-15V 4/5	+15V 4/6	+15V 4/7	-15V 4/10	+15V 4/11	-15V 4/12	+15V 4/13
86		7.5	7.8	7.8	7 5	8.0	7.7	7.7	7.6	7.8	7.6
88		7.8	8.0	8.2	7.9	8.1	8.0	7.9	8.0	8.3	8.0
92		7.5	7.4	7.4	7.4	7.5	7.3	7.4	7.4	7.5	7.5
94		8.2	8.0	8.0	7.9	8.2	7.9	8.0	8.0	8.1	8.1

(Slice 10-113 in situ etched interface)

No.	Bias Date	Initial 4/26	+15 V 4/27	-15 V 4/28
71		8.1	8.2	8.2
73		7.5	7.6	7.6

(Slice 10-116 in situ etched interface)

	Bias Date	Initial 5/2	+15 V 5/3	-15 V 5/4	+15 V 5/5
68		9.0	9.2	9.0	9.2
70		8.9	9 1	8.9	9.0
72		8.8	9.0	8.8	9.0
73		8.9	9.1	8.9	9.2
74		8.8	9.0	8.8	9.0

TABLE 17

Results of Irradiation
(Dose Rate 1 x 10^{10} e/cm^2 Maximum Dose 5 x 10^{13} e/cm^2)

Device No.	Bias During Irradiation (V)	Initial V_T (V)	V_T After 1 x 10^{13} e/cm^2 (V)	V_T After Maximum Dose (V)
		(Slice 10-102)		
7	-10	-8.3	-17 2	-18 3
86	-10	-8 6	-14 4	-16 1
94	-10	-8 1	-16 8	-18 0
6	-20	-8.9	-23 1	-27 6
2	-20	-6 8	-13 8	-24 2
92	-20	-6.8	-13 0	-23 7
20	-20	-6 1	-	-21.5
3	-10	-5.0	-4 8	-4 1
88	-20	-4 8	-4 9	-2.3
3	-20	-4 1	-	-2 0
5	-20	-8 9	-6.1	-2 3
21	-20	-8 0	-	-3 7
22	-20	-7 5	-	-3 0
23	-20	-7 7	-	-2 2
24	-20	-8 8	-	-3 7
		(Slice 10-113)		
73	-20	-7 5	-14 9	-21.1
24	-20	-6 4	-11 9	-19 3
25	-20	-6 3	-13 6	-20 7
19	-20	-6 6	-12 7	-20 4
71	-20	-8 1	-15 7	-21 9
18	-20	-9 7	-12 7	-20 6

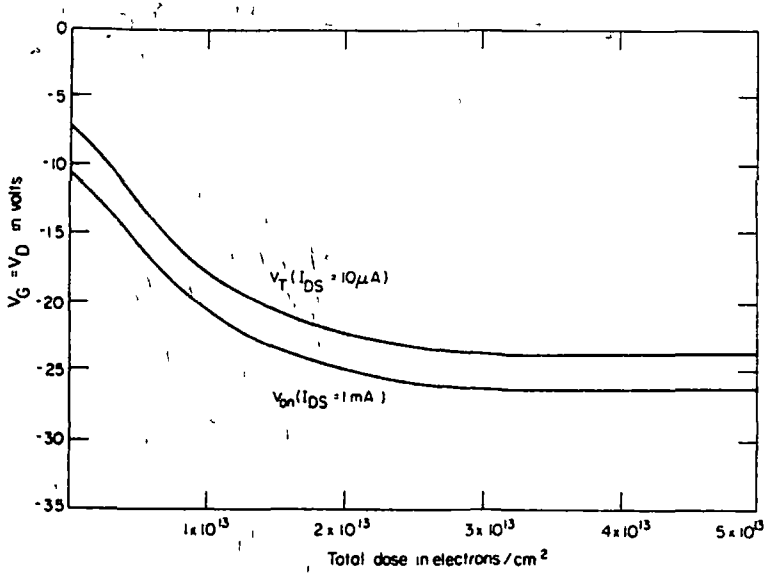


FIG. 7 Plot of V_T and V_{on} as a function of total dose at a dose rate of 1 x 10^{10} electrons/cm^2-sec for MNS transistor 10-102-92. The gate bias during irradiation was -20 V.

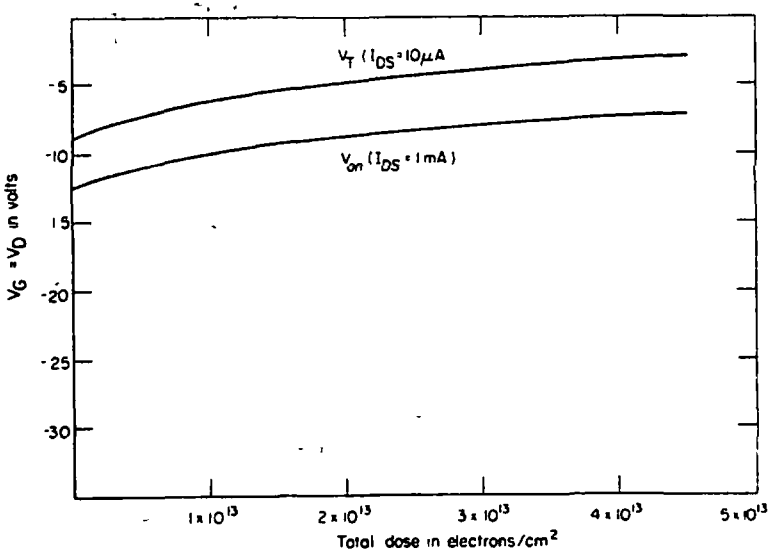


FIG. 8 Plot of V_T and V_{on} as a function of total dose at a dose rate of 1 x 10^{10} electrons/cm^2-sec for MNS transistor 10-102-5. The gate bias during irradiation was -20 V.

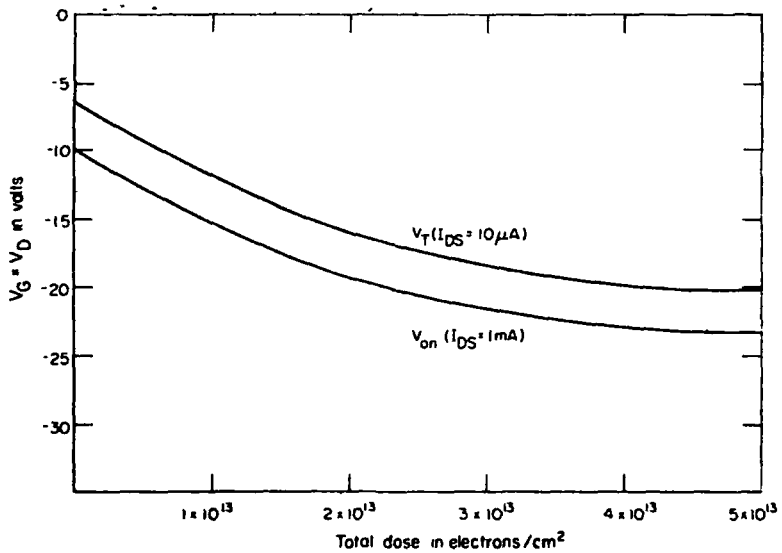


FIG. 9 Plot of V_T and V_{on} as a function of total dose at a dose rate of 1 x 10^{10} electrons/cm^2-sec for MNS transistor 10-113-24. The gate bias during irradiation was -20 V.

The behavior under irradiation of the etched devices then might have given a clue as to the reality of this behavior. Unfortunately, the results from slice 10-133 (Table 17) indicate that they related more closely to the first rather than the second group. Compared to the data of the first group, the in situ etched devices show somewhat smaller shifts and a smaller scatter of the results in general.

The positive result of this experimental series was the fact that some of the devices were more radiation resistant than those made previously. Since the surface treatment used in the successful devices did not differ at all from that used in the previous series ("Thermal Oxidation," "Packaging," "In Situ Oxidation"), it was surmised that the difference lay in the heat treatments that the interface experienced. Taking as an example the "In Situ Oxidation" series, the gate dielectric was formed right after the boron deposition. The drive-in of the boron then represented a heat treatment of the gate dielectric of two hours at 1200°C.

During the "In Situ Etching" series the interface of the gate dielectric was formed right at the outset. Therefore, this interface underwent a larger number of heat treatments.

The first one was associated with the deposition of the boron· ½ hour at 800°C. The next was the deposit of the second nitride layer about ½ hour at 900°C. Finally there was the drive-step, which was in common with the previous series. It was surmised that perhaps heat treatment did have something to do with the radiation resistance encountered in slice 10-102.

G. EFFECT OF HEAT TREATMENTS

1. Purpose. In order to confirm the effect of heat treatment, a device series was initiated where the gate dielectric interface did not experience any heat treatment at all. The results from this experiment could then be compared with the wet chemically prepared interface in the previous section, where the interface had undergone a series of heat treatments over 800°C.

TABLE 18

Characteristics of MNS Transistors from Slice 0-4
(no heat treatment of gate nitride)

No.	V_T	V_{on}	BV_{DSS}
1	2.6	11	60
2	3.4	11	65
3	3.4	12	60
4	2.8	11	48
5	3.2	14	60
6	3.4	14	45
7	3.4	12	55
8	2.4	11	65
9	3.8	12	55
10	4.4	13	50

TABLE 19

Temperature-Bias Test of V_T for Devices from Slice 0-4
(no heat treatment of gate nitride)

No.	Bias: Initial	+15 V	-15 V	+15 V	-15 V
	Date: 5/8	5/9	5/11	5/12	5/15
85	1.0	4.3	1.0	4.5	1.0
86	1.1	6.0	1.5	6.6	1.2
87	1.3	8.2	1.7	8.9	1.4
92	1.0	7.9	1.2	9.3	1.0
93	1.2	5.2	1.7	7.2	1.3

2. Variants. For this variant, the previously used annular geometry was used again, since it was easier to obtain complete overlay betwee shallow diffused junction and gate electrodes. The actual variant consisted of forming the gate dielectric after the boron drive-in had been accomplished. In this way the gate dielectric did not see any more heat treatment, except that associated with the sintering of the aluminum at 560°C, which is common to all approaches.

3. Electrical Results. The devices from series 0-4, which experienced no heat treatment over 570°C of the gate region, are characterized in Tables 18 and 19 The thermal instability of this series was confirmed at GSFC. It was decided not to do any radiation studies on these devices

4 Interpretation. The use of a gate dielectric that was not heat treated resulted in thermally unstable devices.

III. SUMMARY

During the course of the contract, 112 transistors were submitted for irradiation. These transistors formed part of eight experimental series. The devices made for four of these series exhibited large thermal instabilities, so that it appeared unnecessary to irradiate them.

All of the thermally stable devices had a 200 Å layer of oxide between the silicon nitride gate dielectric and the silicon surface. This layer was formed by thermal oxidation in a furnace before the deposition of the silicon nitride in a separate reactor, or it was formed in the silicon nitride reactor immediately before the silicon nitride deposition.

The four series permitted the evaluation of the effect of two packaging procedures, two ways of forming a thermal oxide interface, the presence and absence of in situ etches during the processing, and the effect of heat treatments.

In general, these MNOS devices had a higher radiation resistance than commercially available MOS transistors A comparison of the change in threshold voltage with total dose of representative MNOS devices with that of an MOS transistor is afforded by Fig. 10.

Table 20 summarizes the results obtained from all experiments. Each experimental series is identified by a number to permit a more detailed discussion. The effect of packaging is exemplified by data row Nos. 2 and 3. Unbaked and unsealed devices (#2) had a larger threshold voltage charge and data spread (ΔV_T = -8.1 ± 1.3 V) than vacuum baked and sealed devices (No. 3 ΔV_T = -3 2 ± 0.4 V). An in situ etch (No. 9) resulted in a lower threshold voltage change and spread (ΔV_T = -6.3 ± 1.3 V) than oxidation without in situ pre-etch (ΔV_T = 8.8 ± 2.9) in typical devices It is difficult to assess the effect of heat treatments and the effect of the particular oxidation process

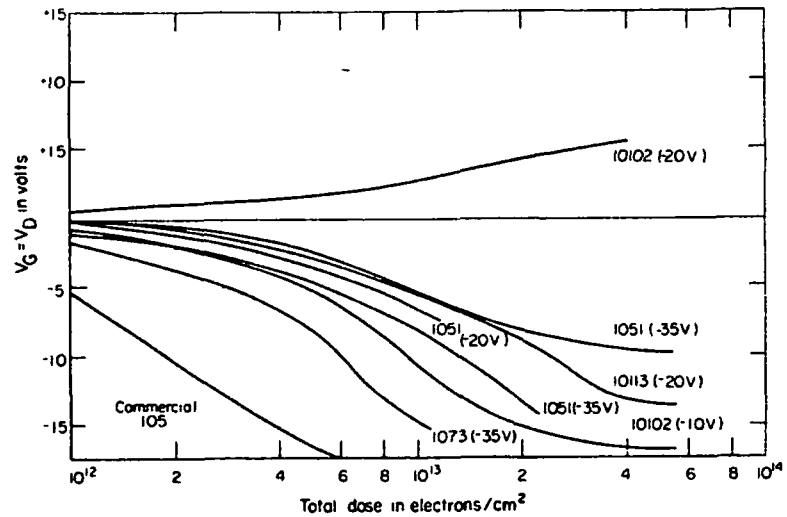


FIG. 10 Comparison of V_T vs total dose plots of representative MNS transistors. The gate bias of individual transistors is given in brackets behind the slice number.

TABLE 20

Summary of All Radiation Data

Process Key	Treatment	Packaged	Bias	ΔV_T for dose at 1×10^{13} e/cm^2	Thermal Stability
1	Furnace Oxide	SRRC	0	-3.2*	±4 V
2	" "	"	0	-8 1 ± 1.3	±1 V
3	" "	SSD	0	-3.2 ± .4	±1 V
4	" "	SSD	-10	-5.2	±1 V
5	Stripe geometry	SRRC	-10	-7.8 ± 1.3	±.1 V
6	" "	SRRC	-10	+0.9	±.1 V
7	Furnace Oxide	SSD	-20	-2.o	±1 V
8	Stripe geometry	SRRC	-20	-8 8 ± 2.9	±.1 V
9	Stripe & Etch	SRRC	-20	-6.3 ± 1.3	±.1 V
10	Stripe geometry	SRRC	-20	+5.2 ± .7**	±.1 V
11	Furnace Oxide	SRRC	-35	+2.6*	±4 V
12	Furnace Oxide	SSD	-35	-5.4 ± 1	±1 V
13	In situ Oxide	SRRC	-35	-12.1 ± .6	±.1 V

* dose was 2×10^{14} e/cm^2
** dose was 5×10^{14} e/cm^2

IV CONCLUSION

Present theory, as exemplified in publications by MacDonald and Everhart[8], and by Mitchell[9], utilizes a simple model for the threshold voltage change of an IGFET under irradiation. It is assumed that the radiation generates mobile electrons and immobile positive charges In an applied field, the electrons drift toward the positive side of the insulator, then cross the phase boundary and enter the external circuit An equal number of positive charges build up a field at the negative side of the insulator. The loss of electrons and the build-up of positive charge continues until the field due to the positive charges cancels that due to the applied voltage

In a p-channel enhancement transistor, the operating gate voltages are negative, so that the positive charges generated by radiation in the dielectric build up near the gate electrode Since these charges are farthest removed from the silicon interface their effect on the threshold voltage is relatively small. (Conversely, of course a positive gate voltage will cause the positive charge density to form at the silicon interface, with major changes in threshold voltage as a consequence.) Experimental evidence confirms the major conclusion of this model

The steady-state condition for this model is reached when the applied field is exactly cancelled by the accumulated positive charge This approach is certainly applicable to MOS transistors. In transistors utilizing silicon nitride, an additional factor has to be taken into account the higher conductivity of silicon nitride For this case, the steady-state condition must be formulated to mean that equal currents enter and leave the dielectric.

The electron current entering the silicon nitride layer is brought about by the sum of the field due to the applied negative voltage and the field due to the positive charge accumulation near that interface. At steady-state it is as high as that leaving the silicon nitride layer under the impetus

of the applied negative voltage minus the effect of the positive charge accumulation. This condition can occur long before the field due to the positive charges has become as large as that due to the applied negative voltage. Therefore a dielectric of a sufficiently high conductivity will result in a reduced positive charge density in the dielectric near the negative electrode. In the present MNS transistors, then, the observed lower threshold voltage changes could be explained by the higher conductivity of silicon nitride.

There is, unfortunately, a complicating factor in the present devices. That is the fact that the dielectric did not consist of silicon nitride throughout, but that it was a laminate of silicon nitride and silicon dioxide. This means that there are two regions of different properties that have to be considered separately The situation at the common boundary will then be determined by a continuity condition. Without going into the details of the mathematical analysis, the following can be stated Each region will separately obey the model for the single layer. That is, the silicon nitride layer will build up a positive charge near the negatively biased electrode, until the current generated by the field between electrode and positive charge into the silicon nitride equals the current generated by the ionizing radiation in the net field of applied bias and positive fixed charges. Separately, the thin oxide layer will also build up a positive charge in the negatively biased side of the layer, until the current crossing the silicon nitride boundary is equal to that crossing the silicon boundary. The continuity condition between the two layers is then the equality of the currents leaving the silicon nitride layers and entering the silicon oxide layer at the common interface. The steady state currents in each layer independently, however, are bound to be different. They each depend essentially on the energy required for pair formation, the absorption coefficient for the particualr types of radiation, and the lifetime of excess carriers, in each separate material. If the independent steady state currents are different, but only one magnitude is permitted by the continuity condition then charge accumulation arising from the large steady-state current must occur at the silicon nitride-silicon oxide interface.

In going from a single layer to a double layer, then we pass from a situation where charges accumulate only in one region to a situation where charges accumulate essentially in three regions. In an MNOS transistor with a negative bias applied the following will occur. Assuming no stored charges at the outset, applied fields will be constant and nearly equal in both insulator regions The conductivity under radiation will be higher in the nitride region than in the oxide region so that a positive charge accumulation will form quickly near the gate electrode This charge will neutralize a large part of the applied voltage, so the field will be small in the oxide region. This will result only in a small amount of positive charge formed in the oxide near the nitride interfaces Simultaneously, however, the larger current from the nitride layer will result in an accumulation of negative charge on the nitride side of the oxide-nitride interface since the current in the oxide is smaller. It is therefore quite conceivable that negative charge of such a density builds up that it neutralizes the field due to the positive charges almost completely or that it is even larger in magnitude. In the latter case, of course the threshold voltage of the transistor would be positive.

This model can explain all results obtained with the MNS and MNOS transistors. The small threshold voltage changes obtained with the first MNS transistors were undoubtedly due to the ease with which electrons could flow from the gate electrode into the silicon nitride, which lead to the build-up of only a small positive charge density under steady-state conditions The good results obtained with well-controlled packaging conditions are probably due to the same effect The changes in theshold voltage in the positive direction, which half of the devices from slice 10-102 exhibited, indicate the accumulation of a preponderant amount of negative charge at the silicon nitride-silicon oxide interface The fact that MNS and MNOS devices exhibited smaller changes in threshold voltage than commercial MOS devices can be explained by the separate or combined operation of a lower positive charge density due to a higher current density of electrons entering the silicon nitride at the gate electrode, and the build-up of a negative charge at the nitride-oxide interface

These explanations open up intriguing possibilities of constructing MNOS devices that exhibit no changes under irradiation. This would involve the metal-silicon nitride interface properties such that a sufficiently high current density could flow into the silicon nitride to neutralize the positive charge generated In addition, the conduction property of silicon nitride under irradiation could be adjusted in such a manner that the negative charge accumulated at the nitride-oxide interface would just neutralize the effect of the remaining positive charge. These conditions should not be too difficult to realize experimentally. Highly conducting silicon nitride can be made under controlled conditions to provide the desired gate electrode-nitride interface. The bulk conductivity of silicon nitride under ionizing irradiation can also be measured using x-rays. Data of this nature could then be used to adjust the conductivity of silicon nitride to the desired value by the incorporation of impurities such as excess silicon to increase it, or oxygen to decrease it.

The location of stored charges can be ascertained by the well established step-etch technique. In the course of this technique, small thicknesses of the insulator are removed by etching, followed alternately by the measurement of the threshold voltage of the device A plot of the measured threshold voltage vs thickness then permits the determination of both magnitude and location of both positive and negative charges.

The three experimental series indicated will lead to the design of an MNOS transistor where both positive and negative stored charges formed under ionizing radiation will neutralize each other so that there is no net change in the threshold voltage of the transistor.

V REFERENCES

1. N. C. Tombs, H. A. R. Wegener, R. Newman, B. T. Kenney, and A. J. Coppola, "A New, Insulated-Gate Silicon Transistor," Proc. IEEE (Letters) 54, 87-89 (January 1966).

2. N. C. Tombs, H. A. R. Wegener, R Newman, B. T. Kenney, and A. J. Coppola, "A New, Insulated-Gate Transistor," 1966 International Solid State Circuits Conference, Digest of Technical Papers 9, 58-51.

3. F. Gordon, Jr. and H E. Wannemacher, Jr., Unpublished data, November, 1965.

4. F. Gordon, Jr. and H. E Wannemacher, Jr., "The Effects of Space Radiation on MOSFET Devices and Some Application Implications of those Affects", Presented at the Annual Conference on Nuclear and Space Radiation Effects, 18-21 July 1966, Palo Alto, California.

5. A. G. Stanley and H. A. R. Wegener "Effects of Electron Irradiation of Metal-Nitride-Semiconductor Insulated-Gate Field-Effect Transistors," Proc. IEEE (Letters) 54, 784-785 (May 1966).

6. A G. Stanley, "Comparison of MOS and Metal-Nitride-Semiconductor Insulated-Gate Field-Effect Transistors under Electron Irradiation," Presented at the Annual Conference on Nuclear and Space Radiation Effects, 18-21 July 1966, Palo Alto, California.

7. E. H. Snow, A. S. Grove, and D. J Fitzgerald, "Effects of Ionizing Radiation on Oxidized Silicon Surfaces and Planar Devices", Proc. IEEE 55, 1168-1185 (July 1967).

8. N. C. MacDonald and T. E. Everhart, 'An Investigation of Electron Beam Irradiation Effects on Metal-Oxide-Semiconductor Transistors", Report No. ERL-66-16-Pt-1, Electronics Research Lab, College of Engineering, University of California, Berkeley (September 1966).

9. J. Peter Mitchell, "Radiation-Induced Space Charge Buildup in MOS Structures", IEEE Trans on Electron Devices 14 No. 11 (November 1967).

NEW TECHNOLOGY APPENDIX

After a diligent review of the work performed under this contract, no new innovation, discovery, improvement or invention was made.