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STUDY OF FAILURE MODES OF MULTILEVEL LARGE SCALE INTEGRATED CIRCUITS

November 1967

Prepared Under Contract NAS12-544
by
Philco-Ford Corporation
Microelectronics Division
Blue Bell, Pennsylvania

Electronics Research Center

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NAS12-544

National Aeronautics and Space Administration
Failure Mechanisms Branch
Qualifications and Standards Laboratory
Components Research
Cambridge, Massachusetts 02139

Because it is anticipated that this program will be continued, this report, which is a final report on the work done on Contract No. NAS 12-544, dated April 15, 1967, is termed an Interim Report. It covers the study program performed between April 15, 1967 and October 14, 1967.

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STUDY OF FAILURE MODES IN MULTILEVEL LARGE SCALE INTEGRATED CIRCUITS

Philco-Ford Corporation
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SUMMARY

Empirical and theoretical studies have improved the understanding of the fundamental electrical properties of the Si-SiO_2 interface of structures having a dielectric layer over the delineated metal layer in multilevel microcircuit structures. A useful model has been developed which provides an over-all view of all the influences on these electrical properties. A number of oxide layers of various materials and deposition processes were evaluated for their possible use as second-layer insulation materials for multilevel LSI circuitry. Vapor-plated SiO_2 and vapor-plated mixed SiO_2-Al_2O_3 were found to be the most promising materials. Feasibility has been demonstrated for a set of test structures, equipment, and techniques for evaluating various insulator materials and deposition processes. Experimental data comparing the immobile and mobile charge densities in various types of oxide layers were taken. The effects of surface ions were studied. Data were recorded on the migration of contaminants from regions

adjacent to regions beneath metal layers. An extensive array of data has been compiled on both n-on-p and p-on-n test structures, both with and without a vapor-plated SiO_2 second insulator layer. The behavior of surface ions and its dependence on the type of outer surface of the oxide were studied.

Based on these preliminary and feasibility studied, a set of recommendations has been prepared for a more complete program.

INTRODUCTION

Large scale integration (LSI) is rapidly being developed to improve the reliability, performance and cost effectiveness of microcircuitry. LSI takes advantage of recent technological developments for decreasing the dimensions of microcircuit elements and for building microcircuit configurations with several layers of insulation and conductors. In addition to the performance improvements - higher speed, better noise immunity and lower operating power levels - the size, weight, and ease of maintenance are improved.

The reduction in the size of the circuit elements and in the length of interconnections decreases the probability that an imperfection in either the silicon or the insulator material will be included in a critical part of the circuit. The number of bonded interconnections per function performed is decreased and this decreases the number of bond failures - one of the main causes of failure in currently available integrated circuits.

The fabrication of LSI circuits requires a number of new materials and fabrication processes. For example, the first layer of insulation is generally thermally grown SiO_2. Thermally grown oxide was chosen for the first insulator layer to obtain a low density of states at the silicon surface.

The second layer of insulator material must cover the first layer of metal interconnections, and therefore a technique other than thermal oxidation must be used. The process by which the second insulator layer is formed must be compatible with the processes and materials used for forming the microcircuit. For example, if the first layer metal is aluminum, the structure cannot be heated above the aluminum-silicon eutectic temperature (577°C) during the formation of the second layer of insulation. The material and process chosen for the formation of the second layer must not contaminate the oxide with mobile ions (sodium ions or protons) that can drift into the first layer of oxide. It is desirable that the second layer act as a protective barrier to such contamination. The second layer must also be free from pinholes to prevent shorting at the crossover points between first and second layer metallic interconnections.

In general, the potential reliability and performance advantages of LSI must not be compromised by failure modes arising from the additional steps required to obtain multilevel metalizations. Such failure modes might be entirely new or they might be previously recognized failure modes that appear more frequently. The probability of failure may increase because of a decrease in stability or because of a change in

the initial characteristics which provides less tolerance for instability.

It was the objective of this study program to develop fundamental information to improve the understanding of the possible failure modes in LSI circuitry. This study included the effects on performance and reliability of the insulator layers; it did not include problems (shorts, opens, noisy contacts) associated with the metallic layers.

The metallic material was limited to aluminum. Aluminum is an attractive one-metal system which has a well developed technology. It promises to remain the most widely used metal for the conductor layers in both single and multilevel microcircuits.

The deposition processes that were considered include vapor-plated or pyrolytically formed, evaporated, and r-f sputtered oxides. Other deposition processes, such as chemical, thermal or electrochemical oxidation of the metal layers, were not studied in this program for a number of reasons. Step heights at the edge of metalized regions would be increased beyond desirable bounds by an oxide preparation process that selectively oxidizes the metal. An electrochemical process would present some difficult contacting problems. A suitable aqueous chemical process has not yet been developed.

The approach taken in this program combined both theoretical and experimental studies of the fundamental electrical properties of the insulator-silicon interface. The emphasis was on the effects on these properties of the materials and processes used to build structures having several levels of insulator material. The fundamental properties that were studied include the surface potential of the silicon, the surface recombination velocity, the carrier mobility in an inversion layer, and both slow and fast states.

The results of this program can be applied to predict and understand the reliability and performance of both MOS and bipolar arrays.

This report covers Phase I of this program. The work was performed during the period from April 15, 1967 to October 14, 1967. The objectives of this phase were exploratory - to identify the problems and to develop test structures, test equipment, and test procedures for studying the mechanisms associated with failure modes of multilevel LSI structures.

THEORETICAL APPROACH

Literature Review

A literature review, conducted on a related company-sponsored program, provides a useful basic theoretical understanding of the various types of charge that may influence the electrical properties of the oxide-silicon interface (Ref. 1).

Model of Charge Distribution

Based on the work in the published literature and our own experience, we have developed a useful model that facilitates the discussion and understanding of the basic causes of variations in the performance and reliability of LSI circuitry. A schematic drawing of this model is shown in Figure 1.

The fundamental electrical properties of the insulator-silicon interface are:

1. Surface potential,
2. Surface recombination velocity,
3. Carrier mobility in the inversion layer,
4. Effects of slow and fast states.

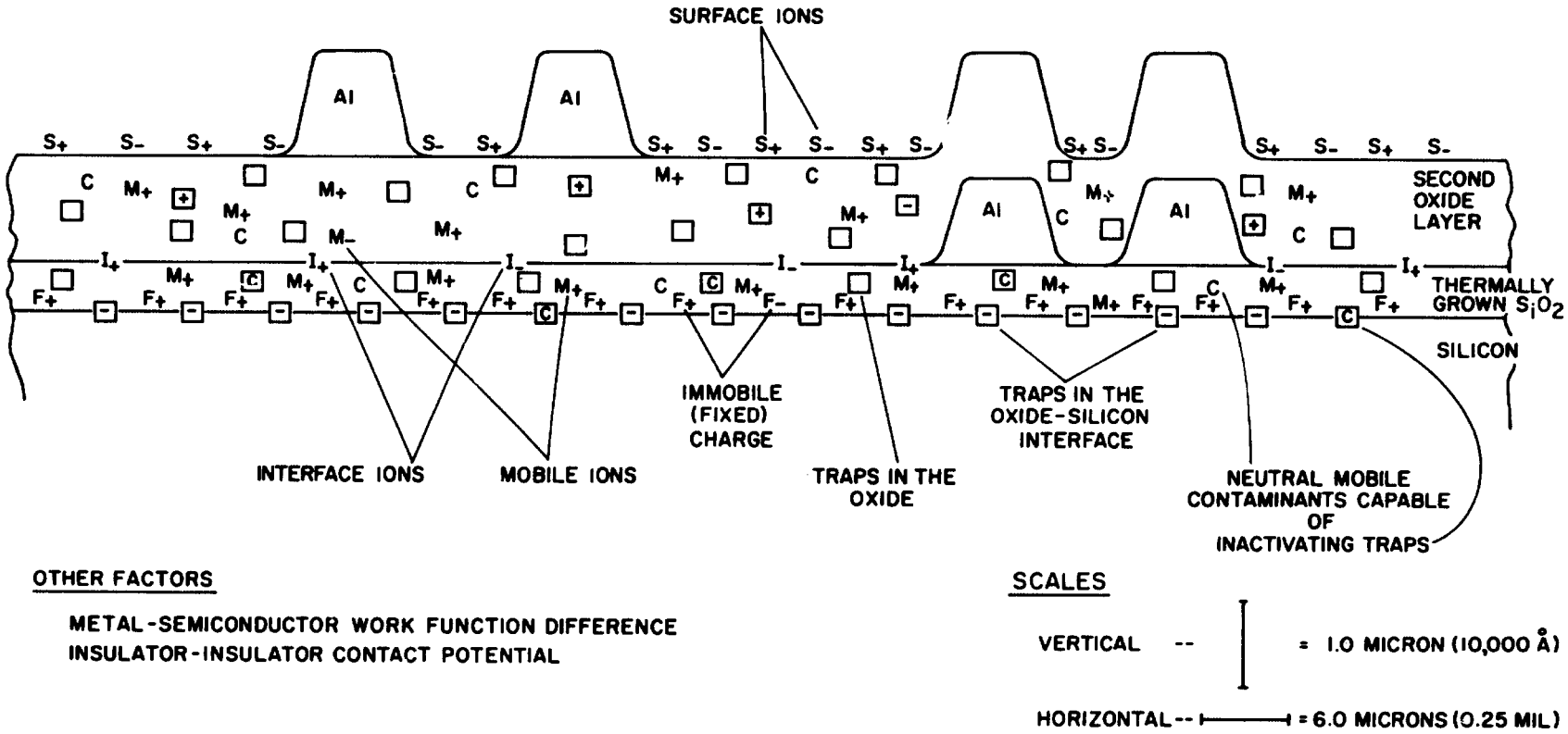


Figure 1. Factors influencing silicon surface potential.

The surface potential is determined by the total charge distribution in the oxide and its relative proximity to the silicon and to other conducting layers. It affects the formation of channels, diode leakage current, diode breakdown voltages, and the threshold voltage of MOS transistors. Instabilities in the surface potential make for unreliable device characteristics.

The surface recombination velocity depends on the density of recombination centers at the insulator-silicon interface and on the surface potential. The current gain of a bipolar transistor and the leakage current of a reverse biased diode are sensitive functions of the surface recombination velocity.

The carrier mobility in the inversion layer depends on the density of scattering sites at the insulator-silicon interface and on the density of carrier immobilizing traps. The transconductance of MOS transistors is proportional to the carrier mobility.

Slow states in the oxide cause device instability due to a change in the surface potential caused by a gradual change in the number of charged states in the oxide. The direction of the surface potential change can be understood as follows. A positive voltage on the metal electrode would repel holes

or attract electrons in states and thereby make the surface potential of the silicon more positive.

Fast states at the silicon-oxide interface are capable of immobilizing carriers in an inversion layer. They increase the threshold voltage of MOS transistors because they must be filled during the formation of the inversion layer before the channel can conduct current.

Charts I, II, and III summarize these phenomena. The fundamental properties of the $Si-SiO_2$ interface (surface potential, surface recombination velocity, inversion-layer carrier mobility, and the effects of both slow and fast states) very significantly influence the behavior of both bipolar and MOS devices. These fundamental properties affect device parameters as indicated in Chart I. The fundamental properties of the $Si-SiO_2$ interface depend on the factors listed in Chart II. The factors which affect the fundamental properties of the $Si-SiO_2$ interface are dependent on variations in the production cycle shown in Chart III.

CHART I

Effects of Fundamental Interface Properties

Properties	Effects
Surface potential	Channel formation Diode leakage current Diode breakdown voltage Threshold voltage of MOS transistors Stability of devices
Surface recombination velocity	Diode leakage current Beta of bipolar transistors
Carrier mobility	Transconductance of MOS transistors
Effects of slow and fast states	Stability of devices Diode leakage current Beta of bipolar transistors Transconductance of MOS transistors

CHART II

Factors Affecting Fundamental Interface Properties

Immobile charge in the oxide,

Mobile charge (sodium, protons) in the oxide,

Ions between insulator layers,

Ions on the surface of the insulator,

Traps at the oxide-silicon interface,

Traps in the oxide,

Mobile contaminants (water, hydrogen) that have no charge of their own but can alter the density of the immobile charge, and of traps and generation-recombination centers,

Insulator-insulator contact potentials and metal-semiconductor work function differences.

CHART III

Production Cycle Variations Affecting

Fundamental Interface Properties

Heat and annealing treatments that affect immobile charge densities;

The moisture and hydrogen content that affect immobile and trapped charge densities;

The density of mobile alkali ions or protons;

Phosphorus or hydrophobic surface treatments that influence the density and mobility of surface ions;

The techniques by which the oxide is formed which may influence the immobile and trapped charge densities;

The lack of cleanliness or reproducibility of processes or materials.

Influences on Charge Distribution

The immobile charge density has been reviewed by Deal et al. (Ref. 2). It is independent of applied voltage, is stable at temperatures below 250° C, and is located within 200 Å of the silicon interface. It depends on the crystalline orientation of the silicon and on the final ambient gas and temperature of a thermal oxidation process.

Heat treatments at temperatures of 300 to 600° C in water or hydrogen can increase the immobile charge density. The immobile charge density can also be increased by applying negative (metal relative to silicon) fields at temperatures higher than 250° C. The immobile charge appears to be intrinsically associated with the SiO_2-Si interface due to excess silicon ions in the region of the oxide within 200 Å of the silicon. Beyond this, it also depends on the presence of water or hydrogen.

Mobile ions in SiO_2 layers have been shown (Refs. 3,4,5,6,7) to be sodium ions and protons. The migration of mobile ions in the insulator layers, in regions underlying metal layers changes the surface potential of the silicon. Mobile ions have been a very important cause of instability in microcircuitry having a single insulator layer. In multilevel structures, the problems of preventing contamination

by sodium or protons are increased with each additional layer, material, and process.

Mobile ions at the insulator-insulator interface must be considered as a possible cause of instability. The available information at this time is insufficient to establish the level of importance of interface ions.

Ions at the surface of the insulator have been shown to be important by various investigators (Refs. 8,9, 10, 11, 12, 13, 14). The density of surface ions can be predicted from the available data on the conductivity and carrier mobility on glass surfaces. The surface conductivity of fused quartz is reported (Ref. 15) to vary between 10^{-15} and 10^{-9} ohms as the relative humidity varies between 0 and 100%. In water, the ionic mobility of H^+ is 0.0036 $cm^2/Vsec$ and that of OH^- is 0.00205 $cm^2/Vsec$ at 25° C (Ref. 16). These values can be used to estimate that this surface ion density is more than 10^{12} ions/cm^2 at 100% relative humidity at 25° C. Figure 2 shows the surface charge density that will invert silicon having a given volume dopant density. It shows that a surface charge of 10^{12} ions/cm^2 is capable of inverting silicon having a bulk dopant density of more than 10^{17} atoms/cm^3. The density of surface ions would be expected to depend

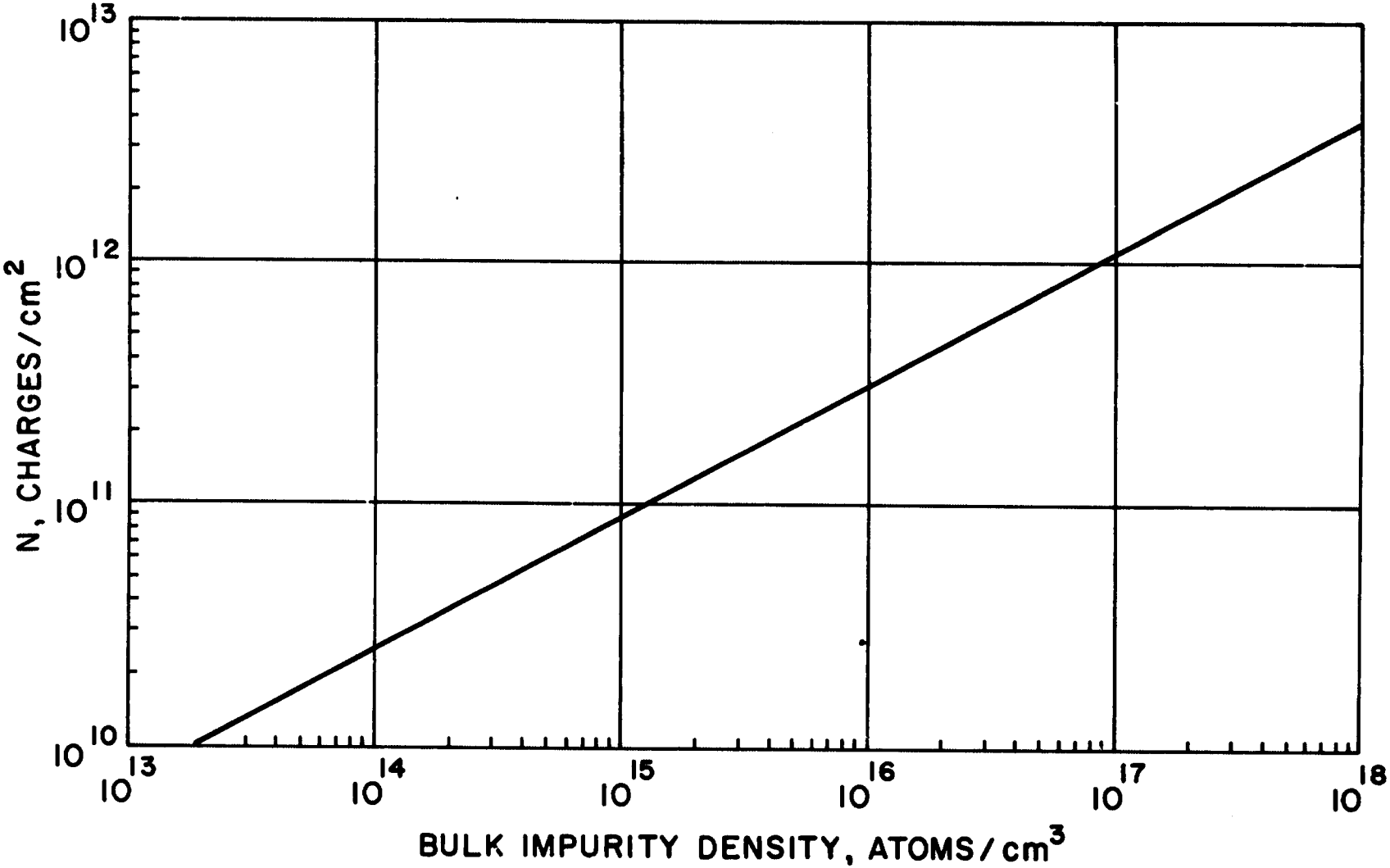


Figure 2. Effective oxide charge density, N, necessary to invert silicon.

on the outermost dielectric material, on how the material was formed, and on how it was treated after it was formed. For example, phosphosilicate glasses are hygroscopic and can be expected to enhance the mobility of surface ions. On the other hand, treatments designed to render the surface hydrophobic might decrease the effects of mobile ions on the surface. Surface ionic behavior depends strongly on ambient conditions which in turn are influenced by such factors as the package hermeticity. The behavior of surface ions would also be expected to depend on the structural design of the device and on the electric field strength along the surface.

The density of traps depends on how the oxide is formed on the silicon. It can be modified by the diffusion of hydrogen or water related species into the oxide. It may be influenced by stresses caused by mismatches in the thermal coefficients of expansion.

Mobile contaminants, such as water or hydrogen, affect the immobile charge density and the effective trap density.

Metal-semiconductor work function differences and insulator-insulator contact potentials also affect the surface potential.

EXPERIMENTAL APPROACH

Introduction

The experimental approach in this program included four main areas of effort. In the first, a number of experiments were performed with existing test pattern mask sets to generate and develop as much information as practical early in the program. In the second, based on the literature review and on the results of the early experiments, a set of masks was designed and built to make it possible to extend our ability to extract all of the fundamental information concerning the electrical properties of the insulator-semiconductor interface. In the third, test equipment was set up for evaluating the test structures. In addition, a special mask was developed so that a metal pattern provides the means of measuring discrete transistors in a chip from a production line of commercial microcircuits. From this the effects of different second layer insulators can be studied on structures that have been subjected to the complicated series of steps used to fabricate complex, commercially available, bipolar microcircuits. In the fourth, a body of data was collected using the test structures and test equipment.

There are three practical processes by which oxides can be deposited over insulator or metal layers - vapor plating or pyrolytic deposition, r-f sputtering, and evaporation. Oxides prepared by each of these processes were evaluated in this program. The oxide materials that were evaluated were SiO_2, Al_2O_3, mixed SiO_2-Al_2O_3 and titanium oxide. The study of Al_2O_3-containing layers for this application has been reported at several recent meetings (for example, see Ref. 17).

Silicon monoxide and silicon nitride were considered but were not evaluated because our experience and that reported in a large body of literature, shows that these materials are difficult to prepare with reproducible properties, probably because of difficulties involved in reproducing the stoichiometry of the layers. Also, these types of insulators are not currently being used in LSI.

Preliminary Evaluations of Insulator Layers

Preliminary evaluations were made of materials and processes by measuring the capacitance-voltage (C-V) relationship of MOS capacitors after each of a series of of steps in which a bias was applied at a controlled temperature to drift any mobile charge in the oxide.

These measurements yielded the density of immobile charge and the densities of mobile charge at 300°C and at room temperature. To the degree that any trapped charge density exceeds the mobile charge density, trapped charge densities were measured. The apparatus and test structures used for this work were described in our final report, "Design, Development, Fabrication and Delivery of Improved MOS Transistors," dated June 1966, on Contract #NAS8-11926 with the National Aeronautics and Space Administration, Huntsville, Alabama.

The immobile charge density is the effective charge density after drifting the mobile charge at 300°C under an applied voltage of -12 volts (the voltage polarity is that on the metal) for 2 minutes. The bias was always maintained during the cooling time and up to just before the C-V measurements were taken. To determine the mobile charge densities, the effective charge density was measured both after drifting the mobile charge with an applied voltage of +12 volts for 2 minutes at 300°C and again after drifting with an applied voltage of -12 volts for 5 minutes at room temperature. The change in the effective charge density during the drift at room temperature is the mobile charge at room temperature. The change in the effective charge density during the drift at

+12V, 300°C minus the change during the room temperature drift is the mobile charge at 300°C.

In the remaining part of this subsection, we describe the experimental results of our evaluation of oxides made with various combinations of forming process and material.

Thermally grown SiO_2 on silicon. - To provide reference levels for the types of charge reported below, we note that a thermally grown layer of SiO_2 on silicon (grown at 1200°C in dry O_2 to a thickness of 2000 Å) would typically have

2×10^{11} immobile charges/cm^2,

0.5×10^{11} mobile charges/cm^2 at 300°C,

0.1×10^{11} mobile charges/cm^2 at 25°C.

Vapor-plated SiO_2 on silicon. - The following tabulation shows the measured charge levels that were found in samples of SiO_2 that were deposited on bare silicon by vapor plating. The deposition was made at 400°C with the reaction

$$SiH_4 + 2O_2 \longrightarrow SiO_2 + 2H_2O.$$

Sample #	Oxide Thickness	Immobile Charges/cm^2	Mobile (300°C) Charges/cm^2	Mobile (25°C) Charges/cm^2
284	6000 Å	5.0×10^{11}	2.0×10^{11}	0.1×10^{11}
285	6000	5.0	2.4	<0.1
504	2000	9.9	1.3	0.4
505	2000	10.7	1.3	0.1

Vapor-plated SiO_2 on thermally grown SiO_2. - Vapor-plated oxides were deposited on thermally grown oxide layers and the following results were measured:

Sample#	Oxide Thickness Lower Layer	Oxide Thickness Upper Layer	Immobile Charges/cm^2	Mobile (300° C) Charges/cm^2	Mobile (25° C) Charges/cm^2
300	6000Å	7000Å	9.4×10^{11}	5.6×10^{11}	0.1×10^{11}
301	6000	7000	8.1	6.6	<0.1
532	2000	5000	4.5	2.0	<0.1

Vapor-plated SiO_2 with phosphosilicate layer on thermally grown SiO_2. - Other samples were prepared having a layer of phosphosilicate glass (1250 Å) between the 7000 Å of vapor-plated oxide and the 6000 Å of the underlying thermally grown SiO_2. These data should be compared with those for the other halves of the same wafers (300 and 301 above), which had a higher level of mobile ions than is normally present.

Sample #	Immobile Charges/cm^2	Mobile (300° C) Charges/cm^2	Mobile (25° C) Charges/cm^2
300A	4.0×10^{11}	0.4×10^{11}	0.2×10^{11}
301A	4.3	0.3	<0.1

R-F sputtered SiO_2 on silicon. - SiO_2 layers were r-f sputtered to a thickness of 5000 Å on bare silicon. The charge densities measured were:

Sample #	Immobile Charges/cm^2	Mobile (300° C) Charges/cm^2	Mobile (25° C) Charges/cm^2
528A	4.0×10^{11}	24×10^{11}	0.3×10^{11}
529A	2.1	32	2.8

The source target of the SiO_2 was analyzed to have 5 ppm of sodium. To decrease the mobile charge (300° C), other source material having less than 0.04 ppm of sodium was ordered. This was not available during the time period covered by this report.

R-F sputtered SiO_2 on thermally grown SiO_2. - SiO_2 layers were r-f sputtered on 2000 Å of thermally grown SiO_2 to a total thickness of 6300 Å. The capacitance-voltage relationship on MOS capacitors was so poorly shaped that the data are difficult to interpret. It appears that the results are similar to those for the sputtered SiO_2 on silicon.

Vapor-plated Al_2O_3 on thermally grown SiO_2. - We vapor-plated Al_2O_3 layers 3000 Å thick on 2000 Å of thermally grown SiO_2. We found (in Sample #507) an immobile charge density of 5×10^{11} cm^{-2} and a mobile charge density of 20×10^{11} cm^{-2}. The charge densities in a similarly vapor plated 3000 Å thick layer of Al_2O_3 on bare silicon could not be measured because the capacitors were not able to support 12 volts at 300° C.

Evaporated Al_2O_3 on thermally grown SiO_2. - An Al_2O_3 layer was evaporated by means of an electron beam to a thickness of 3000 Å on top of 2000 Å of thermally grown SiO_2 (Sample #510). The measured immobile charge density was 4×10^{11} negative immobile charges/cm^2. It is important to note that this polarity of the immobile charge is unusual; in nearly all other oxides examined by us or reported by others, it is positive. From a quarter to a half of this immobile charge may be due to the insulator-insulator contact potential which was reported by Nigh et al. (Ref. 18) to be in the range of 1.0-2.0 volts. The measured mobile charge in our samples is roughly 20×10^{11} cm^{-2} at 300° C. There appeared to be no mobile charge at room temperature.

An attempt was made to measure the charge densities in a similarly evaporated 3000 Å thick layer of Al_2O_3, on bare

silicon, but the capacitors were unable to support the 12 volts at 300°C.

At present we do not consider evaporated layers to hold much promise, both because of the high density of mobile charge and because of the low breakdown voltage.

Vapor-plated mixed Al_2O_3 and SiO_2. - Because mixed Al_2O_3 and SiO_2 has a faster etch rate than Al_2O_3 and because a 1:1 mixture of Al_2O_3 and SiO_2 is reported to have a coefficient of thermal expansion approximately matching that of silicon, we prepared samples of vapor-plated mixed (actually an amorphous solid solution) of Al_2O_3 and SiO_2. The composition was estimated to be 60% Al_2O_3 and 40% SiO_2, based on a measured density of 3.2 g/cc and a measured index of refraction of 1.56.

Sample #521 contained 3000 Å of vapor-plated mixed Al_2O_3 and SiO_2 on bare silicon. The flatband voltage was unstable between +80 V and -10 V at 300°C. Our calculations indicated that there are 80×10^{11} negative immobile charges/cm^2 and 90×10^{11} mobile charges/cm^2 (300°C). These calculations are based on an assumption that the mobile charge is all positive. It may be that an undeterminable amount of the mobile charge is negative. It should be recognized that this lack of knowledge of the exact species of charge is not as important as

are the values of the range and limits of the effective charge density, which are known.

Sample #519 consisted of 2000 Å of vapor-plated mixed SiO_2 and Al_2O_3 on 2000 Å of thermally grown SiO_2. In this case, the flatband voltage shifted only between +3 and -3 volts. This indicates that most of the mobile ions in the vapor-plated Al_2O_3-SiO_2 mixture are not mobile in thermally grown oxide, and that these mixed oxides are comparatively stable.

Titanium oxide over thermally grown SiO_2. - It has been reported (Ref. 19) that titanium improves the insulation properties of dielectric layers by absorbing reaction products and impurities to improve the lifetime of devices. We measured charge densities in a sample (#540) prepared as follows:

1. SiO_2 was thermally grown to 3000 Å in dry O_2 at 1200°C;
2. Titanium was evaporated to a thickness of 2000 Å;
3. The wafer was baked at 500°C for 20 minutes in dry N_2 to oxidize some of the titanium by reaction with the SiO_2;
4. The metallic titanium was etched away in hot HCl, leaving the titanium oxide;

5. Aluminum was evaporated and delineated into MOS capacitors.

We found 2.8 x 10^{11} immobile charges/cm^2, 18 x 10^{11} mobile charges/cm^2 at 300°C, and 29 x 10^{11} mobile charges/cm^2 at room temperature.

Summary. - In summary, MOS C-V measurements were made on vapor-plated, r-f sputtered and evaporated layers of SiO_2, Al_2O_3, mixed Al_2O_3- SiO_2, and titanium oxide. The data summarized in the following table show that vapor-plated SiO_2 and vapor-plated mixed SiO_2-Al_2O_3 have the lowest immobile and mobile charge densities, and are therefore preferred for use as second-layer dielectric materials for multilevel circuits. However, r-f sputtered oxides should not yet be ruled out because the use of purer source materials may reduce the mobile charge density.

Measured Charge Densities

in Various Types of Oxides

Oxide Type	10^{11} Charges/cm^2 Immobile	Mobile (300°C)	Mobile (25°C)
Thermally grown SiO_2 on Si	2	0.5	0.1
Vapor-plated SiO_2 on Si	5	2	0.1
Vapor-plated SiO_2 on thermally grown SiO_2 on Si	8	5	0.1
Vapor-plated SiO_2 on phospho-silicate layer on thermally grown SiO_2	4	0.4	0.1
R-f sputtered SiO_2 on Si	3	28	1.0
Vapor-plated Al_2O_3 on thermally grown SiO_2 on Si	5	20	---
Evaporated Al_2O_3 on thermally grown SiO_2	-4	20	---
Vapor-plated mixed Al_2O_3-SiO_2 on Si	-80	90	---
Vapor-plated mixed Al_2O_3-SiO_2 on thermally grown SiO_2 on Si	-1.5	3	---
TiO_2 on thermally grown SiO_2	3	18	29

Migration of Contaminants from Regions Adjacent to Regions Beneath Metalized Areas

An experiment was conducted to determine what effects a vapor-plated oxide overlying a metal pattern on thermally grown oxide has on the properties of the oxide-silicon interface beneath the metal. The test structure used was a MOS capacitor formed into a resistor pattern with a linewidth of 1 mil. Three types of samples were prepared for the experiment. One group of samples had only a layer of 2000 Å of thermally grown SiO_2 under the metal; a second group had a layer of 5600 Å of vapor plated oxide between the metal and the silicon; and a third group had a 2000 Å layer of thermally grown SiO_2 between the silicon and the metal, and 5600 Å of SiO_2 vapor plated over the metal and the first layer of SiO_2.

These three groups were measured to determine the immobile and the mobile charge after several intervals of time during which the devices were stored at 300° C under three conditions of applied bias, +12, 0, and -12 volts.

The results are given in Figures 3, 4 and 5. The significant findings in these data are discussed in the following paragraphs.

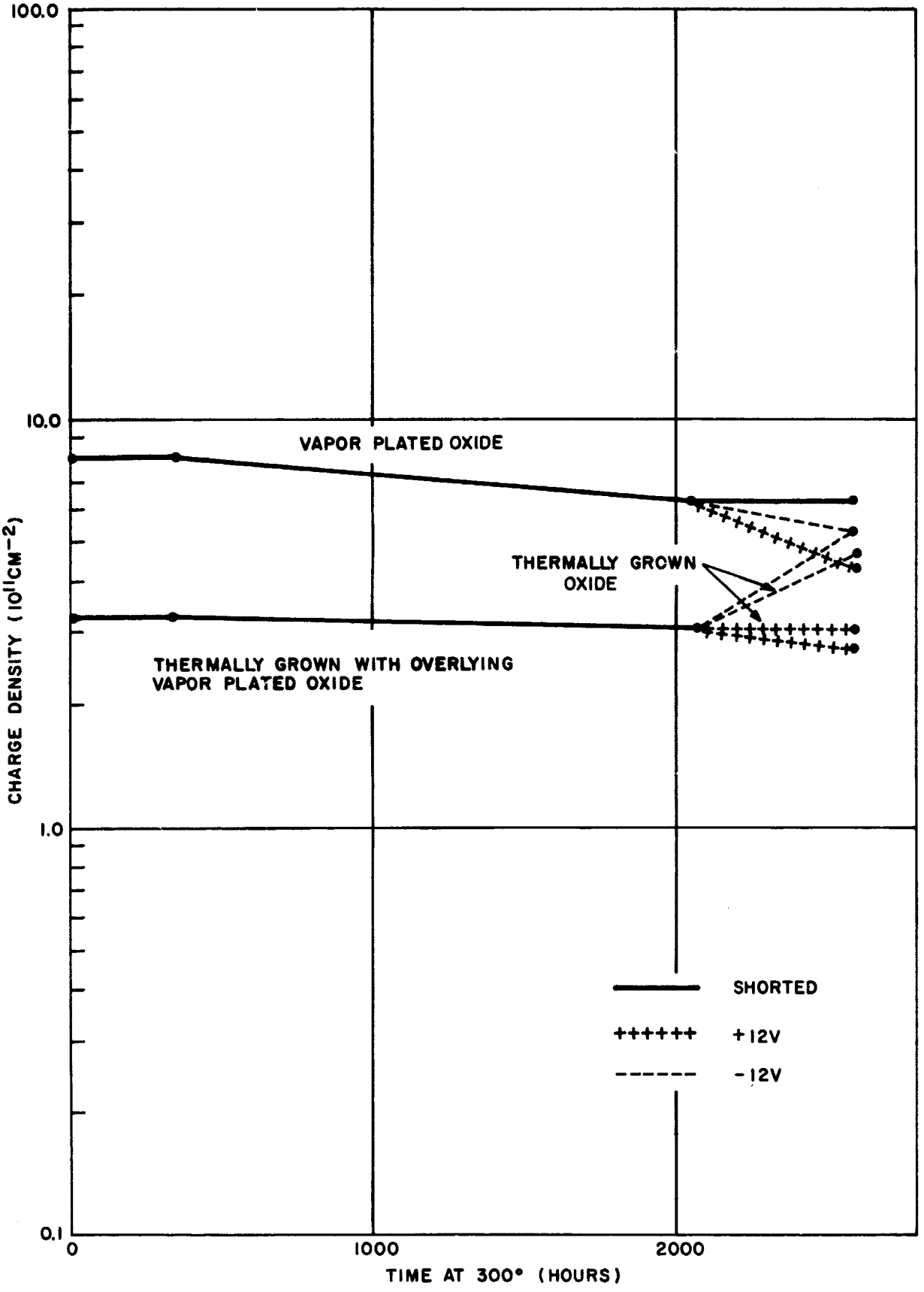


Figure 3. Effects of contaminant migration beneath metal layers on immobile charge density.

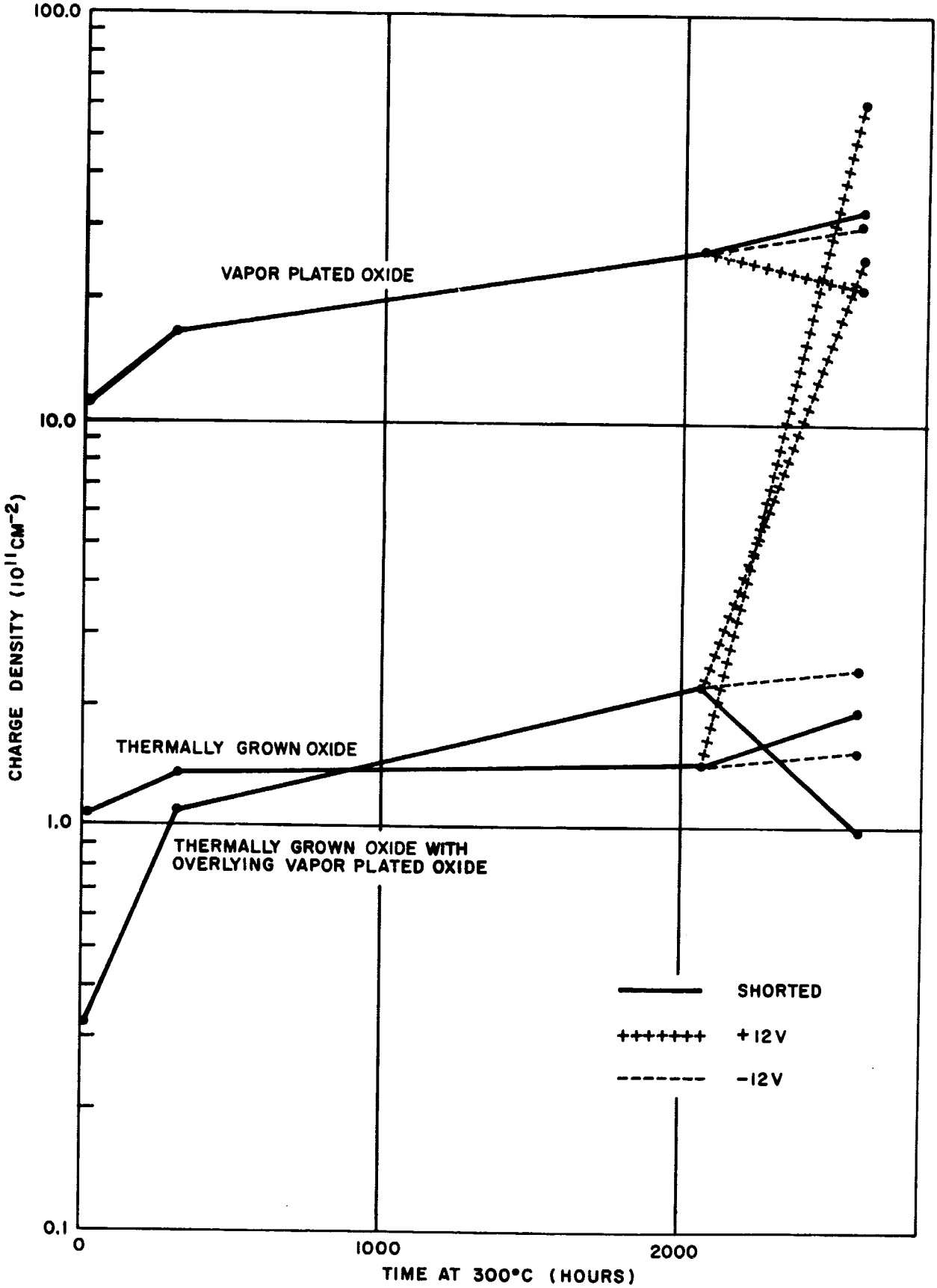


Figure 4. Effects of contaminant migration beneath metal layer on mobile (300° C) charge density.

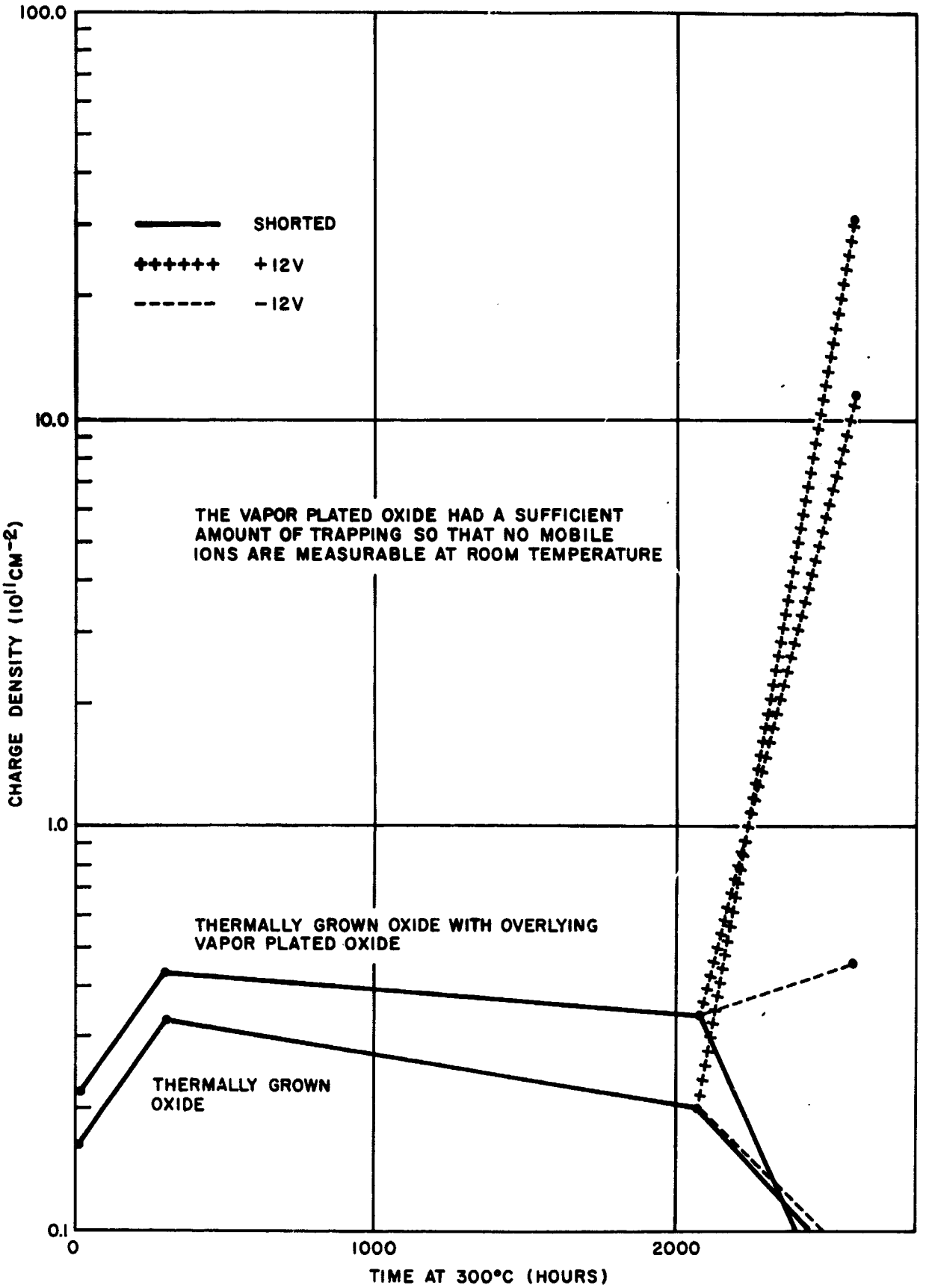


Figure 5. Effects of contaminant migration beneath metal layer on mobile (25° C) charge density.

Immobile Charge. - The immobile charge density of thermally grown oxides is hardly affected by a 300° C bake for more than 2000 hours under either a zero or a positive applied bias.

The immobile charge density of vapor-plated oxides (on silicon) is somewhat decreased under a positive bias at 300° C for 520 hours.

The immobile charge density of thermally grown oxides increases during a 300° C bake for 520 hours under a negative bias. This result has been reported in the literature (Ref. 2).

The vapor-plated oxide over the metal and first layer of oxide does not greatly influence the immobile charge density of the underlying thermally grown oxide.

Mobile Charge. - The mobile charge (at 300° C) is increased during a 300° C bake under zero applied bias in all three types of samples.

The increase in mobile charge (300° C) is much greater under a positive bias than under a zero or a negative bias. This might be expected because the mobile charge is believed to consist of cations.

The increase in mobile (300° C) ions is very large for the thermally grown oxide, both with and without the vapor plated

oxide over the metal pattern. This is believed to be due to residual sodium left from the photolithographic steps needed to fabricate the metal pattern.

It is important to note that contamination either in the second layer or on top of a single layer is able to move from areas adjacent to areas beneath metal regions. This should be borne in mind in the design of future devices which might not have phosphorus gettering and which may be operated with a positive voltage on the metal. The result also suggests that attention should be directed to the photolithographic steps in a search for sources of contamination.

The amount of mobile charge at room temperature is not greatly increased by the presence of the vapor-plated oxide.

The amount of mobile charge (25°C) is not greatly affected in thermally grown oxide, with or without a vapor-plated oxide over the metal pattern, by a 300°C bake under zero bias or negative bias.

The amount of mobile charge (25°C) is greatly increased by a 300°C bake under a positive bias. This is consistent with the theory that the mobile charge at room temperature is a more mobile form of sodium than the form seen only at higher temperatures.

No Initial Change in Device Performance Due to a Second Layer of SiO_2 (Vapor-Plated)

A number of experiments were performed that demonstrate that the deposition of a vapor-plated SiO_2 layer over either bipolar or MOS transistors (i.e., over the metal pattern) does not significantly alter the performance of the devices. In this connection, one should guard against the illusion that a device is not degraded by a second layer of oxide on the basis of only the initial performance of the device.

Surface Ions

An experiment was conducted to demonstrate the effects of surface ions on the outer surface of the oxide.

The experiment was conducted on existing structures, pictured in Figures 6 and 7. The chip is from the production line of high-performance linear amplifier integrated circuits and the metal pattern was chosen for testing discrete devices in ways in which the effects of the applied bias on metalized regions might be expected to influence the performance of devices in the chip. The resistivity of the n-type region between the p-type diffused regions is 5 ohm-cm. Metal electrodes overlying the oxide layer, labeled A and B, were used to apply electric fields along the surface of the

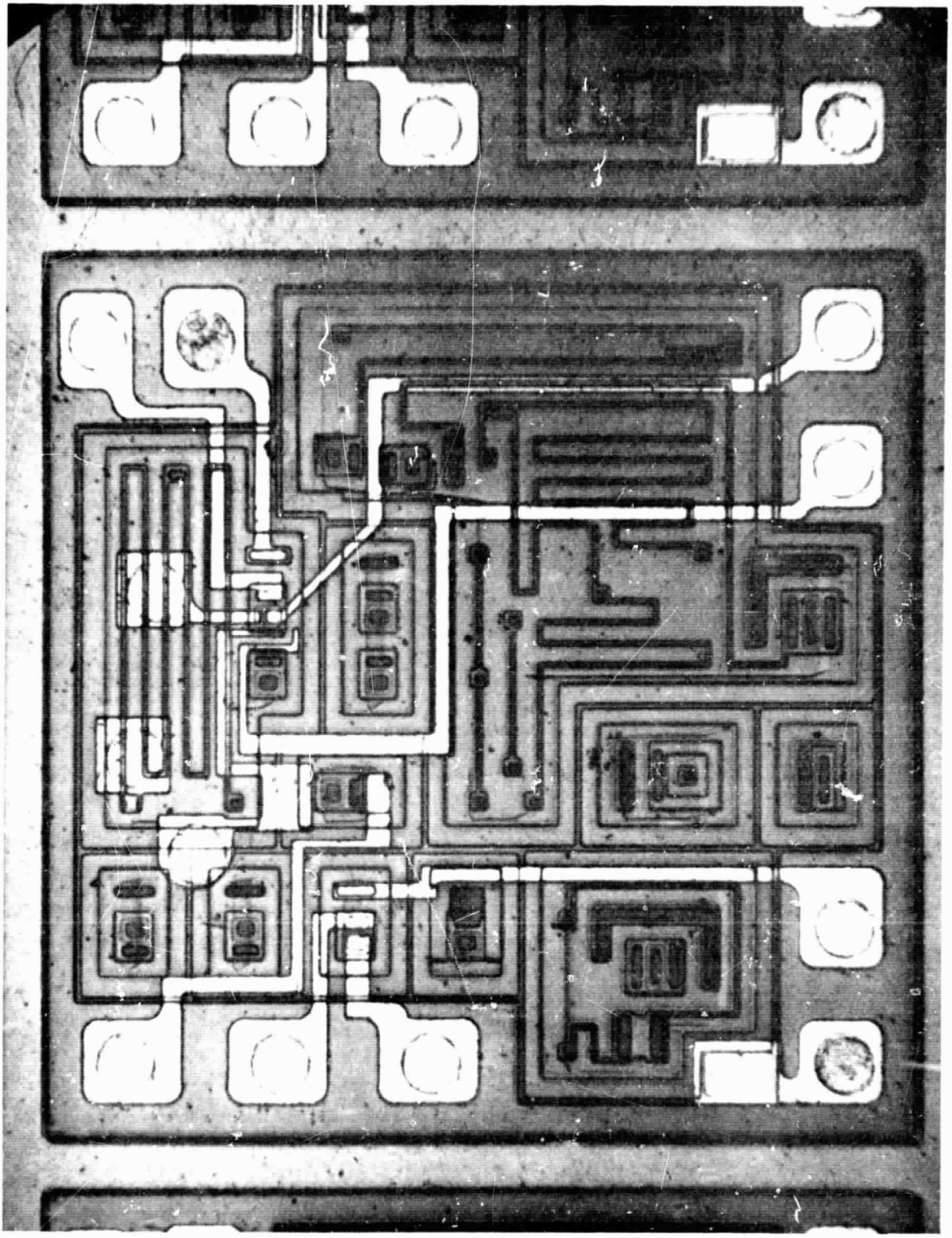


Figure 6. Structure used for studying surface ions.

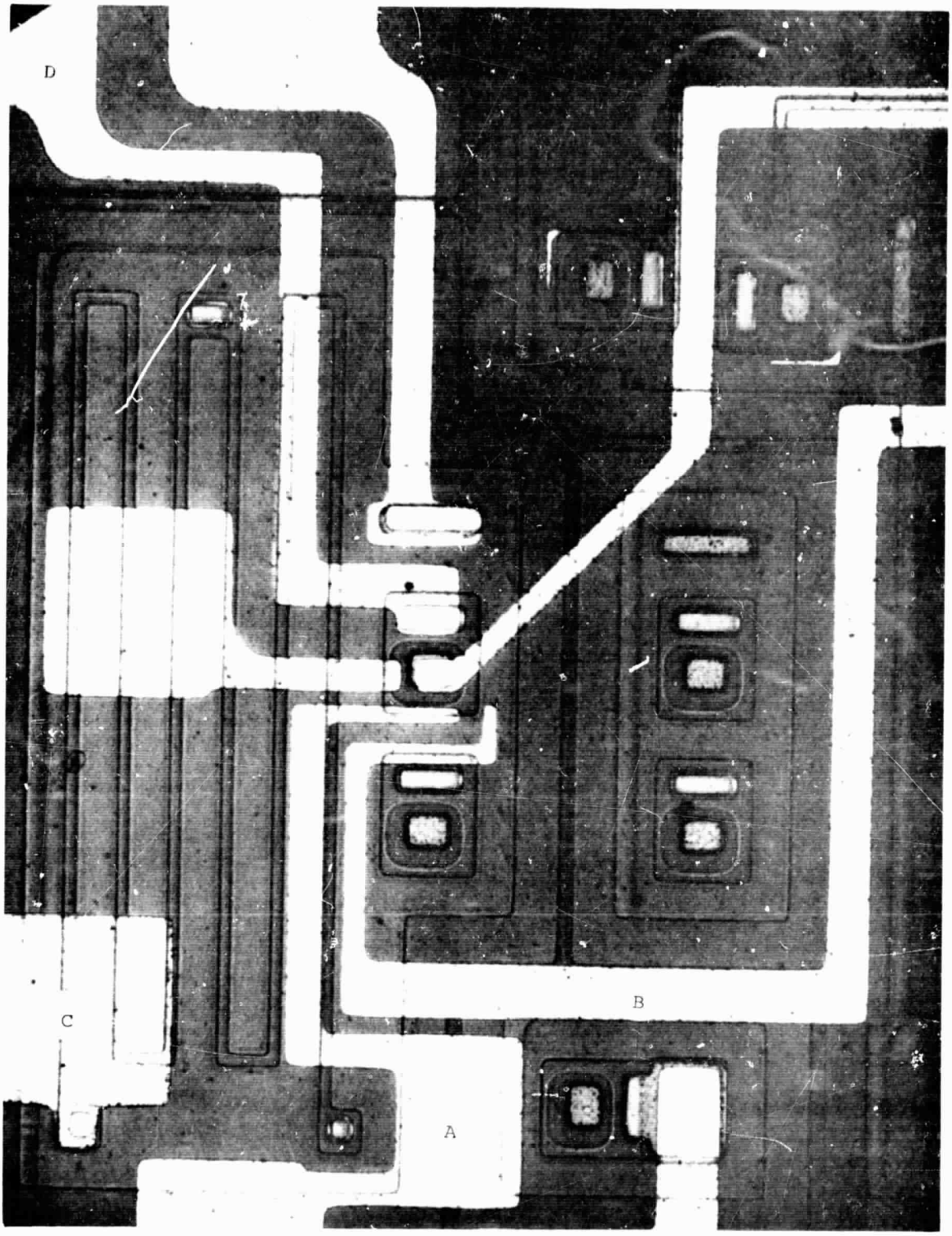


Figure 7. Close-up view of structure used for studying surface ions.

oxide to drift surface ions. Their effects were monitored by measuring the current between contacts C and D after the surface ions were drifted. Contacts C and D provide electrical connectors to two isolated p-type diffused regions. Electrode A overlies the oxide layer over each of these regions. Therefore, a pileup of negative surface ions along conductor A can invert the n-type regions and alter the resistance between the regions contacted by C and D.

The current measurements were made after one minute of bias on the electrodes AB. The electrodes AB were shorted to one of the p-type diffused regions for the current measurement. Data taken on this structure under various conditions are tabulated below. Wet ambients were obtained by bubbling N_2 through water at room temperature. Dry ambients were obtained in a dry nitrogen jet stream.

These data indicate that, as expected, surface ions are more of a problem in wet ambients, that surface ions move in times of the order of one minute in wet ambients but not in dry ambients, and that the second layer of oxide protects against the influence of surface ions.

Measurement Conditions in Sequence		Measured Current*	
Voltage AB	Ambient	On Devices without Second Layer	On Devices with Vapor Plated SiO_2 Second Layer
0 V	Dry	0 mA	0 mA
50 V	Dry	0	0
50 V	Wet	69	0
50 V	Dry	69	0
0 V	Dry	3	0
0 V	Wet	0	0

* V_{CD} = 25 V

A second set of data was taken under different conditions. In this case, the potential was applied to conductor A relative to the underlying n-type silicon both for the one-minute drift period and during the current measurement. The results are tabulated below.

Measurement Conditions in Sequence		Measured Current*	
Voltage	Ambient	On Devices without Second Layer	On Devices with Vapor Plated SiO_2 Second Layer
0 V	Dry	0 mA	0 mA
-50 V	Dry	50	37
-50 V	Wet	69	12
-50 V	Dry	105	38
0 V	Dry	42	0
0 V	Wet	0	0

* V_{CD} = 5 V

These data may be interpreted as follows: The oxide surface on the samples without the second layer has a phosphorus-rich surface due to its use as a diffusion mask. This phosphorus-rich surface is hygroscopic, and therefore its surface ions are abundant and quite mobile. It should, therefore, have a more conductive surface. A more conductive surface apparently can increase the effective area of the electrode by causing the surface potential of the oxide near the electrode to approach that of the electrode. This could explain why the measured currents are higher for devices without the second oxide layer. It also could explain why the current is not reduced to zero in a dry ambient.

The effectiveness of the second layer is believed to be due to at least three factors:

1. Because the second layer contains no phosphorus, the surface is less hygroscopic and therefore the surface ions are fewer in number and less mobile;
2. The structural difference between a one- and a two-dielectric layer device may yield weaker electric fields along the surface in the case of two layers;
3. An insulator layer over the edge of a metal layer may make it possible for surface ions to move up and over the metal so that the metal shields the silicon from the effects of the surface ions.

These results demonstrate the importance of the effects of surface ions. The test structures described in this report for measuring the effects of surface ions have been demonstrated to yield practical empirical data. It is possible to compare the surfaces of two different samples. On the other hand, there are many difficulties encountered when attempting to develop a quantitative theoretical basis for interpreting the data from these test structures. Among these are the following:

1. Ions moving through the oxide also influence the measured current;
2. Changes in the measured current may be due to changes in an induced channel joining the diffused junctions or due to changes in surface potential which influence the carrier generation rate, and, therefore, the reverse current of the reverse biased junction;
3. The current is time dependent. The time constant could be expected to depend on the applied field along the surface, on the ambient humidity, on the surface condition, and on whether the oxide layer covers the edge of the metal;
4. The degree to which a pile-up of surface ions depends on the applied field and on the area from which ions are drifted is as yet unknown. Whether a wider electrode spacing decreases the surface ion effects because of the lower electric field or increases their effects because ions are collected from a larger area is still a matter of conjecture.

Test Structure Mask Sets

Introduction. - Two mask sets were prepared for fabricating a variety of test structures designed to provide data concerning the fundamental electrical properties of the insulator-silicon interface.

The first mask set to be described was designed and built during this program. Figure 8 shows a photograph of the test structures made with this mask set. The chip size is 70 x 70 mils. The set contains masks for

1. Cutting openings in the oxide to create a diffusion mask,
2. Cutting openings in the oxide for the metal-silicon contacts,
3. Delineating the metal pattern,
4. Cutting openings in a second insulator layer for welding leads to the bonding pads.

MOS Capacitor. - The large square on the upper left of Figure 8 is an MOS capacitor. The capacitance-voltage relationship taken on MOS capacitors is very useful for studying the surface potential of silicon under insulators layers. From the change in the C-V characteristics under applied voltages (± 12 volts) at 300° C and at room temperature, one can calculate the density of immobile and mobile

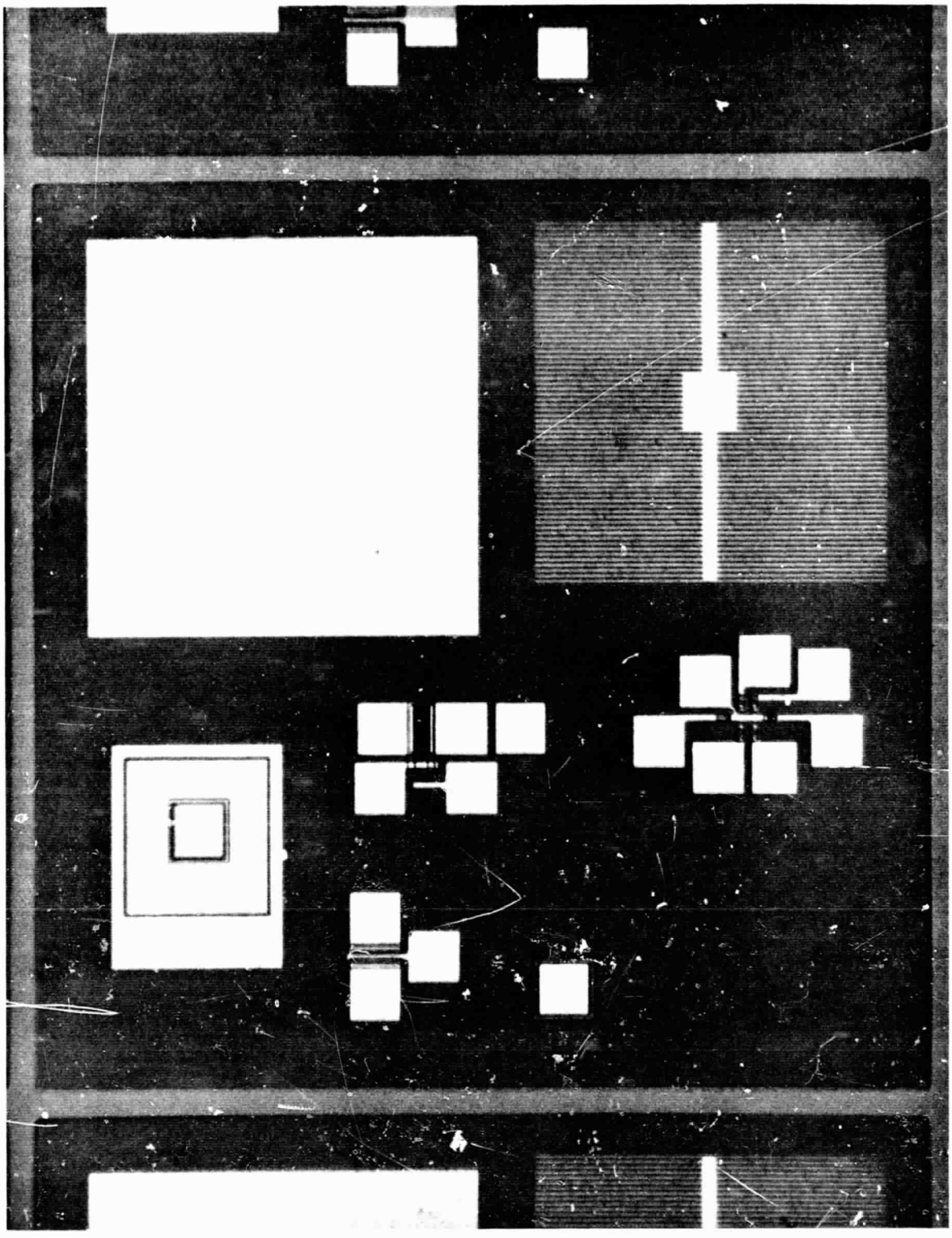


Figure 8. Basic test structure chip.

(at 300°C and at room temperature) charge and the density of slow states in the oxide or at its interface with the silicon. The theory of the capacitance-voltage technique for studying oxidized silicon surfaces using MOS capacitors has been described by Grove et al. (Ref. 20).

Structure for studying lateral contaminant migration under metal layers. - Several variations in the structural design of MOS capacitors extend the usefulness of the C-V technique. In the upper right part of Figure 8 the capacitor has a high ratio of perimeter to area. This capacitor was designed to study the migration of mobile species of charge or of neutral atoms from regions adjacent to metal layers to regions beneath metal layers on oxides. The line and spacing widths for this structure are two mils.

MOS Hall structure. - A specially designed MOS transistor, shown in Figure 8, forms an inversion layer having a sufficient number of connections that Hall measurements and sheet conductivity measurements can be taken to measure the density of mobile carriers and their mobility in the inversion layer. This structure is shown in Figure 8 directly below the capacitor with the high perimeter-to-area ratio. It consists of six diffused p-n junctions

with contact lands and an MOS capacitor formed to create an inversion layer in the shape required to make Hall measurements on the inversion layer. Figure 9 shows a closeup of this structure. This structure is similar to that reported by Colman and Mize (Refs. 21-23) except that it is much smaller. Our structure is 2.5 mils long and 0.5 mil wide, whereas that used by Colman and Mize was 90 mils long and 10 mils wide.

Diode. - Diffused p-n junction diodes are included for studying effects on diode leakage currents and diode breakdown voltages. The small square area in the lower right portion of Figure 8 is one of these diodes.

Surface recombination velocity test structure. - Diffused junction diodes with surrounding field plates are used to measure the surface recombination velocity. These devices are in the lower left of Figure 8. The second field plate surrounding the first field plate was included to permit cutting off any undesired inversion layer that might exist outside the region covered by the first field plate. Details for calculating the surface recombination velocity from measurements of the reverse-biased diode current as a function of the field-plate voltage have been published by Grove and Fitzgerald (Ref 24).

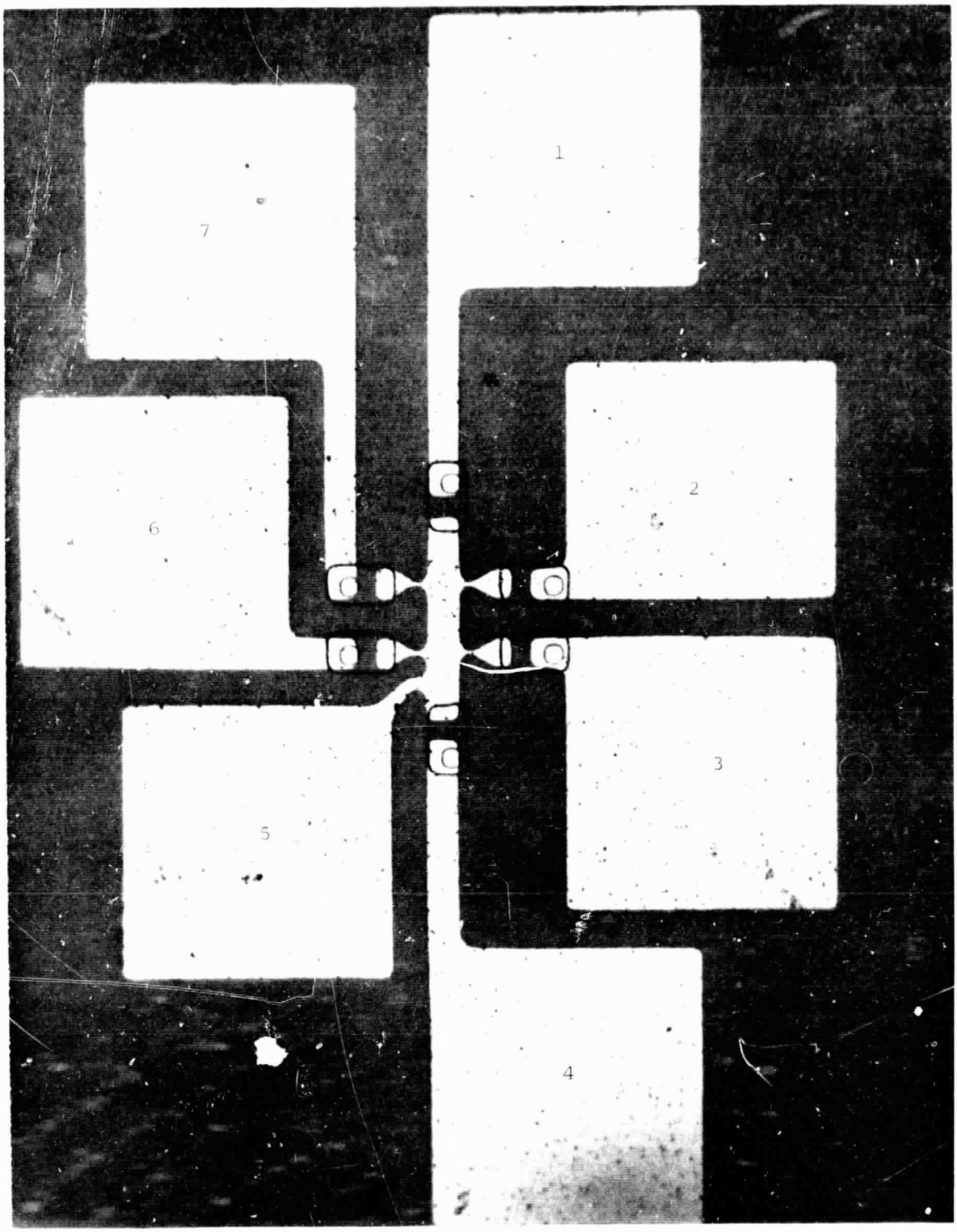


Figure 9. Hall measurement test structure.

MOS transistor. - The chip shown in Figure 8 includes a MOS transistor. This transistor alone is shown in Figure 10. By comparing the threshold voltage of the MOS transistor with the voltage at which the inversion layer forms in the MOS capacitor, the density of surface states of the type that immobilize carriers in the inversion layer can be measured. This technique was described by Kooi (Ref. 25). By using the measured transconductance value of the MOS transistor in the equation for transconductance the mobility of carriers can be calculated,

$$g_m = \frac{\epsilon_{ox}\,\mu w}{LT_{ox}} \quad (V_g - V_p)$$

where g_m is the transconductance, ϵ_{ox} is the dielectric constant of the oxide,

μ is the carrier mobility,

w is the channel width,

L is the channel length,

T_{ox} is the oxide thickness,

V_g is the gate voltage,

V_p is the pinch-off voltage.

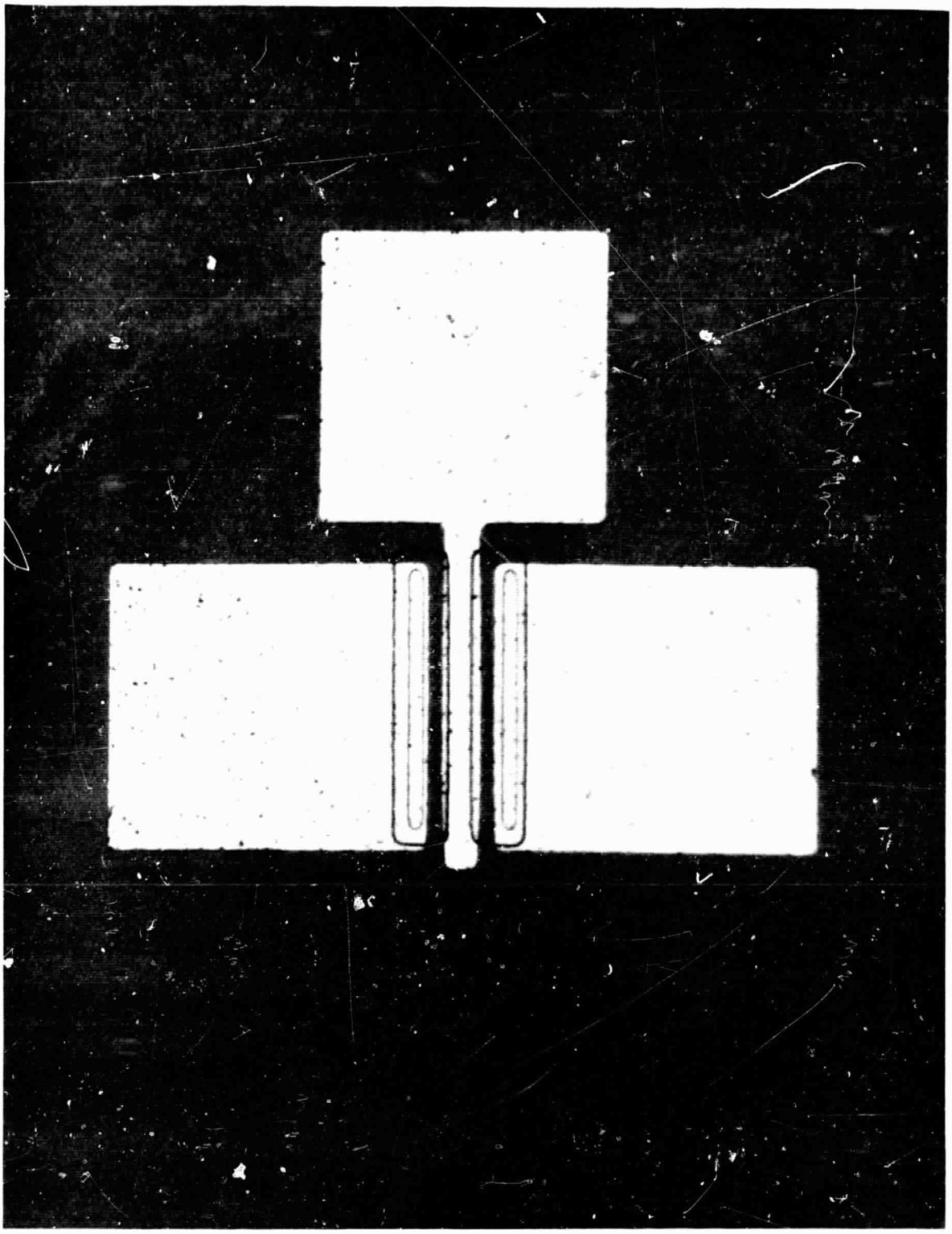


Figure 10. MOS transistor.

Surface ion test structure. - The test device shown in Figure 8 includes a test structure for studying mobile ions on the oxide surface. This structure, shown in Figure 11, consists of two parallel metal conductors, on top of the oxide with contact lands. One of the conductors overlies two diffused p-n junctions. The application of a voltage between the conductors causes surface ions to move along the surface and pile up near one of the conductors. If this pile-up of surface charge is sufficiently large, it can invert the silicon beneath the oxide and thereby form a channel between the two diffused p-n junctions. This is sensed by a measurement of the impedance between the diffused regions.

The theoretical interpretation of the measurements taken in this way is difficult. The impedance between the two diffused regions may change not only because of a channel but because of changes in surface potential that affect the diode reverse current of one of the junctions. In spite of the interpretation difficulties the structure is a sensitive indicator of surface ion effects.

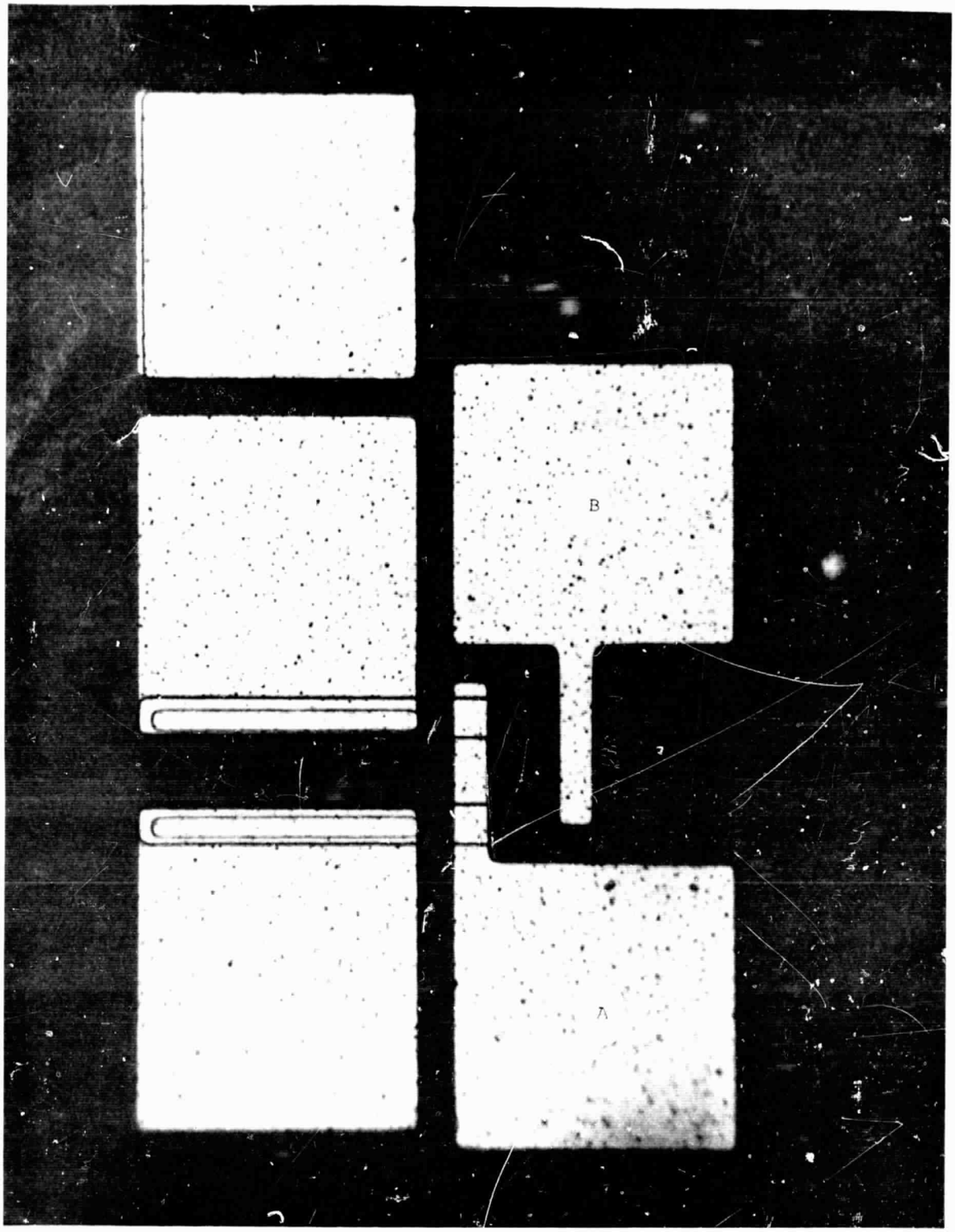


Figure 11. Surface ion test structure.

Test structures on production microcircuit chip. - Figure 12 shows a second set of test structures that were chosen to study the effects of a second layer of dielectric material on devices that were prepared by a complex processing sequence used in the production of commercially available microcircuits. These devices were taken from the production line of PA7709 high performance operational amplifier linear integrated circuits.

A special set of masks was prepared for forming the delineated metal and the contact cuts in the oxide over the metal in a pattern that enables one to measure the characteristics of discrete devices. Among the devices that were tested in this structure are bipolar double diffused npn transistors of two geometrical configurations, bipolar pnp transistors with substrate collectors, and lateral bipolar pnp transistors. Bipolar pnp transistors with substrate collectors are single diffused transistors which are formed so that the collector region is formed in a portion of the unaltered p-type starting wafer. The base region is formed in an n-type epitaxial layer (which is isolated by p-type diffusion layers) and the emitter region is formed by the same diffusion of donors used to form the base region of the double diffused npn transistors.

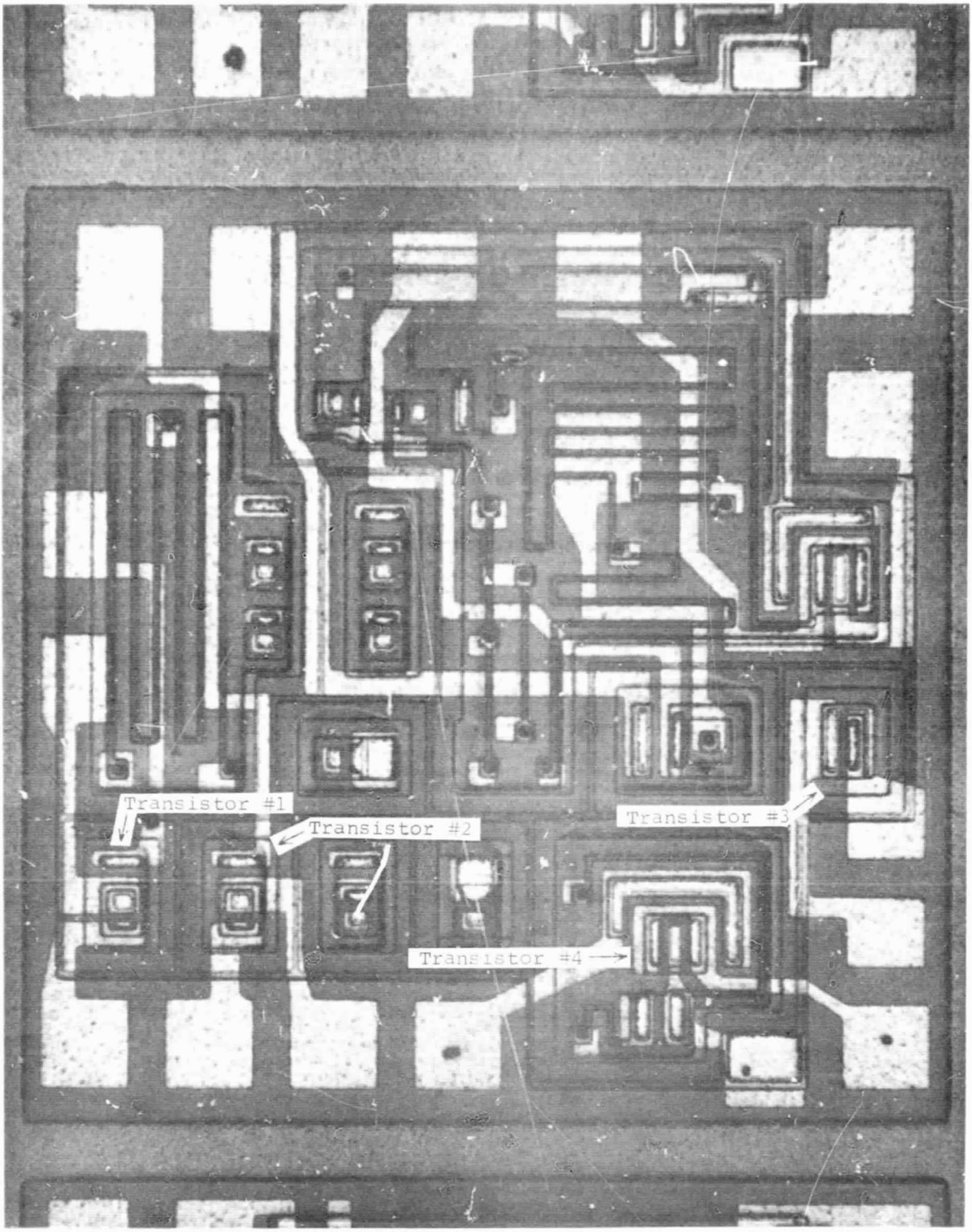


Figure 12. Microcircuit chip with special metalization pattern for testing discrete devices.

The lateral pnp transistors are formed in the n-type diffusion layer by diffusing the p-type emitter and collector regions with the same diffusion as that used to form the base of the npn transistors and the emitter of the pnp substrate collector transistor. The resistivity of the n-type epitaxial layer is 5 ohm-cm.

Equipment for Testing Test Structures

Introduction. - This subsection describes the test equipment that was set up for taking measurements on the test structures fabricated for this program. Also included is a discussion of problem areas that were encountered.

C-V measuring equipment. - The equipment for measuring the C-V relationship is shown in the schematic diagram of Figure 13. The basic instrument for measuring the capacitance is a Tektronix L-C Meter that provides a direct reading measurement of the capacitance in the range of 0 to 300 pF at a measurement frequency of 140 kHz. The 10^6 ohm resistor isolates the power supply from the L-C Meter so that the capacitance of the power supply is not measured. The 0.01-μF capacitor prevents d-c current from flowing through the L-C Meter. The X axis of the X-Y recorder records the voltage applied to the device and the Y axis records the voltage at the terminals

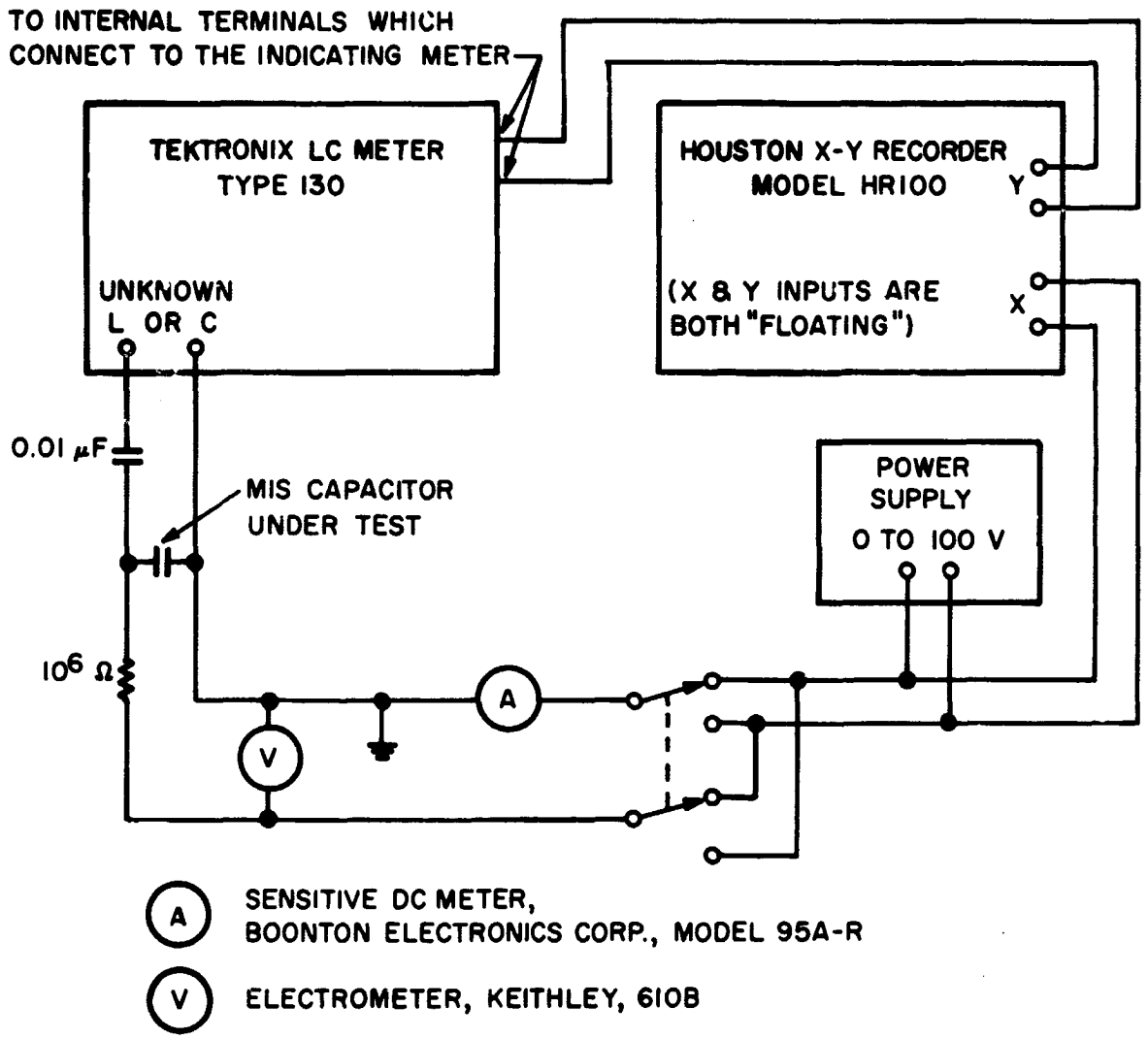


Figure 13. Diagram of equipment set-up for measuring C-V relationship of metal-insulator-silicon structures.

of the indicating meter in the L-C Meter. The current meter indicates any d-c leakage current through the capacitor.

MOS transistor measuring equipment. - Figure 14 shows a schematic diagram of the equipment used to evaluate MOS transistors. It records the drain current as a function of the gate voltage for a given constant drain-to-source voltage. The threshold voltage and transconductance can easily be obtained from the plotted curve as shown in Figure 15.

Surface recombination velocity measurements. - Figure 16 shows a schematic diagram of the circuit used to measure surface recombination velocities in the manner described by Grove and Fitzgerald (Ref. 26). To minimize noise and ground loop problems, the apparatus is located in a screen room, and the battery voltage sources are enclosed in a metal box with coaxial connecting leads to the electrometer. The circuit provides a voltage to bias the second field plate so that the area of the carrier generation region is accurately shown. Figure 17 shows sample data taken by this measurement technique. The surface recombination velocity is calculated as shown in Figure 18.

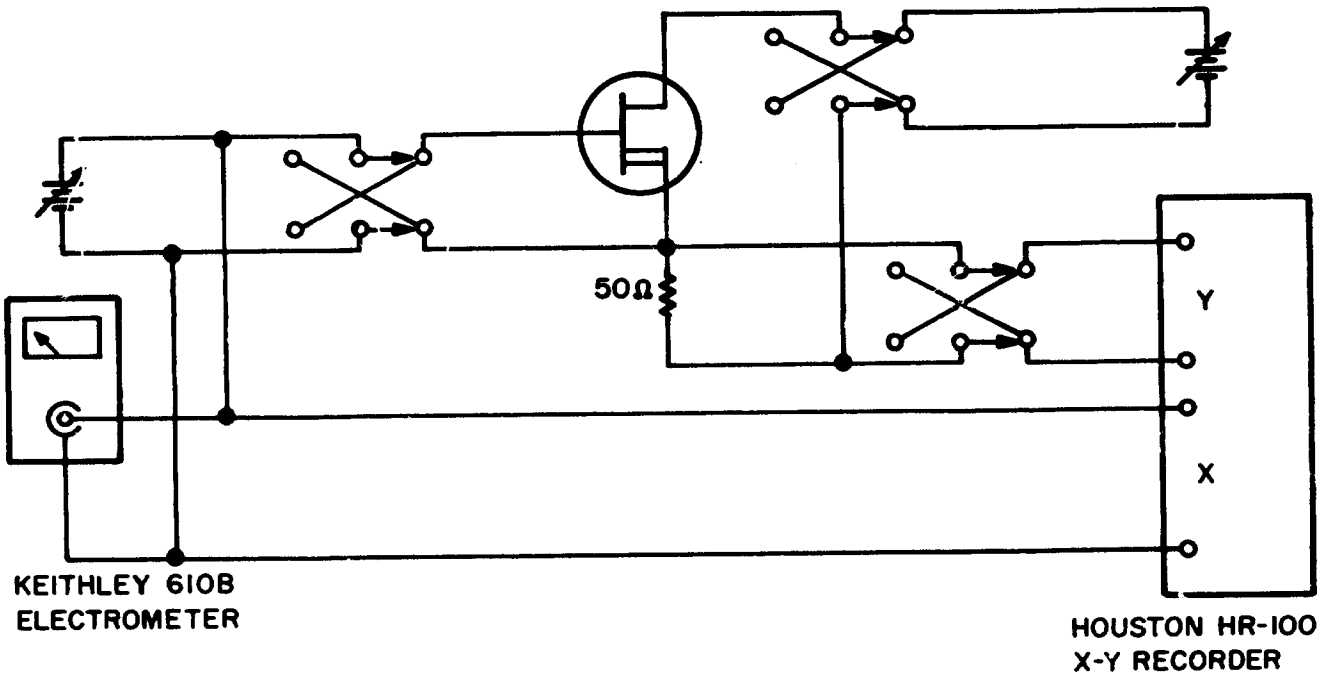


Figure 14. MOS transistor measuring equipment.

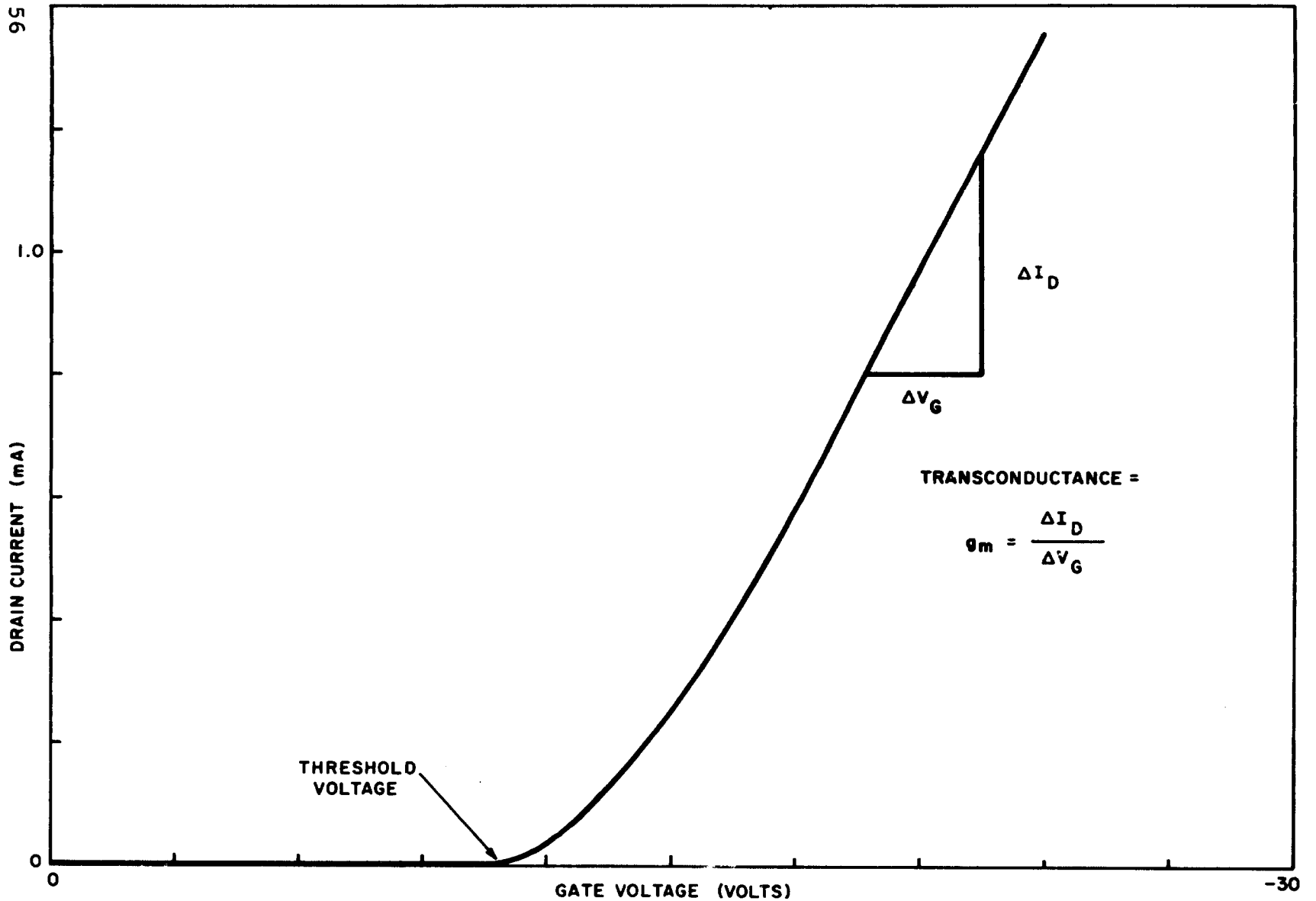


Figure 15. Typical I-V curve of MOS transistor.

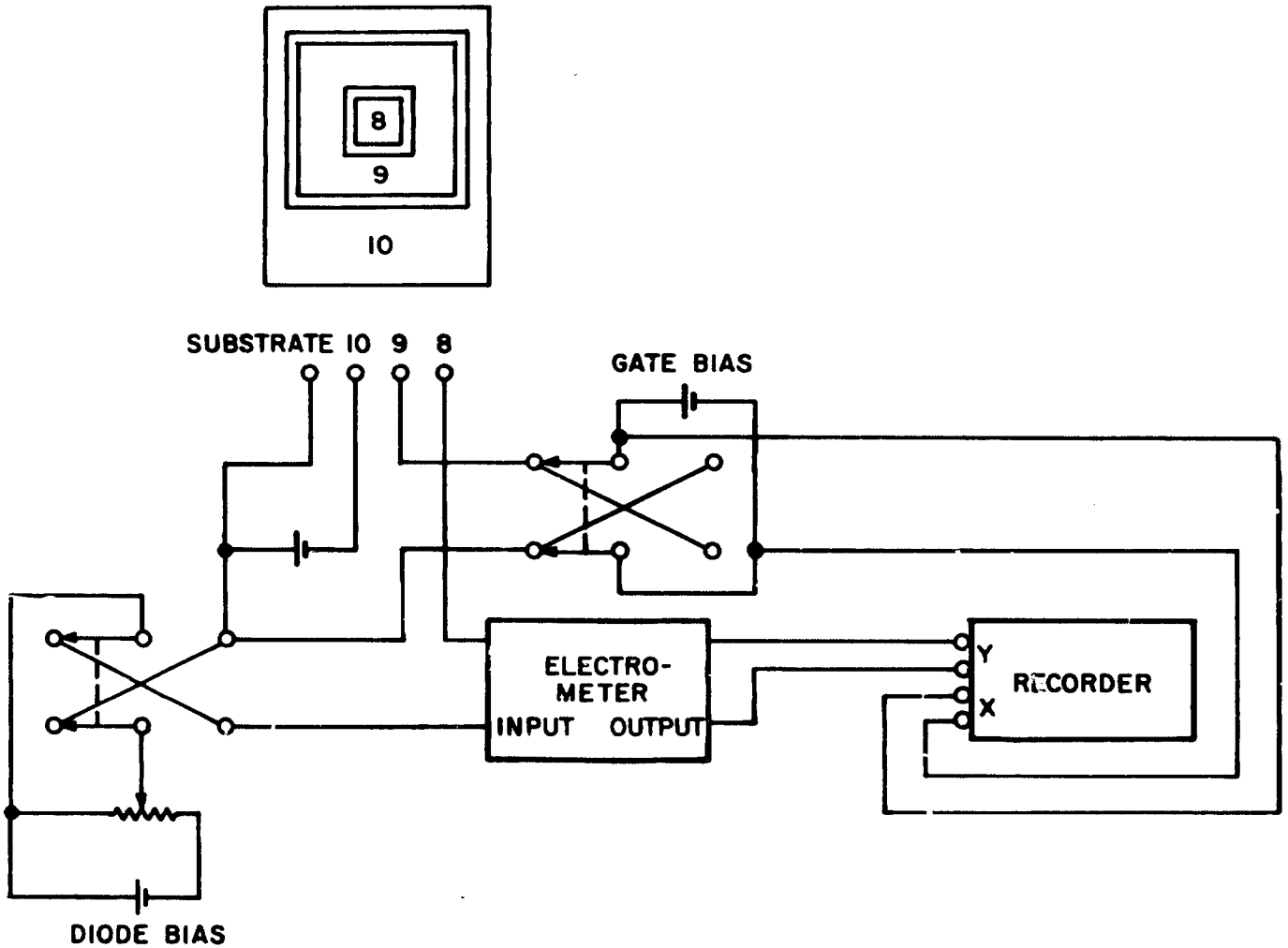


Figure 16. Diagram of equipment for measuring surface recombination velocity.

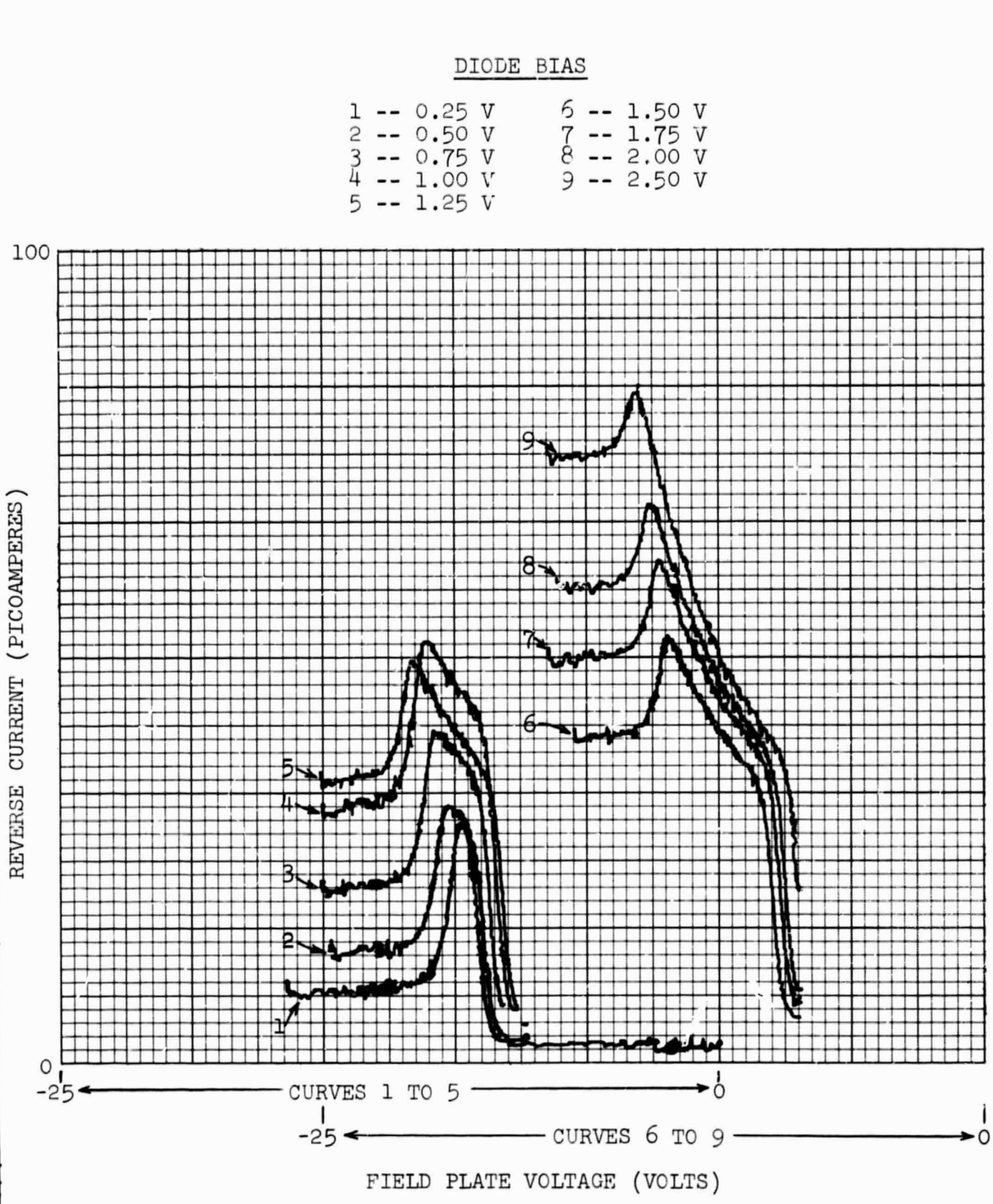


Figure 17. Sample data from surface recombination velocity measurements.

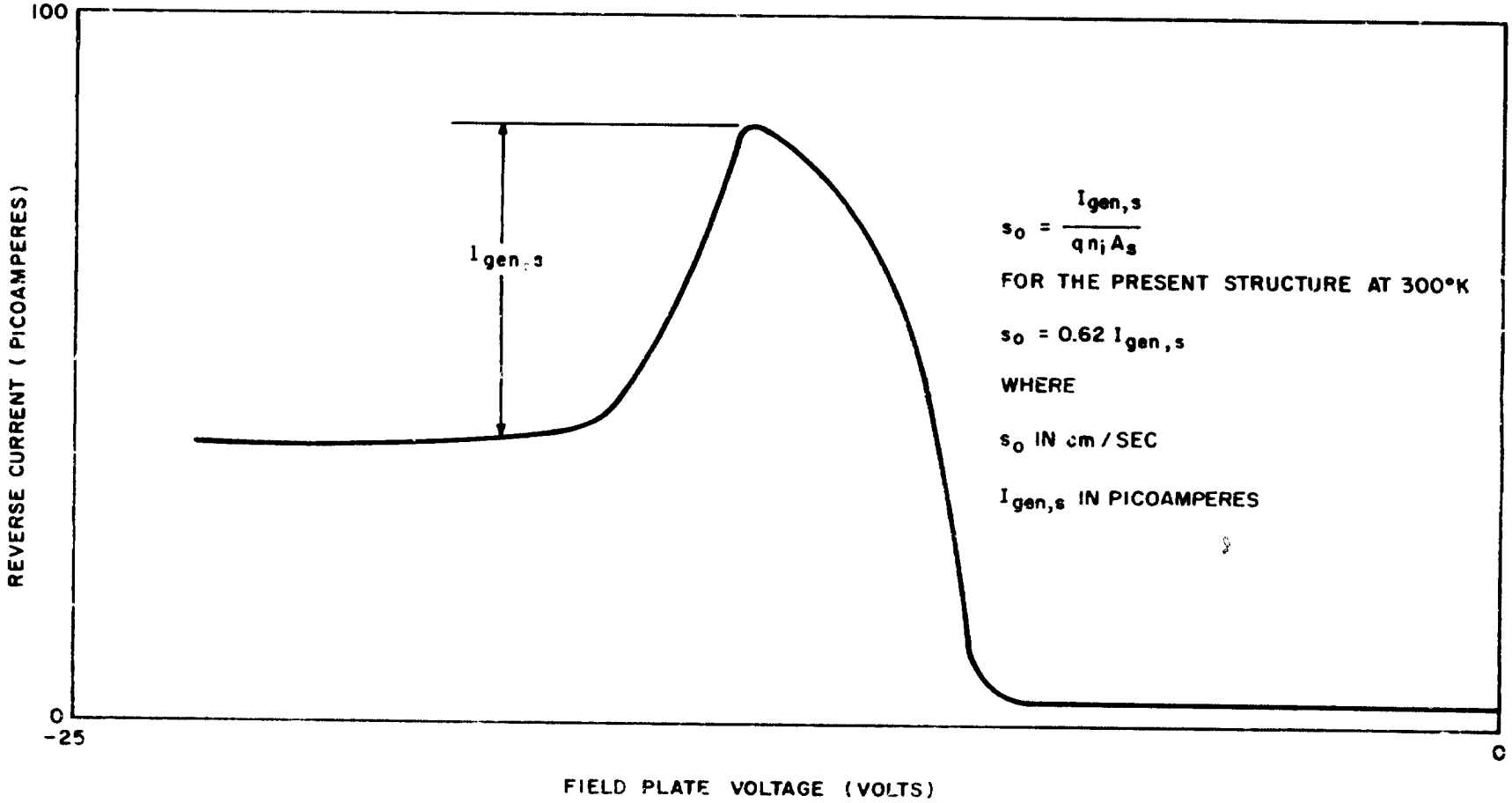


Figure 18. Calculation of surface recombination velocity, S_o, on a typical device.

Hall measurements. - Figure 19 shows a schematic diagram of the equipment that we use to make Hall measurements on inversion layers. This technique was developed by Colman and Mize (Refs. 21-23). Figure 20 shows a photograph of the experimental setup. It consists of a 4200-gauss magnet mounted on a hinge; a switching arrangement so that the voltage across each of the important sets of terminals can be measured on the electrometer; and a fixture for mounting, connecting to, and holding the test sample for the measurement. There is a reversing switch on the current source. Because non-magnetic packages were not available during this program, the mounting arrangement used is practical mainly for establishing feasibility of the method. Non-magnetic packages are on order.

Measurement of surface ion effects. - Figure 21 shows a schematic diagram of the circuit that was set up for measuring the effects of surface ions. It consists of a battery voltage source enclosed in a metal box with coaxial leads to the electrometer. The apparatus is located in a screen room. It is capable of measuring currents as low as 10^{-11} amperes. Because the electrometer measures voltage and current simultaneously, it is easy to check that each measured current is being read with a

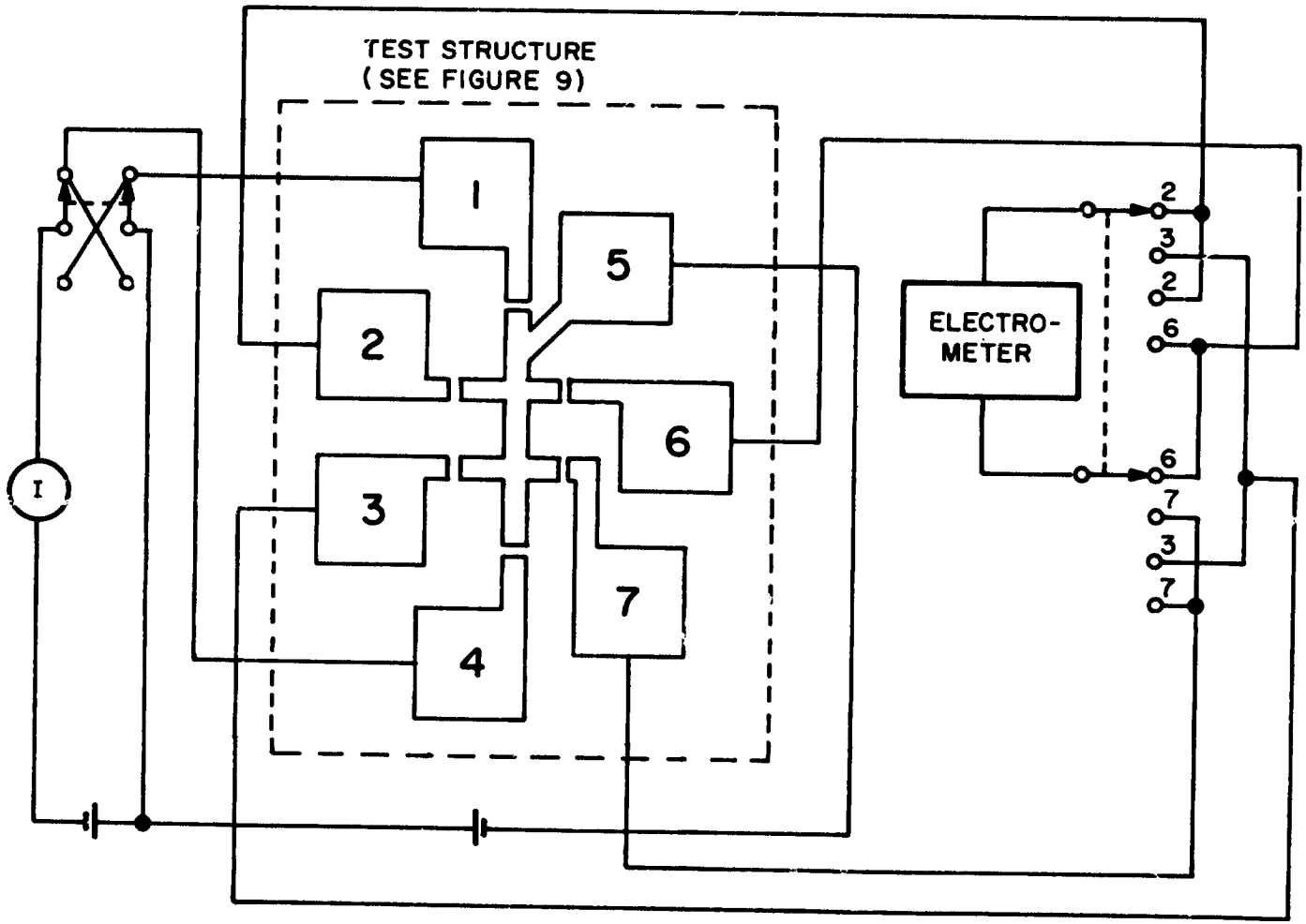


Figure 19. Diagram of equipment for Hall measurements.

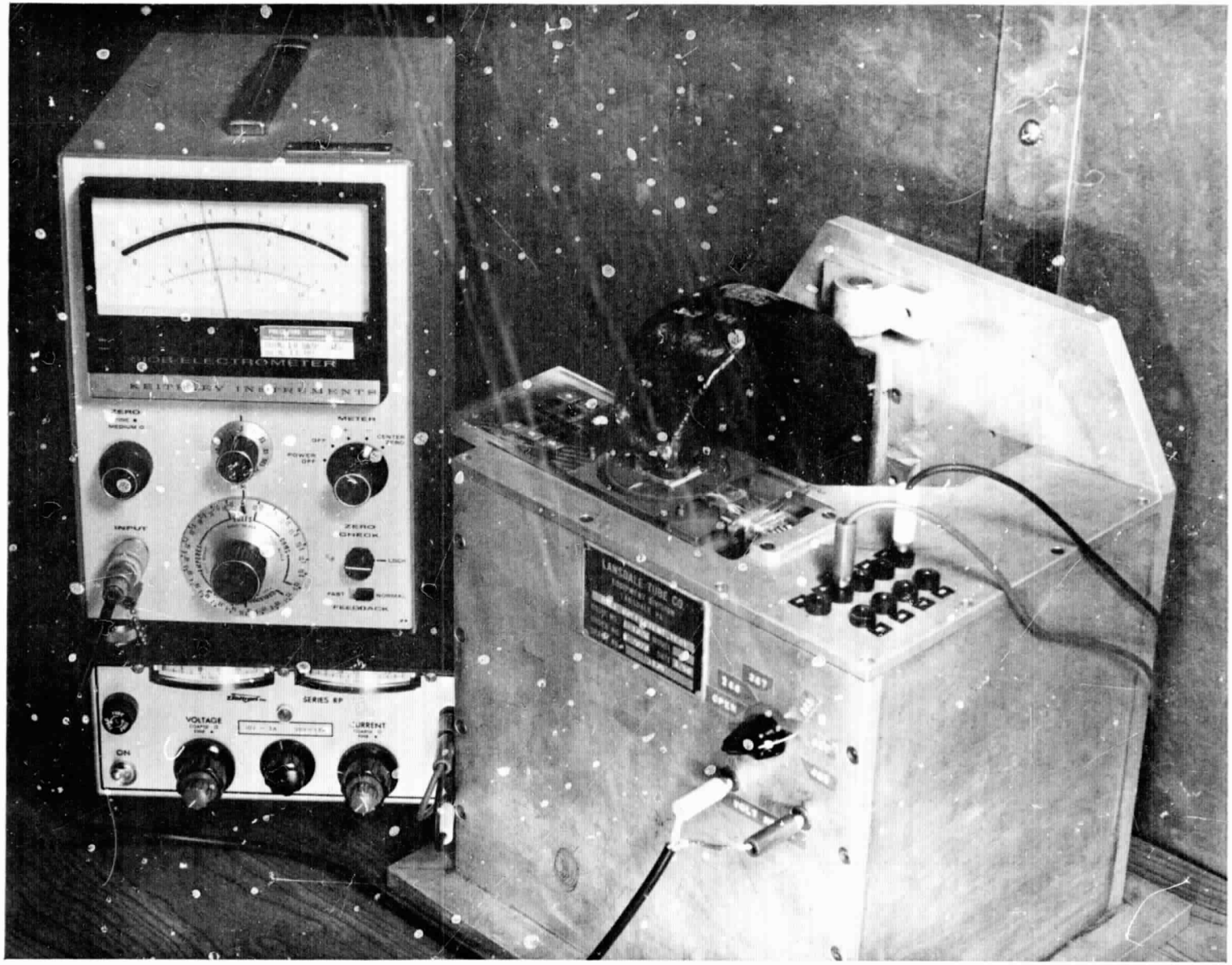


Figure 20. Hall measurement equipment.

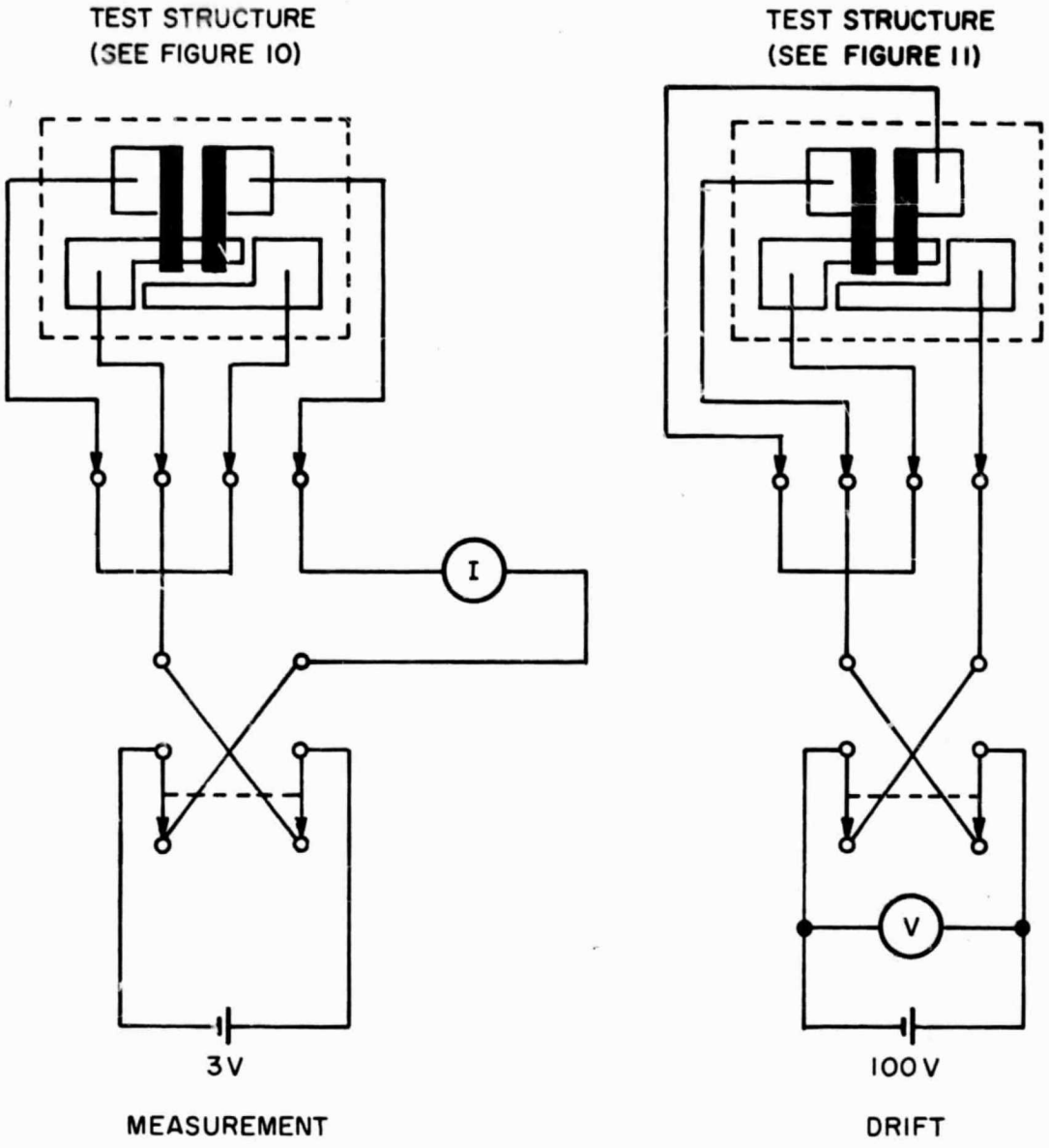


Figure 21. Diagrams of equipment for studying surface ions.

meter input impedance low enough that the voltage developed across the meter is negligible compared to that across the test structure, thus insuring that all of the current measurements are taken with the same voltage across the device.

As shown in Figure 21, the two metal electrodes on the oxide are electrically shorted to one of the diffused regions when the current is being measured, so that any influence of the potential of these electrodes on the underlying silicon is controlled and repeated to the same degree each time a measurement is made. If this were not well controlled, stray charge in random amounts would be present on these electrodes, which would influence the resistance between the diffused regions. The resulting random variation in the measured current would make the data meaningless.

The biasing circuit for drifting the surface ions is given in Figure 21. Note that in this case the two diffused junction regions are shorted electrically to the metal electrode that lies over them. This is done to prevent mobile ions from moving beneath the metal in a direction normal to the plane of the structure while the structure is under the bias to move surface ions. It is important

that the mobile ion density (measured on the MOS capacitors) be considered when analyzing and interpreting the data from the surface ion test structure.

Diode reverse current. - The reverse current of the p-n junction diode is measured on the same equipment used to measure the effects of surface ions (see Figure 21).

Diode breakdown voltage. - The diode breakdown voltages are measured on a Tektronix Type 575 Transistor Curve Tracer.

Evaluation of bipolar transistors. - The bipolar transistors were measured on equipment and by trained personnel in our Reliability and Quality Control Department.

Experimental Results Taken On Test Structures

Test structure preparation. - Samples were prepared in both of the test structure chip configurations as described previously.

An n-type 5 ohm-cm, phosphorus-doped, <111> oriented silicon wafer and a p-type 3.5 ohm-cm, boron doped, <111> oriented silicon wafer were chosen for the substrates for the test structure pattern shown in Figure 8. In each case, a 6000 Å oxide was grown in dry oxygen at 1200° C. The n-type wafer was boron diffused to a sheet

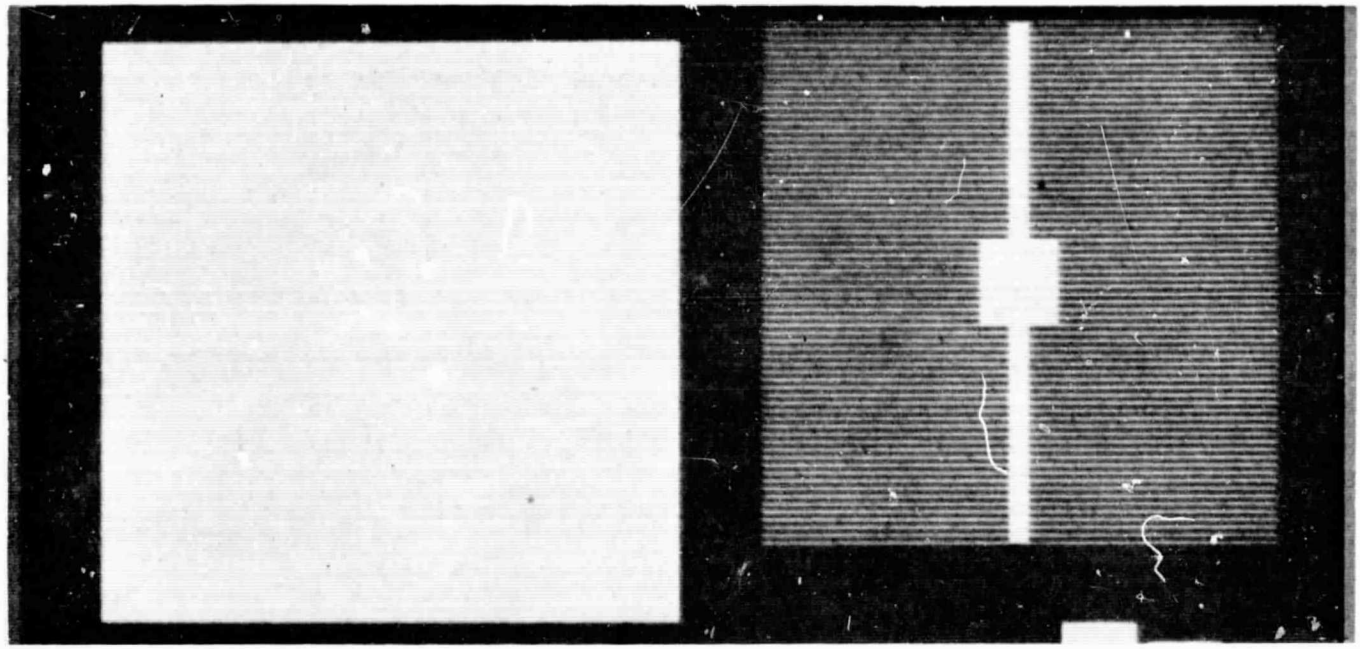
resistivity of 42 ohms/square and to a depth of 1.6 microns, and the p-type wafer was phosphorus diffused to a sheet resistivity of 4.6 ohms/square and to a depth of 2.4 microns. The cuts in the oxide were made using KTFR and the aluminum metal was delineated with AZ 1350 resist. The aluminum was evaporated using an electron beam.

After each wafer was processed into the test structures, it was scribed into halves. Half of each wafer was vapor plated with 10,000 Å of SiO_2, formed at 400°C with the reaction

$$SiH_4 + 2O_2 \longrightarrow SiO_2 + 2H_2O \quad .$$

Contact cuts were made in this second oxide layer and the devices were mounted and tested.

Capacitors. - The important information obtained from a C-V curve taken on an MOS capacitor is the effective immobile charge and the mobile charge at both 300°C and at room temperature. The table on the following page summarizes the data taken on MOS capacitors of the test structures shown in Figure 8.



A B

	10^{11} Charges/cm^2					
	Immobile		Mobile (300° C)		Mobile (25° C)	
	A	B	A	B	A	B
N-type substrate						
Not vapor plated	2.4	2.4	1.0	2.2	0.1	0.1
Vapor plated	2.4	1.5	1.2	3.5	0.2	1.5
P-type substrate						
Not vapor plated	2.7	2.8	1.6	5.0	0.3	2.2
Vapor plated	1.5	3.0	2.2	2.5	0.5	0.8

As might be expected, the measurements on capacitors having a high perimeter-to-area ratio can best be characterized as having a gradual transistion region in the C-V curve and a

fairly wide variation in flatband voltages within each group. These capacitors were designed to show the effects of the migration of impurities from regions adjacent to regions beneath the metalized regions.

The data discussed below were abstracted from C-V data taken on the capacitors having a high perimeter-to-area ratio.

The immobile and mobile (at 300° C and at 25° C) charge density was measured both before and after a bake at 300° C for five days at either plus or minus 12 volts bias. (These tests were conducted on different devices, not consecutively.) The data taken are tabulated below.

P-type substrate	Immobile Charges/cm^2	Mobile (300° C) Charges/cm^2	Mobile (25° C) Charges/cm^2
Not vapor plated			
Before bake	2.8×10^{11}	5.0×10^{11}	2.2×10^{11}
After (-12V)	4.1	6.0	5.0
After (+12V)	2.8	7.0	5.0
Vapor plated			
Before bake	3.0	2.5	0.8
After (-12V)	4.1	0.9	0.3
After (+12V)	2.8	7.0	5.0
N-type substrate			
Not vapor plated			
Before bake	2.4	2.2	0.1
After (-12V)	No data	No data	No data
After (+12V)	No data	No data	No data
Vapor plated			
Before bake	1.5	3.5	1.5
After (-12V)	1.8	3.9	<0.1
After (+12V)	2.7	3.0	<0.1

These data show that the vapor-plated oxide layer did not significantly affect the immobile charge density either initially or after a 300°C bake for five days under either plus or minus 12 volts bias. It would appear that the vapor-plated oxide does not degrade the mobile ion density; moreover, it even appears to improve it.

MOS transistors. - The tabulation below gives the threshold voltage and the transconductance of the MOS transistors in the test structure chip. It should be recognized that the threshold voltage V_{th} and the transconductance, g_m, both appear to be a factor of five poorer than they would be on a typical transistor because the oxide thickness below the gate would be a factor of five thinner than the 6000 Å in these devices. These data are given for both before and after a 300°C bake for seven days under either +12 or -12 volts bias on the gate.

These data indicate that:

1. The threshold voltage level is not seriously degraded by the presence of vapor-plated oxide,

2. The transconductance is degraded in both p-MOST's and n-MOST's by a 300° C bake for seven days under applied bias,

N-MOST	V_{TH}	g_m (1mA, 5V)
Not vapor plated		
Before bake	0 to -2V	150 μmho
After -12V bake	0	116
After +12V bake	0*	136
Vapor plated		
Before bake	0	156
After -12V bake	0	120
After +12V bake	0	120
P-MOST		
Not vapor plated		
Before bake	12 - 14	119
After -12V bake	No data	No data
After +12V bake	No data	No data
Vapor plated		
Before bake	11	115
After -12V bake	15	104
After +12V bake	12.5	100

*Several devices have parallel n channels.

Surface recombination velocity test structure. - Surface recombination velocity measurements were made on samples on both the p- and the n-type substrates. Grove and Fitzgerald (Ref. 24) have shown how the surface recombination velocity can be calculated from the dependence of the reverse current of the diode on the voltage on the field plate. The equation for calculating the surface recombination

velocity is

$$s = \frac{I}{qn_iA}$$

where I is the current due to surface generation,

q is the charge per carrier,

n_i is the intrinsic carrier density,

A is the area of the field plate.

The area of our field plate is $6.8 \times 10^{-4} cm^2$; therefore, at 25° C this equation is

$$s = 0.62\ I$$

where s is in cm/sec and I is in picoamperes.

We measured surface recombination velocities on samples having a single layer of thermally grown SiO_2. The values measured on three samples on p-type silicon were 10, 14 and 21 cm/sec. Three samples on n-type silicon had measured surface recombination velocities of 22, 24 and 37 cm/sec.

Figure 17 shows a set of sample curves of the diode reverse current as a function of the voltage on the field plate and the diode reverse voltage. These data are similar to those published by Grove and Fitzgerald. These data show that the measured surface-generated current depends on the diode reverse voltage. Note that a higher gate voltage is required to maintain an inversion layer as the diode voltage is increased, because an

inversion layer can exist only when the surface potential due to the field plate is higher than the potential on the reverse biased diode. If the potential on the reverse biased diode is higher than the surface potential induced by the field plate, the diode collects the carriers from the inversion layer faster than they are thermally generated. On the basis of these curves we chose to measure surface recombination velocities at an applied voltage of 0.5 volt, so that the field strengths in the inversion layer parallel to the plane of the structure are minimized.

Structure for measuring surface ions. - Test structures for measuring surface ions were prepared with and without a vapor plated layer. Both p on n and n on p type structures were prepared. They were sealed in dry N_2 (<15 ppm water) without a vacuum bake before sealing. The devices were subjected to -100 volts (on electrode B relative to electrode A in Figure 11) at room temperature for 66 hours and then the following currents were measured at 3 volts:

Not vapor plated		Vapor plated	
n on p	p on n	n on p	p on n
3.0×10^{-5} A	6.0×10^{-5} A	0.3×10^{-5} A	7.0×10^{-5} A
9.0×10^{-5}	3.0×10^{-5}	0.2×10^{-5}	0.06×10^{-5}
0.3×10^{-5}	5.0×10^{-5}	0.5×10^{-5}	0.7×10^{-5}
0.3×10^{-5}	8.0×10^{-5}	0.8×10^{-5}	0.2×10^{-5}

Next, +100V was applied for 24 hours and the following data were taken:

Not vapor plated		Vapor plated	
n on p	p on n	n on p	p on n
30×10^{-5} A	3×10^{-11} A	10×10^{-5} A	4×10^{-11} A
20×10^{-5}	5×10^{-11}	10×10^{-5}	4×10^{-11}
20×10^{-5}	4×10^{-11}	40×10^{-5}	4×10^{-11}
40×10^{-5}	5×10^{-11}	10×10^{-5}	4×10^{-11}

The data show that:

1. A negative voltage on electrode B creates a channel on the p-on-n structures and does not on the n-on-p structures.
2. A positive voltage on electrode B creates a channel on the n-on-p structures and not on the p-on-n structures.
1. The n on p structures have relatively high current levels because the positive charge always present in SiO_2 layers creates shunting channels;
2. There is no significant effect of the vapor plating on either p on n or n on p structures; on the level of the measured currents.
3. The high sensitivity of the structure to surface ion motion has been demonstrated.

Further work is called for in the following areas:

1. Time constants and activation energies associated

with the migration of surface ions should provide a more complete understanding of the kinetics and exact species of the charge.

2. The effects of vacuum baking before hermetically sealing the package should be more completely determined.

Hall measurements. - The Hall voltage test structure that was designed into the test structure chip is almost two orders of magnitude smaller than that reported by Colman and Mize (Ref. 21). The demonstration of the effectiveness of such a small structure makes it attractive as one of a number of test structures on a chip that might be included on each wafer.

Sample Hall data taken on a p on n structure are given in the following table. The voltage between the drain and the source is 1 volt in each case. The voltages are those across the numbered terminals shown in Figure 19.

V_{gate}	I	$V_{2,6}$	$V_{3,7}$	$V_{2,3}$	$V_{6,7}$	$\frac{V_{2,6}+V_{3,7}}{V_{2,3}+V_{6,7}}$
20V	3.0μA	2.0mV	2.8mV	0.44V	0.42V	0.0054
30	6.0	2.0	4.0	0.43	0.45	0.0068
40	8.5	2.5	2.3	0.42	0.43	0.0057
60	13.5	8.0	2.0	0.40	0.43	0.012

The current was then reversed and the measurements were repeated:

V_{gate}	I	$V_{2,6}$	$V_{3,7}$	$V_{2,3}$	$V_{6,7}$	$\frac{V_{2,6}+V_{3,7}}{V_{2,3}+V_{6,7}}$
20V	4.0μA	2.0mV	2.3mV	0.40V	0.42V	0.0053
30	5.2	3.0	2.0	0.40	0.42	0.0061
40	8.0	3.3	1.6	0.40	0.42	0.0060
60	12.0	5.5	1.8	0.39	0.41	0.010

The values in the last column are one half of the Hall angle ($\theta/2$) because the distance between probes along the length of the sample is twice the width of the sample.

The Hall mobility is given by the equation (Ref. 27)

$$\mu = \frac{10^8\theta}{H}$$

where θ is the Hall angle and H the magnetic field in gauss.

Our magnetic field strength is 4200 gauss, and therefore,

$$\mu = 2.38 \times 10^4\theta,$$

and the value measured on the above sample was approximately $2.38 \times 10^4 \times 2 \times 0.006 = 285\ cm^2/V\text{-}sec$.

Transistors in a microcircuit array. - Several wafers were taken from the production line of PA7709 high performance operational amplifier integrated circuits. A special set of masks made it possible to delineate a metal pattern so that discrete transistors can be tested. The structure is shown in Figure 12.

A vapor-plated SiO_2 layer was deposited over the metal pattern on one-half of each wafer and contact cuts were made through this second insulation layer. A 6000 Å was deposited in 2 minutes at 400° C.

A number of transistor parameters were measured, before and after a bake at 175° C for five days under a reverse bias of 6 volts, on both the emitter and collector junctions of two pnp and two npn bipolar transistors.

The data are presented in histogram form in Figures 22 through 37. Transistors #1 and #2 are similar npn double-diffused transistors. Transistor #3 is a pnp substrate collector transistor and transistor #4 is a pnp lateral transistor.

The substrate collector pnp bipolar transistor is a single-diffused transistor in which a part of the p-type substrate region becomes the collector, a part of the n-type epitaxial layer becomes the base region, and the

TRANSISTOR NO. 1

Not Vapor Plated

Before

After

TRANSISTOR NO. 2

Not Vapor Plated

Before

After

Vapor Plated

Before

After

100 200 300 400

Vapor Plated

Before

After

100 200 300 400

TRANSISTOR NO. 1

Not Vapor Plated

Before

After

TRANSISTOR NO. 2

Not Vapor Plated

Before

After

Vapor Plated

Before

After

100 200 300 400

Vapor Plated

Before

After

100 200 300 400

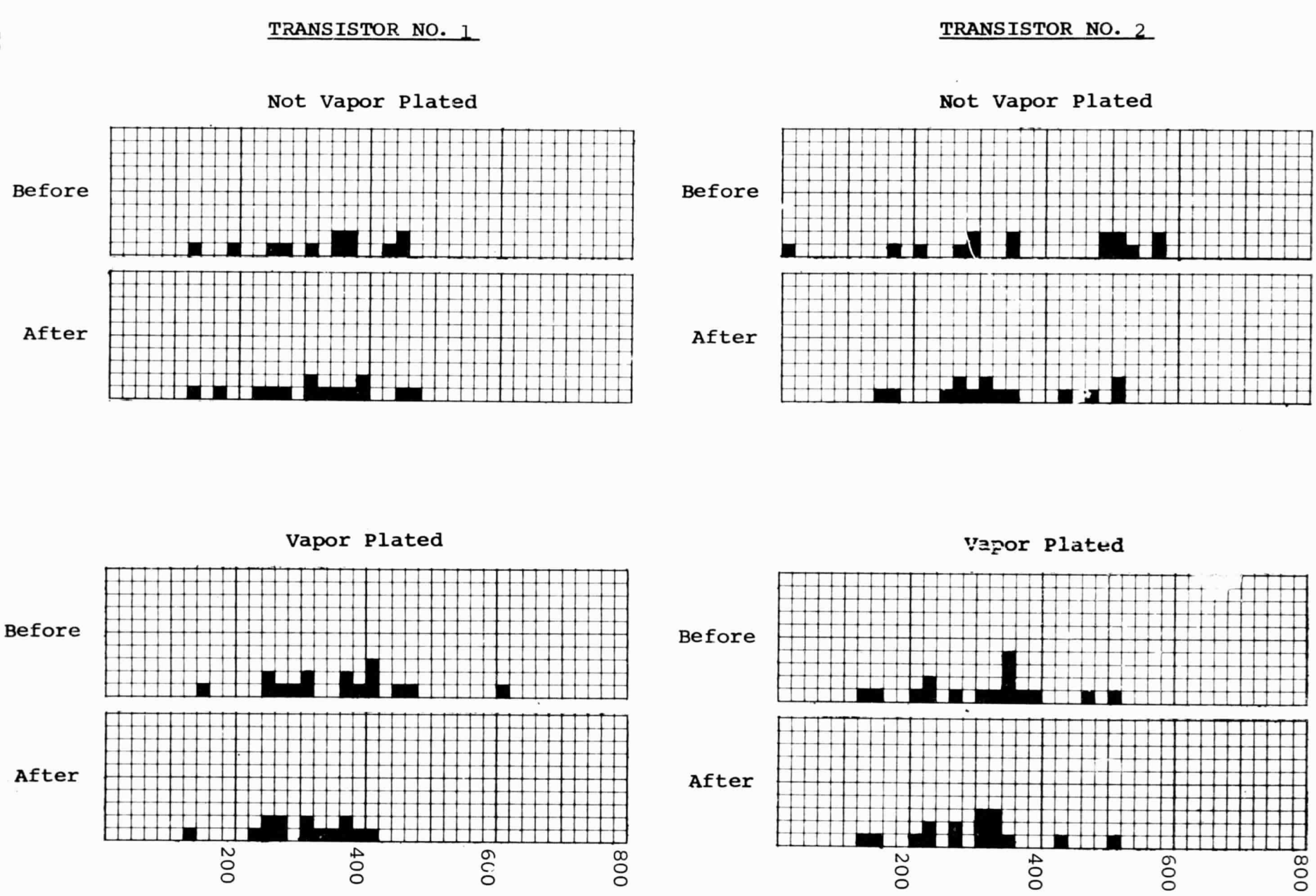


Figure 23. h_{FE} (1 mA, 3 V) of npn bipolar transistors.

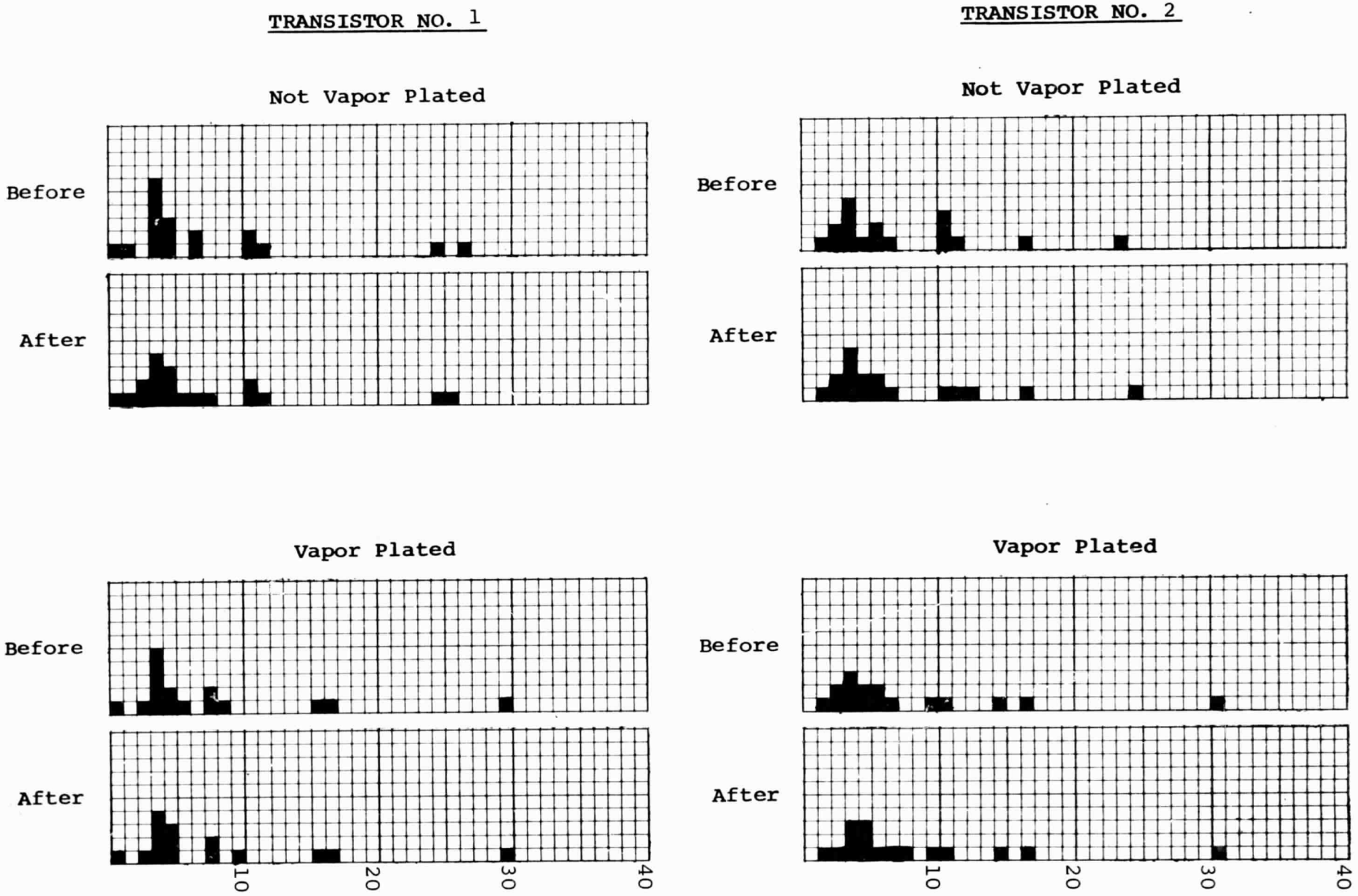


Figure 24. BV_{CEO} (volts) at 10 μA of npn bipolar transistors.

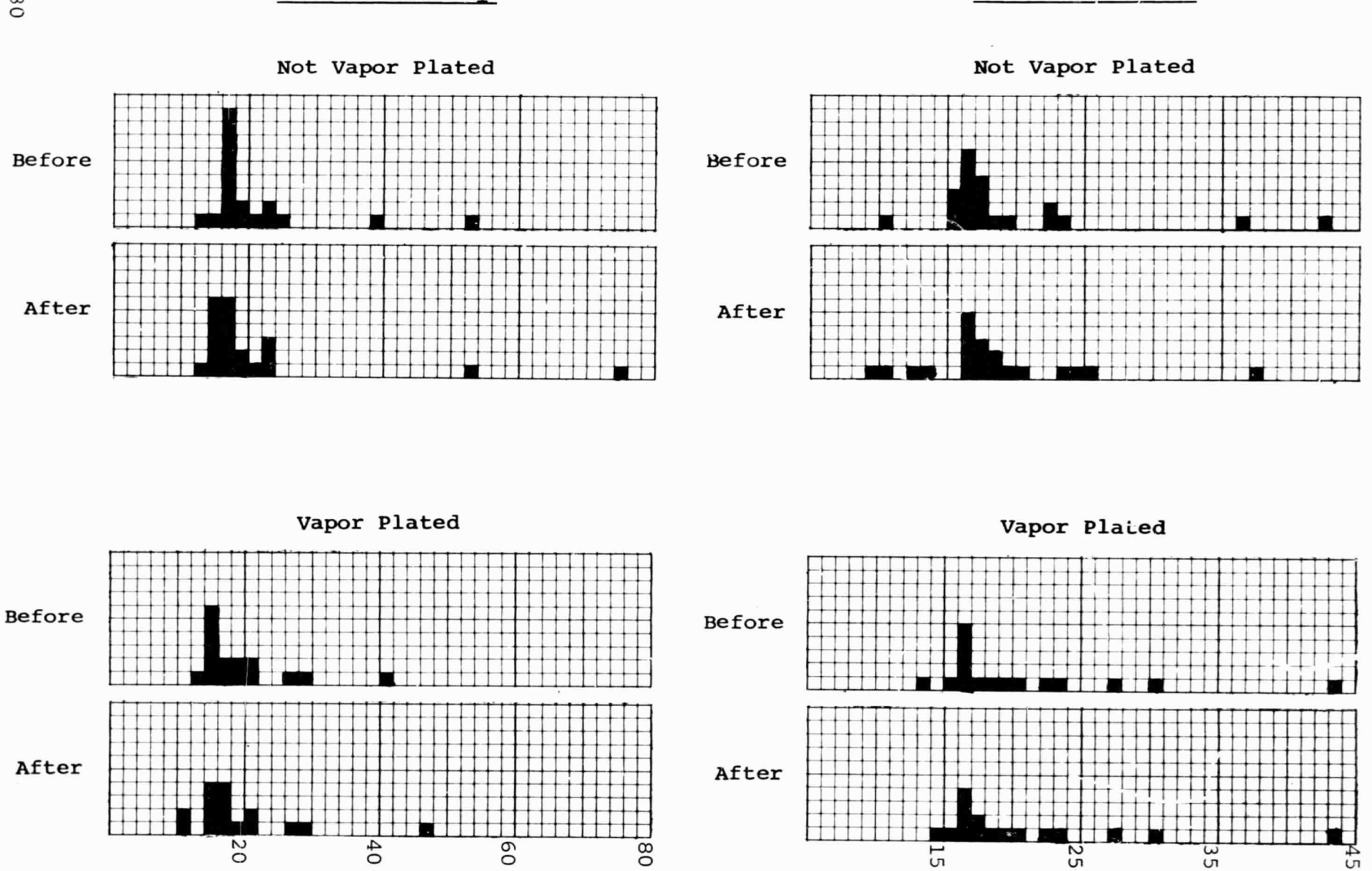


Figure 25. BV_{CBO} (volts) at 50 μA of npn bipolar transistors.

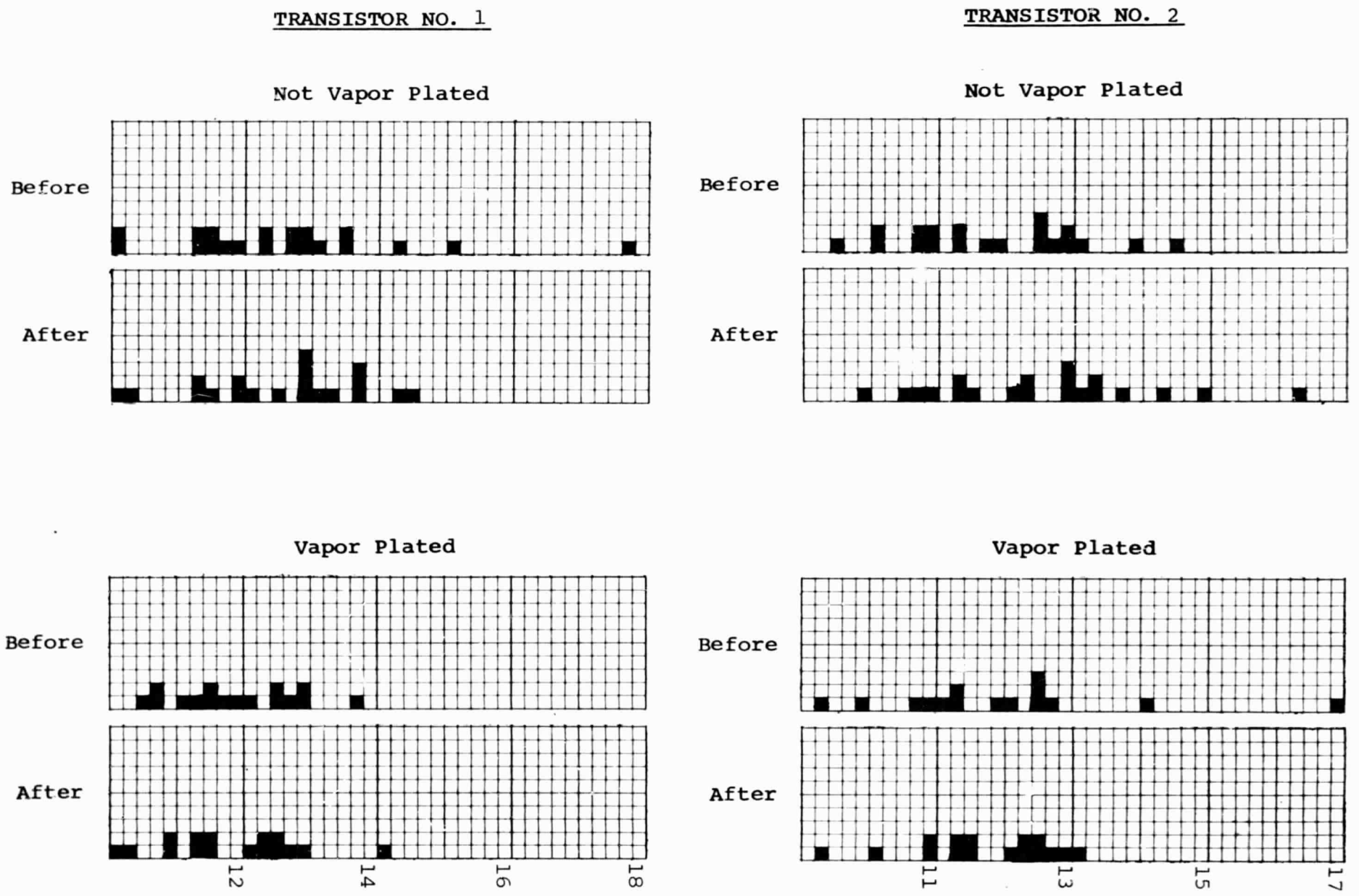


Figure 26. BV_{EBO} (volts) at 50 μA on npn bipolar transistors.

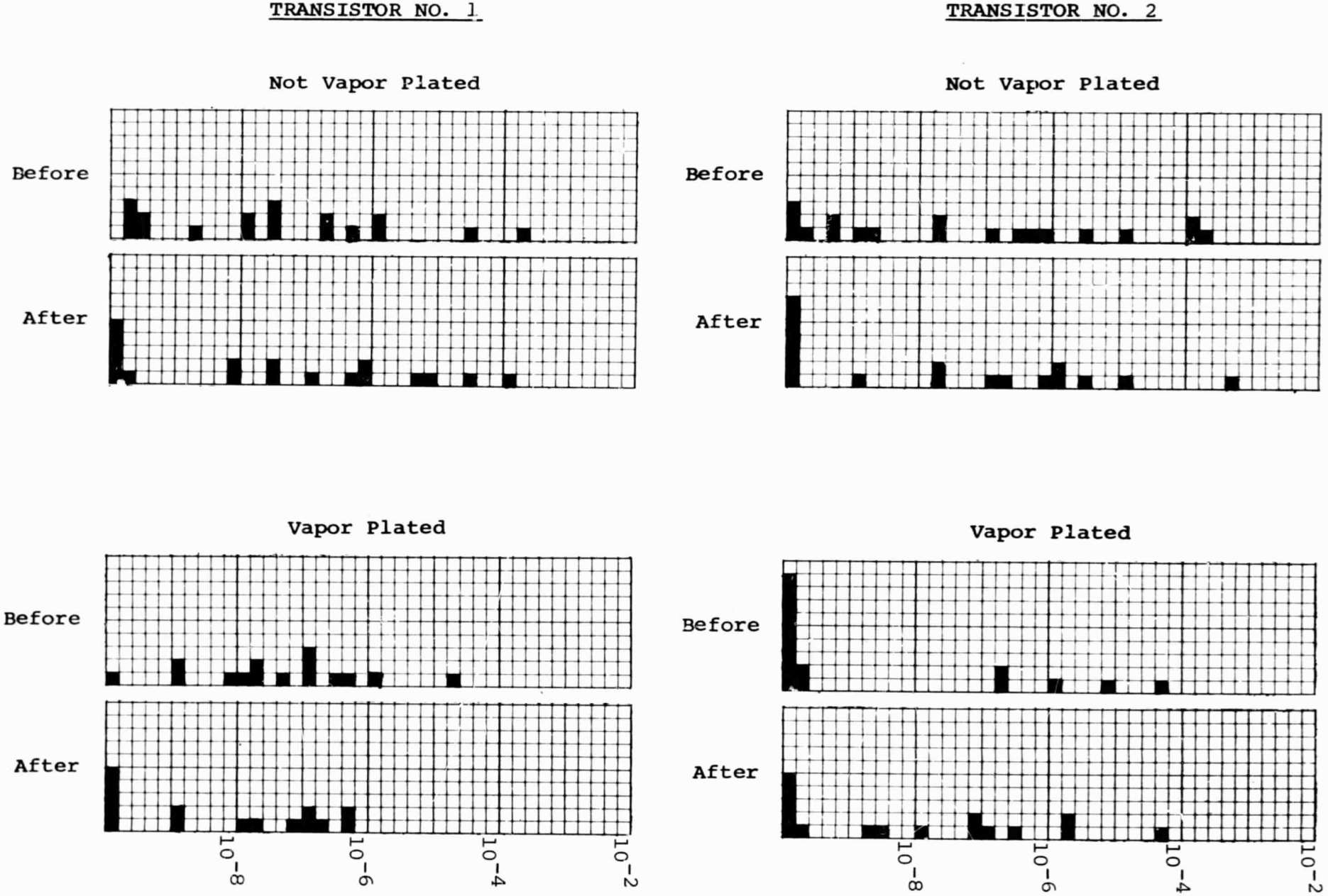


Figure 27. I_{CEO} (A) at 3 V of npn bipolar transistors.

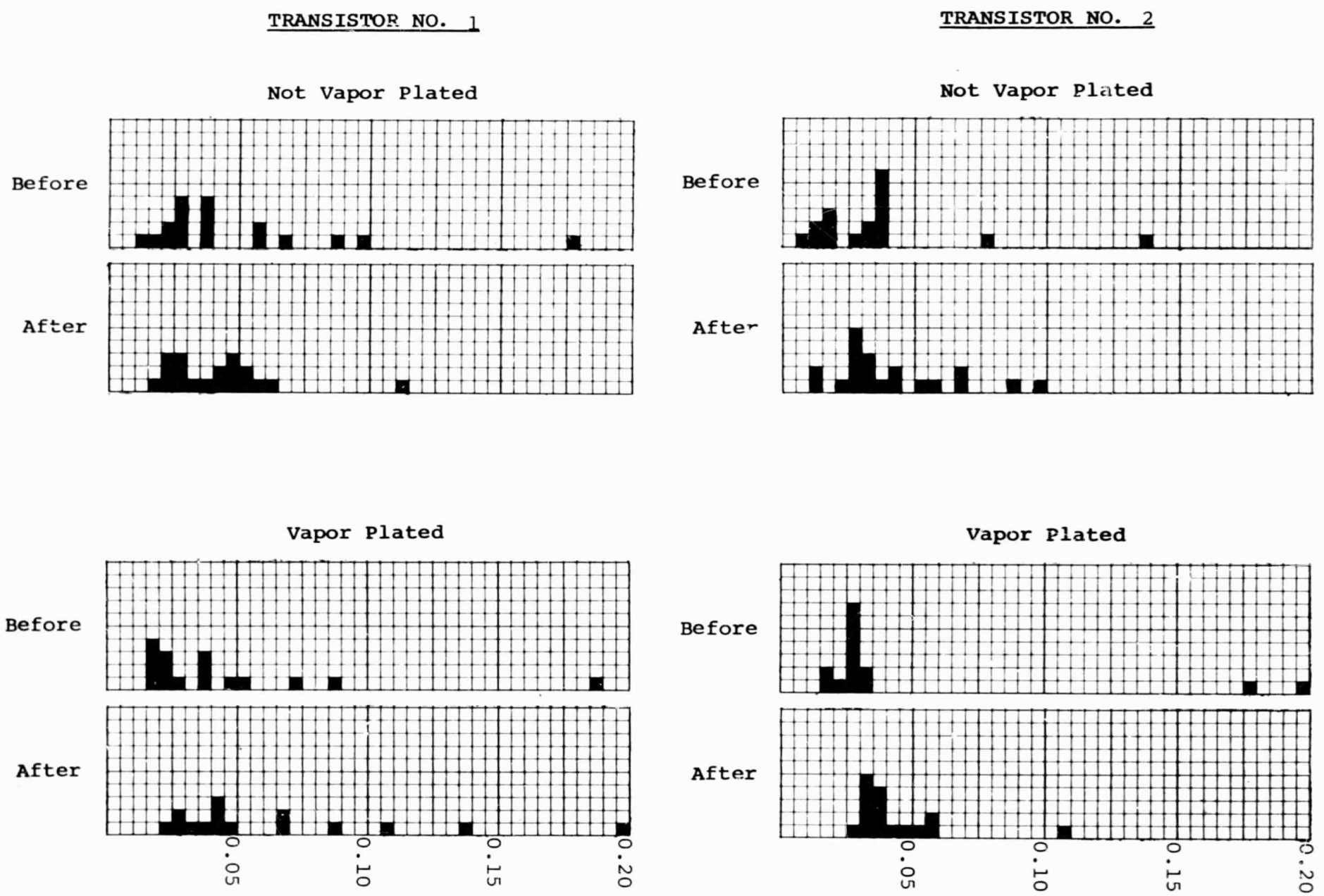


Figure 28. I_{CBO} (A) at 3 V of npn bipolar transistors.

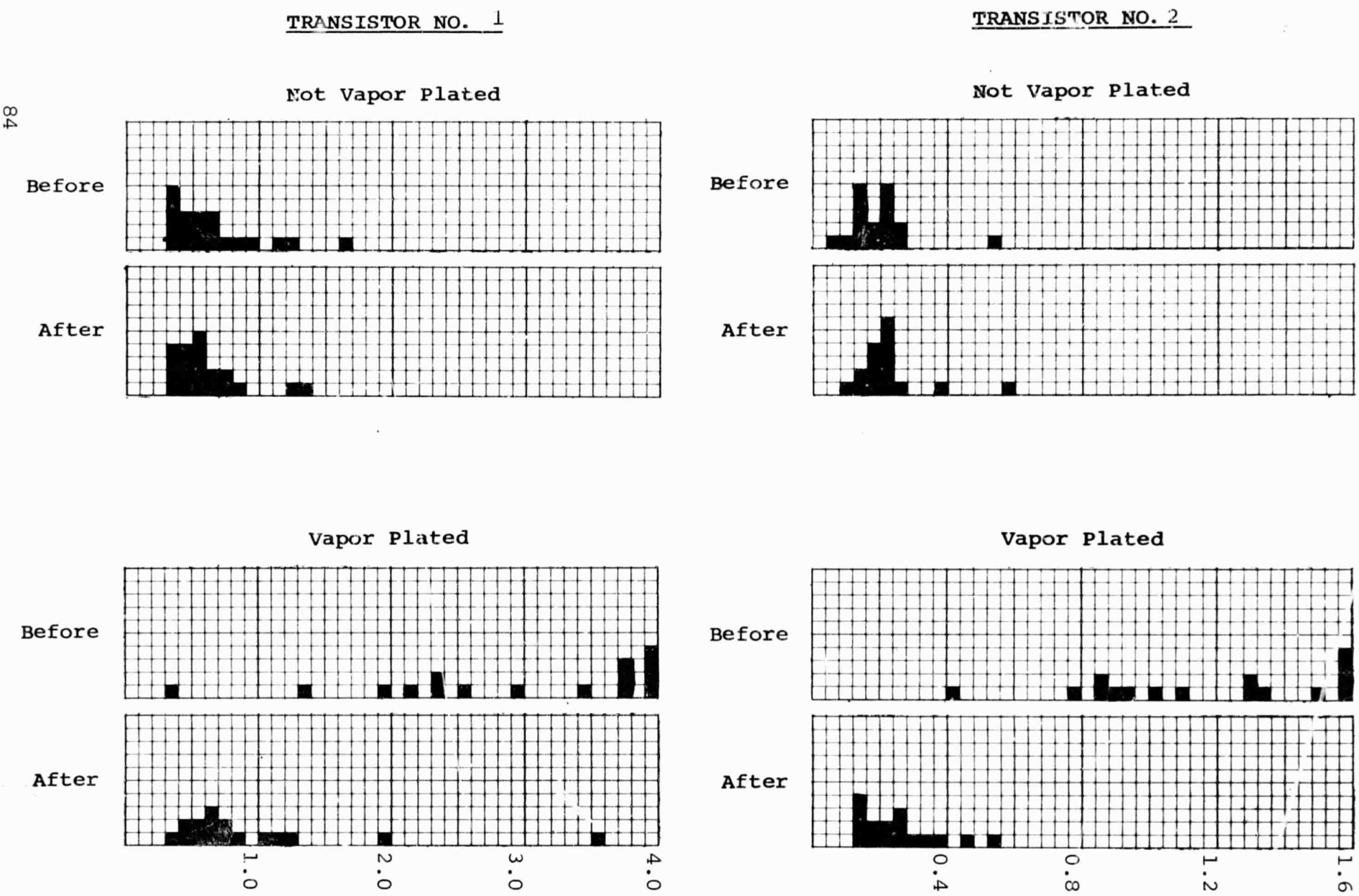


Figure 29. I_{EBO} (A) at 3 V of npn bipolar transistors.

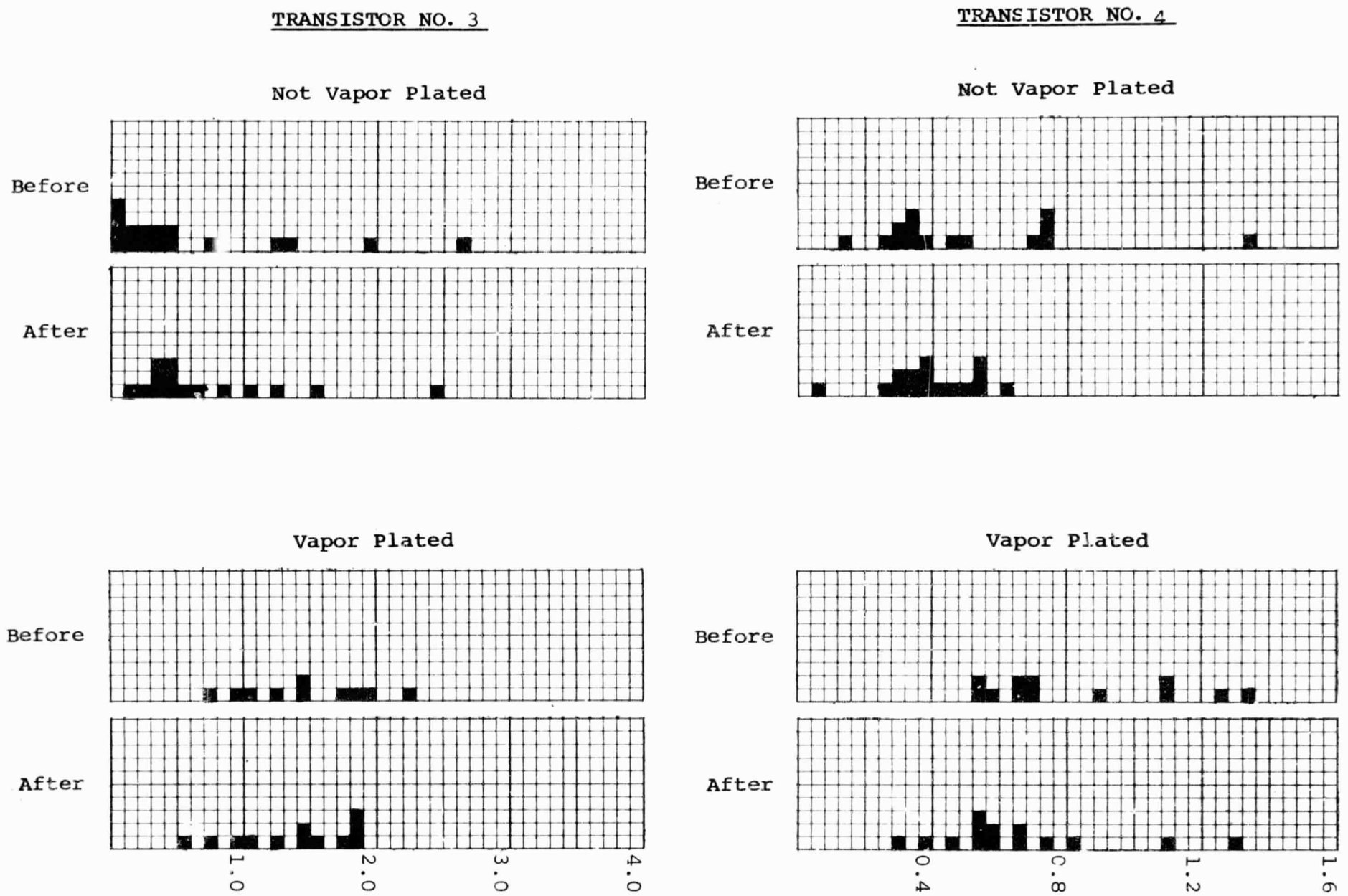


Figure 30. h_{FE} (1 μA, 3 V) of pnp bipolar transistors.

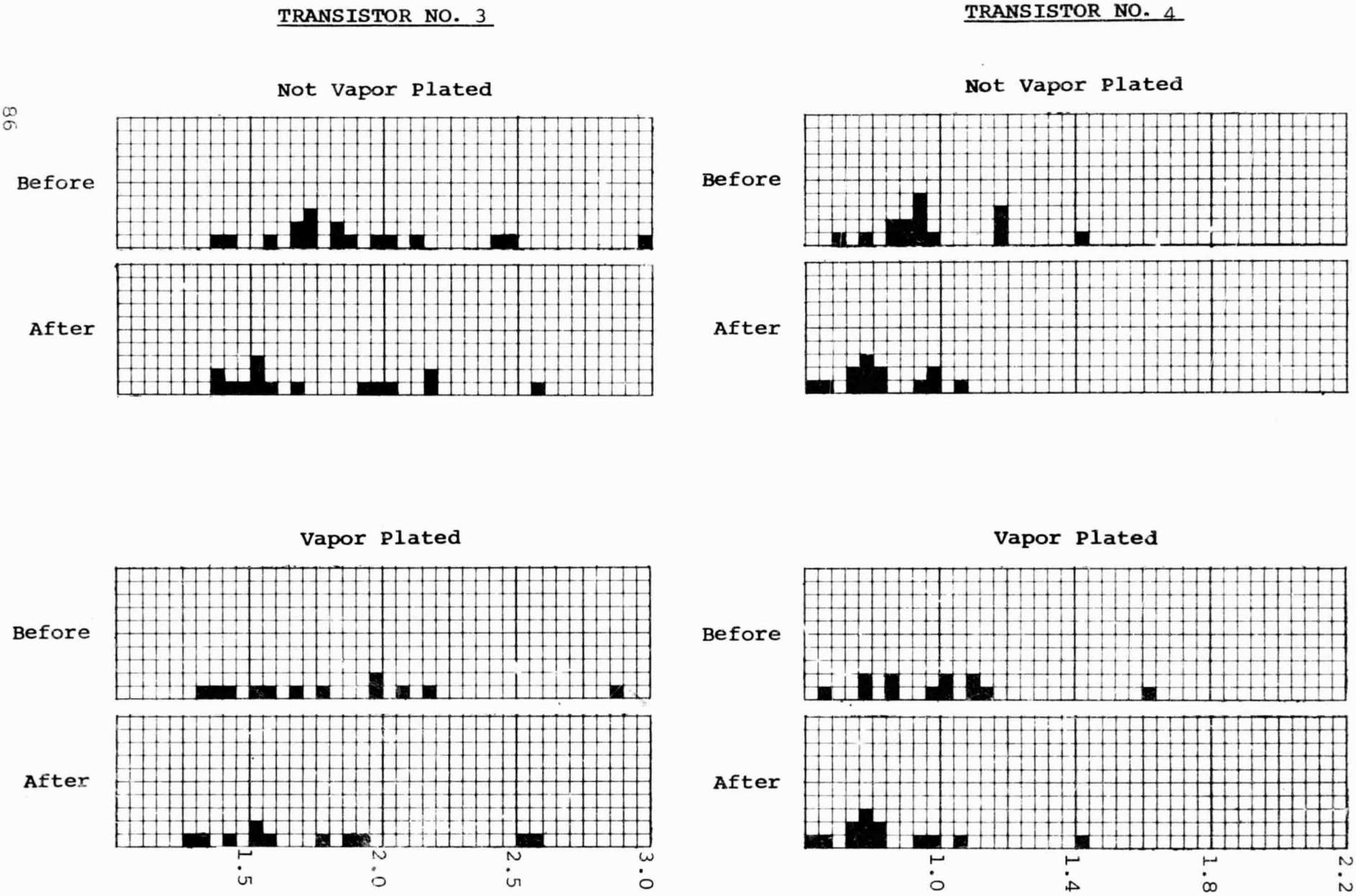


Figure 31. h_{FE} (1 mA, 3 V) of pnp bipolar transistors.

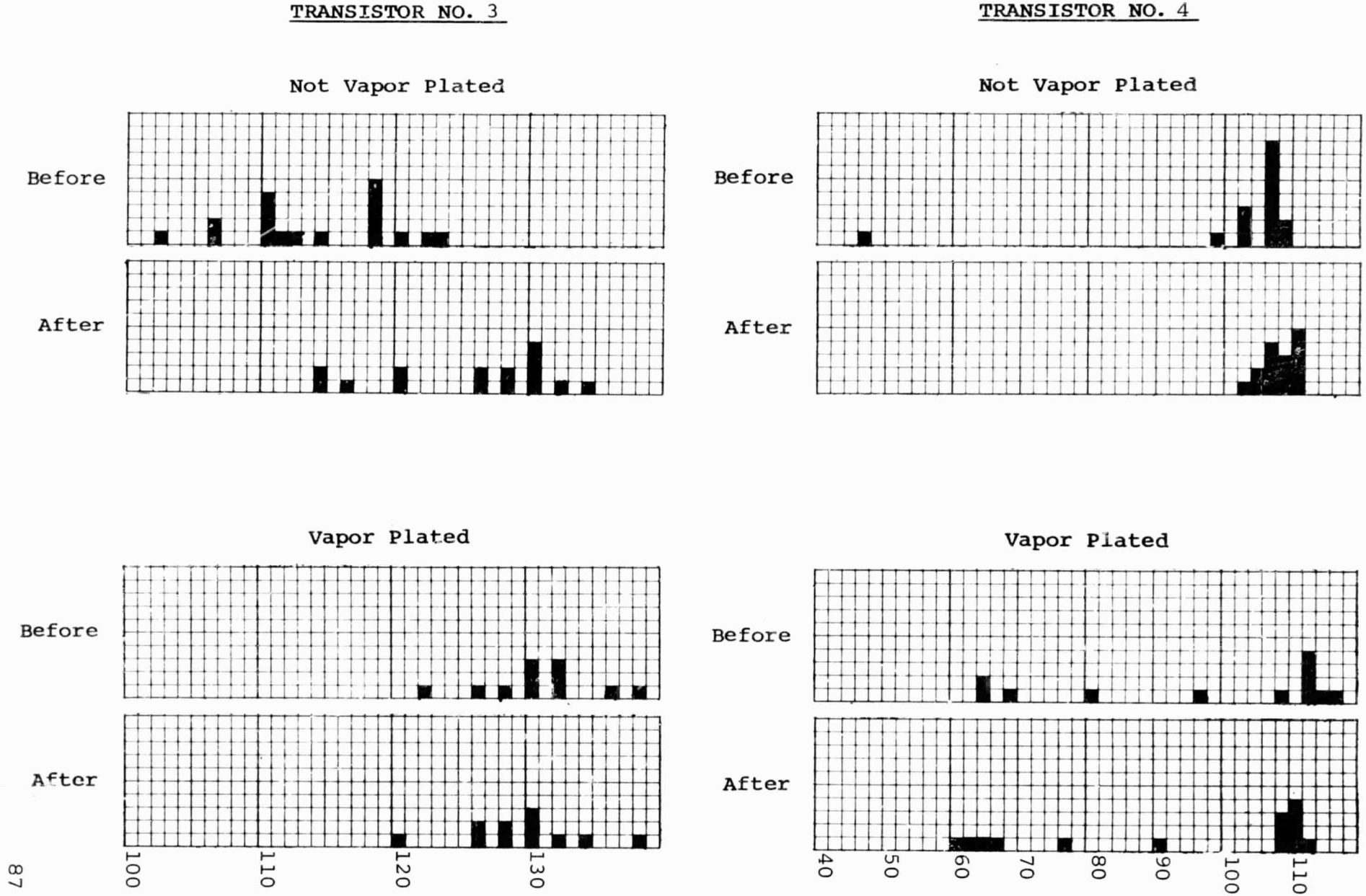


Figure 32. BV_{CEO} (volts) at 10 μA of pnp bipolar transistors.

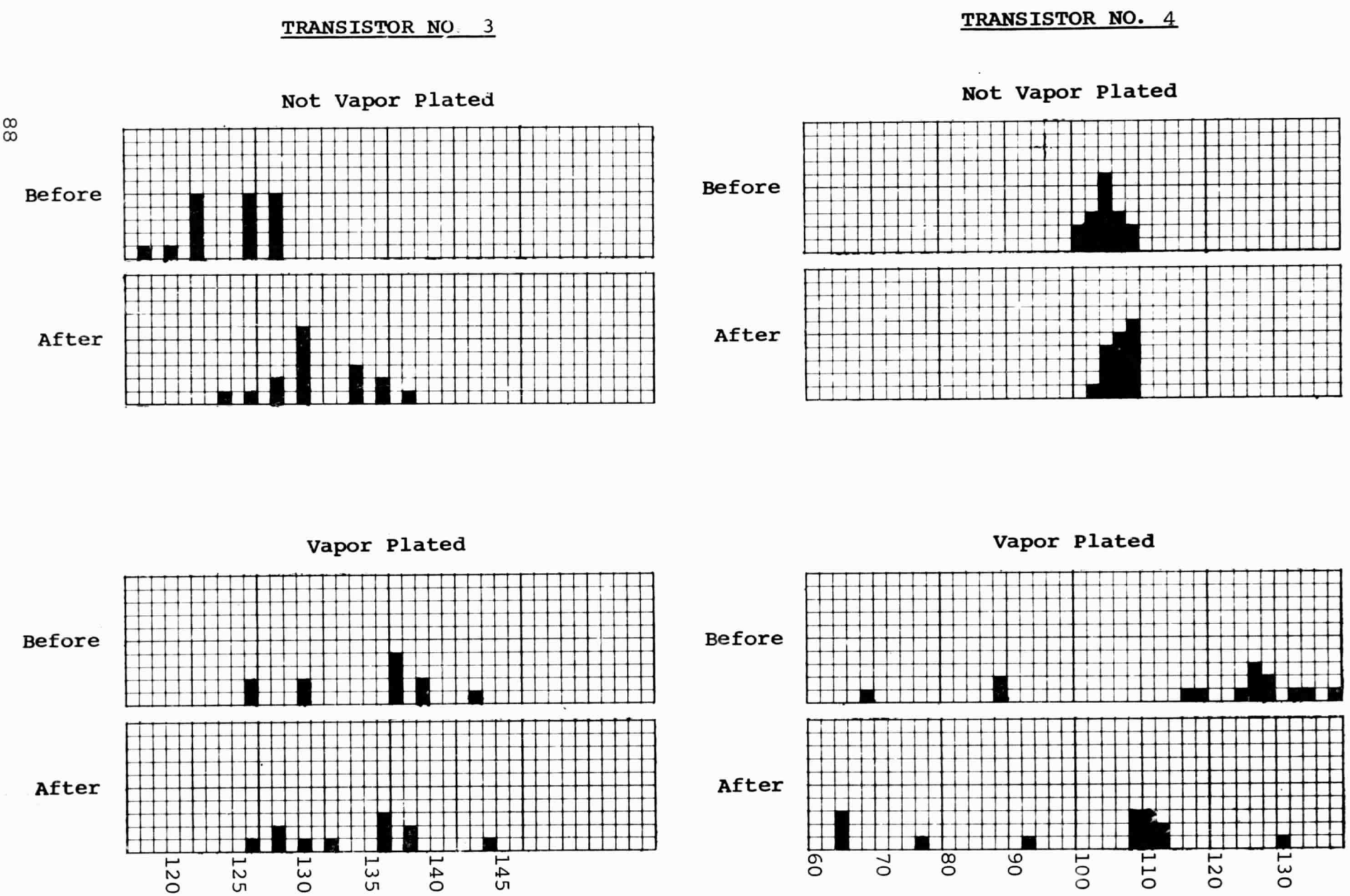


Figure 33. BV_{CBO} (volts) at 50 μA, 3 V of pnp bipolar transistors.

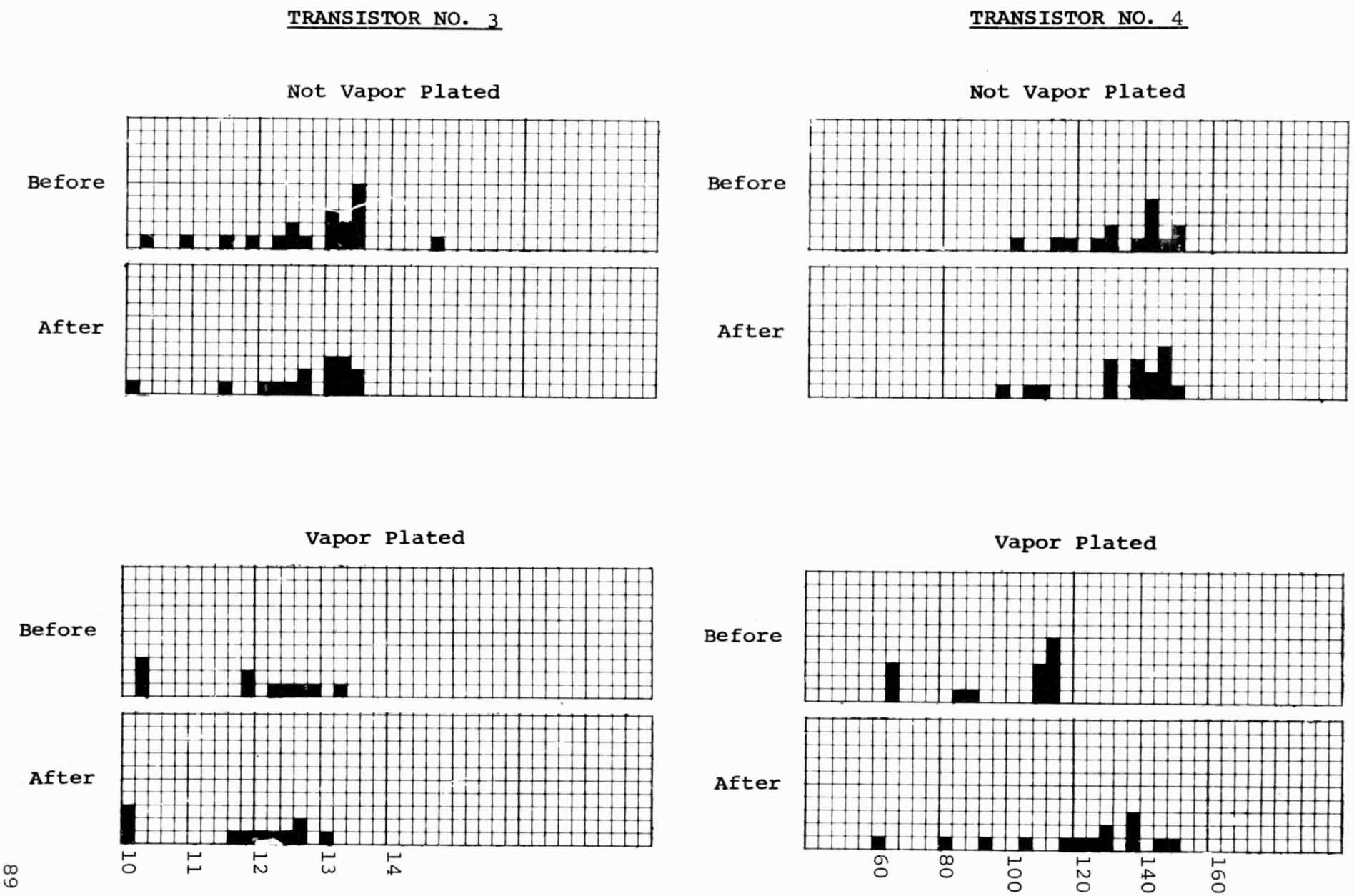


Figure 34. BV_{EBO} (volts) at 50 μA of pnp bipolar transistors.

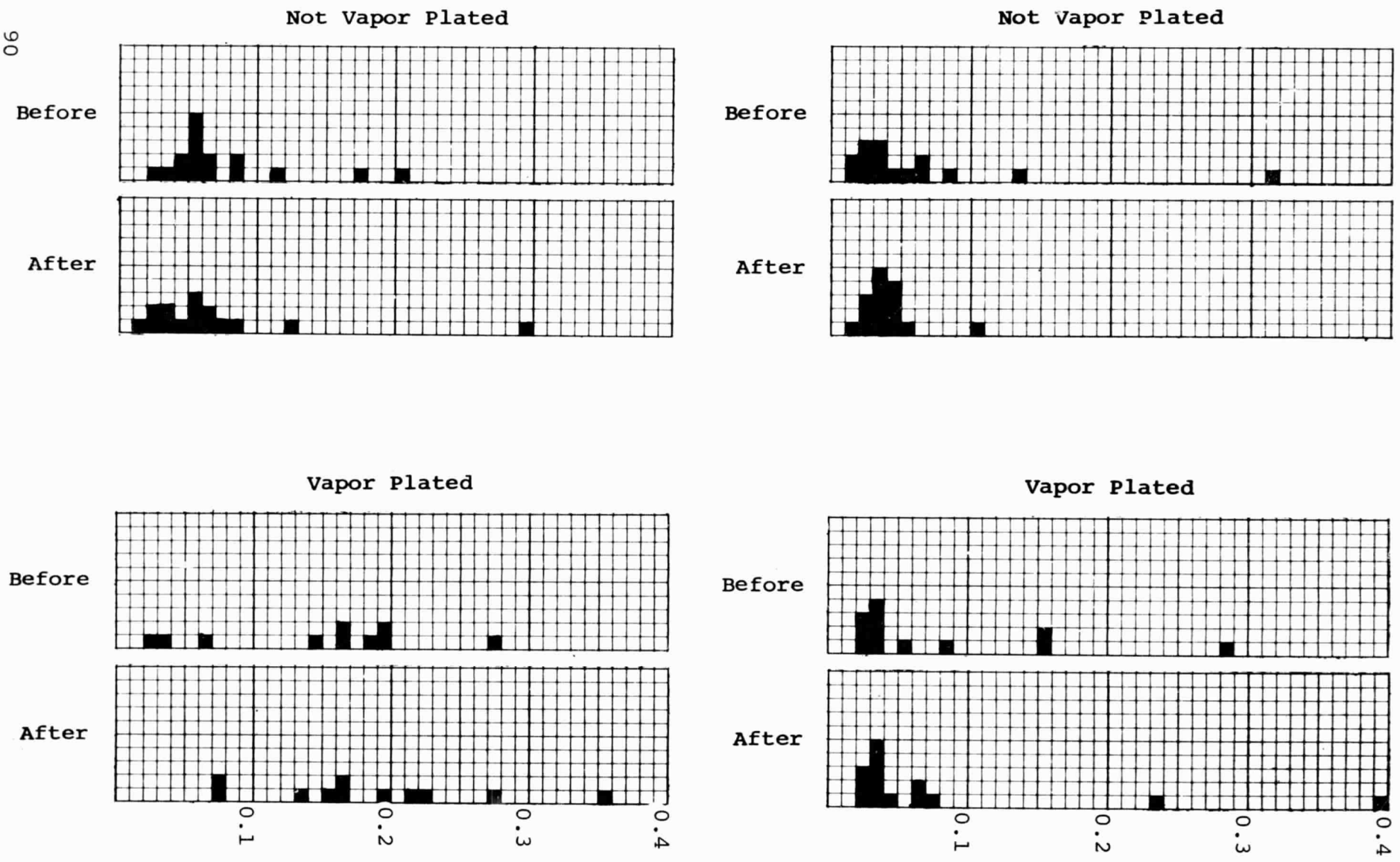


Figure 35. I_{CEO} (A) at 3 V of pnp bipolar transistors.

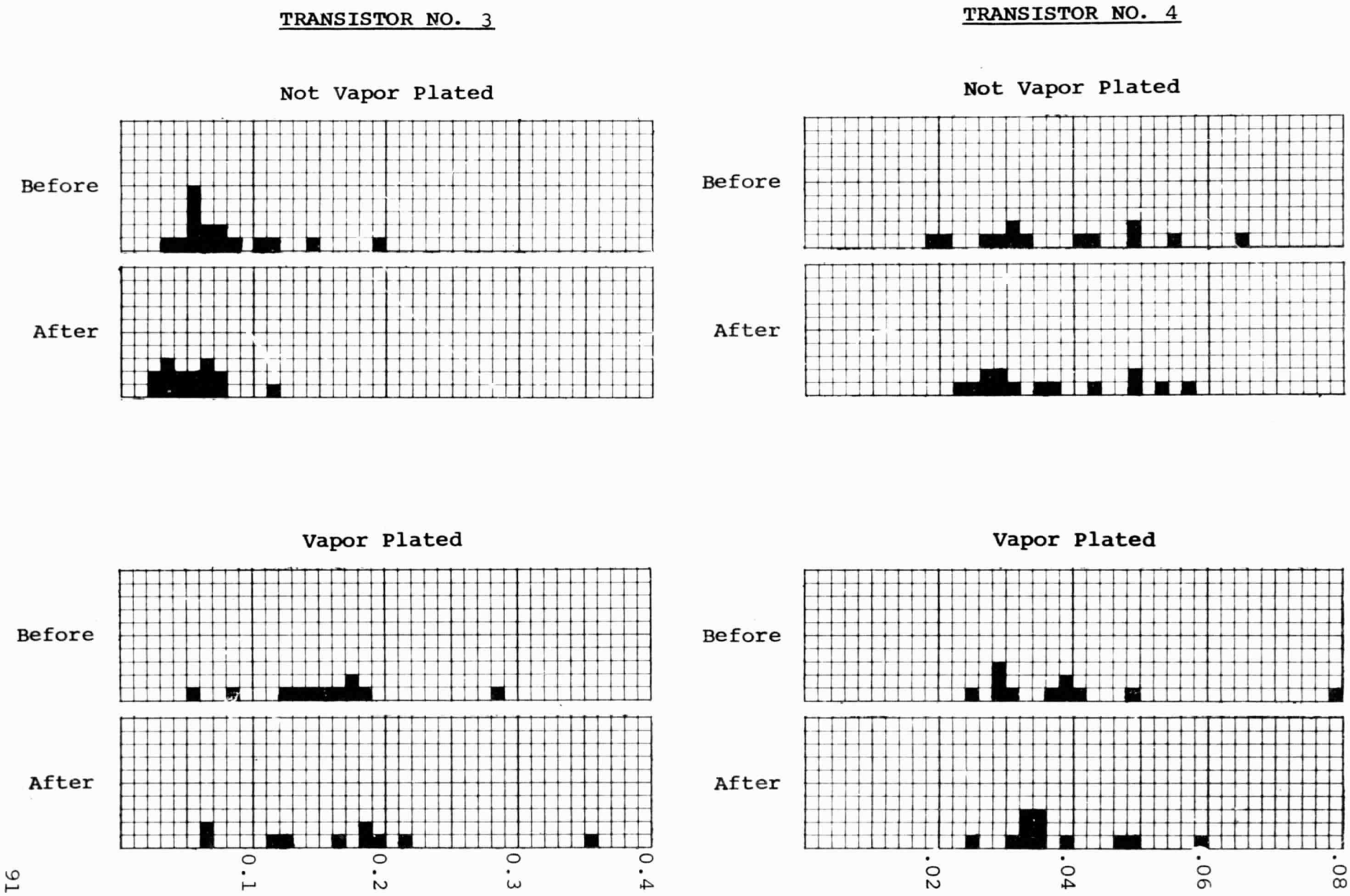


Figure 36. I_{CBO} (A) at 3 V of pnp bipolar transistors.

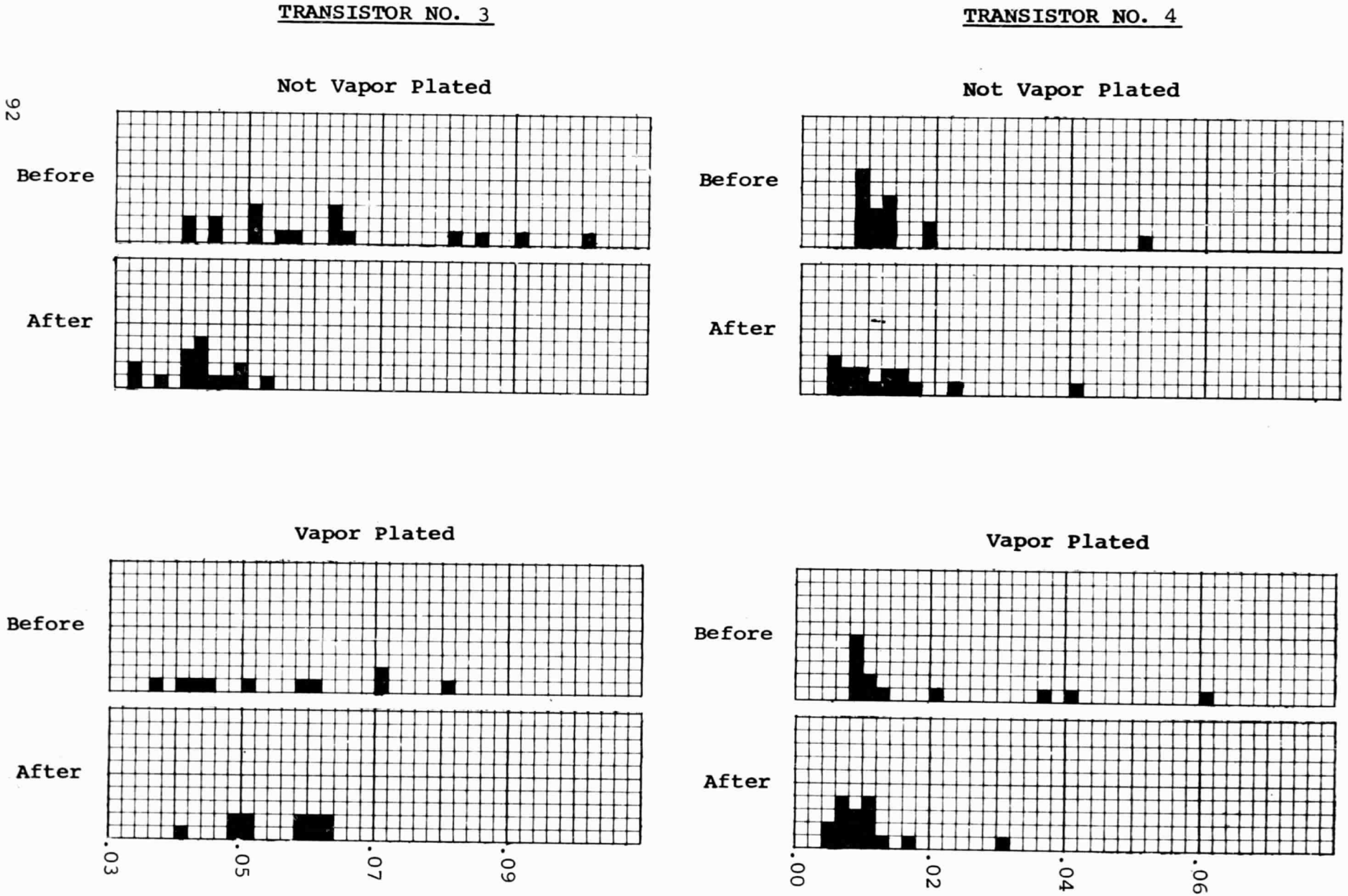


Figure 37. I_{EBO} (A) at 3 V of pnp bipolar transistors.

diffusion operation that forms the base region of the double-diffused npn transistor (formed in the same chip) forms the emitter.

The lateral transistor is formed by using two diffused regions, formed by a single diffusion operation, as the emitter and collector. Lateral transistors are described in references 28 through 31.

The data for npn bipolar transistors show that:

1. The vapor plating degraded the I_{EBO} (at 3V) initially but the bake recovered these reverse diode currents to the level of the devices without the vapor-plated layer;
2. The presence of a vapor-plated layer degrades the h_{FE} measured at 3 V and 3 μA;
3. The bake substantially degrades the h_{FE} measured at 3 V and 3 μA, regardless of the presence of the vapor-plated layer;
4. Neither the bake nor the vapor plating operation affected the following parameters:

   BV_{CBO} at 50 μA

   BV_{EBO} at 50 μA

   BV_{CEO} at 10 μA

   I_{CBO} at 3 V

I_{CEO} at 3 V

h_{FE} at 3 V & 1 mA

The data for pnp transistors show that:

1. The h_{FE} measured at 1 μA and 3 V is improved by the presence of the vapor-plated SiO_2 layer. At 1 mA and 3 V the h_{FE} is not affected by the presence of the vapor-plated layer;
2. Vapor plating increases the BV_{CEO} of the substrate collector pnp transistor and decreases the BV_{CEO} in the lateral pnp transistor;
3. Vapor plating increases the spread of values of both BV_{CBO} and BV_{CEO};
4. The BV_{CBO} and BV_{CEO} data show the effect of vapor plating to be mainly that due to the heat treatment. That is, the 300° C bake for five days produced an effect quite similar to that of the vapor plating which was done at 400° C for 2 minutes;
5. I_{EBO} is improved by the 300° C, 5-day bake. This improvement is more pronounced on devices without the vapor-plated SiO_2;
6. Vapor plating increases the I_{CBO} and the I_{CEO} of the substrate collector pnp transistor.

CONCLUSIONS

A firm practical basis has been established for studying the fundamental electrical properties of the $Si-SiO_2$ interface of structures having two dielectric layers on silicon.

1. All of the effects of the electrical properties of insulator layers and of insulator-semiconductor interfaces on the performance and reliability of semiconductor devices and microcircuits have been reviewed and summarized.

2. A useful model has been developed that combines into a single chart all of the types of electrical species, in an insulator or at the insulator-silicon interface, that influence the electrical properties of the semiconductor.

3. Two mask sets have been designed and built for making test structures designed for the measurement of the fundamental electrical properties of the insulator-semiconductor interface (surface potential, surface recombination velocity, carrier mobility in an inversion layer and slow and fast states).

4. Equipment has been built and proven effective for taking measurements on the test structures.

5. These test structures and the equipment provide a capability on a single 70 x 70 mil^2 chip, which might be included on each wafer on a production line, to measure:

a. The capacitance-voltage relationship on MOS capacitors. The C-V relationship yields the surface potential of the semiconductor, the insulator layer thickness (assuming the capacitor area and the dielectric constant are known) and the average dopant density in the semiconductor near the surface. Combined with drifting treatments at several temperatures under applied voltages, the C-V data taken on MOS capacitors provides a measure of the density of mobile charge and of slow states or traps;

b. The drain-current gate-voltage relationship of MOS transistors. The transconductance is a measure of the carrier mobility. The threshold voltage - when compared with the point of inversion taken on an MOS capacitor - is a measure of the density of fast states that immobilize carriers in the inversion layer;

c. The C-V relationship on MOS capacitors with a narrow-line structure with a large ratio of perimeter to area. This type of structure provides the means of measuring the effects of migration of impurities from areas adjacent to areas beneath metal layers;

d. Hall measurement on inversion layers. MOS transistors shaped in the form used for Hall measurements provide

a means by which the carrier density and carrier mobility can be measured in inversion layers;

e. The surface recombination velocity. The surface recombination velocity is calculable from the dependence of the reverse current of a p-n junction on the voltage of a gate electrode of known area surrounding and slightly overlapping the junction;

f. The presence of surface ions. Surface ions can be studied by measuring the variation in resistance between two p-n junctions due to surface ion drift between two parallel conductors overlying the oxide and the junctions;

g. Diode characteristics. Diode reverse currents are a simple and sensitive measure of differences in carrier generation rates at the surface of the semiconductor. Diode breakdown voltages are a simple sensitive measure of effects of oxide charge (both mobile and immobile) on field strengths in a depletion layer near the surface of the silicon;

h. The characteristics of discrete transistors in the configuration of complex microcircuits, that is, transistors that have been prepared by the complete and complex series of processing steps used for bipolar microcircuit production.

6. Capacitance-voltage measurements on MOS capacitors were used to compare insulator layers of various types of material and of deposition process. The two most promising oxide layers suitable for second layer insulation are vapor-plated SiO_2 and vapor-plated mixed SiO_2-Al_2O_3. These two types of oxides have lower immobile charge densities, lower mobile charge densities and break down less frequently under an applied voltage than evaporated Al_2O_3, vapor-plated Al_2O_3, r-f sputtered SiO_2, or titanium oxide.

7. The effect of mobile ions present from a second layer can be reduced by a phosphosilicate layer between the first and second oxide layer.

8. The effective charge density in either vapor-plated Al_2O_3 or vapor-plated mixed Al_2O_3- SiO_2 overlying (in each case) thermally grown SiO_2 is frequently found to be negative in contrast to the positive charge density always found in thermally grown oxides. A substantial part of this apparent negative charge may be due to an insulator-insulator contact potential. It has not been determined whether the negative charge is mobile or immobile.

9. Contaminants migrate from regions adjacent to the regions beneath a metal layer during a 300°C bake for hundreds of hours under various conditions of applied bias as follows:

a. There appears to be no significant influence on the immobile charge density due to the migration of contaminants;

b. Positive ions (both at 25°C and 300°C) migrate to regions underlying metals. This occurs to a much greater extent when the applied bias is positive than when it is zero or negative.

c. The migration of positive ions is similar when there is a layer of vapor-plated SiO_2 overlying the metal pattern and the thermally grown SiO_2, and when there is none. One might infer from this that the source of the mobile ions is from the photolithographic processes. This problem is minimized in today's MOS microcircuits because n-channel devices contain phosphosilicate diffusion layers, and p-channel devices are not subjected to positive voltages.

d. The observations concerning charge which is mobile at room temperature and that which is mobile at 300°C

are similar. This is consistent with the belief that the charge which is mobile at room temperature is a form of sodium which is more mobile than that observed at 300°C.

10. The deposition of a layer of vapor plated SiO_2 over either bipolar or MOS transistors (metalized in each case) does not significantly alter the initial performance of the devices. In this connection, one should guard against the illusion, based on only the initial performance of the device, that the device reliability has not been degraded.

11. The following surface ion characteristics have been observed:

a. In a wet (N_2 jet from a water bubbler) ambient, significant surface ion motion occurs in one minute at room temperature. In a dry ambient, surface ion motion requires hours.

b. A phosphorus-rich surface is hygroscopic; consequently surface ions are abundant, quite mobile and relatively influential on the properties of the underlying silicon. A pure (vapor-plated) SiO_2 layer is comparatively free of surface ion motion. A borosilicate surface appears to

be similar to the pure vapor plated SiO_2. These results appear to be consistent with the relative wettability observed for these three types of surfaces in etching experiments.

c. Surface ion effects appear to occur in at least three ways. One, a conductor with a negative potential can attract positive ions to the region near by. Two, a surface that is conductive due to the presence of surface ions is, in effect, an extended area of a conductor and therefore can assume the same potential as that of the conductor, i.e., nearby regions have a pile-up of charge of the same polarity as that on the conductor. Third, surface ions may drift up and over a metal to a position where they cannot influence the underlying semiconductor.

12. The structure we developed for measuring the effects of surface ions is simple and useful and, we believe, has not been discussed in previous literature. Its value lies in its practicality and sensitivity rather than in its clarity of theoretical interpretation. An analysis of the data should take the following into account:

a. Ions moving through the oxide would influence the data,

b. Surface ions may influence the data either by influencing channel formation or by effecting the surface potential and the carrier generation rate in the depletion layer of a reverse biased junction,

c. The data is time-dependent and the time constant can be expected to depend on the applied field strength, on the humidity in the ambient and on whether the insulator layer covers the edge of a metal layer smoothly.

13. The feasibility of the test structures, the test equipment, and the testing techniques for the intended purposes has been established, in experiments involving samples with a vapor-plated SiO_2 second layer and with control wafers without the second layer, and involving p-type diffused regions in n-type substrates, and n-type diffusions in p-type substrates. While time did not permit a complete series of experiments with the test structures designed and built during this program, the following conclusions can be drawn from the data that was collected:

a. The initial immobile and mobile ($25^{\circ}C$ and $300^{\circ}C$) charge densities were very similar for both types of substrate, and with and without the second insulator layer;

b. Measurements of the effects of a bake, at 300°C for five days under either a positive or a negative applied bias, on the charge densities in capacitors having narrow line widths to maximize the effects of contaminant migration beneath the metal show no significant differences due to differences in conductivity type or due to vapor plating.

c. Preliminary data was taken on MOS transistors. The results should be supplemented with additional information. A 300°C bake appears to have reduced the g_m of the P-MOST's and increased it slightly on N-MOST's. The threshold voltage on the P-MOST increased from 0 to -12 volts and that of the N-MOST was hardly changed.

d. The voltage at the onset of inversion in the MOS capacitors has been found to be equal to the threshold voltage of the transistors, indicating that the fast state density is negligible;

e. Surface recombination velocities have been measured on n on p diodes to be 10-21 cm/sec, and on p on n to be 23-37 cm/sec;

f. The effects of surface ions are very sensitive to the ambient moisture;

g. It has been demonstrated that Hall measurements can be made on the inversion layer in specially designed MOS transistors whose dimensions are almost two orders of magnitude smaller than those reported in the literature. The Hall mobility was measured to be 285 $cm^2/V\text{-}sec$ on a p on n-type structure having no vapor-plated layer;

h. Measurements taken on double diffused npn bipolar transistors, pnp substrate-collector bipolar transistors, and lateral pnp bipolar transistors on production microcircuit wafers show that vapor plating does not seriously degrade the devices either initially or during a 300°C bake for 5 days under 6 V of reverse bias on both the emitter and collector.

The effects of the vapor plating that were observed were similiar to the effects of the 300°C bake. It would appear that the effect of the vapor plating is mainly due to the heat treatments involved in forming the vapor-plated layer.

Either the heat treatment or the vapor plating decrease the low-current h_{FE} of the npn bipolar transistors and increase it on pnp bipolar transistors. This can be explained as being due to an increase in

effective charge in the oxide. This increase makes the surface potential less p-type in the base region of the npn transistor and makes the surface potential more n-type in the base region of the pnp transistor. Because the surface recombination velocity is higher in nearly intrinsic material than in either strongly p- or n-type regions (ref 32), both the heat treatment and the vapor plating increase the surface recombination velocity in the base of the npn device and decrease it in the base region of the pnp device. This yields the observed decrease in the h_{FE} in the npn transistor and the observed increase in h_{FE} in the pnp transistors.

Vapor plating increases the BV_{CEO} of the substrate collector pnp bipolar transistor and decreases the BV_{CEO} of the lateral pnp transistor.

RECOMMENDATIONS

We recommend that the capability that has been demonstrated herein be applied to a continuing effort to further refine and improve the understanding of the mechanisms associated with the failure modes of multilevel LSI circuits. Design rules should be established to improve the performance and to assure the reliability of LSI circuitry. The continuing program should include the following:

1. The relative merits of the two most promising second layer insulator materials - vapor-plated SiO_2 and vapor-plated mixed SiO_2-Al_2O_3 should be determined;
2. It should be established whether the use of purer source material makes r-f sputtered SiO_2 a worthy competitor of the vapor plated SiO_2 layers. If so, determine its relative merits;
3. Beyond the feasibility studies, empirical data should be generated to provide a better measure of the reproducibility of the observed effects;
4. Information should be developed for optimizing the individual techniques for evaluating the fundamental

electrical properties of oxide semiconductor interfaces so that the most meaningful, sensitive and useful data are obtained;

5. A relative measure of the value and sensitivity of each technique for comparing and controlling the properties of insulator layers might be established.

6. Design rules for building better performing and more reliable multilevel LSI circuitry should be established.

7. The extent to which photolithographic processing imparts mobile ions to oxide layers should be more clearly determined.

8. The effect of the spacing between two parallel conductors over an oxide surface, on the degree to which surface ions pile up should be more clearly understood. An answer should be developed for the question of whether a wider spacing decreases the surface ion pile-up because the field strength along the surface is lower or does it increase the pile-up because charges are "collected" from a larger area.

9. The voltage, temperature and time dependence of surface ion effects should be studied to attain a better understanding of surface ion behavior.

10. The effects of different surface treatments of different surface ion behavior should be studied.

11. Possible initiation of an effort to evaluate the significance of mobile ions at an interface between two insulator layers.

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NEW TECHNOLOGY APPENDIX

To conform to the requirements of the New Technology clause of Contract NAS12-544, a review meeting was held to determine the reportable items. Personnel participating in the review included G. L. Schnable, the Program Manager, and E. S. Schlegel, the principal investigator on the program.

A list of reportable items is given below. The items are innovations or improvements in the technology. No inventions were made during the performance of the work under the contract and no invention disclosures have been prepared. Philco-Ford does not consider these items to be susceptible to protection under United States patent laws and thus does not consider the provisions of parts (1) and (2) under paragraph (h) of Section III of the New Technology clause to be applicable.

No subcontracts were let under this contract.

1. Model of Charge Distribution (pages 5, 6)

Information was assembled from the literature and from experiments performed during the program and was used to prepare an improved (more comprehensive) model of the distribution of electric charge in multilevel metalized metal-insulator-semiconductor structures. This model provides a

better understanding of the effects of a second layer of insulator material on the performance and reliability of both bipolar and MOS microcircuitry.

2. Structure for Studying Contaminant Migration Beneath Metal Layers (pages 43, 67, 68)

A special MIS capacitor designed to have a large ratio of perimeter to area has been shown to be effective for studying the migration of charge from regions adjacent to metalized layers to regions beneath metalized layers. This is a simple structure, not requiring diffusion for its construction, which permits evaluation of long term reliability problems caused by migration of contaminants from the regions adjacent to regions beneath metal layers.

3. Microstructures for Hall Measurement (pages 43, 45, 60-62, 74-75)

The feasibility has been demonstrated of measuring Hall voltages and carrier mobility in inversion layers of MIS devices in structures nearly two orders of magnitude smaller than previously reported. The area capable of being measured is of the order of one mil^2. The value of this capability is that Hall measurements can be conducted on structures similar in size to the elements in microcircuits.

4. Structure for Studying Surface Ion Behavior (pages 48, 49 60, 63-65, 72-74)

A useful structure for studying the effects of surface ion migration on an insulator layer over silicon was demonstrated to provide a sensitive and practical means for studying mechanisms which influence the reliability of multilevel microcircuit structures.

5. Combination of Basic Test Structures in One Chip (pages 41-49)

A mask set has been designed that provides the capability to build a combination of seven basic test structures in one 70- by 70-mil chip. This combination of test structures would be suitable for use on standard production microcircuit wafers for purposes of process control, for yield analysis, and for more sensitive life testing.