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INVERTER-CONVERTER PARALLEL OPERATION

by G. W. Ernsberger, H. R. Howell, and J. L. Klingenberger

Prepared by
WESTINGHOUSE ELECTRIC CORPORATION
Lima, Ohio
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ABSTRACT

Mathematical analysis of circuit operation for harmonic-neutralized, static inverters operating in parallel have been developed and experimentally verified. Inverters can be operated in parallel provided that: (a) all inverters operate at exactly the same frequency; (b) the internal voltages of all inverters are in phase at all times; (c) all nominal regulated output voltages are the same; and (d) circuit provisions in each inverter insure load division. Static converters can be operated in parallel provided that: (a) all converters have the same nominal regulated output voltage, and (b) circuit provisions are provided in each voltage regulator circuit to cause the converters to share load current.

PREFACE

The work described herein was done at the Aerospace Electrical Division, Westinghouse Electric Corporation, under NASA Contract NAS3-2792. Mr. Francis Gourash, Space Power Systems Division, NASA-Lewis Research Center, was the Project Manager for NASA. The entire program, "Parallel Operation of Static Inverters and Converters and Evaluation of Magnetic Materials," is described in five reports:

"Inverter-Converter Parallel Operation" defines and experimentally verifies the circuit conditions that must exist for operating static inverters and static converters in parallel (NASA CR-1224).

"Inverter-Converter Automatic Paralleling and Protection" defines and experimentally verifies the electrical control and protection circuits necessary for isolating faulted inverters and converters from a parallel system while maintaining continuity of high-quality electric power to load equipment (NASA CR-1225).

"Evaluation of Magnetic Materials for Static Inverters and Converters" defines the magnetic characteristics of improved materials for magnetic components as applied in advanced static inverters or static converters (NASA CR-1226).

"Load Programmers, Static Switches, and Annunciator for Inverters and Converters" assesses the characteristics of static electrical switches for both ac and dc systems, defines the characteristics of a load programmer for maintaining power to the critical system loads, and provides an annunciator function for displaying inverter and/or converter operating conditions (NASA CR-72454).

"Parallel Operation of Static Inverters and Converters and Evaluation of Magnetic Materials" is the summary report (NASA CR-72455).

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SUMMARY

Mathematical analysis of circuit operation for harmonic-neutralized, static inverters operating in parallel have been developed and experimentally verified. A parallel system using two 750-VA, 3-phase, 400-Hz harmonic-neutralized inverters was tested to verify analytical techniques. Tests were conducted to assess voltage transients, voltage regulation, frequency locking, phase locking, real and reactive load division with balanced and unbalanced three-phase loads, real and reactive load division with unequal inverter input voltages, and real and reactive load division during induction motor starting. These test data confirmed that static inverters can be operated in parallel provided that: (a) all inverters operate at exactly the same frequency; (b) the internal voltages of all inverters are in phase with each other at all times; (c) all nominal regulated output voltages are the same; and (d) circuit provisions are incorporated in each inverter to insure load division.

Laboratory test evaluations of static converter paralleling circuits concluded that static converters can be operated in parallel provided that: (a) all converters have the same nominal regulated output voltage and (b) circuit provisions are provided in each voltage regulator circuit to cause the converters to share load current.

Two companion reports (NASA CR-1225 and CR-72454) present related technologies for applying static inverters or converters in a paralleled electrical system for future space vehicles.

NASA CR-1225 discusses circuit techniques needed for controlling and protecting these inverters and converters in a paralleled system.

NASA CR-72454 discusses static switches for circuit interruption, load programmers for maximizing continuity of electric power to the most critical loads at the expense of power removal from less critical loads and a system annunciator for visually displaying the operating state of the electrical system.

INTRODUCTION

Static inverters and converters are often used in satellites and similar long-life, low-maintenance missions. Reliable operation throughout the life of a mission is critical. Each time a different mission is defined, a different inverter with a different rating is required. The size and complexity of an inverter depend on the value of input voltage and on the limitations of the semiconductors used. Each newly developed inverter must be tested and modified until the desired degrees of performance and reliability are obtained. One method for obtaining high degrees of reliability is through redundancy (i.e., by having several system-rated inverters on standby). Such an approach results in a relatively high system weight.

A better solution to the weight-reliability problem is to use several smaller, highly developed inverters operating electrically in parallel to obtain the system rating and the desired system reliability. With such an approach, a new system is built by adding or deleting inverters. No new circuits are necessary.

The requirements for such a parallel system are: (1) each unit must be capable of operating independently, (2) each unit must be capable of operating in parallel with any number of similar units, and (3) provisions must be included for automatic voltage regulation and for load sharing among paralleled units. Prior to the inception of this NASA program, very little technology existed for applying static inverters or converters in parallel electrical systems for space vehicles.

Parallel operation of electrical systems has been used on commercial and military aircraft for many years. These systems use alternators as the source of electric power. The design philosophies and techniques from these aircraft systems represent an excellent starting point for developing the required technology for static inverters and converters.

This program was undertaken to define the criteria that must be achieved for either multiple inverters or multiple converters operating in parallel. The requirements for satisfactory paralleling of inverter and converter circuits were established mathematically. The optimum method for meeting these paralleling requirements was selected. Circuits were designed for automatic locking of independent frequency references, automatic voltage regulation, and load sharing.

Two static inverter models of an existing design were built, incorporating these circuits. The static inverter models were easily changed to converter operation. Using these models, the feasibility of paralleling both inverters and converters was

demonstrated. Data showing this operation are contained in the main body of this report. In addition to normal voltage regulation, tests included division of real and reactive loads at various power factors, overloads and fault conditions.

A qualitative description of the factors contributing to increased system reliability resulting from paralleling inverters is presented in appendix E. This information permits the system designer to evaluate the possibilities for increased reliability and reduced weight for a given system configuration.

The developed technology reported herein represents an excellent framework for applying any configuration of a static inverter or converter to a vehicle system. This technology will either be directly applicable to the specific application or will provide a good basis for whatever variations are necessary to achieve the desired parallel system operation.

SYMBOLS

$\dot{I}_1$	is the current supplied by one inverter.
$\dot{I}_0$	is the inverter current if all paralleled inverters were supplying an equal amount of the load current.
$R(\dot{I}_1 - \dot{I}_0)$	is the component of unbalanced current that is in phase with the bus voltage.
$Q(\dot{I}_1 - \dot{I}_0)$	is the component of unbalanced current that is in quadrature with the bus voltage.
E_0	is the magnitude (rms) of internal voltage if it was adjusted so that differential current was zero.
θ_0	is the angle (with terminal voltage as a reference) of the internal voltage if it was adjusted so that differential current was zero.
$\dot{Z}_1 = Z_1 \angle \theta_1$	is the internal impedance of the voltage source.
ΔE and $\Delta\theta$	are incremental quantities.
θ_2	is the angle (with terminal voltage as a reference) of a developed voltage to achieve circuit operation.
$\dot{Z}_L = Z_L \angle \Psi$	is the load impedance.

V_s	is the voltage applied to the voltage regulator sensing circuit.
V_t	is the inverter terminal voltage.
E	is the magnitude (rms) of internal voltage of the inverter.
I_{DQ}	is the reactive load-division current.
N	is the number of inverters in parallel.
e, and i	are instantaneous values of voltages and currents.
R	is resistance.
L	is inductance.

CONSIDERATIONS FOR PARALLELING STATIC INVERTERS

The method for operating static inverters in parallel is described later in detail but can be summarized as follows: (1) All inverter control circuits must be connected so that the phase A, no-load output voltage of each inverter is in phase with the phase A, no-load output voltages of all other inverters before paralleling. The phase sequence of all inverters must be the same before paralleling. (2) After paralleling two or more inverters, control of the magnitude of the interval voltage of each inverter must be achieved so that load current is divided equally among the inverters. ("Internal" voltage of an inverter is defined as the imaginary voltage behind the internal impedance of the inverter. The internal voltage equals the output terminal voltage only at zero load. The output filter of the inverter must be considered as part of the load.) This control is achieved by making the internal voltage regulator sensitive to both terminal voltage and certain components of the differential load current. (Differential load current is the difference between an actual inverter output phase current and the average of all inverter output currents of the same phase.) The component of the differential current to which the internal voltage regulator must be made most sensitive can be calculated after the internal impedance of the inverter has been determined. A procedure for these calculations is given in appendix C.

Mathematical Analysis

Load-Sharing Control Method. - Successful operation of a system consisting of two or more inverters supplying a common

bus requires that the total system load be divided nearly equally among the parallel inverters. In the event of unequal load sharing, the problem is to sense or detect the cause or causes and to initiate the proper corrective actions. This is accomplished in the case of paralleled alternators by sensing real and reactive power. Any change in the average real power of an alternator must be accomplished by changing the governor or control on its prime mover. The reactive load is then adjusted by changes in excitation. There seems to be no such inherent separation of functions in the present type static inverter.

An analysis based on Thevenin's equivalent circuit approach (equations (1) and (2) derived and numbered (A23) and (A24) in appendix A and repeated below) indicates that, for inverters, an unbalance in reactive load does not necessarily result from a difference in voltage magnitudes. Likewise, an unbalance in real load does not necessarily result from a difference in phase.

$$R(\dot{I}_1 - \dot{I}_0) \cong \frac{\Delta E}{Z_1} \cos(\theta_0 - \theta_1) - \frac{E_0 \Delta\theta}{Z_1} \sin(\theta_0 - \theta_1) \quad (1) \text{ or } (A23)$$

$$Q(\dot{I}_1 - \dot{I}_0) \cong \frac{\Delta E}{Z_1} \sin(\theta_0 - \theta_1) + \frac{E_0 \Delta\theta}{Z_1} \cos(\theta_0 - \theta_1) \quad (2) \text{ or } (A24)$$

The controlling factor is the angle $(\theta_0 - \theta_1)$. Since the angle θ_0 is a function of both the internal impedance and load impedance, these two impedances are the controlling factors. (See appendix A, equation (A14).) If $(\theta_0 - \theta_1) \cong 90°$, equations (1) and (2) become

$$R(\dot{I}_1 - \dot{I}_0) = \frac{E_0}{Z_1} \Delta\theta \quad (1a)$$

$$Q(\dot{I}_1 - \dot{I}_o) \cong \frac{-\Delta E_0}{Z_1} \quad (2a)$$

and a real component would indicate phase difference and a reactive component would indicate a magnitude difference.

If $(\theta_0 - \theta_1) = 0°$, equations (1) and (2) become

$$R(\dot{I}_1 - \dot{I}_0) \cong \frac{\Delta E_0}{Z_1} \quad (1b)$$

$$Q(\dot{I}_1 - \dot{I}_0) \cong \frac{E_0}{Z_1} \Delta\theta \qquad (2b)$$

and the exact opposite is indicated.

If $(\theta_0 - \theta_1) = -45°$, equations (1) and (2) become

$$R(\dot{I}_1 - \dot{I}_0) \cong 0.707 \frac{(\Delta E + E_0 \Delta\theta)}{Z_1} \qquad (1c)$$

$$Q(\dot{I}_1 - \dot{I}_0) \cong 0.707 \frac{(E_0 \Delta\theta - \Delta E)}{Z_1} \qquad (2c)$$

and therefore, the real or the reactive component could be a result of a difference in magnitude and/or phase.

If $\theta_1 \cong 90°$, that is the internal impedance of the inverter is practically a pure inductance, and if θ_0 is small, equations (1a) and (2a) indicate that the internal phase should be controlled by sensing differential real current and the magnitude of the internal voltage should be controlled by sensing differential reactive current.

In practice, it might not be practical to make the internal impedance purely inductive or purely resistive. (A pure resistance would make equations (1b) and (2b) hold.) However, in appendix A it is shown that the in-phase component of $(I_1 - I_0)$ with a phasor θ_2 degrees ahead of the corresponding terminal voltage is given by:

$$R_{\theta_2}(\dot{I}_1 - \dot{I}_0) \cong \frac{\Delta E}{Z_1} \cos(\theta_0 - \theta_1 - \theta_2) - \frac{E_0 \Delta\theta}{Z_1} \sin(\theta_0 - \theta_1 - \theta_2) \qquad (1d) \text{ or } (A23d)$$

and the in-quadrature component is given by:

$$Q_{\theta_2}(\dot{I}_1 - \dot{I}_0) \cong \frac{\Delta E}{Z_1} \sin(\theta_0 - \theta_1 - \theta_2)$$

(2d) or (A24d)

$$+ \frac{E_0 \Delta\theta}{Z_1} \cos(\theta_0 - \theta_1 - \theta_2)$$

If equations similar to equations (1a) and (2a) are to hold for this case:

$$\theta_0 - (\theta_1 + \theta_2) \cong -90° \text{ or } (\theta_1 + \theta_2) \cong 90 + \theta_0 \qquad (3)$$

Therefore, if the internal impedance is not purely inductive, it can be compensated for by using a reference phasor that leads the terminal voltage by θ_2 degrees such that:

$$\theta_2 \cong 90° + \theta_0 - \theta_1 \qquad (4)$$

As discussed in appendix D and illustrated by figure 31, θ_2 can easily be made a multiple of 30 degrees with a set of three-phase voltages. This leading phasor can be one of the line-to-line voltages if θ_2 is 30 degrees or another line-to-neutral voltage if θ_2 is 60 degrees. If θ_2 must be something other than a multiple of 30 degrees, one of the voltages can be phase shifted.

If it is assumed that differential current sensing and comparing are provided in such a manner as to make equations (1d) and (2d) hold, there are two basic methods of parallel control.

Method 1: Lock the oscillators to assure frequency lock. Since it is possible to have the frequencies of the internal voltages the same but be out of phase, some method of assuring that the internal voltages are in phase must be provided. With "front-ends" locked, means for quadrature current control based on equations (1d) and (2d) with $\Delta\theta$ set equal to zero could be provided.

Method 2: This method with no cross ties between "front-ends" of the inverters is very similar to that now used in alternator systems. Differential current sensing and comparing are achieved in the same manner as in Method 1. The quadrature component would again control the magnitude. However, the in-phase

component would directly control the frequency. Changes in phase would be accomplished by changing the frequency for a small interval of time.

Method 1 was used in the experimental work because it requires less complex control circuits, it was more readily adaptable to existing inverter circuits, and it would not interfere with precise frequency requirements. If the reference phasor is picked such that

$$\theta_0 - \theta_1 - \theta_2 \cong -90° \tag{5}$$

and if one of the inverters has an internal voltage greater than the average, that inverter will take more lagging reactive current (in reference to a voltage θ_2 degrees ahead of the phase voltage in which the differential current loop is placed) than the average. Its reactive load division circuit would need to reduce the "excitation" voltage of that inverter. θ_0 is related to the internal impedance by the following equation

$$\text{Tan } \theta_0 = \frac{\sin (\theta_1 - \Psi)}{\frac{2Z_{Lp}}{Z_1} + \cos (\theta_1 - \Psi)} \tag{6}$$
or (A18)

for a two-inverter system. Therefore, if Z_1 is known, a proper value of θ_2 may be determined.

Sensing circuit gain calculation. - The open-loop relation for internal voltage is derived in appendix B and given below.

$$\Delta E = (V_{pL} - V_{1L}) \frac{\partial E}{\partial V_s} + \frac{\left|\dot{Z}_1 + \dot{Z}_L\right|}{Z_L} (V_{1L} - V_0) + \frac{\partial E}{\partial I_{DQ}} (\Delta I_Q) \tag{7}$$
or (B9)

The voltage regulator gain, $\frac{\partial E}{\partial V_s}$, can be calculated from the single-unit circuitry, or if one has knowledge of the single-unit, closed-loop regulation, it can be calculated by use of the following formula:

$$\frac{\partial E}{\partial V_s} = \frac{V_{N.L.} - \left|\frac{\dot{Z}_1 + \dot{Z}_L}{Z_L}\right| V_{F.L.}}{V_{N.L.} - V_{F.L.}} \qquad (8)$$

If Z_1 and V_{1L} are known (assume $V_{pL} = V_o$), equations (7) and (2d) can be solved simultaneously for parallel control circuit gain, $\frac{\partial E}{\partial I_{DQ}}$, for a given load and allowable differential current, ΔI_Q.

Therefore:

$$\frac{\partial E}{\partial I_{DQ}} = \frac{Z_1}{\sin(\theta_0 - \theta_1 - \theta_2)} - \left[\frac{(V_{pL} - V_{1L})\left(\frac{\partial E}{\partial V_s} - \left|\frac{Z_1 + Z_L}{Z_L}\right|\right)}{\Delta I_Q}\right] \qquad (9)$$

Internal Impedance Calculation and its use. - It will be observed that in order to make use of the relationships stated on the preceding page, the internal impedance, $\dot{Z}_1$, must be known. If balanced loads are assumed, the equivalent circuit for calculating the per-phase internal impedance is shown in figure 1.

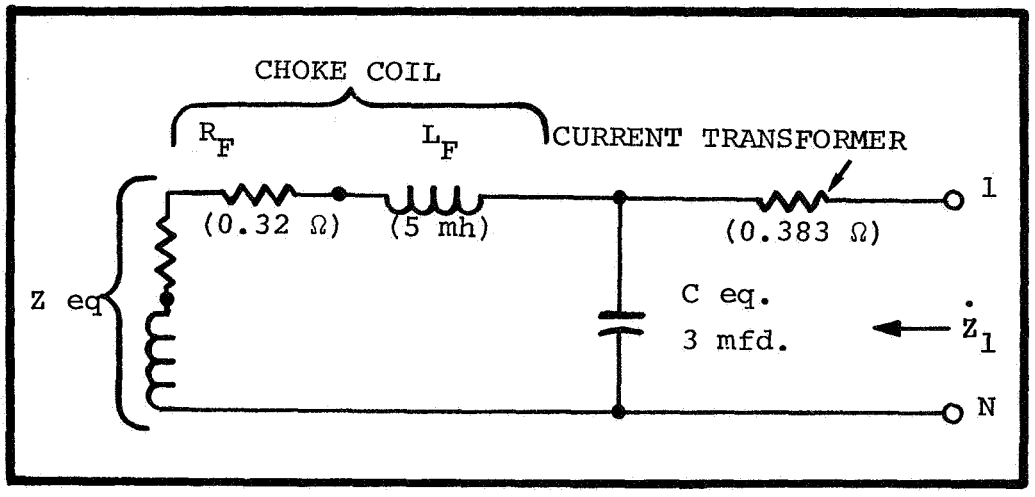


Figure 1. The Equivalent Circuit for Internal Impedance of a Static Inverter Under Balanced Load Conditions

The impedance looking back into the series-connected secondaries in phase one is Z_{eq}. In appendix C, an equation is developed for determining Z_{eq}. (Equation (C40)). With Z_{eq} known, the internal impedance of the inverter can thus be calculated by substituting values in the circuit of figure 1 and making a few series-parallel transformations.

In appendix D the internal impedance of the static inverter models which will be used in this program is calculated and is $Z_1 = 0.27$ pu $\underline{/77.8°}$. The required inverter voltage regulator gain is calculated using this internal impedance and voltage regulation limit of 115 ± 0.7 volts and is $\frac{\partial E}{\partial V_s} = -38.0$.

By assuming an initial full-load voltage setting accuracy of ± 0.2 volts, and a load division accuracy of 10%, the required gain of the reactive load-division-circuit is calculated in appendix D and is $\frac{\partial E}{\partial I_{DQ}} = 0.412$ where E and I_{DQ} are in per unit values.

Circuit Development

Frequency & Phase Locking Circuits. - In the paralleling method chosen for this study, the frequency and phase must be the same on all sources prior to connecting them in parallel. Therefore, all inverters to be paralleled must operate from the same frequency reference and be locked in phase with each other.

For increased reliability, each inverter must be capable of operating independently or in parallel with similar inverters. To operate independently means that each inverter must have its own frequency reference. The requirement that they operate in parallel with similar inverters means that all inverters must obtain their frequency reference signal from a single reference. Therefore, a means was derived to remove all but one frequency reference signal and connect that frequency reference signal to all inverters whenever parallel operation is desired.

The only practical way devised to achieve the circuit functions is shown in figures 2 and 3. When inverter #1 is operating independently, switches S1 through S5 are open (figure 2). Transistor Q24 is normally on (i.e., driven into saturation). Its base current is delivered by resistor R62. Then the tuning fork oscillator #1 (TF01) is on and provides a 3200-pulse-per-second signal to the Unijunction Transistor Relaxation Oscillator (UTRO) on its own breadboard. The UTRO provides a 3200-pps

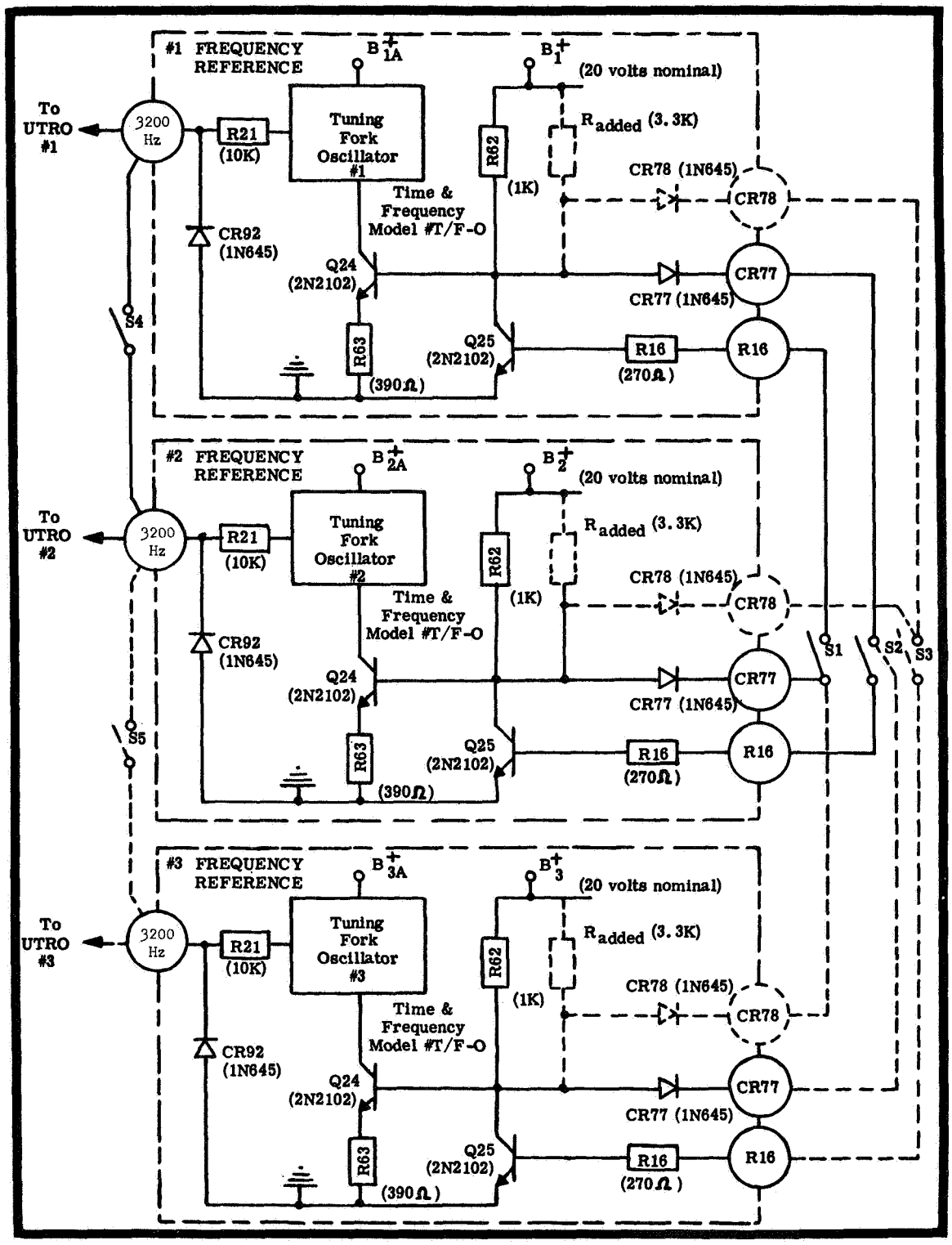


Figure 2. Frequency Locking Circuits

(Solid interconnections show two units paralleled; solid and dotted interconnections show three units paralleled.)

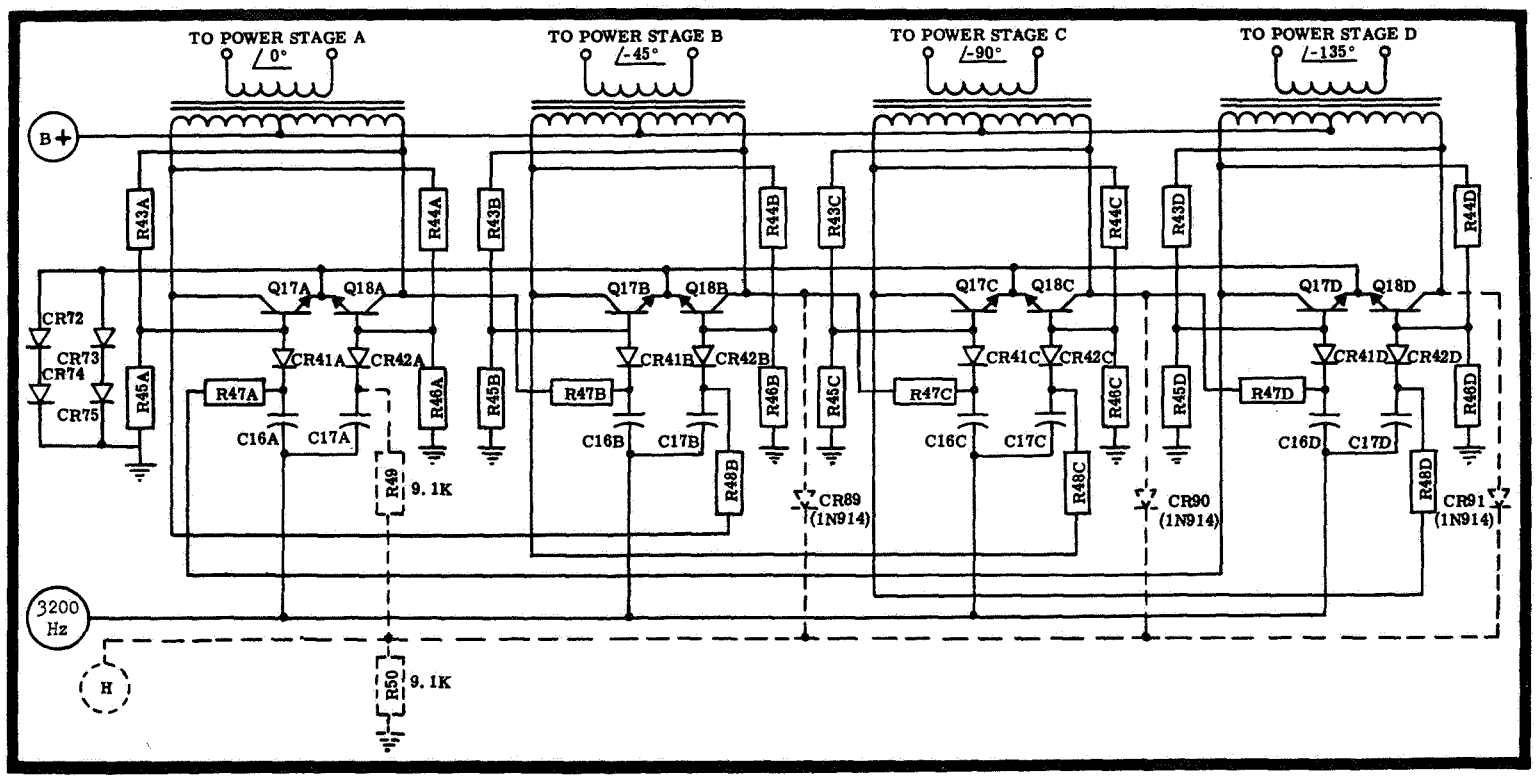


Figure 3. Schematic Diagram of a Typical Countdown Circuit with Phase Locking Provisions

(The dotted components ensure proper phase locking)

signal for operating the countdown circuit of figure 3. The operation of the countdown is described in reference 1. Inverter #2 will operate independently in an identical manner.

The method selected to accomplish the removal of all but one frequency reference signal and to connect that frequency signal to all inverters to be paralleled was based on the assumption that any of the frequency references on any of the inverters to be paralleled would operate within the frequency accuracy required. The circuit shown in figure 2 was designed to arbitrarily select one of the two references in the following manner. With switches S1, S2 and S4 closed, dc voltage is applied to both inverters. The UTRO's of both inverters will free run at different frequencies until a frequency reference is selected. Transistor Q24 on one of the inverters and transistor Q25 on the other inverter will turn on because of unbalance in the bistable circuit involved. Assume that Q24 on inverter #1 and Q25 on inverter #2 turn on first. Then R62 of inverter #1 will supply base drive for Q24 on inverter #1 and Q25 on inverter #2. Consequently, Q25 on inverter #2 will divert base drive away from Q24 on inverter #2 and Q25 on inverter #1 to ground. TFO #1 will operate but TFO #2 will not operate. The operating TFO will supply its frequency signal to both UTRO's so both inverters will operate at the same frequency. If Q24 on inverter #2 and Q25 on inverter #1 turn on first, then replace each #1 by #2 and #2 by #1 in the above description.

Proper phase sequence of the output voltages is ensured by the addition of an inhibit circuit to the countdown circuit. This inhibit circuit consists of R49, R50, CR89, CR90, and CR91 shown in figure 3. The paths provided by those components ensure that Q18B, Q18C, and Q18D are on before Q18A can be turned off by a signal from the UTRO.

The signal from the UTRO varies from about 10 volts positive to 0 volts with respect to ground at a 3200-pps rate. The countdown flip-flops change state only under certain conditions. One of these conditions is that the signal from the UTRO must be zero. The other condition is that the capacitor (C16 or C17) in series with the base of the transistor to be shut off must be charged positive with respect to ground so that its base current can be diverted to ground. If the countdown flip-flops start in the correct sequence, each flip-flop can change states every fourth zero from the UTRO, i.e., one flip-flop changes state during one UTRO pulse. If the countdown circuit does not start in the correct sequence, then either Q18B, Q18C, or Q18D will be off when Q18A is set up to be shut off. Therefore, CR42A will be reverse-biased by the collector voltage of either Q18B, Q18C, or Q18D so that Q18A cannot be shut off. When Q18A is on, Q17A is off. The collector voltage of Q17A charges C17B through R48B, C16B,

R47B and Q18A negative with respect to ground so that once Q18B is turned on it cannot be turned off by a pulse from the UTRO. Q18C and Q18D have similar conditions set up in C - D sequence. When Q18B, Q18C, and Q18D are on, Q18A can be shut off by the next UTRO signal. The correct phase sequence for each inverter is thus established.

The next requirement is that respective phase voltages on all inverters must correspond before paralleling the inverters. By connecting the (H) terminals (figure 3) of all inverters to be paralleled together, all inverters will operate in phase with each other. Of course, all inverters must be operating at the same frequency prior to making that connection since the phase of all inverters cannot be the same if they are operating at different frequencies.

Three or more units are paralleled in a similar manner. The interconnections to parallel three units are shown dotted on figure 2. It should be noted that for every inverter added to the bus, a diode (CR78) and a resistor (3.3K), shown dotted in figure 2, must be added to all inverters. This diode and resistor supply base current for the added frequency reference. Also, if only two inverters are to be paralleled, then CR77 can be replaced by a short circuit.

This circuit selects one frequency reference immediately after dc voltage is applied to the inverters. The connection of all (H) terminals together must be delayed until that one frequency reference is operating. With the tuning fork oscillators selected for the inverter models, this delay will be from three to five seconds. If an instant-starting-type frequency reference was used (i.e., crystal oscillator, multivibrator, etc.), this delay would be unnecessary.

Load Division Circuit. - The ac load division designed for this purpose (figures 4 and 5) is an adaptation of techniques used in voltage regulators for ac parallel generator systems. The voltage reference in this circuit consists of two 43.4-volt Zener diodes (CR55 and CR56) connected in a bridge which balances with 86.8 volts applied and has a nominal dc current requirement of 15 milliamperes. When load is divided perfectly, there is no circulating current through R64, R65, and C21 from the load division sensing current transformer (T27), and all voltage and current for balancing the voltage reference bridge is supplied by the voltage sensing transformer (T29) through the full-wave rectifiers (CR51, 52, 53, 57, 58, and 59) and the voltage adjusting resistor R15.

Transformer T28 consists of two separate 2:1 step-down transformers which are used for impedance transformation and to provide

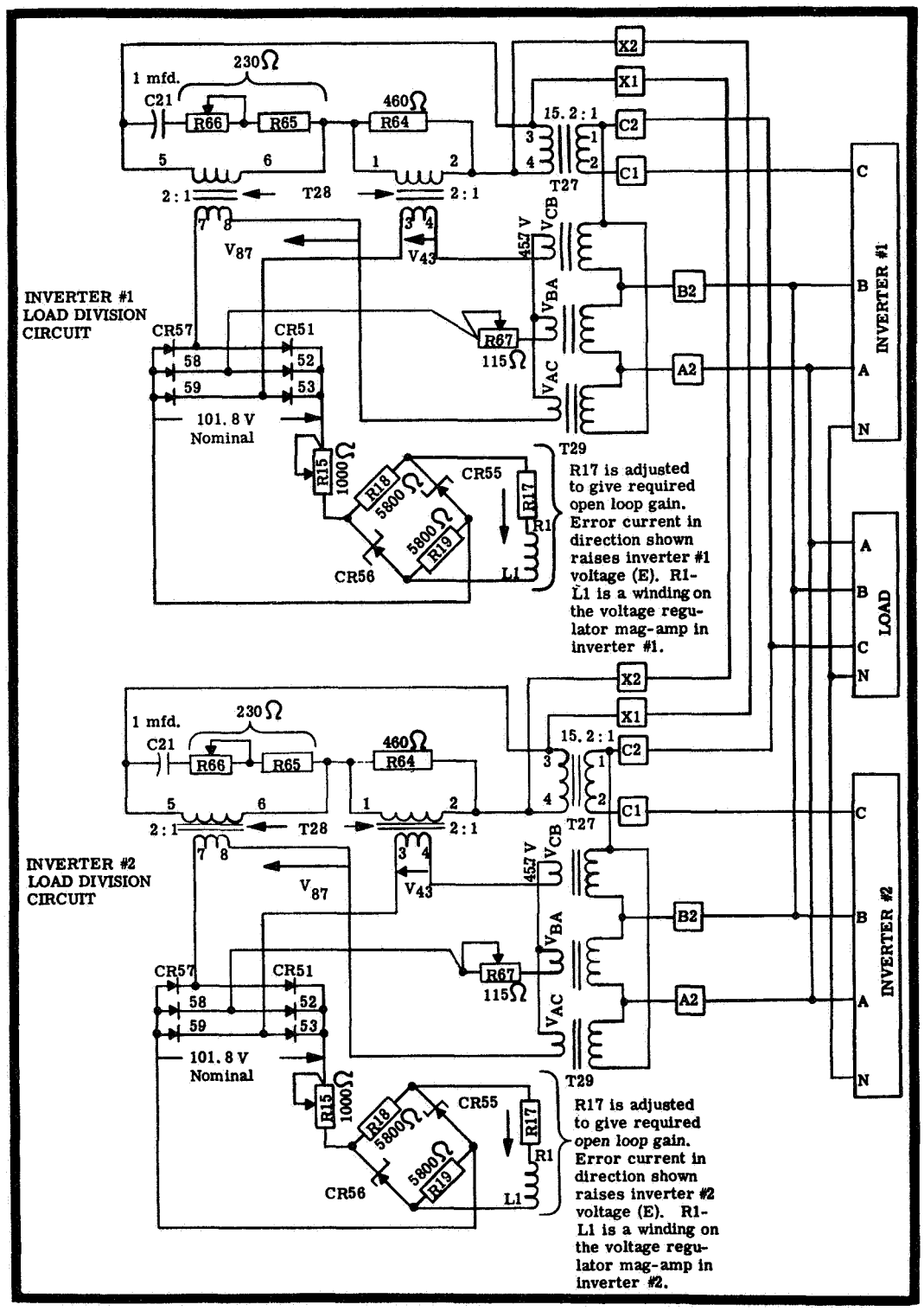


Figure 4. Two Inverter Block Diagrams Connected in Parallel with AC Load Division Circuits Shown

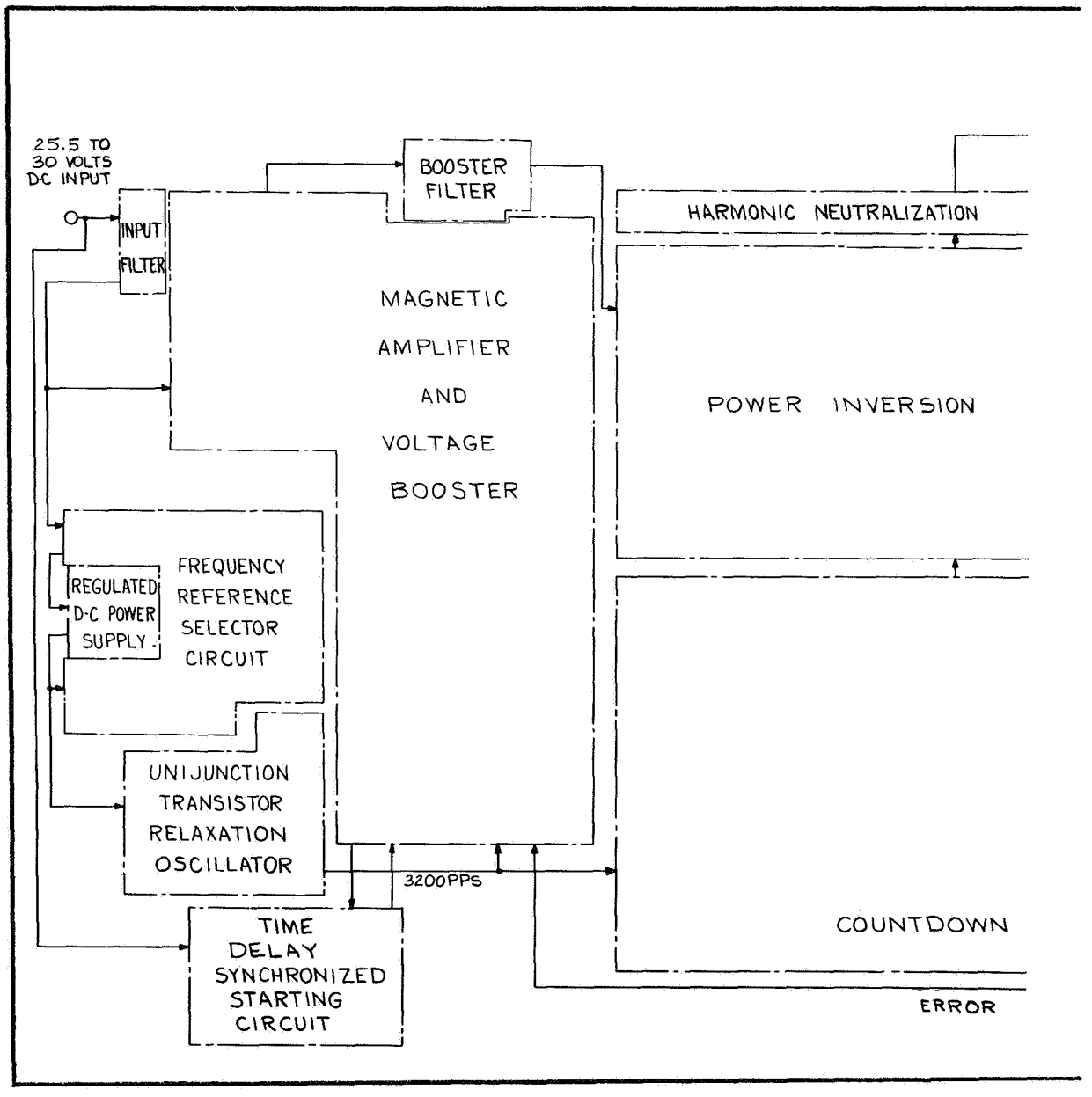
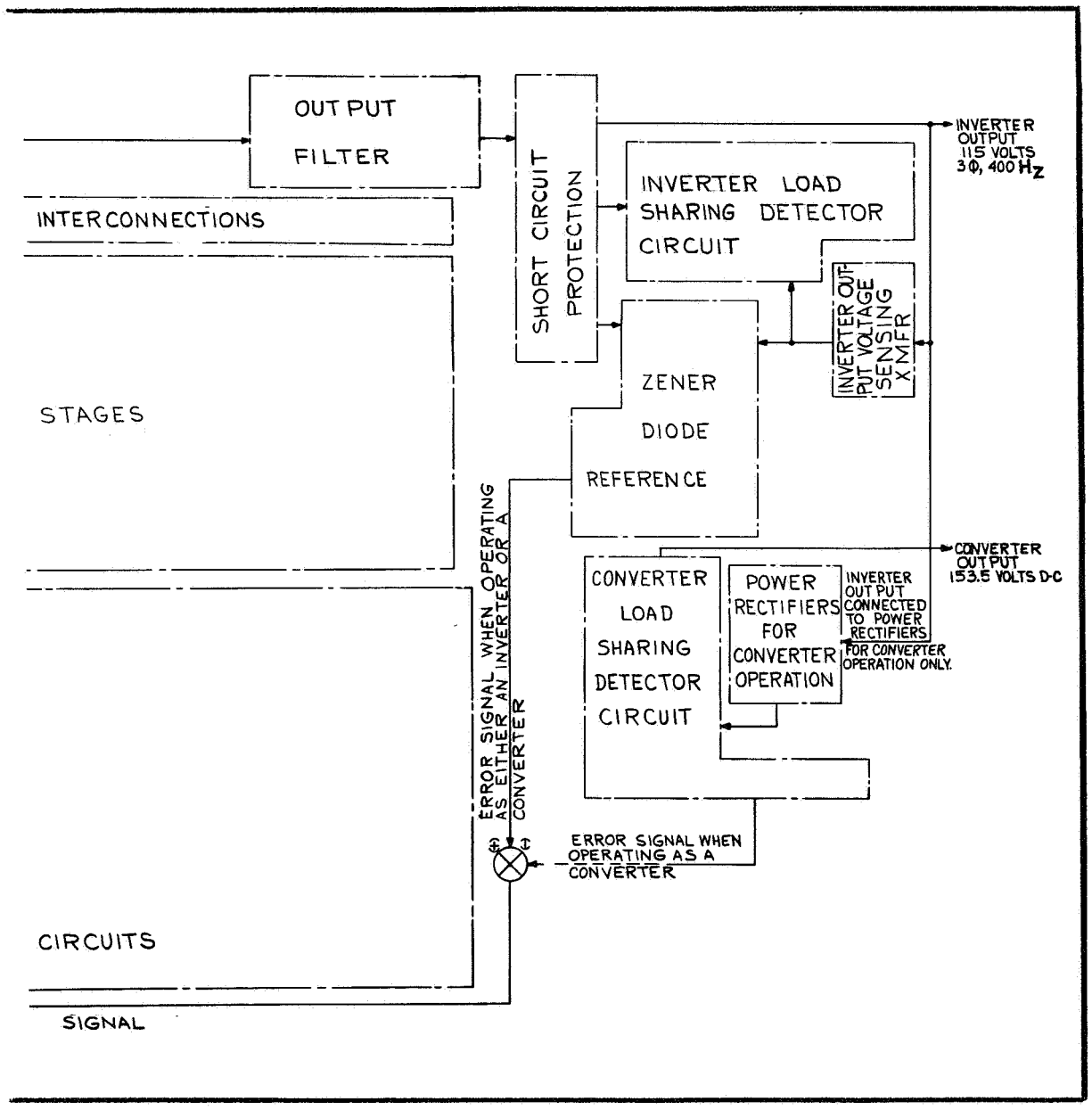


Figure 5. - Block Diagram of Inverter/Converter Models to be Used



to Demonstrate Parallel Operation

isolation. A value of 1 microfarad was chosen for C21. Resistors R65 and R66 are adjusted so that the voltage across the series combination lags the 400-Hz current through it by 60 electrical degrees.

$$R65 + R66 = \frac{X_{C21}}{\tan 60°} = \frac{1}{2\pi 400 \times 1 \times 10^{-6} \times \sqrt{3}} = 230 \text{ ohms} \tag{10}$$

The voltage across R64 will be in phase with the current through it. To keep the voltage across R64 equal to the voltage across the R65, R66, and C21 combination, the impedance of R64 must be the same as the impedance of the RC combination.

$$R64 = \sqrt{(R65 + R66)^2 + (X_{C21})^2} = \sqrt{(230)^2 + (398)^2} = 460 \text{ ohms} \tag{11}$$

The impedance presented by the secondaries of transformer T28, under conditions of perfect load division, is approximately equal to the turns ratio squared times the primary impedance

$$(1/2)^2 \times 460 = 115 \text{ ohms} \tag{12}$$

To present balanced voltages to the three-phase bridge rectifier (CR51, 52, 53, 57, 58, and 59) resistor R67 was set at approximately 115 ohms.

Resistor R15 was assumed to be nominally set at 1000 ohms. Then, the required secondary voltage of T29 was determined as follows: the dc voltage required out of the full-wave bridge rectifier equals the nominal voltage reference level (86.8 volts) plus the nominal voltage drop across R15 (1K x 15 ma = 15 volts) making a total of 101.8 volts. The required line-to-neutral voltage and current into the full-wave bridge rectifier were determined by the usual bridge rectifier characteristics.

$$I_{ac} = 15 \text{ ma} \times 0.816 = 12.2 \text{ ma},$$

$$E_{LN} = \frac{0.74 \times 101.8 \text{ volts} + 2 \times 0.7}{\sqrt{3}} = 44.3 \text{ volts} \tag{13}$$

Transformer T29 must supply this voltage plus the voltage drops from the secondaries of T28 and R67 which gives (44.3 volts + 0.0122 amps x 115 ohms) a total secondary voltage of 45.7 volts. Therefore, T29 was designed to provide 45.7 volts output per phase with 200 volts input per phase.

To determine the required turns ratio of the load division current transformer (T27), it was assumed that X1 and X2 were disconnected and that the inverter was supplying an output current of 1 pu $\angle -60°$ = 2.18 amps $\angle -60°$. Under these conditions, the inverter output voltage should be caused to drop to 67.5 volts line-to-neutral by the voltages introduced in the sensing circuit transformer T28. By knowing these secondary voltages, the primary voltages (T28) and the required secondary current of T27 were determined. Figure 6 is a phasor diagram of this circuit under these conditions with phase C voltage taken as the reference phasor. The secondary voltages of T29 (V_{CB}, V_{BA}, and V_{AC}) will have a magnitude of 26.8 volts ($45.7 \times \frac{67.5}{115}$). Temporarily neglecting the voltage drop across R67, the voltages required from T28 (V_{43} and V_{87}) must have a magnitude of 30.4 volts:

$$|V_{87}| = |V_{43}| = 44.3 \times \sqrt{3} \text{ (line-to-line voltage required into bridge rectifier)}$$

$$- 26.8 \times \sqrt{3} \text{ (line-to-line voltage from T29)} = 30.4 \text{ volts.} \qquad (14)$$

The voltage drop across R67 (0.0124 amps x 115 ohms = 1.4 volts) subtracts from V_{BA} and was compensated for by increasing both V_{43} and V_{87} by the vectorial equivalent amount of 0.8 volts $\left(\frac{1.4 \text{ volts}}{2 \cos 30°} = 0.808 \text{ volts}\right)$. Therefore, the desired secondary voltages of T28 under this unbalanced condition are 30.4 + 0.8 = 31.2 volts.

The current through R64 to obtain the required primary voltage is

$$I_{R64} = \frac{V_{43} \times 2}{R64} = \frac{31.2 \times 2}{460} = 0.136 \text{ amps} \qquad (15)$$

The current through the transformer primary (T28) is equal to the secondary current divided by the turns ratio $\frac{(0.01224 \text{ amps})}{2}$ = 0.00612 amps plus a small transformer exciting current. These currents are small compared to I_{R64} and were provided for by

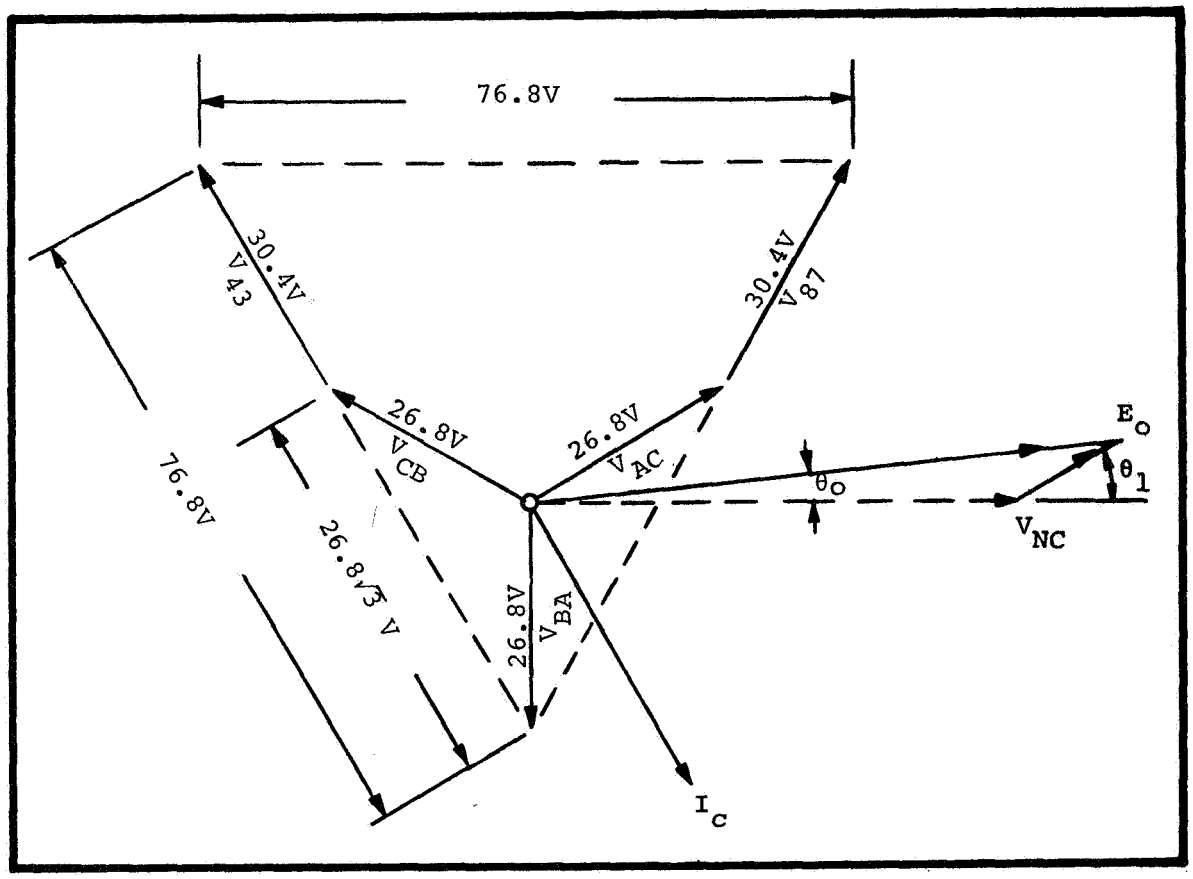


Figure 6. - Phasor Diagram of AC Load Division Circuit with a Differential Load Current of 1 pu $\underline{/-60°}$

letting $I_{CT} = 1.05 \times I_{R64} = 1.05 \times 0.136 = 0.143$ amps with one per unit primary current.

The required turns ratio of the load division transformer (T27) were then determined:

$$\text{Turns ratio (T27)} = \frac{1 \text{ pu}}{0.143 \text{ amps}} = \frac{2.18}{0.143} = 15.2. \qquad (16)$$

Current transformer T27 was wound with this turns ratio.

The above example calculations were for the purpose of designing the load division circuit with sufficient gain to assure load division within 10 percent. The phasor diagram of figure 6 is

for a load unbalance 10 times this amount. Other phasor diagrams could have been drawn to illustrate operation under more typical unbalance load conditions. In actual parallel operation, I_C (figure 6) can be considered the differential current and may lag V_{NC} by any angle from 50° to 70°. This load division circuit is most sensitive to differential currents which lag V_{NC} by 60°.

During parallel operation of the two model inverters, X1 from one inverter must be connected to X2 of the other inverter and vice versa. (Any number of inverters could be connected in this loop.) In this manner, the current which circulates in these interconnecting wires is proportional to the average current supplied by both (all) inverters, and the CT current which circulates through R64, 65, 66, and C21 is proportional to the differential current. The differential current is the difference between the actual current delivered by one inverter and the average current delivered by all inverters. The operation of this load division circuit always tends to reduce this differential current toward zero.

The component values determined above for figure 4 were tested in the laboratory.

The results of the laboratory tests indicated that the load division circuit performance was much better than expected. Closer examination of the design procedure showed that the value calculated for the open-loop gain was used as the value for the closed-loop gain. This resulted in a much higher open-loop gain than that derived in appendix D, hence, better performance.

The new value of open-loop gain was used to determine the expected performance limits of the test circuit. The calculated performance was very close to the exhibited performance of the test circuit, indicating that the design procedure is accurate. The recalculation of the performance limit is shown below.

As shown in appendix D, the open-loop gain of the reactive load division circuit should have been

$$\frac{\partial E}{\partial I_{DQ}} = 0.412 \tag{17}$$

However, as noted above, this value was assumed to be the value of the closed-loop gain. So, let the closed-loop gain be denoted by the symbol

$$\frac{\partial V_t}{\partial I_{DQ}} \tag{18}$$

which is equal to 0.412.

If we assume $\Delta R_s \approx 0$, then equation (B1) of appendix B can be written as

$$\Delta E = \frac{\partial E}{\partial V_s} (V_{pL} - V_0) + \frac{\partial E}{\partial I_{DQ}} \Delta IQ = \frac{1}{K} V_{pL} - V_0 \tag{19}$$

Since $\frac{1}{K}$ is very close to unity for a 1.0 pu, 0.5 lagging PF load, the above expression can be rearranged:

$$\frac{V_{pL} - V_0}{\Delta I_Q} = \frac{\frac{\partial E}{\partial I_{DQ}}}{1 - \frac{\partial E}{\partial V_s}} \triangleq \frac{\partial V_t}{\partial I_{DQ}} \tag{20}$$

This is the expression which relates the closed-loop, load-division circuit gain to the open-loop, load-division circuit gain. Then the open-loop gain will have a value of

$$\frac{\partial E}{\partial I_{DQ}} = (1 - \frac{\partial E}{\partial V_s}) \frac{\partial V_t}{\partial I_{DQ}} = 39(0.412) = 16.1 \tag{21}$$

This higher gain value allowed a much wider isolated voltage setting tolerance while maintaining the original 10 percent current division accuracy. This wider tolerance was determined by equation (B9) as follows

$$\Delta E = (V_{pL} - V_{IL}) \frac{\partial E}{\partial V_s} + \left|\frac{\dot{Z}_1 + \dot{Z}_L}{Z_L}\right| (V_{IL} - V_0) + \frac{\partial E}{\partial I_{DQ}} \Delta I_Q \tag{22}$$

The differential current ΔI_Q is related to ΔE by equation (2b)

$$Q(\dot{I}_1 - I_0) \cong - \frac{\Delta E_o}{Z_1} = \Delta I_Q \tag{23}$$

If we assume $V_o = V_{PL}$, then

$$-Z_1 \Delta I_Q - (V_{IL} - V_{PL})\left(\left|\frac{\dot{Z}_1 + \dot{Z}_L}{Z_1}\right| - \frac{\partial E}{\partial V_s}\right) + \frac{\partial E}{\partial I_{DQ}} \Delta I_Q \tag{24}$$

or

$$V_{IL} - V_{PL} = \frac{-\left(\frac{\partial E}{\partial I_{DQ}} + Z_1\right)}{\frac{\dot{Z}_1 + \dot{Z}_L}{Z_L} - \frac{\partial E}{\partial V_s}} \Delta I_{DQ} \tag{25}$$

where $\dot{Z}_1 = 0.27$ pu $\angle 77.8°$ from appendix D. Assume a 1.0 pu, 0.5 lagging PF load; then

$$V_{1L} - V_{PL} = \frac{(16.1 + 0.27)(0.1)}{(1.29 + 38)} = -0.0417 \text{ pu} = -4.8 \text{ volts} \tag{26}$$

Thus, a ten percent current division accuracy can be maintained by this current division circuit if the initial setting on each inverter is within 115 $\pm$ 4.8 volts rms. Or from another viewpoint for the original voltage setting limits of 115 $\pm$ 0.2 volts, the current division will be considerably better than 0.1 pu unbalance as shown by the performance of the test circuit.

Thus,

$$\frac{\partial V_t}{\partial I_{DQ}} = 0.412 \tag{27}$$

for differential load currents which lag the phase voltages by 60 degrees. This means that if an inverter was supplying a current equal to 1 pu $\angle 60°$ more than the average phase current supplied by each inverter, the load division circuit should be capable of causing the inverter output voltage to drop 0.412 pu to 67.5 volts line-to-neutral. Figure 7 illustrates the response of this circuit.

Inverter/Converter Test Model

One of the inverter/converter test models is shown in figure 8. The capital letters designate important component and circuit locations on the test model. Those designated are: (A) terminal boards which permit operation of the test models as either a static

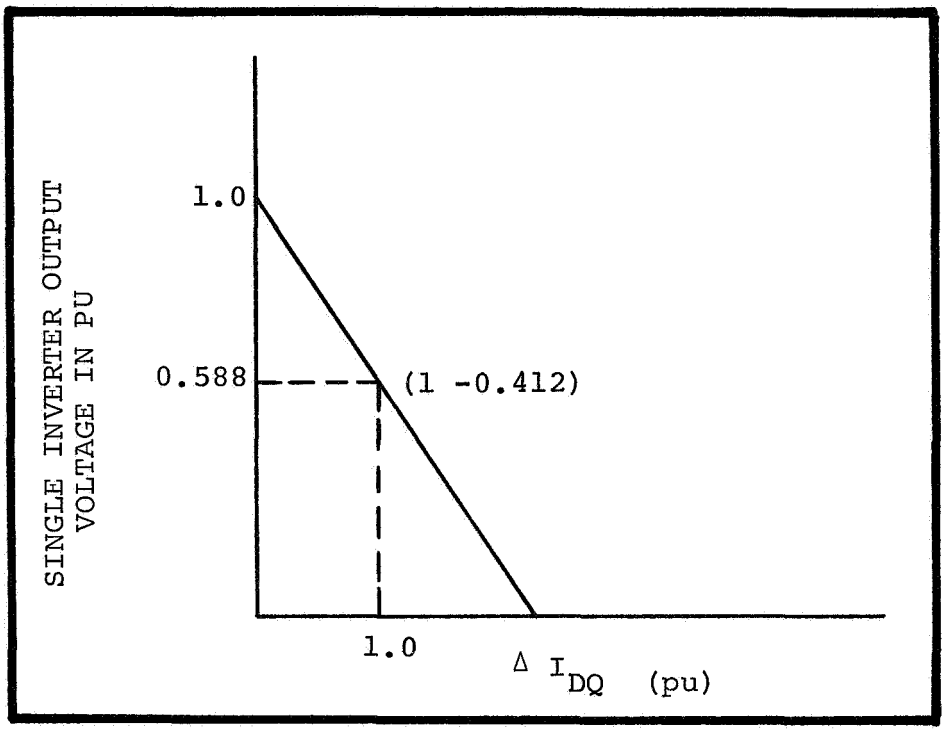


Figure 7. - Desired Transfer Curve for the AC Load Division Circuit

converter or an a static inverter; (B) one of the quadratic transformers; (C) the heat sink on which the power inversion stage components are mounted; (D) the countdown circuits; (E) the inverter load sharing detector circuit; (F) the current-limiting current transformers; (G) the inverter output filter; (H) the voltage-booster and booster filter; (I) the input filter; (J) the voltage regulator, magnetic-amplifier circuit board; (K) the tuning-fork-oscillator frequency reference; (L) the frequency-reference selector circuit board; (M) the unijunction-transistor, relaxation-oscillator circuit board; (N) the inverter output voltage sensing transformer; (O) the six power rectifiers used for converter operation; and (P) the simple saturable reactor used in the static converter load-division circuit.

Test Program for Laboratory Evaluation of the Parallel Inverters

The electrical models were first operated as isolated static inverters to measure the load-division-circuit gain. The accuracy of this circuit design was checked by supplying rated load current

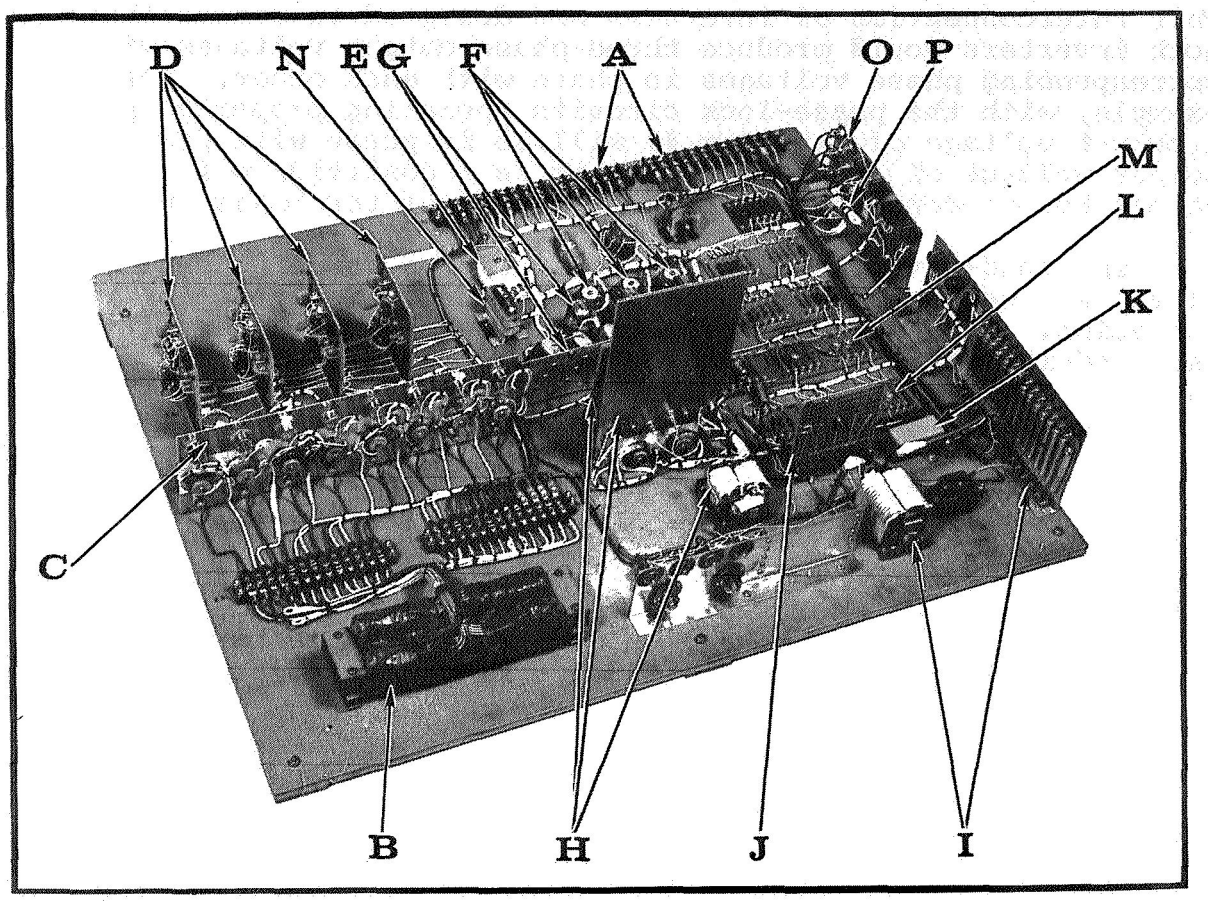


Figure 8. - A Static Inverter/Converter Test Model

at 0.5 lagging power factor from one inverter model. When the load-division current-transformer secondary is not shorted, the inverter output voltage is designed to decrease from a nominal value of 115 volts to approximately 67.5 volts. This characteristic was checked on both inverter models.

Next, the operation of the frequency-locking circuits was checked. When both inverter models were energized, only one of the two tuning-fork frequency references started and determined the output frequency of both inverter models. This frequency-locking circuit was designed to select one of two or more tuning-fork oscillators in the parallel inverter system, and to use the selected oscillator to control the frequency of all the paralleled inverters. In some parallel system applications, it may be preferable to eliminate this frequency-locking circuit by using only one frequency reference for the entire system.

The operation of the phase-lock circuits was then tested. This interconnection of inverters was designed to assure that both inverters would produce three-phase output voltages with corresponding phase voltages in phase with each other. For example, with the phase-lock circuits operating properly, phase A output voltage of inverter #1 will be in phase with phase A output voltage of inverter #2. This is a condition which must be met before connecting the inverter output terminals in parallel.

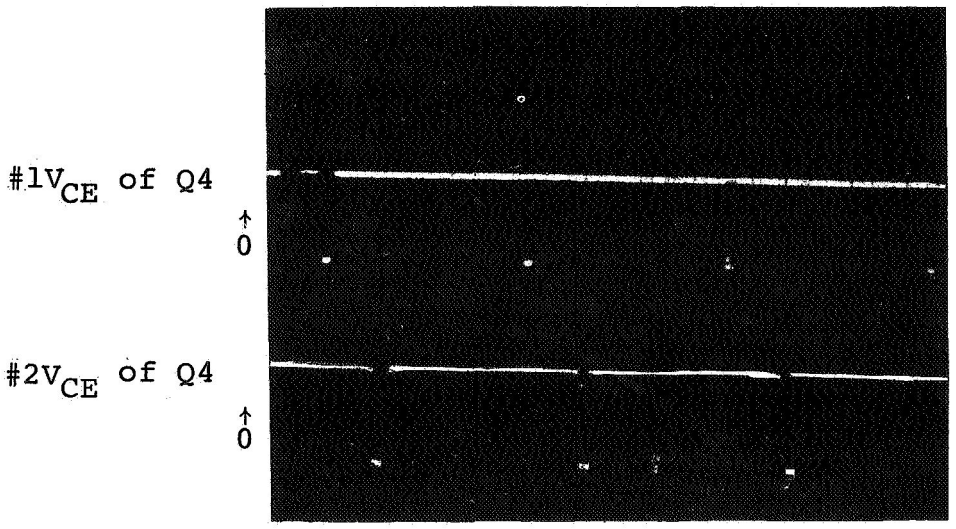
The load-division current-transformer secondary terminals, X1 and X2, were short circuited during normal isolated-inverter operation. This allows an electrical load to be connected to the isolated-inverter without the output voltage drooping because of the load division circuit. When the inverter-model output terminals were connected in parallel, the load-division current-transformer secondaries were connected in a series loop as shown in figure 5. These current-transformer secondary terminals were short circuited automatically with auxiliary contacts on the paralleling circuit breaker during isolated operation. Ammeters and wattmeters were used to determine how well the load was shared between inverters under steady-state conditions. A recording oscillograph was used to record load-sharing characteristics during paralleling transients and load transients.

Static Inverter Paralleling Evaluation

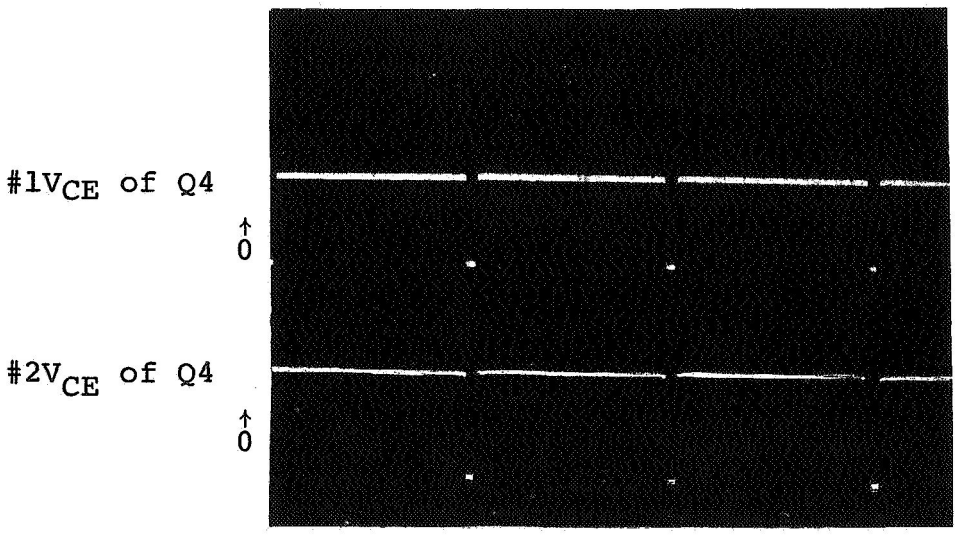
An improved phase-locking method became apparent through testing and is discussed in the phase-locking section. The test data obtained are discussed in detail in their appropriate sections.

Frequency locking. - The frequency-locking circuits functioned as planned. Figure 9(a) shows the oscilloscope trace of the collector-to-emitter voltage of transistor Q4 on each inverter prior to closing switches K1, K2, and K3. It is obvious that these voltages are not in phase. These voltages are also occurring at slightly different frequencies. The difference frequency between the two tuning fork oscillators was only about 0.04 Hz. This small frequency difference is not apparent on this photograph. Figure 9(b) shows these same voltages after switches K1, K2, and K3 are closed. These voltages are in phase and are occurring at the same frequency.

It should be noted that closing K1, K2, and K3 does not assure that the output voltages of the inverters are in phase. The output voltages are phase locked, but they can be out of phase by $45n°$, where $n = 0, 1, 2, \cdots, 7$. Of course, since n can be zero, the output voltages can be in phase if switches K1, K2, and K3 are closed under certain conditions. The last two statements are strictly true only when both inverters have identical loads. This



(a) Prior to Closing Switches K1, K2, and K3



(b) After Closing Switches K1, K2, and K3

Figure 9. - Oscilloscope Tracing of the Collector-to-Emitter Voltage of Transistor Q4 on Each Inverter

subject is discussed fully under the heading "Phase Locking".

There are two problems associated with this frequency-locking circuit which should be discussed: the long start-up time of tuning-fork oscillators and the number of components and interconnections required between paralleled inverters.

The long start-up time (two to four seconds) of a tuning-fork oscillator presents a problem if the tuning-fork oscillator that is operating in a paralleled system should fail. The failed tuning-fork oscillator must be shut off and one of the other tuning-fork oscillators must be started. The inverters must be unparalleled during the transition period since each inverter would be operating at its own unijunction-transistor relaxation-oscillator frequency. The use of faster starting oscillators such as crystal oscillators, multivibrators, etc., would shorten the transition period considerably. It should be noted that a parallel inverter system will always be disturbed for at least a fraction of a second if the operating frequency reference should fail.

It would be difficult to instantly switch to another frequency reference and to have the new frequency reference operate at the same frequency and in phase with the voltage pulses that would have occurred if the first frequency reference had not failed. A suitable circuit has been developed for accomplishing this switching function and achieves this transition in less than one millisecond.

The second problem associated with the frequency-locking method is that for each additional inverter that is inserted in a parallel inverter system, a resistor and a diode must be added to every inverter in the parallel system. For a parallel inverter system having n inverters, there must be n-1 such resistors and n-1 such diodes in each of the inverter frequency-locking circuits. With this frequency-locking method, the number of interconnections between inverters increases as the number of inverters in the system increases. Hence, as the number of necessary interconnections increases, the reliability of these interconnections decreases.

Another important consideration is that the maximum number of static inverters of a given design which can be operated in parallel is limited by the number of resistors and diodes in each frequency-locking circuit. It would be more desirable to be able to parallel an unlimited number of static inverters of a given design. In this way, a standard inverter design could be utilized in a wide variety of applications.

A practical solution to this problem is available and is recommended. The solution is to use a single frequency reference which is physically separated from all of the inverters.

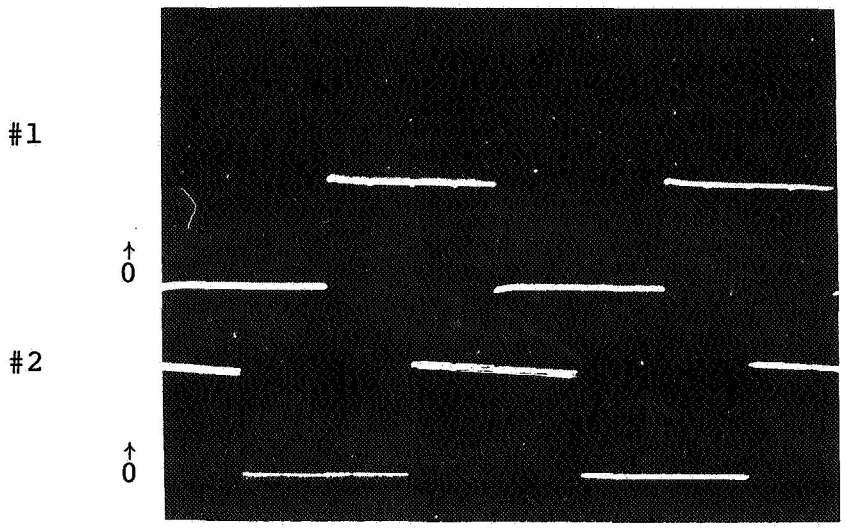
The frequency reference should contain as many frequency standards as required to meet the desired reliability with a "frequency locking circuit" similar to the one used in this study. A new "frequency locking circuit" was developed which allows all of the frequency standards to operate continuously. The circuit used in this evaluation shuts off all but one of the frequency standards. The new circuit by-passes the disadvantage of the long start-up time of a tuning-fork oscillator mentioned above and minimizes the frequency disturbance which results from changing frequency standards.

Each inverter package should contain its own unijunction-transistor relaxation-oscillator or some other type oscillator, which can be synchronized with the frequency reference. Then each inverter can be operated unparalleled and independent of the frequency reference if the frequency reference were to fail completely. A unijunction-transistor relaxation-oscillator can be accurate to about one percent. The number of necessary interconnections between the inverters would not be affected by the number of inverters in the parallel system. The number of components in each inverter would not be affected by the number of inverters in the parallel system. Therefore, a standard inverter of this type could be built and operated independently or in parallel with an unlimited number of similar inverters.

Phase Locking. - The phase-locking circuits functioned properly. The oscilloscope traces in figure 10 show the inverters operating out of phase and in phase. The inverters were forced to operate in phase by closing switch K4 shown in figure 9.

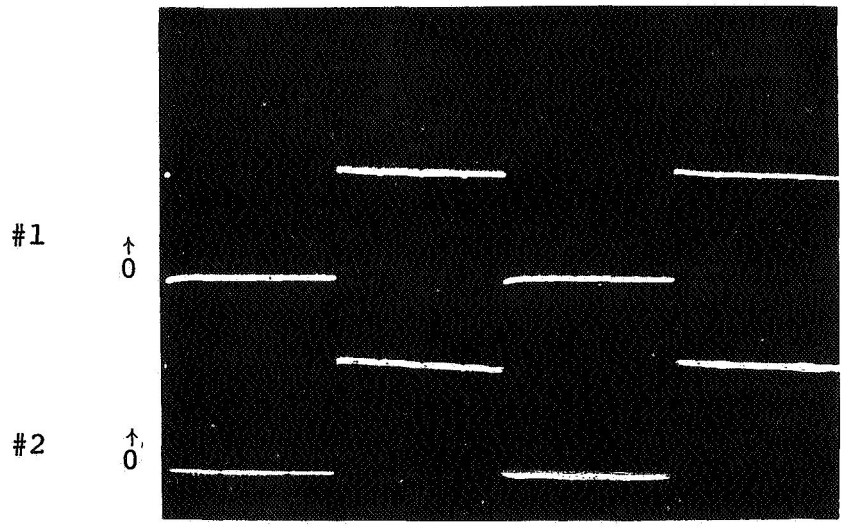
The method of closing switch K4 to lock the inverter countdown circuits in phase is undesirable from a system transient standpoint. As mentioned previously, when the frequency-locking circuits are energized, the output voltages can be out of phase by $45n°$, $n = 0, 1, 2, \cdots, 7$. When switch K4 is closed, one or both of the countdown circuits in the inverters must be disturbed and must shift until both countdown circuits operate in phase with each other. The output voltages will be disturbed during this period of time. If switches K1, K2, and K3 are closed simultaneously and at random, there is no way of knowing which one (or if both) of the countdown circuits will change when switch K4 is closed. Thus, the system load voltage could be distorted for as long as one output cycle while the two inverters are getting in phase with each other. This is not harmful to the inverters but could be detrimental to the proper operation of gyro-motors or other frequency-sensitive devices operating on the bus.

This phase-locking transient can be completely eliminated if switches K1, K2, and K3 are initially closed only at an instant



(Picture #3)

(a) Switches K1, K2, and K3 closed



(Picture #4)

(b) Switches K1, K2, K3, and K4 closed

Figure 10. - Oscilloscope Tracing of the Collector-to-(-inp) Voltage of Transistor Q17A on Each Inverter Showing (a) the Inverters Operating at the Same Frequency but Out of Phase and, (b) the Inverters Operating at the Same Frequency and In Phase

when the two inverter countdown circuits are in phase with each other. By locking the inverter frequencies together at that instant, the inverters will remain in phase with each other without closing switch K4.

This method of simultaneous frequency and phase locking was experimentally verified in the laboratory by manually closing switches K1, K2, and K3 when the two inverter countdown circuits were observed (on a dual-channel oscilloscope) to be in phase with each other. For output frequency differences above 0.1 cycle per second, it would be impossible to physically observe the proper paralleling conditions and to manually close switches K1, K2, and K3 at the proper instant. Thus, an automatic paralleling circuit is needed to assure that paralleling is achieved at the proper instant. Such an automatic paralleling circuit was developed on this program and is reported in NASA CR-1225.

Conventional methods for the automatic paralleling of rotating ac generators rely on observations of the corresponding generator terminal voltages to determine whether two generators are near enough in phase to be paralleled. This method is not sufficiently accurate for paralleling static inverters because of the static inverter internal impedance. For example, if two identical isolated static inverters are dissimilarly loaded and their respective output voltages are exactly in phase with each other, the two countdown circuits will not be in phase with each other. For this reason, the static inverter terminal voltages cannot be used to determine whether two countdown circuits are in phase. Fortunately, the instant that the countdown circuits are in phase can be easily determined with simple static logic circuits. Two inverter countdown circuits are in phase with each other and can be connected to the same frequency reference during the periods when transistors Q4, Q18A, A18B, Q18C, and Q18D of both inverters are conducting. (See figure 11.) This moment can be determined by a "NOR" circuit as discussed in NASA CR-1225.

Load Division. - The data taken during the parallel inverter tests show that the load-division circuit performance met or exceeded the performance specified previously. These data are discussed in detail in the following paragraphs.

Load-division circuit gain: The actual load-division circuit gain was measured in the laboratory. The gain was determined on an isolated inverter as follows:

(1) First the no-load terminal voltage (V_{NL} REG) was measured.

(2) Then all external leads to the load division CT terminals X1 and X2 were disconnected.

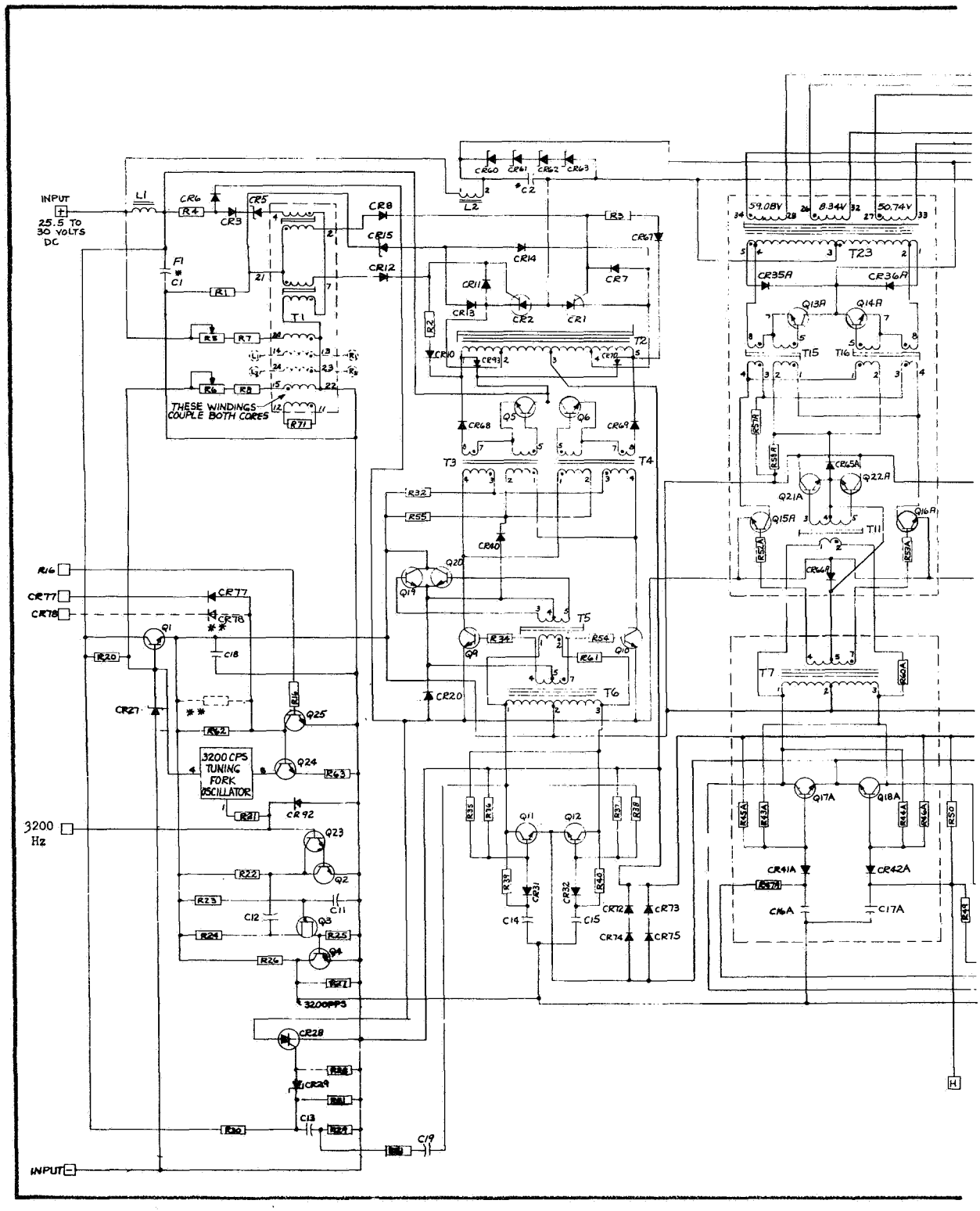
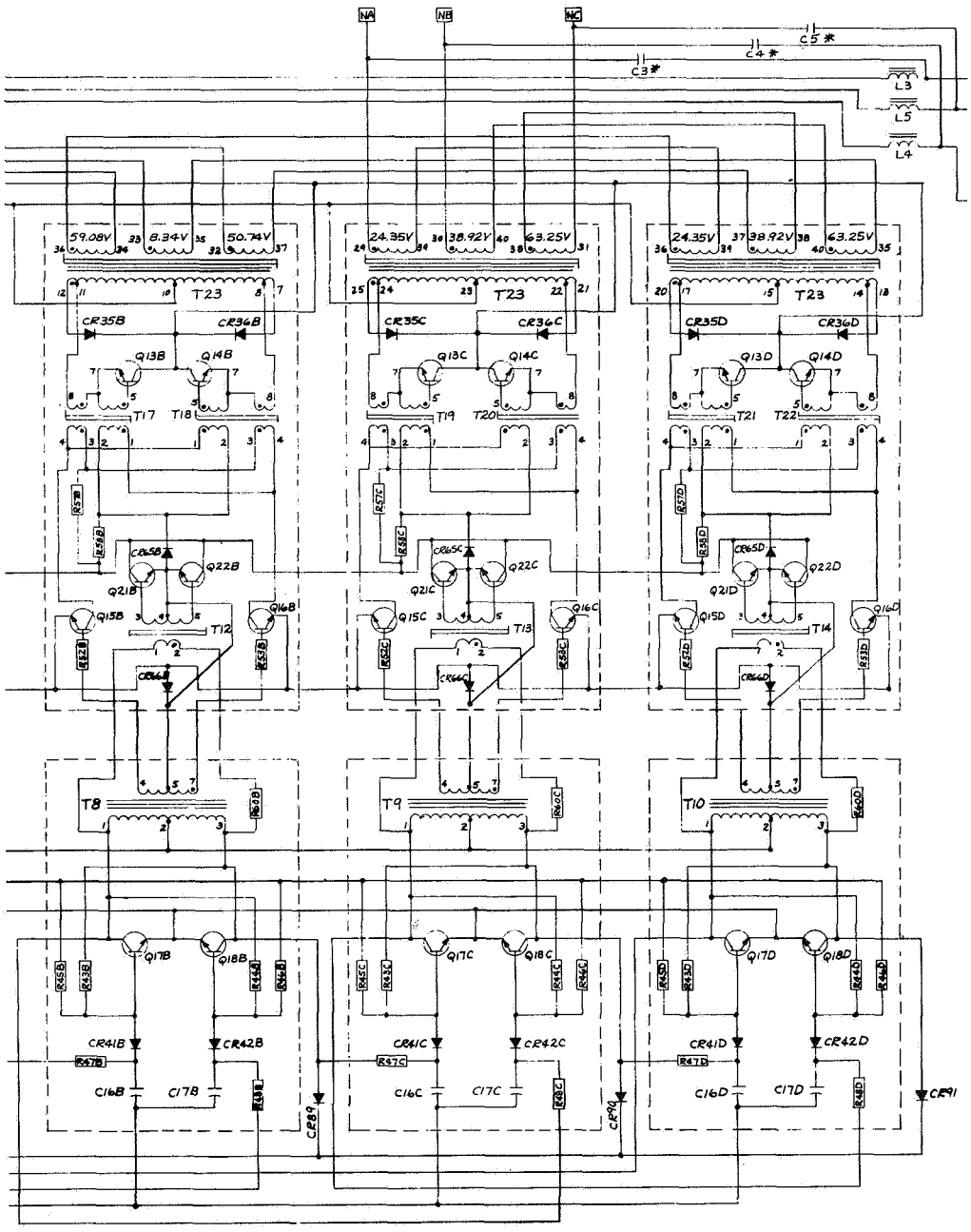


Figure 11. - Schematic Diagram of Inverter/Converter Models to



* C1, C2, C3, C4 & C5 ARE PARALLEL CAPACITOR COMBINATIONS

** ADDITIONAL RESISTORS & DIODES ADDED WHEN MORE THAN TWO INVERTERS ARE OPERATED IN PARALLEL.

be Used to Demonstrate Parallel Operation

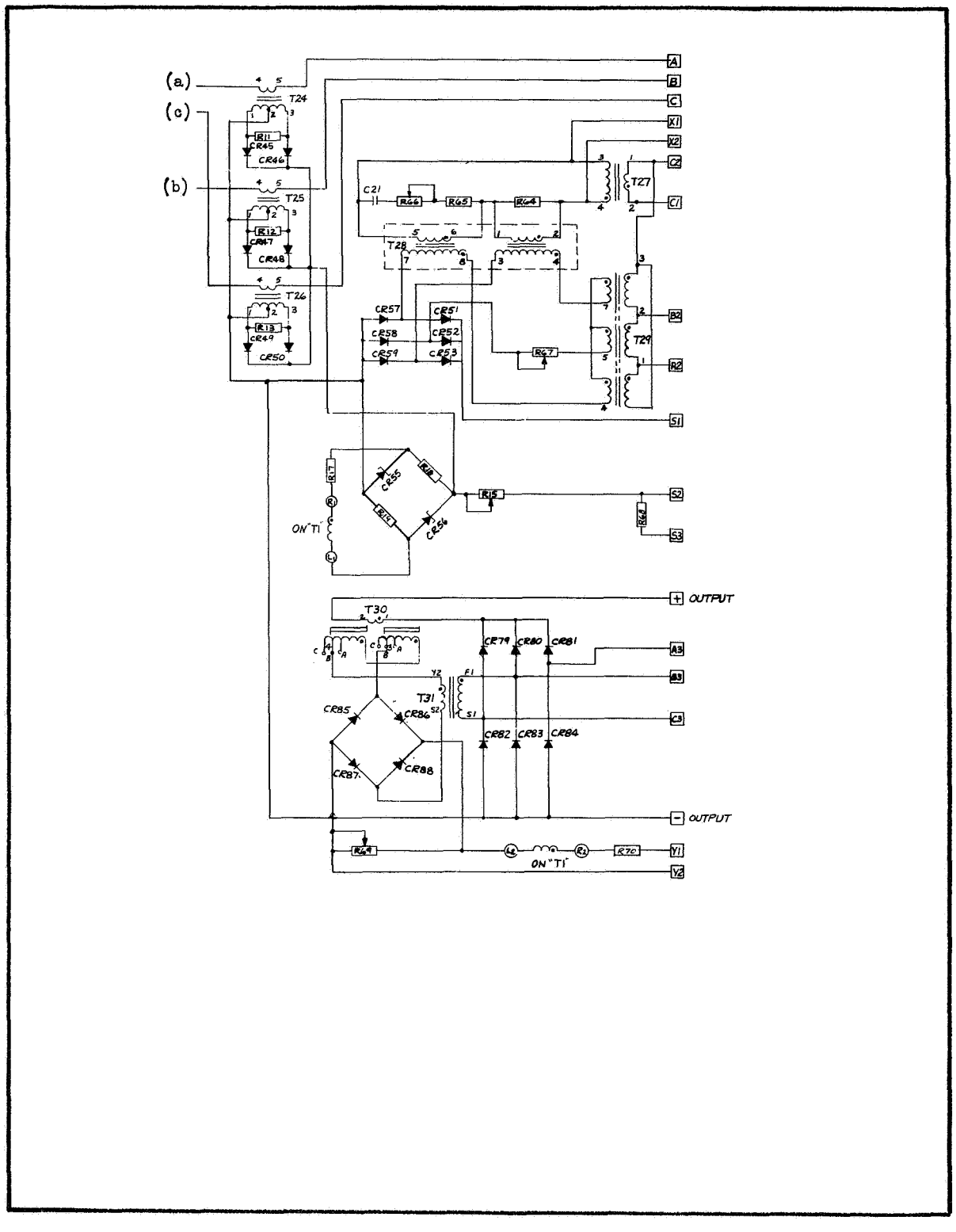


Figure 11. - Continued

(3) Then a balanced 0.5 lagging PF load that drew a 1.0 pu current per phase was connected to the inverter. The new terminal voltage V' was then measured,

then the actual load-division-circuit gain can be calculated:

$$\frac{\partial V_t}{\partial I_{DQ}} = -\left(1 - \frac{V'}{V_{NL\ REG}}\right) \tag{28}$$

The actual gain obtained by the above procedure was

$$\frac{\partial V_t}{\partial I_{DQ}} = -0.45, \tag{29}$$

which exceeds the design goal of

$$\frac{\partial V_t}{\partial I_{DQ}} = -0.412. \tag{30}$$

Load division with balanced three-phase loads: The load-division circuit performance for balanced three-phase loads was very close to the performance predicted by the theory. The test data were taken with 0.5 pu loads of both 1.0 and 0.75 lagging PF.

The 1.0 PF load case gave a 9 percent current unbalance and 6.9 percent real load unbalance. The 0.75 PF case gave a 7.8 percent current unbalance, a 4.6 percent real load unbalance, and a 8.6 reactive load unbalance.

The current unbalance obtained with the two power factor loads can be further verified by use of the measured load-division-circuit gain and the measured internal impedance of the inverter (see earlier discussion of Static Inverter Paralleling Evaluation). These values are

$$\dot{Z}_1 = 0.305 \text{ pu } \underline{/70.3^\circ} = 0.103 + j\ 0.288 \tag{31}$$

and

$$\frac{\partial V_t}{\partial I_{DQ}} = -0.45 \tag{32}$$

The actual value of $\frac{\partial E}{\partial I_{DQ}}$ is obtained by using the following

equation:

$$\frac{\partial E}{\partial I_{DQ}} = (1 - \frac{\partial E}{\partial V_S}) \quad \frac{\partial V_t}{\partial I_{DQ}} = 39(-0.45) = -17.55 \tag{33}$$

For the unity power factor 0.5 pu test case,

$$\frac{|\dot{Z}_1 + \dot{Z}_L|}{Z_L} = \frac{|2.103 + j\ 0.288|}{2} = 1.06. \tag{34}$$

The terminal voltage for 50 percent load was set on one inverter at 110.5 volts. Since equation (2b) gives $\Delta E \approx -Z_1\ \Delta I_Q$, then equation (B9a) becomes

$$-0.305\ \Delta I_Q = (1.06 + 38)\ (\frac{110.5 - 115.2}{115}) + 17.55\ \Delta I_Q \tag{35}$$

or

$$\Delta I_Q = \frac{(39.06)(0.0408)}{17.855} = 0.0895 \text{ pu} \tag{36}$$

which is very close to the test values of 0.09 pu.

Similar calculations for the 0.75 lagging PF, 0.5 pu test case give

$$\Delta I_Q = 0.084 \text{ pu} \tag{37}$$

while the actual test data give

$$\Delta I_Q = 0.078 \text{ pu} \tag{38}$$

These results verify the design procedure quite well.

The transient response of the inverters during paralleling was determined by a recording oscillograph. There was essentially no transient when paralleling two equally loaded inverters; so those oscillographs are not shown. A typical oscillograph recording of the transient caused by paralleling an unloaded inverter with a loaded inverter is shown in figure 12. The transient lasts about 30 milliseconds. The transient caused by suddenly applying rated load to two parallel inverters is shown in figure 13.

Solid Lines Show Envelope of Transient

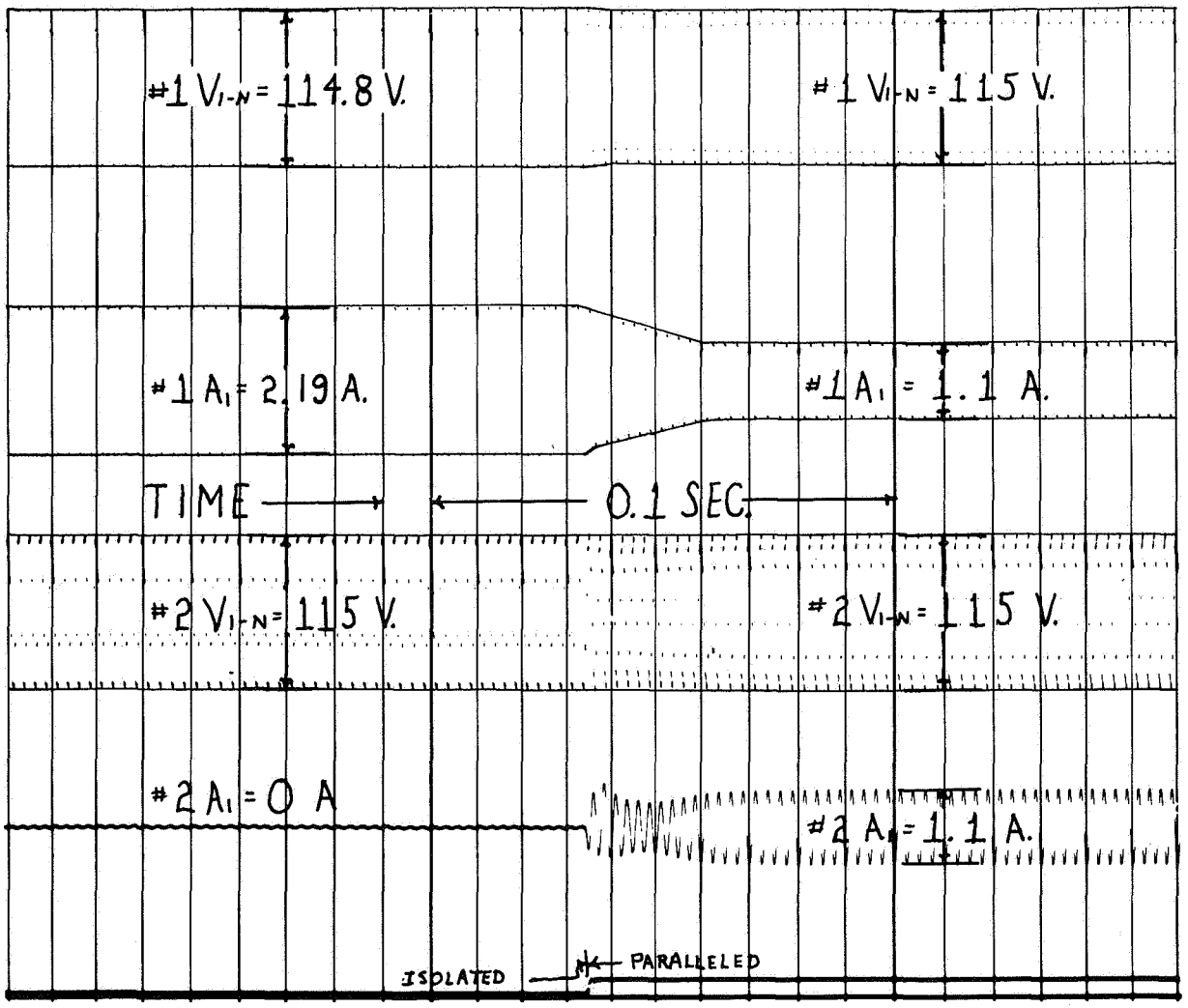


Figure 12. - Oscillogram of the Transient Caused by Paralleling a Loaded Inverter with an Unloaded Inverter

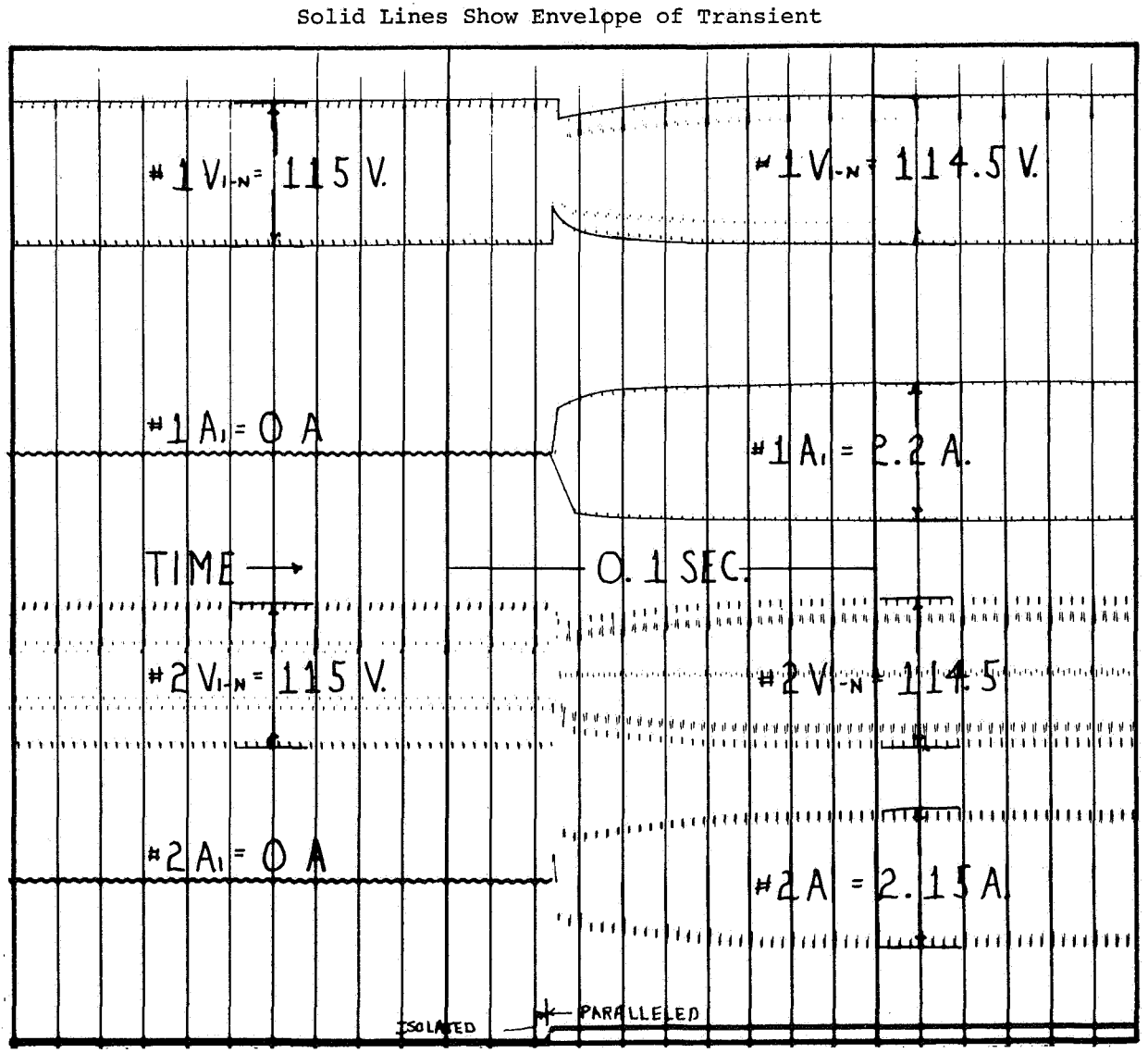


Figure 13. - Oscillogram of the Transient Caused by Suddenly Applying Rated Load to Two Parallel Inverters

Load division with unbalanced three-phase loads: It was desired to demonstrate that the paralleled inverters would share load satisfactorily under unbalanced load conditions, particularly if there was no load on phase C. The load-division circuit senses the differential current of only one phase in each inverter. Figure 11 shows that phase to be phase C. Phase C current is designated as A3 on figure 14. Figure 14 contains before and after paralleling data taken under one of the different unbalanced load conditions tested. The oscillograph recording shows phase A currents and voltages for both inverters for that condition. The individual phase currents and watts were shared within 14 percent of rated current and watts in all cases. The worst case, as expected, occurs when phase C is unloaded.

These data (not shown) illustrated a possible disadvantage of regulating the average of the three-phase voltages. The output terminal voltages under the individual phase loads can be made to share very closely without sensing all three of the phase currents. The individual phase voltages can be made to stay within a predetermined range with a predetermined amount of load unbalance by judiciously designing the output filter. Individual phase voltage regulation should be used when extremely close individual phase voltage regulation is required. This approach requires a more complex voltage regulation circuit and requires that differential load currents be sensed in each output phase.

Load division with unequal inverter input voltages: The inverters were designed to operate with an input voltage range of 26 to 30 volts dc. The effect on the load-division circuit operation due to variation of the input voltage was insignificant.

Load division while starting an induction motor: Figure 15 is an oscillograph recording showing a 1/8 hp induction motor starting current transient being supplied by inverter #1. Figure 16 is an oscillograph recording showing the motor starting current being supplied by the two inverters connected in parallel. Note that the parallel inverters share current during the starting transient. This shows that a motor which requires more starting current than one inverter can supply, can be started with two or more inverters connected in parallel.

Experimental determination of static inverter internal impedance. - The internal impedance of the static inverter was determined analytically in appendix D. The internal impedance was found to be

$$\dot{Z}_1 \cong 0.27 \text{ pu } \angle 77.8° \tag{37}$$

The actual internal impedance of the static inverter breadboard was determined experimentally by the use of Thevinen's Theorem.

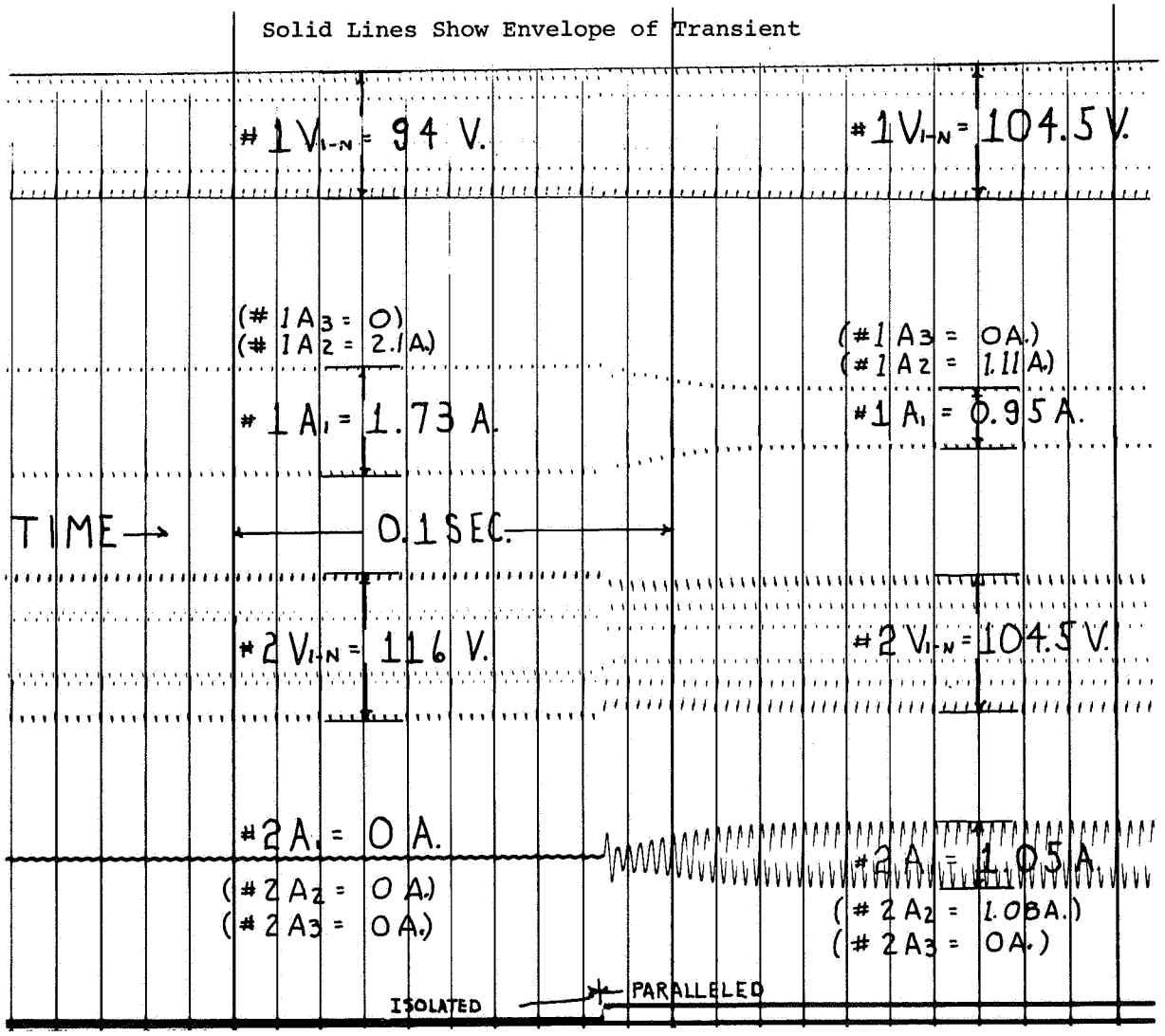


Figure 14. - Oscillogram of the Transient Caused by Paralleling the Inverters with Unbalanced Loads

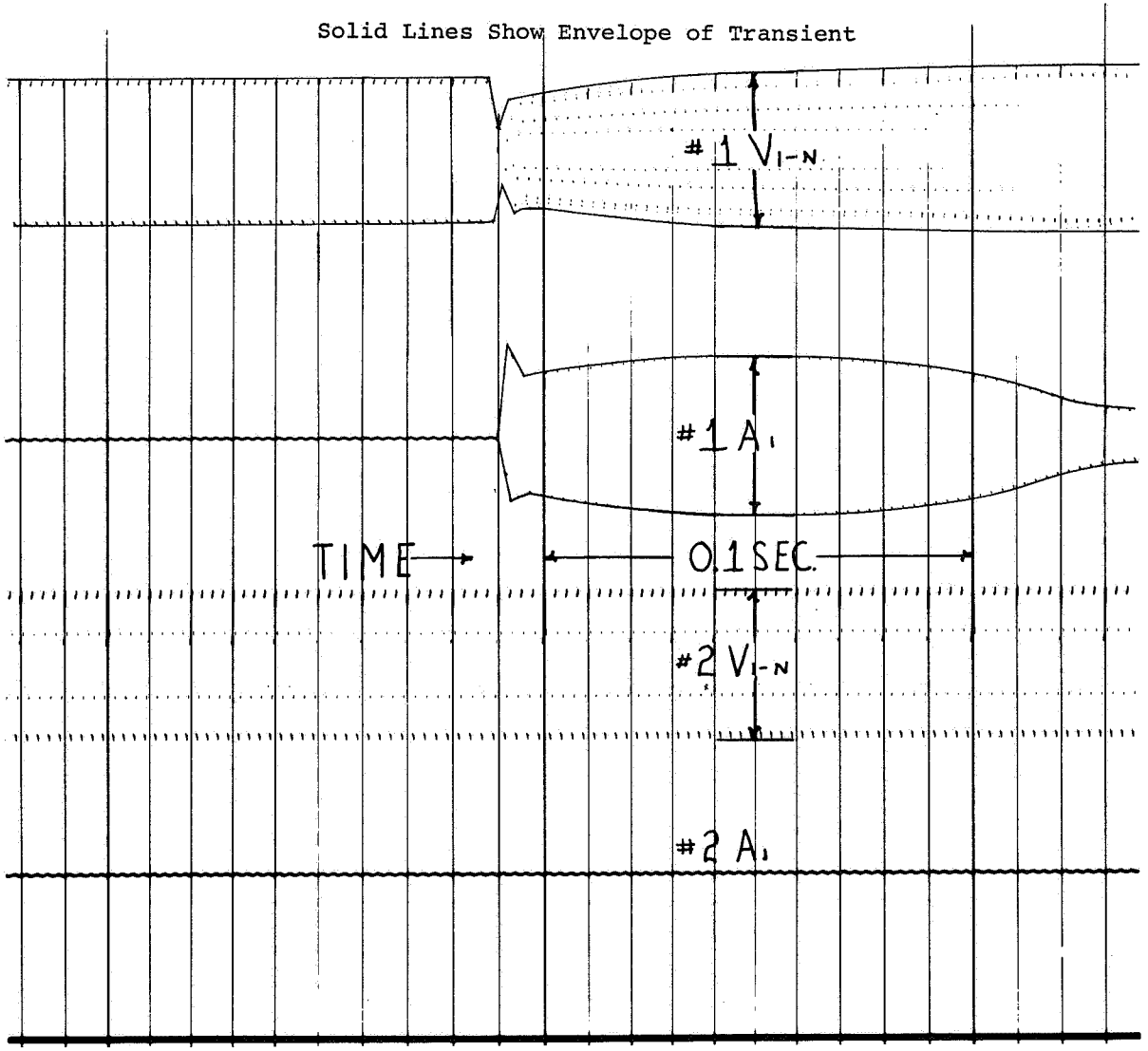


Figure 15. - Oscillogram of One Inverter Starting a 1/8 HP Motor

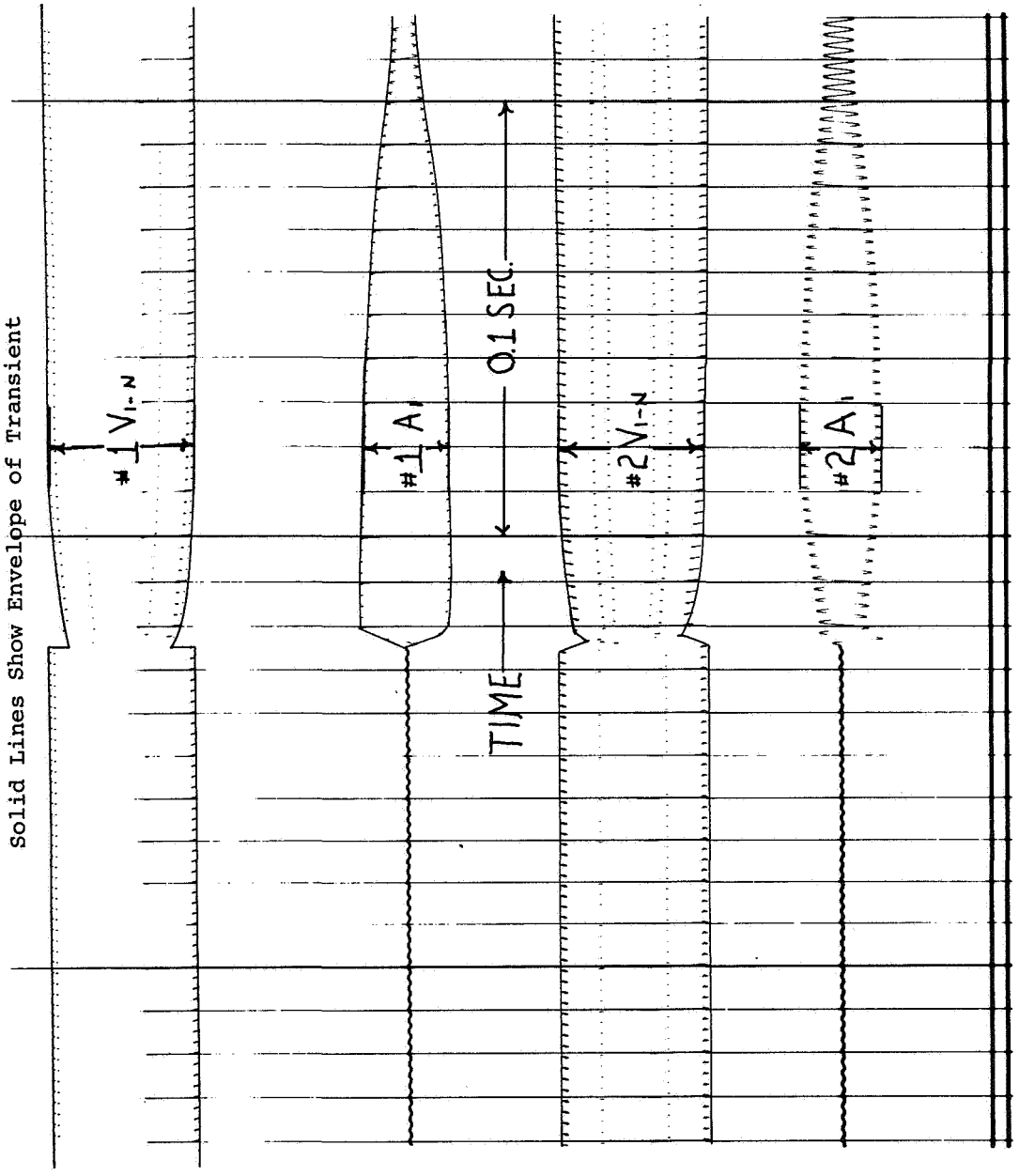


Figure 16. - Oscillogram of Two Parallel Inverters Starting a 1/8 HP Motor

The actual value was determined to be

$$\dot{Z}_1 \cong 0.305 \text{ pu } \underline{/70.3°} \tag{38}$$

which is in reasonably close agreement with the originally calculated value above.

Because of the relative ease of measuring the internal impedance of a static inverter, this procedure is preferred to the calculation method described in appendix D and should be used whenever an inverter model is available for the purpose.

CONSIDERATIONS FOR PARALLELING STATIC CONVERTERS

Load-Sharing Control Method

Load sharing between paralleled converters can be accomplished by adjusting the internal voltage of each converter as a function of differential load current. The output current of each converter must be sensed and compared to the average output current of all paralleled converters. The internal voltage of each converter should be automatically adjusted to give proper load division. The proper load-division ratio for each converter is determined by the ratio of the kW rating of the individual converter to the sum of the kW ratings of all paralleled converters. This study is concerned with paralleling similar converters, so each converter should supply an equal current.

The load-division circuit incorporated in the two model converters is shown schematically in figures 17 and 11. Figure 17, which shows two converters connected in parallel, will be referred to in describing the operation of the load-division circuit.

The converter operation and voltage regulation method are described later under the heading "Single Converter Operation Test." The transductor circuit remains unchanged except for the addition of a filter capacitor, C23, across its output. This capacitor and a converter output filter, L6 and C22, were found necessary to prevent low frequency modulation of the individual converter load currents during parallel operation. When CONVERTER A LOAD CURRENT equals CONVERTER B LOAD CURRENT, the transductor outputs across R69A and R69B are equal. During this condition, there is no potential difference to cause a current to flow in the Y1 circuit. If CONVERTER B LOAD CURRENT exceeds CONVERTER A LOAD CURRENT, then the voltage across R69B exceeds the voltage

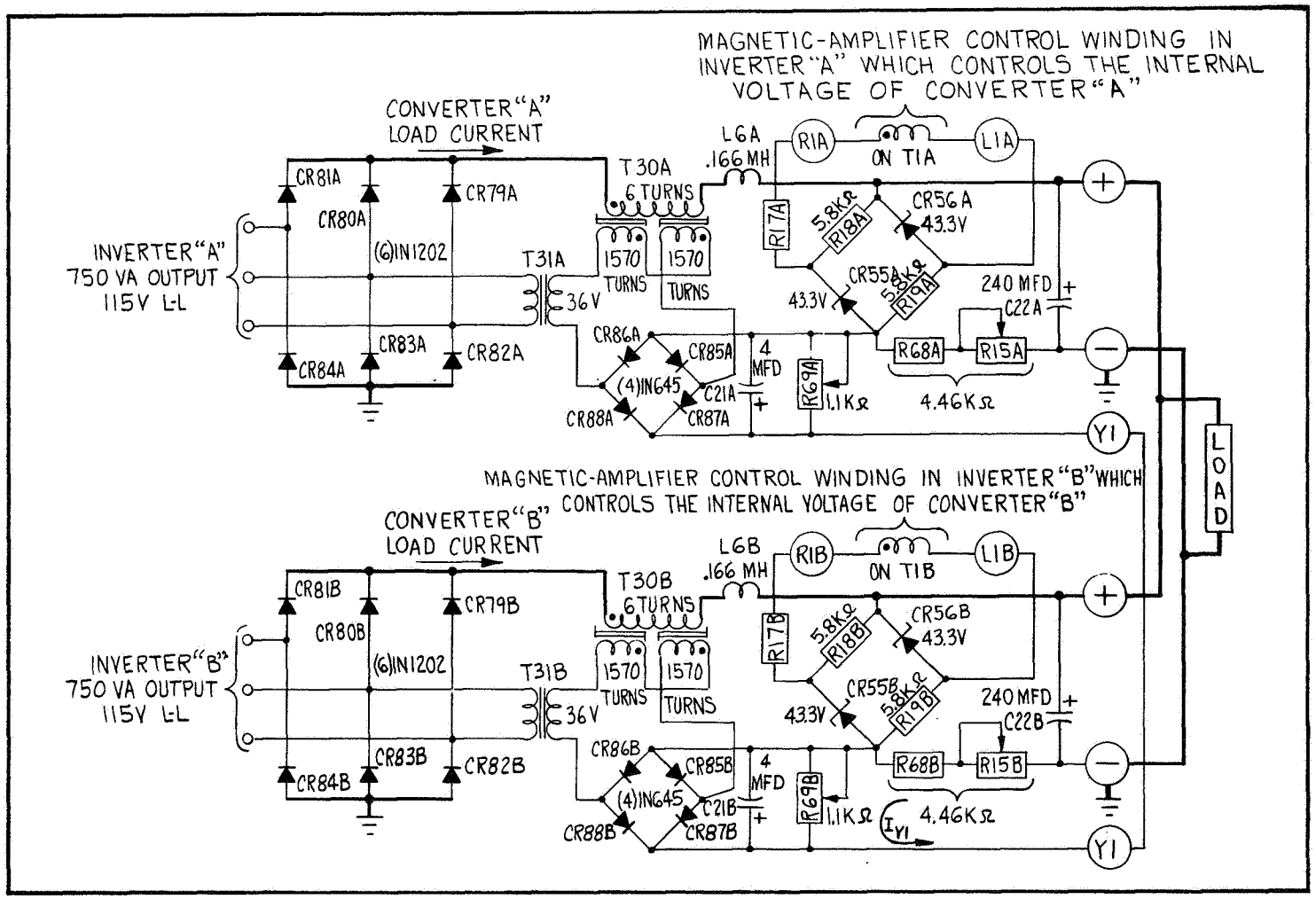


Figure 17. - Schematic Diagram of the Modified Converter Load Division Circuit

across R69A and a current, I_{Y1}, will flow in the direction shown. This current reduces the voltage drop across R68B and R15B which increases the voltage across the voltage detector bridge: R18B, R19B, CR55, and CR56. The unbalanced bridge causes a current to flow in the magnetic-amplifier control winding in the direction shown; this control current causes the associated voltage-booster to reduce the dc voltage applied to INVERTER B which causes CONVERTER B LOAD CURRENT to decrease. The polarity of I_{Y1} shown causes the opposite effect in CONVERTER A LOAD CURRENT. These effects together tend to cause the converter load currents to remain nearly equal. Any number of similar converters may be connected in parallel by this method.

Circuit Design Calculations

In the circuit design, the open-loop gain value was used as the closed-loop gain value. Therefore, the actual open-loop gain was higher than was necessary to meet the design criterion. The maximum allowable current unbalance is derived below.

The converter internal voltage, E (i.e., the no-load output voltage), will change an amount equal to the voltage across resistors R68 and R15 which is caused by current I_{Y1}. The transductor output voltage can be considered a voltage source with an internal impedance of R69. The transductor output voltage is related to the converter output current by the following ratio:

$$\frac{\text{Transductor output volts}}{\text{Converter load current}} = \frac{20 \text{ volts}}{4.88 \text{ amps}}$$

If CONVERTER B OUTPUT CURRENT exceeds the AVERAGE CONVERTER OUTPUT CURRENT, the difference between transductor B output voltage and the average transductor output voltage will be proportional to the differential current I_{DR}. The portion of the differential transductor output voltage which affects the voltage across resistors R68 and R15 is determined by the ratio of R68 + R15 to R68 + R15 + R69. The closed-loop load-division circuit gain is therefore:

$$\frac{\partial V_t}{\partial I_{DR}} = \frac{\text{Transductor output volts}}{\text{Converter load current}} \times \frac{R68 + R15}{R68 + R15 + R69} \tag{39}$$

$$= \frac{-20 \text{ volts}}{4.88 \text{ amps}} \times \frac{4.46K}{5.56K}$$

$$= -3.28 \frac{\text{converter dc volts change}}{\text{dc amperes unbalanced current}} \tag{40}$$

This gain calculated in per-unit values is:

$$\frac{\partial V_t}{\partial I_{DR}} = -3.28 \times \frac{1 \text{ pu dc volts}}{153.5 \text{ dc volts}} \times \frac{4.88 \text{ dc amperes}}{1 \text{ pu dc amperes}} \tag{41}$$

$$= -0.105 \frac{\text{pu dc volts}}{\text{pu dc unbalanced current}}$$

$$= -0.105 \frac{(0.816)(115)}{153.5} = -0.061 \frac{\text{pu ac volts}}{\text{pu unbalanced ac current}} \tag{42}$$

The load unbalance limit for this load-division circuit gain will be derived next.

The open-loop gain of the voltage regulator is expressed as follows:

$$\frac{\partial E}{\partial V_S} = - \left| \frac{E_{FL} - V_{NL\ REG}}{V_{NL\ REG} - V_{FL\ REG}} \right| \tag{43}$$

where E_{FL} is the internal voltage necessary to obtain rated terminal voltage $V_{FL\ REG}$ (at full load), and

$$E_{FL} = \frac{|\dot{Z}_1 + \dot{Z}_L|}{Z_L} V_{FL\ REG} \tag{44}$$

If the closed loop regulation is 0.7 volts line-to-neutral or 0.0061 pu volts and assuming $V_{NL\ REG} = 1.0$ pu and $V_{FL\ REG} =$ 0.9939 pu volts, then

$$\frac{\partial E}{\partial V_S} = - \left| \frac{\left| \frac{\dot{Z}_1 + \dot{Z}_L}{Z_L} \right| (0.9939) - 1}{0.0061} \right| \tag{45}$$

where $\dot{Z}_1 = 0.27 \angle 77.8°$ pu (appendix D), and $\dot{Z}_L$ must be determined.

A resistive load on a three-phase full-wave bridge appears as an impedance of 0.955 power factor lagging (reference 2) to the source.

Also

$$I_{ac} = 0.816\ I_{dc} \tag{46}$$

The VA of the source is expressed as

$$VA = \sqrt{3}\ V_{acLL} I_{ac}\ , \tag{47}$$

so the watts supplied by the source, including the diode losses are:

$$W_T = \sqrt{3}\ V_{acLL} I_{ac} (0.955) \tag{48}$$

$$= \sqrt{3}\ (115)\ (0.816)\ (4.886)\ (0.955)$$

$$= 757.5 \text{ watts} \tag{49}$$

Also

$$(I_{dc})^2\ R_L = 750 \text{ watts} \tag{50}$$

$$(I_{dc})^2\ R_{eq_L} = 757.5 \text{ watts}$$

so

$$R_{eq_L} = \frac{757.5}{750}\ R_L = 1.01 \text{ pu} \tag{51}$$

$$\therefore\ \dot{Z}_L \doteq \frac{1.01}{0.955}\ \underline{/\cos^{-1}\ 0.955} = 1.058$$

$$\underline{/\cos^{-1}\ 0.955} \text{ pu} \tag{52}$$

Knowing $\dot{Z}_1$ and $\dot{Z}_L$, the required voltage regulator gain can now be determined:

$$\frac{\partial E}{\partial V_S} = -\left| \left[\frac{\left| (0.27\underline{/77.8}\ + 1.058\ \underline{/\cos^{-1}\ 0.955}) \right|}{\dfrac{1.058}{0.0061}} \right] (0.9939) - 1 \right| \tag{53}$$

$$= -22.87$$

This gain means that if the converter is operated open loop (i.e., the output-voltage-sensing circuit is disconnected from the converter output terminals), a one-volt increase in sensing voltage will decrease the converter output voltage 22.87 volts. The gain of the voltage regulator was set to that value.

Equation B9 of appendix B is:

$$\Delta E = |E_{pL}-E_o| = (V_{pL}-V_{lL}) \frac{\partial E}{\partial V_S} + \frac{1}{K} (V_{lL}-V_o) + \frac{\partial E}{\partial I_{DR}} (\Delta I). \quad (54) \text{ or } (B9)$$

Assuming 115 ± 0.2 volts line-to-line voltage tolerance setting, then letting

$$V_{lL} = 1.00174 \text{ pu}$$

and

$$V_o = V_{pL} = 1.0 \text{ pu}$$

will give the maximum change.

So

$$\Delta E = 0.00174(22.87 + 1.146) + \frac{\partial E}{\partial I_{DR}} (\Delta I)$$

$$= (0.0419) + \frac{\partial E}{\partial I_{DR}} (\Delta I). \quad (55)$$

Since ΔI max.

$$= \frac{\Delta E \text{ max}}{Z_1}$$

$$= \frac{\Delta E \text{ max}}{0.27} \quad (56)$$

Therefore,

$$0.27 \ \Delta I \text{ max} = (0.0419) + \frac{\partial E}{\partial I_{DR}} \ \Delta I \text{ max}, \quad (57)$$

or

$$\Delta I \text{ max} = \frac{0.0419}{0.27 - \frac{\partial E}{\partial I_{DR}}} \tag{58}$$

The expression which relates the open-loop gain $\frac{\partial E}{\partial I_{DR}}$ to the closed-loop gain $\frac{\partial V_t}{\partial I_{DR}}$ is

$$\frac{\partial E}{\partial I_{DR}} = (1 - \frac{\partial E}{\partial V_S}) \frac{\partial V_b}{\partial I_{DR}} = -(23.87)(0.061) = -1.39 \tag{59}$$

So,

$$\Delta I \text{ max} = \frac{0.0419}{1.66} = 0.025 \text{ pu} \tag{60}$$

This is a close limit for a load-division circuit. From the derivation of this gain, it is apparent that the load-division circuit can be designed to have any desired gain for any desired load-division limit. Permitting a wider tolerance on the initial input voltage setting (e.g., 115 ± 4.8 volts instead of 115 ± 0.2 volts) requires an increase in the open-loop gain of the load-division circuit. In order to maintain a 0.10 pu current unbalance with a voltage setting of 115 ± 4.8 volts, the open-loop gain of the load-division circuit would have to be -9.78 instead of -1.39 as used above. The load-division circuit gain can be increased by increasing the rated transductor output voltage and/or decreasing the rated output voltage of the converter. Actual test results of this circuit are given in the following section, Single Converter Operation Test.

Single-Converter Operation Test

Terminal board interconnections were made on each inverter/converter model. This changes the static inverter output from wye to delta and connects this output to a three-phase full-wave rectifier. The output of the rectifier is considered the output of the static converter model. This dc output voltage was connected to the same zener voltage reference and voltage regulator circuit that was used for the static inverter. Resistor R15 regulates the converter output voltage at 153.5 volts dc, the rated converter output voltage.

Load-Division Circuit Evaluation

To evaluate the parallel performance of the load-division circuit, the two static converter models were interconnected. The converter output current went through transductor T30 to produce a dc output voltage proportional to the converter dc output current. The transductor output voltage appears across the variable resistor, R69. This variable resistor was set in each static converter model by applying rated load (4.88 amperes dc) to each converter and adjusting resistor R69 until 20 volts dc was measured across it. The transductor operating characteristics were recorded for each model from 0 to 6 amperes. This data is plotted in figure 18. Figure 18 shows the good linearity and repeatability which can be obtained from these simple-saturable-reactor circuits. This linearity and repeatability are necessary to obtain good current division between or among converters over wide load ranges.

Subsequent test results indicated that a filter capacitor was necessary across R69 to eliminate low frequency modulation of the converter output voltage. A four microfarad capacitor was added across R69 and the transductor operating characteristics were measured again. The addition of this filter capacitor across the transductor output required a small adjustment of R69.

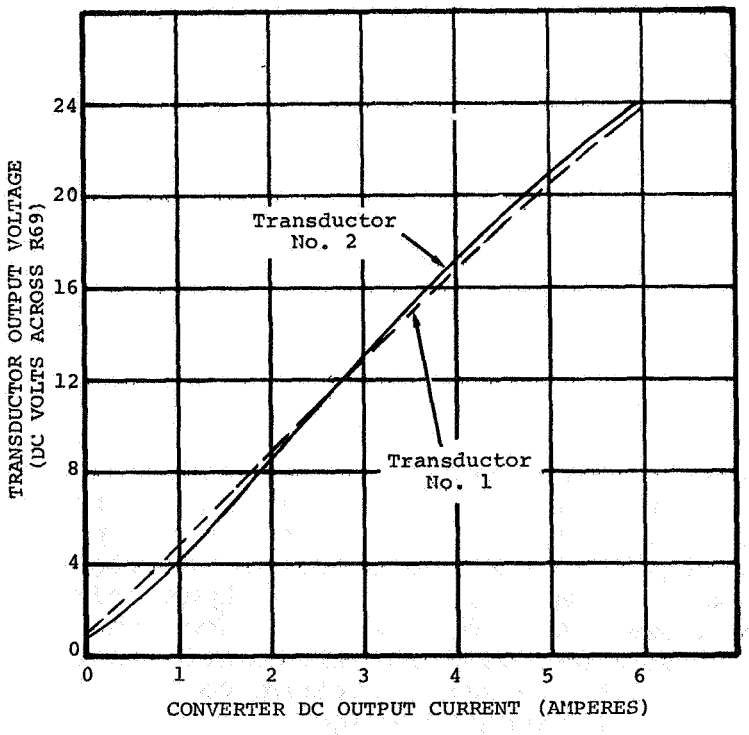


Figure 18. - Linearity of Transductor Unfiltered Output Voltage

When the two converters were connected in parallel, load current was shared better than expected. The requirements for paralleling converters are simple compared to those encountered for paralleling inverters. The converter output voltages must be nearly the same before paralleling. The Y1 terminals must be connected at the same instant the converter output terminals are connected in parallel. For the initial paralleling evaluation, each converter output voltage was set at 153.5 volts, no-load, prior to paralleling. After paralleling, load division was determined for 0, 25, 50, 75, 100, and 125 percent loads. These test results are plotted in figure 19. Oscillograph recordings were made of both converter output voltages and currents during the paralleling operations. Figure 20 is the oscillograph recording made during the paralleling operation with rated load on each converter prior to paralleling. This is typical of the oscillograph recordings made at the other loads.

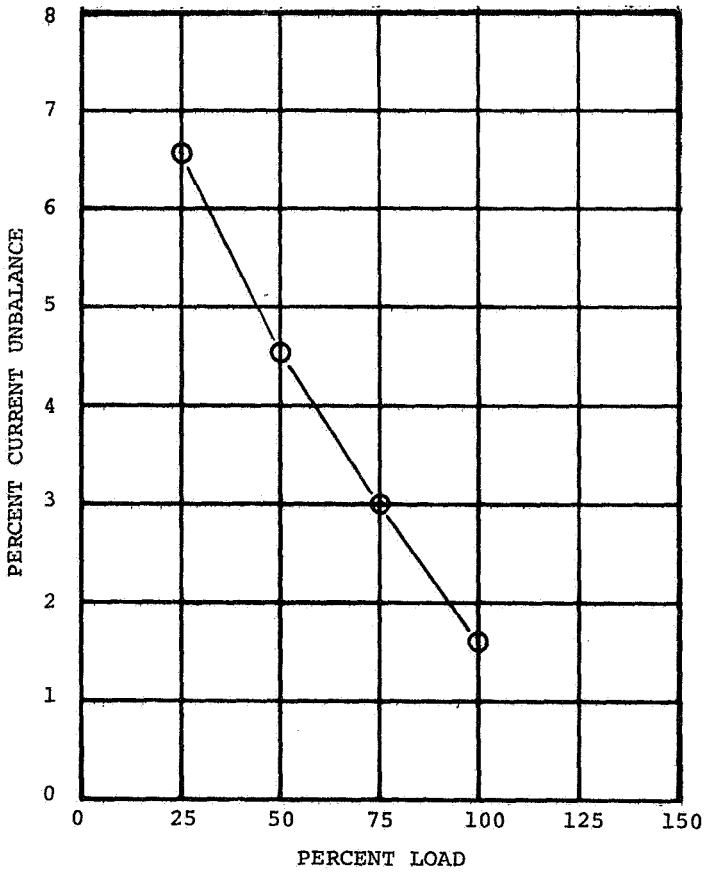


Figure 19. - Current Unbalance Between Two Converters

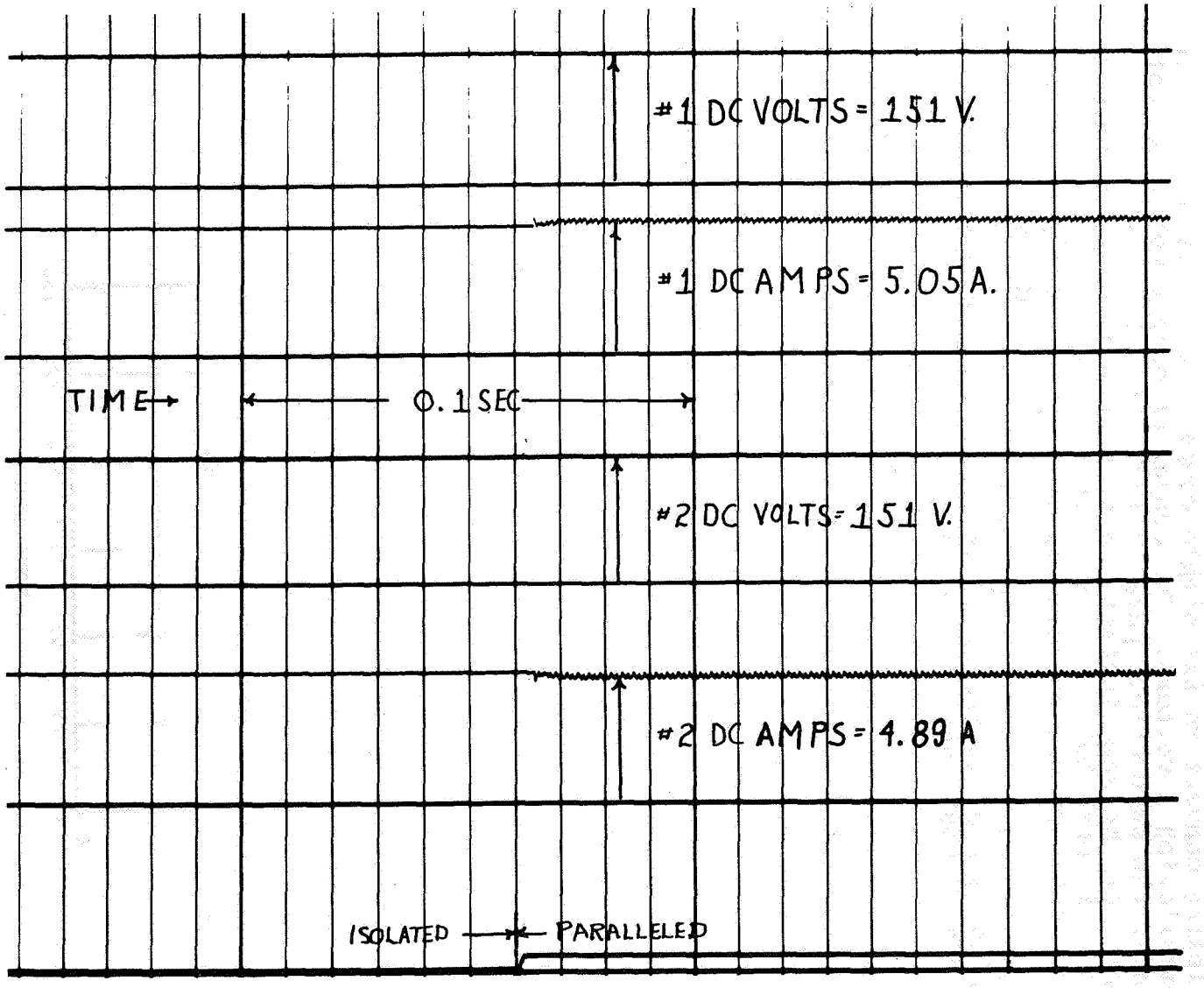


Figure 20. - Oscillogram of the Transient Caused by Paralleling Two Static Converters. Each Converter was Loaded with 100% Rated Load Prior to Paralleling

Figure 21 is an oscillograph recording taken to demonstrate that an unloaded converter could be paralleled with a fully loaded converter. The load current unbalance between converters was 1.4 percent after paralleling.

To demonstrate that large load transients can be sustained by the paralleled converters, the unloaded converters were connected in parallel. A 100 percent rated load was then applied simultaneously to both converters. Figure 22 is the oscillograph recording of this load transient.

Identical regulated static converters will share load perfectly when paralleled without a load-division circuit if the regulated voltage of each converter is exactly the same before paralleling. However, this is not usually the case. The real purpose of incorporating a load-division circuit in each converter is to assure that load current will be satisfactorily divided for the general case when the regulated voltage of each converter is not exactly the same before paralleling. To ensure that the incorporated load-division circuit satisfactorily meets this purpose, tests were conducted with the regulated voltage of each converter intentionally set to different levels before paralleling. For one series of tests, one converter no-load output voltage was set at 148 volts dc and the other converter no-load output voltage was set at 158 volts dc, prior to paralleling. After paralleling, the converter output voltage became 154 volts dc at light loads, which is nearly the average of the two output voltages prior to paralleling. The maximum load current unbalance was 4.5 percent, which is very good for these test conditions. Figure 23 is an oscillograph recording of the paralleling transient with 100 percent load connected to each converter prior to paralleling.

NOTE: The signal which appears on the bottom of all converter paralleling oscillographs to indicate whether the converters are paralleled or isolated is controlled by an auxiliary contact on the paralleling breaker. This signal occurs from 3 to 5 milliseconds before the converters appear to be paralleled. (See figure 23 for example.) It is believed that the particular breaker used for paralleling the converters had this characteristic. That is, the auxiliary contacts actually closed before the main contacts closed. This was not noticeable with the breaker used to parallel the inverters.

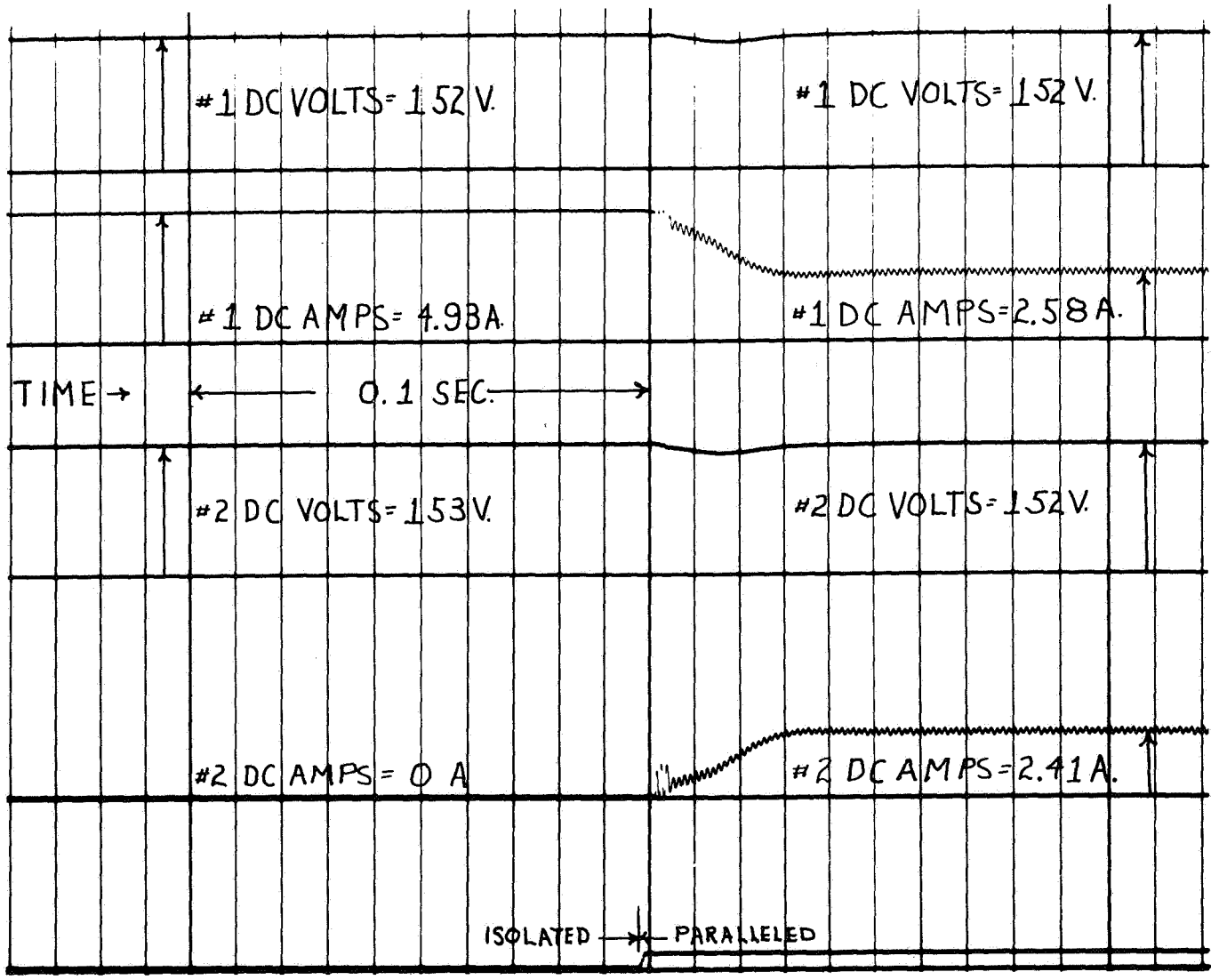


Figure 21. - Oscillogram of the Transient Caused by Paralleling a Loaded Converter with an Unloaded Converter

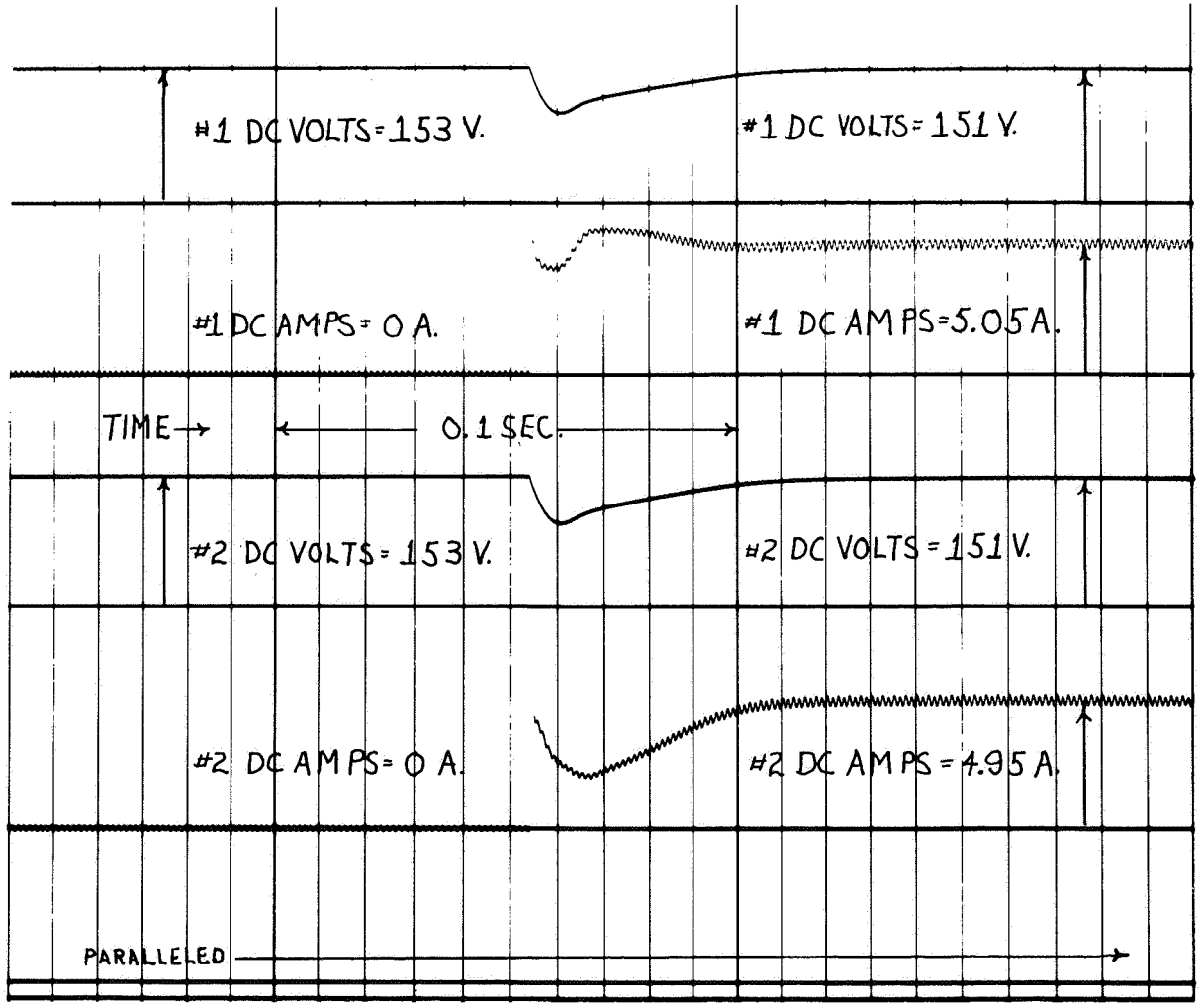


Figure 22. - Oscillogram of the Transient Caused by Placing Rated Load on Two Paralleled-Unloaded Converters

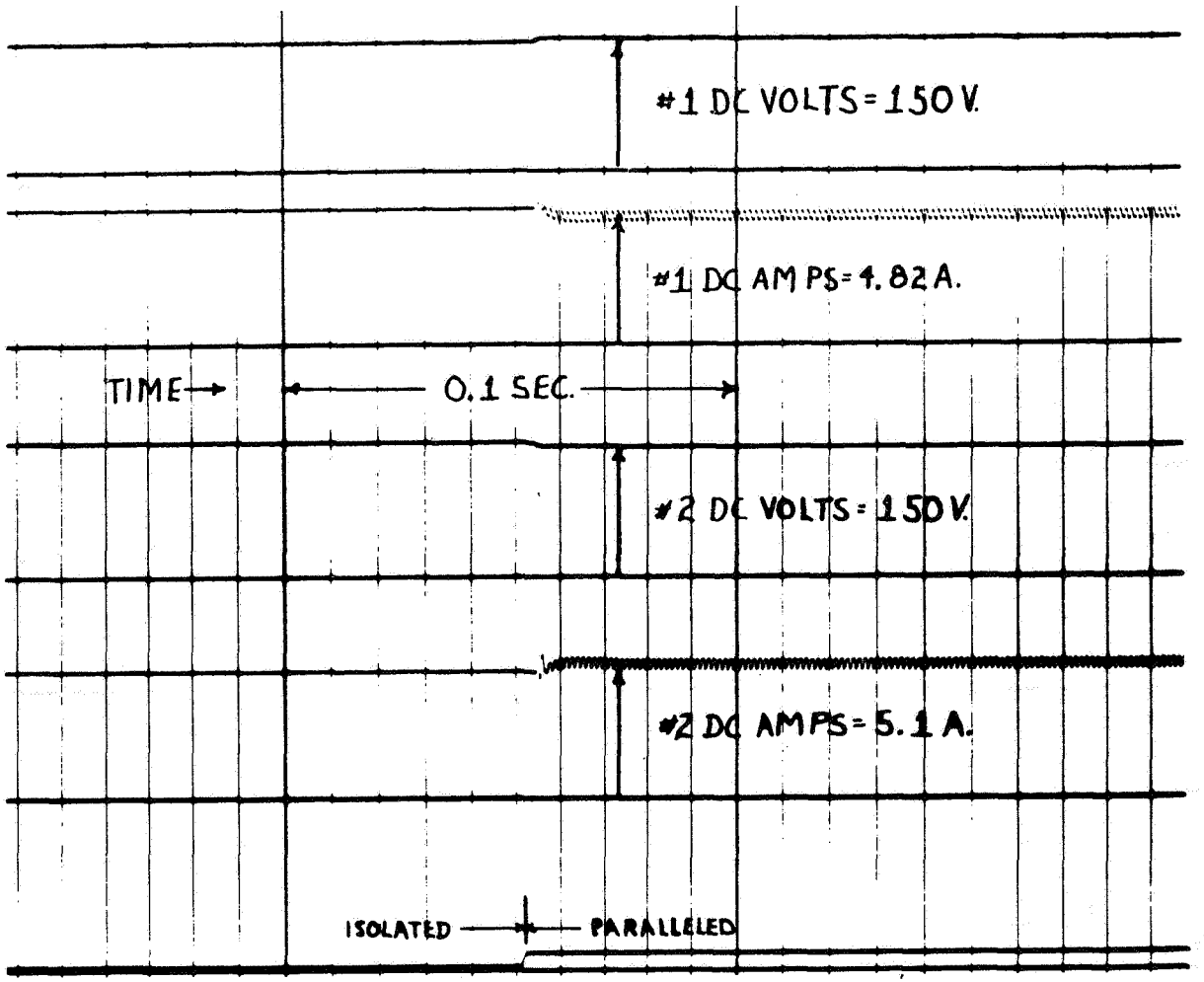


Figure 23. - Oscillogram of the Paralleling of Two Fully Loaded Converters Whose No-Load Output Voltages Had Been Preset at 148 and 158 Volts DC Prior to Paralleling

DISCUSSION OF RESULTS

The good correlation between experimental data and calculated values from the developed analytical techniques indicates that the developed analytical technique is valid. This method of analysis for static inverters or static converters operating in parallel is an excellent starting point for analyzing how any type of inverter can be operated and controlled in a parallel system.

In analyzing the parallel operation of any inverter configuration, one should start with the analytical techniques developed herein and apply these principles, with whatever modifications are necessary because of the inverter circuits under consideration, to determine how the system under consideration will operate.

CONCLUSIONS

Analytical techniques have been developed to define the electrical circuit conditions that must be satisfied in order for static inverters to be operated in parallel. Similar conditions have been defined for static converters operating in parallel.

The results of laboratory evaluation of the static-inverter paralleling circuits demonstrated that inverters can be satisfactorily paralleled if the necessary conditions are satisfied. Briefly these conditions are: (a) all inverters must operate at exactly the same frequency; (b) the internal voltage of all inverters must be in phase with each other at all times; (c) all nominal regulated output voltages must be the same; and (d) each inverter must have provisions for insuring proper load division.

The test results demonstrated conclusively that both real and reactive load can be divided satisfactorily between paralleled static inverters. The actual load division between paralleled inverters was even better than predicted by the design procedure. Any reasonable load division requirement can be met and any number of inverters can be operated in parallel with this method.

The laboratory evaluation of the static-converter paralleling circuits showed that static converters can be operated in parallel if the necessary conditions are met. These conditions are: (a) the converters must have the same nominal regulated output voltage; and (b) provisions must be provided in each voltage regulator circuit to cause the converters to share load current.

The converter load division method is adaptable to a wide range of converter output voltages and currents and can be designed to give any desired load division accuracy. Any number of converters can be operated in parallel with this method.

APPENDIX A

The Effect of Incremental Changes in the Internal Voltage Source Magnitude and Phase on the Phasor Components of the Differential Current in Parallel Voltage Source Systems

Consider the circuit of figure 24 which represents a voltage source, $\dot{E}_1$, with an internal impedance, $\dot{Z}_1$, in parallel with similar units. In general, there are two basic modes of steady-state operation of this system of N paralleled units.

First Mode. - Called equal load division. In this mode the total load ($\dot{I}_{Lp}$) is divided equally among the N units. The subscript o will be used to identify quantities for this mode of operation, since the quantity would be equal for all units.

Second Mode. - Called unequal load division. In this mode the N units are assumed to be supplying the same total load at the same terminal voltage as in the first mode, but now the load is assumed not to be divided equally among the units. The subscript 1 will be used to refer to unit number 1 quantities, subscript 2 for unit number 2 quantities, and so forth.

A phasor diagram showing the quantities used in the following derivation is given in figure 25.

For the first mode of operation, taking V_o as reference phasor, the equations for the various quantities become:

$$\dot{V}_o = V_o \angle o^o; \quad v_o = \sqrt{2}\, V_o \sin(\omega t + o) \tag{A1}$$

$$\dot{I}_o = \frac{\dot{I}_{Lp}}{N} = \frac{1}{N}\frac{\dot{V}_o}{\dot{Z}_{Lp}} = \frac{V_o}{NZ_{Lp}} \angle -\Psi \tag{A2}$$

$$i_o = \frac{\sqrt{2}}{N}\frac{V_o}{\dot{Z}_{Lp}} \sin(\omega t - \Psi), \text{ where } \Psi \text{ is the total power factor angle.} \tag{A3}$$

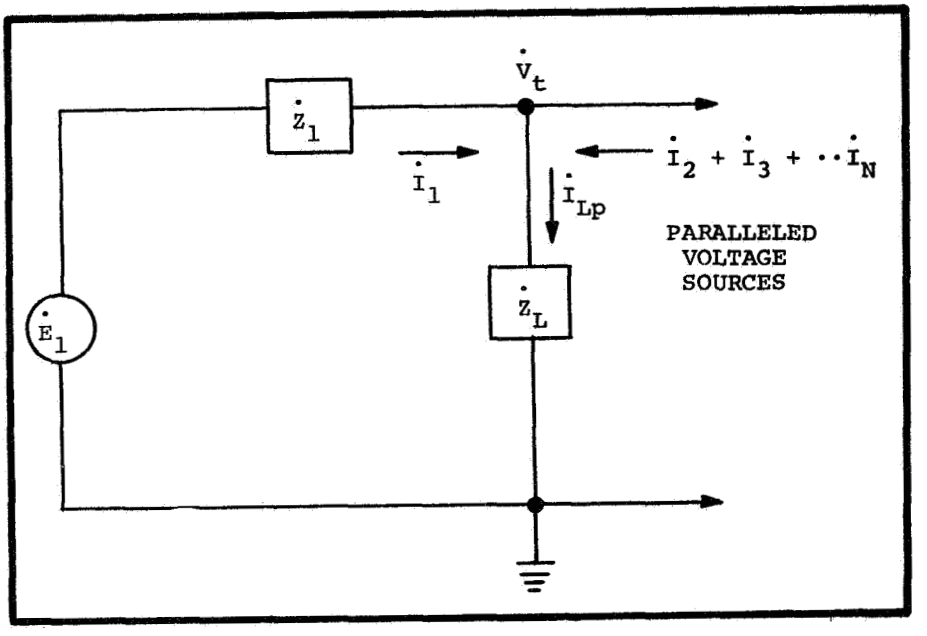


Figure 24. - Equivalent Circuit of Voltage Source System

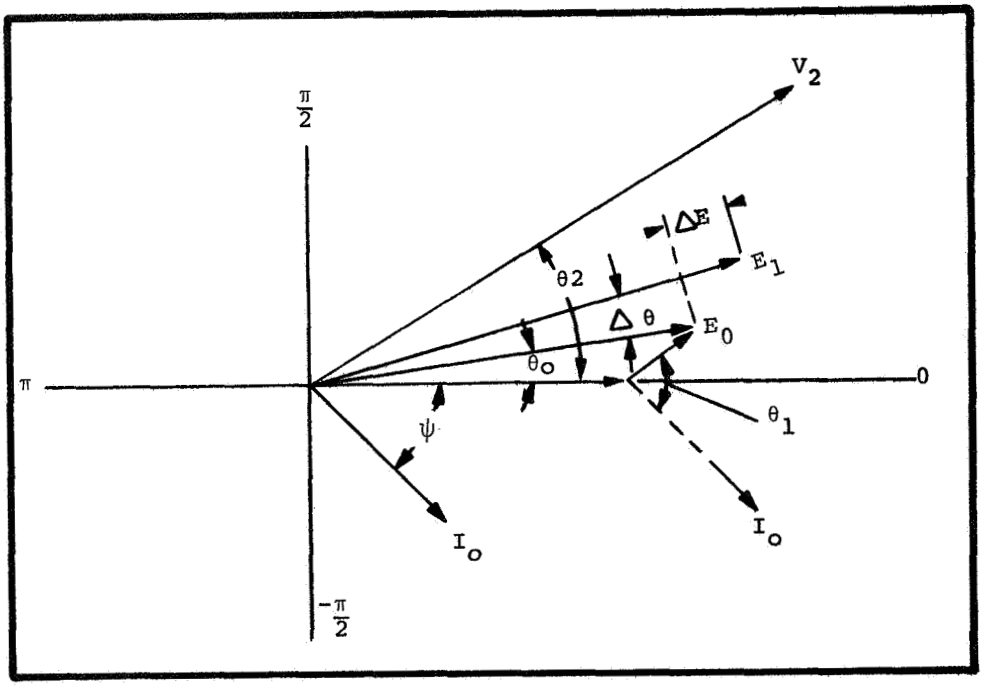


Figure 25. - Phasor Diagram Showing Quantities and Parameters Used in Appendix A Derivation

The general mode equation for figure 25 is:

$$\frac{\dot{E}_1 - \dot{V}_t}{\dot{Z}_1} = \dot{I}_1 \tag{A4}$$

For the first mode type of operation,

$\dot{I}_1 = \dot{I}_o$; $\dot{E}_1 = \dot{E}_o$ and $V_t = V_o$ therefore,

$$\frac{\dot{E}_o - \dot{V}_o}{\dot{Z}_1} = \dot{I}_o; \quad \dot{E}_o - \dot{V}_o = \dot{I}_o\dot{Z}_1 \tag{A5}$$

Substitute Equation (A3) into equation (A5)

$$e_o - v_o = \frac{\sqrt{2}}{N} \frac{V_o Z_1}{Z_{Lp}} \sin(\omega t - \Psi + \theta_1), \tag{A6}$$

$$e_o = \frac{\sqrt{2}}{N} \frac{V_o Z_1}{Z_{Lp}} \sin(\omega t - \Psi + \theta_1) + \sqrt{2}\, V_o \sin(\omega t), \tag{A7}$$

where θ is the phase angle of the internal impedance.

Using trig. formula for expansion of sine of sum of two angles:

$$e_o = \frac{\sqrt{2} V_o Z_1}{N Z_{Lp}} \cos(\theta_1 - \Psi) \sin \omega t + \frac{\sqrt{2}}{N} \frac{V_o Z_1}{Z_{Lp}} \sin(\theta_1 - \Psi) \times \cos \omega t + \sqrt{2}\, V_o \sin \omega t \tag{A8}$$

Collecting sin ωt and cos ωt terms:

$$e_o = \sqrt{2}\, V_o \frac{Z_1}{NZ_{Lp}} \cos(\theta_1 - \Psi) + 1 \sin \omega t + \sqrt{2}\, V_o \frac{Z_1}{NZ_{IP}} \sin(\theta_1 - \Psi) \cos \omega t \tag{A9}$$

But

$$e_o = \sqrt{2}\, E_o \sin(\omega t + \theta_o), \text{ where } \theta_o \text{ is the angle} \qquad (A10)$$

between the internal voltage, E_o, and the terminal voltage, V_o.

Or

$$e_o = \sqrt{2}\, E_o \cos\theta_o \sin\omega t + \sqrt{2}\, E_o \sin\theta_o \cos\omega t \qquad (A11)$$

Comparing Equations (A9) and (A11), the following results:

$$\sqrt{2}\, E_o \cos\theta_o = \sqrt{2}\, V_o \left[\frac{Z_1}{NZ_{Lp}} \cos(\theta_1 - \Psi) + 1 \right], \qquad (A12)$$

$$\sqrt{2}\, E_o \sin\theta_o = \sqrt{2}\, V_o \frac{Z_1}{NZ_{Lp}} \sin(\theta_1 - \Psi). \qquad (A13)$$

Therefore,

$$\tan\theta_o = \frac{\frac{Z_1}{NZ_{Lp}} \sin(\theta_1 - \Psi)}{1 + \frac{Z_1}{NZ_{Lp}} \cos(\theta_1 - \Psi)} \qquad (A14)$$

For the second mode type of operation, let $\dot{E}_1$ differ from $\dot{E}_o$ in the following manner:

$$e_1 = \sqrt{2}\, (E_o + \Delta E) \sin(\omega t + \theta_o + \Delta\theta). \qquad (A15)$$

Let us require $\dot{V}_t$ for the unbalanced condition be the same as $\dot{V}_o$ and substract equation (A5) from equation (A4):

$$\dot{I}_1 - \dot{I}_o = \frac{\dot{E}_1 - \dot{E}_o}{\dot{Z}_1}, \qquad (A16)$$

$$(i_1 - i_o) = \frac{\sqrt{2}\, (E_o + \Delta E)}{Z_1} \sin(\omega t + \theta_o + \Delta\theta - \theta_1) - \frac{\sqrt{2} E_o}{Z_1} \sin(\omega t + \theta_o - \theta_1) \qquad (A17)$$

Expanding the sine of the sum of two angles:

$$(i_1 - i_o) = \frac{\sqrt{2}(E_o + \Delta E)}{Z_1} \cos \Delta\theta \sin (\omega t + \theta_o - \theta_1) - \frac{\sqrt{2}E_o}{Z_1} \tag{A18}$$

$$\text{x } \sin (\omega t + \theta_o - \theta_1) + \frac{\sqrt{2}(E_o + \Delta E)}{Z_1} \sin \Delta\theta \cos (\omega t + \theta_o - \theta_1).$$

Combining terms and then expanding $\sin (\omega t + \theta_o - \theta_1)$ and $\cos (\omega t + \theta_o - \theta_1)$:

$$(i_1 - i_o) = \left[\frac{\sqrt{2}(E_o + \Delta E)}{Z_1} \cos \Delta\theta - \frac{\sqrt{2}E_o}{Z_1} \right] \cos (\theta_o - \theta_1) \sin \omega t$$

$$+ \left[\frac{\sqrt{2}(E_o + \Delta E)}{Z_1} \cos \Delta\theta - \frac{\sqrt{2}E_o}{Z_1} \right] \sin (\theta_o - \theta_1) \cos \omega t$$

$$+ \left[\frac{\sqrt{2}\ (E_o + \Delta E)}{Z_1} \sin \Delta\theta \right] \cos (\theta_o - \theta_1) \cos \omega t$$

$$- \left[\frac{\sqrt{2}(E_o + \Delta E)}{Z_1} \sin \Delta\theta \right] \sin (\theta_o - \theta_1) \sin \omega t \tag{A19}$$

Collecting sin (ωt) and cos (ωt) terms

$$(i_1 - i_o) = \left[\left(\frac{\sqrt{2}(E_o + \Delta E)}{Z_1} \cos \Delta\theta - \frac{\sqrt{2}E_o}{Z_1} \right) \cos (\theta_o - \theta_1) \right.$$

$$\left. - \frac{\sqrt{2}(E_o + \Delta E)}{Z_1} \sin \Delta\theta \sin (\theta_o - \theta_1) \right] \sin \omega t$$

$$+ \left[\left(\frac{\sqrt{2}(E_o + \Delta E)}{Z_1} \cos \Delta\theta - \frac{\sqrt{2}E_o}{Z_1} \sin (\theta_o - \theta_1) \right) \right. \tag{A20}$$

$$+ \frac{\sqrt{2}(E_o + \Delta E)}{Z_1} \sin \Delta\theta \cos (\theta_o - \theta_1) \Big] \cos \omega t. \qquad \text{(A20) Cont.}$$

Since the terminal (bus) voltage was taken as the reference, the coefficient of the sin (ωt) term in equation (A20) will be the real component of ($i_1 - i_o$) (component in phase with bus voltage) and the coefficient of the cos (ωt) term in equation (A20) will be the reactive component of ($i - i_a$) (component at right angles to bus voltages).

Therefore:

$$R(\dot{I}_1 - \dot{I}_o) = \left(\frac{(E_o + \Delta E)}{Z_1} \cos \Delta\theta - \frac{E_o}{Z_1} \right) \cos (\theta_o - \theta_1)$$

$$- \frac{(E_o + \Delta E)}{Z_1} \sin \Delta\theta \sin (\theta_o - \theta_1) \qquad \text{(A21)}$$

$$Q(\dot{I}_1 - I_o) = \left(\frac{(E_o + \Delta E)}{Z_1} \cos \Delta\theta - \frac{E_o}{Z_1} \right) \sin (\theta_o - \theta_1)$$

$$+ \frac{(E_o + \Delta E)}{Z_1} \sin \Delta\theta \cos (\theta_o - \theta_1). \qquad \text{(A22)}$$

If $\Delta\theta$ and ΔE are very small:

$$\cos \Delta\theta = 1; \ \sin \Delta\theta = \Delta\theta \text{ radians}; \ (E_o + \Delta E) \cong E_o.$$

Then equations (A21) and (A22) become:

$$R(\dot{I}_1 - \dot{I}_o) \cong \frac{\Delta E}{Z_1} \cos (\theta_o - \theta_1) - \frac{E \Delta\theta}{Z_1} \sin (\theta_o - \theta_1), \qquad \text{(A23)}$$

$$Q(\dot{I}_1 - \dot{I}_o) \cong \frac{\Delta E}{Z_1} \sin (\theta_o - \theta_1) + \frac{E_o \Delta\theta}{Z_1} \cos (\theta_o - \theta_1). \qquad \text{(A24)}$$

It is desirable to have equations of the components $(\dot{I}_1 - \dot{I}_o)$ with respect to a phasor other than the terminal voltage of the

phase in which current is being sensed. Therefore, consider equation (A18) once more. It could be written as follows, where θ_2 is any angle:

$$(i_1 - i_o) = \frac{\sqrt{2}(E_o + \Delta E)}{Z_1} \cos \Delta\theta \sin [\omega t + \theta_2 + (\theta_o - \theta_1 - \theta_2)] - \frac{\sqrt{2}E_o}{Z_1} \sin [\omega t + \theta_2 + (\theta_o - \theta_1 - \theta_2)] \quad \text{(A18a)}$$

$$+ \frac{\sqrt{2}(E_o + \Delta E)}{Z_1} \sin \Delta\theta \cos [\omega t + \theta_2 + (\theta_o - \theta_1 - \theta_2)]$$

Combining terms and then expanding $\sin [\omega t + \theta_2 + (\theta_o - \theta_1 - \theta_2)]$ and $\cos [\omega t + \theta_2 + (\theta_o - \theta_1 - \theta_2)]$:

$$(i_1 - i_o) = \left[\frac{\sqrt{2}(E_o + \Delta E)}{Z_1} \cos \Delta\theta - \frac{\sqrt{2}E_o}{Z_1}\right] \cos (\theta_o - \theta_1 - \theta_2) \sin (\omega t + \theta_2) \quad \text{(A19a)}$$

$$+ \left[\frac{\sqrt{2}(E_o + \Delta E)}{Z_1} \cos \Delta\theta - \frac{\sqrt{2}E_o}{Z_1}\right] \sin (\theta_o - \theta_1 - \theta_2) \cos (\omega t + \theta_2)$$

$$+ \frac{\sqrt{2}(E_o + \Delta E)}{Z_1} \sin \Delta\theta \cos (\theta_o - \theta_1 - \theta_2) \cos (\omega t + \theta_2)$$

$$- \frac{\sqrt{2}(E_o + \Delta E)}{Z_1} \sin \Delta\theta \sin (\theta_o - \theta_1 - \theta_2) \sin (\omega t + \theta_2)$$

Collecting $\sin (\omega t + \theta_2)$ and $\cos (\omega t + \theta_2)$ terms:

$$(i_1 - i_o) = \left[\left(\frac{\sqrt{2}(E_o + \Delta E_o)}{Z_1} \cos \Delta\theta - \frac{\sqrt{2}E_o}{Z_1}\right)\cos (\theta_o - \theta_1 - \theta_2) - \left(\frac{\sqrt{2}(E_o + \Delta E)}{Z_1} \sin \Delta\theta\right) \sin (\theta_o - \theta_1 - \theta_2)\right] \sin (\omega t + \theta_2) \quad \text{(A20a)}$$

$$+\left[\left(\frac{\sqrt{2}(E_o + \Delta E)}{Z_1}\cos\Delta\theta - \frac{\sqrt{2}E_o}{Z_1}\right)\sin(\theta_0 - \theta_1 - \theta_2)\right.$$

$$\left.+\frac{\sqrt{2}(E_o + \Delta E)}{Z_1}\sin\Delta\theta\cos(\theta_o - \theta_1 - \theta_2)\right]$$

$$\cos(\omega t + \theta_2) \qquad \text{(A20a) Cont.}$$

Since the terminal voltage (line-to-neutral voltage of the phase in which differential current is measured) was taken as reference, the coefficient of the sin $(\omega t + \theta_2)$ term in equation (A20a) is the component of $(i - i_o)$ in phase with a phasor θ_2 degrees ahead of the terminal voltage and the coefficient of the cos $(\omega t + \theta_2)$ term in equation (A20a) is the component of $(i - i_o)$ at right angles with a phasor θ_2 degrees ahead of the terminal voltage.

Therefore:

$$R_{\theta_2}(\dot{I}_1 - \dot{I}_o) \cong \frac{\Delta E}{Z_1}\cos(\theta_o - \theta_1 - \theta_2) - \frac{E\Delta\theta}{Z_1}\sin(\theta_o - \theta_1 - \theta_2) \qquad \text{(A23d)}$$

$$Q_{\theta_2}(\dot{I}_1 - \dot{I}_o) \cong \frac{\Delta E}{Z_1}\sin(\theta_o - \theta_1 - \theta_2) + \frac{E\Delta\theta}{Z_1}\cos(\theta_o - \theta_1 - \theta_2) \qquad \text{(A24d)}$$

APPENDIX B

The Effect of Voltage Regulator Adjustments on the Steady-State Unbalance of Load Currents in a System of Parallel Connected Voltage Sources

Consider an inverter (or alternator or other voltage source) that is operating open loop. That is, the voltage regulator sensing circuit is not connected to the output bus, but is connected to a separate voltage source, V_s. In like manner, the reactive load-division current transformer (or any other sensing device that might be used) is operated open loop and is connected to a separate supply.

With the voltage applied to the voltage regulator sensing circuit (V_s) equal to V_o volts, let the regulator setting be such that the terminal voltage (V_t) is also equal to V_o volts. (A load of Z_L ohms assumed connected to the output.) Let us denote this regulator setting as R_{so} and the resulting value of the internal voltage as E_o. (No signal applied to reactive load division circuit.)

Any change in V_s from V_o will now result in E changing from the value of E_o. Any change in the R_s setting from R_{so} will also result in E changing from E_o. Also, if a signal is applied to the reactive load circuit, E will change from E_o. If all these changes occur at the same time, the net change in E will be equal to the algebraic sum of the changes due to each cause acting independently. If we denote the quantity $(E-E_o)$ as ΔE, the quantity (V_s-V_o) as ΔV_s; the quantity (R_s-R_{so}) as ΔR_s, and the differential quadrature component of current as ΔI_Q, we can express this mathematically as:

$$\Delta E = \frac{\partial E}{\partial V_s} \Delta V_s + \frac{\partial E}{\partial R_s} \Delta R_s + \frac{\partial E}{\partial I_{DQ}} \Delta I_Q \qquad \text{(B1)}$$

The quantities $\frac{\partial E}{\partial V_s}$, $\frac{\partial E}{\partial R_s}$, $\frac{\partial E}{\partial I_{DQ}}$ denote the corresponding control circuit open loop gains. How these gains are achieved--that is,

what circuitry is used--is of no concern in the development of the relationship that follows. These relationships are of a general nature and hold for a variety of regulating methods.

For closed-loop operation ($V_s = V_t$) of a loaded single-unit system and regulator setting R_s different from R_{so}, equation (B1) becomes:

$$(E_{1L} - E_o) = \frac{\partial E}{\partial V_s} (V_{1L} - V_o) + \frac{\partial E}{\partial R_s} (R_s - R_{so} \qquad \text{(B2)}$$

where E_{1L} and V_{1L} denote the value of the quantities E and $V_t = V_s$, for regulator as set and operating as a single-unit system.

But for a fixed load on a single-unit system the following is a general relationship:

$$V_t = \left[\frac{Z_L}{|Z_1 + Z_L|} \right] E_1 = KE_1 \qquad \text{(B3)}$$

where V_t is the terminal voltage and E_1 is the internal voltage for any particular set of conditions. Therefore $V_o = KE_o$ and $V_{1L} = KE_{1L}$ and

$$V_{1L} - V_o = KE_{1L} - KE_o = K\,[E_{1L} - E_o], \qquad \text{(B4)}$$

and equation (B2) becomes:

$$(E_{1L} - E_o) \left[1 - K \frac{\partial E}{\partial V_s} \right] = \frac{\partial E}{\partial R_s} (R_s - R_{so}). \qquad \text{(B5)}$$

Now let us further require that the V_o, E_o, and R_{so} values of V_s, E, and R_s, used above be the necessary values of V_s, E, and R_s for the unit to operate in a parallel system with zero differential current.

For parallel operation under closed-loop control $V_s = V_{pL}$ = bus voltage of loaded parallel system and equation (B1) becomes:

$$(E_{pL} - E_o) = \frac{\partial E}{\partial V_s} (V_{pL} - V_o) + \frac{\partial E}{\partial R_s} (R_s - R_{so}) + \frac{\partial E}{\partial I_{DQ}} \Delta I_Q \qquad \text{(B6)}$$

Substituting equation (B5) into (B6) we have:

$$(E_{pL} - E_o) = \frac{\partial E}{\partial V_s}(V_{pL} - V_o) + (E_{1L} - E_o)\left[1 - K\frac{\partial E}{\partial V_s}\right] + \frac{\partial E}{\partial I_{DQ}}\Delta I_Q \tag{B7}$$

or

$$(E_{pL} - E_o) = (V_{pL} - V_o - KE_{1L} + KE_o)\frac{\partial E}{\partial V_s} + (E_{1L} - E_o) + \frac{\partial E}{\partial I_{DQ}}\Delta I_Q \tag{B8}$$

or

$$(E_{pL} - E_o) = (V_{pL} - V_{1L})\frac{\partial E}{\partial V_s} + -(V_{1L} - V_o) + \frac{\partial E}{\partial I_{DQ}}\Delta I_Q \tag{B9}$$

If the bus voltage of the loaded parallel system is the same for Mode One type operation (equal load division) as for the Mode type operation (unequal load division), $V_{pL} = V_o$ we could then express equation (B9) as:

$$E = (E_{pL} - E_o) = \left[\frac{1}{K} - \frac{\partial E}{\partial V_s}\right](V_{1L} - V_{pL}) + \frac{\partial E}{\partial I_{DQ}}\Delta I_Q \tag{B9a}$$

Equation (B9) and/or (B9a) related single-unit operation to parallel-system operation. The voltage regulator circuit gain, $\frac{\partial E}{\partial V_s}$, is a function of the single-unit operation voltage regulation requirements. If the internal impedance is known the necessary value of $\frac{\partial E}{\partial V_s}$ can be calculated from the voltage regulation specifications. V_{1L} depends on how close each unit (operating independently as a single unit system) can be expected to regulate to the same voltage. In fact if all units regulated to exactly the same voltage under all loading conditions, there would be no need for a load division circuit when the units are operated in parallel. The value of V_{1L} to be used in equation (B9) and/or (B9a) is taken equal to the regulated voltage of the unit that, for any allowable reason, regulates farthest from nominal voltage of the specification for V_{pL}.

In appendix A, equation (A24d) relates ΔE, ΔI_Q, and Z_1. If

the maximum allowable value of ΔI_Q is specified and Z_1 is known, the required value of $\frac{\partial E}{\partial I_{DQ}}$ can be calculated using equation (A24d) and equation (B9a). A method for calculating Z_1 is given in appendix E. An example of the calculations suggested above is given in appendix D.

APPENDIX C

Method of Calculating Balanced Load Internal Impedance of a Four-Power-Stage Three-Phase Static Inverter

When first presented, the problem of determining analytically the internal impedance of a static inverter which used a harmonic interchange transformer connection appeared to require the solution of a very large number of long simultaneous equations if any degree of rigor was to be required.

It was felt that a digital computer program would be required to aid in the investigation of the relative importance of various parameters as to internal impedance. It was hoped that, as insight into the problem was then gained, a slightly less complicated method of calculation could be developed lending itself to hand calculations.

For several reasons, it was decided to use a modification of a digital computer program already in existence for an inverter other than the subject NASA inverter: (1) there was a definite time limit; (2) many of the needed constants were already available for this other inverter; (3) actual test information was also available for this inverter; (4) there was even the possibility of experimentally checking some of the analytical results that one would obtain. All of these considerations pointed to using a study of this other inverter to gain insight into the problem rather than starting from scratch and developing a computer program for a different inverter.

As insight and experience were gained on the internal impedance problem, a method was devised to calculate the "balanced condition" internal impedance without the aid of a digital computer. The development of this method is presented in this appendix.

The schematic diagram of the particular output transformer to be used in the test model inverters is given in figure 26. The equation derived in this section gives the impedance looking into the terminals of Phase 1. Equation (C40) can be applied to inverters with any number of power stages although the derivation is based on a four-power-stage inverter. The following assumptions and definitions are an essential part of this derivation.

(1) Let the subscript p refer to 1/2 the primary winding of any power stage (all power stages primary windings assumed the same).

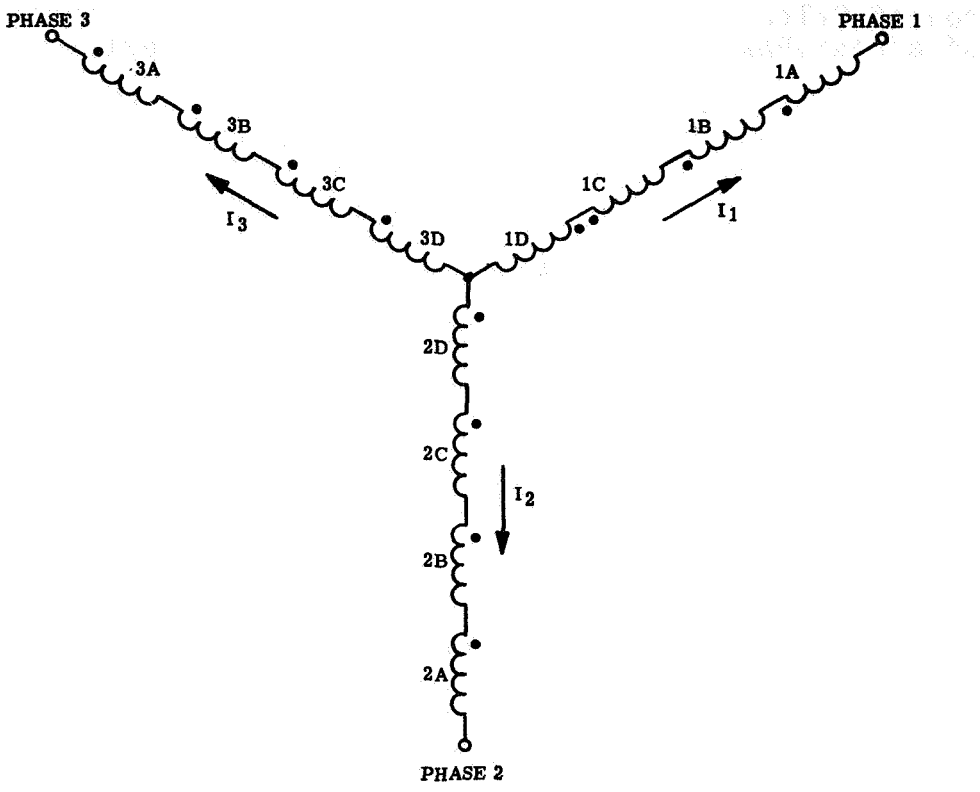


Figure 26. Schematic Diagram of Output Transformer Secondary Connections

(2) Let all the secondary windings of the power stages in Phase 1 be designated winding #1 for that stage.

(3) Let all the secondary windings of the power stages that are in Phase 2 be designated winding #2 for that stage.

(4) Let all the secondary windings of the power stages that are in Phase 3 be designated winding #3 for that stage.

(5) Let all number of turns of a winding be expressed in pu, based on 1/2 the primary winding of power stage as base value.

(6) Let L_{pp}, L_{11}, L_{22}, etc., be defined in the following manner. The voltage drop jwI_p (L_{pp}) is the voltage induced in

winding p by that part of the flux, due to I_p, which lies entirely or partially outside the iron core (core-self-leakage inductance of winding p). In the work that follows, assume that all constants and voltages are referred to 1/2 the primary winding and expressed in inverter per unit (pu). The secondary currents (phase currents I_1, I_2, I_3) are in pu not referred to primary.

(7) Let L_{p1}, L_{12}, L_{23}, etc., be defined in the following manner. The quantity $w(L_{p1})$ is the core-mutual-leakage reactance of winding p with respect to winding 1 or of winding 1 with respect to winding p. It differs from the mutual reactance between winding p and 1 by being caused by only that portion of the mutual flux of those two windings that does not lie entirely within the core.

(8) Define a true leakage reactance of winding p with respect to winding 1 ($wL_{p(1)}$) as follows. This true leakage reactance of one winding with respect to another is the reactance used in the treatment of the conventional two-winding transformer. The true leakage reactance of winding p with respect to winding 1 is caused by that part of the flux, due to I_p, which <u>does not link winding 1</u>. It may produce linkage with windings 2 or 3 or with other windings if there are more than four. Thus,

$$w\,L_{p(1)} = wL_{pp} - wL_{p1}$$

Refer to figure 27. To clarify the definitions (6,7, and 8) pertaining to leakage reactances, this sketch shows some typical leakage flux paths in a three-winding transformer when only the primary winding, p, conducts current. Solid-line flux links winding p only. Long-dash-short-dash-line flux links winding p and winding 1. Dashed-line flux links all three windings.

The flux that is associated with the core-self-leakage reactance L_{pp} would be the sum of the three types of leakage flux illustrated. (Solid line + [long-dash-short-dash line] + short dash line.)

The flux that is associated with the core-mutual-leakage reactance of winding p with respect to winding 1, L_{p1}, would be the sum of the fluxes illustrated by the long-dash-short-dash lines and the short-dash lines.

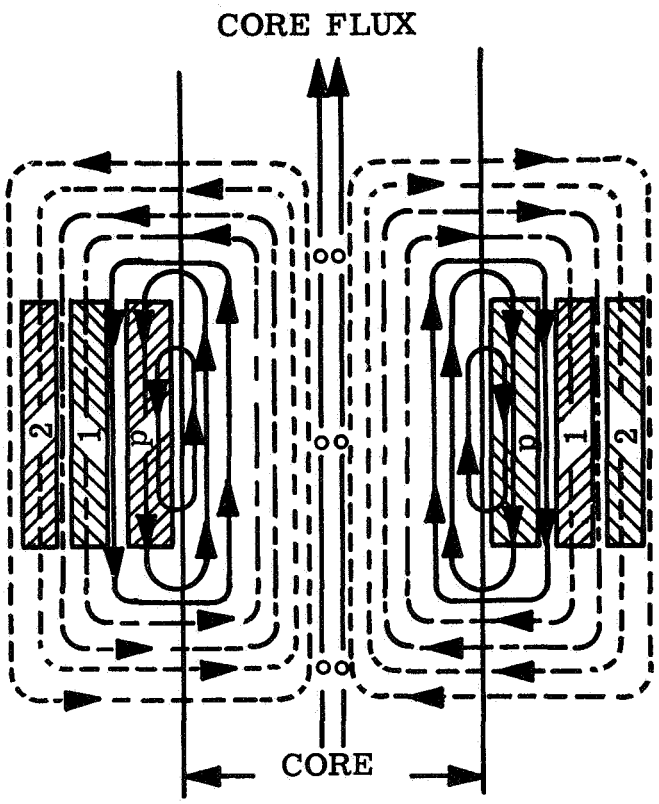


Figure 27. Flux Due to Current in Winding p of a Three-Winding Transformer

The flux associated with the core-mutual-leakage reactance of winding p with respect to winding 2, L_{p2}, would be illustrated by the short-dash lines only.

The flux associated with the true leakage reactance of winding p with respect to winding 1, $L_{p(1)}$, would be illustrated by the solid lines only.

The flux associated with the true leakage reactance of winding p with respect to winding 2, $L_{p(2)}$, would be the sum of the fluxes illustrated by solid lines and the long-dash-short-dash lines.

(9) Define the sum $\sum_{S21} (N_2)\ (N_1)\ (wL_{2(p)} - wL_{2(1)})$ as the arithmetic sum of the leakage reactances for all power stages that have secondary windings in both Phase 2 and Phase 1, the sign of the term to be considered positive if the assumed directions for the phase currents both enter the dot terminals or both leave the dot terminals of the particular secondary windings. In the work to follow, all three-phase currents are assumed to flow out from neutral point when they are positive.*

(10) Define the sum $\sum_{S31} (N_3)\ (N_1)\ (wL_{3(p)} - wL_{3(1)})$ similar to (9) above except for all power stages that have secondary windings in both Phase 3 and Phase 1.

(11) Define the sum $\sum_{S1} (N_1)^2\ (R_{11} + jwL_{1(p)})$ as the sum of the impedances of all the secondary windings connected in series in Phase 1. All terms are taken to be positive.

(12) T.R. - transformer ratio. This is the ratio of transformer open-circuit, secondary Phase 1 voltage to the fundamental rms primary applied voltage of the power stage assumed to be excited first. Therefore, it is a phasor quantity. It can be calculated as:

$$\dot{T.R.} = \sum_{S1} \dot{N}_1 = |\dot{T.R.}|\ \angle\theta_R,$$

where the number of turns, N, (in pu) are considered phasors. The phasor angle 0° is assigned to that stage whose primary is assumed to be excited positive first. Each succeeding stage (in order of excitation) has its assigned phasor angle $\frac{180°}{NS}$ less than previous excited stage. NS = total number of power stages. The sign before a term is taken positive if the assumed Phase 1 current flows out of the dot terminal of the corresponding secondary winding. Figure 28 shows a phasor plot for phase one of the transformer connections shown in figure 27.

(13) Define sum $\sum_{S1} (\dot{N}_1)\ (R_p + jwL_{p(1)})$ as the phasor sum of the products of primary impedance times pu phasor turns of the winding of that stage in Phase 1. The angles assigned to the turns and the sign before each term is the same as in (12) preceding.

* N's are in pu and L's are referred to p and are in pu.

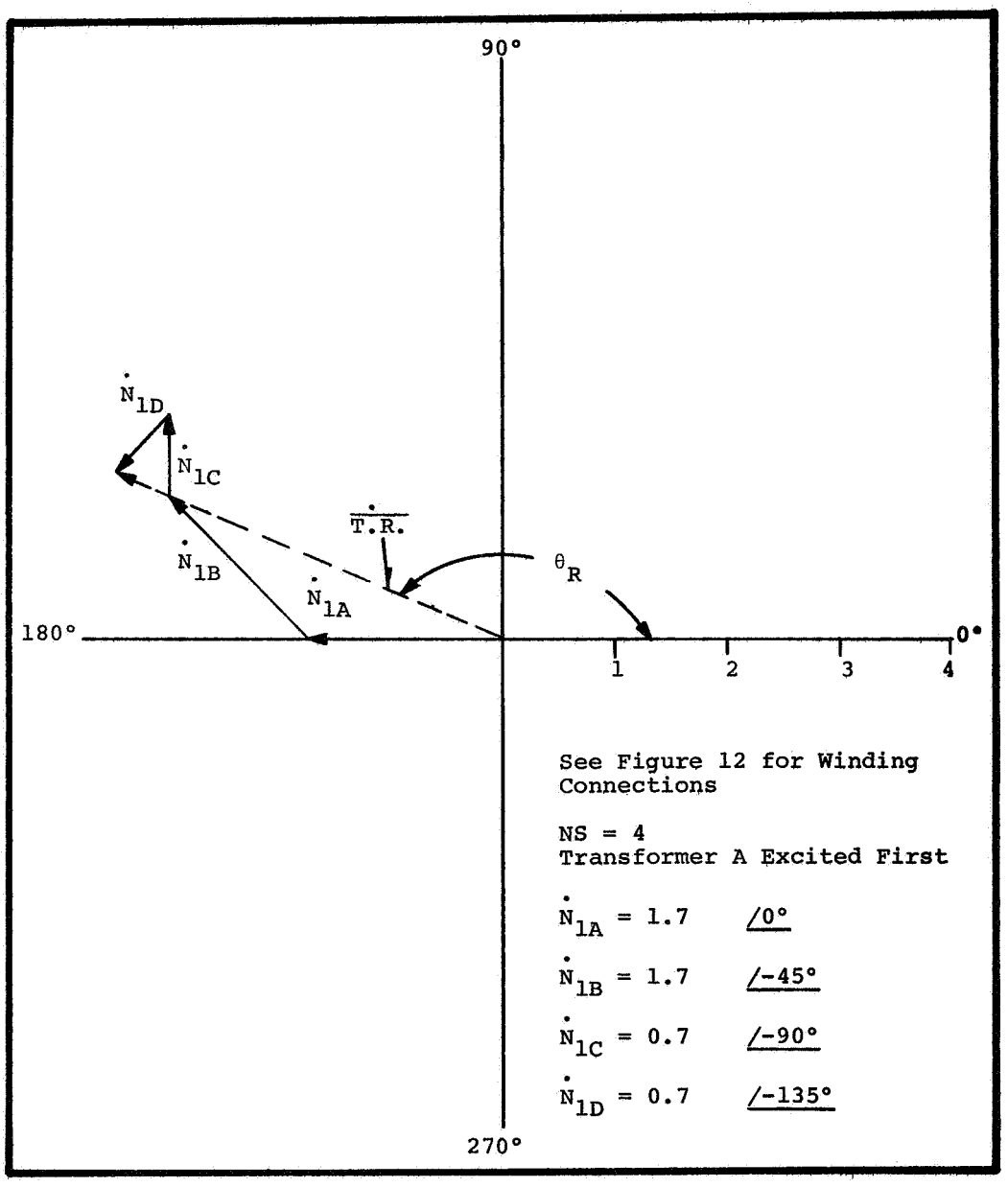


Figure 28. - Phasor Diagram for Phase On $\overline{\dot{T.R.}}$

Four fundamental equations can be written for each of the power stage transformers, shown in figure 29 in terms of core-self-leakage inductance and core-mutual-leakage inductance, as follows:

$$\dot{E}_{pA} = \dot{I}_{pA}\,(R_{pA} + jwL_{ppA}) + \dot{I}_1\,(N_{1A})\,jwL_{1pA} - \dot{I}_2(N_{2A})\,jwL_{2pA} - \dot{I}_3\,(N_{3A})\,jwL_{3pA} + \dot{E}_{CA} \qquad (C1)$$

$$\dot{E}_{1A} = \dot{I}_{pA}jwL_{p1A} + \dot{I}_1(N_{1A})(R_{11A} + jwL_{11A}) - \dot{I}_2(N_{2A})\,jwL_{21A} - \dot{I}_3\,(N_{3A})\,jwL_{31A} + \dot{E}_{CA} \qquad (C2)$$

$$\dot{E}_{2A} = \dot{I}_{pA}jwL_{p2A} + \dot{I}_1(N_{1A})jwL_{12A} - \dot{I}_2\,(N_{2A})(R_{22A} + jwL_{22A}) - \dot{I}_3\,(N_{3A})jwL_{32A} + \dot{E}_{CA} \qquad (C3)$$

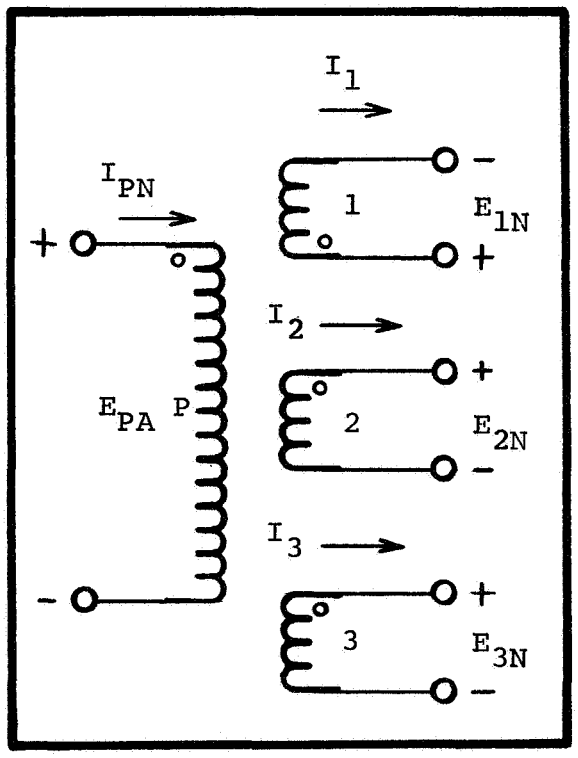


Figure 29. Schematic Diagram of Transformer Winding on Leg N, Where N is A, B, C, or D

$$\dot{E}_{3A} = \dot{I}_{pA} jwL_{p3A} + \dot{I}_1 (N_{1A}) jwL_{13A} - \dot{I}_2 (N_{2A}) jwL_{23A} - \dot{I}_3 (N_{3A}) (R_{33A} + jwL_{33A}) + \dot{E}_{CA} \quad \text{(C4)}$$

$$\dot{E}_{pB} = \dot{I}_{pB} (R_{pB} + jwL_{ppB}) + \dot{I}_1 (N_{1B}) jwL_{1pB} - \dot{I}_2 (N_{2B}) jwL_{2pB} - \dot{I}_3 (N_{3B}) jwL_{3pB} + \dot{E}_{CB} \quad \text{(C5)}$$

$$\dot{E}_{1B} = \dot{I}_{pB} jwL_{p1B} + \dot{I}_1 (N_{1B}) (R_{11B} + jwL_{11B}) - \dot{I}_2 (N_{2B}) jwL_{21B} - \dot{I}_3 (N_{3B}) jwL_{31B} + \dot{E}_{CB} \quad \text{(C6)}$$

$$\dot{E}_{2B} = \dot{I}_{pB} jwL_{p2B} + \dot{I}_1 (N_{1B}) jwL_{12B} - \dot{I}_2 (N_{2B}) (R_{22B} + jwL_{22B}) - \dot{I}_3 (N_{3B}) jwL_{32B} + \dot{E}_{CB} \quad \text{(C7)}$$

$$\dot{E}_{3B} = \dot{I}_{pB} jwL_{p3B} + \dot{I}_1 (N_{1B}) jwL_{13B} - \dot{I}_2 (N_{2B}) jwL_{23B} - \dot{I}_3 (N_{3B}) (R_{33B} + jwL_{33B}) + \dot{E}_{CB} \quad \text{(C8)}$$

$$\dot{E}_{pC} = \dot{I}_{pC} (R_{pC} + jwL_{ppC}) + \dot{I}_1 (N_{1C}) jwL_{1pC} + \dot{I}_2 (N_{2C}) jwL_{2pC} - \dot{I}_3 (N_{3C}) jwL_{3pC} + \dot{E}_{CC} \quad \text{(C9)}$$

$$\dot{E}_{1C} = \dot{I}_{pC} jwL_{p1C} + \dot{I}_1 (N_{1C}) (R_{11C} + jwL_{11C}) + \dot{I}_2 (N_{2C}) jwL_{21C} - \dot{I}_3 (N_{3C}) jwL_{31C} + \dot{E}_{CC} \quad \text{(C10)}$$

$$\dot{E}_{2C} = \dot{I}_{pC} jwL_{p2C} + \dot{I}_1 (N_{1C}) jwL_{12C} + \dot{I}_2 (N_{2C}) (R_{22C} + jwL_{22C}) - \dot{I}_3 (N_{3C}) jwL_{32C} + \dot{E}_{CC} \quad \text{(C11)}$$

$$\dot{E}_{3C} = \dot{I}_{pC} jwL_{p3C} + \dot{I}_1 (N_{1C}) jwL_{13C} + \dot{I}_2 (N_{2C}) jwL_{23C} - \dot{I}_3 (N_{3C}) (R_{33C} + jwL_{33C}) + \dot{E}_{CC} \quad \text{(C12)}$$

$$\dot{E}_{pD} = \dot{I}_{pD}(R_{pD} + jwL_{ppD}) - \dot{I}_1(N_{1D})jwL_{1pD} + \dot{I}_2(N_{2D})jwL_{2pD} - \dot{I}_3(N_{3D})jwL_{3pD} + \dot{E}_{CD} \quad (C13)$$

$$\dot{E}_{1D} = \dot{I}_{pD}jwL_{p1D} - \dot{I}_1(N_{1D})(R_{11D} + jwL_{11D}) + \dot{I}_2(N_{2D})jwL_{21D} - \dot{I}_3(N_{3D})jwL_{31D} + \dot{E}_{CD} \quad (C14)$$

$$\dot{E}_{2D} = \dot{I}_{pD}jwL_{p2D} - \dot{I}_1(N_{1D})jwL_{12D} + \dot{I}_2(N_{2D})(R_{22D} + jwL_{22D}) - \dot{I}_3(N_{3D})jwL_{32D} + \dot{E}_{CD} \quad (C15)$$

$$\dot{E}_{3D} = \dot{I}_{pD}jwL_{p3D} - \dot{I}_1(N_{1D})jwL_{13D} + \dot{I}_2(N_{2D})jwL_{23D} - \dot{I}_3(N_{3D})(R_{33D} + jwL_{33D}) + \dot{E}_{CD} \quad (C16)$$

The line-to-neutral voltage of phase 1 in figure 27 is:

$$\dot{E}_{LN1} = (N_{1A})\dot{E}_{1A} - (N_{1B})\dot{E}_{1B} - (N_{1C})\dot{E}_{1C} + (N_{1D})\dot{E}_{1D} \quad (C17)$$

However,

$$\begin{aligned}\dot{E}_{pA} - \dot{E}_{1A} &= \text{eq. (C1)} - \text{eq. (C2)} \\ &= \dot{I}_{pA}\,[R_{pA} + jw(L_{ppA} - L_{p1A})] - \dot{I}_1(N_{1A})\,[R_{11A} \\ &\quad + jw(L_{11A} - L_{1pA})] - \dot{I}_2(N_{2A})jw(L_{2pA} = L_{21A}) \\ &\quad - \dot{I}_3(N_{3A})jw(L_{3pA} - L_{31A}) \end{aligned} \quad (C18)$$

or since

$$\begin{aligned}(L_{2pA} - L_{21A}) &= (L_{22A} - L_{21A}) - (L_{22A} - L_{2pA}) \\ &= L_{2(1)A} - L_{2(p)A} \end{aligned} \quad (C19)$$

$$\begin{aligned}(L_{3pA} - L_{31A}) &= (L_{33A} - L_{31A}) - (L_{33A} - L_{3pA}) \\ &= L_{3(1)A} - L_{3(p)A} \end{aligned} \quad (C20)$$

$$\dot{E}_{pA} - \dot{E}_{1A} = \dot{I}_{pA}(R_{pA} + jwL_{p(1)A}) - \dot{I}_1(N_{1A})(R_{11A} + jwL_{1(p)A}) - \dot{I}_2(N_{2A})jw(L_{2(1)A} - L_{2(p)A}) - \dot{I}_3(N_{3A})jw(L_{3(1)A} - L_{3(p)A}) \quad (C21)$$

In a similar manner the following equations result.

$$\dot{E}_{pB} - \dot{E}_{1B} = \dot{I}_{pB}(R_{pB} + jwL_{p(1)B}) - \dot{I}_1(N_{1B})(R_{11B} + jL_{1(p)B}) - \dot{I}_2(N_{2B})jw(L_{2(1)B} - L_{2(p)B}) - \dot{I}_3(N_{3B})jw(L_{3(1)B} - L_{3(p)B}) \quad (C22)$$

$$\dot{E}_{pC} - \dot{E}_{1C} = \dot{I}_{pC}(R_{pC} + jwL_{p(1)C}) - \dot{I}_1(N_{1C})(R_{11C} + jwL_{1(p)C}) + \dot{I}_2(N_{2C})jw(L_{2(1)C} - L_{2(p)C}) - \dot{I}_3(N_{3C})jw(L_{3(1)C} - L_{3(p)C}) \quad (C23)$$

$$\dot{E}_{pD} - \dot{E}_{1D} = \dot{I}_{pD}(R_{pD} + jwL_{p(1)D}) + \dot{I}_1(N_{1D})(R_{11D} + jwL_{1(p)D}) + \dot{I}_2(N_{2D})jw(L_{2(1)D} - L_{2(p)D}) - \dot{I}_3(N_{3D})jw(L_{3(1)D} - L_{3(p)D}) \quad (C24)$$

Substituting (C21), (C22), (C23) and (C24) in (C17), the following results.

$$\begin{aligned}\dot{E}_{LN1} = {} & (N_{1A})\dot{I}_{pA}(R_{pA} + jwL_{p(1)A}) - \dot{I}_1(N_{1A})^2\,[R_{11A} + jwL_{1(p)A}] \\ & - N_{1A}\dot{E}_{pA} - \dot{I}_2(N_{1A})(N_{2A})jw(L_{2(1)A} - L_{2(p)A}) \\ & - \dot{I}_3(N_{1A})(N_{3A})jw(L_{3(1)A} - L_{3(p)A}) \\ & + N_{1B}\dot{I}_{pB}(R_{pB} + jwL_{p(1)B} - \dot{I}_1(n_{1B})^2\,[R_{11B} + jL_{1(p)B}] \\ & - N_{1B}\dot{E}_{pB} - \dot{I}_2(N_{1B})(N_{2B})jw(L_{2(p)B} - L_{2(1)B}) \\ & - \dot{I}_3(N_{1B})(N_{3B})jw(L_{3(1)B} - L_{3(p)B}) \\ & + N_{1C}\dot{I}_{pC}(R_{pC} + jwL_{p(1)C}) - \dot{I}_1(N_{1C})^2\,(R_{11C} + jwL_{1(p)C}) \\ & - N_{1C}\dot{E}_{pC} + \dot{I}_2(N_{1C})(N_{2C})jw(L_{2(1)C} - L_{2(p)C}) \\ & - \dot{I}_3(N_{1C})(N_{3C})jw(L_{3(1)C} - L_{3(p)C}) - N_{1D}\dot{I}_{pD}(R_{pD}\end{aligned} \quad (C25)$$

$$+ jwL_{p(1)D}) - \dot{I}_1(N_{1D})^2(R_{11D} + jwL_{1(p)D})$$
$$+ N_{1D}\dot{E}_{pD} - \dot{I}_2(N_{1D})(N_{2D})jw(L_{2(1)D} - L_{2(p)D})$$
$$+ \dot{I}_3(N_{1D})(N_{3D})jw(L_{3(1)D} - L_{3(p)D}) \quad \text{(C25) Cont.}$$

Equation (C25) can be rearranged to group the terms into five separate catagories:

$$\dot{E}_{LN1} = \left[-N_{1A}\dot{E}_{pA} - N_{1B}\dot{E}_{pB} - N_{1C}\dot{E}_{pC} + N_{1D}\dot{E}_{pD}\right]$$
$$+ (N_{1A})\dot{I}_{pA}(R_{pA} + jwL_{p(1)A}) + (N_{1B})\dot{I}_{pB}(R_{pB} + jwL_{p(1)B})$$
$$+ N_{1C}\dot{I}_{pC}(R_{pC} + jwL_{p(1)C}) - N_{1D}\dot{I}_{pD}(R_{pD} + jwL_{p(1)D})$$
$$- \dot{I}_1\left[(N_{1A})^2[R_{11A} + jwL_{1(p)A}] + (N_{1B})^2[R_{11B} + jwL_{1(p)B}]\right.$$
$$\left. + (N_{1C})^2[R_{11C} + jwL_{1(p)C}] + (N_{1D})^2[R_{11D} + jwL_{1(p)D}]\right]$$
$$- \dot{I}_2\left[(N_{1A})(N_{2A})jw(L_{2(1)A} - L_{2(p)A})\right.$$
$$+ (N_{1B})(N_{2B})jw(L_{2(1)B} - L_{2(p)B}) - (N_{1C})(N_{2C})jw(L_{2(1)C}$$
$$\left. - L_{2(p)C}) + (N_{1D})(N_{2D})jw(L_{2(1)D} - L_{2(p)D})\right]$$
$$- I_3\left[(N_{1A})(N_{3A})jw(L_{3(1)A} - L_{3(p)A})\right.$$
$$+ (N_{1B})(N_{3B})jw(L_{3(1)B} - L_{3(p)B})$$
$$+ (N_{1C})(N_{3C})jw(L_{3(1)C} - L_{3(p)C}) - (N_{1D})(N_{3D})jw(L_{3(1)D}$$
$$\left. - L_{3(p)D})\right] \quad \text{(C26)}$$

Since

$$|\dot{E}_{pA}| = |\dot{E}_{pB}| = |\dot{E}_{pC}| = |\dot{E}_{pD}| \quad \text{(C27)}$$

If

$$\dot{E}_{pA} = |E_{pA}| \angle 0° \quad \text{(C28)}$$

$$\dot{E}_{pB} = |E_{pA}| \angle \frac{-180°}{NS}\ ;\ \dot{E}_{pC} = |E_{pA}| \angle \frac{-360°}{NS};\ \dot{E}_{pD}$$
$$= |E_{pA}| \angle \frac{-540°}{NS} \quad \text{(C29)}$$

The first group of equation (C26) can then be written

$$\left[-N_{1A} \angle 0° \quad -N_{1B} \angle \frac{-180°}{NS} \quad -N_{1C} \angle \frac{-360°}{NS} + N_{1D} \angle \frac{-540°}{NS}\right] |\dot{E}_{pA}|$$

$$= (|\overline{\dot{T.R.}}| \angle \theta_R) |\dot{E}_{pA}| \qquad \text{(C30)}$$

which is the no load (neglecting excitation current) open circuit transformer line-to-neutral voltage of Phase 1.

The second group of terms can be expressed as follows, assuming balanced loads:

$$- \dot{I}_{pA} \sum_{S1} (\dot{N}_1) (R_p + jwL_{p(1)}) \qquad \text{(C31)}$$

Where $\dot{N}_1$ signifies a phasor. The angles of these phasors and the signs are the same as in equation (C30).

The third group of terms can be expressed as follows:

$$- \dot{I}_1 \sum_{S1} (N_1)^2 (R_{11} + jwL_{1(p)}) \qquad \text{(C32)}$$

where all terms of the summation are taken positive.

The fourth group of terms can be expressed as follows:

$$- j\dot{I}_2 \sum_{S21} (N_1)(N_2)w(L_{2(p)} - L_{2(1)}) \qquad \text{(C33)}$$

where the sign of the term in the summation is determined as follows. If the assumed direction for the phase current ($\dot{I}_1$ and $\dot{I}_2$) both enter the dot terminals or both leave the dot terminals of the particular secondary windings under consideration, the sign of the term is taken as positive.

The fifth group of terms can be similarly expressed as follows:

$$- j\dot{I}_3 \sum_{S31} (N_1) (N_3)w(L_{3(p)} - L_{3(1)}) \qquad \text{(C34)}$$

where the sign of a term is determined as in equation (C33).

For balanced loads, the following relationships hold:

$$\dot{I}_2 = \dot{I}_1 \angle -120°; \quad \dot{I}_3 = \dot{I}_1 \angle -240°. \tag{C35}$$

If excitation current is neglected and if primary load current losses are transferred to the secondary, the following fundamental frequency volt-ampere relationship holds:

$$(NS)\,|E_{pa}|I_{pA}| = 3|\dot{E}_{LN1} \text{ (open circuit)}|\dot{I}_1| \tag{C36}$$

or

$$|\dot{I}_{pA}| = \frac{3}{(NS)} \frac{|\overline{T.R.}||\dot{E}_{pA}||\dot{I}_1|}{|\dot{E}_{pA}|} = \frac{3|\overline{T.R.}||I_1|}{(NS)}. \tag{C37}$$

Since the total input power must equal total output power, and the total input reactive power must equal total output reactive power in equation (C36), the phasor angle between E_{LN1} (open circuit) and $\dot{I}_1$ must be the same as the phasor angle between $\dot{E}_{pA}$ and $\dot{I}_{pA}$.

Therefore,

$$\dot{I}_{pA} = \frac{3|\overline{T.R.}|}{NS} \dot{I}_1 \angle -\theta_R . \tag{C38}$$

Substitution of equation (C30) thru (C38) in equation (C26) results in the following expression:

$$\dot{E}_{LN1} = \dot{E}_{LN1} \text{ (open circuit)} - \dot{I}_1 \left[\frac{3|\overline{T.R.}|}{(NS)} \angle -\theta_R \sum_{S1} (\dot{N}_1)(R_p + jwL_{p(1)}) + \sum_{S1} (N_1)^2 (R_{11} + jwL_{1(p)}) + \sum_{S1} (N_1)^2 (R_{11} + jwL_{1(p)}) + \sum_{S21} (N_1)(N_2) w (L_{2(p)} - L_{2(1)}) \angle -30° + \sum_{S31} (N_1)(N_3) w (L_{3(1)}) \angle -150° \right] \tag{C39}$$

The expression inside the bracket in equation (C39) represents the internal impedance of the power transformer (under balanced load).

The impedance looking into the line-to-neutral terminals of Phase 1 is then given by the following expression:

$$Z_{eq} = \frac{3|\dot{T.R.}|}{(NS)}\left[\sum_{S1}(N_1)(R_p + jwL_{p(1)})\right] \angle -\theta_R + \sum_{S1}(N_1)^2(R_{11} + jwL_{1(p)}) + \left[\sum_{S21}(\dot{N}_2)(N_1)(wL_{2(p)} - wL_{2(1)})\right] \angle -30° + \left[\sum_{S31}(N_3)(N_1)(wL_{3(p)} - wL_{3(1)})\right] \angle -150° \quad \text{(C40)}$$

where R_p is the total effective series resistance of the primary winding of a power stage plus any equivalent series resistance associated with internal impedance of the dc source. Likewise $L_{p(1)}$ includes the true leakage reactance plus any external equivalent series inductance. Z_{eq} will be in inverter pu ohms if resistances, inductive reactances and constants are in pu ohms.

APPENDIX D

Example of Internal Impedance Calculation and Its Use

Transformer Constants

Although the calculation of the leakage reactances of multi-winding transformers is a difficult problem, certain simplifying assumptions in regard to leakage fluxes can be made. These assumptions somewhat reduce the complexity of the problem and are justified, to an extent, by the fact that the leakage reactances of transformers calculated in accordance with these assumptions check reasonably well with the measured values. The approximate method used here is that given in reference 3.

The equivalent leakage reactance between two equal-length windings, referred to the one with N_2 turns, is given by (all dimensions in inches)

$$X_e = \frac{20.1}{2} f \frac{N_2^2 M}{L} \left(d_3 + \frac{d_1}{3} + \frac{d_2}{3}\right) \times 10^{-8} \qquad (D1)$$

where d_1 and d_2 are the thickness of windings 1 and 2 respectively, d_3 is the spacing between the windings. M is mean length of turns in both windings. L is the length of winding.

These dimensions along with other information on the winding positions and geometry are illustrated in figure 30.

The various windings are not of equal length. This increases the difficulty of accurately calculating the leakage reactance of such a design by elementary formulas. Fortunately, the problem at hand does not require that the leakage reactances be known to such a degree of accuracy as to warrant the use of formidable "exact" methods.

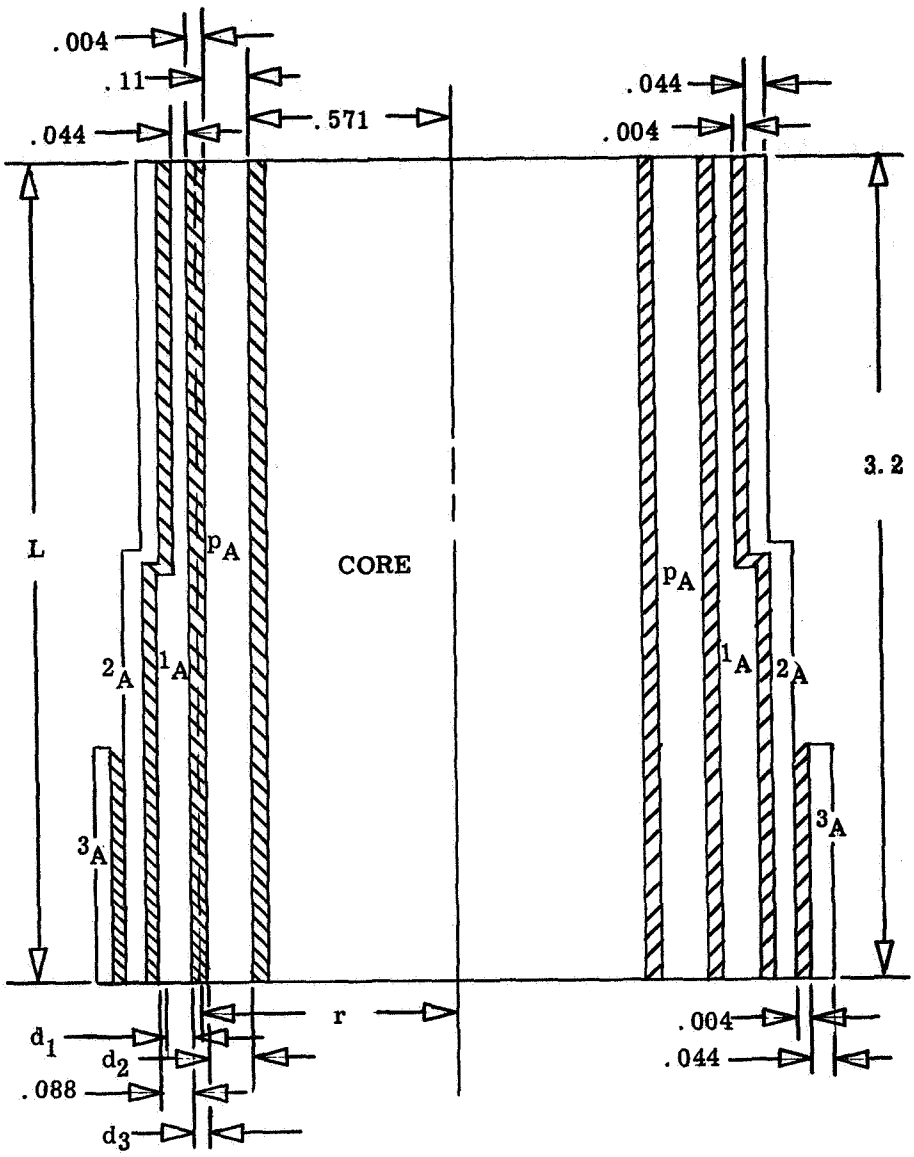
The method used is to adjust the thickness of each winding, while assuming them all to have the same length (L), so that the cross-sectional area of each winding remains the same.

For example, for winding p_A and l_A:

$$d_1 = \frac{0.088 + 0.044}{2} = 0.066$$

$$d_2 = 0.11$$

$$d_3 = 0.044$$



NOTE: Not to scale; dimensions given are all in inches.

Figure 30. - Sketch Used To Calculate Leakage Fluxes of Transformer A

$$L = 3.2$$
$$M = 2\pi r = 2\pi \left(0.571 + 0.11 + \frac{0.004}{2}\right) = 4.29$$
$$f = 400 \text{ Hz}$$
$$N_2 = 50$$

Substitution of these values into the equation for X_e gives:

$$wL_{p(1)} \cong 0.00845 \text{ ohms.} \tag{D2}$$

The leakage reactances used in the Internal Impedance Calculations were calculated in a similar manner. The results are given in table I.

Based on a 750 VA inverter: $V_B = 115$ volts
$I_B = 2.17$ amps
$Z_B = 53$ ohms

The transformer ratio ($\dot{\overline{T.R.}}$) can be calculated as follows:

$$\dot{\overline{T.R.}} = \sum_{S1} \dot{N}1 = -N_{1A} \angle 0° - N_{1B} \angle \frac{-180°}{4} - N_{1C} \angle \frac{-360°}{4} \tag{D3}$$

$$+ N_{1D} \angle \frac{-540°}{4} = -1.7\angle 0° - 1.7\angle -45° - 0.7\angle -90° + 0.7\angle -135°$$

$$\dot{\overline{T.R.}} = -3.67 \angle -22.5° = 3.67 \angle 157.5° \tag{D4}$$

Table I. - Transformer Constants

Transformer	R_p (ohms)	$wL_{p(1)}$ (ohms)	$wL_{1(p)}$ (ohms)	$wL_{2(p)}$ (ohms)	$wL_{2(1)}$ (ohms)	$wL_{3(p)}$ (ohms)	$wL_{3(1)}$ (ohms)	N_1	N_2	N_3
A	0.082	0.0085	0.0085	0.018	0.007	0.017	0.0065	1.7	1.46	0.24
B	0.082	0.0085	0.0085	0.017	0.006	0.018	0.0065	1.7	0.24	1.46
C	0.082	0.022	0.022	0.018	0.007	0.0085	0.007	0.7	1.12	1.82
D	0.082	0.022	0.022	0.0845	0.006	0.018	0.007	0.7	1.82	1.12

The sum defined in definition 13 will be calculated next. The effective internal resistance of the dc supply is approximately 0.0324 ohms. Therefore, the R_p's used in the following equations will be taken as equal to 0.082 + 0.0324 ohms or 0.114 ohms.

$$\sum_{S1} (\dot{N}_1)(R_p + jwL_{p(1)}) = \dot{N}_{1A}(R_{pA} + jwL_{p(1)A}) + \dot{N}_{1B}(R_{pB}+jwL_{p(1)B})$$
$$+ \dot{N}_{1C}(R_{pC}+jwL_{p(1)C}) + \dot{N}_{1D}(R_{pD}+jwL_{p(1)D})$$
$$= 1.7\angle 0° \ (0.144+j0.0085)$$
$$- 1.7\angle -45° \ (0.114+j0.0085) - 0.7\angle -90° (0.114$$
$$+ j0.022) + 0.7\angle -135° (0.114+j0.022)$$
$$= -(0.402 - j0.126) \qquad \text{(D5)}$$

$$\sum_{S1} (\dot{N}_1)(R_p+jwL_{p(1)}) = -0.422\angle -17.5° \text{ ohms or } \frac{-0.422}{53} \angle -17.5° \text{ pu ohms} \qquad \text{(D6)}$$

Note that the first term of equation (C40) can now be evaluated using equation (D4) and equation (D6). Thus,

$$\text{First term eq. (C40)} = 3\left[\frac{\text{T.R.}}{(NS)}\right] \sum_{S1} (\dot{N}_1)(R_p+jwL_{p(1)}) \angle -\theta_R$$
$$= \frac{3}{4}(3.67)(-0.422) \angle -17.5° \ -157.5° \qquad \text{(D7)}$$

$$\text{First term of eq. (C40)} = 1.16 \angle 5° \text{ ohms or } \frac{1.16}{53} \angle 5° \text{ pu ohms} \qquad \text{(D8)}$$

Next consider the second term of equation (C40)

$$\text{Second term of eq. (C40)} = \sum_{S1} (N_1)^2 (R_{11}+jwL_{1(p)}) \qquad \text{(D9)}$$
$$= \sum_{S1} (N_1)^2 R_{11} + \sum_{S1} (N_1)^2 (jwL_{1(p)})$$

The quantity $\sum_{S1} (N_1)^2 R_{11}$ is the total series resistance of the windings connected in Phase 1. Calculated from wire size and length it equals 0.85 ohms; therefore,

$$\begin{aligned}\text{Second term of eq. (C40)} &= 0.85 + (N_{1A})^2 jwL_{1(p)A} \\ &+ (N_{1B})^2 jwL_{1(p)B} + (N_{1C})^2 jwL_{1(p)C} \\ &+ (N_{1D})^2 jwL_{1(p)D} = 0.85 \\ &+ j(1.7)^2(0.0085)+j(1.7)^2(0.0085) \\ &+ j(0.7)^2(0.022)+j(0.7)^2(0.022)\end{aligned} \tag{D10}$$

$$\text{Second term of eq. (C40)} = 0.85 + j0.0706 \text{ ohms or}$$

$$\frac{0.85+j0.0706}{53} \text{ pu ohms.} \tag{D11}$$

Next consider the third term of equation (C40)

$$\begin{aligned}\text{Third term of eq. (C40)} &= \left[\sum_{S21} (N_2)(N_1)(wL_{2(p)} - wL_{2(1)})\right] \underline{/-30°} \\ &= \left[-(N_{1A})(N_{2A})(wL_{2(1)A} - wL_{2(p)A})\right. \\ &- (N_{1B})(N_{2B})(wL_{2(1)B} - wL_{2(p)B}) \\ &+ (N_{1C})(N_{2C})(wL_{2(1)C} - wL_{2(p)C}) \\ &\left. - (N_{1D})(N_{2D})(wL_{2(1)D} - wL_{2(p)D})\right] \underline{/-30°} \\ &= [-(1.7)(1.46)(0.018-0.007) \\ &- (1.7)(0.24)(0.017-0.006) \\ &+ 0.7(1.12)(0.018-0.007) \\ &- (0.7)(1.82)(0.0085-0.006)] \underline{/-30°} \\ &= 0.0264 \underline{/-30°} = -0.0228+j0.0132.\end{aligned} \tag{D12}$$

Third term of eq. (C40) = 0.0228 + j0.0132 ohms or

$$\frac{0.0228+j0.0132}{53} \text{ pu ohms} \qquad \text{(D13)}$$

Next consider the fourth term of equation (C40)

$$\text{Fourth term of eq. (C40)} = \left[\sum_{S31} (N_3)(N_1)(wL_{3(p)} - wL_{3(1)})\right] \angle -150°$$

$$= \left[-(N_{1A})(N_{3A})(wL_{3(p)A} - wL_{3(1)A}) - (N_{1B})(N_{3B})(wL_{3(p)B} - wL_{3(1)B}) - (N_{1C})(N_{3C})(wL_{3(p)C} - wL_{3(p)C}) + (N_{1D})(N_{3D})(wL_{3(p)D} - wL_{3(1)D})\right] \angle -150°$$

$$= [-(1.7)(0.24)(0.017-0.0065) - (1.7)(1.46)(0.018-0.0065) - (0.7)(1.82)(0.0085-0.007) + (0.7)(1.12)(0.018-0.007)] \angle -150°$$

$$= -0.0261 \angle -150° = 0.0226+j0.0130 \qquad \text{(D14)}$$

Fourth term of eq. (C40) = 0.0226+j0.0130 ohms or

$$\frac{0.0226+j0.0130}{53} \text{ pu ohms} \qquad \text{(D15)}$$

Substituting the values of equations (D8), (D11), (D13), and (D15) into equation (C40):

$$\dot{Z}_{eq} = 1.16 + j0.1 + 0.85 + j\ 0.0706 - 0.0228 + j\ 0.0132 + 0.0226 + j\ 0.0130. \qquad \text{(D16)}$$

Collecting terms:

$$\dot{Z}_{eq} = 2.01 + j0.1968 \text{ ohms or } \frac{2.01 + j0.1968}{53} \text{ pu ohms} \qquad \text{(D17)}$$

Referring back to figure 25, $\dot{Z}_1$ can now be calculated:

$$\dot{Z}_{eq}+R_F+jwL_F = 2.01+j0.1968+0.32+j(2.512)5 = 2.33+j12.69 \text{ ohms} \qquad \text{(D18)}$$

C_{eq} = 3 mfd; X_C = 132 ohms

$$\dot{Z}_p = \frac{(2.38+j12.59)(-j132)}{2.38-j119.41} = 2.61+j13.9 \text{ ohms} \quad \text{(D19)}$$

$$\dot{Z}_p + \dot{Z}_{C.T.} = 2.61+j13.9+0.383 \text{ ohms} \quad \text{(D20)}$$

$$\dot{Z}_1 = 3.00+j13.9 = 14.3 \angle 77.8° \text{ ohms} \quad \text{(D21)}$$

or

$$\dot{Z}_{1pu} = \frac{14.3}{53} \angle 77.8° = 0.27 \angle 77.8° \text{ pu ohms} \quad \text{(D22)}$$

If the phasor $\Delta\dot{I}$ has its angle with reference to a voltage, V_2, θ_2 degrees ahead of the phase voltage of the phase in which differential current loop is placed, it is desirable to have:

$$\theta_o - \theta_1 - \theta_2 \cong -90° \quad \text{(D23)}$$

θ_o will generally vary between 0° and 15° depending on the load. For example: at full load unity power factor, equation (A14) gives

$$\tan \theta_o = \frac{\sin(77.8°)}{\frac{1}{0.27} + \cos 77.8°} = 0.249$$

$$\theta_o = 14°$$

at full loads 0.7 power factor lag

$$\tan \theta_o \quad \frac{\sin (77.8° - 45°)}{\frac{1}{0.27} + \cos (77.8° - 45°)} = 0.119$$

at no load condition $\theta_o = 0°$

As is customary with ac generator parallel systems, the differential current sensing loop will be connected in phase C (refer to figure 31), with $V_{LNC} = V \angle 0°$ then $V_{LLAC} = \sqrt{3}\ V \angle 30°$ is a phase voltage $\theta_2 = 30°$ ahead of the phase where differential current is sensed. At full load unity power factor, equation (A24d) becomes

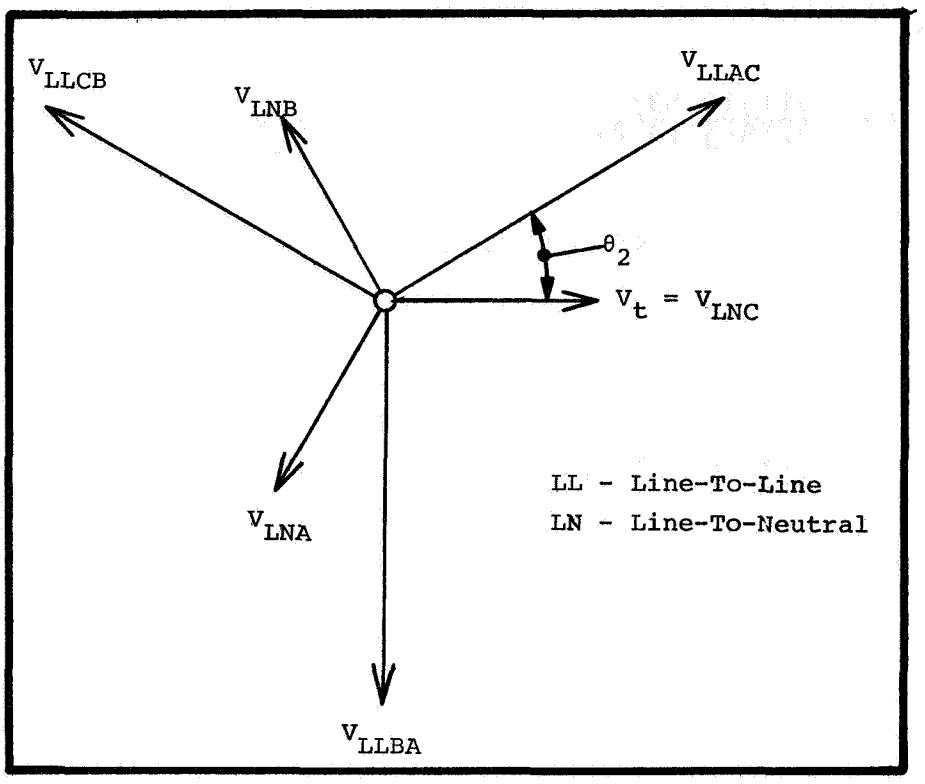


Figure 31. - Phasor Diagram of Terminal Voltages

$$\dot{\Delta I} = \frac{\Delta E}{Z_1} \ \underline{/14°-77.8-30°} = \frac{\Delta E}{Z_1} \ \underline{/-93.8°} \qquad \text{(D23)}$$

and if one of the inverters has an internal voltage greater than the average, it will result in that inverter taking more lagging reactive (in reference to V_{LLAC}) current than the average and its "reactive" load division circuit would need to reduce the "excitation"voltage (dc voltage applied to power stages) of that inverter.

The gain needed in this "reactive" load division circuit may be calculated using the closed loop voltage regulation characteristics of a single unit as follows:

Define $E_{F.L.}$ to be the "internal" developed voltage (Thevenin's equivalent voltage) needed to maintain a full load terminal voltage, defined to be $V_{F.L.}$.

Then:
$$E_{F.L.} = \frac{|\dot{Z}_1+\dot{Z}_L|}{Z_L} V_{F.L.} = \frac{1}{K} V_{F.L.} \qquad \text{(D24)}$$

Define $V_{N.L.\ REG}$ to be the terminal voltage under no load with the voltage regulator loop operating.

Define $V_{F.L.\ REG}$ to be terminal voltage under full load with the voltage regulator loop operating.

If closed loop voltage regulation is ± 0.7 volt = ± 0.0061 pu volts and assuming $V_{N.L.\ REG}$ = 1 pu and $V_{F.L.\ REG}$ = 0.9939 pu volts

$$\frac{\partial E}{\partial V_S} = -\left|\frac{E_{F.L.} - V_{N.L.\ REG}}{V_{N.L.\ REG} - V_{F.L.\ REG}}\right| = -\left|\frac{\frac{|\dot{Z}_1 + \dot{Z}_L|}{Z_L}(0.9939) - 1.}{1 - 0.9939}\right| \quad \text{(D25)}$$

For Full Load 0.7 power factor lag

$$\frac{\partial E}{\partial V_S} = \left|\frac{|0.27\ \underline{/77.8°} + 1\underline{/45°}|\ (0.9939) - 1}{0.0061}\right| \quad \text{(D26)}$$

$$\frac{\partial E}{\partial V_S} = -38 \quad \text{(D27)}$$

where V_S = voltage to sensing circuit = $V_{L.N.}$

Assuming a 115 ± 0.2 volt individual unit voltage setting,

V_{1L} = 1.00174 pu volts max.

and $V_o = V_{pL}$ = 1 pu

Equation (B9) becomes:

$$\Delta E = |E_{pL} - E_o| = (1-1.00174)\frac{\partial E}{\partial V_S} + \frac{1}{K}(1.00174-1) + \frac{\partial E}{\partial I_{DQ}}(\Delta I) \quad \text{(D28)}$$

$$\Delta E = 0.0682 + \frac{\partial E}{\partial I_{DQ}}(\Delta I) \quad \text{(D29)}$$

If the design objective is to assure that the load unbalance will never exceed 10%, the maximum allowable ΔE can be obtained from the expression:

$$\Delta I_{max} = 0.1\ \text{pu} = \frac{\Delta E_{max}}{Z_1} = \frac{\Delta E_{max}}{0.27} \quad \text{(D30)}$$

$$\Delta E_{max} = 0.027 = 0.0682 + \frac{\partial E}{\partial I_{DQ}} \quad (0.1), \text{ so} \tag{D31}$$

$$\frac{\partial E}{\partial I_{DQ}} = \frac{0.027 - 0.0682}{0.1} = - 0.412 \tag{D32}$$

This is the required gain of the reactive load-division circuit expressed in pu volts droop per load current unbalance in pu. Since the reference voltage is $V_{LLAC} = \sqrt{3}V\underline{/30°}$ (figure 31), 60° lagging loads would appear as a 90° lagging current with respect to the reference voltage. Therefore, the reactive load-division circuit should be made most sensitive to 60° lagging loads.

APPENDIX E

Reliability and System Weight

The discussion of factors involved in increasing reliability is concerned specifically with dc-to-ac static-inverter systems operating at power levels suitable for spacecraft auxiliary power.

Three types of systems are considered: (1) several inverters, one operating and the rest used as standby (or backup) units; (2) several inverters operating isolated; and (3) several inverters operating in parallel.

Factors Affecting Weight and Reliability of a Single Static Inverter. - The quality of power required of the inverter is an important factor in determining inverter weight. Accurate voltage and frequency regulation, phase displacement regulation and low-harmonic content all require additional electrical components, which add weight. To cite an extreme example, some inverters, designed for the relatively undemanding task of driving induction motors, allow a drastic weight reduction by eliminating all power transformers and filters.

The means of cooling and the temperature of the cooling medium affect the weight of an inverter, but the kind of cooling system is usually determined on bases other than minimizing inverter weight.

Another variable is input voltage. There is an optimum input voltage for every inverter design, and wide variance from the optimum causes reduced efficiency and increased weight. While 28 volts dc has been a very common level, 56 volts is a more desirable input voltage for transistor inverters. This higher value is more desirable for two reasons. First, for a given power level, the higher voltage results in a lower current which reduces resistive power losses. Second, 56 volts can be conveniently switched by transistors without exceeding the voltage ratings of transistors.

Unlike an electro-dynamic inverter (motor-generator), a static inverter has very little inherent capacity for overloads. If the inverter is required to carry overloads for extended periods of time (beyond a few minutes), the inverter weight increases because the unit must be designed for the peak power requirement rather than for normal load.

With so many factors affecting the basic weight-to-power relationship, it is difficult to accurately predict the weight of a new inverter design. However, to define a standard of

reference for the numerical examples given later, a curve of inverter weight as a function of power rating has been drawn, figure 32. This curve has been established on the basis of empirical data and represents approximately the present state-of-the-art. The equation of the curve results from inspection and not from any theorectical consideration.

Basis of Reliability Calculations. - In the final analysis, the determining factor in reliability is time. The Department of Defense defines reliability as "The probability that a piece of equipment will give satisfactory performance for a specified period of time, under specified operating conditions."

The lifetime of a piece of equipment, such as an inverter, is usually thought to be composed of three periods: the early failure or "burn-in" period; the "random-failure" period; and the end-of-life or "wearout" period. The failure rate is high during the first and third periods and relatively low during the second period.

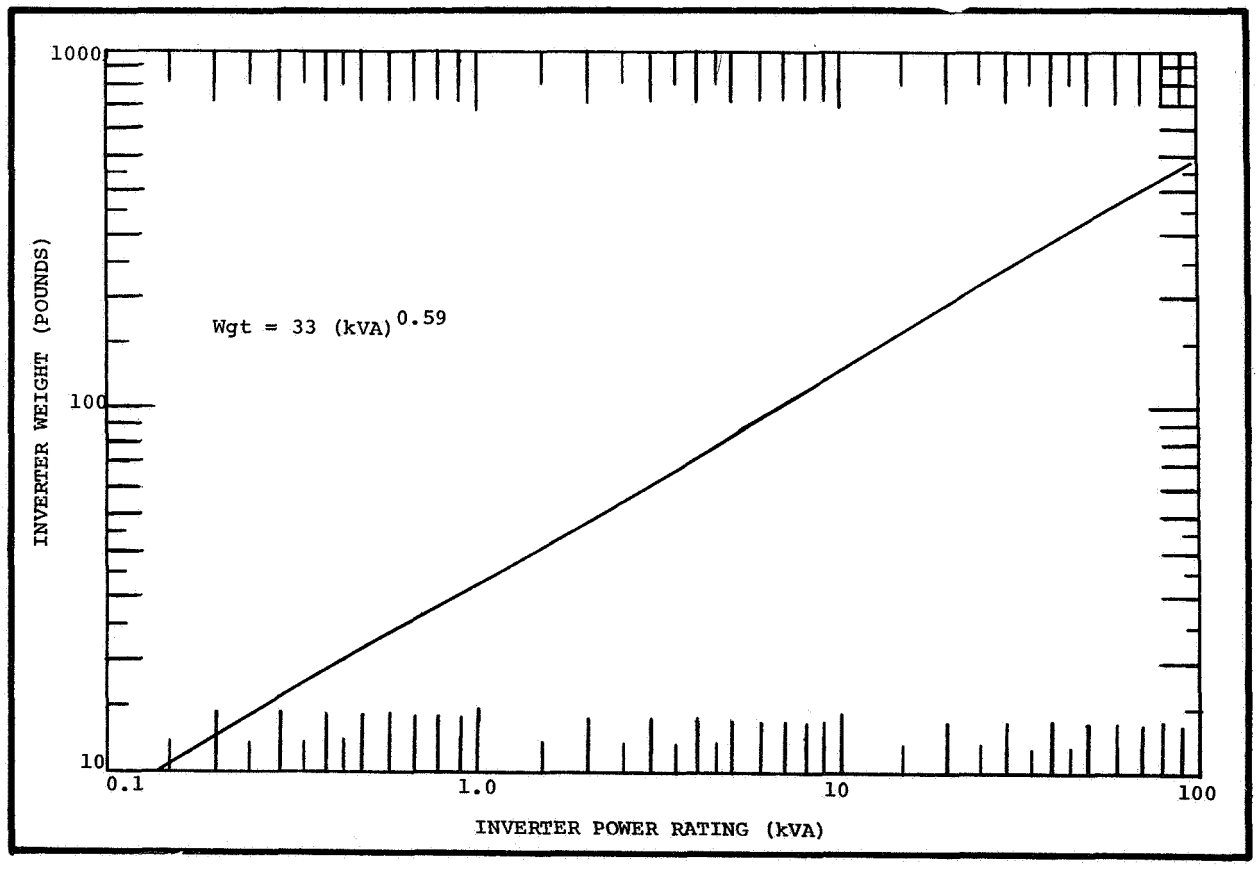


Figure 32. - Typical Weight Versus Power Rating of Static Inverters

An inverter for use in a spacecraft power system would be tested for a considerable time prior to launch, or long enough to cover the early-failure period. The mission duration would be short enough so that the "wearout" period would not be reached. Thus attention is focused on the random-failure period of the inverter's life.

During this period, the inverter reliability can be described as a time function:

$$R = e^{-ft} \tag{E1}$$

where

R is the reliability

t is the time

f is the failure rate (reciprocal of MTBF)

MTBF is the mean-time-between-failures or mean-time-to-failure of a non-repairable item.

This equation is plotted in figure 33 to show graphically the dependence of reliability on time. The units of time on the horizontal axis are MTBF units. The ordinate, reliability, is the probability that the inverter survives for the specified period of time, assuming it was operating successfully at time zero.

The binomial expansion is used to calculate the reliability of a redundant system (reference 4).

$$(R + Q)^n = 1^n = 1$$

where

n is the number of items

R is the reliability of an item

Q is the probability of failure

R + Q = 1 by definition.

The probability of failure (Qs) of a redundant system is from this expression:

$$Qs = Q^n + nQ^{n-1}R + \frac{n(n-1)}{2!} Q^{n-2}R^2 + \frac{n(n-1)(n-2)}{3!} Q^{n-3}R^3 + \text{---}$$

where

The first term is the probability of exactly n failures on n items.

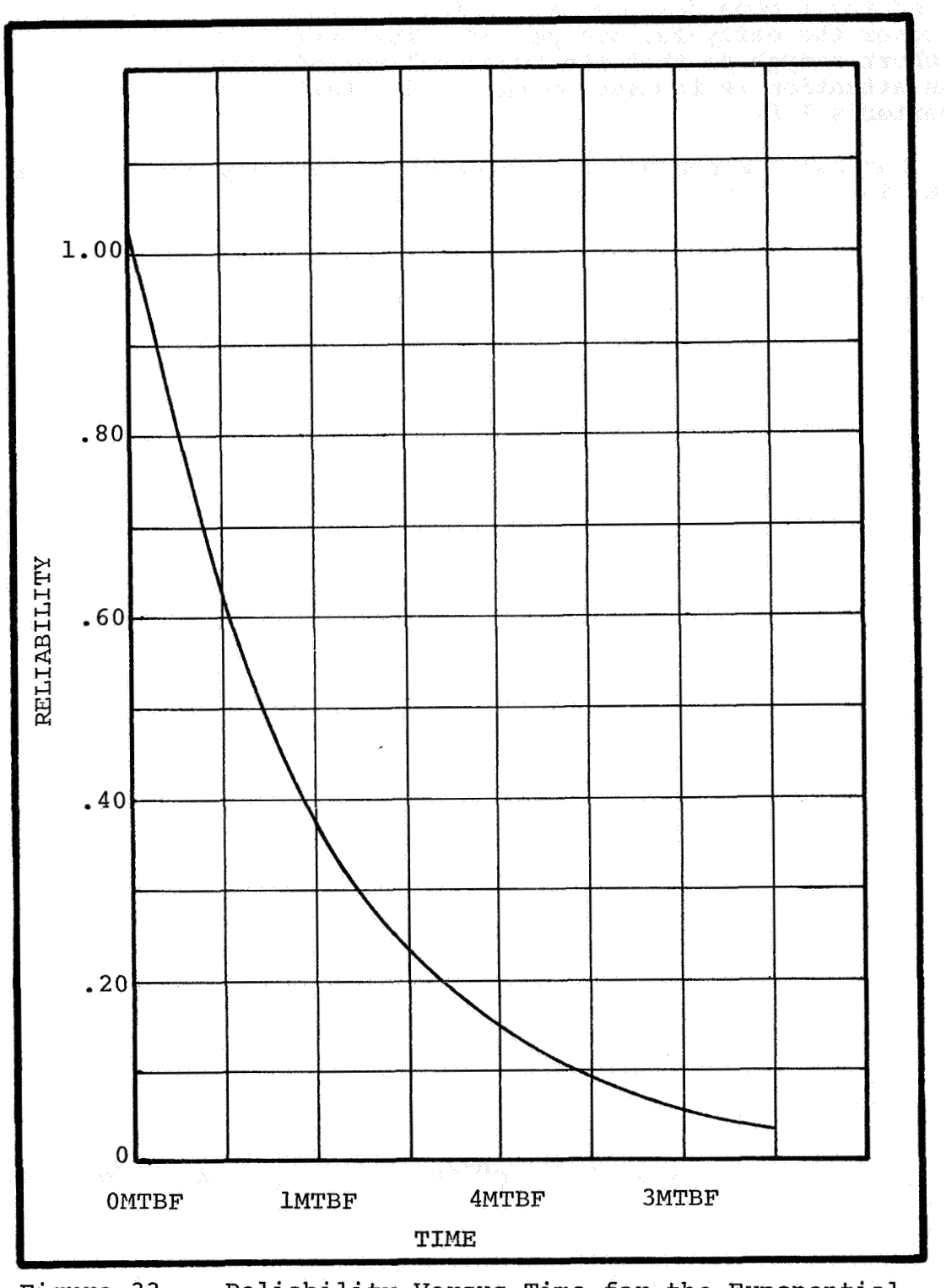


Figure 33. - Reliability Versus Time for the Exponential Distribution

The second term is the probability of exactly n-1 failures on n items.

The third term is the probability of exactly n-2 failures on n items.

The fourth term is the probability of exactly n-3 failures on n items, etc.

The system unreliability (Qs) is determined by adding the number of terms equal to the number of failures allowed. For example, in a seven-item system with three failures allowed, the first three terms of the previous equation are added together. The system reliability (Rs) is then:

$$Rs = 1 - Qs \qquad (E2)$$

Reliability and System Weight. - The assumptions made thus far are (1) the failure rate of the inverter is independent of rating, and (2) the specific weight decreases with rating according to figure 32.

Redundancy, or improved reliability, is achieved by providing more system capacity than is required. Thus as inverters fail, the required system capacity can still be met by the remaining inverters. If a system's capacity is to be met by using either a single unit with 0.90 reliability, or two half-rated units each with 0.90 reliability, the reliability of the first system is 0.90 while that of the second system is 0.81.

From this it is evident that more stand-by units are required in the second system. However, the second system has smaller-rated units, and therefore less weight per unit. The selection now depends on the weight characteristics of the units as a function of rating.

Using the inverter weight curve presented earlier, the single inverter with a standby is lighter for a given reliability.

The following two examples are presented to compare a standby system with a multiple system.

System 1 is the standby system. System 2 consists of multiple, lower-rated inverters, all operating simultaneously.

Ri is the inverter reliability, 0.90

Rl is the reliability of System 1

R2 is the reliability of System 2

Qi = 1 - Ri

Example 1

The system rating is three kVA with a system reliability of 0.99.

System 1 requires two 3-kVA inverters.

$$R1 = 1-(Qi)^2 = 1 - (0.1)^2 = 0.99$$

From figure 32, the weight of System 1 is:

(2 units)(64 pounds/unit) = 128 pounds.

System 2 requires four, 1.5 kVA inverters.

$$R2 = 1 - (Qi^4 + 4Qi^3 Ri) = 1 - 0.0037 = 0.9963$$

From figure 32, the weight of System 2 is:

(4 units)(42 pounds/unit) = 168 pounds

This example shows that the standby redundant system is lighter in weight. However, as example 2 shows, a change in the reliability requirement results in System 2 being lighter.

Example 2

The system requirements are the same as for example 1 except the system reliability is increased to 0.995.

System 1 requires three, 3-kVA inverters.

$$R1 = 1 - (Qi)^3 = 1 - (0.1)^3 = 0.999$$

The weight of System 1 is:

(3 units)(64 pounds/unit) = 192 pounds

Referring to Example 1, the reliability of System 2 is 0.9963 with four, 1.5 kVA inverters and the system weight is 168 pounds.

For the second example, System 2 is the lighter.

The results of the above examples show that the best system arrangement, considering only weight and reliability, depends on the reliability requirements and the specific weight for the inverter. Thus, these two criteria alone cannot be used to select a system approach.

Obviously, if a single inverter meets the reliability requirements and the system rating, there is no need to add complication to the system. Should a single inverter not meet these requirements, one of the three methods described at the beginning of this Appendix must be used.

If the failure rate is independent of rating, the full-rated, single-inverter system with standby will generally provide the lightest and most reliable system. The multiple unit system (isolated or paralleled) has the disadvantage of its higher specific weight. The multiple unit system is better when an additional standby unit is required with only a few percentage points missed in the reliability goal.

The maximum power that a single inverter can deliver is limited by the power rating of electric parts (such as transistors) available at the time the inverter is designed. Of course, paralleling of load-carrying elements within the inverter can provide higher power capacity but at the expense of increasing both specific weight and failure rate. Use of multiple units (paralleled or isolated) can improve system reliability with smaller increases in system weight. The increased reliability is achieved because one failure within an inverter with paralleled components would effectively fail two inverters.

In a multiple system, older, more refined inverter designs can be used, and the system reliability can be predicted with confidence. Higher power systems would simply use a larger number of inverters. By contrast, the standby-type system would probably require a new inverter design for each new power level, resulting in lower reliability, less confidence in the reliability prediction, and higher cost.

Another advantage of the multiple inverter system is that each inverter would be operating at less than maximum rating throughout most of the mission. This would provide some increase in reliability since the stress levels would be less. The paralleled system would be better than an isolated system because the load on all inverters would increase incrementally as inverters failed. The isolated system would require one inverter to assume the total load of a failed inverter. Another advantage of having multiple, smaller-rated inverters is that is one unit fails some power is still available even though the full system capacity cannot be met.

The choice between a paralleled load-bus system and an isolated load-bus system depends on the load requirements.

The isolated load-bus system consists of several inverters, each furnishing power to a load bus. This approach assumes that

no single load is greater than the capacity of one inverter. Should an inverter fail, the load buses would be interconnected such that the load could be switched to an operating inverter. The switching arrangement would be comparable to that of a parallel system. Control circuits would be required to prevent one inverter from handling more than its rating. Fault-clearing capacity of the isolated system would be limited by the capability of a single inverter. The weight and reliability of the isolated, load-bus system would be slightly better than an equivalent parallel system.

The paralleled load-bus system consists of several inverters each furnishing power to a load bus. The load busses would be interconnected during normal operations. Current sharing circuits are required to insure proper distribution of loads between the inverters. The advantages of the parallel system over the isolated system are (1) higher fault-clearing capacity (equal to or greater than a single, full-rated inverter), (2) better overload capacity for such loads as induction motors which may require as much as 500 percent rated current when started, (3) capability of a continuous flow of power even if one inverter should fail, and (4) practically unlimited total load capacity.

Table II is a summary of the preceding discussion on the merits of each approach. The choice of approaches is, as always, dependent upon the conditions prevailing for a particular application.

Table II. - Comparison of Inverter Systems

Type of System	Standby Redundant	Multiple Inverter Isolated Bus	Multiple Inverter Paralleled Bus
Reliability	Improves in discrete steps as more units are added.	Any Specified reliability can be met.	Any Specified reliability may be met.
Weight	Weight depends on reliability	Weight depends on reliability	Weight depends on reliability
Maximum power	Limited by components	Unlimited - except by the largest single load	Unlimited - Any number of units may be paralleled
Complexity	Simplest	Complex	Slightly more than isolated system
Results of failing one	Momentary loss of power	Momentary loss of power to the failed bus	No loss of power
Fault clearing	1.5 pu current	Limited by overload rating* $\frac{1.5}{m}$ current	Limited by number of inverters connected n(1.5) pu current Minimum

* m = number of systems needed to supply 1 pu system power

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