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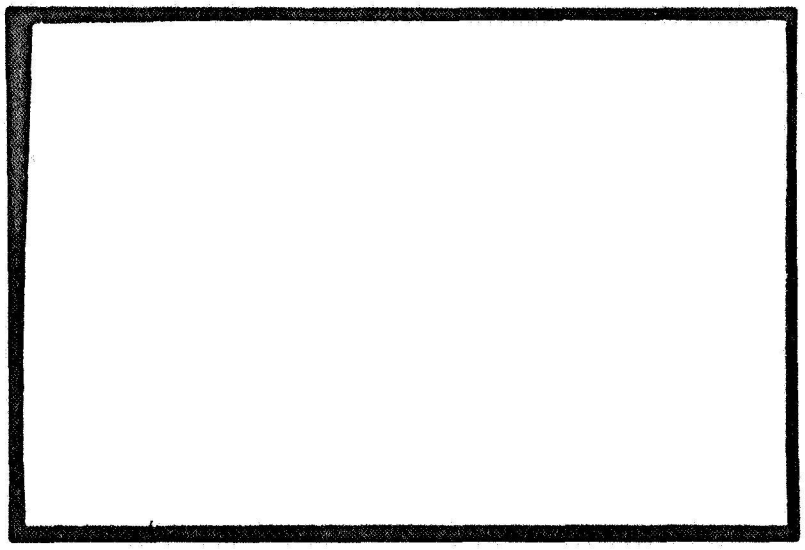

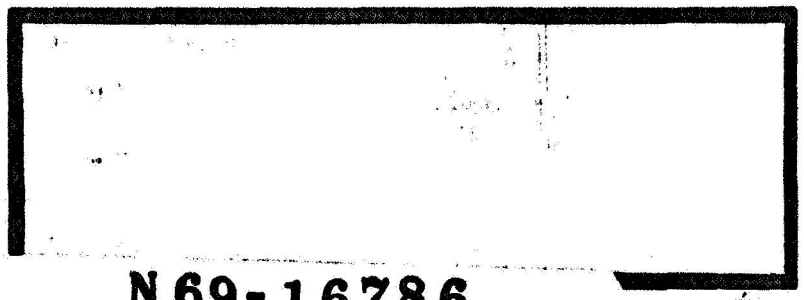

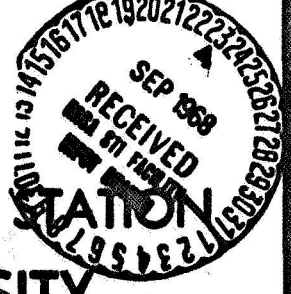

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THE ANALYSIS AND DESIGN OF A CLASS-D AMPLIFIER

Prepared by

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FOREWORD

This is a technical report of a study conducted by the Electrical Engineering Department, Auburn University, toward fulfillment of Contract NAS8-11344. This report represents a summary of the research conducted to date on class-D power amplifiers.

ABSTRACT

Switching-mode, or class-D, amplification may be used to take advantage of the high efficiency of operating transistors in the saturation region. This report describes the theoretical analysis of a basic switching-mode amplifier configuration, and reduces the theoretical material to a specific procedure for the practical design of switching-mode amplifiers for a variety of applications. The basic configuration features high overall efficiency, low quiescent power consumption, a filtered, analog output signal, and adaptability to a wide variety of input, feedback and load configurations. Included is a design example with a maximum d-c power output of 150 watts at an overall efficiency of 90% at maximum power output.

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THE ANALYSIS AND DESIGN OF A CLASS-D AMPLIFIER

M. A. Honnell, J. K. Newell, and M. T. McPherson

1. INTRODUCTION

Class-D amplification may be defined as the following generalized process: (1) an analog input signal is converted to a modulated constant-amplitude pulse signal; (2) the modulated pulse signal is amplified; (3) an analog output signal is obtained by demodulating the modulated pulse signal. Class-D amplification may be accomplished by switching a transistor from its non-conducting ("off") state, to its saturated ("on") state at a certain rate such that an output pulse of a certain duration is obtained. If, for example, either the pulse width or pulse frequency is modulated by an input signal, then the input information can be recovered by passing the output pulses through a low pass filter. Thus class-D amplification may be employed to take advantage of the most efficient type of transistor operation, the saturated-switching mode.

This report presents a basic class-D amplifier circuit configuration in a general form, which is readily adaptable to a wide variety of specific applications. In the following chapters the theoretical aspects of the basic design are considered first with a stage-by-stage analysis. Also considered from a theoretical point of view are feed-

back, input, and output (load) configurations, and the frequency spectrum of the pulse-width-modulated signal. From this material a practical design procedure is formulated. This procedure is then employed in the design of a 150-watt amplifier. The results of actual performance tests made on the amplifier are also presented.

The block diagram of the basic class-D amplifier design developed is shown in Fig. 1-1. The input stage amplifies the difference voltage, a signal proportional to the difference between the input and feedback voltages. This provides a control voltage to the pulse-width modulator. The modulator, driver and output stages each have two separate, but similar circuits, referred to as the "P" channel, which responds to positive control voltages and produces negative output voltages, and the "N" channel which responds to negative control voltages and produces positive output voltages. The polarity of the control voltage determines which channel is to be activated and the magnitude of the control voltage determines the pulse width produced by the modulator. The pulses generated by the modulator undergo power amplification in the driver stage and are coupled to the output stage, causing the output stage to operate in the switching mode. The high-power pulse signal generated is filtered to provide an analog output voltage, e_o.

Some of the features possessed by the basic amplifier design presented are: (1) the capability of producing both a-c and bipolar d-c output voltages (a d-c voltage of either polarity); (2) a maximum power output of several hundred watts without significant departure from the basic design; (3) overall d-c efficiency of 90% at maximum power output with efficiency remaining relatively high over most

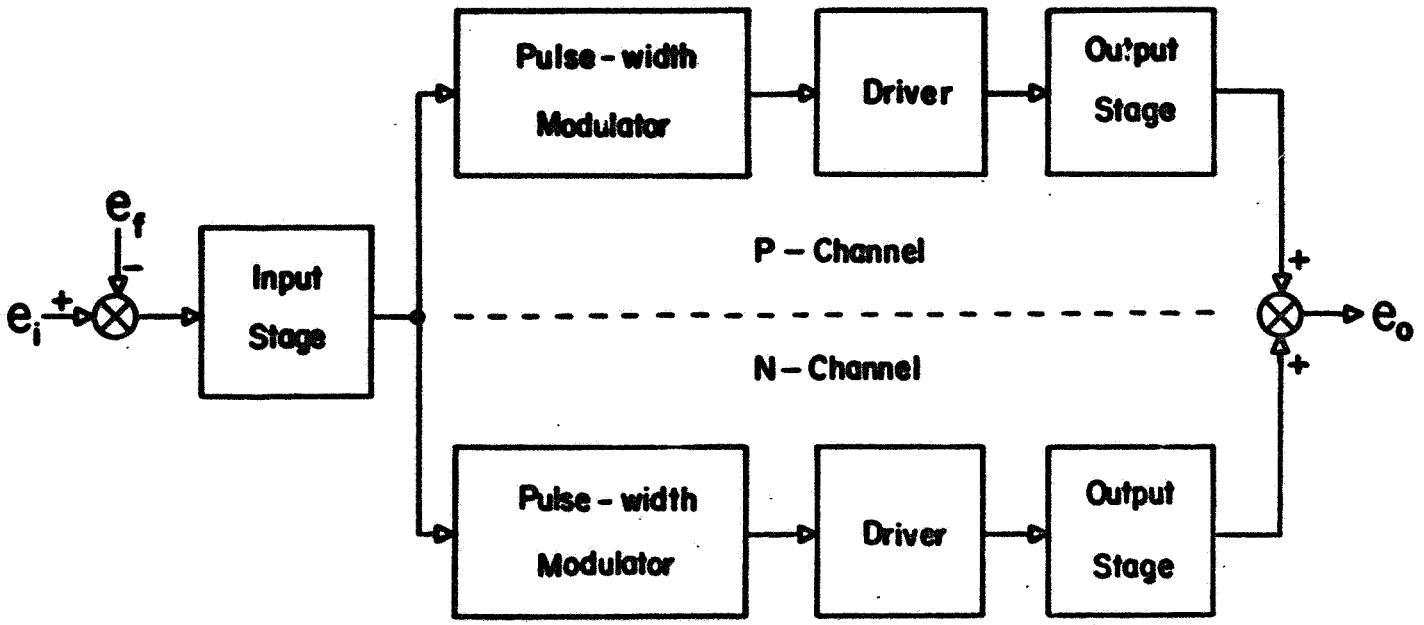

Fig. 1-1.--A block diagram of a basic pulse-width-modulated, class-D amplifier.

of the range of power output; (4) very low quiescent power consumption; and (5) input and output circuitry adaptable to a wide variety of signal sources, loads, and feedback configurations.

2. INPUT STAGE

The input stage is a high-gain operational amplifier with local feedback, connected such that the stage is a non-inverting amplifier. A schematic diagram of the input stage is shown in Fig. 2-1. The primary function of the input stage is to provide the complete class-D amplifier with a high open-loop voltage gain. In addition, the input stage provides the complete amplifier with a high-impedance input and also provides a convenient means of introducing frequency compensation for stabilization of the complete amplifier.

The diodes D_{11}, D_{12}, D_{13} and D_{14} may be disregarded in presenting the theoretical operation of the input stage. Their function will be discussed later in the chapter.

For the presentation of the theoretical aspects of the input stage the operational amplifier, A_{11}, will be assumed to have infinite input impedance, zero output impedance, and infinite voltage gain. Two very important restraints are usually assumed for the input terminals of an ideal operational amplifier. First, no current flows into either of the input terminals; and second, when negative feedback is applied around an ideal operational amplifier, the voltage between the input terminals will approach zero.[1]

Referring again to Fig. 2-1, it may readily be seen that if no current flows into either input terminal, then no current will flow at the terminal marked e_d. Therefore, the input impedance of the input

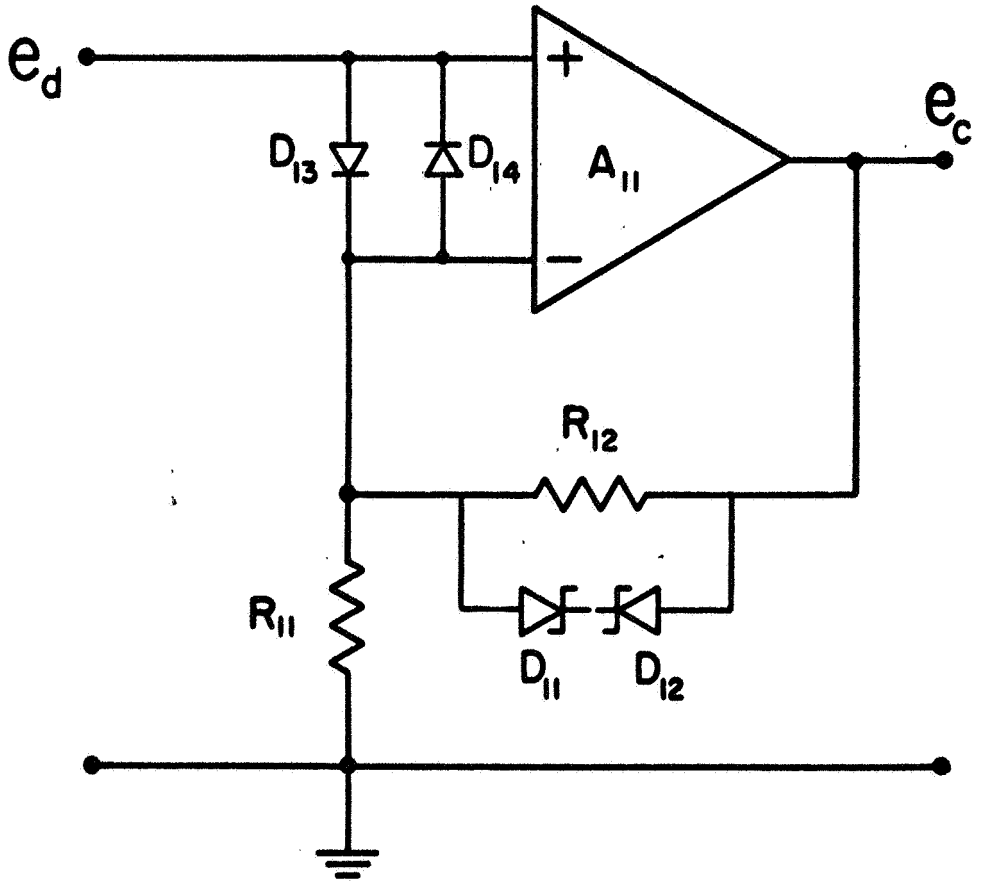

Fig. 2-1--Schematic diagram of the input stage.

stage is infinite for the non-inverting configuration shown. Such would not be the case if an inverting configuration were used.

The voltage gain of the input stage may be derived from the circuit of Fig. 2-2. Since local negative feedback would tend to make the voltage between the input terminals equal to zero, both inputs are at the same potential and the current i is given by

$$i = \frac{e_d}{R_{11}}$$

The output voltage of the stage is called the control voltage, e_c, since this voltage controls the pulse-width modulator. This voltage is given by

$$e_c = i\ (R_{11} + R_{12}) .$$

Thus the voltage gain of the input stage is given by

$$A_1 = \frac{e_c}{e_d} = \frac{R_{11} + R_{12}}{R_{11}} . \qquad (2\text{-}1)$$

The input stage is designed to use an integrated-circuit operational amplifier, although a discrete-component operational amplifier may be more desirable for some applications. Regardless of what type of operational amplifier is used, it will have less-than-infinite input impedance and less-than-infinite voltage gain. Taking into account these two departures from the ideal, the input stage may be represented by the

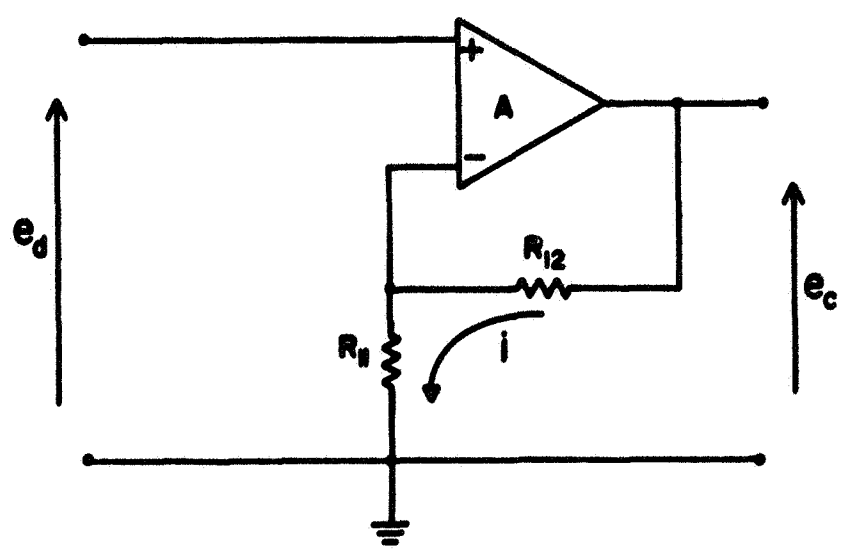

Fig. 2-2--Simplified schematic diagram of the input stage.

circuit of Fig. 2-3.

The loop equations are

$$e_d = i\ (R_1 + R_{11}) - i' R_{11}$$
$$-e_c = -i\ R_{11} + i' (R_{11} + R_{12})$$

where R_1 is the input resistance of the operational amplifier. Other relations are

$$e_1 = i R_1$$

and

$$e_c = Ae_1 ,$$

where A is the voltage gain of the operational amplifier. From these relations the input resistance of the input stage is

$$R_i = \frac{e_d}{i} = R_1 + R_{11} - R_{11} \frac{(R_{11} - AR_1)}{(R_{11} + R_{12})} \qquad (2\text{-}2)$$

The input stage voltage gain is

$$A_i = \frac{e_c}{e_d} = \frac{(R_{11} + R_{12})}{\frac{(R_1 + R_{11})(R_{11} + R_{12})}{AR_1} - \frac{R_{11}(R_{11} - AR_1)}{AR_1}} \qquad (2\text{-}3)$$

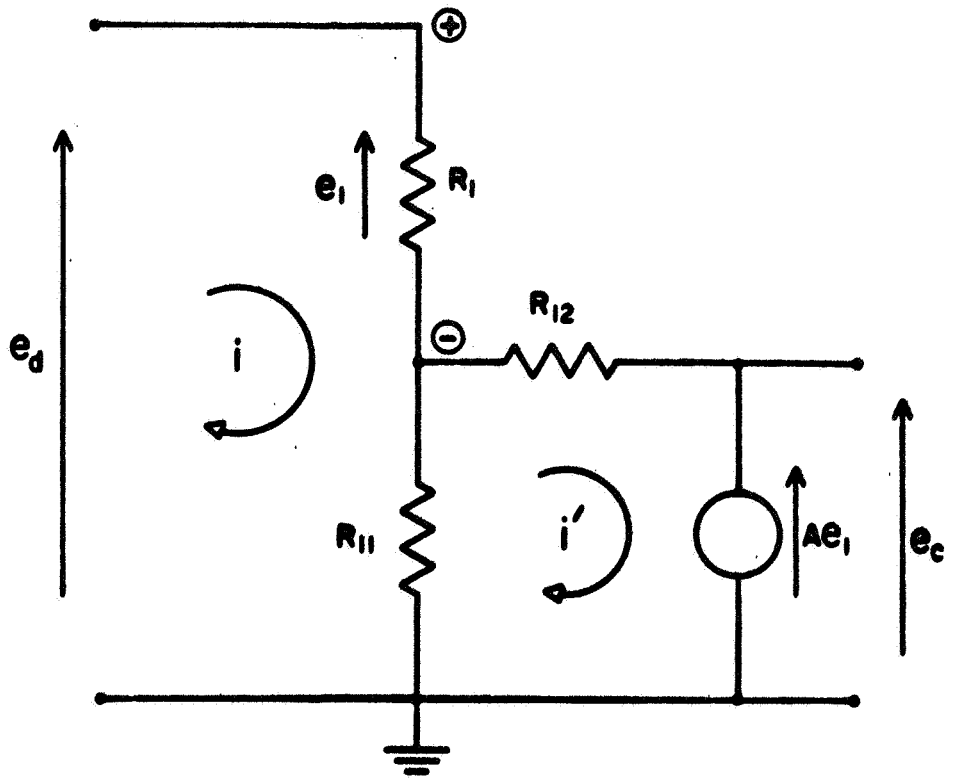

Fig. 2-3.--A circuit model of the input stage assuming a non-ideal operational amplifier.

These relations predict the performance of the input stage using a practical operational amplifier.

An operational amplifier for this application should have the following features: high input impedance; high open-loop voltage gain; low offset voltage; low quiescent power consumption; and a symmetric, bipolar output with ample voltage swing to drive the pulse-width modulator. Another desirable feature is a provision for external frequency compensation networks which may be used to alter the frequency response of the input stage. This makes it relatively easy to stabilize the complete amplifier.

The zener diodes, D_{11} and D_{12} in Fig. 2-1 limit the maximum output voltage of the amplifier, A_{11}. The phenomenon of latch-up is avoided by limiting the output of A_{11} to a value less than that which causes the input transistors of A_{11} to saturate. D_{11} and D_{12} should be chosen to have a zener voltage greater than the voltage needed to obtain maximum pulse width from the modulator, and less than the saturated output voltage of A_{11}. Diodes D_{13} and D_{14} limit the maximum voltage across the input terminals of A_{11}. This prevents damage to the input stage if extremely large voltages are applied to the input of the amplifier.

A characteristic of importance in the application of the operational amplifier is the offset voltage which is defined as that voltage required at the input of the open-loop amplifier to produce a zero output voltage. It has been shown in the literature that the offset voltage remains about the same when the amplifier is operated closed loop.[2] Thus, for an offset voltage of 1 mv and an input stage gain of 1000, it is expected

that the control signal (output of the input stage) would be about 1 volt. As will be shown in Chapter 3, the effect of this offset may be cancelled by proper adjustment of the modulator, if the control signal with zero input is less than two or three volts. However, the amplifier described in Chapter 9 employs a nulling circuit recommended by the manufacturer to eliminate the offset.

3. PULSE-WIDTH MODULATOR

The class-D amplifier output stage requires a driving signal which contains the information of the input signal and which will also cause the output transistors to switch quickly from saturation to cutoff. The modulator shown in Fig. 3-1 produces a pulse-width modulated signal which, after amplification in the driver stage, is applied to the output stage.

There are three basic types of pulse-width modulation. In one type the leading edge of the pulse is fixed at recurrent intervals and the trailing edge is modulated. In another type the trailing edge is fixed at recurrent intervals and the leading edge is modulated. In a third type both edges of the pulse are modulated. The modulator described herein uses double-edge modulation.

This modulator is composed of an astable multivibrator which generates a triangular waveform, and two comparators, one in each channel, which generate the pulse-width-modulated signal.

Three linear integrated-circuit operational amplifiers with symmetric bipolar outputs are used in the design.

In Fig. 3-1 A_{21} along with R_{23}, R_{24}, R_{25}, and C_{21} form an astable multivibrator which functions as a triangular waveform generator. Fig. 3-2 is a schematic diagram of this section of the modulator. The voltage waveforms of interest are shown in Fig. 3-3. Amplifier A_{21} has a very high gain and is driven into saturation when a very small difference

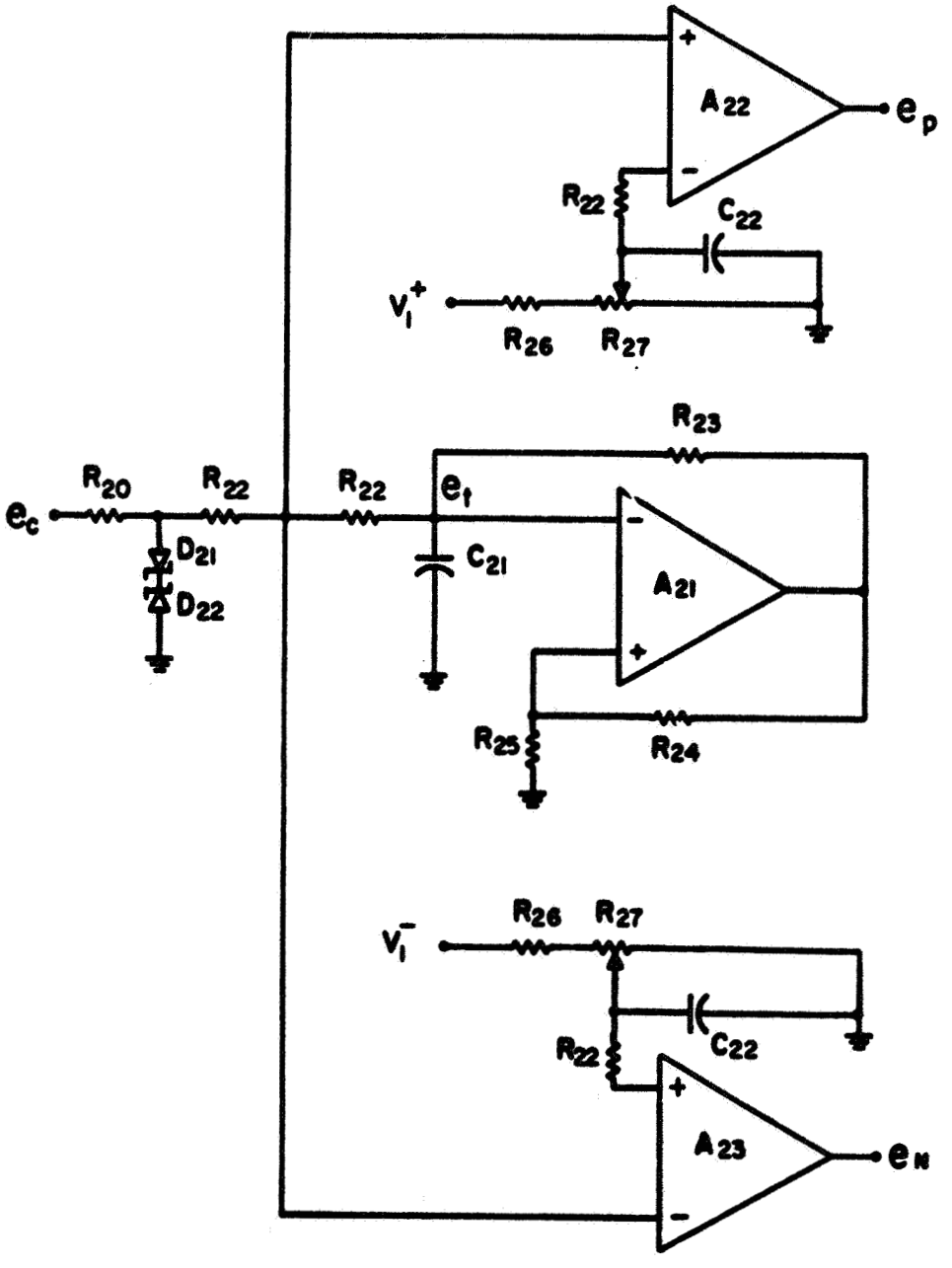

Fig. 3-1--Schematic diagram of the pulse-width modulator.

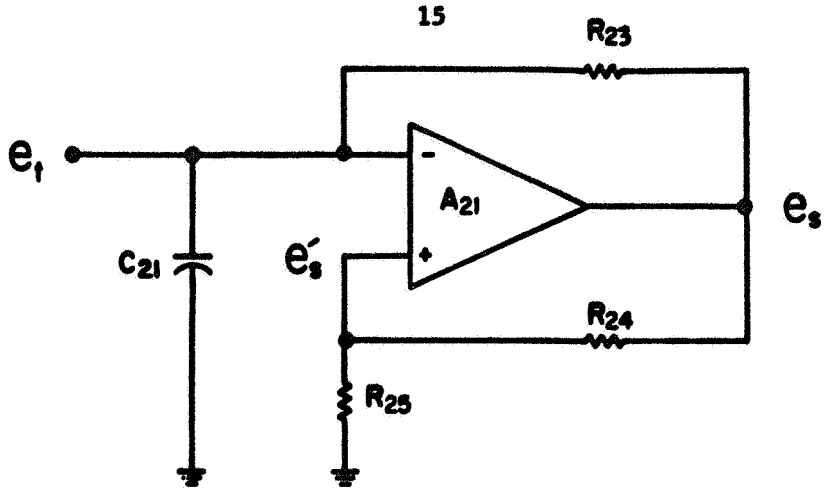

Fig. 3-2--Schematic diagram of the astable multivibrator.

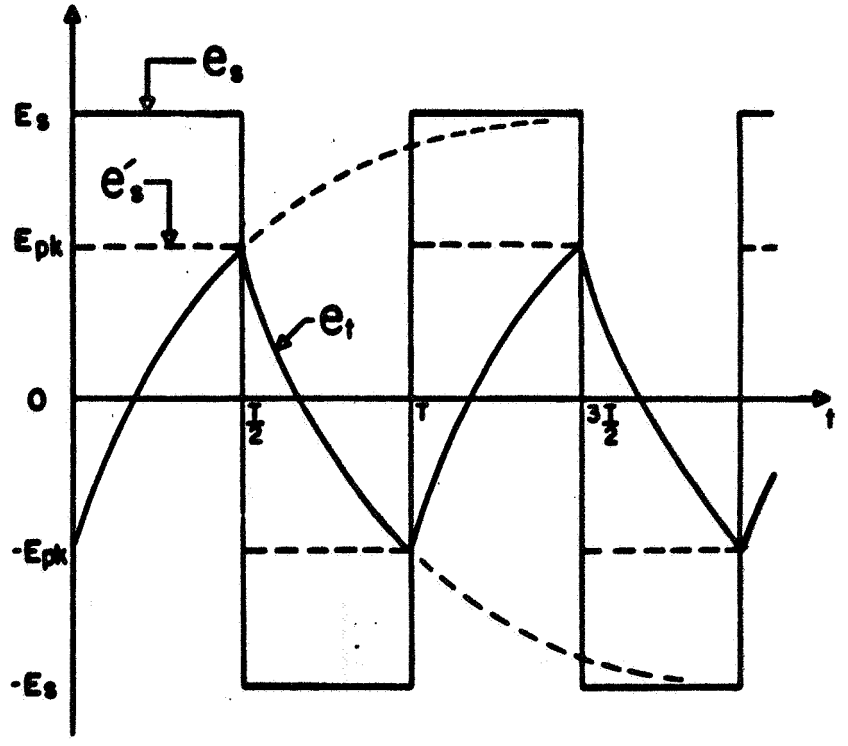

Fig. 3-3--Waveforms associated with the astable multivibrator.

in potential exists between its two inputs. The output voltage, e_s, of A_{21} is negative when the inverting input is positive with respect to the non-inverting input, and positive when the inverting input is negative with respect to the non-inverting input. The magnitude of the output voltage is E_s.

Assume that the oscillator has been operating a long time and that the output of A_{21} is positive at $+ E_s$ as shown at $t = 0$ in Fig. 3-3. A portion of the output voltage is fed back to the non-inverting input by the voltage divider composed of R_{24} and R_{25}. The voltage at the inverting input rises exponentially toward the output voltage at a rate determined by the time constant $R_{23} C_{21}$. When the voltage at the inverting input becomes positive with respect to that portion of the output voltage appearing at the non-inverting input, then the amplifier will quickly change states and the output becomes negative. The voltage on capacitor C_{21} now begins to approach $-E_s$, exponentially. The voltage on the capacitor continues to change until the non-inverting input is slightly positive with respect to the inverting input. Then the output voltage again changes states to $+ E_s$. This sequence repeats itself at a rate determined by the RC-time constant and the portion of the output voltage that is fed back to the non-inverting input. In this manner a triangular waveform of constant frequency is generated at the inverting input.

The frequency of the triangular-wave generator is derived as follows. Assume that the oscillator has reached steady-state operation and the output voltage has changed from negative to positive at $t = 0$. For the period of oscillation T, the triangular waveform for $0 \leq t \leq T/2$

is given by

$$e_t(t) = \frac{-R_{25}\, E_s}{R_{24} + R_{25}} + \left(1 + \frac{R_{25}}{R_{24} + R_{25}}\right) E_s \left(1 - \epsilon^{-\frac{t}{R_{23}\, C_{21}}}\right) \tag{3-1}$$

and for $T/2 \leq t \leq T$,

$$e_t(t) = \frac{R_{25}\, E_s}{R_{24} + R_{25}} - \left(1 + \frac{R_{25}}{R_{24} + R_{25}}\right) E_s \left(1 - \epsilon^{-\frac{t}{R_{23}\, C_{21}}}\right). \tag{3-2}$$

The derivation of these expressions assumes that the input impedance of A_{21} is infinite.

For simplicity in later derivations we define the voltage division factor, K, using

$$\frac{R_{25}}{R_{24} + R_{25}} = \frac{1}{K}. \tag{3-3}$$

Also,

$$E_{pk} = \frac{R_{25}}{R_{24} + R_{25}}\, E_s = \frac{E_s}{K} \tag{3-4}$$

where E_{pk} is the peak value of the triangular waveform. Using (3-3) and (3-4), (3-1) and (3-2) become, for $0 \leq t \leq T/2$,

$$e_t(t) = K\, E_{pk} - E_{pk}(K + 1)\, \epsilon^{-\frac{t}{R_{23}\, C_{21}}}, \tag{3-5}$$

and for $T/2 \leq t \leq T$,

$$e_t(t) = -K E_{pk} + E_{pk} (K + 1) \epsilon^{-\frac{t}{R_{23}C_{21}}} . \qquad (3\text{-}6)$$

The period of oscillation is determined from (3-5) at $t = T/2$ we know that $e_t(T/2) = E_{pk}$. This yields

$$T = 2 R_{23} C_{21} \ell n \left(\frac{K + 1}{K - 1} \right) . \qquad (3\text{-}7)$$

Therefore the frequency of oscillation of the multivibrator is,

$$f_s = \frac{1}{2 R_{23} C_{21} \ell n \left(\frac{K + 1}{K - 1} \right)} . \qquad (3\text{-}8)$$

Referring to Fig. 3-1, amplifiers A_{22} and A_{23} function as comparators for the P-channel and N-channel respectively. Fig. 3-4 presents the basic comparator circuit for the P-channel. The waveforms associated with its operation are shown in Fig. 3-5. For purposes of discussing the operation of the comparators, the triangular waveform $e_t(t)$ is assumed to be perfectly triangular.

The $e_t(t)$ is summed with the control signal, $e_c(t)$ from the input stage, according to (3-9) below, and applied to the non-inverting input of A.

$$e_m(t) = \frac{R_c}{R_t + R_c} e_t(t) + \frac{R_t}{R_t + R_c} e_c(t) \qquad (3\text{-}9)$$

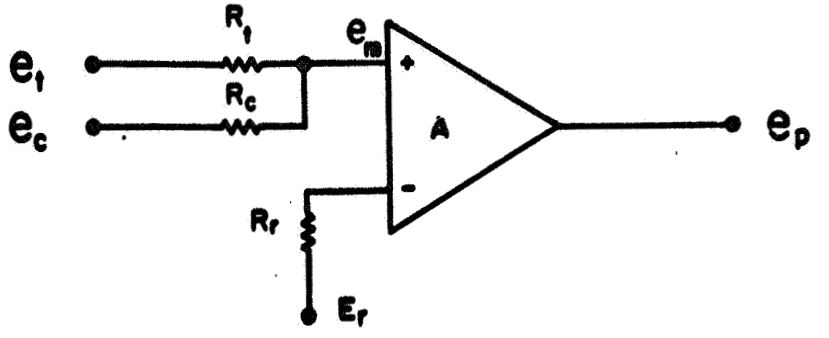

Fig. 3-4.--Schematic diagram of the basic comparator circuit.

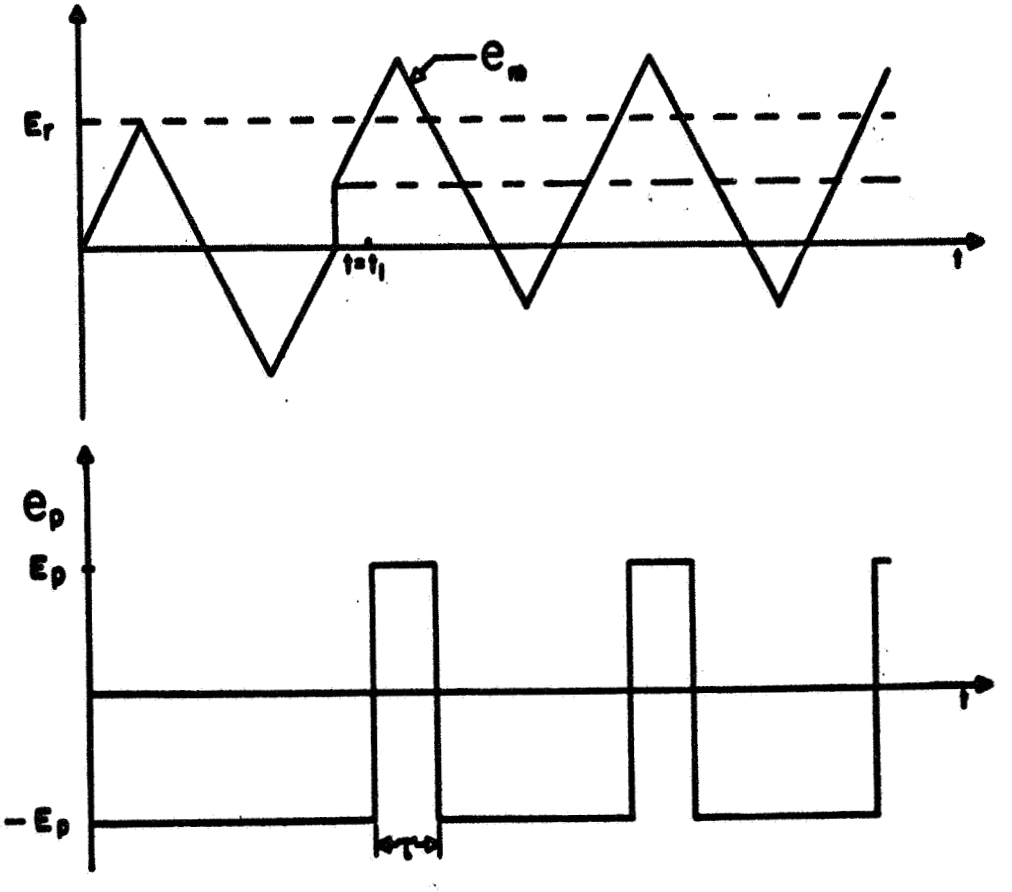

Fig. 3-5.--Waveforms associated with the operatio the comparator circuit.

A positive reference voltage, E_r, is applied to the inverting input of A through R_r. When $e_m(t)$ is positive with respect to E_r, the output of A is $+E_p$. When $e_m(t)$ is negative with respect to E_r, the output of A is $-E_p$. If the reference voltage is adjusted so that it is slightly greater than the peak of $e_m(t)$ with the control voltage $e_c(t) = 0$, then the output of A is a constant, $-E_p$, as shown to the left of $t = t_1$ in Fig. 3-5.

If $e_c(t)$ is a voltage step applied at $t = t_1$ as in Fig. 3-5, then the voltage at the non-inverting input, $e_m(t)$, is positive with respect to the reference, E_r, for a length of time, τ, which is proportional to the magnitude of the voltage step. Therefore, the output of A is $+E_p$ for the length of time that $e_m(t) > E_r$ and $-E_p$ for all other time. Pulse-width modulation is accomplished since the magnitude of the control signal, e_c, determines the width of pulses appearing at the output of A. The N-channel operates in a similar manner with the exception that a negative reference is applied to the non-inverting input and the control signal summed with the triangular waveform is applied to the inverting input. Both channels then produce positive pulses.

When a positive control signal is present, the N-channel output remains a constant negative voltage. Similarly, for negative inputs, the P-channel output remains negative.

It should be noted that in the complete schematic of the modulator, shown in Fig. 3-1, all redundant summing resistors in the comparator section were eliminated. The remaining summing resistors are equal, with the symbol R_{22}. Under these conditions, and assuming that R_{20} and

the output resistance of the input stage are both smaller than R_{22}, (3-9) becomes

$$e_m(t) = \frac{1}{2} e_t(t) + \frac{1}{2} e_c(t). \qquad (3\text{-}10)$$

The reference voltages are derived from the voltage divider networks composed of R_{26} and R_{27}. The capacitors labelled C_{22} are used to maintain a constant reference voltage. Zener diodes D_{21} and D_{22} limit the control signal, e_c, and hence limit the maximum pulse width. This is a necessary feature which prevents the output stage from being driven beyond the maximum designed pulse width. Resistor R_{20} serves as a current limiter when the zener voltage is exceeded.

It may be readily deduced that there exists a relationship between the magnitude of the triangular waveform and the "gain" of the modulator. Referring to Fig. 3-5, if $e_t(t)$ is assumed perfectly triangular, then the pulse width τ is given by,

$$\tau = \left(\frac{T R_t}{2E_r (R_t + R_c)} \right) e_c. \qquad (3\text{-}11)$$

Note that if a greater pulse width is obtained for a given control voltage, e_c, then an increase in the open loop gain for the overall amplifier will result, since the overall amplifier output is proportional to the pulse width. Thus, attenuating the triangular waveform and correspondingly reducing the reference voltage, E_r, results in an increase in the ratio $\frac{\tau}{e_c}$. Therefore, the open loop gain of the complete

amplifier may be varied quite easily in the modulator.

A condition can exist in the amplifier for which small input signals do not cause the modulator to produce pulses in either channel. This is called dead-zone. This condition is caused by improper adjustment of the modulator. This is illustrated in Fig. 3-6. If E_r is made greater than the peak value of $e_m(t)$ when $e_c = 0$, then a dead-zone results. That is, for control voltages less than the difference between E_r and $e_m(t)$ when $e_c = 0$, no output pulse is produced.

Normally the reference level is adjusted to equal the peaks of the triangular waveform, $e_m(t)$, when the control voltage is zero. However, if the input stage produces an off-set voltage (as discussed in Chapter 2), then the reference level can be adjusted to compensate for the off-set. Fig. 3-7 shows the modulator waveforms when the input stage causes a positive off-set. Under open loop conditions a series of pulses is produced with zero voltage applied to the input stage.

In Fig. 3-8 the reference, E_r, has been adjusted to a new value, E_r', in order to compensate for the off-set of the input stage. No pulses are now produced with zero input to the input stage. Of course, a similar adjustment of the N-channel reference voltage would also be required.

The linearity of the modulator is dependent on the waveshape of the triangular waveform, $e_t(t)$, and the constancy of the reference voltage. Referring to Fig. 3-3 and recalling the discussion of the astable multivibrator, one sees that $e_t(t)$ is composed of excursions along an exponential curve which is the potential on capacitor C_{21}. The portion of the output of A_{21} that is fed back to the noninverting input,

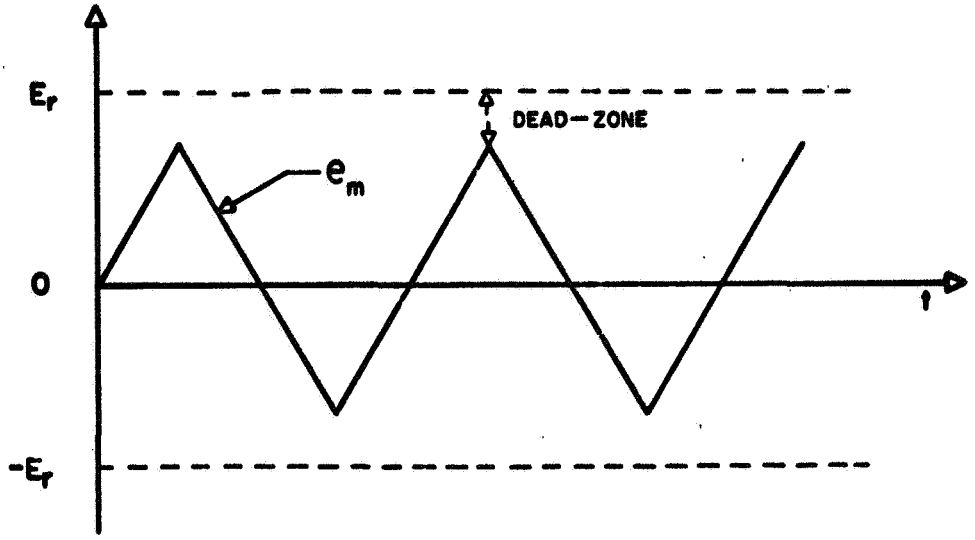

Fig. 3-6--Waveforms in the modulator when the reference voltage is adjusted to produce a dead zone.

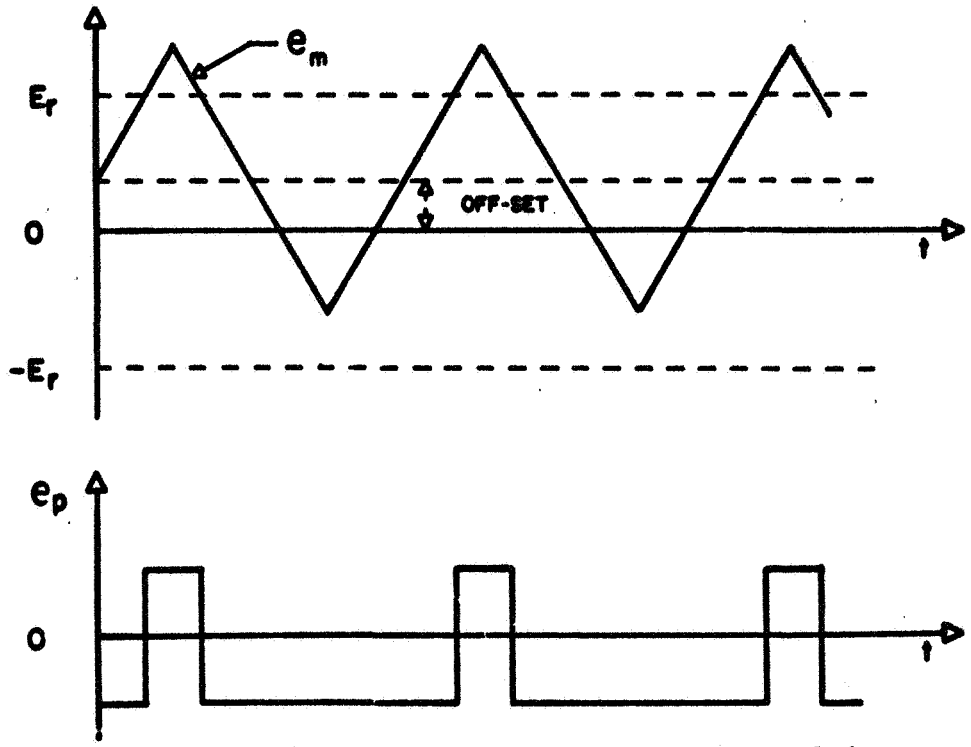

Fig. 3-7--Waveforms in the modulator when off-set of the input stage causes erroneous pulses.

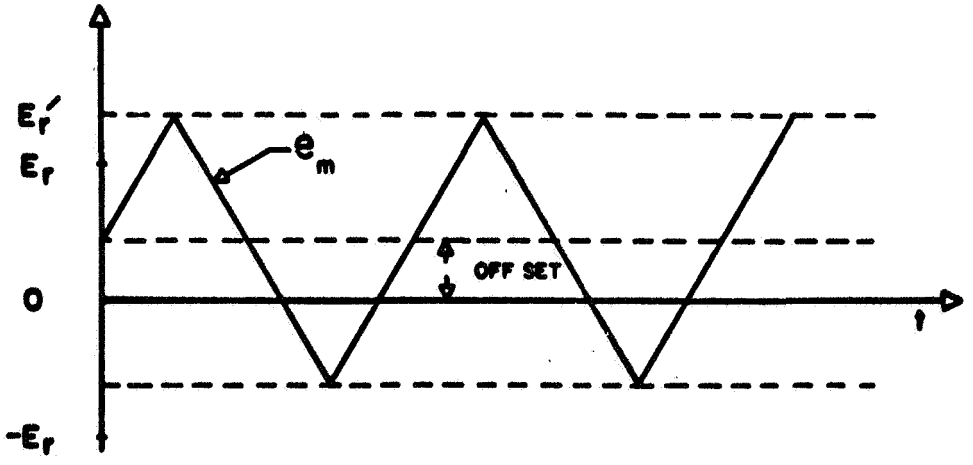

Fig. 3-8--Waveforms in the modulator when the reference is adjusted to compensate for the off-set of the input stage.

$\frac{R_{25}}{R_{24}+R_{25}} = \frac{1}{K}$, determines the peak voltage reached by $e_t(t)$. As R_{24} and R_{25} are chosen such that the peak of $e_t(t)$ becomes smaller in comparison to E_s, then the excursions of $e_t(t)$ become better approximations of straight lines. This provides improved linearity. Using (3-5), (3-6), and (3-7), an expression is obtained for the exact pulse-width, τ, as a function of the control voltage e_c.

$$\tau = R_{23} C_{21} \ell n \left(\frac{K + 1}{K - 1} \right) \left[\frac{(K - 1) E_r + K' e_c}{(K + 1) E_r - K' e_c} \right] \qquad (3\text{-}12)$$

where $K' = \frac{Rc}{R_c+R_t}$ in Fig. 3-4. For the schematic shown in Fig. 3-1, K' reduces to $K' = 1/2$ since the resistors corresponding to R_c and R_t (R_{22}) are chosen equal.

If an error function is defined as the difference in the actual pulse width and the pulse-width obtained if a perfect triangular waveform were used, then this error, α, is given by

$$\alpha = \frac{TK'e_c}{2E_r} - R_{23}C_{21} \ell n \left(\frac{K + 1}{K - 1} \right) \left[\frac{(K+1) E_r + K'e_c}{(K-1) E_r - K'ec} \right] . \qquad (3\text{-}13)$$

Percent error is

$$\alpha' = \frac{2 \alpha E_r}{T K' e_c} (100\%) . \qquad (3\text{-}14)$$

This is an expression of the percent error as a function of the parameters K and e_c. All other variables are determined by the selected frequency of oscillation and other considerations. The larger the value of K

selected, the smaller the excursions on the exponential curve and, in general, the more linear the pulse-width modulation. However, if the triangular waveform is made too small, adjustment of the reference voltages and the maximum pulse width becomes difficult. The percent error is generally greatest for small values of the control voltages. Using (3-14) the percent error may be checked over the range of expected control voltages for a given value of K. The largest value of K that provides an acceptable percent error should be used in order to simplify adjustment of the modulator. For most applications letting K = 3 yields satisfactory results with α exceeding 3% only for relatively small values of e_c. With negative feedback around the complete amplifier, the effect of this error is negligible.

4. DRIVER STAGE

The driver stage of the amplifier amplifies the pulse-width modulated signal to a level sufficient to drive the output stage transistors. It provides a sufficient level of drive to keep the output transistors in saturation for the duration of each pulse and provides a waveform that will cause the output transistors to switch quickly, resulting in efficient operation.

For brevity only one channel of the driver stage is described in this chapter. As noted in Chapter 1, however, two separate channels are required to produce a bipolar output signal. A given driver stage will then require two independent driver circuits.

For the purpose of describing the driver circuit, it is assumed that the output stage is in the simplified form given in Fig. 4-1. This simplified circuit is an accurate representation of the output stage for only one switching cycle, because the actual output circuit incorporates a circuit which returns the inductor current to zero at the end of each cycle. The complete output stage is presented in Chapter 5. The important point to be understood is that when the output transistor is driven into saturation ("on"), the collector current is a ramp due to the inductor L_4. Since the collector current is quite small during the turn-on interval, very little power is dissipated during this transition. Thus the only switching interval which contributes appreciably to power loss is the turn-off interval. Each of the driver circuits to be discussed

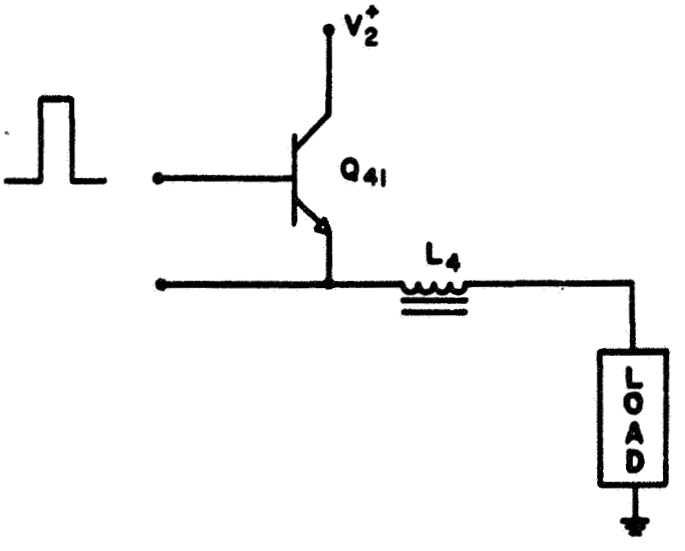

Fig. 4-1--Schematic diagram of a simplified circuit for the P-channel of the output stage.

uses rapidity of turn-off as a criterion for judging performance.

The collector current transients at turn-off are often described in terms of the storage delay time, t_s, and the fall time, t_f. These two parameters are defined pictorially in Fig. 4-2. The storage delay time, t_s, is the time interval required for the transistor to respond to the trailing edge of the driving pulse. The fall time is the time required for the collector current to fall from 90 percent to 10 percent of the saturated state value. The storage delay time and the fall time can be shortened considerably by various methods. Circuit techniques that will reduce one of these time delays will reduce the other also.

When a transistor is operating in the saturated state, the base current is usually greater than the minimum value required to saturate the transistor. This results in storage of excess minority carriers in the base region during the "on" interval. The excess minority carriers in the base must be eliminated before the collector current can begin to fall in magnitude. The elimination of excess minority carriers may be accomplished in several ways. First, if the base is open-circuited, then the excess minority carriers in the base will recombine with excess majority carriers at an exponential rate which depends upon the recombination tendency of these excess stored carriers. An alternative is to provide a reverse base current, since it will partly consist of excess minority carriers flowing back into the emitter region. For this case the storage time will decrease with increased reverse base drive. Yet another method is to short-circuit the base and emitter. This results in a redistribution of charge resulting in a return to quiescent conditions. A speed-up capacitor in parallel with the base resistor may be used to create a

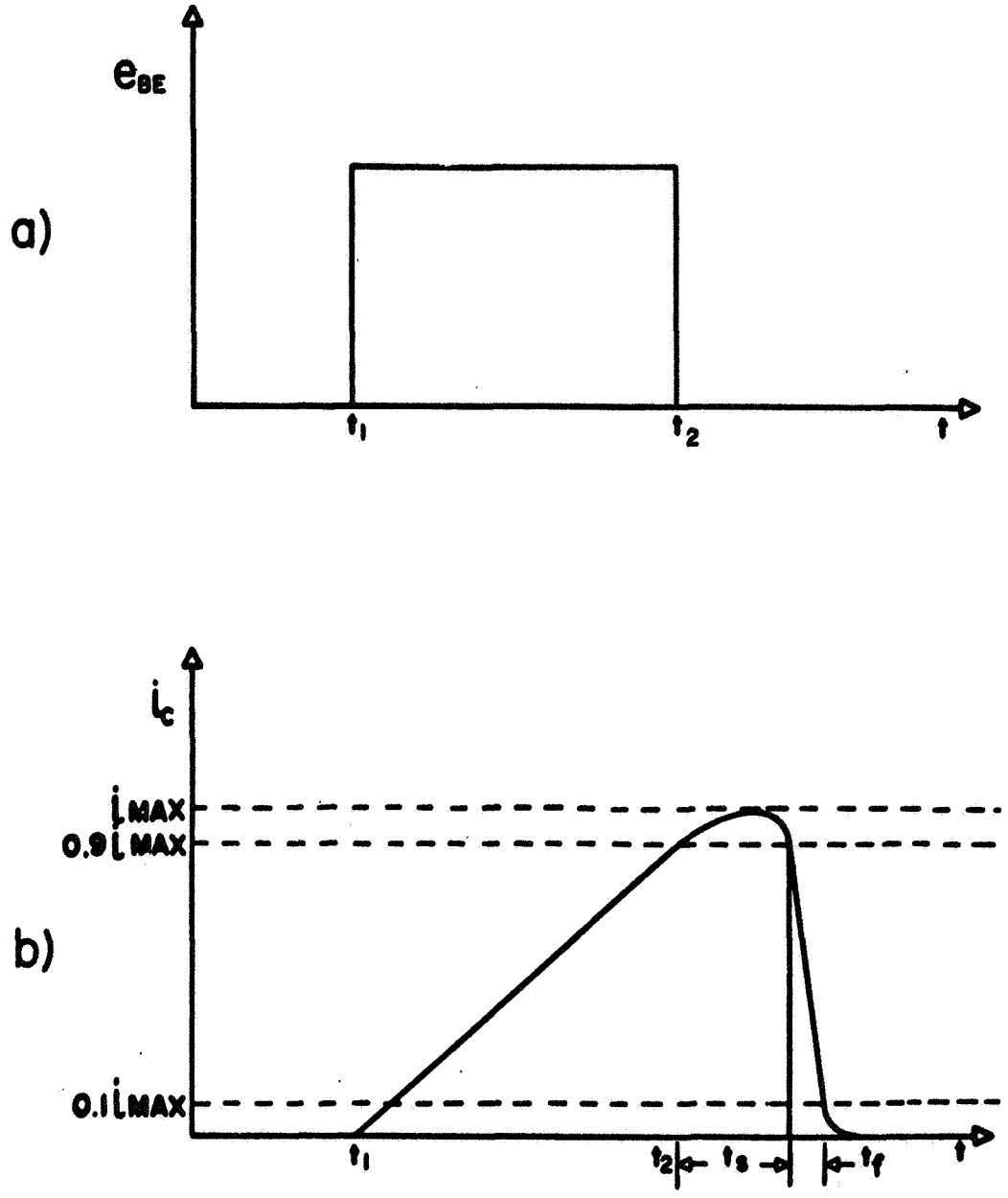

Fig. 4-2--The base-emitter voltage waveform (a), and the collector current waveform (b) for the output transistor.

reverse base drive at turn-off. The capacitor should be selected such that the charge developed on the capacitor is greater than the total excess charge stored in the base. This is usually done experimentally. When the driving voltage drops, the capacitor discharges, quickly removing the excess carriers. This reduces both the storage delay time and the fall time. A direct-coupled driver circuit using a speed-up capacitor is shown in Fig. 4-3. Only one channel is shown. Complimentary symmetry could be used to develop a similar channel for bipolar d-c output voltages.

The effectiveness of this circuit in providing efficient switching is largely determined by the output transistors used. Generally, transistors with low maximum current ratings have lower t_s and t_f than the higher current units. With low-current transistors in the output stage the circuit in Fig. 4-3 will provide reasonably fast turn-off. However, presently available high-current transistors cannot be switched efficiently using the circuit of Fig. 4-3.

A second approach to the problem of achieving fast switching of the output transistors is to employ transformer coupling. Fig. 4-4 shows one channel of a transformer-coupled driver. When the driver transistor, Q_{31}, is driven into saturation by the modulator, a pulse is coupled to the base of Q_{41}. When Q_{31} is driven off by the modulator, a transient condition exists in the transformer which results in a reverse base drive voltage spike which appears at the secondary terminals. This reverse spike removes the excess charge stored in the base of output transistor Q_{41}. The use of speed-up capacitors C_{31} and C_{41} also aids in quickly turning off the driver and output transistors, as discussed previously.

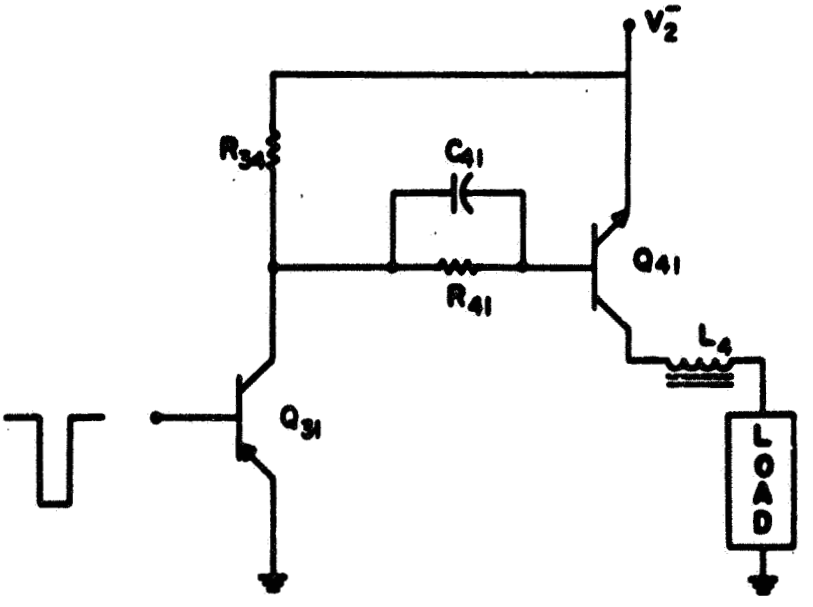

Fig. 4-3--Schematic diagram of a direct-coupled driver and simplified output circuit.

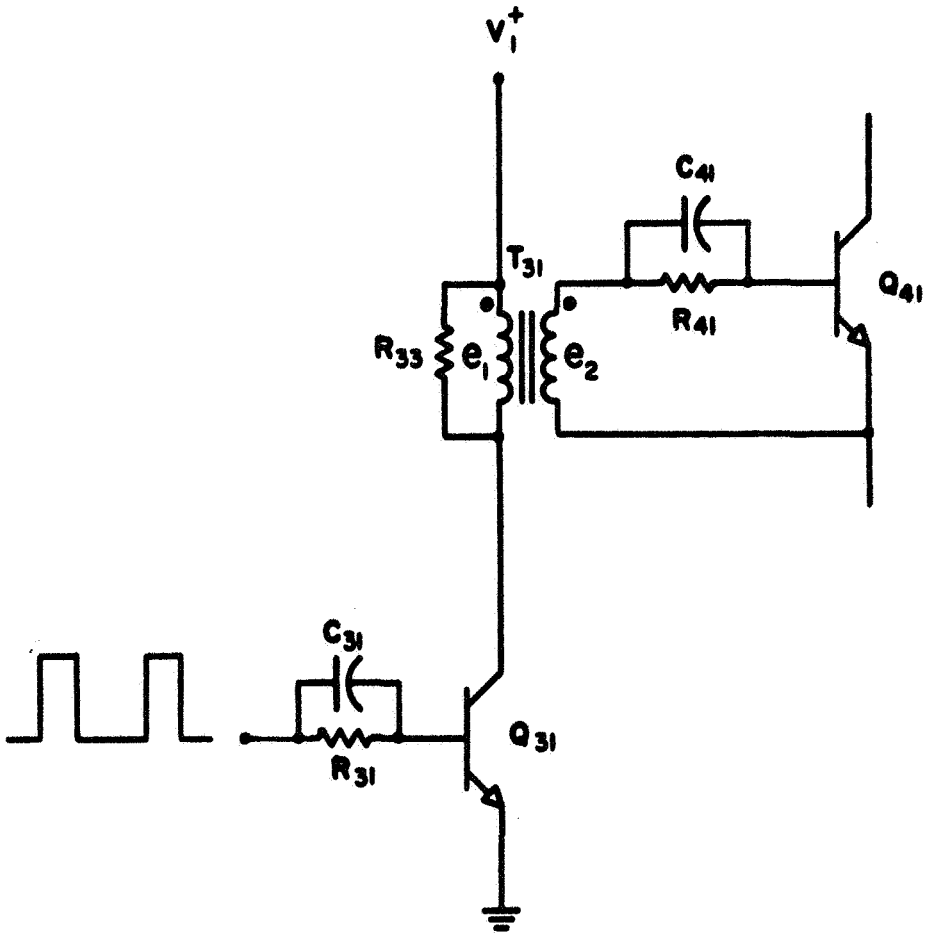

Fig. 4-4--Schematic diagram of a transformer-coupled driver stage.

Transformer coupling allows the use of the same type power transistors for both the N and P-channels, where the previous direct-coupled design required complimentary transistor types. This assures similar performance of the two channels. The circuit presented in Fig. 4-4 has been used successfully in each channel of the basic amplifier with high quality output transistors having peak collector currents up to 10 amperes.

The transformer-coupled circuit of Fig. 4-4 may prove to be inadequate in effecting efficient turn-off of power transistors rated at more than 10 amperes, as higher-rated units often have correspondingly greater minority-carrier storage. Also, if economy dictates the use of slower, less expensive transistors in the output stage, some other form of turn-off may be necessary.

A third driver circuit which provides efficient switching is shown in Fig. 4-5. This circuit is basically the same as the transformer-coupled circuit of Fig. 4-4. However, an extra winding has been added to transformer T_{31} to be used as a "shorting" circuit. When the output of the modulator is positive, transistor Q_{32} is not conducting and a positive pulse is delivered to the base of Q_{41} as before. When the modulator output goes negative, Q_{31} is turned off and Q_{32} is driven into saturation. However, at this time the transient condition in the transformer causes diode D_{31} to be reverse-biased. When this transient dies out, D_{31} becomes forward-biased and the base and emitter of Q_{41} are essentially short-circuited. The charge stored in the base of Q_{41} is quickly removed, allowing the transistor to switch quickly. Note that this technique requires no additional power from the power supply, and uses two of the

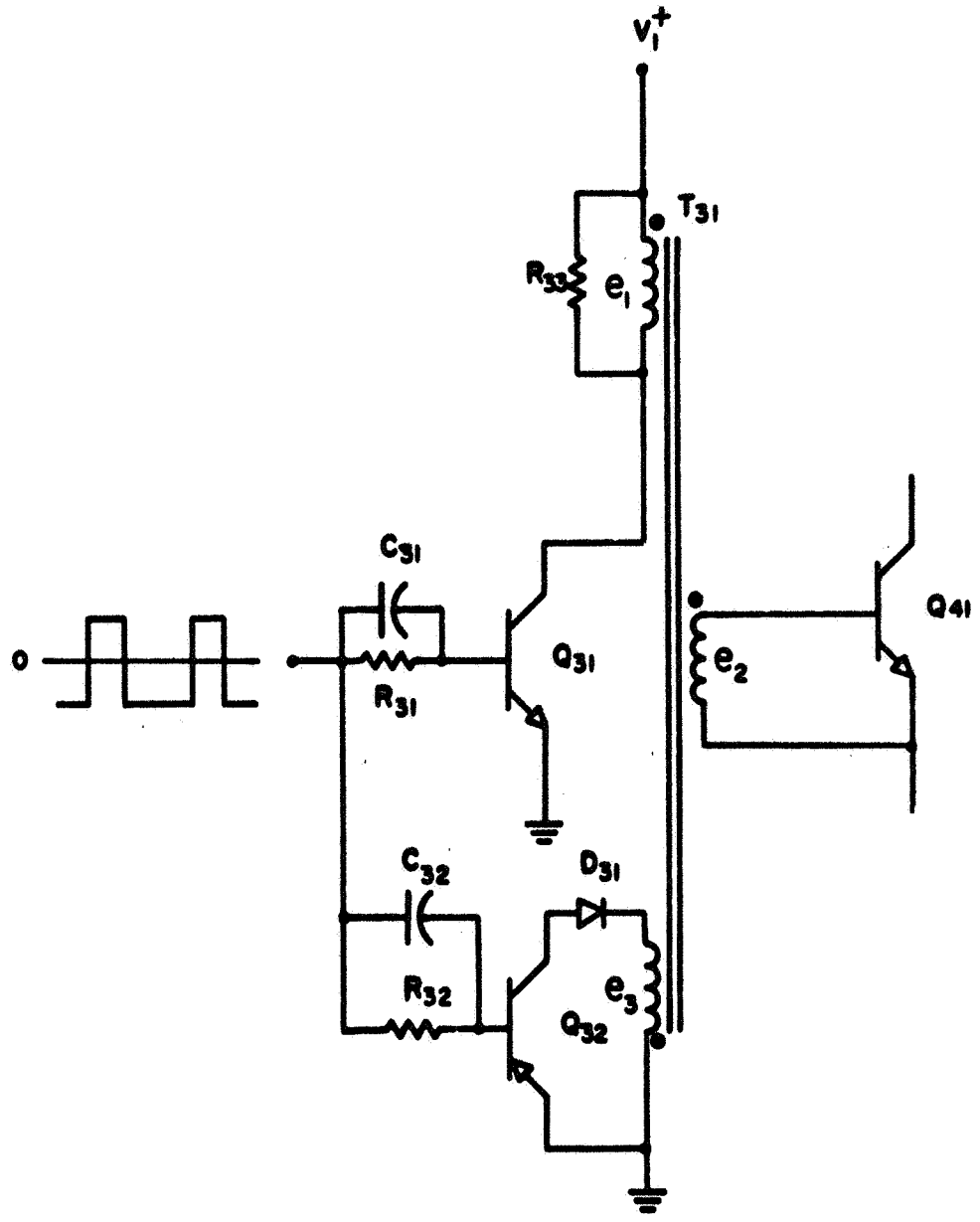

Fig. 4-5--Schematic diagram of a transformer coupled driver circuit with a "shorting circuit."

turn-off techniques in sequence.

Amplifiers designed to produce over 100 watts maximum d.c. power output have been built using this type of driver circuit. Efficiencies improved from 3 to 6 percent over a transformer-coupled driver stage without the shorting circuit.

The success of this driver circuit depends on the design of the transformer. The transformer design should dictate core material and size, turns ratio, inductance requirements, and wire sizes. Powdered-permalloy toroidal cores were used for the driver transformers. Core material and permeability were selected to give a high Q at the switching frequency. Refer to Fig. 4-4, the basic transformer-coupled driver circuit. To determine the driver transformer turns ratio, $\frac{N_1}{N_2}$, one must first know the base-emitter voltage and the base-current required to keep the output transistor in saturation at the time of maximum collector current. (These quantities are designated V_{BE} and I_B.) R_{41} may be selected to be some convenient value, approximately equal to $\frac{V_{BE}}{I_B}$. Then the voltage appearing at the secondary of the driver transformer must be,

$$e_2 = V_{BE} + I_B R_{41}. \tag{4-1}$$

Also, for Fig. 4-4, when Q_{31} is saturated

$$\frac{N_1}{N_2} = \frac{e_1}{e_2} = \frac{V_1}{e_2}, \text{ so,} \tag{4-2}$$

$$\frac{N_1}{N_2} = \frac{V_1}{V_{BE} + I_B R_{41}} \tag{4-3}$$

The number of turns required for the auxiliary "shorting winding", shown in Fig. 4-5, is not critical. However, since the voltage that appears at the secondary of the driver transformer is the base-emitter saturation voltage of Q_{41} which is usually between 1.0 and 1.5 volts, the ratio of the number of shorting winding turns to the number of transformer secondary turns should be greater than one to assure that the voltage appearing across the shorting winding will exceed the threshold voltage of the diode D_{31}, when the shorting circuit is in operation. The resistors R_{31} and R_{32} are determined by the output of the modulator and the transistors chosen for Q_{31} and Q_{32}.

$$R_{31} = \frac{E_D + V_{BE}}{I_B} \tag{4-4}$$

where V_{BE} and I_B refer to Q_{31}. Similarly,

$$R_{32} = \frac{-E_D + V_{BE}}{I_B} \tag{4-5}$$

where V_{BE} and I_B refer to Q_{32}. Note that V_{BE} and I_B are negative quantities for a PNP transistor.

It is preferred that the pulse transformer have large primary and secondary inductances in order to transfer the driving pulse with little distortion. An analysis of the transformer equivalent circuit as shown in Fig. 4-6 will yield a relation between component values and expected performance. The pulse source is approximated by an ideal source and switch with series resistor, R_s. In Fig. 4-6(b) the source is referred

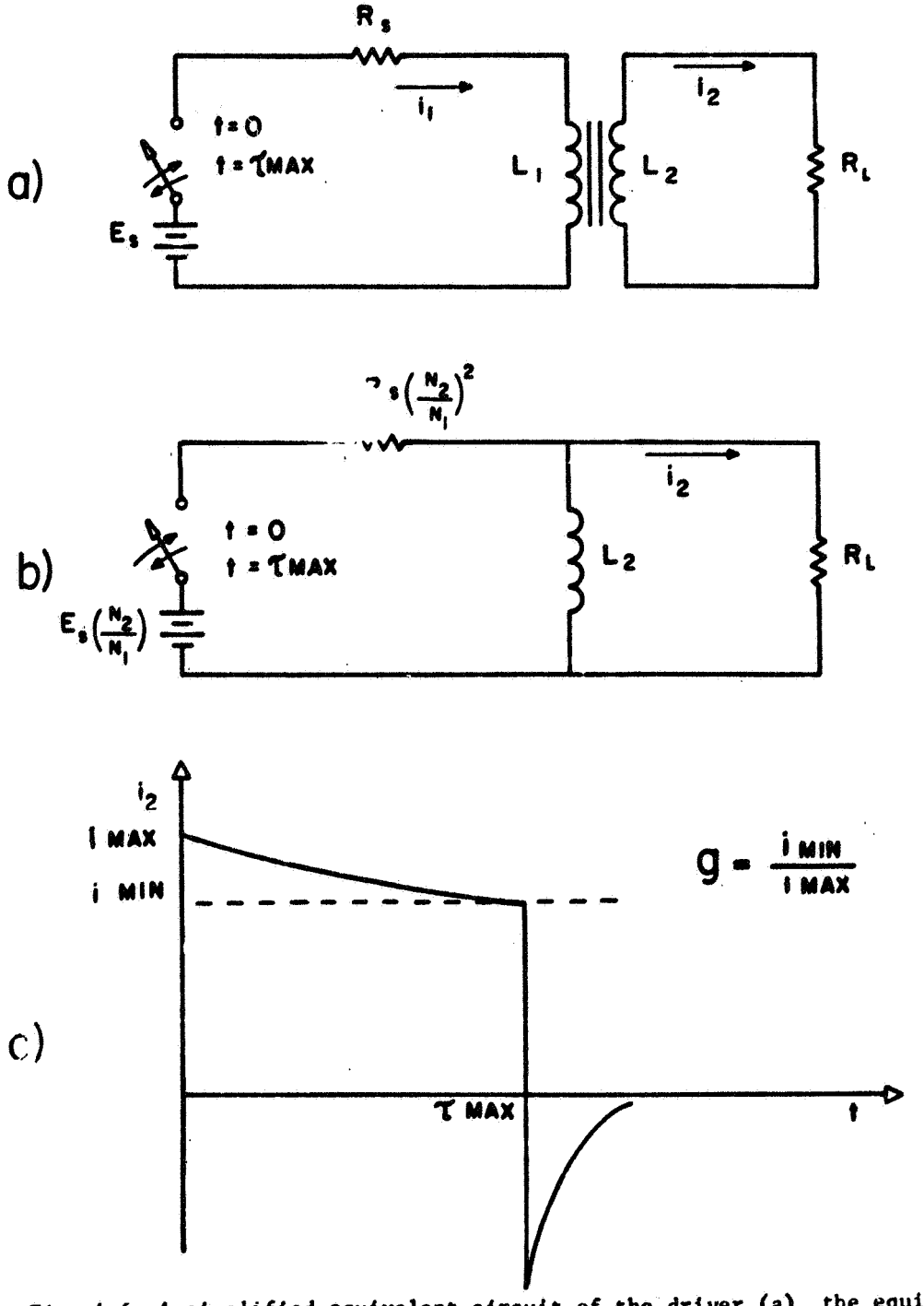

Fig. 4-6--A simplified equivalent circuit of the driver (a), the equivalent circuit referred to the secondary (b), and the load-current waveform (c).

to the secondary. Leakage inductance and winding resistance have been neglected as well as winding capacitance. The magnetizing inductance is approximately equal to L_2, the secondary inductance. The current i_2, delivered to the load is of interest. The ratio of minimum to maximum current in each pulse is designated g, as defined by Fig. 4-6 (c) and can be used as a measure of the ability of the transformer to sustain a pulse. For $0 \leq t \leq \tau_{max}$, the secondary current is given by

$$i_2 = \frac{E_s\left(\frac{N_2}{N_1}\right)}{R_L + R_s\left(\frac{N_2}{N_1}\right)^2} \epsilon^{-\frac{R_L R_s\left(\frac{N_2}{N_1}\right)^2 t}{L_2\left[R_L + R_s\left(\frac{N_2}{N_1}\right)^2\right]}}. \qquad (4\text{-}6)$$

The current ratio, g, is therefore

$$g = \frac{i_2(\tau_{max})}{i_2(0^+)} \qquad (4\text{-}7)$$

where τ_{max} is the maximum pulse width to be encountered. This may be written as

$$g = \epsilon^{-\frac{\tau_{max}}{L_2\left[\frac{1}{R_s}\left(\frac{N_1}{N_2}\right)^2 + \frac{1}{R_L}\right]}}. \qquad (4\text{-}8)$$

In designing a transformer the parameter g should be specified, indicating the maximum allowable decay of the secondary current. From (4-8) the required secondary inductance, L_2, may be obtained in terms of $\frac{N_1}{N_2}$, τ_{max}, g, R_s, and R_L, all of which are either specified or determined by other circuit requirements. Solving for L_2 we have,

$$L_2 = \frac{\tau_{max}}{\left(\ell n \frac{1}{g}\right)\left[\frac{1}{R_s}\left(\frac{N_1}{N_2}\right)^2 + \frac{1}{R_L}\right]}$$

For the circuit of Fig. 4-4,

$$R_s = R_{SAT}$$

$$R_L = R_{41} + \frac{V_{BE}}{I_B}$$

where R_{SAT} is the collector-emitter saturation resistance of the driver transistor and I_B is the current required to keep the output transistor in saturation at maximum collector current. Thus,

$$L_2 = \frac{\tau_{max}}{\left(\ell n \frac{1}{g}\right)\left[\frac{1}{R_{SAT}}\left(\frac{N_1}{N_2}\right)^2 + \frac{1}{R_{41} + \frac{V_{BE}}{I_B}}\right]} \quad . \tag{4-9}$$

Also of interest is the peak primary current. By referring the load, R_L in Fig. 4-6(a), to the primary, a derivation of i_1 for $0 \leq t \leq \tau_{max}$ yields

$$i_1(t) = \frac{E_s}{R_s + R_L\left(\frac{N_1}{N_2}\right)^2} \epsilon^{-\frac{R_s R_L \left(\frac{N_1}{N_2}\right)^2 t}{\left[R_s + \left(\frac{N_1}{N_2}\right)^2 R_L\right] L_1}} + \frac{E_s}{R_s} - \frac{E_s}{R_s} \epsilon^{-\frac{R_s R_L \left(\frac{N_1}{N_2}\right)^2 t}{\left[R_s + \left(\frac{N_1}{N_2}\right)^2 R_L\right] L_1}} \quad . \tag{4-10}$$

The maximum value of i_1 occurs at $t = \tau_{max}$ and may be found from (4-10) by making the following substitutions,

$$R_s = R_{SAT} ,$$

the collector-emitter saturation resistance of Q_{31}, and

$$R_L = R_{41} + \frac{V_{BE}}{I_B} ,$$

where V_{BE} and I_B refer to Q_{41} for maximum designed collector current.

Thus, an acceptable driver transformer may be designed using (4-3) to determine the turns ratio, and (4-9) to determine the secondary inductance, while the peak primary current may be determined using (4-10). The required base resistors may be determined using (4-4) and (4-5).

Three driver circuits have been presented here. The simplest circuit utilizes direct coupling with a speedup capacitor used to improve turn-off. This circuit is suitable for low-power applications. The second circuit discussed uses transformer coupling. This circuit should be used when the storage time and the fall time of the output transistors have a significant effect on switching efficiency. For amplifiers designed to produce over 100 watts, it may prove advantageous to use the third circuit described. The third design uses transformer coupling with an additional winding used in a "shorting" circuit. Although the circuit produces an improvement in efficiency, in some applications the designer may not feel that this improvement warrants the additional circuitry required. The degree of improvement and the value of the shorting circuit should be determined

for the particular amplifier under consideration. The design example in Chapter 9 utilizes the third design.

5. OUTPUT STAGE

The cutput stage must perform two functions. First, it must produce power amplification of the pulse-width-modulated signal from the driver. Secondly, the output stage must demodulate the pulse-width-modulated signal to produce an output signal which is as nearly identical as possible to the original input signal. For this latter function the load may be used to provide some filtering.

A very simple output circuit which would perform both of these functions is shown in Fig. 5-1. The driver circuit produces a pulse-width-modulated signal of sufficient magnitude to drive Q_{41} into saturation for the duration of each pulse. When Q_{41} is in saturation the load is essentially connected to the power supply, V_2^+. The result is that the time-averaged power delivered to the load is proportional to the signal at the input of the overall amplifier. If the pulse (or switching) frequency is reasonably high and if the inductive component of the load is sufficiently large then the inductive component of the load will produce sufficient filtering of the output pulse signal. This technique may be adequate for loads such as motors.

Of course, the circuit of Fig. 5-1 will produce only positive output voltages. A bipolar output would require another driving signal, and another output transistor operating from a negative supply to the load.

There are several drawbacks to this circuit. Losses in the transistor, during the switching interval, are relatively large. The efficiency of the circuit is often less than could be obtained with a class-B circuit. Large voltage spikes (due to the inductor) at the collector require high

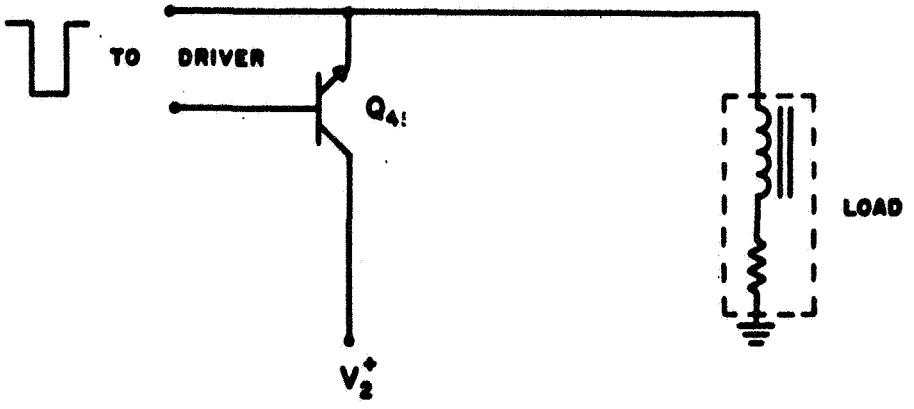

Fig. 5-1--Schematic diagram of one channel of a simple output circuit.

voltage transistors or some means of suppression. While the inductive load may be designed to provide adequate filtering, some high-frequency roll-off is inevitable.

Fig. 5-2 shows the basic class-D output circuit developed. This circuit incorporates two important features. The first feature is a clamping diode, D_{41}, ahead of the inductor, L_4. When Q_{41} is driven "on", D_{41} is reverse-biased, current flows in the inductor, and energy is stored in the magnetic field of the inductor. When Q_{41} is driven "off", the voltage across L_4 changes sign, forward biasing D_{41}. With D_{41} forward biased, L_4 is essentially connected across the load and the energy stored in the magnetic field is transferred to the load. Addition of this clamping diode can add 10% — 40% to the circuit efficiency. The second feature is the low-pass filter formed by L_4 and C_{42}. The capacitor C_{42} may be selected to provide a relatively good analog output voltage with low ripple. Thus the load need not provide filtering. The filtered output signal proves especially desirable where harmonics of the switching frequency may cause considerable interference. It should be noted that the direct-coupled circuit of Fig. 5-2 is unipolar; an output voltage of only one polarity may be produced. A bipolar output circuit with an improved clamping circuit is presented on page 67, however the present circuit provides the required model for analysis.

Fig. 5-3 is a somewhat simplified representation of Fig. 5-2 with the transistor and clamping diode replaced by a rotary switch. If it is assumed that the driver pulses have remained of the same width for several pulses, then steady-state conditions will exist in the output circuit. Fig. 5-4 shows the inductor current, $i_4(t)$, and emitter voltage

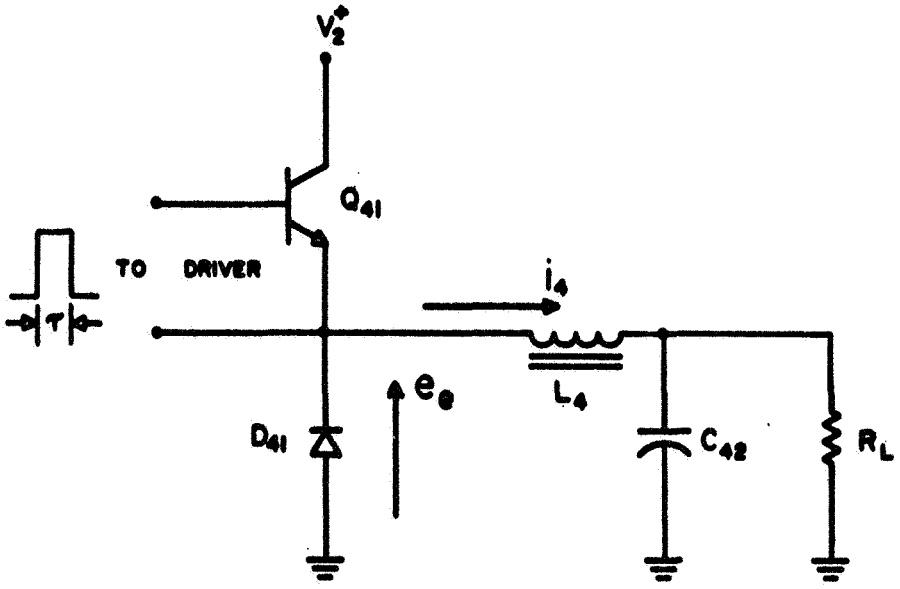

Fig. 5-2--Schematic diagram of a single-channel output circuit with a clamping diode and filter capacitor.

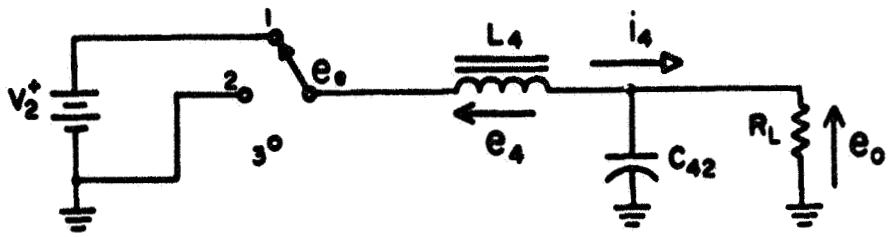

Fig. 5-3--Simplified schematic diagram of the output circuit of Fig. 5-2.

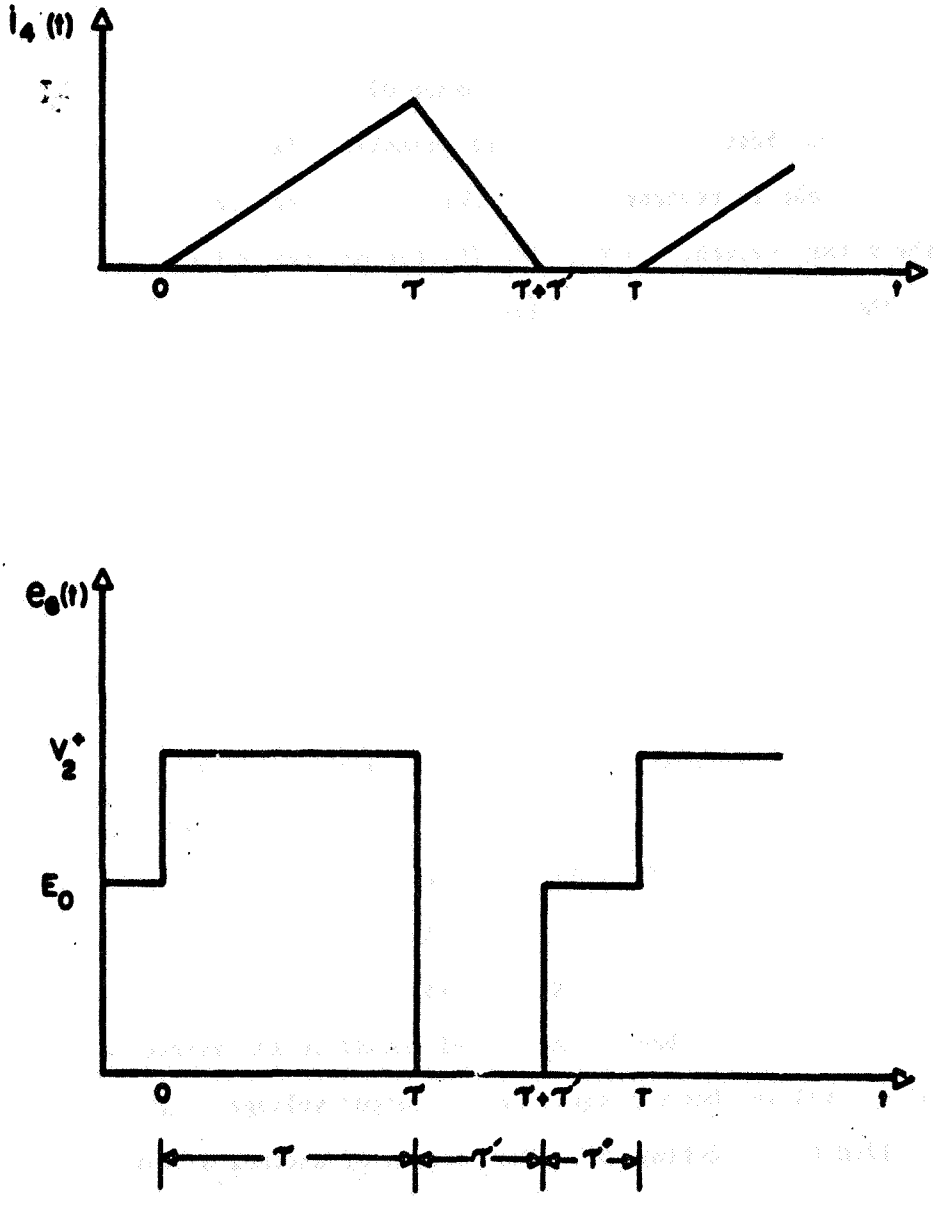

Fig. 5-4--The inductor current (a), and the emitter voltage (b) for the circuit of Fig. 5-3.

$e_e(t)$, waveforms for the output circuit under steady-state conditions.

The following description details the sequence of events in the operation of the output circuit. At $t = 0$ the transistor is driven on (saturated) and the diode is reverse-biased. This corresponds to position 1 of the rotary switch. In Fig. 5-4 (b) the emitter voltage now approximates the supply voltage, V_2^+. Since the clamping diode provides a zero initial condition for the inductor current, and since the on-time (pulse-width), τ, is small compared with the time constant of the circuit, then the inductor current, i_4, approximates a ramp which begins at $t = 0$ and which rises to some peak value I_p, during the time that the transistor is on. After τ seconds have elapsed, the transistor is driven off and the inductor voltage (e_4 in Fig. 5-3) reverses polarity to oppose the change in current flow. This polarity reversal forward-biases the diode and corresponds to position 2 of the rotary switch. This places the inductor in parallel with the capacitor and load. The energy stored in the magnetic field of the inductor is now transferred to the capacitor and load, and the inductor current is a decaying ramp during the clamping time, τ'. When inductor current ceases to flow at $t = \tau + \tau'$, the inductor voltage becomes zero, and the diode is reverse biased as the emitter voltage becomes equal to the output voltage, E_o, for an interval called the dead-time, τ''. The arrival of another driver pulse at $t = T$ begins another cycle. The period T is equal to the reciprocal of the switching frequency, f_s.

In switching circuits of this type the majority of the power loss occurs during the switching transitions. This is due to the simultaneous

combination of large collector current and large collector-emitter voltage which occurs briefly as the device changes states. The use of the inductor L_4 as shown in Fig. 5-2 causes the collector current to rise slowly while Q_{41} is being switched from the "off" state to the "on" state. This practically eliminates any power loss during the turn-on interval. It also eases the driver requirements because the driving pulse rise time is not critical, since collector current is nearly zero at turn-on.

Equations describing the operation of the output circuit will now be derived. Referring again to Fig. 5-3, the inductor voltage is given by

$$e_4 = L_4 \frac{di_4}{dt} = -e_o + V_2 \qquad 0 < t < \tau \qquad (5\text{-}1)$$

$$e_4 = L_4 \frac{di_4}{dt} = -e_o \qquad \tau < t < \tau + \tau' \qquad (5\text{-}2)$$

$$e_4 = L_4 \frac{di_4}{dt} = 0 \qquad \tau + \tau' < t < T \qquad (5\text{-}3)$$

Since $R_L C_{42} >> T$, if the pulse width τ has remained constant for several cycles, then steady-state conditions will exist and $e_o = E_o$, a constant.

The solution for the inductor current, i_4, is obtained by integration of the preceding equations, which yields

$$i_4 = \frac{V_2 - E_o}{L_4} t \qquad 0 < t < \tau \qquad (5\text{-}4)$$

$$i_4 = -\frac{E_o}{L_4} t + \frac{V_2 \tau}{L_4} \qquad \tau < t < \tau + \tau' \qquad (5\text{-}5)$$

$$i_4 = 0 \qquad \tau + \tau' < t < T. \qquad (5\text{-}6)$$

The peak current, I_p, in the transistor and clamping diode may now be found. The peak current is given by (5-4) at $t = \tau$.

$$I_p = \frac{(V_2 - E_o)}{L_4} \tau \qquad (5\text{-}7)$$

The clamping time may be found using (5-5). Since at $t = \tau + \tau'$, the inductor current becomes zero, then

$$i_4(\tau + \tau') = 0 = - \frac{E_o}{L_4} (\tau + \tau') + \frac{V_2 \tau}{L_4}$$

The clamping time is then

$$\tau' = \frac{(V_2 - E_o)}{E_o} \tau . \qquad (5\text{-}8)$$

Using (5-7), the clamping time may also be written as

$$\tau' = \frac{L_4 I_p}{E_o} \qquad (5\text{-}9)$$

The dead-time, τ'', is defined by the equation

$$\tau'' = T - (\tau + \tau') . \qquad (5\text{-}10)$$

Through the use of (5-8), the dead-time may be written as

$$\tau'' = T - \tau \left[\frac{V_2}{E_o}\right] . \qquad (5\text{-}11)$$

The average supply current, I_2, is the time-averaged integral of the emitter current over the on-time, τ.

$$I_2 = \frac{1}{T} \int_0^{\tau} \frac{I_p}{\tau} t \, dt = \frac{I_p \tau}{2T} . \qquad (5\text{-}12)$$

The average output current, I_o, is the sum of the time-averaged integral of the emitter current over the on-time, τ, and the time-averaged integral of the clamping diode current over the clamping time, τ'.

$$I_o = \frac{1}{T} \int_0^{\tau} I_p \frac{t}{\tau} dt + \frac{1}{T} \int_{\tau}^{\tau+\tau'} I_p \left(1 - \frac{t-\tau}{\tau'}\right) dt$$

$$I_o = \frac{I_p \tau}{2T} + \frac{I_p \tau'}{2T}$$

$$I_o = \frac{I_p (\tau + \tau')}{2T} \qquad (5\text{-}13)$$

One significant quantity has yet to be determined; that quantity is the output voltage, E_o. Unfortunately, E_o is not a linear function of the on-time, τ. A most useful expression relating E_o to τ and several parameters may be derived from an expression for the output stage efficiency.

The output stage efficiency, η_o, is the ratio of output power to the

load P_o, to input power, P_2, from the power supply which is connected to the output stage. The output power may be written as

$$P_o = \frac{E_o^2}{R_L} \tag{5-14}$$

and the input power may be written, using (5-10) as

$$P_2 = V_2 I_2 = \frac{V_2 I_p \tau}{2 T} . \tag{5-15}$$

The output stage efficiency may now be written as

$$\eta_o = \frac{P_o}{P_2} = \frac{\frac{E_o^2}{R_L}}{\frac{V_2 I_p \tau}{2T}}$$

Using (5-7), this may be rewritten as

$$\eta_o = \frac{E_o^2 (2 T L_4)}{\tau^2 R_L V_2 (V_2 - E_o)}$$

which may in turn be written as a quadratic equation in E_o,

$$E_o^2 + \frac{V_2 \tau^2 R_L \eta_o}{2TL_4} E_o - \frac{V_2^2 \tau^2 R_L \eta_o}{2 T L_4} = 0. \tag{5-16}$$

This equation may be simplified by normalizing the output voltage to the supply voltage as

$$E = \frac{E_o}{V_2} \quad , \tag{5-17}$$

by defining a duty cycle, Δ, as

$$\Delta = \frac{\tau}{T} \quad , \tag{5-18}$$

and by defining certain parameters as a lumped constant

$$a = \frac{\eta_o R_L T}{2} \quad . \tag{5-19}$$

Using these definitions, (5-16) may be re-written as

$$E^2 + \left(\frac{a}{L_4}\right) \Delta^2 E - \left(\frac{a}{L_4}\right) \Delta^2 = 0 \tag{5-20}$$

A plot of this function is useful. The lower limit of E, as defined by (5-17), is zero, as the output voltage could not have a polarity different from the power supply. The upper limit of E approaches one. Re-writing (5-11) using (5-17) and (5-18) yields

$$\tau'' = T\left[1 - \frac{\Delta}{E}\right] . \tag{5-21}$$

From this it is clear that if $\Delta \leq E$, then $\tau'' \geq 0$. This corresponds to the desired mode of operation as diagrammed in Fig. 5-4. Note that if $\Delta > E$, then $\tau'' < 0$. In the context of this analysis, a negative dead-

time would simply mean that the inductor current did not return to zero before the beginning of the next cycle of operation. Such a condition would result in an initial step in collector current at the beginning of each cycle. This is a slightly less efficient mode of operation, as explained earlier. Therefore, the upper limit of E will be set by the condition $E = \Delta$. This assures that the inductor current will be zero at the beginning of each cycle. A plot of (5-20) with $\frac{L_4}{a}$ as a parameter for $0 \leq E \leq \Delta$ is shown in Fig. 5-5. The preceding equations and Fig. 5-5 provide the necessary information for a complete analysis of the performance of a given output circuit.

In order to simplify the design of an output stage for a specific application, certain relationships may be derived. The fixed parameters for this design problem will be assumed to be the maximum output voltage (max E_o), the load resistance (R_L), and the upper cut-off frequency (f_2). In Chapter 7 it is shown that, given f_2, the switching frequency (f_s) may be specified. Since T is the reciprocal of f_s, a given value of f_2 fixes the period, T. Since the output circuit efficiency (η_o) varies little over most of the range of operation, η_o may also be assumed a fixed parameter. This means that for a given design problem the value of max E_o is a constant and the value of "a" is a constant, as defined in (5-19). There remain but two parameters which may be adjusted to optimize the operation of the output circuit; these are the inductance, L_4 and the power supply voltage, V_2. Equations will now be obtained which will relate the output circuit performance to these two design variables.

From Fig. 5-5 note that max E_o occurs when $E = \Delta$. Therefore, when

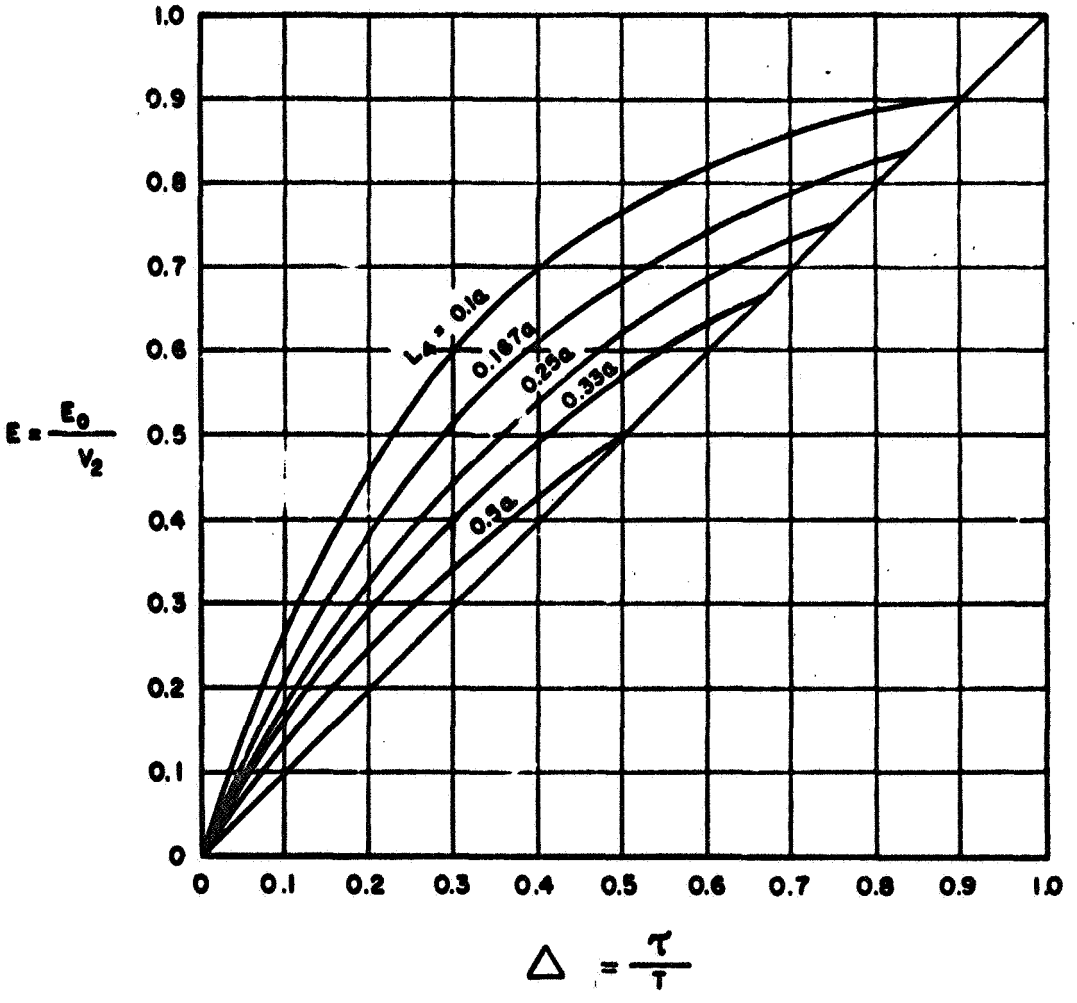

Fig. 5-5--A plot of normalized output voltage versus duty cycle.

$E = \Delta$, (5-17) may be written as

$$\Delta = E = \frac{\max E_o}{V_2} .$$

Substituting this relation into (5-20) yields,

$$\frac{V_2}{\max E_o} = \frac{1}{1 - \left(\frac{L_4}{a}\right)} . \qquad (5\text{-}22)$$

This equation shows that, for a given design, the choice of a particular value for V_2 will denote the required value for L_4. This relationship is depicted in the graph of Fig. 5-6, which is a plot of (5-22).

Another relationship which is necessary for the design is one between the peak current and the duty cycle. By rewriting (5-7) the following expression may be obtained:

$$I_p = \frac{(V_2 - E_o)}{L_4} \tau = \left(\frac{V_2 T}{L_4}\right)\left(1 - \frac{E_o}{V_2}\right)\frac{\tau}{T}$$

$$I_p = \left(\frac{V_2 T}{L_4}\right)(1 - E)\Delta . \qquad (5\text{-}23)$$

If (5-22) is solved for V_2, and if (5-19) is solved for T, the substitution of the results into (5-23) yields,

$$I_p = \Delta(1 - E)\left[\frac{2a}{\eta_o R_L}\right]\left[\frac{a (\max E_o)}{L_4 (a - L_4)}\right] . \qquad (5\text{-}24)$$

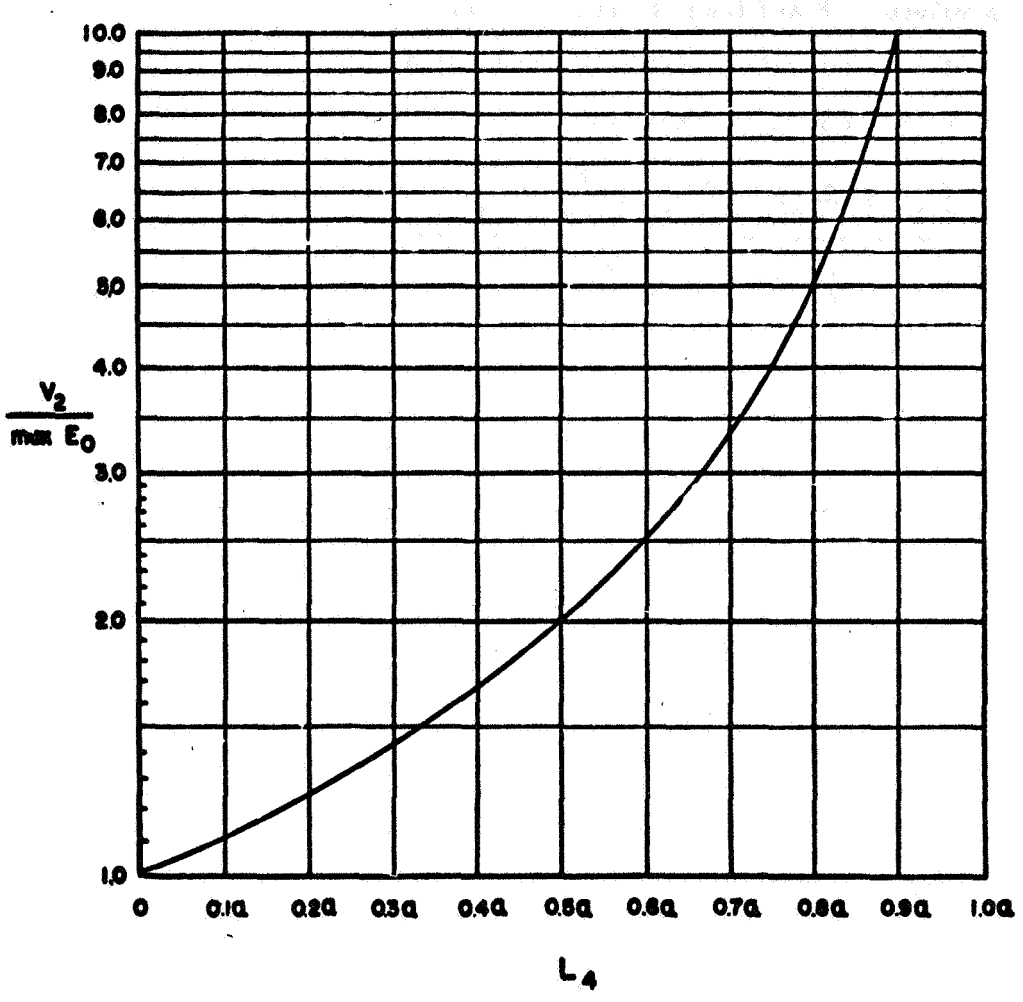

Fig. 5-6--A normalized plot of the relationship between power-supply voltage and the inductance, L_4.

This expression for I_p is probably the easiest for computational purposes since simultaneous values of E and Δ may be read from Fig. 5-5. However, if (5-20) is solved for E, and this solution is substituted in (5-24), the following expression for I_p is obtained:

$$\left[\frac{\eta_o R_L}{2\,(\max E_o)}\right] I_p = \frac{\Delta\left\{2 + \left(\frac{a}{L_4}\Delta^2\right) - \left[\left(\frac{a}{L_4}\Delta^2\right)^2 + 4\left(\frac{a}{L_4}\Delta^2\right)\right]^{1/2}\right\}}{2\left(\frac{L_4}{a}\right)\left(1 - \frac{L_4}{a}\right)} . \tag{5-25}$$

The maximum value of the peak current with respect to the duty cycle may now be found. Assuming that the values of all output circuit parameters are fixed, the peak current, I_p, as given in (5-24) will be directly proportional to some

$$I = \Delta\,(1 - E). \tag{5-26}$$

Again assuming that all output circuit parameters are fixed, this expression may be maximized with respect to Δ as follows.

$$\frac{dI}{d\Delta} = (1 - E) + (-\Delta)\,\frac{dE}{d\Delta} = 0$$

On solving this equation, the following condition is obtained for maximum I with respect to Δ.

$$\frac{dE}{d\Delta} = \frac{(1 - E)}{\Delta} . \tag{5-27}$$

Differentiating (5-20) with respect to Δ yields

$$\frac{dE}{d\Delta} = \frac{2\left(\frac{a}{L_4}\right)\left(1-E\right)\Delta}{2E + \left(\frac{a}{L_4}\right)\Delta^2} \quad . \tag{5-28}$$

Equating the right-hand sides of (5-27) and (5-28) yields

$$E = \frac{1}{2}\left(\frac{a}{L_4}\right)\Delta^2 \tag{5-29}$$

Thus I_p (which is directly proportional to I) is at its maximum value when (5-29) is satisfied. Substitution of the right-hand side of (5-29) for E in (5-20) shows that I_p is at its maximum value when

$$\Delta = \frac{2}{\sqrt{3\left(\frac{a}{L_4}\right)}}, \tag{5-30}$$

which, in (5-29) corresponds to the condition

$$E = \frac{2}{3} \quad . \tag{5-31}$$

Checking this result with the curves of Fig. 5-5 shows that the arbitrary limit of $E = \Delta$ precludes the satisfaction of (5-31) for $L_4 > 0.33a$. When $L_4 > 0.33a$, the largest value of I_p occurs when $E = \Delta$.

Fig. 5-7 is a graph of (5-25) for various values of the parameter $\frac{L_4}{a}$. Note, however, that the value of the parameter $\frac{L_4}{a}$ has been replaced by the corresponding value of $\frac{V_2}{\max E_o}$ as given by (5-22).

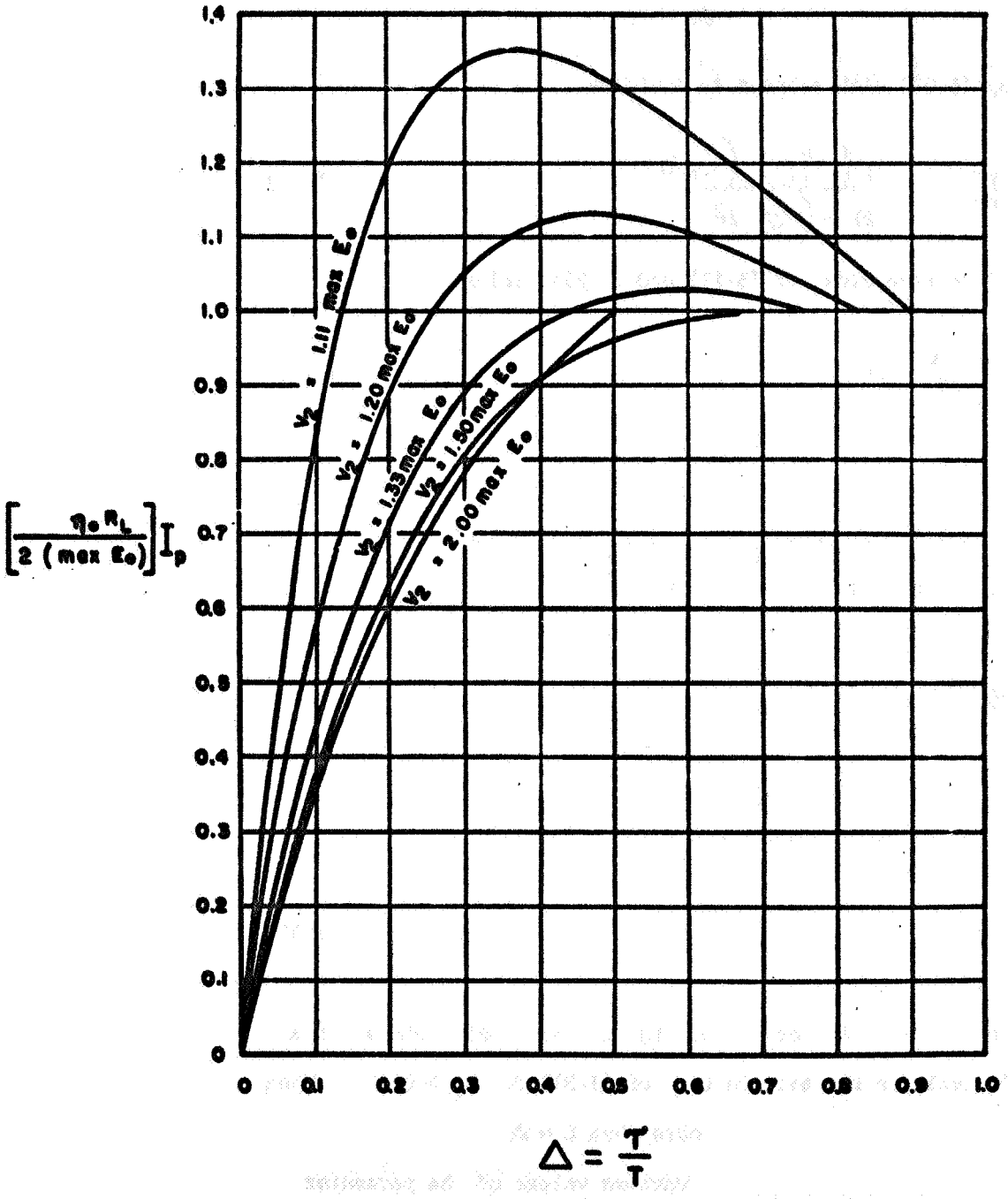

Fig. 5-7--A plot of normalized peak collector current versus duty cycle.

Some significant conclusions may be drawn from Fig. 5-7. As $\frac{V_2}{\max E_o}$ becomes smaller than 1.50, the largest value of the peak collector current increases considerably. However, as $\frac{V_2}{\max E_o}$ becomes greater than 1.50, the largest value of the peak collector current remains the same, and occurs when $E = \Delta$. Referring back to Fig. 5-2, it is easily deduced that as the power supply voltage increases, the collector-emitter breakdown voltage rating of the transistor must also be increased to assure reliable operation. For many cases the optimum combination of lowest collector current and lowest collector-emitter voltage may be obtained by selecting

$$V_2 \approx 1.50 \max E_o. \tag{5-32}$$

For convenience, Fig. 5-5 was replotted as Fig. 5-8 with the parameter changed to $\frac{V_2}{\max E_o}$ using (5-22).

While the circuit of Fig. 5-2 has been completely adequate for analysis purposes, it is obvious that the clamping diode will be a short-circuit for negative output voltages. For a bipolar output voltage the clamping circuit must be modified. A practical clamping circuit is shown in Fig. 5-9.

Comparing Fig. 5-9 with Fig. 5-2 reveals that a "clamping" winding has been placed on L_4, resulting in T_{41}. During the clamp-time, τ', the clamping winding drives Q_{42}, the clamping transistor, into saturation, effectively grounding the anode of D_{41}. The clamping diode, D_{41}, is still required, since a short-circuit to ground would exist for positive

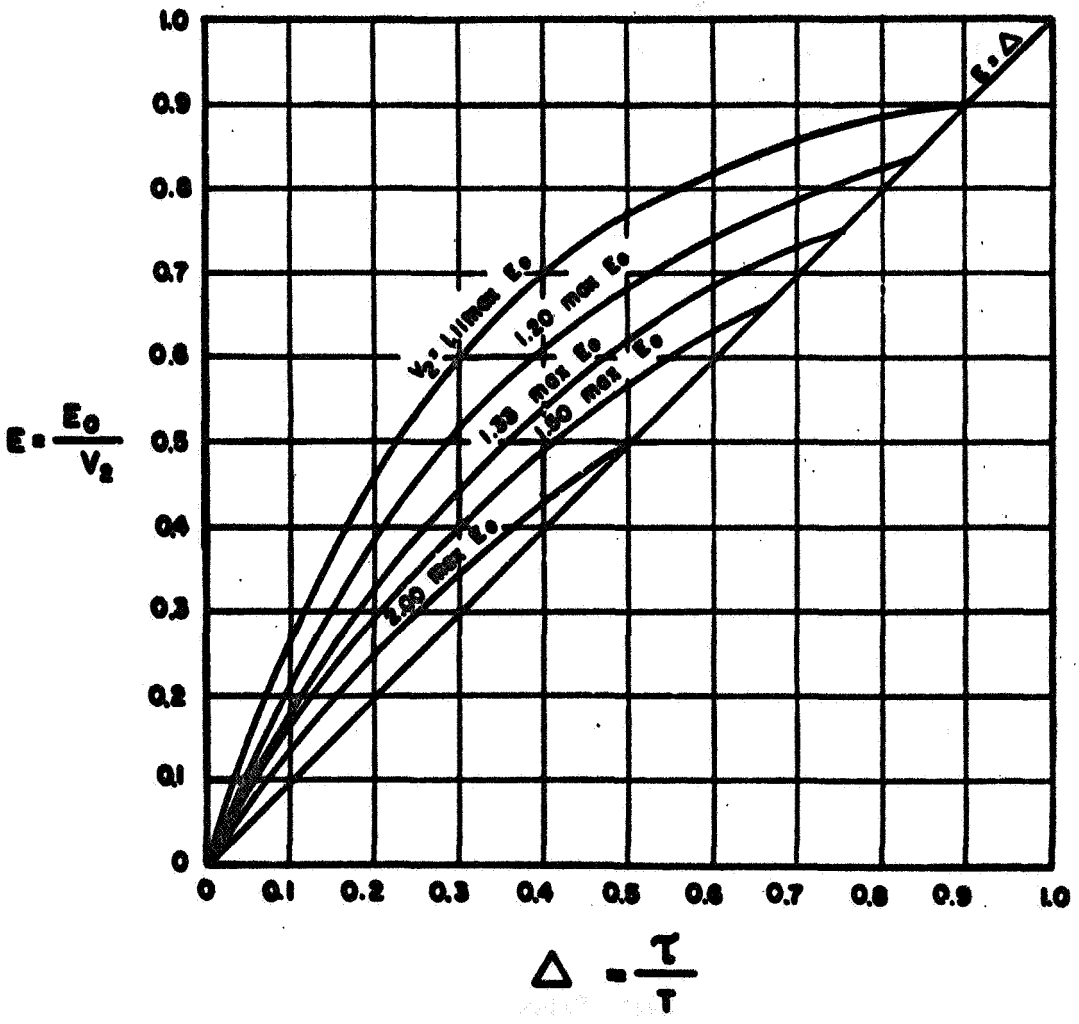

Fig. 5-8--A plot of Fig. 5-6 with the parameter changed to $\frac{V_2}{\max E_0}$.

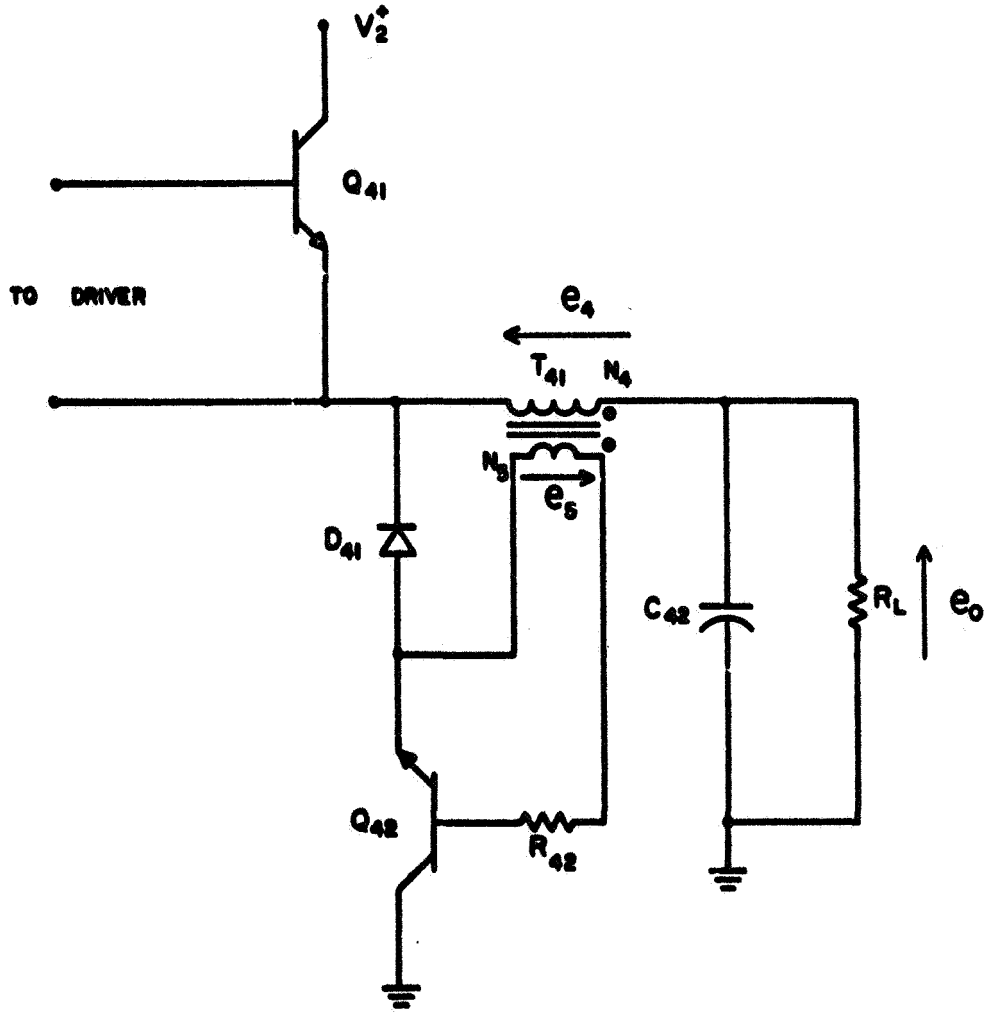

Fig. 5-9--Schematic diagram of the N-channel of the output stage with a complete clamping circuit.

output voltages, through the clamping winding, R_{42}, and the base-collector junction of Q_{42}.

The number of turns required for the clamping winding is determined in the following manner. The maximum voltage which will appear across L_4 (the primary of T_{41}) is

$$e_{4\ max} = |V_2 + max\ E_o|. \tag{5-33}$$

This occurs when Q_{41} is saturated with a negative voltage present across C_{42}. The maximum voltage across the base-emitter junction of Q_{42} will be

$$e_{5\ max} = \frac{N_5}{N_4}\ e_{4\ max} \tag{5-34}$$

where N_4 is the number of turns on the primary of T_{41} and N_5 is the number of turns on the clamping winding. Since $e_{5\ max}$ must be less than BV_{BE} the base-emitter breakdown voltage, for Q_{42}, the upper limit on the number of turns for the clamping winding is given by

$$e_{5\ max} < BV_{BE}$$

$$max\ N_5 = \frac{N_4\ BV_{BE}}{|V_2 + max\ E_o|} \tag{5-35}$$

Referring back to Fig. 5-3 it may be noted that, during the clamping interval when the switch is in position 2, the inductor voltage is

$$|e_4| = |e_o| \qquad \tau < t < \tau + \tau'. \tag{5-36}$$

The voltage on the clamping winding will be

$$|e_5| = \frac{N_5}{N_4} |e_o| . \tag{5-37}$$

In order to obtain adequate base drive for Q_{42}, the case for maximum collector current will be considered. The maximum collector current will be max I_p, and a corresponding maximum value of the base current, max i_5, will be required to saturate Q_{42}. Under these conditions the emitter-base voltage of Q_{42} will take on some maximum value, V_{BE}. Thus, to saturate Q_{42}, e_5 must be

$$|e_5| = |\max i_5 R_{42} + V_{BE}| \tag{5-38}$$

and N_5 is given by

$$N_5 = \frac{N_4 |\max i_5 R_{42} + V_{BE}|}{|\max E_o|}. \tag{5-39}$$

The output capacitor, C_{42}, (Fig. 5-9) in parallel with the load, R_L, acts as a low-pass filter. For many applications there exists some latitude in the choice of C_{42}; however, there are limits.

The upper limit on the value of C_{42} depends upon the desired upper cutoff frequency, f_2, for the amplifier. The value of C_{42} which would

result in the desired f_2 is

$$C_{42} = \frac{1}{2\pi f_2 R_L} . \qquad (5\text{-}40)$$

The lower limit on the value of C_{42} depends upon the amount of ripple which is allowable at the output. If better filtering is desired a more elaborate filter such as a π-section could be used in place of the capacitor, C_{42}.

The schematic diagram of a complete output stage is shown in Fig. 5-10.

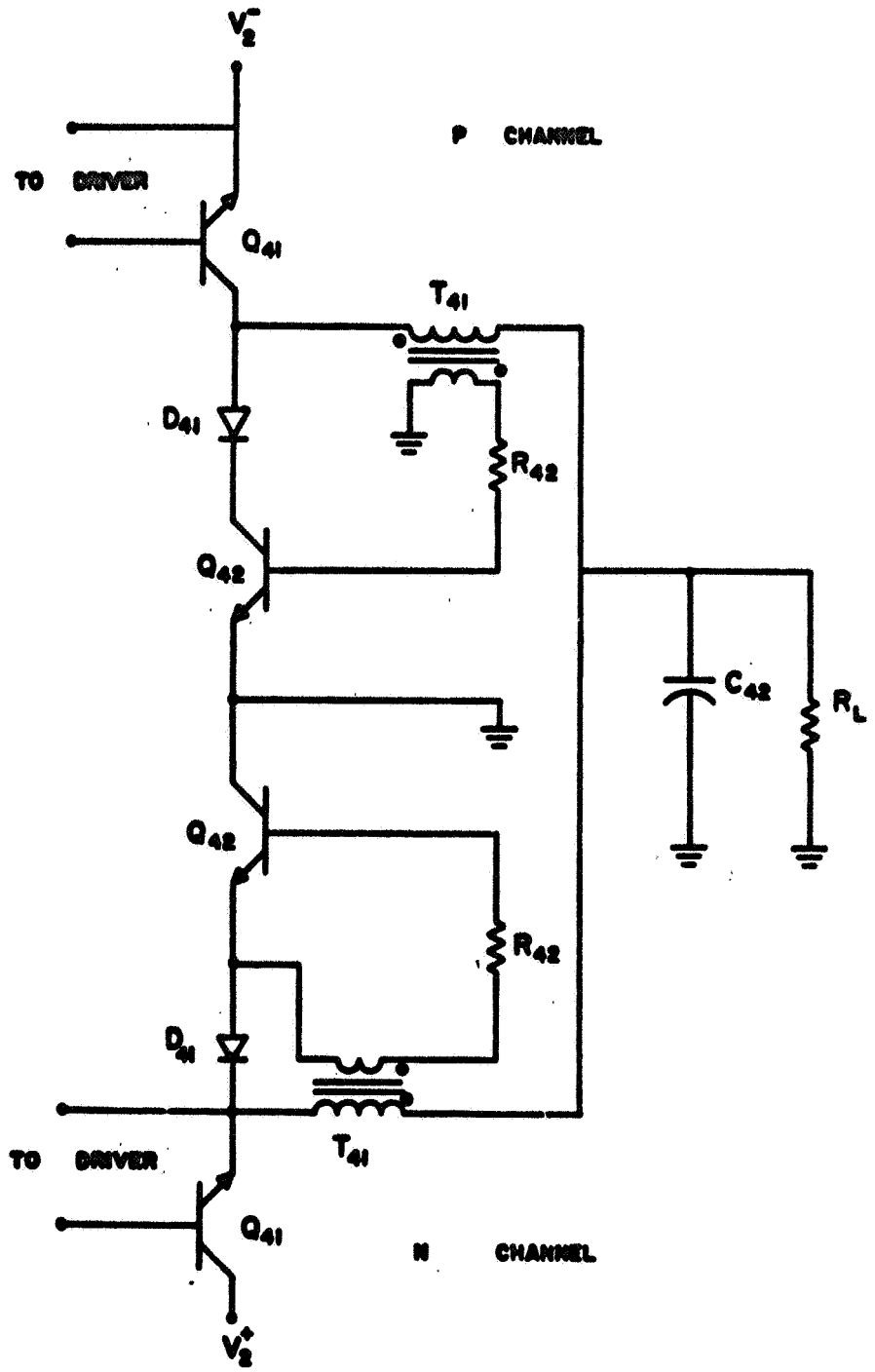

Fig. 5-10--Schematic diagram of the output stage.

6. AMPLIFIER CONFIGURATIONS

A block diagram of a basic class-D amplifier was shown in Fig. 1-1. In discussing amplifier configurations a more convenient diagram is desired. As will be seen later, the input stage is shown in schematic form because of the multiple function of some of its components. The remainder of the amplifier is represented by a single block.

As previously presented the amplifier was designed with a P-channel which responds to positive inputs and produces a negative output and an N-channel which responds to negative inputs and produces a positive output. Thus, this section of the amplifier can be represented as a block with gain -A.

Ideally, any amplifier used as an operational amplifier should have infinite gain, infinite input impedance, and zero output impedance.

Of course, in practice such characteristics cannot be obtained. However, it has been shown elsewhere[1] that derivations of gain and impedance levels assuming ideal amplifiers predict quite accurately the performance actually obtained from physical amplifiers if the following open loop characteristics are met:

$A_v \geq 10{,}000$

$Z_{in} \geq 50\ k\Omega$

$Z_{out} \leq 100\ \Omega$

All of these requirements are easily met with the class-D amplifier

described in this report. Therefore, the following statements regarding gain and input impedance of the various operational amplifier configurations are made assuming ideal characteristics.

One of the basic operational amplifier configurations is the inverting amplifier. The class-D amplifier used in this configuration is shown in Fig. 6-1. Assuming ideal amplifier characteristics, the voltage gain is given as,

$$A_v = \frac{-R_3}{R_1} \quad . \tag{6-1}$$

The input impedance of the inverting amplifier is,

$$Z_{in} = R_1 \quad . \tag{6-2}$$

The non-inverting amplifier may be implemented as in Fig. 6-2. It is necessary to eliminate the sign reversal that was previously associated with the modulator, driver, and output stages. This is easily done by interchanging outputs of the modulator such that a pulse-width modulated signal produced by positive control signals is used to drive the N-channel driver and the modulated signal produced by negative control signals is used to drive the P-channel driver. Note that R_{11} has a dual function. It is a factor in determining the gain of the input stage and is also a factor in determining the gain of the non-inverting amplifier configuration. This gain is given by

$$A_v = \frac{R_{11} + R_3}{R_{11}} \quad . \tag{6-3}$$

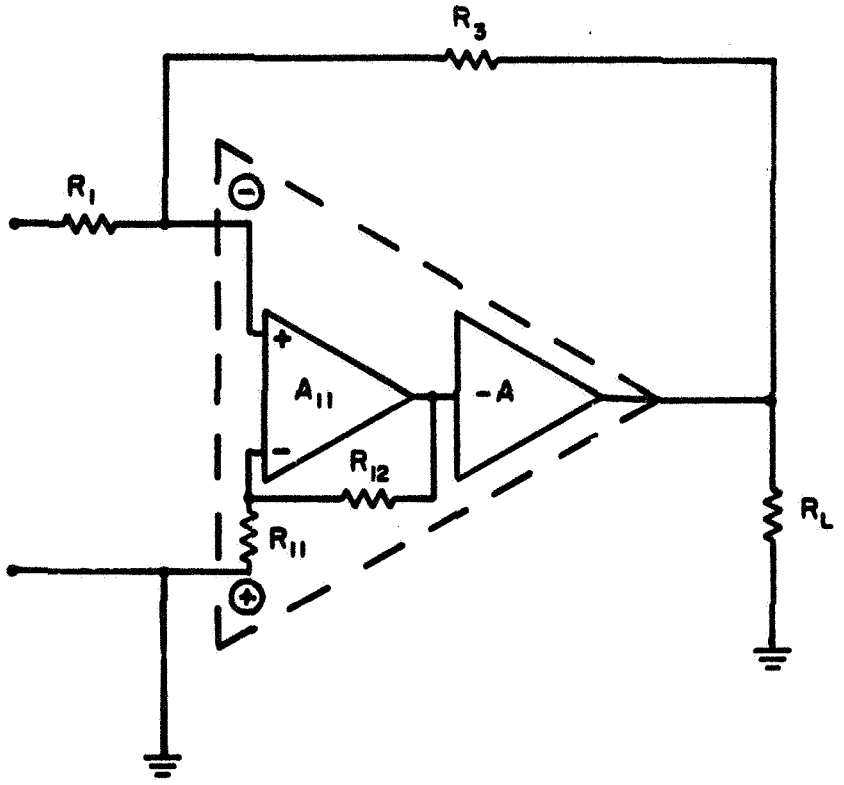

Fig. 6-1--The basic class-D amplifier connected as an inverting amplifier.

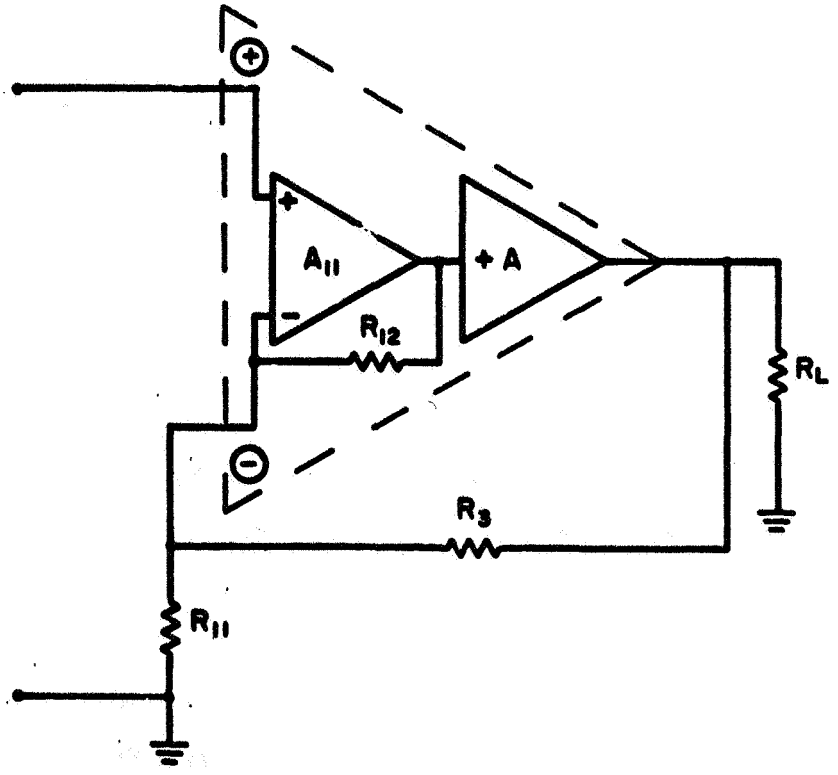

Fig. 6-2--The basic class-D amplifier connected as a non-inverting amplifier.

The input impedance of the non-inverting amplifier is essentially infinite.

A third basic configuration is the differential amplifier, as shown in Fig. 6-3. Again R_{11} assumes a dual role in determining the gain of both the input stage and the overall differential amplifier. R_1 should be chosen equal to R_2, and R_3 chosen equal to R_{11} for this configuration. The gain of the differential amplifier is,

$$A_v = \frac{R_3}{R_1} = \frac{R_{11}}{R_2} \quad . \tag{6-4}$$

The input impedance of this configuration is,

$$Z_{in} = R_1 + R_2 \quad . \tag{6-5}$$

The previous circuits all employed voltage feedback as shown in Fig. 6-4(a). Current feedback may also be employed, as shown in Fig. 6-4(b). Note that a feedback voltage, proportional to load current, is developed across R_I. Current feedback is often used where the load current is of interest.

The transconductance of an amplifier using current feedback may be easily determined. Referring to Fig. 6-4(b), the voltage gain from the current-sampling resistor to the input is,

$$A_v = \frac{R_f}{R_1} \tag{6-6}$$

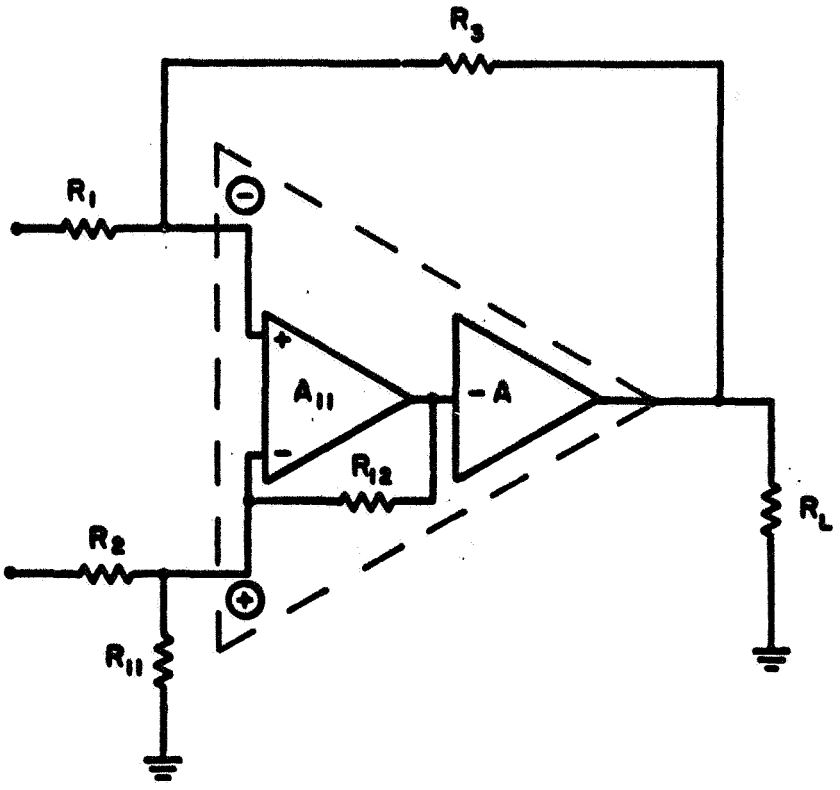

Fig. 6-3--The basic class-D amplifier connected as a differential amplifier.

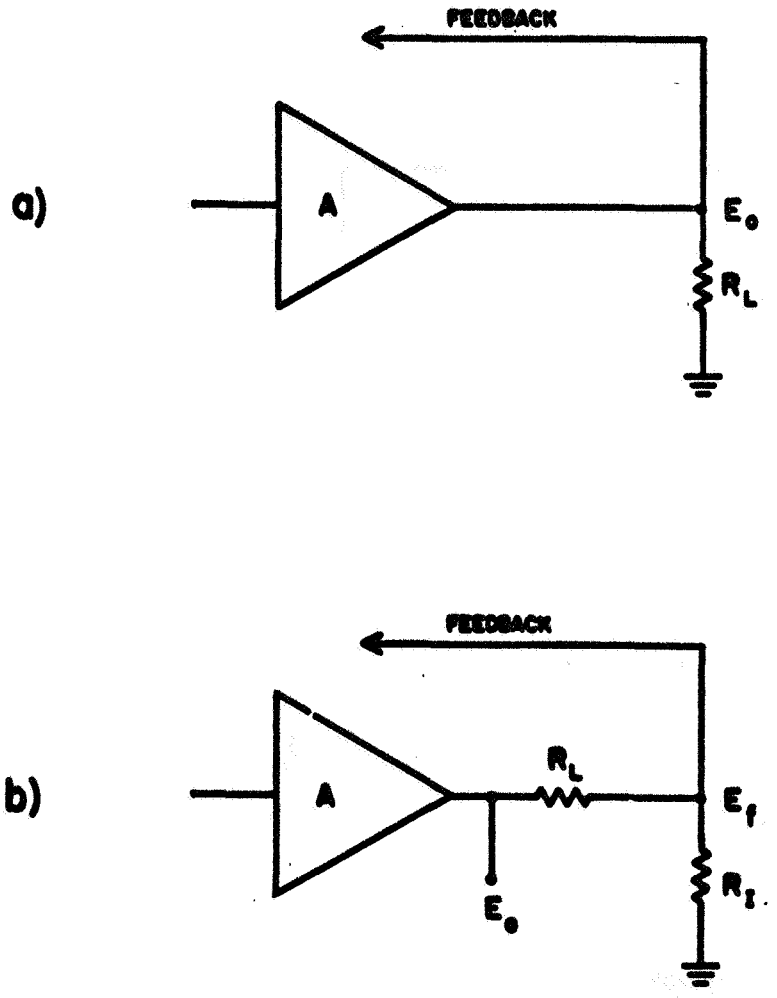

Fig. 6-4--A voltage-feedback configuration (a), and a current-feedback configuration (b).

where E_i is the input voltage. The gain is determined by the amplifier configuration as with voltage feedback. From Fig. 6-4(b),

$$E_f = I_L R_I, \tag{6-7}$$

therefore the transconductance, G, is given by

$$G = \frac{I_L}{E_i} = \frac{A_v}{R_I}. \tag{6-8}$$

Some phase shift of the analog signal occurs because of the low-pass filter consisting of T_{41} and C_{42} at the output in Fig. 5-10. When the feedback loop is closed, stability problems may exist. Standard compensation techniques may be applied to the input stage to obtain stability. As may be seen from Fig. 5-6, there is an inherent non-linearity in the gain characteristic of the output stage. When the amplifier is operated closed-loop this slight variation in gain has essentially no effect on the linearity of the amplifier. The open-loop gain is greatest for low-level inputs.

The compensation used depends upon the particular amplifier employed in the input stage. In some cases the components required to compensate the system may become physically large and the alternative of lowering the open-loop gain of the amplifier may have to be taken. In most cases this should cause essentially no deterioration of closed-loop performance.

As shown in this chapter, the class-D amplifier may easily be adapted to three basic operational amplifier configurations: inverting; non-inverting; and differential. Voltage or current feedback may be used

with each of the configurations.

7. SAMPLING TECHNIQUE

As mentioned in Chapter 3, there are three basic types of pulse-duration modulation. They are leading-edge, trailing-edge, and double-edge modulation. Each of these types of pulse-width modulation may be generated by the use of either fixed or natural sampling. The process of fixed sampling requires that the input signal be sampled at precisely periodic intervals, and that its instantaneous value at the time of sampling be held while a pulse of appropriate width is generated.

Natural sampling is used in the pulse-width modulator described in Chapter 3. As explained there, the control voltage, e_c, (input to the modulator) is added to a triangular waveform e_t, and the intersection of $e_c + e_t$ with the constant reference voltage determines the leading and trailing edges of the pulses. The width of the pulse produced is proportional to both the amplitude and the shape of $e_c + e_t$ during the sampling interval.

One should notice that with natural sampling of a time-varying signal as in Fig. 7-1, the center lines of the pulses do not occur exactly at periodic intervals. This in effect produces a phase shift θ, as shown in Fig. 7-1. The higher the sampling frequency, the more negligible the phase shift becomes.

The pulse-width-modulated waveform may be represented by a Fourier series. For double-edge modulation the series is[3]

$$e(t) = \frac{BH}{\pi} + \frac{KH}{\pi}\cos\omega_c t + \sum_{m=1}^{\infty}\sum_{n=-\infty}^{\infty}\frac{2H}{m\pi}J_n(mK)\sin\left(mB + \frac{n\pi}{2}\right)\cos\left[(m\omega_s + n\omega_c)t\right] \qquad (7\text{-}1)$$

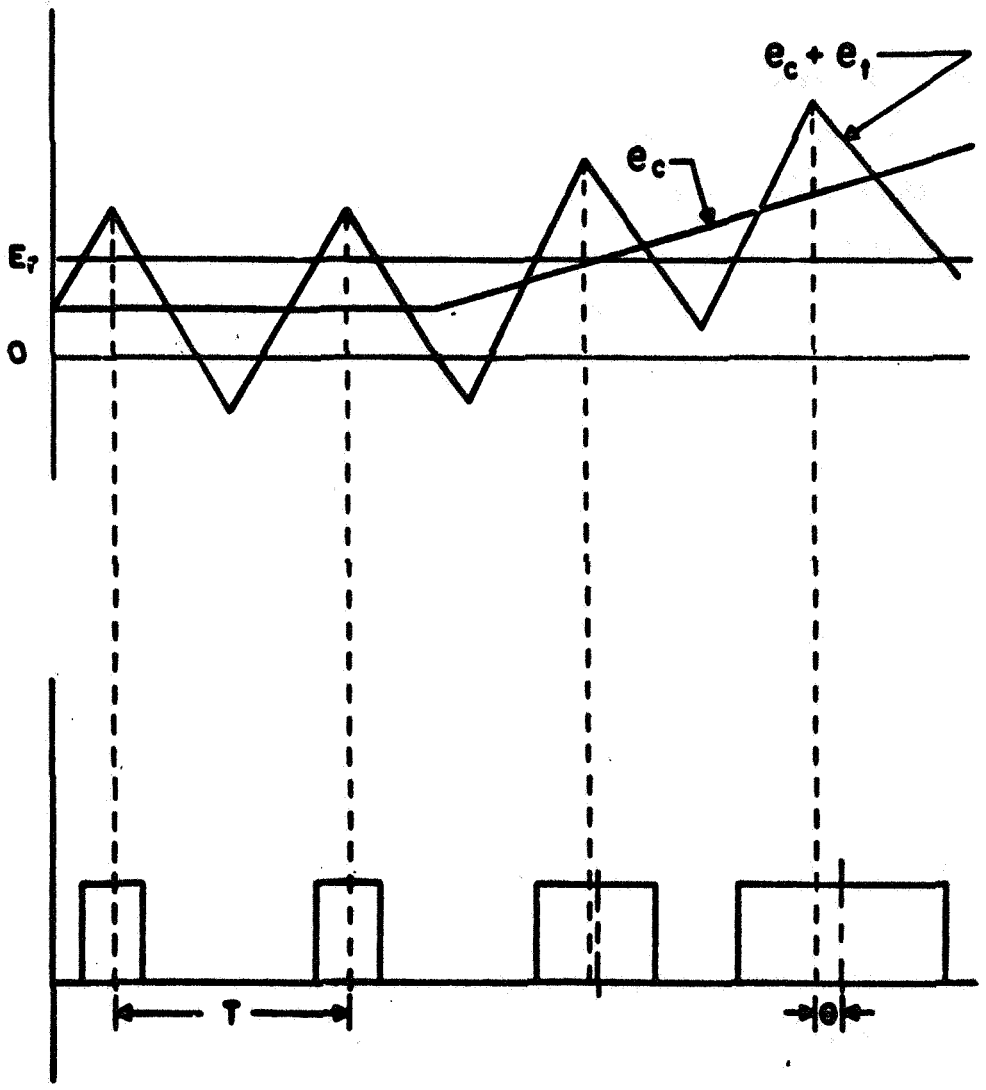

Fig. 7-1--Modulator waveforms associated with natural sampling.

where

B = the d-c component of the control signal

E = the peak value of the a-c component of the control signal

H = the output pulse magnitude

ω_s = the switching frequency (radians)

ω_c = the control signal frequency (radians)

$J_n(x)$ = Bessel function of the first kind of order n with modulus x.

Due to the nature of the mathematical model used, (7-1) yields information concerning only the relative magnitudes and the frequencies of the components involved. Scaling factors would be required in order to predict the true magnitudes of the components produced by an actual circuit. The first term in (7-1) is the d-c component, the second term is the control signal frequency component, and the final term includes the switching frequency and intermodulation components. The frequency spectrum of the double-edge, pulse-width modulated waveform is shown in Fig. 7-2. The intermodulation components are those with angular frequencies of the form $m\omega_s \pm n\omega_c$.

If the control signal is of relatively low frequency, the intermodulation components remain closely grouped about the switching frequency. However, as the frequency of the control signal is increased, the $\omega_s - n\omega_c$ components begin to approach the control signal (ω_c) component. Thus the switching frequency (ω_s) should be chosen high enough to prevent the occurrence of intermodulation components of significant magnitude within

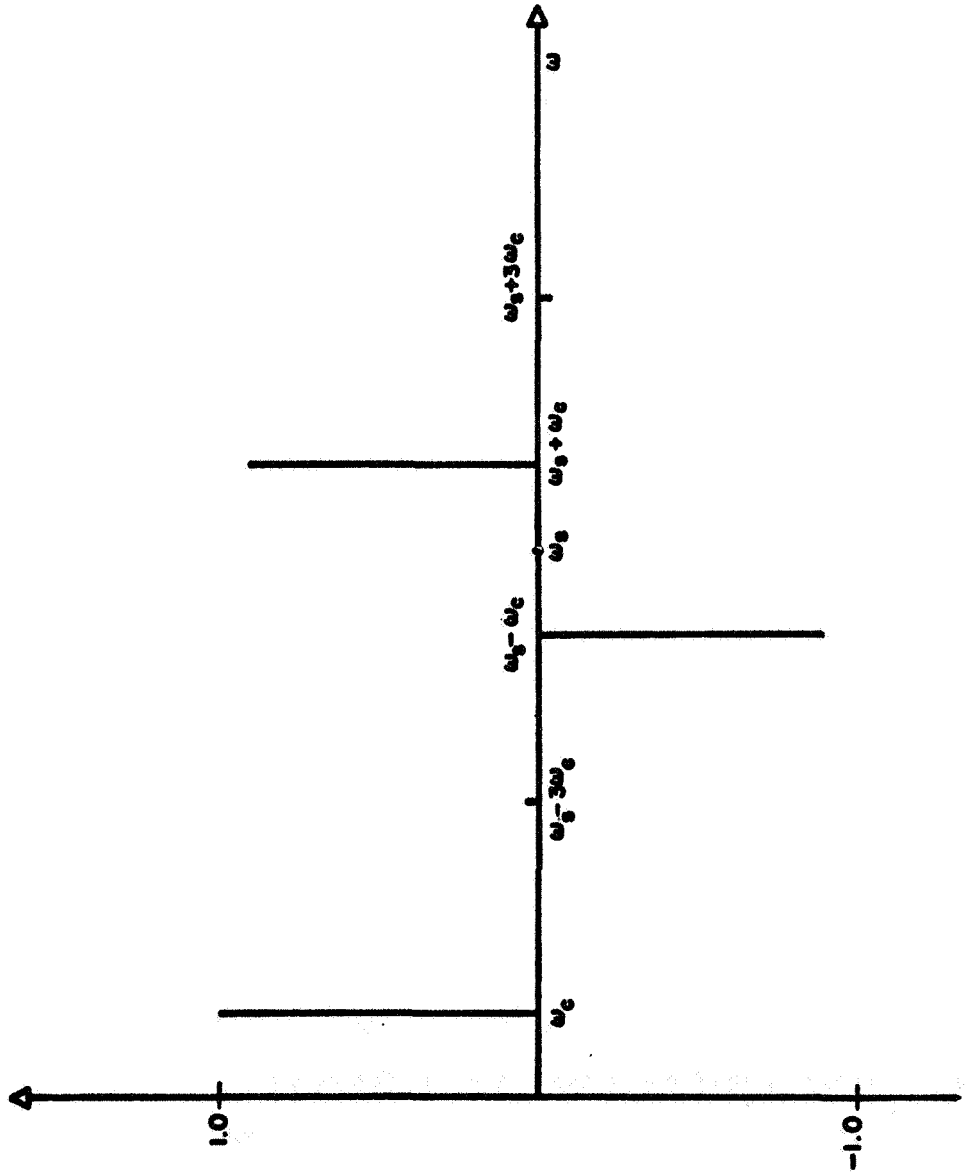

Fig. 7-2--Frequency spectrum of a waveform that is pulse-width-modulated by a sinusoid of frequency ω_c which is naturally sampled at a frequency ω_s.

the amplifier pass-band. An analysis of the spectrum shown in Fig. 7-2 indicates that the $\omega_s-\omega_c$ component is down 1db from the ω_c component, the $\omega_s-3\omega_c$ component is down 28db, and the $\omega_s-5\omega_c$ component is down 66db. The first two intermodulation terms are of sufficient magnitude to cause significant distortion if they should occur within the amplifier pass-band. Thus, ω_s should be selected such that $(\omega_s-3\omega_2)>\omega_2$, or $\omega_s> 4\omega_2$, where ω_2 is the desired upper cut-off frequency of the amplifier. Then the modulated signal can be demodulated by passing the signal through a low-pass filter with a cutoff frequency of f_2, and no significant intermodulation distortion should result. Therefore, the switching frequency may be selected such that

$$f_s \geq 5 f_2. \tag{7-2}$$

In order to use relatively small filter components or to assure very low intermodulation distortion, the switching frequency may be chosen considerably greater than $5 f_2$.

8. DESIGN PROCEDURE

This chapter presents a step-by-step design procedure for the class-D amplifier. The basic amplifier schematic diagram is shown in Fig. 8-2. (This is the last figure in the chapter, and may be left folded out for reference.) Note that feedback arrangements are omitted in Fig. 8-2, because, as shown in Chapter 6, the amplifier can be used with any of several different feedback arrangements. Also, several of the components shown may be omitted, depending upon design requirements.

The format for this chapter is as follows: a list of common amplifier specifications is set forth in Table 8-1; a design procedure for the individual stages is presented, working back from the output stage; and several common feedback configurations are presented. All unique equations used in the procedure are derived in the preceding chapters and are listed with their equation number for reference. A list of the symbols used is given in the Appendix.

TABLE 8-1.

SPECIFIED PARAMETERS

R_L	Load resistance
P_M	Maximum d-c power output
f_2	Upper cutoff frequency
V_2^+, V_2^-	Output stage power supply voltage
V_1^+, V_1^-	Input stage, modulator, and driver power supply voltage
A_v	Closed-loop voltage gain (voltage feedback)
or	
G	Closed-loop transconductance (current feedback)
	Differential (balanced) or unbalanced input?

A. Output Stage

It should be noted that the maximum sinusoidal a-c power output is approximately one-half the maximum d-c power output (P_M). This is because the maximum d-c output voltage is equal to the peak value of the a-c output voltage.

Calculate the maximum d-c output voltage

$$\max E_o = \sqrt{P_M R_L} \quad .$$

Calculate the switching frequency

$$f_s \geq 5 f_2 \quad .$$

Calculate the period of the switching waveform

$$T = \frac{1}{f_s} \quad .$$

Assume that the output stage efficiency is

$$\eta_o = 0.85 \quad .$$

The next several steps refer to the curves of Fig. 8-1, which is a composite of Figures 5-6, 5-7, and 5-8. If V_2 is not specified, let

$$V_2 = 1.50 \max E_o \quad . \tag{5-32}$$

If linearity is critical, observe in Fig. 8-1(a) that the output stage linearity improves for larger ratios of V_2 to $\max E_o$. If V_2 is specified, calculate the ratio of V_2 to $\max E_o$ and interpolate for the desired curves in Fig. 8-1 (a) and (b).

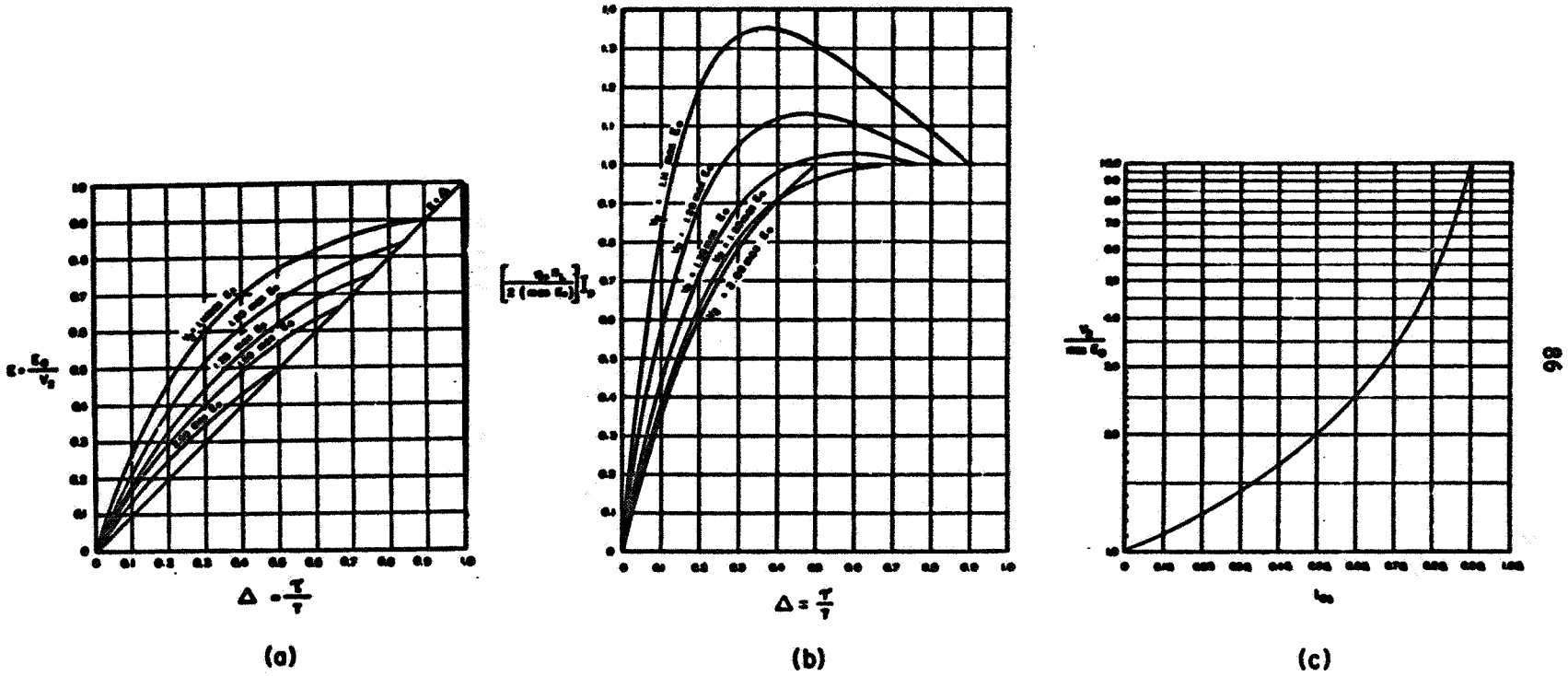

Fig. 8-1.--Graphs of the principal design equations for the output stage from Chapter 5: (a) Fig. 5-8; (b) Fig. 5-7; (c) Fig. 5-6.

Calculate maximum pulse width

$$\max \tau = T \frac{\max E_o}{V_2} \quad .$$

Calculate the constant

$$a = \frac{\eta_o R_L T}{2} \quad . \tag{5-19}$$

Using the appropriate parametric curve in Fig. 8-1(b), determine the maximum value of I_p, the peak collector current.

Select Q_{41} having

$$BV_{CE} \geq 2.5 V_2 ,$$

$$\max I_C \geq \max I_p ,$$

β (at $\max I_p$, in saturation) > 15-20 ,

$$\frac{V_{CE\ SAT} \text{ (at } \max I_p)}{\max I_p} < 0.1\ \Omega ,$$

fast switching characteristics, and collector dissipation > 30% P_M. Note from Fig. 8-1(b) that V_2 may be reduced if a larger value of $\max I_p$ can be accomodated; however, the lower current levels usually result in less power loss.

Select D_{41} having

$PRV \geq 1.5 V_2$,

$\max I_{FWD} \geq \max I_p$, and

fast recovery time.

Select Q_{42} having

$BV_{CE} > 1.5\ V_2$, and

other characteristics which are the same as Q_{41}.

Let R_{42} be approximately equal to the saturation value of the base resistance of Q_{42} at the maximum value of I_p.

From Fig. 8-1(c) determine L_4, the primary inductance of T_{41}. For good efficiency, use a toroidal core with high Q at f_s. Determine the primary turns, N_4, and check that the core will not saturate at max I_p. Calculate the required number of turns for the clamping winding, N_5, using

$$N_5 = \frac{N_4 \left| \max i_5\ R_{42} + V_{BE} \right|}{\left| \max E_o \right|} \qquad (5\text{-}39)$$

where i_5 and V_{BE} are the base current and base-emitter voltage for Q_{42} when it is saturated with a collector current equal to max I_p. Check that this value of N_5 does not exceed the maximum given by

$$\max N_5 = \frac{N_4\ BV_{BE}}{\left| V_2 + \max E_o \right|} \qquad (5\text{-}35)$$

where BV_{BE} is for Q_{42}.

Calculate the value of C_{42} from

$$\frac{1}{2\pi(f_s - 3f_2)RL} < C_{42} < \frac{1}{2\pi f_2 RL}$$

(This is based upon considerations set forth in Chapter 7 and (5-42)). If desired, a more elaborate filter may be used in place of C_{42}.

B. Driver Stage

If $P_m < 100$ watts the circuit associated with Q_{32} may be omitted. (See Chapter 4) Select R_{41} to be approximately 1/2 the effective base resistance of Q_{41}. (R_{41} may be eliminated when large base current is required, so as to decrease power loss in the base drive circuit.)

Calculate the turns ratio,

$$\frac{N1}{N_2} = \frac{V_1^+}{V_{BE} + I_B R_{41}} \quad . \tag{4-3}$$

Estimate the maximum primary current max $i_1 \approx \frac{N2}{N_1} I_B$.

Select Q_{31} having

$BV_{CE} > 2V_1$,

max $I_C >$ max i_1 ,

β (at max i_1 , in saturation) > 30 ,

a low collector-emitter voltage in saturation, and fast switching characteristics.

Specify the tilt factor, $0.9 > q > 0.7$. Estimate R_{SAT} for Q_{31}. Calculate the secondary inductance

$$L_2 = \frac{\tau_{max}}{\left(\ell n \frac{1}{q}\right)\left(\frac{(N_1/N_2)^2}{R_{SAT}} + \frac{1}{R_{42} + V_{BE}/I_B}\right)} \tag{4-9}$$

where V_{BE} and I_B are associated with Q_{41} . Select a core for T_{31}

with high Q at f_s. Determine from the core data the value of N_2 required to obtain L_2.

Calculate N_1 using the turns ratio determined earlier. Calculate L_1 using

$$L_1 = L_2 \left(\frac{N_1}{N_2}\right)^2 .$$

If desired, the peak value of primary current may be determined using (4-10).

Determine R_{33} experimentally by selecting the largest value which eliminates any excessive ringing that may occur when Q_{31} switches. Select R_{31} using

$$R_{31} = \frac{E_b - V_{BE}}{I_B} \qquad (4\text{-}4)$$

where V_{BE} and I_B refer to Q_{31}. Experimentally determine C_{31} and C_{41} by selecting those values which cause the fastest switching of Q_{31} and Q_{41}.

If the shorting circuit is to be used, let

$$N_3 = N_1 .$$

Since the waveforms at the shorting winding are rather unpredictable, it is difficult to accurately specify the requirements for Q_{32}. However, a safe selection may be made by picking Q_{32} to have approximately the same characteristics as Q_{31}. Select D_{31} so that

$$\max I_{FWD} \geq \max I_C \text{ of } Q_{32} .$$

Determine R_{32} by

$$R_{32} = \frac{-E_p + V_{BE}}{I_B} \qquad (4\text{-}5)$$

where V_{BE} and I_B refer to Q_{32} . Experimentally determine C_{32} by selecting a value which results in the most efficient operation of Q_{41}.

Voltage spikes may occur when Q_{31} switches. If needed, a zener diode, D_{32}, may be placed across Q_{31} to prevent failure from voltage spikes in excess of BV_{CE} of Q_{31}.

C. Pulse-Width Modulator

Select a type of operational amplifier or comparator for A_{21}, A_{22}, and A_{23} which meets the following requirements:

symmetric bipolar output;

high gain;

high input impedance;

low output impedance;

and, low quiescent power consumption.

(A μA709 integrated amplifier may prove satisfactory in most cases).

The design of the oscillator will be considered first. For use in (3-4), which follows, selection of K = 3 will yield reasonable linearity and should suffice for most applications. (A discussion of the selection of K follows (3-13) in Chapter 3.) Experimentally determine E_s, the saturated output of A_{21}. Calculate E_{pk} using

$$E_{pk} = \frac{E_s}{k} \quad . \qquad (3\text{-}4)$$

Rewriting (3-8), obtain the product $R_{23}C_{21}$ as

$$R_{23}C_{21} = \frac{1}{2f_s \ln\left(\frac{k+1}{k-1}\right)}$$

Select C_{21} and R_{23} such that the above equation is satisfied. A satisfactory choice of C_{21} for f_s of 10 kHz is 0.005 μfd.

Select R_{24} and R_{25} such that

$$\frac{1}{k} = \frac{R_{25}}{R_{24} + R_{25}} \qquad (3\text{-}3)$$

Values in the range from 10 kΩ to 100 kΩ will yield satisfactory results. The only other restraints on R_{23}, R_{24}, and R_{25} are that they should be large enough to prevent overloading A_{21} and much smaller than the input impedance of A_{21}.

To begin the design of the comparator circuits, calculate the peak of $e_m(t)$ from (3-10) by replacing $e_t(t)$ with $e_c(t) = E_{pk}$ and $e_c(t) = 0$.

$$e_m(t) = \frac{1}{2} e_t(t) + \frac{1}{2} e_c(t)$$

$$\text{peak } e_m = \frac{1}{2} E_{p_k} \qquad (3\text{-}10)$$

R_{26} and R_{27} should be selected such that

$$E_r = \frac{R_{26}}{R_{26} + R_{27}} V_1 = \frac{E_{pk}}{2} \quad .$$

A potentiometer may be used for R_{27}, as shown in the schematic diagram, to provide an adjustable reference, E_r, for precise adjustment of the modulator. The potentiometer may then be replaced by fixed resistors with values corresponding to the voltage division provided by the

potentiometer. The combination of $R_{26} + R_{27}$ should be large in order to reduce quiescent power consumption. Letting $R_{26} + R_{27} = 200$ k will provide satisfactory results. The value of R_{22} is not critical; however, it should be smaller than the input impedance of A_{22} and A_{23}.

R_{20} is selected to be much smaller than R_{22} and large enough to prevent overloading A_{11} when the zener voltage of D_{21} or D_{22} is exceeded.

Calculate max e_c, the value of $e_c(t)$ required to obtain τ_{max} by solving (3-10) for e_c and let $\tau = \tau_{max}$ and $R_c = R_t = R_{22}$.

$$\tau = \frac{TR_t}{2E_r(R_t + R_c)} e_c \qquad (3\text{-}10)$$

$$\max e_c = \frac{4\tau_{max} E_r}{T}$$

Select D_{21} and D_{22} to have zener voltages which are approximately equal to max e_c. The exact value of the zener voltage should be determined experimentally.

D. Input Stage and Amplifier Configurations

The input stage is shown in Fig. 2-1. The first consideration is the selection of A_{11}. A_{11} should have the following characteristics:

high gain;

high input impedance;

low output impedance;

low offset voltage;

low drift;

low quiescent power consumption;

and, a symmetric, bipolar output.

R_{11}, as mentioned in Chapter 6, serves a dual purpose in determining the gain of the input stage and the gain of the overall closed loop amplifier when used as a differential amplifier or a non-inverting amplifier. For instance, in the differential amplifier of Fig. 6-3, the closed-loop gain is,

$$A_v = \frac{R_{11}}{R_2} = \frac{R_3}{R_1} \quad . \tag{6-4}$$

The gain of the input stage is,

$$A_i = \frac{R_{11} + R_{12}}{R_{11}} \quad . \tag{2-1}$$

It is desirable that the gain of the input stage be large in order that the overall amplifier will have a high open-loop gain.

Notice, from (2-1) that for A_i to be large, $R_{11} \ll R_{12}$. Also, from (6-4), for A_v to be greater than 1, $R_{11} > R_2$. Thus,

$$R_2 < R_{11} \ll R_{12} \quad .$$

Also, R_2 should be as large as possible since from (6-5),

$$Z_{in} = R_1 + R_2 \quad , \tag{6-5}$$

and generally a high input impedance is desired. A similar analysis of the non-inverting amplifier would yield similar restrictions on R_{11} and R_{12}. For the inverting amplifier, R_{11} does not affect the closed loop gain of the overall amplifier, and R_{11} and R_{12} may be selected without

regard to overall amplifier considerations.

Considering all of the above restrictions it is apparent that R_{12} should be as large as possible. $R_{12} = 5M\Omega$ has been used successfully. $A_i = 1000$ should prove satisfactory in most applications. After R_{12} and A_i have been decided upon, R_{11} may be calculated by rewriting (2-1) as

$$R_{11} = \frac{R_{12}}{A_i - 1} \quad .$$

If a differential amplifier is desired, as shown in Fig. 6-3, choose

$$R_2 = \frac{R_{11}}{A_v} \quad ,$$

$$R_1 = R_2 \quad , \text{ and}$$

$$R_3 = R_{11} \quad .$$

If the non-inverting configuration is desired, as in Fig. 6-2, choose R_{11} and R_{12} as before, and noting that

$$A_v = \frac{R_{11} + R_3}{R_{11}} \quad , \tag{6-3}$$

select

$$R_3 = (A_v - 1)\, R_{11} \quad .$$

For the inverting amplifier, select R_{11} and R_{12} such that (2-1) yields a satisfactory value for A_i. Then choose R_1 and R_3 such that

$$A_v = -\frac{R_3}{R_1} \tag{6-1}$$

yields the required overall voltage gain. Also, the input impedance is,

$$Z_{in} = R_1 \ , \qquad (6\text{-}2)$$

therefore, R_1 must be chosen large enough to satisfy input impedance requirements.

Zener diodes D_{11} and D_{12} are selected with a zener voltage greater then max e_c and less than the saturated output voltage of A_{11}. Diodes D_{13} and D_{14} are small signal diodes. These diodes along with the pulse-width limiting circuitry allow the amplifier to withstand extremely large input voltages without exceeding the maximum power output or damaging the amplifier.

When current feedback is desired, as in Fig. 6-4(b), a small sampling resistor, R_I, must be inserted in series with the load, and the feedback taken across this element. R_I should be small to minimize power loss in this resistor. With G, the transconductance specified and R_I selected, the required A_v is given by (6-8).

$$G = \frac{A_v}{R_I} \ . \qquad (6\text{-}8)$$

Once A_v is determined, the resistors R_1, R_2, and R_3 are determined as before.

The circuitry and component values needed for compensating the input stage and for nulling the offset, as mentioned in Chapters 6 and 2, depend on the amplifier used in the input stage. This will be treated in the design example in Chapter 9.

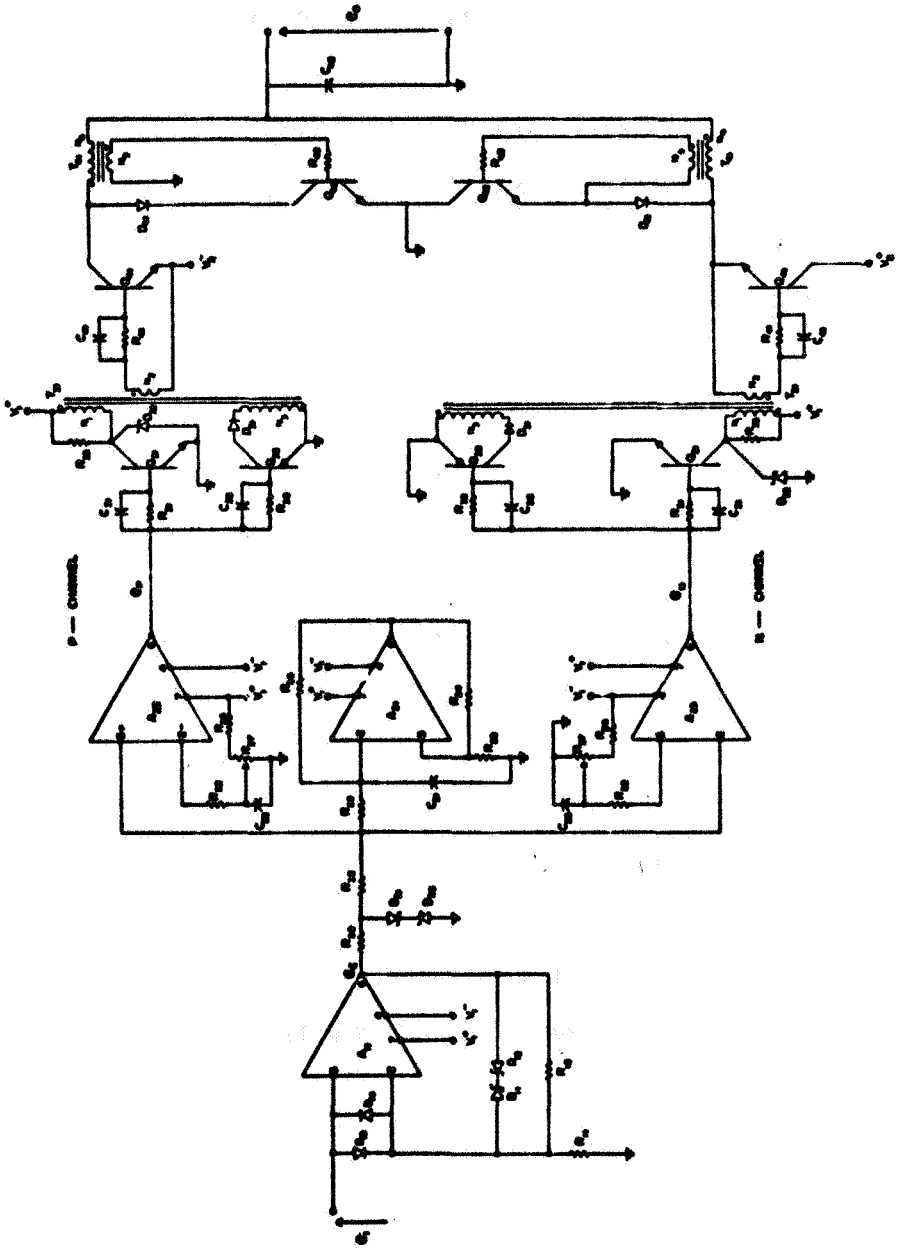

Fig. 8-2--Basic schematic diagram of a class-D amplifier.

9. DESIGN EXAMPLE

This chapter presents a schematic diagram and parts list for a class-D, d-c amplifier which was designed using the procedure presented in Chapter 8. The design specifications are given in Table 9-1. The schematic diagram of the amplifier is shown in Fig. 9-1, and the parts list is given in Table 9-2. The amplifier is in a differential input configuration with current feedback. The switching frequency is 20 kHz., considerably higher than that which is required to provide an upper cutoff freq ncy of 100 Hz. as specified in Table 9-1. A switching frequency of 20 kHz. was chosen to permit the use of smaller transformers and to simplify the filter design.

The μA709 integrated-circuit operational amplifier was selected for use in the input stage. The offset nulling circuitry composed of R_{13}, R_{14}, and R_{15} is the circuitry which is recommended by the manufacturer.[2] The compensation components R_{16}, C_{11}, and C_{12} were chosen to stabilize the overall closed-loop amplifier.

Several tests were made of the performance of the class-D amplifier. The results of these tests are presented graphically. Fig. 9-2 shows the low-level linearity of the amplifier at -40°C., 25°C., and 130°C. There was a dead zone of approximately 0.008 volts at all temperatures. The transfer characteristic of the amplifier is shown in Fig. 9-3. The d-c power efficiency of the class-D amplifier is shown in Fig. 9-4. The d-c efficiency was calculated as d-c power output to the load divided by average power from all power supplies. The power consumption of

TABLE 9-1

SPECIFIED PARAMETERS FOR DESIGN EXAMPLE

R_L = 9.8Ω
P_o = 150 watts
f_2 = 100 Hz.
V_2 = ± 60 volts
V_1 = ± 12 volts
Current feedback, G = 0.2 amp/volt.
Differential input configuration.

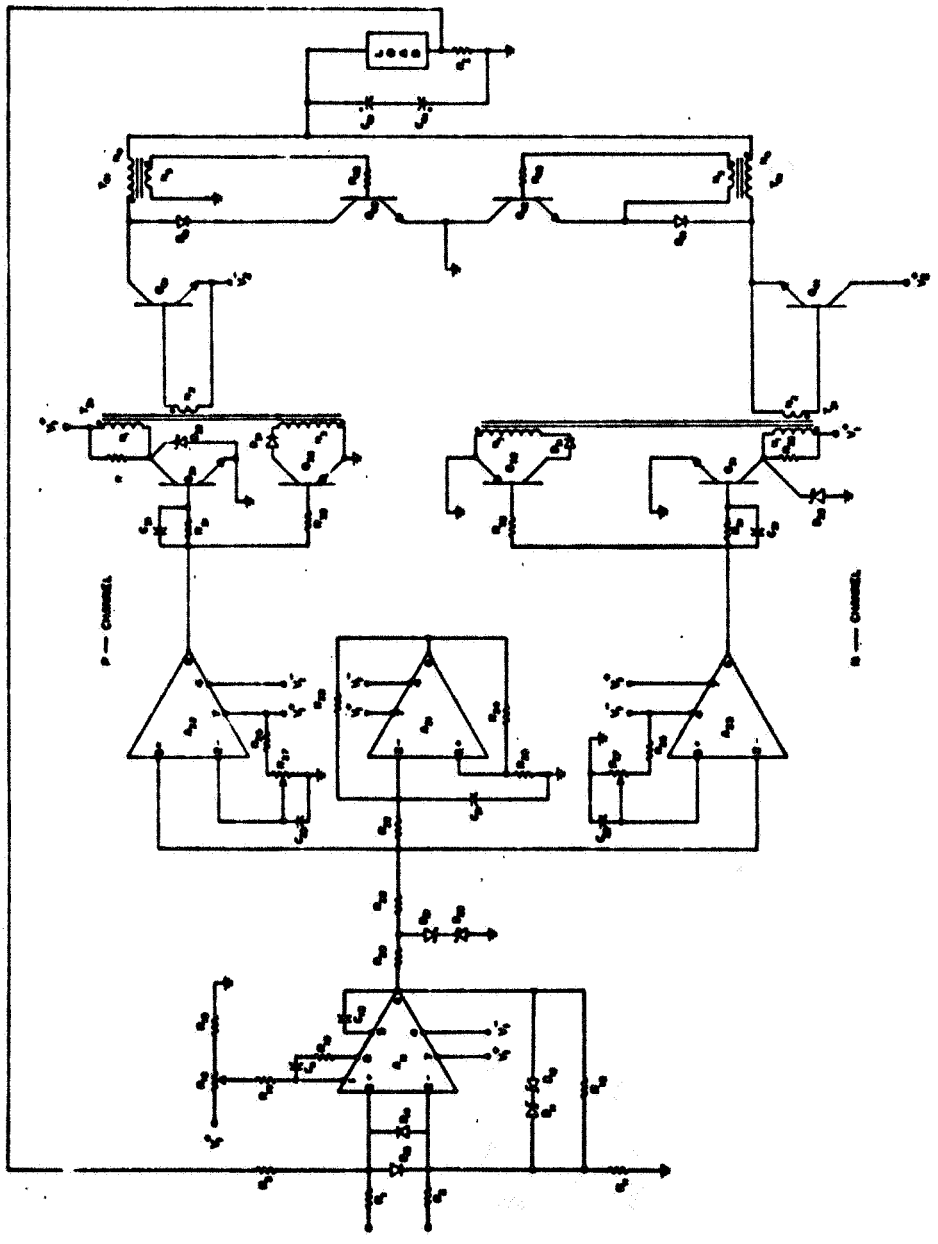

Fig. 9-1--Schematic diagram of a 150-watt, class-D, d-c amplifier with differential input and current feedback.

TABLE 9-2

CLASS-D AMPLIFIER PARTS LIST

Reference Symbol	Description
A_{11}	Linear integrated circuit, μA709 (Fairchild)
A_{21}	Same as A_{11}
A_{22}	Same as A_{11}
A_{23}	Same as A_{11}
C_{11}	Fixed Mylar capacitor, 3.0 μF., 50 Vdc.
C_{12}	Fixed mica capacitor, 20 pF., 100 Vdc.
C_{21}	Fixed mica capacitor, 0.005 μF., 100 Vdc.
C_{22}	Fixed ceramic capacitor, 0.003 μF., 100 Vdc.
C_{31}	Fixed ceramic capacitor, 680 pF., 100 Vdc.
C_{41}	Fixed tantalum capacitor, 365 μF., 100 Vdc.
D_{11}	Zener diode, 1N755
D_{12}	Same as D_{11}
D_{13}	Diode, 1N4448
D_{14}	Same as D_{13}
D_{21}	Zener diode, 1N4360
D_{22}	Same as D_{21}
D_{31}	Diode, 1N3071
D_{32}	Zener diode, UZ5210 (Unitrode)
D_{41}	Diode, 1N3891
Q_{31}	Transistor, 2N4862
Q_{32}	Transistor, 2N3485
Q_{41}	Transistor, SDT 8801 (Solitron)
Q_{42}	Transistor, 2N2814
R_1	Fixed resistor, 49.9 kΩ, 1%, 1/4 watt
R_2	Same as R_1
R_3	Fixed resistor, 1000Ω, 1%, 1/4 watt
R_{11}	Same as R_3
R_{12}	Fixed resistor, 1MΩ, 1%, 1/4 watt
R_{13}	Fixed resistor, 1.5 kΩ, 1%, 1/4 watt
R_{14}	Fixed resistor, 475 kΩ, 1%, 1/4 watt
R_{15}	Potentiometer, 50 kΩ, 5%, 1/4 watt
R_{16}	Same as R_1
R_{20}	Fixed resistor, 2.67 kΩ, 1%, 1/4 watt
R_{22}	Fixed resistor, 20 kΩ, 1%, 1/4 watt
R_{23}	Fixed resistor, 13.5 kΩ, 1%, 1/4 watt
R_{24}	Fixed resistor, 68.1 kΩ, 1%, 1/4 watt
R_{25}	Fixed resistor, 15 kΩ, 1%, 1/4 watt
R_{26}	Fixed resistor, 100 kΩ, 1%, 1/4 watt
R_{27}	Same as R_{15}

TABLE 9-2 — CONTINUED

Reference Symbol	Description
R_{31}	Fixed resistor, 4700 Ω, 10%, 1/4 watt
R_{32}	Fixed resistor, 22 kΩ, 10%, 1/4 watt
R_{33}	Fixed resistor, 10 kΩ, 10%, 1/4 watt
R_{42}	Fixed resistor, 5.1 Ω, 5% 2 watt
R_I	Fixed, non-inductive wire-wound resistor, 0.1 Ω, 0.5%, 10 watt
T_{31}	Transformer, core 55206 (Magnetics) N_1, 818 turns, AWG no. 34 N_2, 106 turns, AWG no. 26 N_3, 1000 turns, AWG no. 37
T_{41}	Transformer, core 55310 (Magnetics) N_4, 29 turns, AWG no. 17 N_5, 2 turns, AWG no. 17

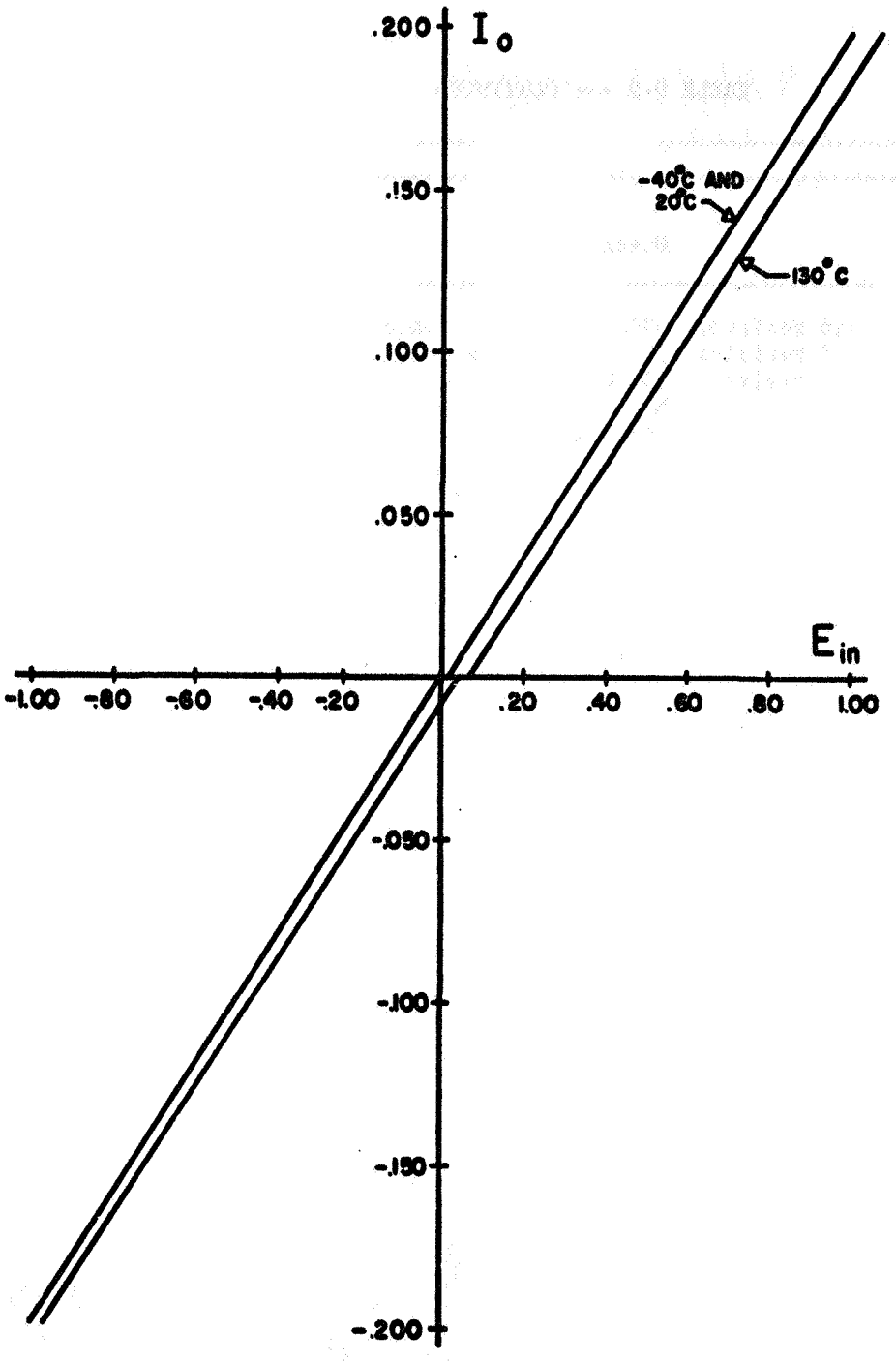

Fig. 9-2--A graph showing the low-level linearity of the class-D amplifier at -40°C, 25°C., and 130°C.

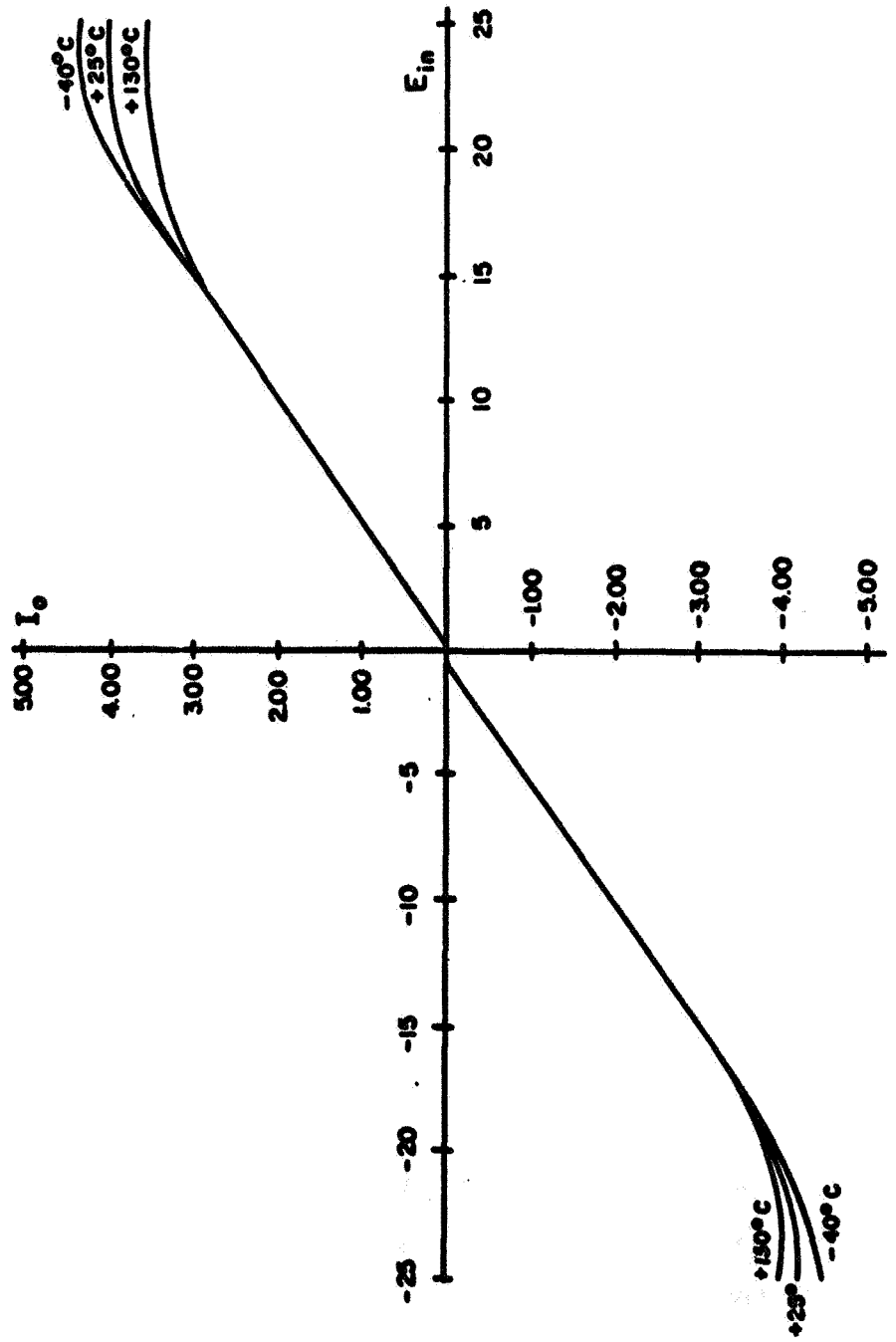

Fig. 9-3--The input-voltage to output-current transfer characteristic of the class-D amplifier.

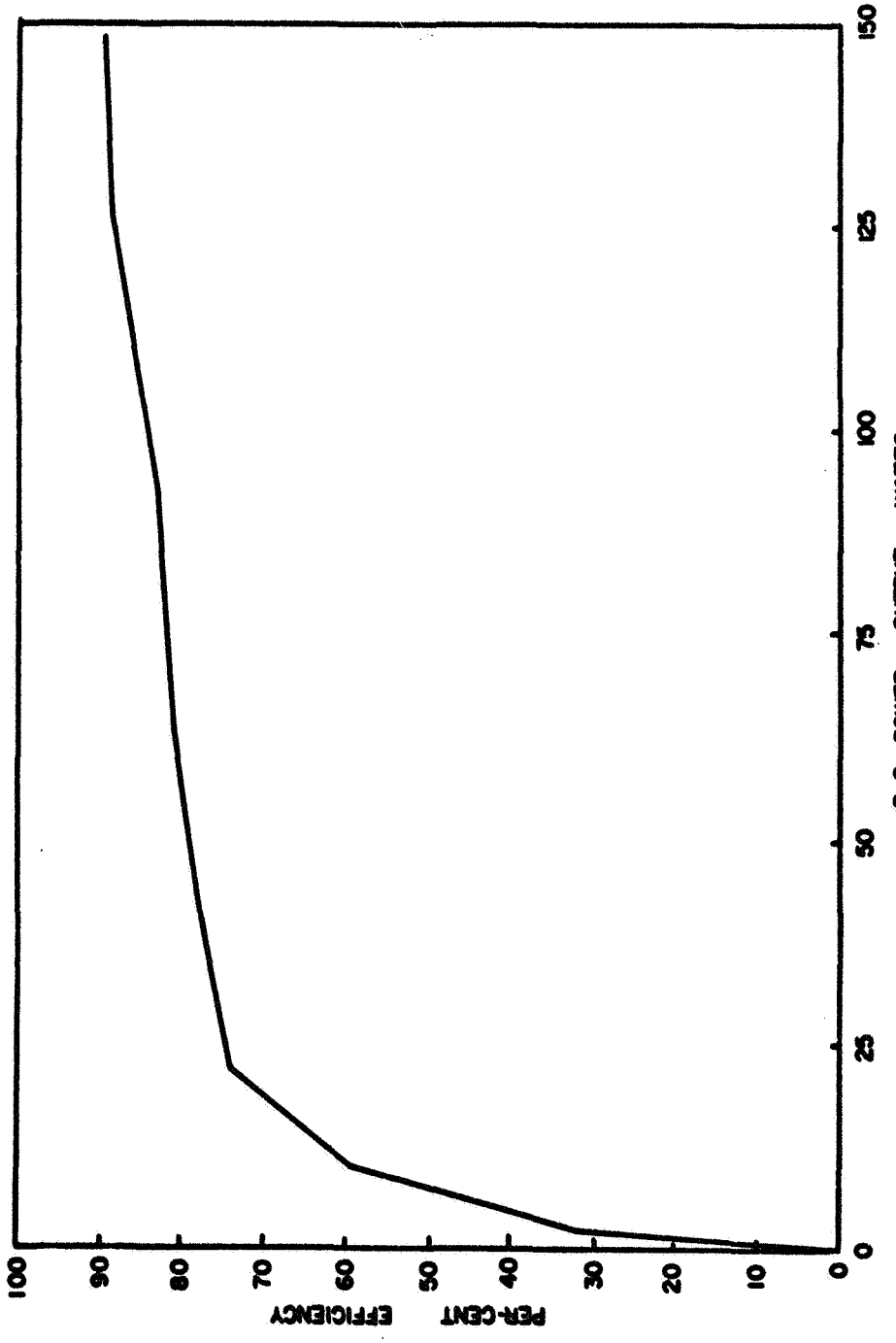

Fig. 9-4--A graph showing the d-c efficiency of the class-D amplifier.

the input stage, modulator, and driver is plotted as a function of power output in Fig. 9-5. It should be noted that quiescent power consumption is less than 250 milliwatts. Plots of the gain and the phase characteristics of the amplifier are shown in Fig. 9-6. The zero db. level of the gain characteristic corresponds to an RMS output voltage of 14.1 volts.

Fig. 9-7 is an oscilloscope photograph of the output current waveform with the amplifier operating into an inductive load. The load, which simulates a torque motor, is 9.8Ω in series with an inductance of 36 mH. The frequency of the signal shown is approximately 15 Hz.

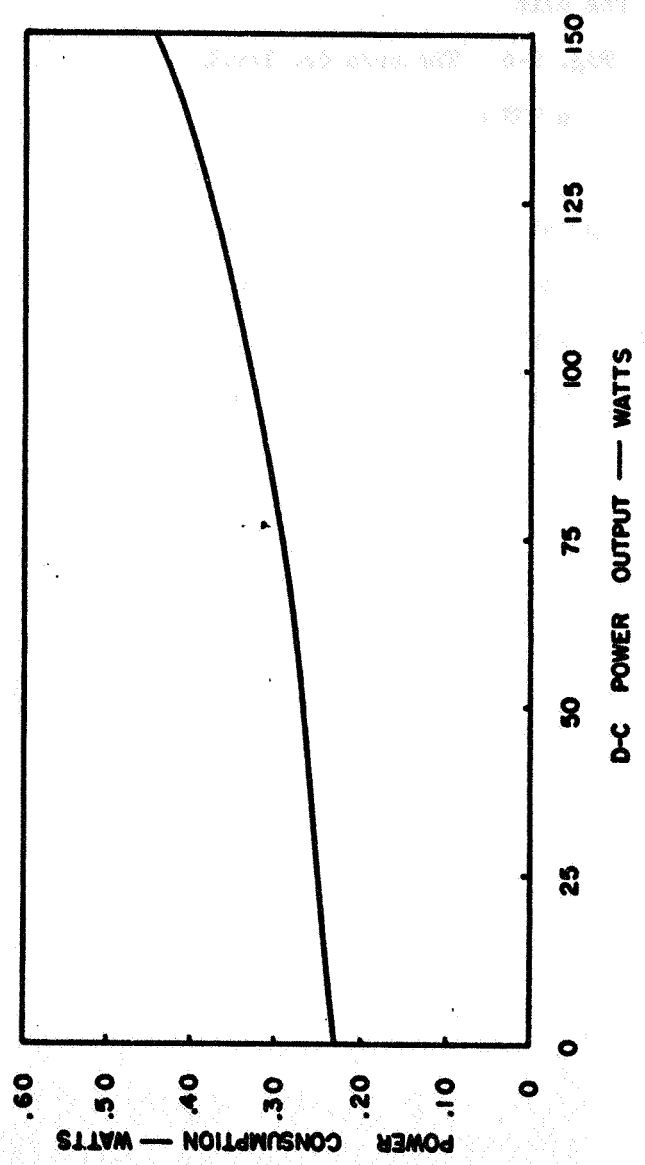

Fig. 9-5--A graph showing the power consumption of the input stage, modulator, and driver as a function of d-c power output.

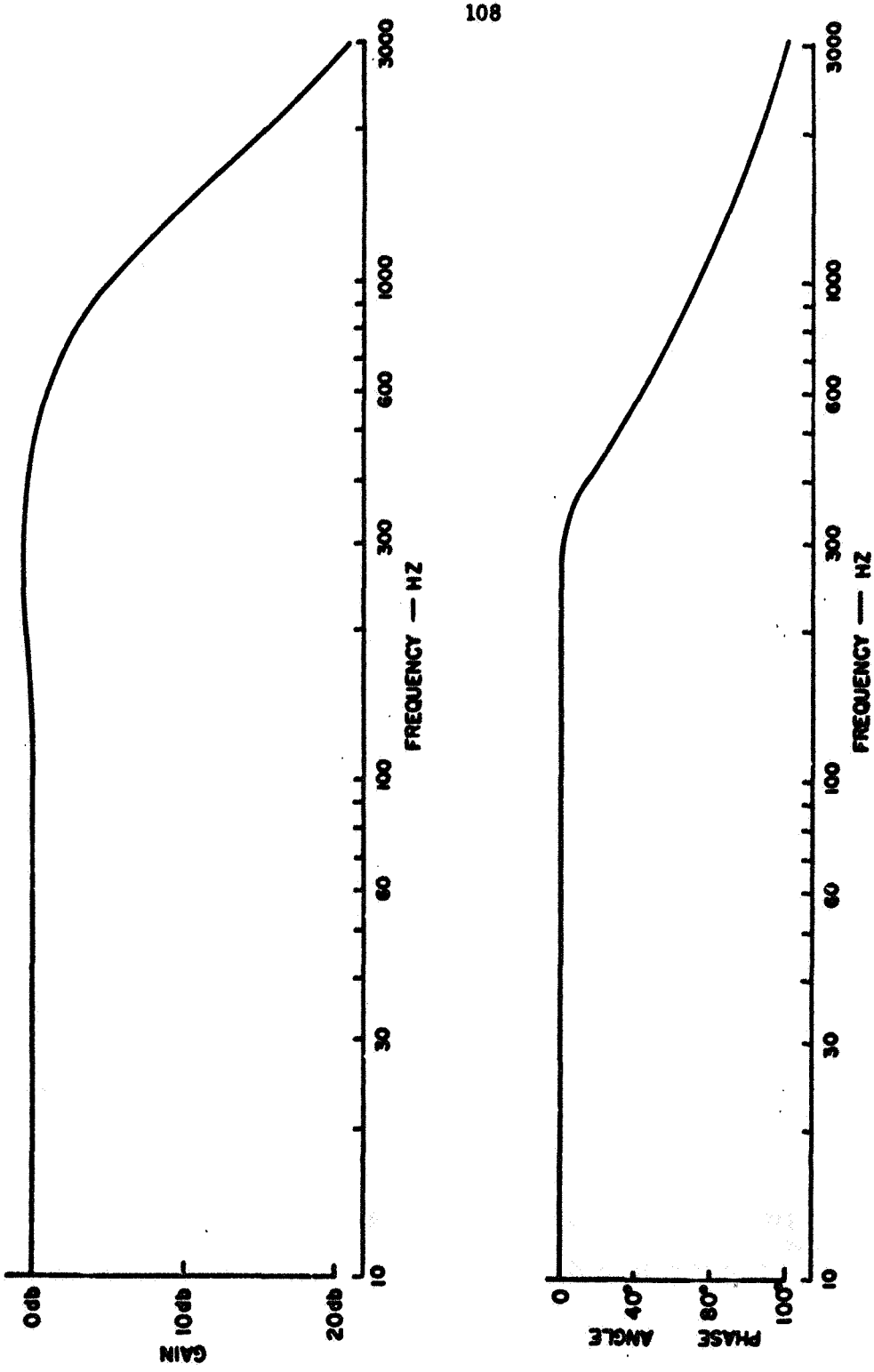

Fig. 9-6--The gain and phase characteristics of the class-D amplifier.

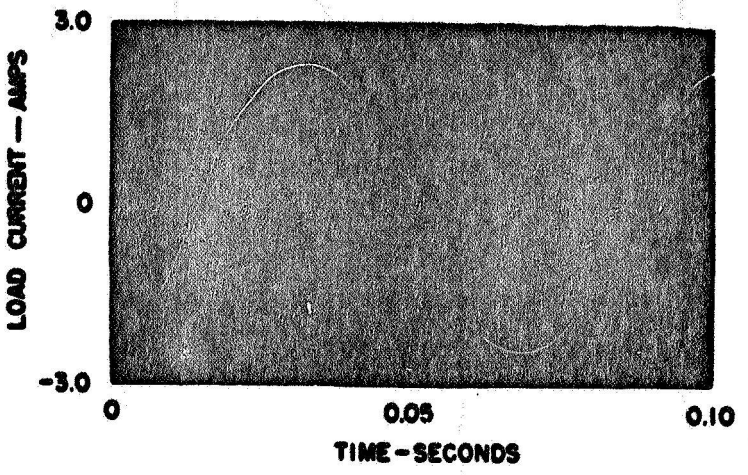

Fig. 9-7--Output current waveform due to a 15-Hz. sinusoidal input signal with the class-D amplifier operating into a inductive load.

10. CONCLUSIONS

The class-D amplifier exhibits several characteristics which are advantageous in a power amplifier. The class-D amplifier, which was presented as a design example in Chapter 9, produced bipolar output voltages from d-c to approximately 800 Hz with high efficiency. Figures 9-2 and 9-3 demonstrate the linearity which was obtained using negative feedback. The use of the saturated-switching mode of operation in the driver and output stages, and the use of integrated circuits in the other stages resulted in a quiescent power consumption of less than 0.25 watts, as shown in Fig. 9-5. It may also be noted that the power consumption of the first three stages of the amplifier is relatively quite small in comparison with the power output of the amplifier.

In order to depict the d-c efficiency which may be expected of a class-D amplifier using the output circuit which has been presented, the d-c efficiency of several class-D amplifiers, which were constructed, was plotted in Fig. 10-1. In order to allow direct comparison the data was plotted as a function of per-cent power output, and the region where the curves fell was shaded. Class-D amplifiers rated at less than the 150 watts tended to be more efficient, and the curves for these fell generally along the upper edge of the shaded region. A 365-watt design produced the curve which follows the lower edge of the shaded region.

Although the circuit presented is highly efficient, a disadvantage is the need for two separate power supplies for the output stage. Each

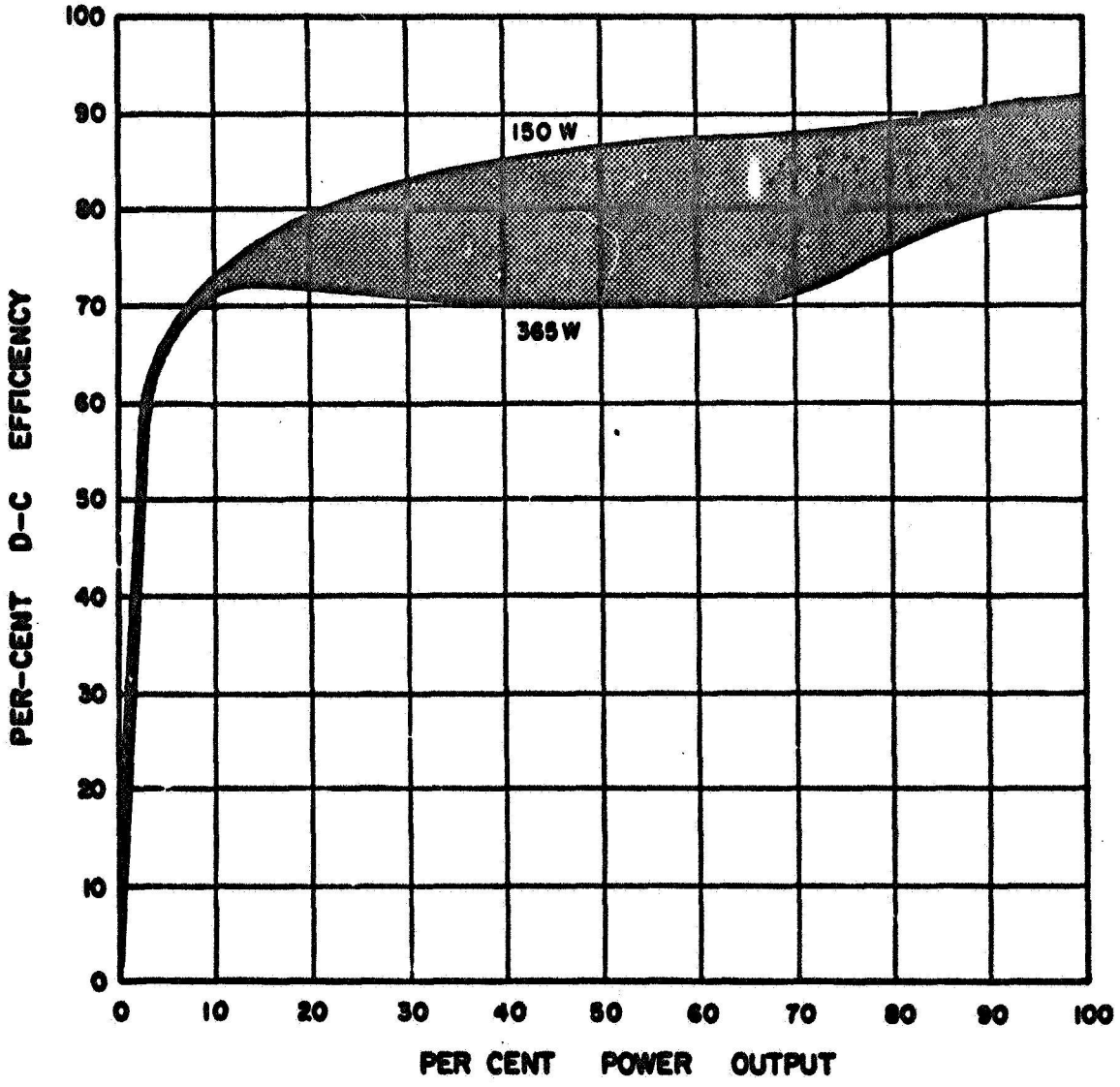

Fig. 10-1--A graph showing the cumulative d-c efficiencies of several class-D amplifiers.

power supply must be able to supply the maximum power requirement at full output. It may also be noted that, due to the direct-coupled nature of the output circuit, the maximum output voltage cannot be greater than the supply voltage.

Radio-frequency interference may be a problem in some applications. This interference is primarily the result of voltage transients associated with the inductive elements in the output stage.

Since low-pass filtering is employed to demodulate the output signal, there will be considerable phase shift in the output signal near the upper cutoff frequency. Therefore, when using negative feedback, proper care must be taken to assure stability.

On the basis of the information presented, class-D amplification appears to be suitable for power amplification where high efficiency and low quiescent power consumption are desirable. It has also been shown that good linearity may be obtained when negative feedback is employed.

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APPENDIX

LIST OF SYMBOLS

a - Lumped constant defined in (5-19).

A_i - Closed loop voltage gain of input stage.

A_v - Closed loop voltage gain of overall amplifier.

BV_{BE} - Base-emitter breakdown voltage.

E - Ratio of d-c output voltage to supply voltage.

e_{BE} - Emitter - base voltage.

e_c - Control voltage (output of the input stage).

e_d - Difference voltage between e_f and e_i.

e_e - Emitter voltage.

e_f - Feedback voltage.

e_i - Input voltage.

e_m - Scaled sum of e_c and e_t in modulator.

e_N - Output voltage of the N-channel comparator.

e_o - Output voltage across the load.

E_o - D-C output voltage across the load.

e_p - Output voltage of the P-channel comparator.

E_p - Peak value of e_p.

E_{pk} - Peak value of e_t.

E_r - Reference voltage in modulator.

e_s - Square wave output voltage of the multivibrator.

e_s' - Scaled square wave at non-inverting terminal of A_{21}.

E_s - Peak value of e_s.

e_t - Triangular waveform generated by the multivibrator.

e_1 - Driver transformer primary winding voltage.

e_2 - Driver transformer secondary winding voltage.

e_3 - Driver transformer auxiliary (shorting) winding voltage.

e_4 - Voltage across inductor L_4 (primary of output-circuit transformer).

e_5 - Voltage across secondary (clamping winding) of output-circuit transformer.

$e_{4\ max}$ - Maximum value of e_4.

$e_{5\ max}$ - Maximum value of e_5.

f_s - Switching frequency (of the pulse-width modulated waveform).

f_2 - Upper cutoff frequency of the amplifier.

g - Ratio of minimum to maximum current in each driver pulse.

G - Closed-loop transconductance of the overall amplifier when current feedback is used.

I - Normalized value of I_p.

I_B - Base saturation current at maximum collector current.

I_L - D-C load current.

I_o - Average output current to the load.

I_p - Peak collector current in the output transistor.

i_1 - Driver transformer primary current.

i_2 - Driver transformer secondary current.

I_2 - Average current from the V_2 supply.

i_4 - Current through inductor L_4(primary of output-circuit transformer).

K - Ratio of E_s to E_{pk} for multivibrator.

K' - Scaling factor used in modulator design (p. 25).

L_1 - Primary inductance of driver transformer.

L_2 - Secondary inductance of driver transformer.

L_4 - Primary inductance of the output-circuit transformer.

max e_c - Control voltage required for maximum pulse-width.

max E_o - Maximum d-c output voltage.

max I_c - Maximum collector current for a transistor.

max I_{FWD} - Maximum forward current for a diode.

max i_1 - Peak primary current in the driver transformer.

$\frac{N_1}{N_2}$ - Primary-to-secondary turns ratio of driver transformer.

N_4 - Number of turns on primary of the output-circuit transformer.

N_5 - Number of turns on the secondary of the output-circuit transformer.

P_m - Maximum d-c power output.

P_o - Output power to the load.

P_2 - Input power from the V_2 supply.

R_I - Current-sampling resistor used in current feedback configuration.

R_L - Load resistance.

R_s - Source resistance.

R_{SAT} - Collector-emitter saturation resistance at maximum collector current.

T - Period of the pulse-width modulated (switching) waveform.

t_f - Fall time for a transistor.

t_s - Storage delay time for a transistor.

V_{BE} - Base-emitter saturation voltage at maximum collector current.

V_1^+ - Positive supply voltage for the input stage, modulator, and driver.

V_1^- - Negative supply voltage for the input stage, modulator, and driver.

V_2^+ - Positive supply voltage for the output stage.

V_2^- - Negative supply voltage for the output stage.

Z_{in} - Input impedance of the overall amplifier.

α - Measure of non-linearity of $e_t(t)$.

α' - Per-cent non-linearity of $e_t(t)$.

Δ - Ratio of pulse width to period of switching waveform.

η - Overall amplifier efficiency.

η_o - Output stage efficiency.

τ - Modulated pulse width (on-time of the driver and output transistors).

τ' - Clamping interval of the output circuit.

τ'' - Time between the end of the clamping interval and the beginning of the next output pulse(dead-time).

τ_{max} - Maximum pulse width (maximum on-time for the driver and output transistors).

ω_c - Angular frequency of the control signal.

ω_s - Angular switching frequency.

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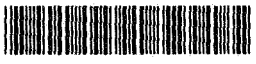

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