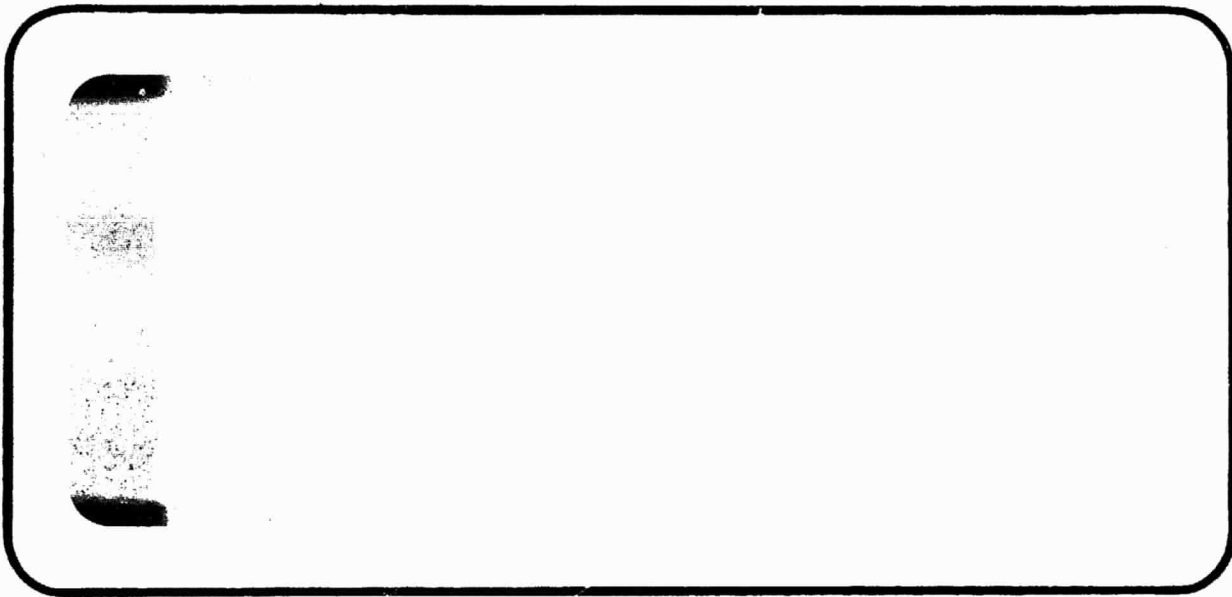


General Disclaimer

One or more of the Following Statements may affect this Document

- This document has been reproduced from the best copy furnished by the organizational source. It is being released in the interest of making available as much information as possible.
- This document may contain data, which exceeds the sheet parameters. It was furnished in this condition by the organizational source and is the best copy available.
- This document may contain tone-on-tone or color graphs, charts and/or pictures, which have been reproduced in black and white.
- This document is paginated as submitted by the original source.
- Portions of this document are not fully legible due to the historical nature of some of the material. However, it is the best reproduction available from the original submission.

John + Don 7/12



FACILITY FORM 602

N 00 0050	
(ACCESSION NUMBER)	(THRU)
63	1
(i AGES)	(CODE)
073712	11
(NASA CR OR TMX OR AD NUMBER)	(CATEGORY)

TRW.

SYSTEMS GROUP

ONE SPACE PARK • REDCNOO BEACH, CALIFORNIA



X

Final Report
for
Fast Response Solar Array Simulator
(25 June 1968 - 25 October 1968)
Contract No. NAS 5-11581

Prepared for:

Goddard Space Flight Center
Greenbelt, Maryland

Contracting Officer: J. A. Maloney
Technical Monitor: John Davis 7/6
f.

Prepared by:

TRW Systems Group
One Space Park
Redondo Beach, California

Project Engineer: David W. Zerbel

Approved:

[Signature]
for A. D. Schoenfeld

ABSTRACT

The objective of this contract was to perform tradeoff studies to determine the design requirements for a fast response solar array simulator capable of delivering output power in the range of 20 to 5000 watts. Evaluation of the tradeoff studies led to the selection of a reference design that includes the following features:

- ° Generation of the static and dynamic characteristics of the solar array through the use of a forward biased solar cell as an analog reference.
- ° Programming of these characteristics for variation in illumination and temperature with time by digital techniques.
- ° A 500w module as the basic building block for a 5000w system.
- ° Current accuracy of $\pm 0.5\%$ of the short circuit current setting.

TABLE OF CONTENTS

1. INTRODUCTION
2. TRADEOFF STUDIES
 - 2.1 Frequency and Transient Response
 - 2.2 Digital versus Analog Tradeoffs
 - 2.3 Optimization of Power Modules
 - 2.4 Output Accuracy Considerations
 - 2.5 Summary of Tradeoff Studies
3. DESIGN REQUIREMENTS
4. PRELIMINARY DESIGN
 - 4.1 Electrical Design
 - 4.2 Mechanical Design
5. SUMMARY
 - 5.1 General
 - 5.2 Materials Report
 - 5.3 New Technology
6. BIBLIOGRAPHY

LIST OF FIGURES

<u>Figure</u>		<u>Page</u>
1	Solar Cell Impedance Test	
2	Illuminated Cell, I vs V	
3	Illuminated Cell, Z vs f	
4	Illuminated Cell, R_p vs f	
5	Illuminated Cell, C_p vs f	
6	Forward Biased Cell, I vs V	
7	Forward Biased Cell, Z vs f	
8	Forward Biased Cell, R_p vs f	
9	Forward Biased Cell, C_p vs f	
10	Digital System Block Diagram	
11	Analog System Block Diagram	
12	Power Module Concept	
13	Locus of Operation	
14	Reference System Block Diagram	
15	Reference V - I Curve	
16	FRSAS System Block Diagram	
17	Series Regulator and Reference Stage	
18	Current Amplifier	

LIST OF TABLES

Table

I	Diode Impedance vs Voltage
II	Current and Voltage Accuracy
III	Variation of G
IV	Variation of g_{m1}
V	Variation of Z
VI	Preliminary Parts List

List of Symbols

- Z = solar cell impedance
- R_p = equivalent parallel resistance of solar cell
- C_p = equivalent parallel capacitance of solar cell
- θ = phase angle associated with solar cell impedance
- C_J = junction capacitance
- A_J = junction area
- V_J = junction potential
- C_D = diffusion capacitance
- I_d = diffusion current
- τ = minority carrier lifetime
- I_{sc} = short circuit current
- V_{oc} = open circuit voltage
- V_L = load (output) voltage
- I_L = load (output) current
- K = Boltzman's constant
- q = electron charge
- T = absolute temperature in °K
- $V_t = KT/q$
- n_s = the number of cells in series
- n_p = the number of cells in parallel
- I_s = the short circuit current of a single cell at the reference temperature and illumination
- I_o = the reverse saturation current of a single cell at the reference temperature and illumination

K_1 = a variable constant to account for variations in illumination due to sun angle and spinning
 t_R = risetime
 f_H = upper half power frequency
 I_R = reference current
 I_D = diode current
 V_D = diode voltage
 V_R = diode voltage when $I_D = I_R$
 $\mathcal{E}$ = error voltage
 T_R = the reference temperature
 ΔT = temperature variation
 H = current amplifier transfer function
 $n = n_s \frac{K T}{q}$
 P_{MP} = maximum power output of SAS
 V_s = maximum voltage of power supply
 I_s = maximum current of power supply
 V_{CE} = collector to emitter voltage of series regulating transistor(s)
 I_c = collector current of series regulating transistor(s)
 P_T = power dissipation of series regulating transistor(s)
 G_{CL} = closed loop gain
 Z_D = diode impedance
 G = transfer function of voltage amplifier
 M_I = current accuracy
 M_V = voltage accuracy
 $\mathcal{E}_{m1}$ = forward gain of voltage amplifier
 Z_L = load impedance
 R_L = load resistance

1. INTRODUCTION

This report contains the results of tradeoff studies which were performed to determine the design requirements for a fast response solar array simulator capable of delivering output power in the range of 20 to 5000 watts. This solar array simulator must simulate the static and dynamic characteristics of the solar array in a manner which allows other power subsystem components such as regulators to be tested and evaluated in a manner which is unconstrained or limited by improper or inaccurate array characteristic simulation. In addition the simulator must be capable of being programmed to allow variation of the characteristics as a function of time. The tradeoff studies were divided into four major areas:

- ° Frequency and transient response considerations
- ° Digital versus analog characteristic generation and programming
- ° Optimum power module size
- ° Accuracy considerations

Based on an evaluation of these tradeoffs a reference design was selected, design requirements were established and preliminary design calculations were performed to verify the ability of the reference design to meet the design requirements.

2. TRADE OFF STUDIES

2.1 Frequency and Transient Response

This study considered two basic areas. The first was to determine what are the AC characteristics of solar arrays and the second was to consider how important these characteristics are to typical regulators.

In order to determine the former a literature survey was first performed which uncovered little quantitative information on the AC characteristics of solar cells. Qualitatively the literature indicates that the cell exhibits a capacitive reactance; however, no information was found which showed how this capacitance varied as a function of cell area, current, voltage, or frequency. Therefore, it was decided to perform a simple test on a representative cell.

The cell chosen for the test was a silicon, 2 ohm-cm, n on p, 3.8 cm² cell. The test circuit is shown in Figure 1. The cell was subjected to a constant illumination of approximately 120 mw/cm² and was maintained at a constant temperature of 110°F. Various DC operating points were selected by varying the load resistor R₃. The resulting V-I curve is shown in Figure 2. An AC signal was injected with a wave analyzer and the resulting voltage vectors were also measured by the wave analyzer. From these three measurements the magnitude of the cell impedance, Z, and the phase angle, θ, were determined by the following relationships.

$$Z = \frac{V_1}{I_1} = \frac{V_1 R_2}{V_2}$$
$$\theta = \cos^{-1} \frac{V_1^2 + V_2^2 - V_3^2}{2 V_1 V_2}$$

A plot of Z vs frequency is shown in Figure 3. Knowing Z and θ the impedance can be separated into an equivalent circuit of a resistance, R_p, in parallel with a capacitance, C_p, by the following relationships.

$$R_p = \frac{Z}{\cos \theta}$$
$$C_p = \frac{\sin \theta}{2\pi f Z}$$

Solar Cell Impedance Test

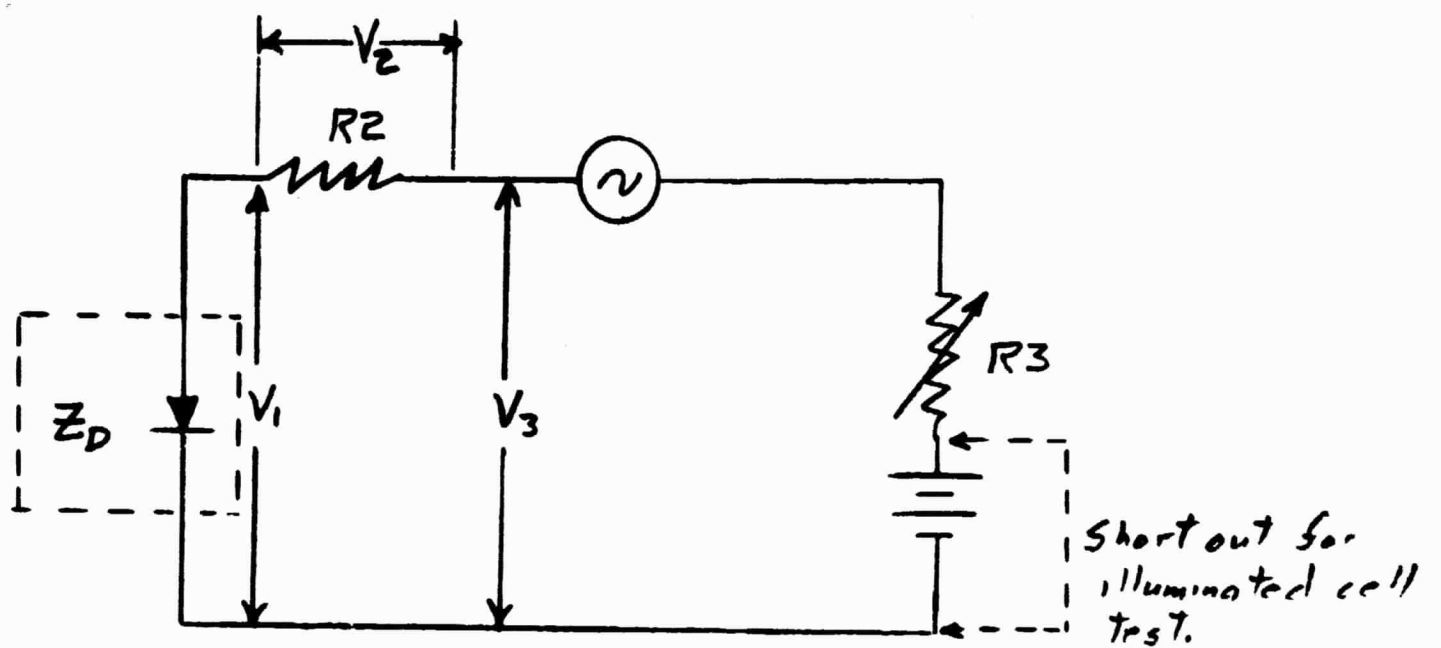


Figure 1

CURRENT-VOLTAGE CHARACTERISTICS FOR 2 x 2 CM SOLAR CELLS

DESIGNATION B 2
 INTENSITY 139.5 mw/cm²
 TEMPERATURE 20°C ± 1°C
 DIV. M. READINGS I_{sc} 135.4 ma, V_{oc} 573.9 mv
 STD. CELL NO. AT-17-135 STD. CELL I_{sc} 132.3 ma
 SPECIAL CONDITIONS
 TESTED BY RCS DATE 8-19-68

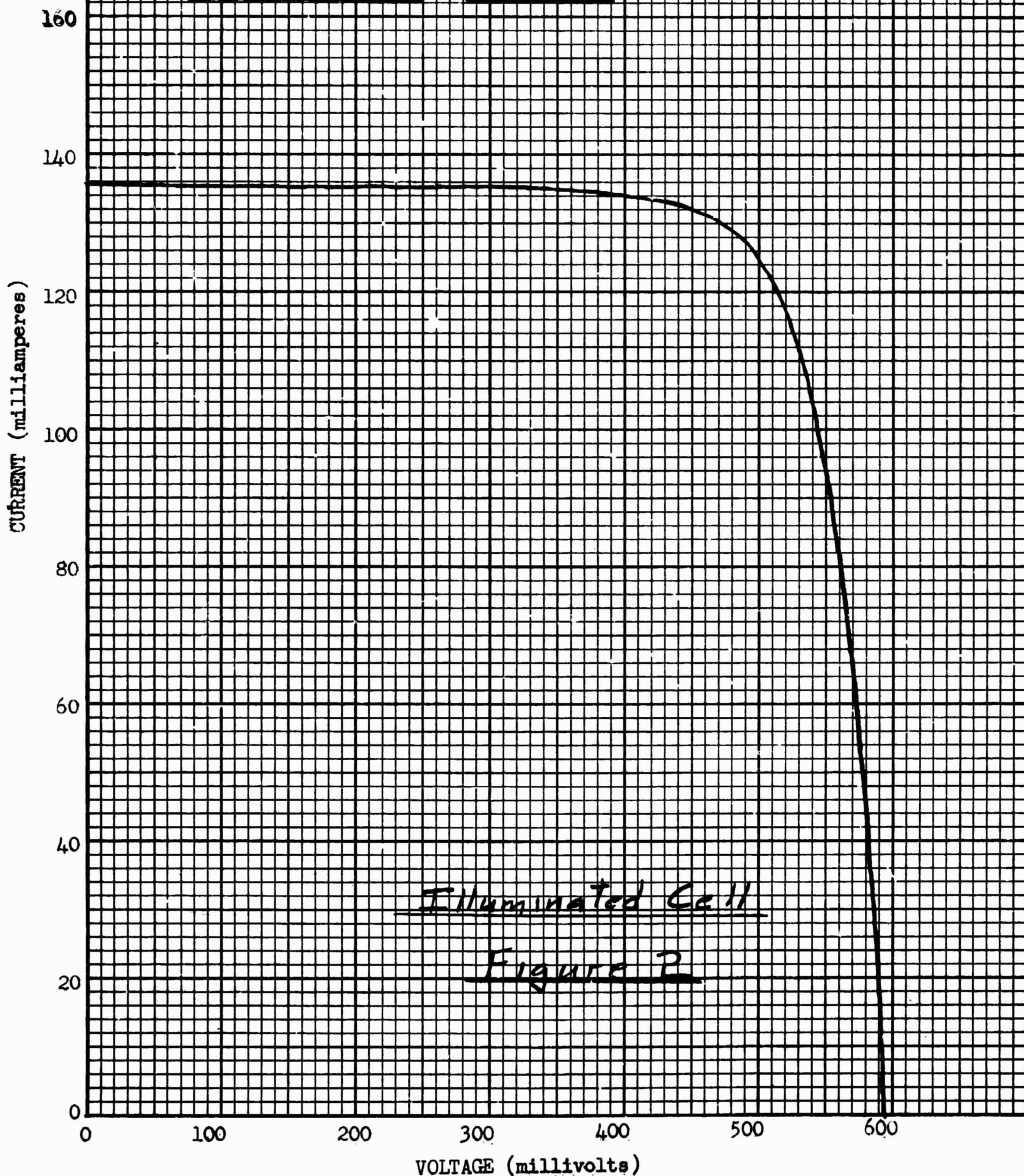
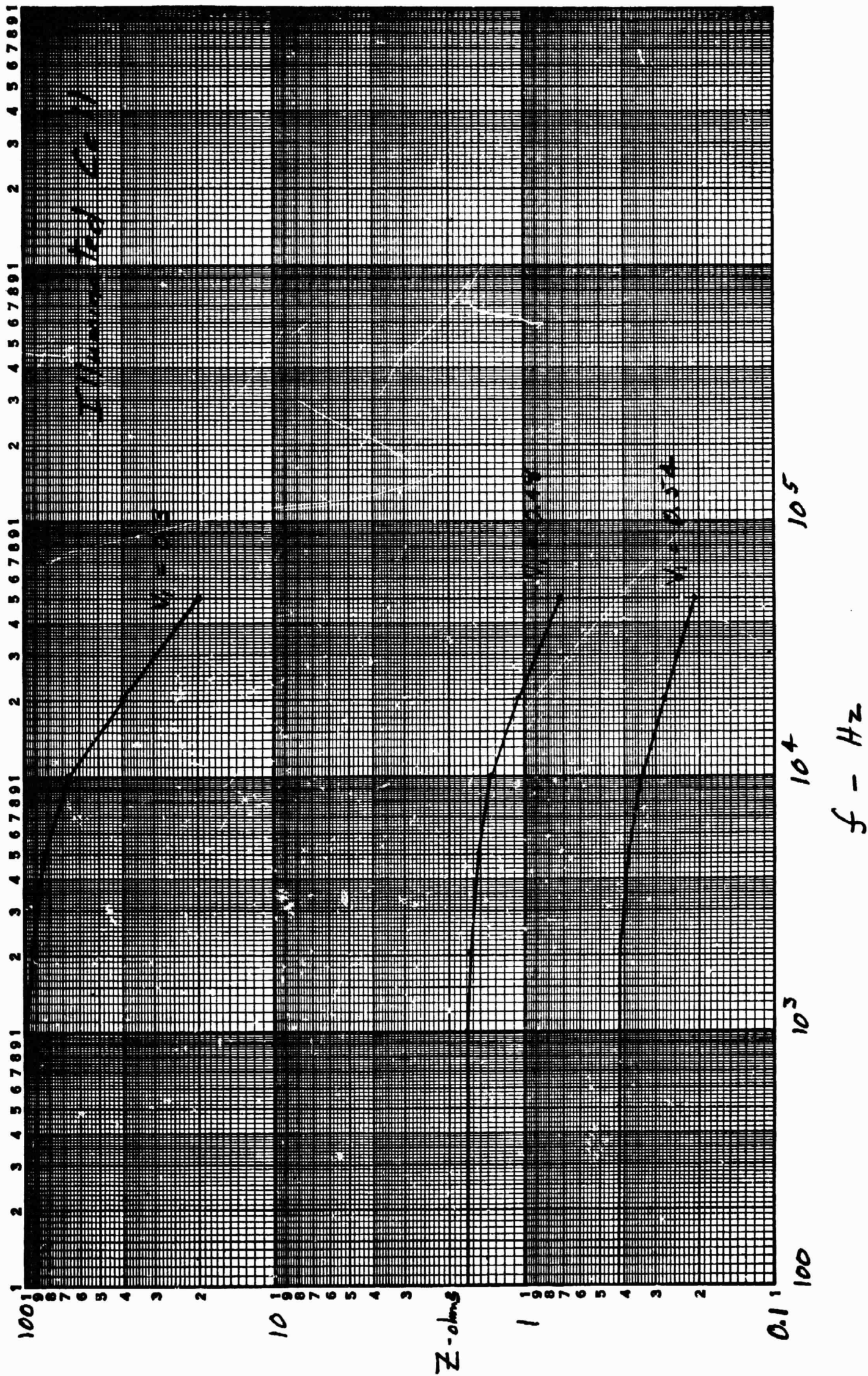


Figure 3



The results of this separation are shown in Figures 4 and 5.

This simple test was not as extensive or as accurate as would be required to reach any valid quantitative conclusions. However examination of the data does provide the following qualitative conclusions:

1. The impedance stays relatively constant out to 5 kHz regardless of operating point.
2. The capacitance seems to be inversely proportional to frequency out to about 10 kHz beyond which it is felt that inductive effects in the measurement circuitry were becoming significant.
3. Capacitance varies inversely with cell current.
4. Resistance begins to fall off with frequency at the same point as the impedance and with the same slope.

Examination of data from earlier tests performed at TRW reveals the same general conclusions. A single curve of impedance versus frequency for a Nimbus array also indicates a constant impedance up to about 5 kHz.

Considering this data and correlating it with junction device theory, it can be seen that the magnitude of the observed capacitances is much greater than can be accounted for by the concept of junction capacitance where

$$C_J \sim \frac{A_J}{V_J^{1/2}}$$

A_J = junction area

V_J = junction potential including built-in potential and any applied potential

However, if the concept of diffusion capacitance is examined where

$$C_D \sim I_D \tau$$

I_D = diffusion current across the junction due to the concentration gradient.

τ = minority carrier lifetime

Figure 4

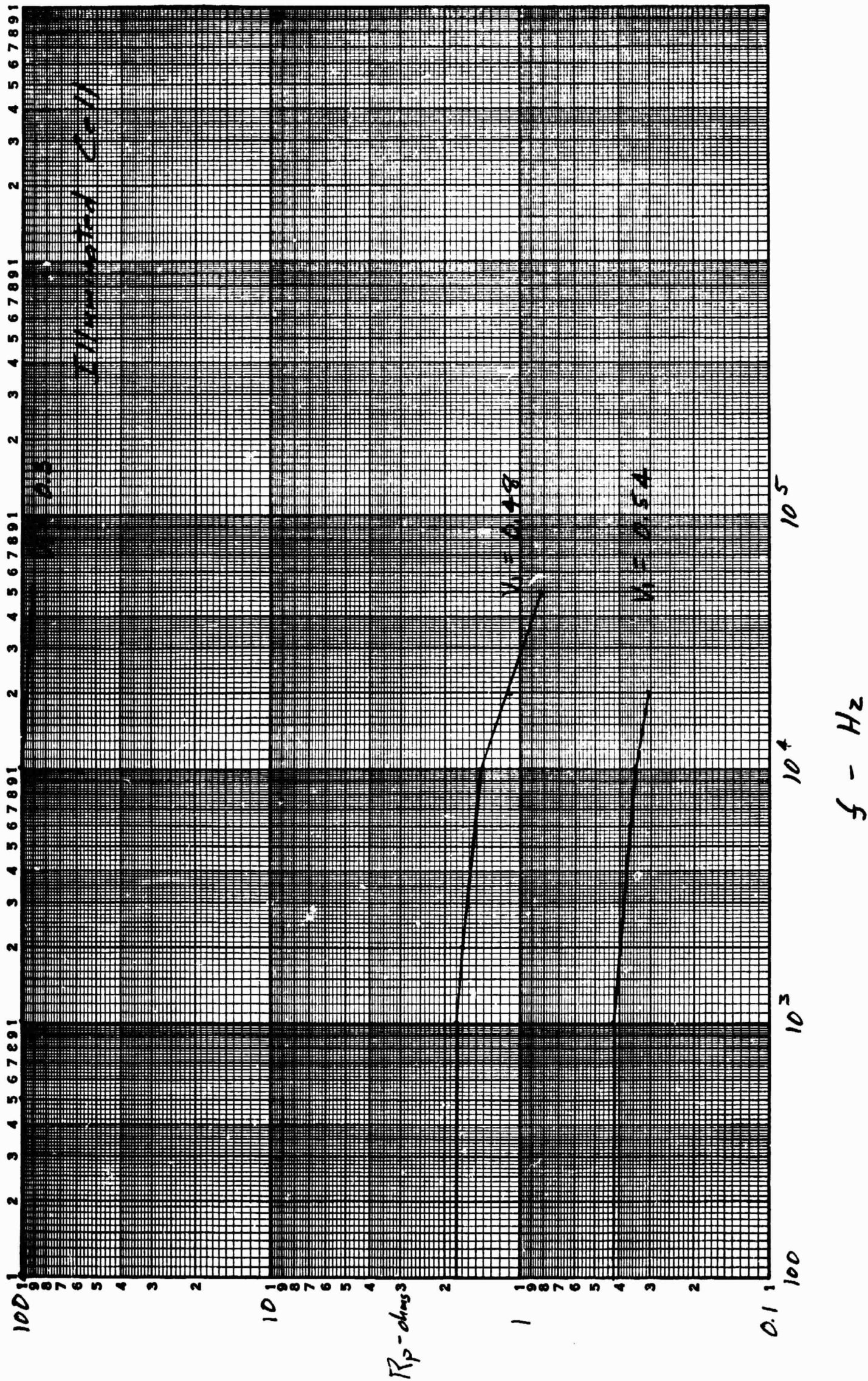
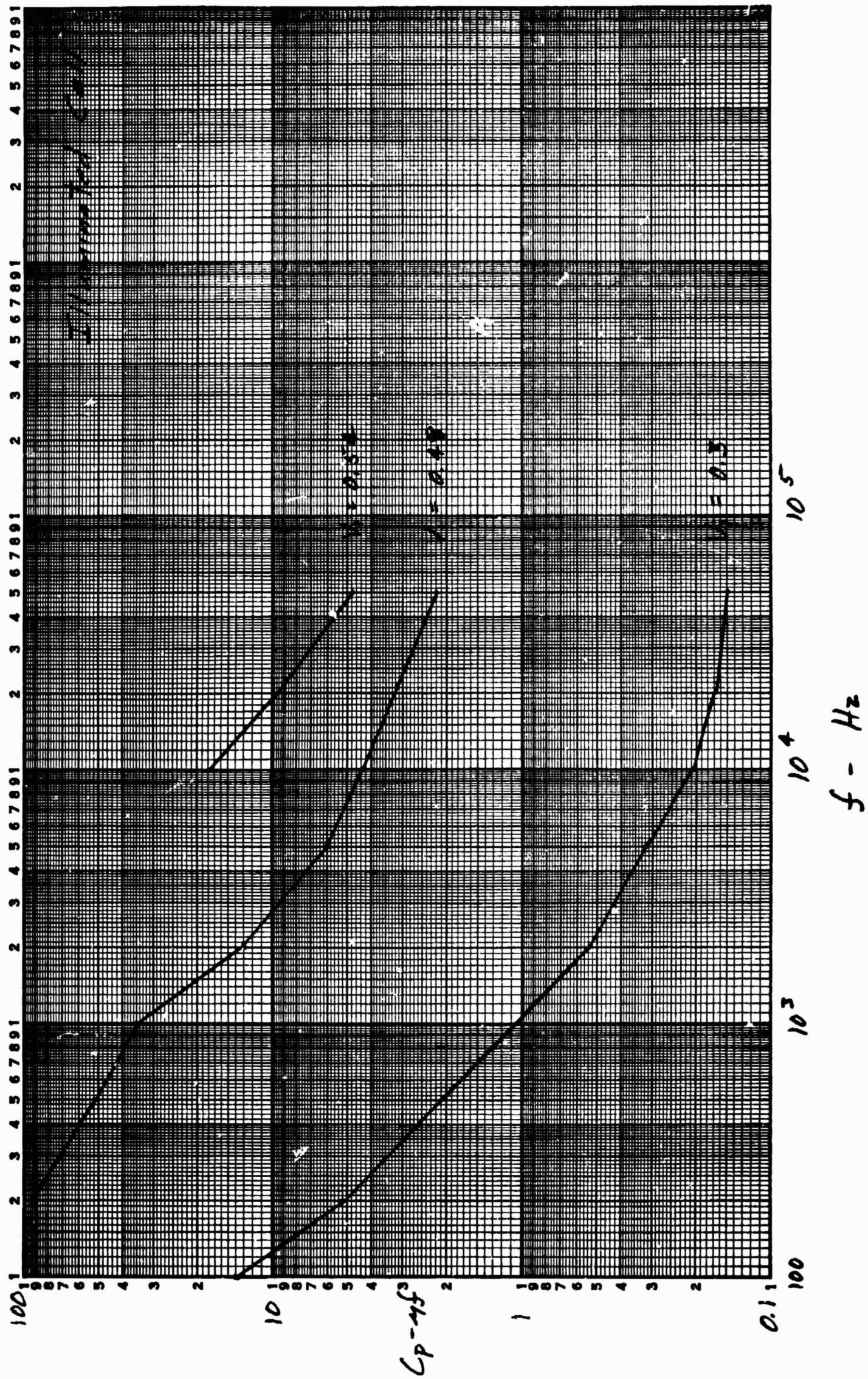


Figure 5



then the agreement is fairly close. Note that diffusion current across the junction is

$$I_d = I_{sc} - I$$

where

$$I_{sc} = \text{short circuit current}$$

$$I = \text{current in the external circuit}$$

(In a conventional forward biased diode the diffusion current is the same as the current in the external circuit.) Since diffusion capacitance may also be thought of as a variation of charge with a variation of voltage; i.e.,

$$C_D = \frac{\Delta Q}{\Delta V}^1$$

Then for a fixed amplitude AC voltage (ΔV), the amount of charge that can diffuse across the junction (ΔQ) is a function of the frequency; and as the frequency increases the time required for charge far from the junction to diffuse to the junction becomes comparable to the period of the AC voltage.¹ Therefore as frequency increases ΔQ decreases and therefore C_D decreases. This explanation seems to fit well with the observed test data and explains the dependence of capacitance on both frequency and current.

In order to further verify these assumptions a second test was run on the same cell only with it operated as a forward biased diode (non-illuminated). The test setup was identical to Figure 1 with the addition of a DC voltage source. The method of data reduction was also identical to the illuminated cell test. The DC V-I curve is shown in Figure 6 and curves of Z , R_p , and C_p vs frequency are shown in Figures 7, 8, and 9 respectively. Examination of these curves reveals the same dependence of C_p on operating point and frequency as for the illuminated cell thus reinforcing the diffusion capacitance concept. The curves for Z and R_p also exhibit the same behavior as for the illuminated cell.

Figure 6

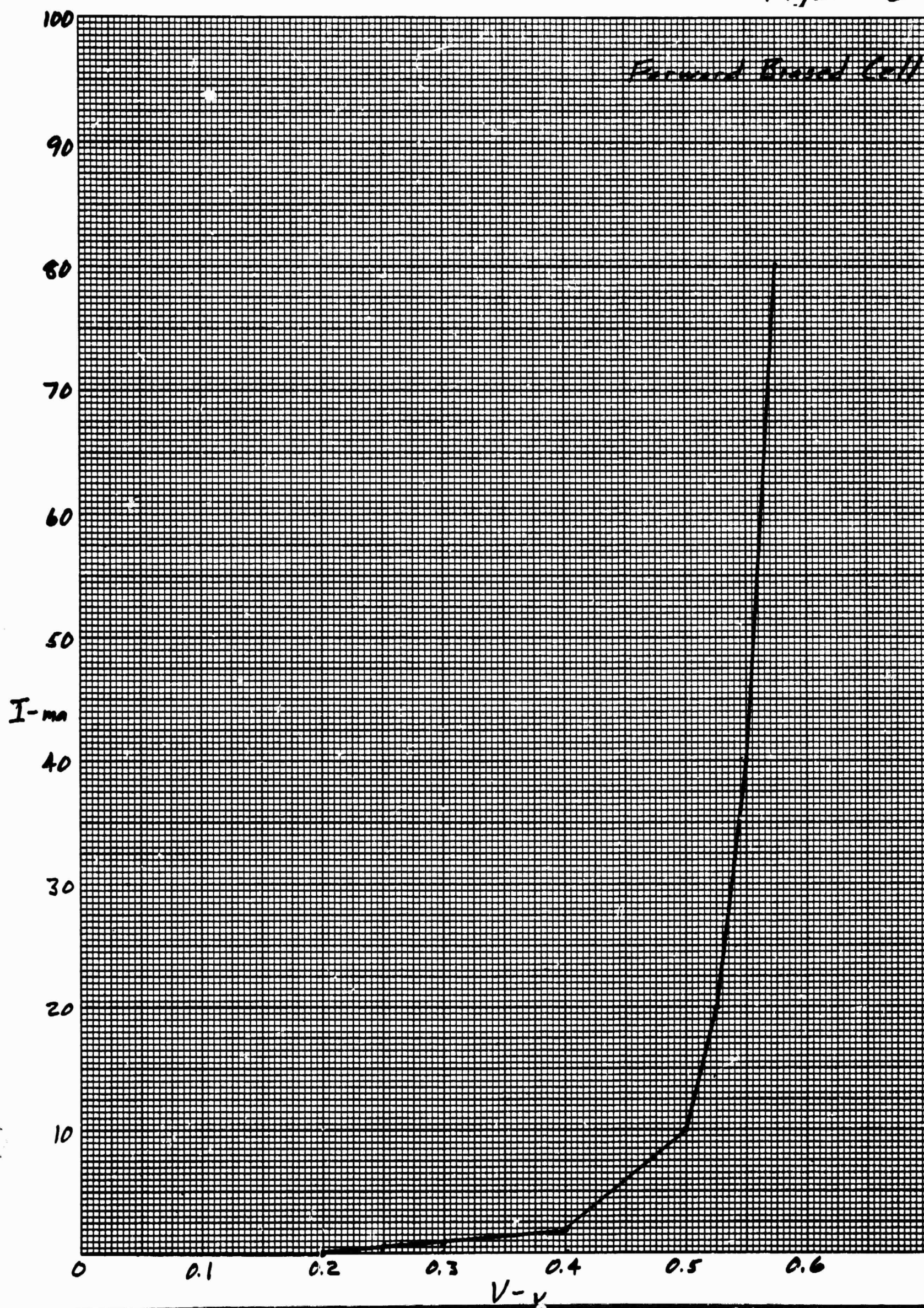


Figure 7

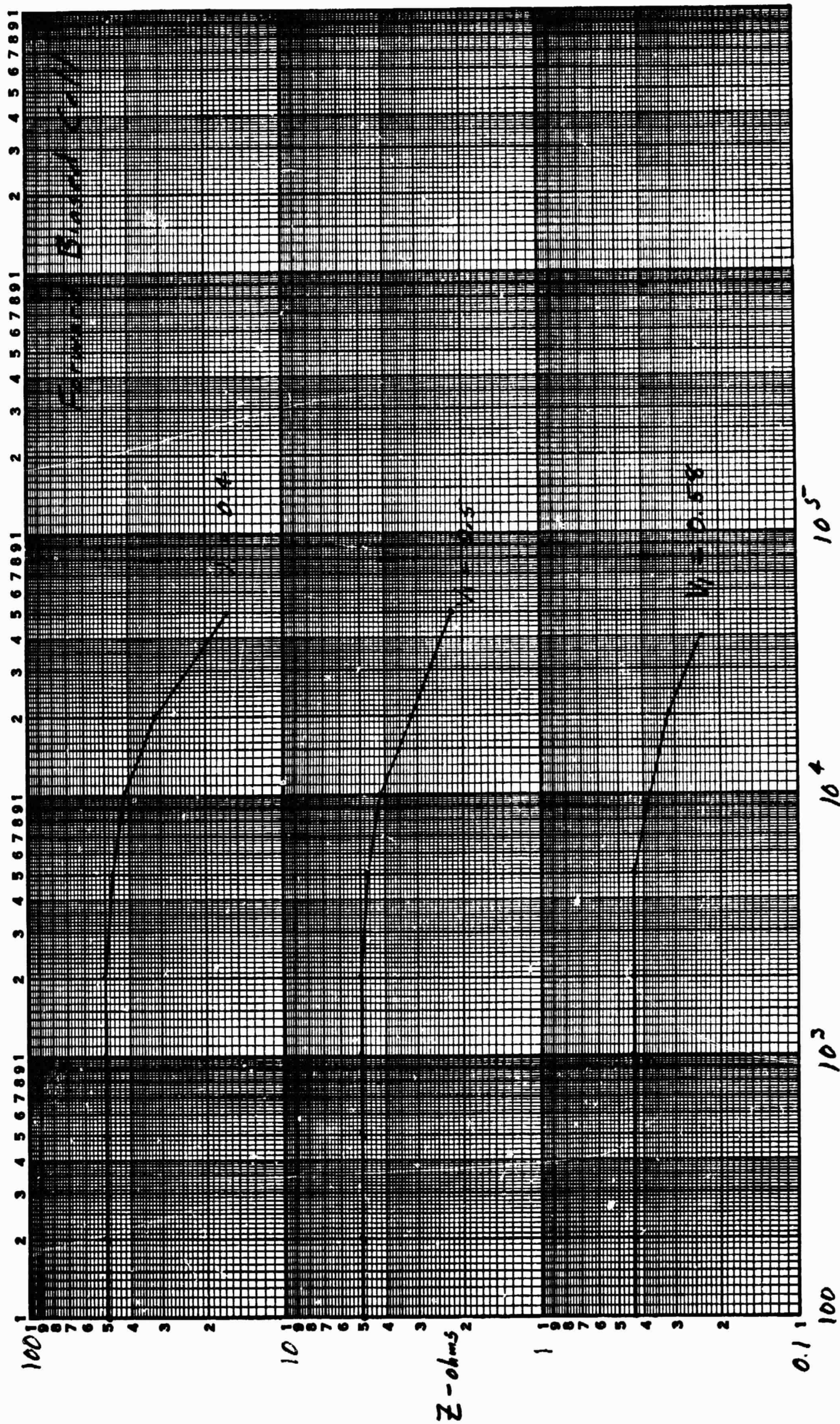


Figure 8

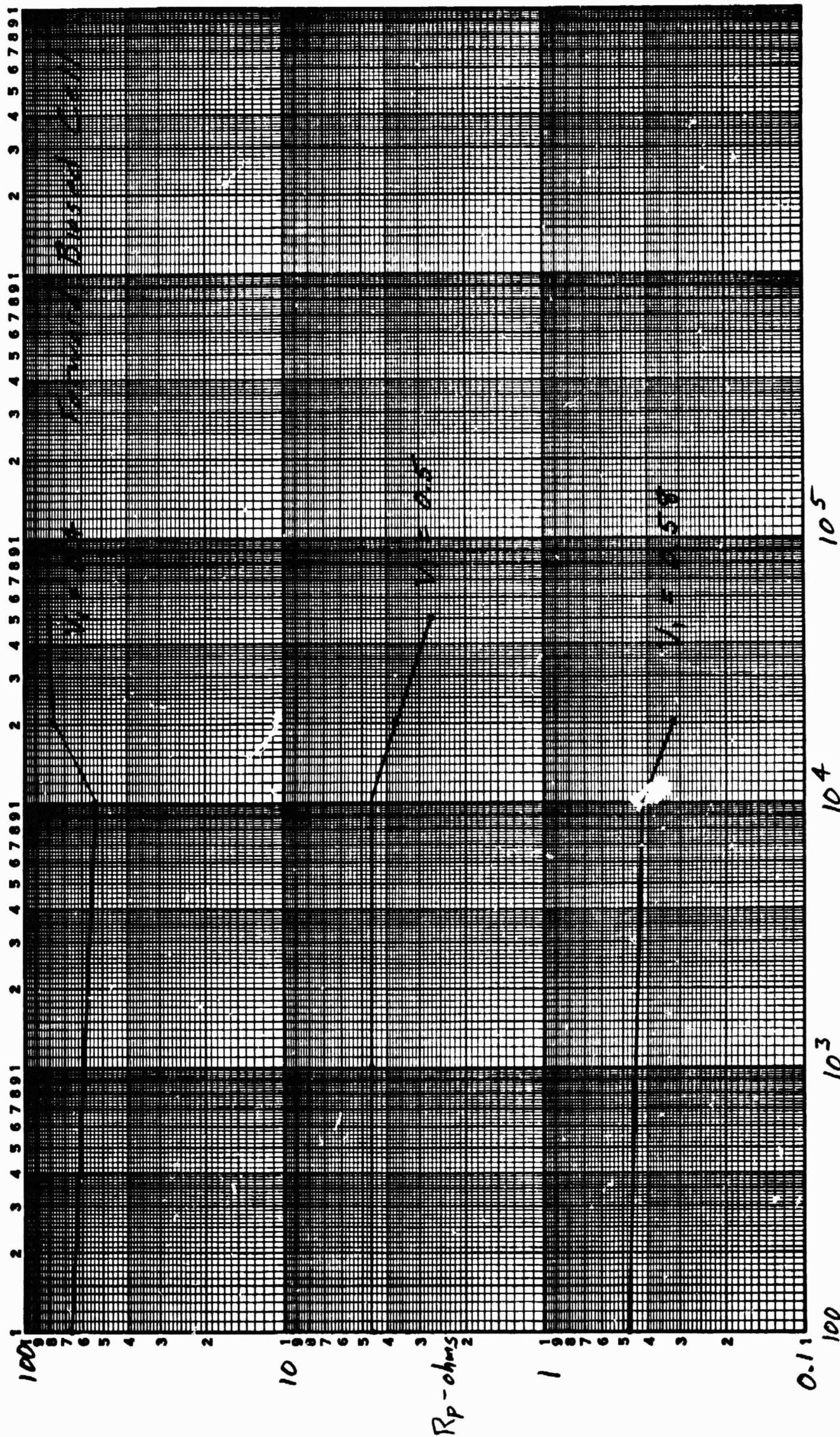
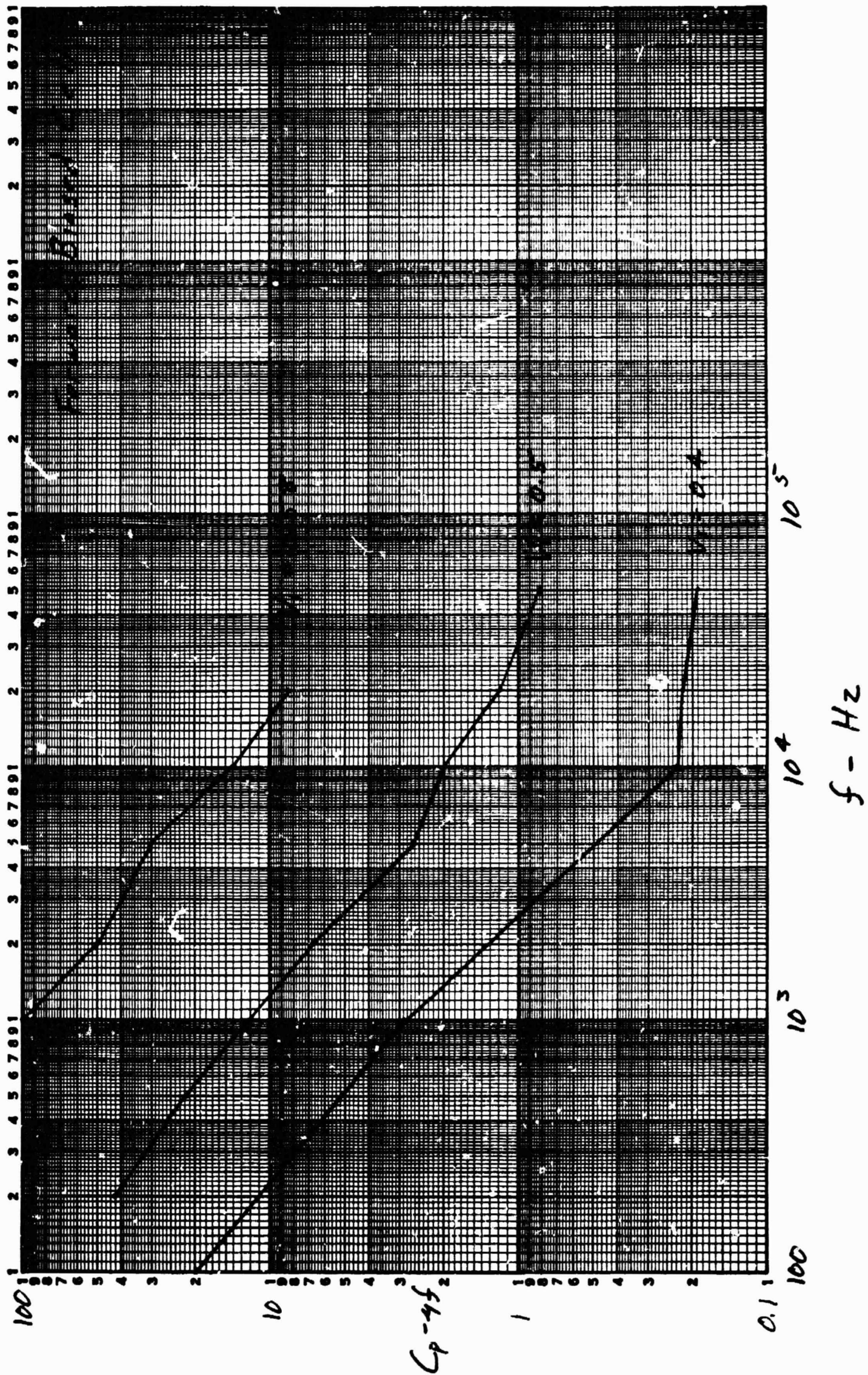


Figure 9



Based on this testing it is concluded that the solar cell impedance is a function of both diffusion current and frequency. While no quantitative conclusions can be reached, it can be seen that a solar cell operated as a forward biased diode exhibits these same characteristics and that properly used it could serve as a reference not only for the DC curve shape but for the AC characteristics as well.

The importance of the array characteristics to typical regulators was discussed in detail in the proposal ² where it was shown that the array impedance enters directly into the feedback loop of the typical shunt type dissipative regulator. Switching type regulators such as would be used in a maximum power point tracking system were also discussed. The final report on the maximum power tracking system being developed for Nimbus ³ emphasizes the importance of the array impedance characteristics as related to the selection of the scan frequency for the tracker. Therefore any realistic test of such a device will require a solar array simulator that closely simulates these characteristics.

In summary the frequency characteristics of the solar cell have been shown to be both a function of operating point and frequency. Therefore it is evident that in order to adequately simulate such a characteristic a reference device must be found that will exhibit these same characteristics. Clearly a fixed RC network on the simulator output will not accomplish this. It has been shown that a solar cell will exhibit these same characteristics if it is operated in the forward biased mode. The importance of the solar array frequency characteristics in typical regulator designs has also been shown.

2.2 Digital versus Analog Tradeoffs

Tradeoff studies were performed to determine the optimum method of generating the basic V-I characteristic and of programming this characteristic as function of time. Three basic schemes were considered; digital generation and programming, analog generation and programming, and analog generation with digital programming.

Two methods of digitally generating and programming the V-I characteristic were considered. Both utilize a digital computer to generate a reference voltage signal in response to samples of the output current. This reference voltage in turn controls a series regulator which adjusts the load voltage according to the desired V-I characteristic. The basic scheme is shown in Figure 10.

In the first case the computer is utilized to perform an on-line calculation of the required load voltage in response to an input load current by the following relationship:

$$V_L = \frac{n_s K T}{q} \ln \left[\frac{K_1 n_p I_s - I_L}{K_1 n_p I_o} + 1 \right]$$

where

V_L = load (output) voltage

I_L = load (output) current

K = Boltzman's constant

q = electron charge

T = absolute temperature in °K. (programmed)

n_s = the number of cells in series

n_p = the number of cells in parallel

I_s = the short circuit current of a single cell at the reference illumination and temperature

I_o = the reverse saturation current of a single cell at the reference illumination and temperature

K_1 = a variable constant to account for variations in illumination due to sun angle and spinning (programmed)

For a given simulation the fixed variables are entered directly into the computer and sub-routines are programmed to generate K_1 and T as a function of time. For a fixed load the output voltage would vary as the variables K_1 and T vary. Even though temperature may vary rather rapidly upon exit from eclipse and K_1 could be

Digital System

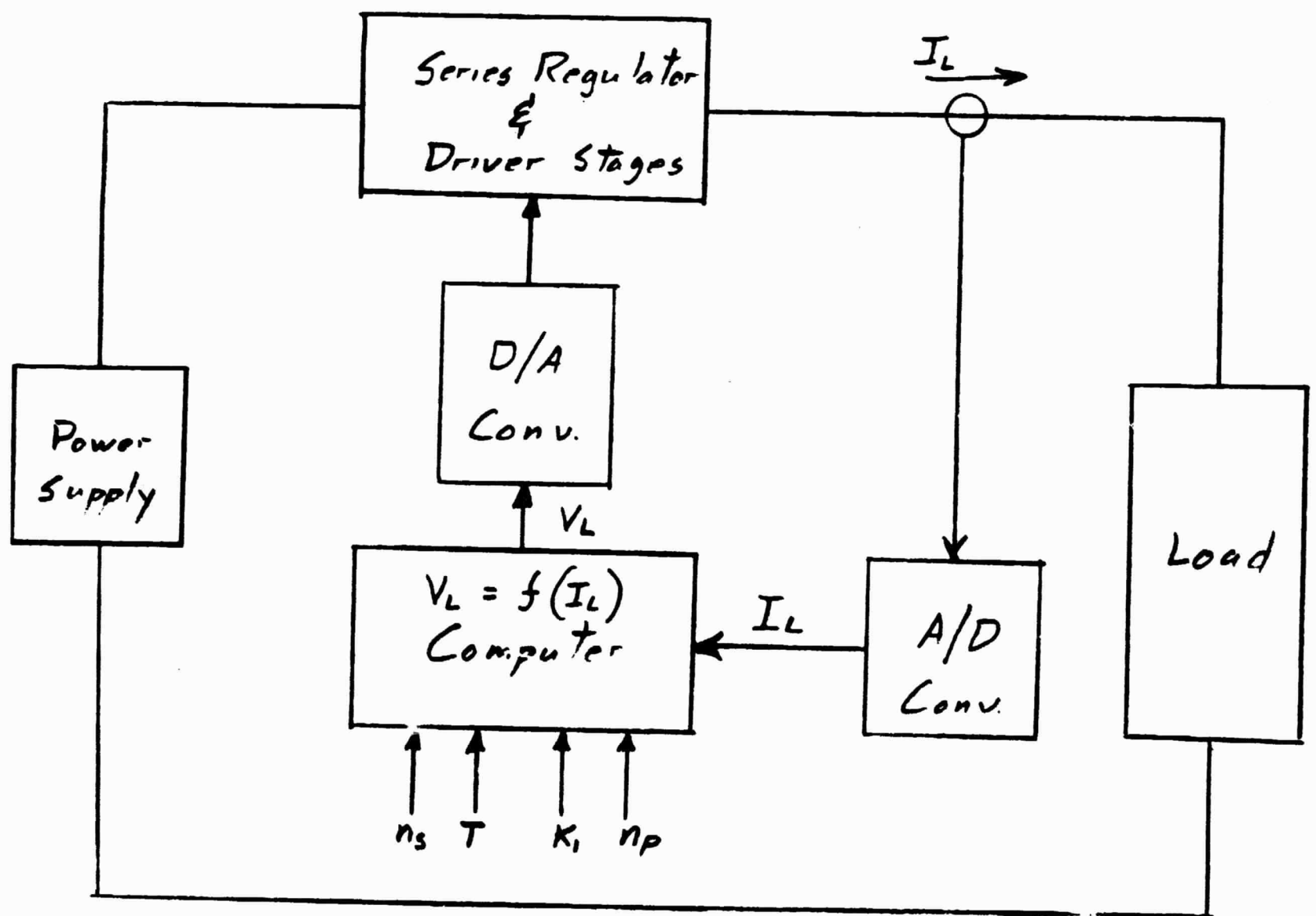


Figure 10

varying at a maximum of a 2 Hz rate in a spinning satellite, these variations are slow compared to the computer calculation time. However in order to be compatible with the frequency response characteristics previously identified, the simulator must be capable of responding at least at a 5 kHz rate: that is for a step change in load the simulator should be at its new operating point in t_R seconds where

$$t_R \approx \frac{0.35}{f_H}$$

Therefore if

$$f_H = 5 \text{ kHz}$$

$$t_R = 70 \text{ usec.}$$

Conversations with various computer manufacturers indicated that computation of the required function in about this length of time would be possible. Note, however, that several iterations would be required before the system could settle down at a new operating point. Clearly this would be in excess of the desired response time.

In order to shorten this time a second scheme was conceived that would considerably shorten the time. Under this method a series of tables of V_L vs I_L would be stored in the computer memory corresponding to the V-I characteristics as a function of time. At any discrete time a single table would be stored in the computer's core memory corresponding to the V-I characteristic for that interval of time. As I_L changed, the corresponding V_L could be outputted in one cycle time, so that now the time limitation falls onto the A/D converter which depending on word length would be of the order of 30 microseconds.

Both of these schemes then seem to be marginal from a response point of view however their most serious disadvantage lies in their inability to simulate the variable impedance of the solar array. Note that while a shift in operating point

will result in an effective change in the DC impedance, if the bandwidth is to remain constant at 5 kHz the capacitance must change by the same percent in the opposite direction. This would be difficult to do digitally in any other than a crude manner. The digital schemes do however offer ease of programming; particularly the first one. Even in the second case the computer could be easily programmed to generate all the required tables in advance from the basic function.

The block diagram for the analog curve generation method is shown in Figure 11. This method utilizes the characteristics of a forward biased solar cell to generate the basic DC curve shape as well as to provide the AC response as discussed in section 2.1. Considering the block diagram we may write:

$$I_R - \frac{I_L}{K_1 n_p} = I_D$$

$$V_D - \frac{V_L}{n_s} = \mathcal{E}$$

Now if A_V is sufficiently large we may write:

$$V_D = \frac{V_L}{n_s}$$

Then

$$\begin{aligned} I_L &= K_1 n_p [I_R - I_D] \\ &= K_1 n_p \left[I_R - I_0 (e^{qV_L/n_s KT} - 1) \right] \end{aligned}$$

where

$$I_R \equiv I_s = \text{short circuit current of the reference cell at the reference illumination and temperature}$$

and all other variables have the same meaning as before. Solving for V_L :

$$V_L = \frac{n_s KT}{q} \ln \left[\frac{K_1 n_p I_R - I_L}{K_1 n_p I_0} + 1 \right]$$

Analog System

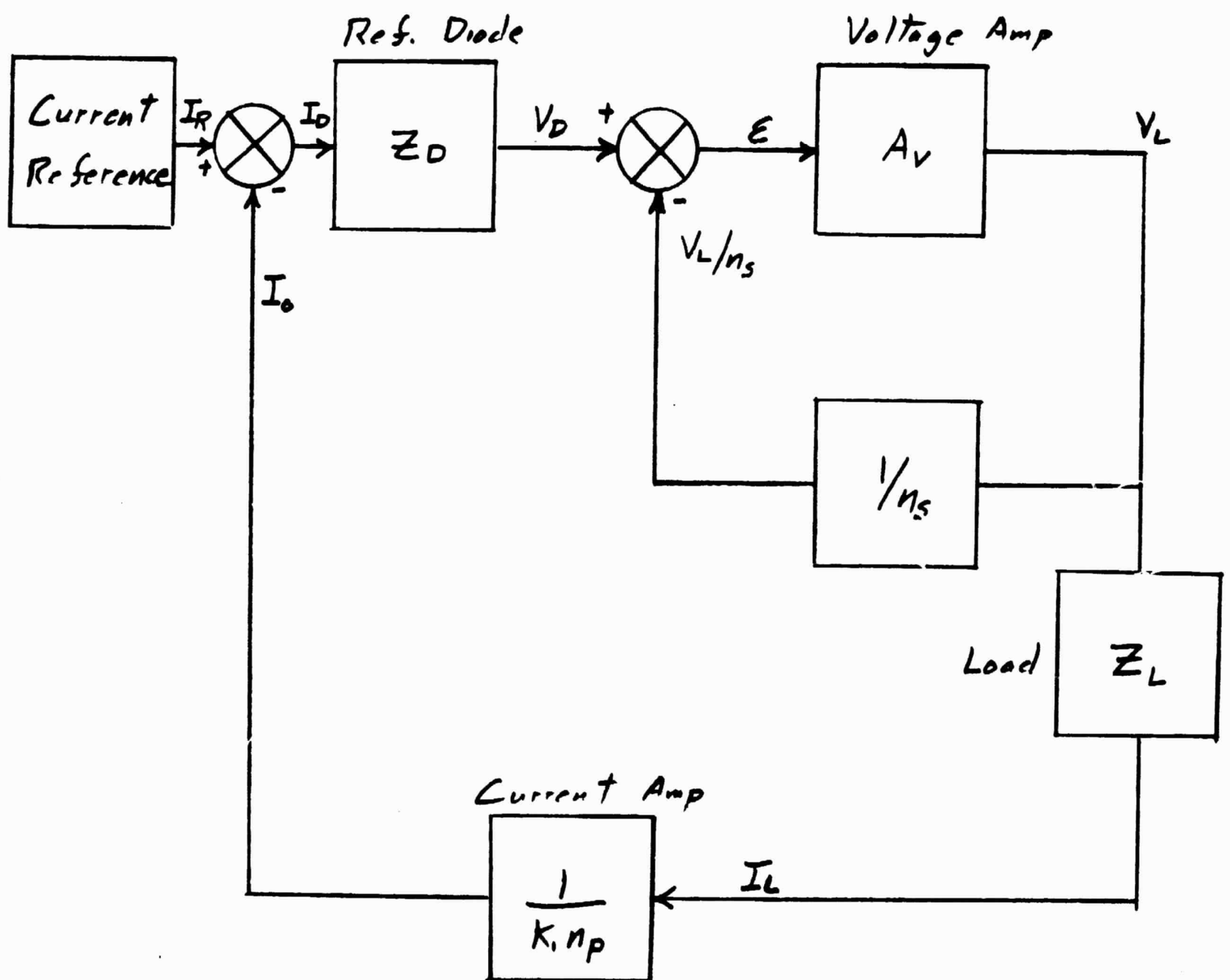


Figure 11

which is identical to the basic function generated in the digital method. In order to simplify the programming we may combine the adjustment of n_s and T into one parameter and K_1 and n_p into a second parameter; i.e. let

$$H = \frac{1}{K_1 n_p}$$

$$nV_t = n_s \frac{K}{q} (T_R + \Delta T)$$

$$V_t = \frac{K T_R}{q}$$

$$n = n_s \frac{K \Delta T}{q}$$

where

T_R = the reference temperature

ΔT = the temperature variation

Therefore $\frac{1}{H}$ may be interpreted as the number of parallel cells in the array as modified by the illumination variation. Notice that at the reference illumination ($K_1 = 1$) and at short circuit current

$$H \equiv \frac{I_R}{I_{sc}}$$

Also n may be interpreted as the number of series cells in the array as modified by the temperature variation. In this case at the reference temperature ($\Delta T = 0$) and at open circuit voltage

$$n \equiv \frac{V_{oc}}{V_R}$$

where

V_R = the reference diode voltage when $I_D = I_R$.

Therefore at reference conditions we may write

$$V_L = nV_t \ln \left[\frac{I_{sc} - I_L}{I_{sc} I_{D0}} + 1 \right]$$

$$I_L = I_{sc} \left\{ 1 - I_{D0} \left[e^{V_L/nV_t} - 1 \right] \right\}$$

where

$$I_{D0} = I_0/I_R$$

Variation of n_s and n_p from array to array is handled as an initial programmer setting of n and H whereas variation from reference conditions for a given array as a function of time is handled by incremental variations of n and H about their initial values. In order to accomplish this with a true analog or linear element would require some relatively complex electromechanical or electro-optical scheme and therefore analog programming has definite disadvantages.

Therefore it appears that an analog generation/digital programming scheme offers the greatest advantages; i.e.

1. True analog generation of the V-I characteristic.
2. True analog simulation of the array impedance through multiplication of the AC response of the forward biased diode analog.
3. Ease of programming inherent to digital systems.

2.3 Optimization of Power Modules

It is desired to determine the optimum size of the basic power module that would be consistent with simulation of arrays ranging in power from 20 to 5000 watts. The basic concept of combining power modules is shown in Figure 12. Each module would operate as a functional entity and would consist of a programmable reference, a power supply, a power stage, and an isolation diode. Therefore these modules could be placed in series or in parallel in the same manner as individual panels are arranged to make up a total array.

Three basic requirements must be considered when determining the size of the individual module.

1. Maximum power capability
2. Range of I_{sc} and V_{oc} allowable at maximum power
3. Range of adjustment downward from maximum power

The relationship between the first two requirements can be seen by reference to Figure 13. That is, for a given maximum power it is obvious that all possible combinations of voltage and current cannot be permitted for a realizable power supply/power stage combination. Suppose that the power supply has a maximum voltage of V_s and a maximum current of I_s and for simplification assume that the regulator is lossless and that the V-I characteristic is a rectangle. Then the maximum power output would be:

$$P_{MP} = V_s I_s$$

If this were chosen as the maximum power rating of the module, then clearly only one set of values of I_{sc} and V_{oc} would permit this maximum to be attained. However if for example the maximum power rating of the module were chosen to be

$$P_{MP} = 1/2 V_s I_s$$

then various sets of V_{oc} and I_{sc} would be permitted ranging from

Power Module Concept

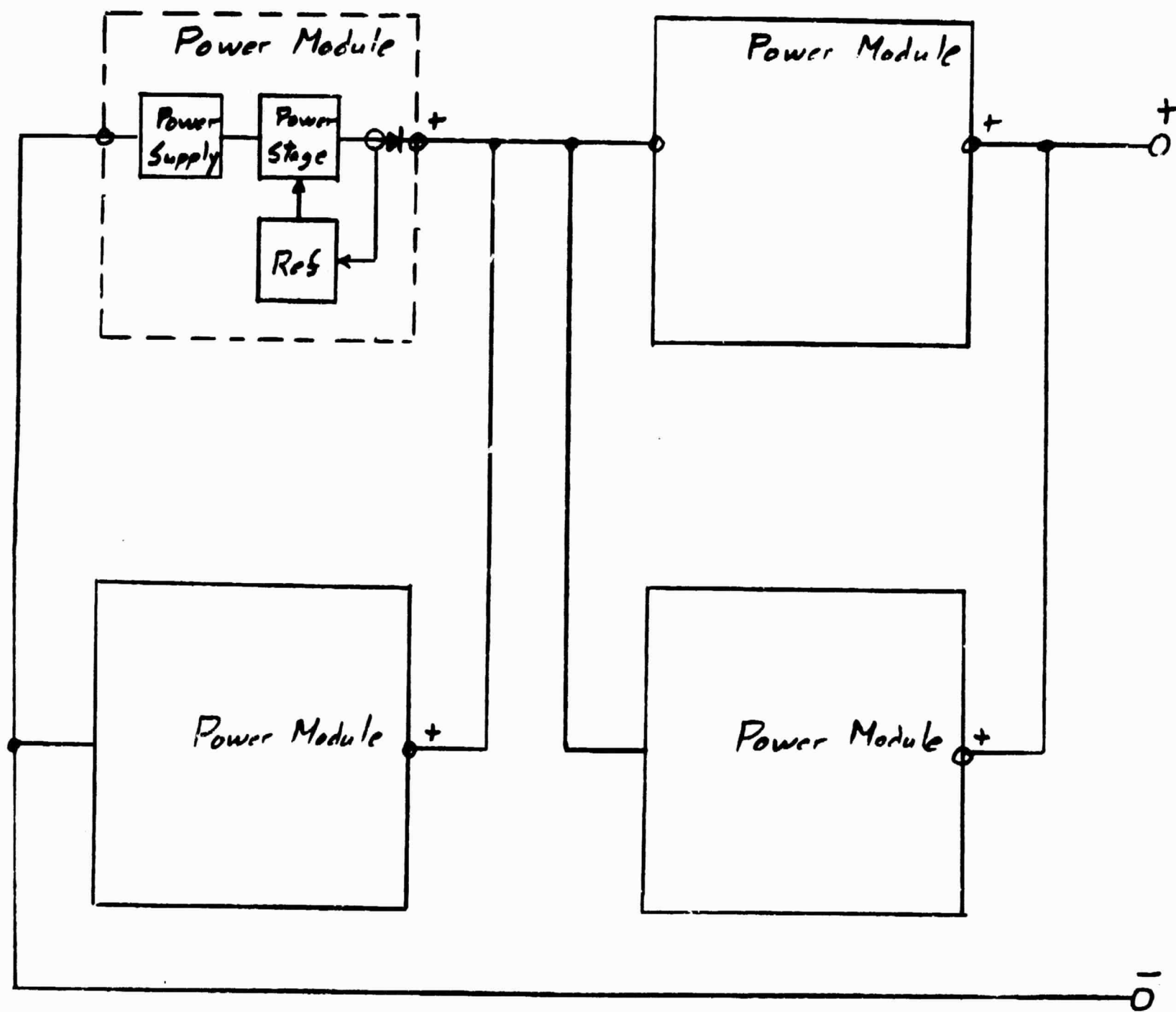
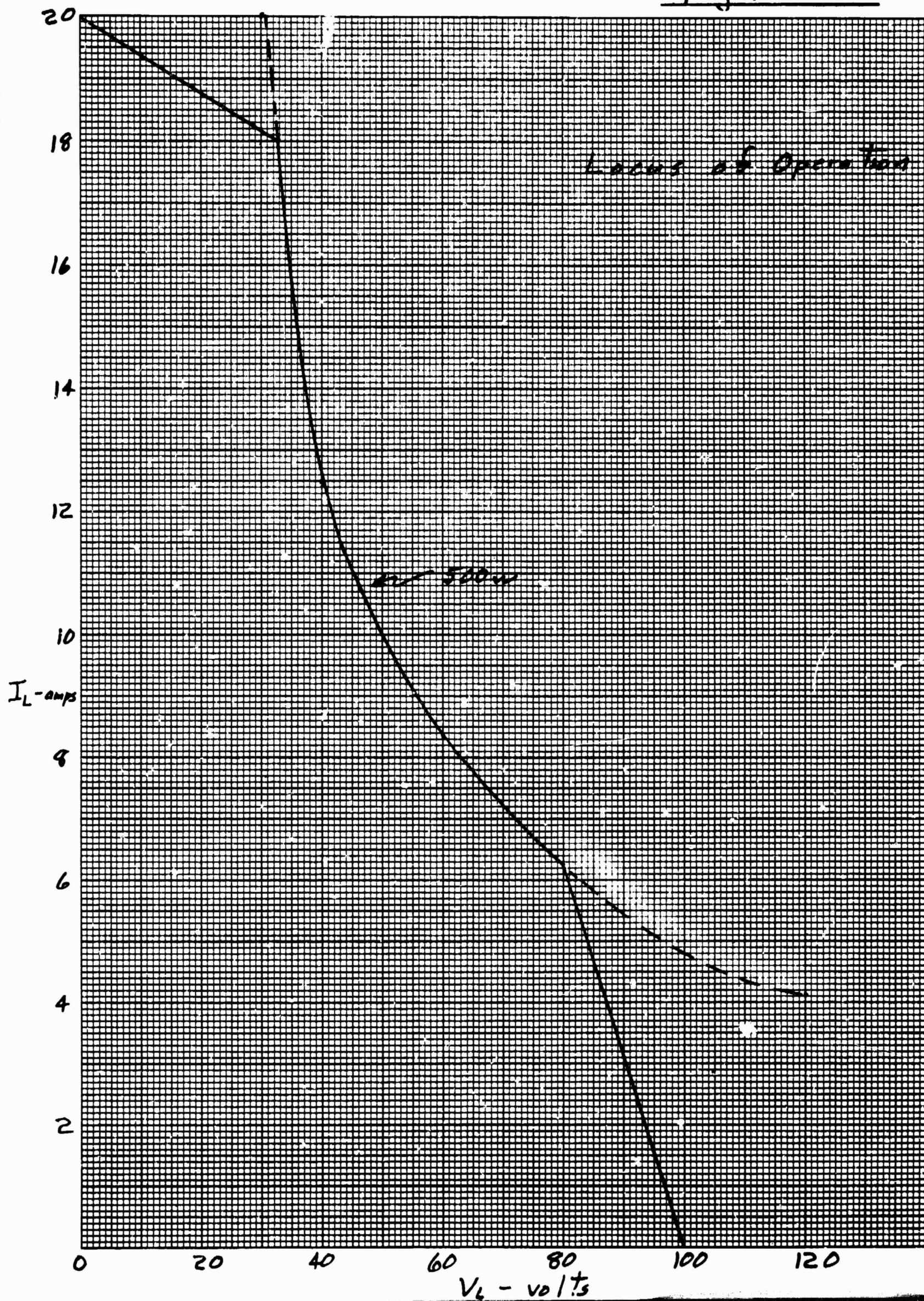


Figure 12

Figure 13



$$V_{oc} = V_s$$

$$I_{sc} = 1/2 I_s$$

to

$$V_{oc} = 1/2 V_s$$

$$I_{sc} = I_s$$

With this type of maximum power rating then, a wide range of I_{sc} and V_{oc} can be accommodated for a given power supply.

In addition to the power supply limitations, the limitations of the series transistor(s) in the power stage itself must be considered. For example the most severe operating condition for the transistor occurs when the simulator is operating at short circuit, i.e.

$$V_{ce} = V_{oc}$$

$$I_c = I_{sc}$$

$$\therefore P_T = V_{oc} I_{sc}$$

In this case the power being dissipated in the power stages is $1.4 P_{MP}$ and output power is zero (since $V_L = 0$). Therefore if as in the previous example the rating of module is

$$P_{MP} = 1/2 V_s I_s$$

then the minimum rating of the power transistor(s) must be

$$V_{CE \max} = V_s \text{ at } I_c = 1/2 I_s$$

$$I_{C \max} = I_s \text{ at } V_{ce} = 1/2 V_s$$

$$P_{T \max} = 1/2 V_s I_s$$

In addition all combinations of voltage and current between the two extremes must not exceed the second breakdown limitations of the transistor. Of course suitable derating must be included in determining the maximum ratings required of the power transistor.

Once the maximum power rating and the range of V_{OC} and I_{SC} are determined for the module then the minimum power capability must also be examined. Obviously any power within the envelope of Figure 13 can be achieved as far as the power supply and power stage are concerned however the problem here is related to the range of adjustment of the current amplifier, i.e. since

$$H = \frac{I_R}{I_{SC}}$$

it is obvious that I_{SC} cannot be adjusted to zero. Similarly V_{OC} cannot be adjusted to less than V_R . Therefore as a practical matter both V_{OC} and I_{SC} have to have some lower limit of adjustment.

These three factors make up the main technical considerations on module size however two additional factors which also should be considered are cost and flexibility. From a cost point of view the larger the module the less the cost will be primarily due to the necessity of having individual supplies for each module and also due to the programmer if individual programmers are used for each module. From a flexibility standpoint the smaller the module the greater the flexibility.

Considering these five factors the following module size was selected as optimum

$$P_{MP} = V_{MP} I_{MP} = 500w$$

$$V_{MPmax} = 80v @ I_{MP} = 6.25a$$

$$I_{MPmax} = 18a @ V_{MP} = 27.7v$$

therefore

$$V_{OCmax} = 100v @ I_{SC} = 7a$$

$$I_{SCmax} = 20a @ V_{OC} = 34v$$

assuming

$$V_{MP} \approx 0.8 V_{OC}$$

$$I_{MP} \approx 0.9 I_{SC}$$

Also for the minimum operating adjustments

$$V_{oc \min} = 10v$$

$$I_{sc \min} = 0.1a$$

Therefore the maximum power requirement of 5000w can be attained with a variety of V_{oc}/I_{sc} settings and series/parallel combinations. For example at the extremes it could be attained with 10 modules in series and

$$V_{oc} = 1000$$

$$I_{sc} = 7$$

or with 10 modules in parallel and $V_{oc} = 34$, $I_{sc} = 200$.

The minimum power at the maximum power point would be

$$P_{MP \min} = 7.2w$$

corresponding to

$$I_{sc} = 0.1a$$

$$V_{oc} = 10v$$

2.4 Output Accuracy Considerations

For the purposes of this study accuracy is defined as the following:

Accuracy is the ability of the solar array simulator to reproduce the reference V-I characteristic for a fixed set of inputs H and n as previously defined. This shall include both repeatability and long term stability.

In order to perform a qualitative accuracy analysis a reference system must be selected. Therefore the hybrid analog/digital system has been selected as shown in Figure 14. The following operating parameters are also specified:

$$I_{sc \min} = 0.1a$$

$$I_{sc \max} = 20a \text{ at } V_{oc} = 34v$$

$$V_{oc \min} = 10v$$

$$V_{oc \max} = 100v \text{ at } I_{sc} = 7a$$

$$P_{MP \max} = 500w$$

Reference System

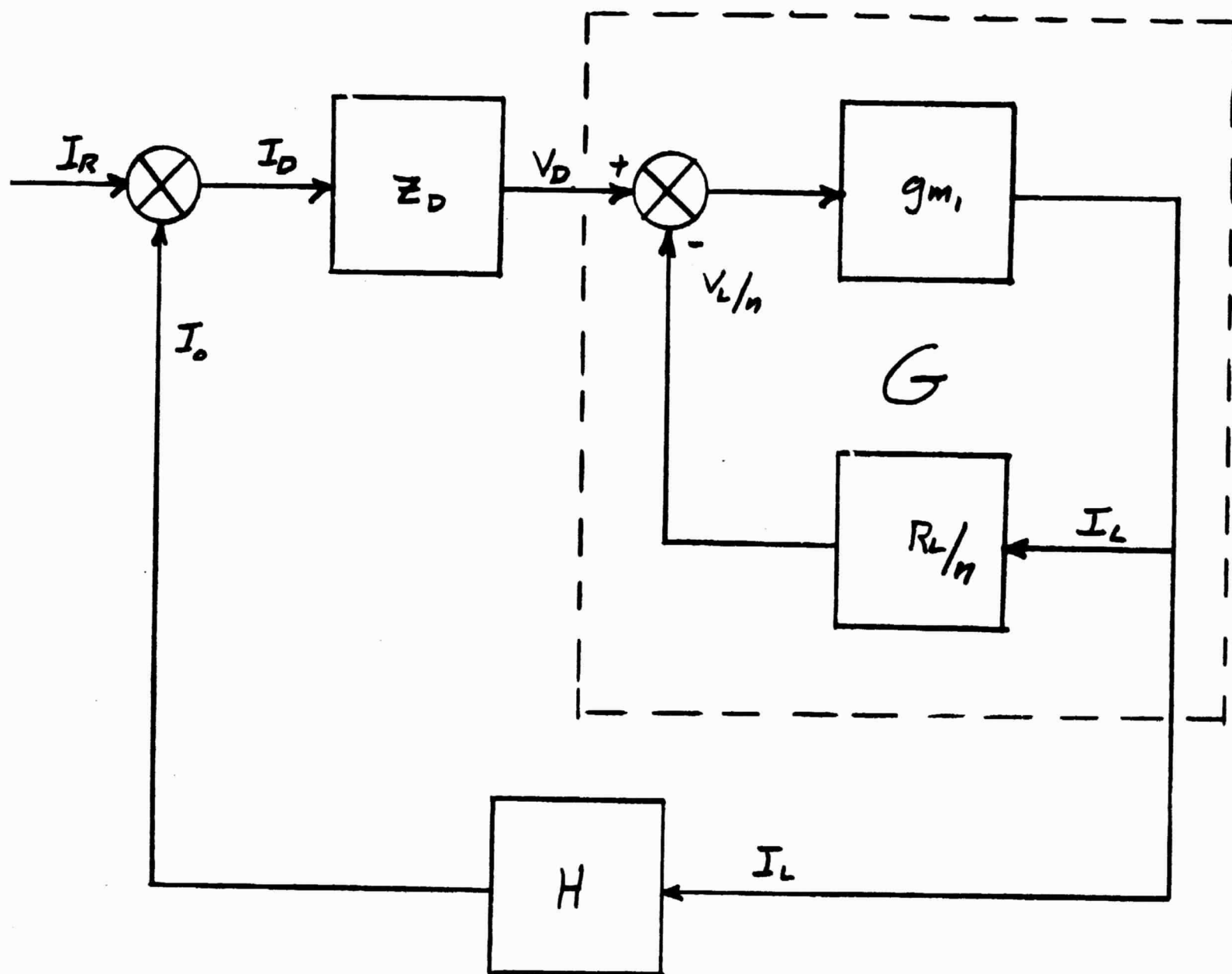


Figure 14

The closed loop transfer function for this system may be written as

$$G_{CL} = \frac{Z_D G}{1 + Z_D G H}$$

In terms of I_L the closed loop gain may be written as

$$G_{CL} = I_L / I_R$$

Therefore since I_R is fixed

$$\Delta I_L = \Delta G_{CL} I_R$$

In terms of a ratio the current accuracy may be defined as

$$M_I = \frac{\Delta I_L}{I_{sc}}$$

Therefore

$$M_I = \frac{I_R}{I_{sc}} \Delta G_{CL}$$

The voltage accuracy may be defined as

$$M_V = \frac{\Delta V_L}{V_{oc}}$$

Now since the voltage and the current are related by the characteristic function

ΔV_L may be expressed in terms of ΔI_L as

$$\Delta V_L = \frac{V_{oc} V_t}{V_R} \ln \left[\frac{\Delta I_L}{I_{sc} I_{D0}} e^{-V_L / n V_t} + 1 \right]$$

Therefore both the current and voltage accuracy can be determined if the variation of the closed loop gain due to all the variables that can affect it can be determined.

The first step in this analysis is to determine the variation of the closed loop gain as a function of the variation of the three major blocks of Figure 14; Z_D , G , and H . Therefore by partial differentiation

$$\frac{\Delta G_{CL}}{\Delta G} = \frac{-Z_D}{D}$$

$$\frac{\Delta G_{CL}}{\Delta Z_D} = \frac{-G}{D}$$

$$\frac{\Delta G_{CL}}{\Delta H} = \frac{Z_D^2 G^2}{D}$$

Where

$$D = (1 + Z_D G H)^2$$

The individual variations of G_{CL} due to G , Z_D , and H can be expressed as a , b , and c respectively, i.e.

$$a = \frac{-Z_D \Delta G}{D}$$

$$b = \frac{-G \Delta Z_D}{D}$$

$$c = \frac{Z_D^2 G^2 \Delta H}{D}$$

Then by combining these variations using the "root sum of the squares" technique (RSS)

$$M_I = \frac{I_R}{I_{sc}} \sqrt{a^2 + b^2 + c^2}$$

and

$$M_V = \frac{V_t}{V_R} \ln \left[\frac{M_I}{I_{DO}} e^{-V_L/nV_t} + 1 \right]$$

At this point it is necessary to work backwards to determine what G , Z_D , and H can be allowed if the design goal of 1% ($\pm 0.5\%$) is to be met for both M_I and M_V . First examining these accuracies at the extremes of the V-I characteristic, suppose that

$$M_I = .01$$

Then at short circuit current determine M_V by the previous relationship, i.e.

$$M_V = \frac{V_t}{V_R} \ln \left[\frac{M_I}{I_{DO}} e^{-V_L/nV_t} + 1 \right]$$

For purposes of this analysis the following constants were established for the reference diode.

$$I_R = 140 \text{ ma}$$

$$V_R = 600 \text{ mv}$$

$$V_t = \frac{KT}{q} = 26 \text{ mv}$$

$$I_{DO} = 10^{-10} \text{ a}$$

Therefore

$$M_V = \frac{1}{23} \ln \left[M_I e^{-23 V_L/V_{oc}} \times 10^{10} + 1 \right]$$

$$\text{At } V_L = 0, M_I = .01$$

$$M_V = \frac{1}{23} \ln \left[10^8 \right]$$

$$M_V = 0.8$$

Clearly these numbers are not compatible. Either M_I must be reduced by a factor of approximately 10^8 or the range of V_L must be limited to no less than approximately $0.8 V_{oc}$. Neither of these alternatives is acceptable. Examination of the magnitude of Z_D near short circuit (V_D near 0) reveals the cause of the problem. Referring to Figure 14 notice that for a 1% error in I_0 there will be a corresponding 1% error in I_D , i.e.

$$\Delta I_D = .01 I_R$$

Therefore

$$\Delta V_D = .01 I_R Z_D$$

A tabulation of Z_D versus V_D for the reference diode is given in Table I where Z_D is the DC resistance and is determined by the following relationship

$$Z_D = \frac{V_D}{I_D} = \frac{V_D}{I_0 \left[e^{V_D/V_t} - 1 \right]}$$

where

$$I_0 = 1.4 \times 10^{-11} \text{ a}$$

TABLE I

Diode Impedance vs Voltage

<u>V_D - volts</u>	<u>I_D - amps</u>	<u>Z_D - ohms</u>
.03	3 x 10 ⁻¹¹	1 x 10 ⁹
.05	8 x 10 ⁻¹¹	6.25 x 10 ⁸
.1	6.3 x 10 ⁻¹⁰	1.59 x 10 ⁸
.2	3.08 x 10 ⁻⁸	6.5 x 10 ⁶
.3	1.36 x 10 ⁻⁶	2.2 x 10 ⁵
.4	6.63 x 10 ⁻⁵	6.03 x 10 ³
.5	3.02 x 10 ⁻³	165
.55	22 x 10 ⁻³	25
.57	43.5 x 10 ⁻³	13.1
.59	99 x 10 ⁻³	5.95
.6	140 x 10 ⁻³	4.28

It can be seen that at or near V_D = 0 even a very small ΔI_L will result in a large ΔV_L because of the large value of Z_D in this region. Note that this is a simplification since the closed loop will modify the operating point away from V_D = 0 until an equilibrium operating point is attained. However it appears advantageous to modify Z_D by placing a fixed resistor R_p in parallel with it. This results in a new characteristic function for V_L and I_L.

$$I_L = I_{sc} \left[1 - I_{DO} \left(e^{V_L/nV_t} - 1 \right) - \frac{V_L}{nR_p I_R} \right]$$

and the relationship between ΔI_L and ΔV_L becomes

$$\Delta I_L = \frac{I_{sc}}{nI_R R_p} \Delta V_L + I_{sc} I_{DO} e^{V_L/nV_t} \left(e^{\Delta V_L/nV_t} - 1 \right)$$

This cannot be solved explicitly for ΔV_L as was done previously. However as an example determine ΔV_L for the same conditions as before, i.e.

$$M_I = .01$$

$$V_L = 0$$

and with

$$R_p = 100$$

$$n = 50 \text{ (i.e. } V_{oc} = 30)$$

then

$$.01 = .00143 \Delta V_L + 10^{-10} (e^{.77 \Delta V_L} - 1)$$

By trial and error

$$\begin{aligned} \Delta V_L &= 7v \\ M_v &= \frac{\Delta V_L}{V_{oc}} = .234 \end{aligned}$$

While this represents a considerable improvement it is clear that any further improvement will have to be accomplished by improving M_I since further reduction of R_p has too drastic an effect on the slope of the V-I characteristic in the constant current region. By inspection the preceding equation can be simplified to

$$\Delta I_L = \frac{I_{sc}}{n I_R R_p} \Delta V_L$$

Therefore

$$\frac{\Delta V_L}{n} = \frac{\Delta I_L}{I_{sc}} I_R R_p$$

$$M_v V_R = M_I I_R R_p$$

$$M_v = M_I \frac{I_R R_p}{V_R}$$

$$M_v = 23.3 M_I$$

For example if

$$M_I = .005$$

Then

$$M_V = .116 @ V_L = 0$$

At the other extreme of the V-I characteristic no incompatibility between M_I and M_V exists. Using the original relationship (since the effect of R_p is nullified near open circuit) the corresponding M_V for a given M_I can be calculated by

$$M_V = \frac{1}{23} \ln \left[M_I e^{-23 \frac{V_L}{V_{oc}} \times 10^{10}} + 1 \right]$$

Therefore if

$$M_I = .005$$

$$V_L = V_{oc}$$

$$M_V = \frac{1}{23} \ln \left[.005 \times 1.03 + 1 \right]$$

$$M_V = .00022$$

Therefore with the modified diode reference (i.e. $R_p = 100$ in parallel), the parameters G , Z_D , and H and their partials (a, b, and c) can be calculated at the extremes of the V-I characteristic and over the full range of adjustment of I_{sc} . (These parameters are independent of V_{oc}). The expression for G is

$$G = \frac{gm_1}{1 + \frac{gm_1 R_L}{n}}$$

$$\cong \frac{n}{R_L}$$

where it is assumed for now that gm_1 is infinite and Z_L is a resistance. The expression for H is

$$H = \frac{I_R}{I_{sc}}$$

The values of Z_D can be computed from Table I by combining R_p in parallel with the values of Table I. Finally in order to come up with finite values for G the parameters will be computed at

$$V_L = .01 V_{oc}$$

$$I_L \cong I_{sc}$$

and at

$$I_L = .01 I_{sc}$$

$$V_L \approx V_{oc}$$

The following accuracies were assigned for the three blocks

$$\Delta G = .005 G$$

$$\Delta H = .005 H$$

$$\Delta Z_D = .05 Z_D$$

The resulting current and voltage accuracies are tabulated in Table II.

TABLE II - Current and Voltage Accuracy

$V_L - v$	$I_L - a$	$I_{sc} - a$	$G - a/v$	$Z_D -$ ohms	$H - a/a$	a	b	c	$M_I - \%$	$M_V - \%$
.01 Voc	Isc	20	3.33×10^3	100	7×10^{-3}	3.1×10^{-4}	3.1×10^{-3}	.717	0.5	11.6
.01 Voc	Isc	0.1	16.6	100	1.4	1.55×10^{-6}	1.55×10^{-5}	3.58×10^{-3}	0.5	11.6
Voc	.01 Isc	20	0.3	4.1	7×10^{-3}	6.06×10^{-3}	6.06×10^{-2}	5.3×10^{-5}	0.042	0.0019
Voc	.01 Isc	0.1	1.5×10^{-3}	4.1	1.4	3.03×10^{-5}	3.03×10^{-4}	2.65×10^{-7}	0.042	0.0019

The next analysis task is to determine if the Δ 's assumed for Table II are reasonable. Considering G , the first error that must be assessed is due to the fact that gm_1 is not infinite and therefore the assumption that

$$G = \frac{n}{R_L}$$

is not valid; that is there will be some ΔG due to gm_1 not being infinite. Suppose we let $gm_1 = 10^5$.

Then

$$\Delta G = \frac{n}{R_L} - G$$

where

$$G = \frac{gm_1}{1 + \frac{gm_1 R_L}{n}}$$

This error is tabulated in Table III for the extreme operating points.

TABLE III
Variation of G

V_L	I_L	I_{sc}	$\frac{n}{R_L}$	G	ΔG
.01 Voc	Isc	20	3.33×10^3	3.22×10^3	110
.01 Voc	Isc	0.1	16.6	16.6	—
Voc	.01 Isc	20	0.3	0.3	—
Voc	.01 Isc	0.1	1.5×10^{-3}	1.5×10^{-3}	—

Therefore in the worst case for $V_L = .01 V_{oc}$ and $I_L = I_{sc} = 20a$,

$$\frac{\Delta G}{G} = \frac{110}{3220} = .034 = 3.4\%$$

versus 0.5% assumed. However re-examination of Table II reveals that ΔH is the controlling accuracy at this extreme of the V-I characteristic and that $\Delta G/G$ could be increased by a factor of 100 and still not affect M_I or M_V .

Next consider the effects of a variation in g_{m1} itself on G . The partial derivative of G with respect to g_{m1} is

$$\frac{\Delta G}{\Delta g_{m1}} = \frac{-1}{(1 + \frac{g_{m1} R_L}{n})^2}$$

Let ΔG be held to

$$\Delta G \leq .001 G$$

The maximum g_{m1} 's that can be allowed for this limit not to be exceeded are tabulated in Table IV

Where

$$\Delta g_{m1} = -.001G (1 + g_{m1} \frac{R_L}{n})^2$$

$$g_{m1} = 10^5$$

TABLE IV - Variation of g_{m1}

V_L	I_L	I_{sc}	$\frac{n}{R_L}$	G	$\max \Delta g_{m1}$
.01 Voc	Isc	20	3.33×10^3	3.22×10^3	3.1×10^3
.01 Voc	Isc	0.1	16.6	16.6	6×10^5
Voc	.01 Isc	20	0.3	0.3	3.3×10^7
Voc	.01 Isc	0.1	1.5×10^{-3}	1.5×10^{-3}	6.7×10^9

Therefore in the worst case at $V_L = .01 V_{oc}$ and $I_L = I_{sc} = 20a$ the maximum Δg_{m1} allowed for a ΔG of .001G is

$$\frac{\Delta g_{m1}}{g_{m1}} \times 100 = 3.1\%$$

Therefore based on the results of Table III and Table IV it appears that the assumption of a

$$\frac{\Delta G}{G} = 0.5\%$$

is certainly reasonable for use in the overall accuracy determination.

Similar reasoning applied to H confirms that the 0.5% variation assumed there is also reasonable.

Finally considering Z_D it is seen that the main source of variation there is due to temperature. Assuming that the reference diode can be held to $\pm 1^\circ\text{F}$ by a suitable heatsink/cooler, the ΔZ_D for $\pm 1^\circ\text{F}$ about a nominal Z_D at 300°K is computed and tabulated below in Table V.

TABLE V - Variation of Z

<u>V_D</u>	<u>$Z_D (T = 300^\circ\text{K})$</u>	<u>$Z_D (T = 300^\circ \pm .55^\circ\text{K})$</u>	<u>$\frac{\Delta Z}{Z_{300}}$</u>
.1	1.6×10^8	1.61×10^8	.62%
.3	2.2×10^5	2.22×10^5	.91%
.6	4.3	4.52	5.1%

Therefore the assumed ΔZ_D of 5% appears reasonable.

2.5 Summary of Tradeoff Studies

As a result of the tradeoff studies the following conclusions have been reached.

1. The impedance of a solar cell has been shown to be both a function of current and of frequency. A tentative model for this impedance based on the concept of diffusion capacitance was discussed. It was shown that the same cell when operated as a forward biased diode displayed similar impedance versus frequency and impedance versus current behavior. In both cases the capacitive term of the impedance was proportional to diffusion current where in the illuminated cell the diffusion current is short circuit current minus the external current whereas in the cell operated as a forward biased diode the diffusion current is identical to the external current.
2. Tradeoff studies on digital versus analog systems revealed that the optimum system was one that utilized an impedance multiplication scheme based on the impedance analog between the illuminated cell and the forward biased cell mentioned above. Programming of changes in the V-I characteristic due to temperature and illumination variations was found to be best accomplished by digital means.
3. The studies on the optimum size of a power module led to the selection of a 500w module with open circuit voltage adjustment between 10 and 100 volts and short circuit current adjustment between 0.1 and 20 amps.
4. Accuracy studies on the reference analog system revealed that a resistance had to be added in parallel with the reference diode in order to provide reasonable voltage accuracy in the region of operation near short circuit current. Current accuracy was within 1% over

the entire operating range whereas voltage accuracy ranges from a maximum of 11.6% at short circuit current to less than .002% at open circuit voltage. The voltage accuracy drops to 1% or less for voltage greater than approximately 80% of V_{oc} .

Based on the reference analog system a reference V-I characteristic for a single cell was computed and is shown in Figure 15. This characteristic was generated from the characteristic equation

$$\begin{aligned} I_L &= I_{sc} - I_{sc} I_{do} \left[e^{V_L/nV_t} - 1 \right] - \frac{I_{sc} V_L}{nI_R R_p} \\ &= \frac{I_R}{H} - \frac{I_o}{H} \left[e^{V_L/nV_t} - 1 \right] - \frac{V_L}{nHR_p} \end{aligned}$$

with

$$H = 1 \quad (\text{i.e. } n_p = 1, K_1 = 1)$$

$$n = 1 \quad (\text{i.e. } n_s = 1, \Delta T = 0)$$

$$I_L = I_R - I_o \left[e^{V_L/V_t} - 1 \right] - \frac{V_L}{R_p}$$

where

$$I_R = 140 \text{ ma}$$

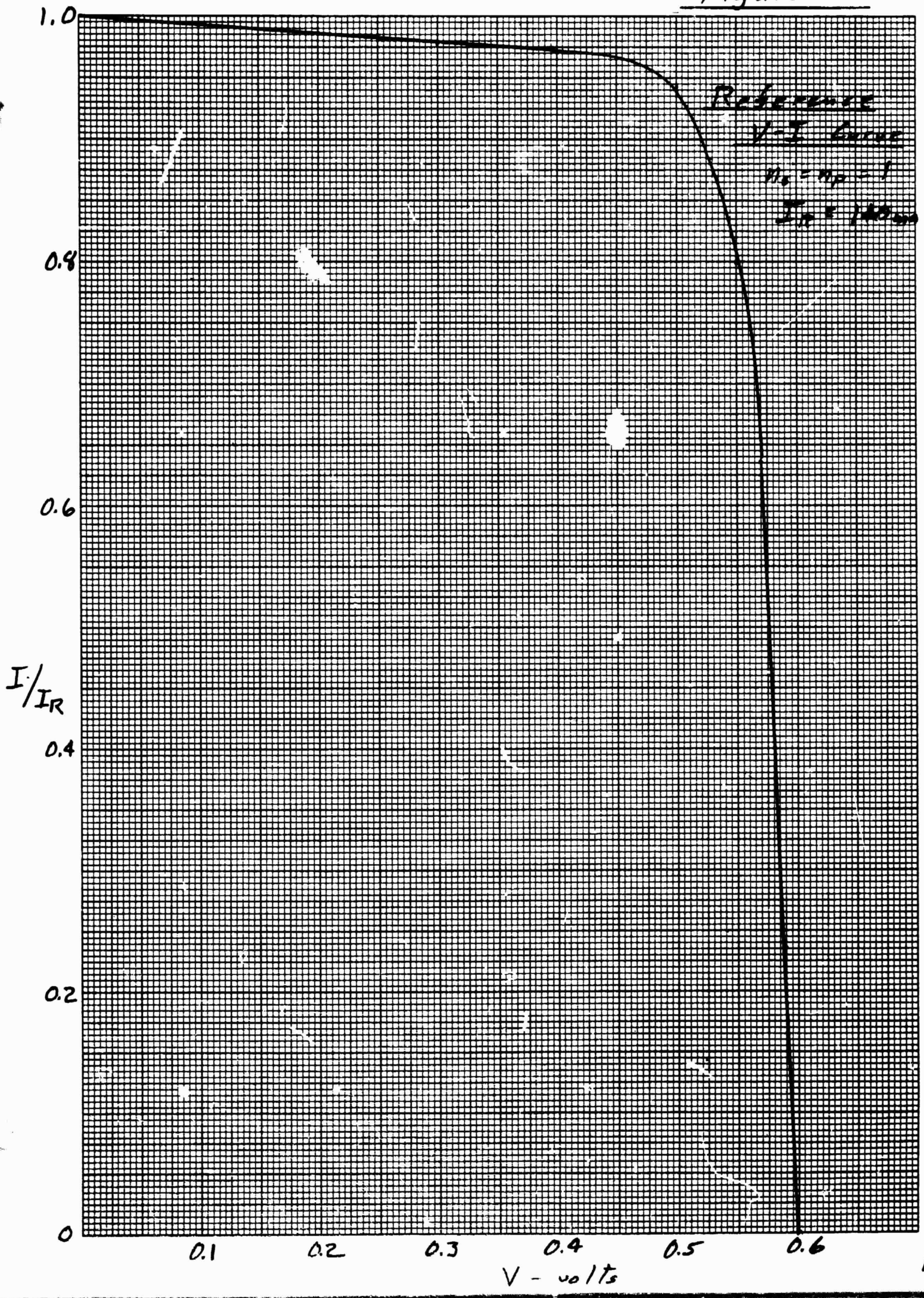
$$I_o = 1.4 \times 10^{-11}$$

$$V_t = 26 \text{ mv}$$

$$R_p = 100 \text{ ohms}$$

This characteristic can be scaled directly for any desired value of n_s or n_p .

Figure 15



3.0 Design Requirements

Based on the conclusions of the tradeoff studies the following design requirements have been established.

I. Range

A. Current

1. I_{sc} shall be adjustable from 0.1 to 20 amps.
2. Variation of I as a function of temperature, sun angle and illumination shall be accomplished by variation of a digitally programmable resistor.
3. Variation of I due to spinning shall be sine wave with an amplitude of no greater than 5% of I_{sc} and a frequency range of 0.1 to 2 Hz. Amplitude settings shall be by variation of a digitally programmable resistor. Frequency shall be set manually.

B. Voltage

1. V_{oc} shall be adjustable from 10 to 100 V.
2. An initial power supply setting shall be made manually to set the nominal V_{oc} for the simulation. This setting shall be 10V above the maximum V_{oc} of the simulation.
3. Variation of V as a function of temperature shall be accomplished by variation of a digitally programmable resistor.

C. Power

1. Maximum power output shall be 500w with $V_{oc} = 100v$, $I_{sc} = 7a$ at one extreme and with $I_{sc} = 20a$ and $V_{oc} = 34v$ at the other.
2. Minimum power at the maximum power point shall be 7.2w.
3. The locus of operating points shall be within the curve of Figure 13.

D. Impedance

The output impedance shall be flat within 3 db for all operating points out to 5 kHz.

E. Environmental

The SAS shall operate in a room environment of 60 to 80°F. Internal blowers shall be provided as necessary.

II. Input

A. Power

1. Input power shall be 115v, 60 Hz, single phase.

B. Internal Control

1. Initial settings shall be made manually at the console.
2. Time variation of I_{sc} and V_{oc} shall be controlled by a punched tape programmer which controls three digitally programmable resistors.

C. External Control

1. Time variation of I_{sc} and V_{oc} shall be capable of being controlled by a digital computer.

III. Output

A. Accuracy

For a given voltage the current shall be as determined from the reference V-I characteristic within $\pm 0.5\%$ of I_{sc} .

B. Ripple

The steady state ripple shall be less than .05% of V_{oc} or 50 mv whichever is less.

C. Curve Shape

The SAS shall exhibit a V-I characteristic which obeys the following relationship:

$$I_L = \frac{I_R}{H} - \frac{I_O}{H} \left[e^{V_L/nV_t} - 1 \right] - \frac{V_L}{nHR_p}$$

where I_R , I_O , V_t and R_p are fixed constants to be determined by the final design.

IV Miscellaneous

1. The SAS shall have a built in load which can sweep the entire V-I characteristic at any intermediate time for purposes of checking. It shall be controlled manually and the output shall be available to external recording devices.

2. The SAS shall be mounted in a single cabinet which contains all the power supplies, blowers, etc. necessary for its operation. Style, color and type shall be approved by the customer.

3. The basic 500w unit shall be modular in design and be mounted behind and on a standard rack panel complete with all heat sinking and blowers as required and connectors for interconnection to additional units, loads, and programmer.

4. Provision shall be made in the electrical design and mechanical design for addition of identical 500w modules in either parallel or series.

4. PRELIMINARY DESIGN

4.1 Electrical Design

An overall block diagram of the system is shown in Figure 16. The two main areas of circuit design were the series power regulator and the current amplifier. The preliminary schematics for these two blocks are shown in Figures 17 and 18 respectively. Maximum use was made of integrated circuit operational amplifiers in both of these designs. Design calculations performed during the course of the design indicate that the DC requirements for G and H can be met as specified in the accuracy analysis of Section 2.4 and that the variations of these parameters as specified can also be held.

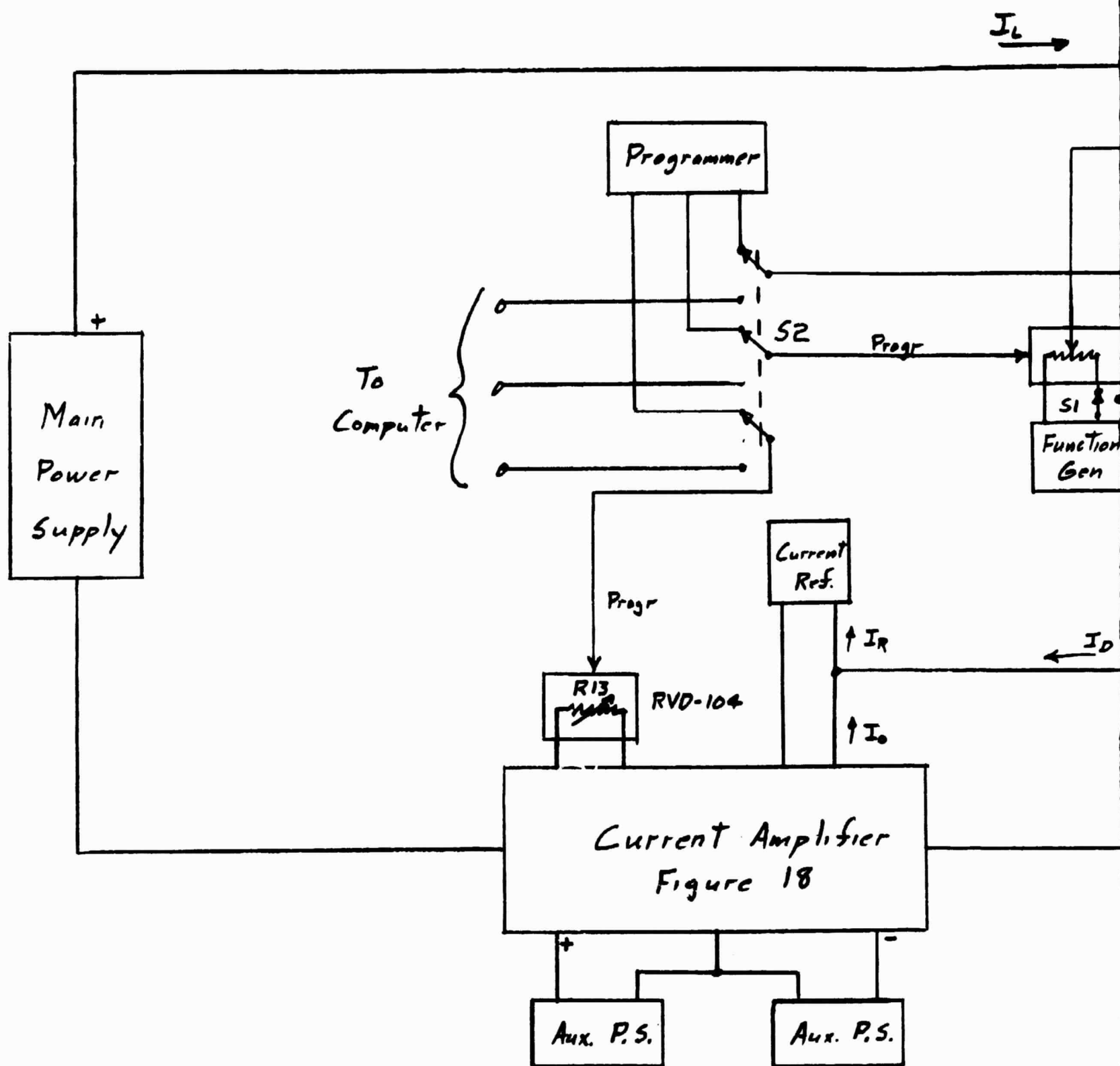
The diode reference will be an n on p silicon solar cell mounted on a thermoelectric cooler in order to maintain a constant temperature within $\pm 0.5^\circ\text{F}$.

The power supply selected for the main power supply will actually be two 60 volt, 20 amp supplies in series. The two auxiliary supplies will be standard lab supplies and the current reference will be a highly stable constant current supply.

The variation of H due to spinning will be controlled by a function generator capable of sine, triangular, and square waveforms over the range of .01 Hz to 100 kHz. The frequency and waveshape will be set manually and the amplitude will be varied by a digitally programmable resistor.

The variation of H due to other illumination variations and the variation of G due to temperature variations will be controlled by digitally programmable resistors also. These same resistors are set initially to account for the number of cells in parallel and in series. This can be handled either through the programmer or manually with front panel switches. These two resistors along with the one for the function generator will be four decade, .01% devices with each decade controlled by a 1-2-4-2 BCD code.

SK



ORIGINAL

MJO

SK Figure 16

CHG LTR

I_L

I_{spw}

Progr

R1

RVD 104

RVD-104

To Dummy Load

SI

Function Gen

Series Regulator & Reference Stage

Figure 17

Ref. Diode & Oven

I_D

I_L

From Function Gen

Dummy Load

V

I

Output

ORIGINATOR	DATE	TITLE	ENGINEERING SKETCH
		FRSAS	TRW SYSTEMS
		System Block Diagram	ONE SPACE PARK • REDONDO BEACH, CALIFORNIA
MJO			SK Figure 16
			SHEET OF

SYSTEMS 8238 Rev. 2/66 47

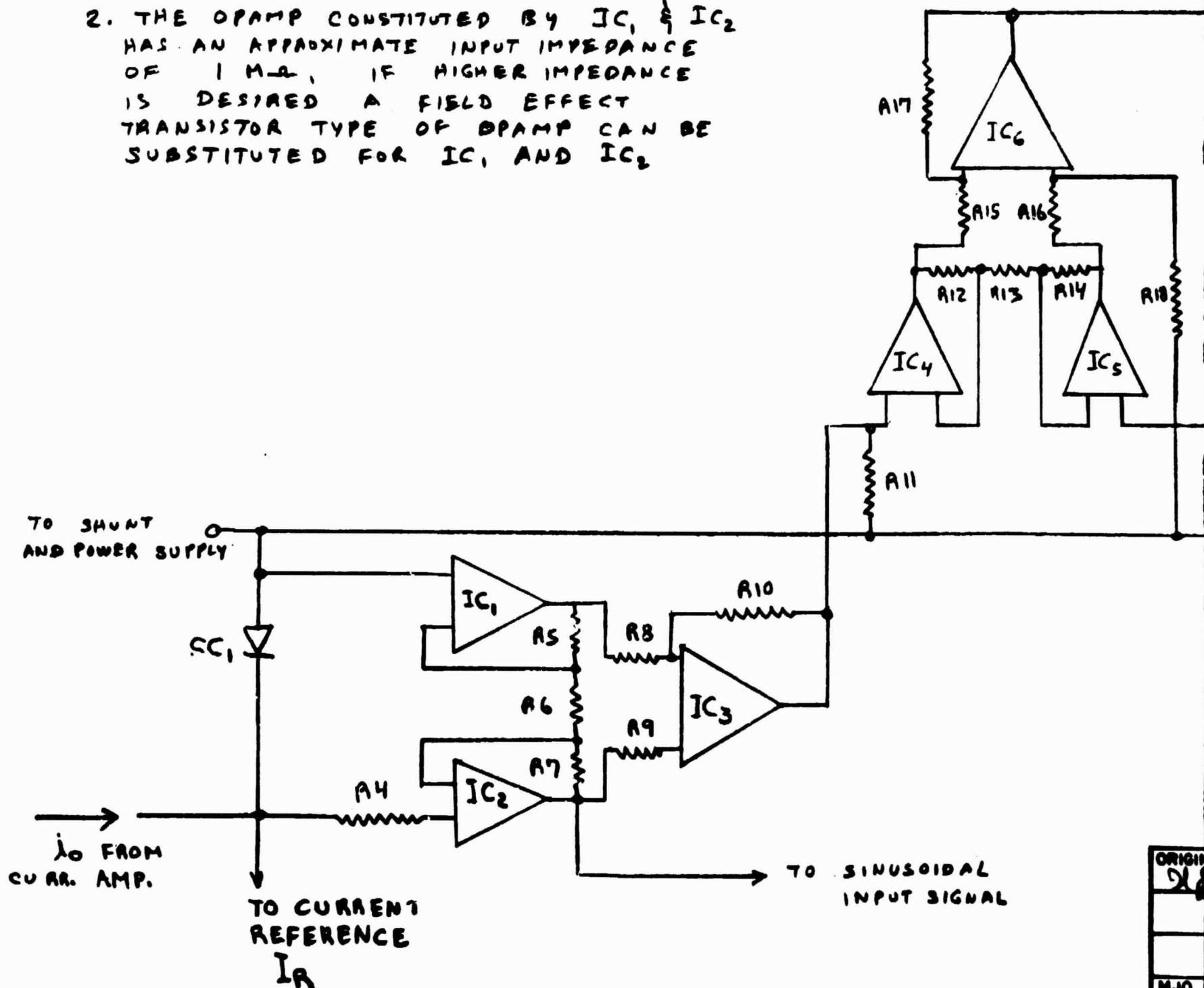
47B

SK

TO POWER SUPPLY

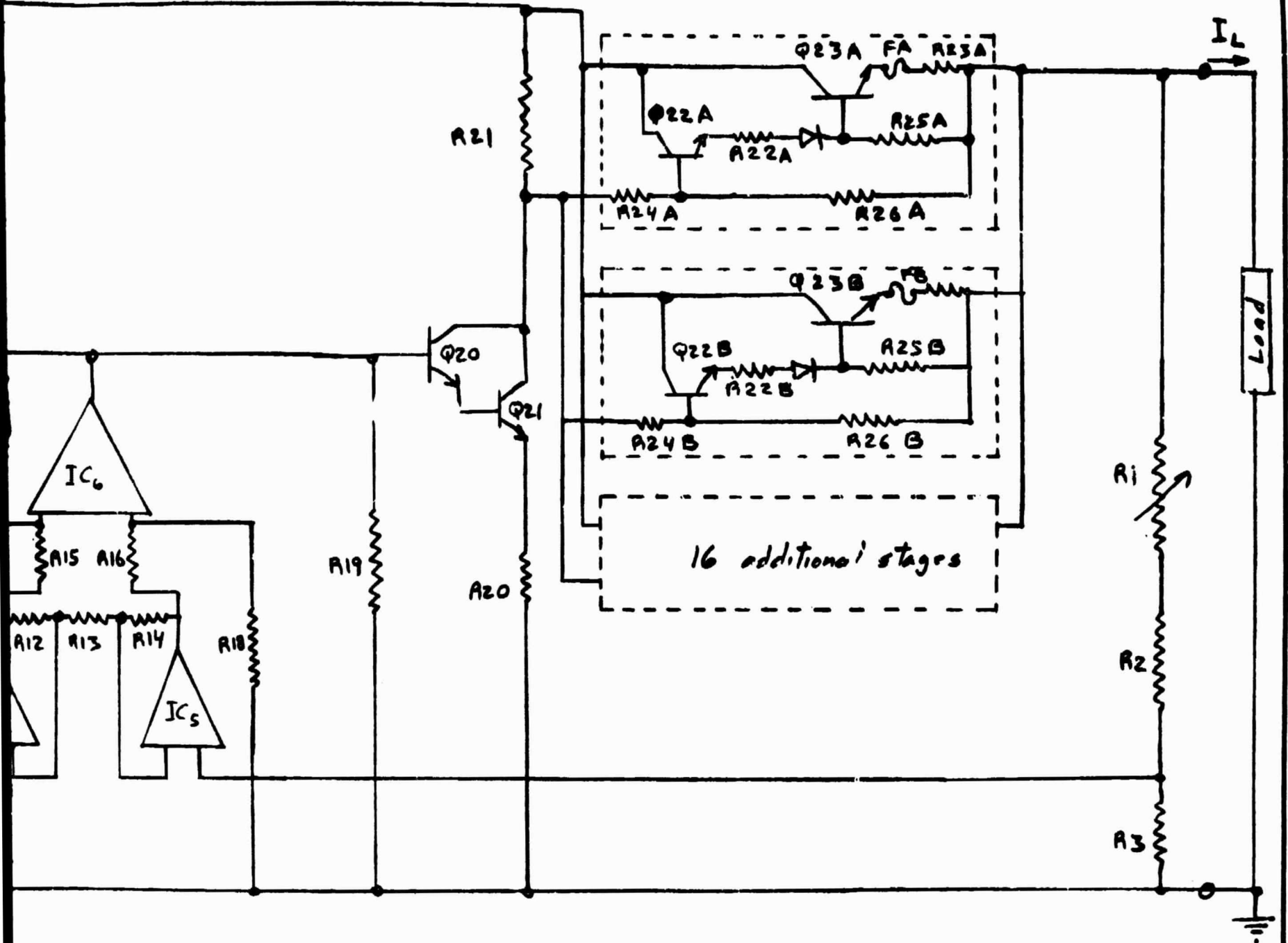
NOTES:

1. THE CURRENT AMPLIFIER GAIN HAS A GAIN THAT MAY CHANGE BY A FACTOR OF 4:1, IF LESS VARIATION IS DESIRED, ONE ADDITIONAL AMPLIFICATION STAGE HAS TO BE ADDED.
2. THE OPAMP CONSTITUTED BY IC_1 & IC_2 HAS AN APPROXIMATE INPUT IMPEDANCE OF $1\text{ M}\Omega$, IF HIGHER IMPEDANCE IS DESIRED A FIELD EFFECT TRANSISTOR TYPE OF OPAMP CAN BE SUBSTITUTED FOR IC_1 AND IC_2 .



SK Figure 17

CHG LTR



ORIGINATOR
J. E. Gavito

DATE
10-7-68

TITLE

FRSAS
Series Regulator
&
Reference Stage

ENGINEERING SKETCH

TRW SYSTEMS
ONE SPACE PARK • REDONDO BEACH, CALIFORNIA

SK Fig. 17

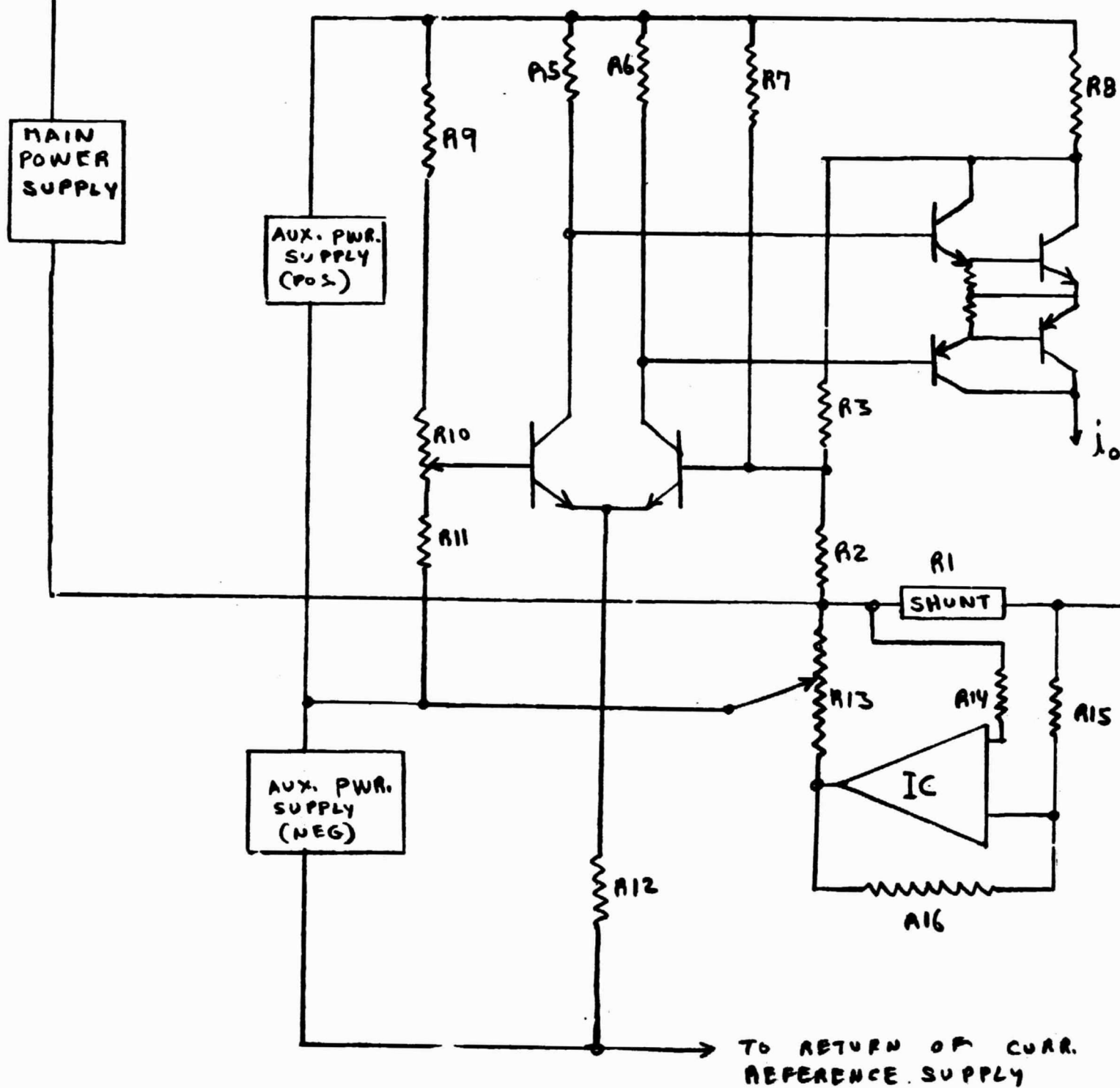
SHEET OF

MJO

SYSTEMS 5238 Rev. 2/66 48

FOLDOUT FRAME 2

SK



- NOT
1. POT
2. RE
DIV
CU

ORIGINAL
MJO

FOLDOUT FRAME /

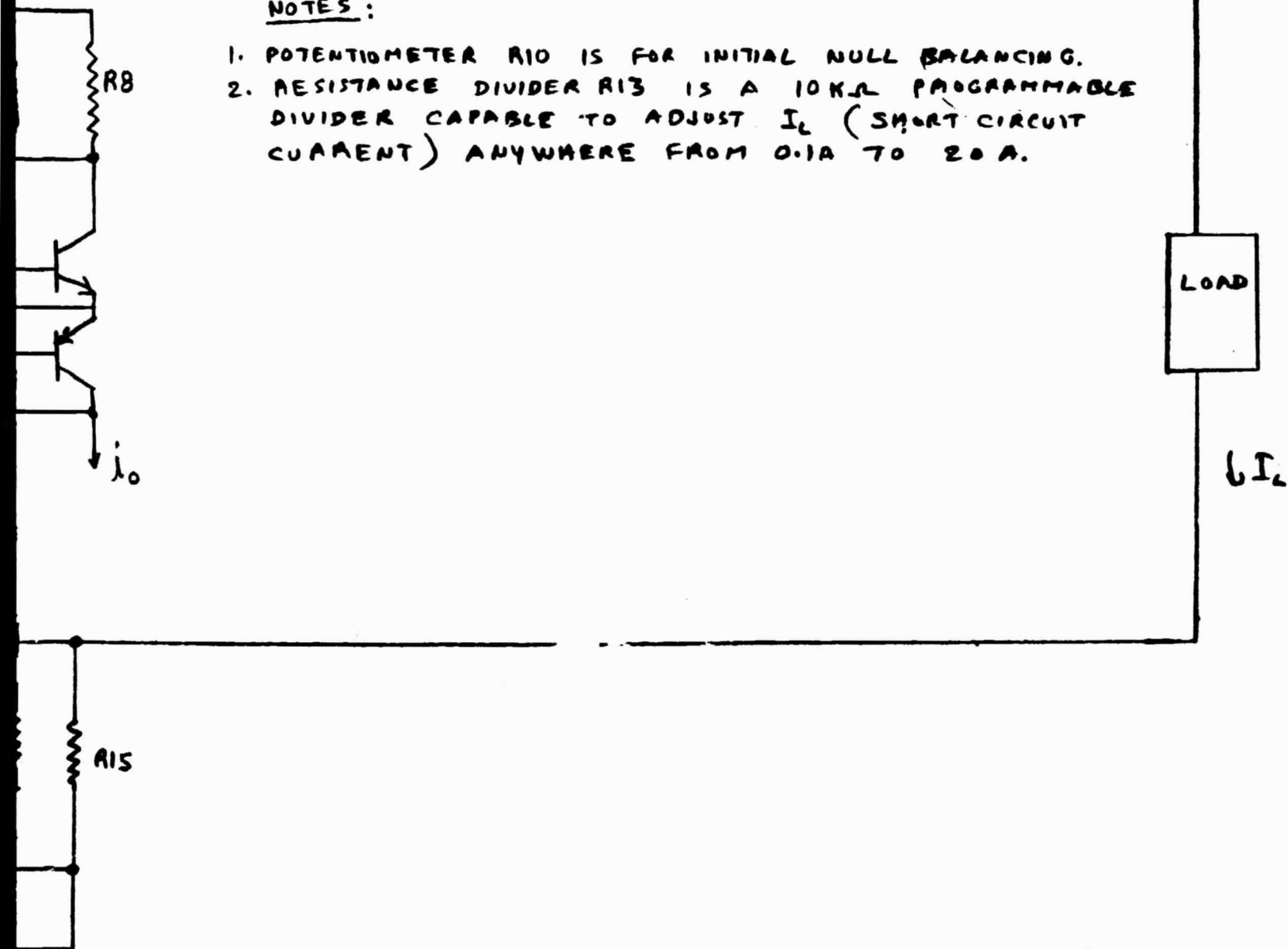
SK Figure 18

CHG LTR

IMPEDANCE EQUALIZER
AND VOLTAGE REGULATOR
USING OPERATIONAL
AMPLIFIERS

NOTES:

1. POTENTIOMETER R10 IS FOR INITIAL NULL BALANCING.
2. RESISTANCE DIVIDER R13 IS A 10K Ω PROGRAMMABLE DIVIDER CAPABLE TO ADJUST I_L (SHORT CIRCUIT CURRENT) ANYWHERE FROM 0.1A TO 2.0A.



ORIGINATOR J E Gavira	DATE 10-7-68	TITLE FRSAS Current Amplifier	ENGINEERING SKETCH TRW SYSTEMS ONE SPACE PARK - REDONDO BEACH, CALIFORNIA
MJO			SK Fig. 18
			SHEET OF

The internal programmer will be a punched tape programmer capable of providing 82 bits of digital information from a mylar tape. Tape advance speed is variable. As well as controlling the three digital resistors the programmer will also completely shut down the simulator for eclipse conditions. A tape punch will also be provided. Provisions will be provided on the front panel and through the rear panel connectors for switching from the internal programmer to external computer control.

A dummy load will be provided which when manually switched to the function generator will sweep the entire operating range at the selected frequency. Provisions will be provided for displaying voltage and current on an oscilloscope or some other suitable recording device.

A preliminary parts list is given below as Table VI.

TABLE VI
Preliminary Parts List

<u>Quantity</u>	<u>Item</u>	<u>Part No.</u>
2	Main Power Supply	Kepco KS-60-20M
2	Aux. Power Supply	HP 6202B
1	Constant Current Supply	HP 6181A
1	Function Generator	HP 3300A
3	Programmable Resistor	JRL RVD-104
1	Programmer	Ind. Timer Mod. 282
1	Diode Reference	
1	Thermoelectric Cooler	Borg-Warner Mod. 920
28	Power Transistor	SDT-8801
30	Med. Power Transistor	SDT-5951
5	Signal Transistor	Misc.

TABLE VI - Preliminary Parts List (Cont'd)

<u>Quantity</u>	<u>Item</u>	<u>Part No.</u>
7	Operational Amplifiers	RA-909
150	Resistors	
30	Diodes	
10	Capacitors	
1	Current Shunt	
3	Heat Sink	Wakefield FCA-800
1	Rack and Blowers	

4.2 Mechanical Design

The system will have to be housed in a double bay rack due to power dissipation and space requirements both. In the worst case approximately 2500 watts will have to be dissipated. The capital equipment alone will occupy one bay with the power stages, dummy load and control panel occupying the other. Power dissipation will be equalized as much as possible between the two bays however.

Provisions for interconnection with the computer, the load, and additional power modules will be provided at the rear of the cabinet. Test points will be provided at the rear with vital test points also being brought out to the front panel.

5. SUMMARY

5.1 General

The tradeoff studies of Section 2 revealed that an analog generation of the basic V-I characteristic utilizing a forward biased solar cell as the basic reference can result in a true simulation of the static and dynamic characteristics of the solar array. This type of a generation scheme however can most easily be programmed by digital means. A 500 watt power module was found to be the best tradeoff between flexibility, accuracy, and cost considerations. Accuracy analysis showed that a current accuracy of $\pm 0.5\%$ of short circuit current could be achieved. Based on these conclusions a reference design based on a 500w analog/digital concept was selected and preliminary design calculations showed it to be capable of meeting the desired design requirements.

5.2 Materials Report

No tests, experiments, developments, studies or other efforts were performed on materials during the period of the study.

5.3 New Technology

The use of the forward biased solar cell as a reference to obtain the dynamic characteristics of the solar array is thought to be a new technology innovation and the required report will be submitted.

6. BIBLIOGRAPHY

1. Transistor Engineering; A. B. Phillips, p. 252, McGraw-Hill, 1962.
2. Proposal for the Fast Response Solar Array Simulator; TRW Systems
Proposal No. 11799.000, May 20, 1968.
3. Advanced Voltage Regulator Techniques As Applied To Maximum Power
Point Tracking Systems For The Nimbus Meteorological Satellite;
Final Report, 16 June 1965 through 10 October 1967, Contract
No. NAS5-3248.