FINAL REPORT

PROJECT A-919

DESIGN AND DEVELOPMENT OF A MULTI-LAYER MEMORY SYSTEM

F. L. GRISMORE, L. H. GLASSMAN, R. P. WOODWARD
AND M. D. CARITHERS

Contract No. NAS8-20577

28 January 1966 to 27 January 1967

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Engineering Experiment Station
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I. INTRODUCTION

The purpose of this research was to study the feasibility of completely integrating a small magnetic memory on a single substrate. The ultimate goal is envisioned as a substrate of silicon with the complete complement of electronic circuitry formed by diffusion processing around the outer periphery. The memory array, per se, would be fabricated by multilayer vacuum deposition in the central region of the substrate. Interconnection of the array transmission lines and electronic circuits would be affected by thin film metallization employing vacuum evaporation.

A memory of this type would be extremely compact and lightweight. Because there are no hand-formed interconnections the scheme provides for potentially high reliability. Once fabricated the memory becomes essentially a single "block" and as such should be physically rugged, and able to operate under high ambient accelerations and vibration without failure. Finally, a compact memory plane of this type complete with selection, driving, and sensing electronics provides a basic modular unit which can be easily stacked to form a wide variety of larger memories. These characteristics make a memory plane of this type ideally suited for space applications where reliability and flexibility, coupled with small size and lightweight, are of utmost importance.

As an initial step toward completion of this overall memory concept, this one year program has concentrated on developing a hybrid system. The memory array has been fabricated on a separate substrate. This array contains all the drive and sense transmission lines and the thin magnetic film memory cells. In addition, the selection diodes are mounted on the word lines of this array. The electronic circuits are mounted on daughter boards by type, i.e., driver gates, bit drivers, sense amplifiers, etc., and these are, in turn, interconnected with each other and the memory plane by a system mother board. This latter printed circuit board contains a centrally located recess which accepts the array substrate and provides the interconnection patterns to complete the system. The electronics are designed to be completely fabricated by monolithic techniques. However, in the system constructed, some discrete components were used to avoid the excessive cost of fabricating prototype integrated circuits for this initial model.

The program effort was divided into the four major areas: system design and analysis, keeper development, circuit design and analysis, and

memory array fabrication. In the system design and analysis phase the overall parameters and performance-fabrication trade-offs were decided. Digital and analog computer programs were written to perform general memory array analysis. These should be useful to M.S.F.C. in future memory system analysis problems. A flexible keeper material was designed and tested which has a relative permeability of approximately 10 to above 200 MHz. This is a critical component to all flat thin film memory systems. As a result of the circuits effort a completely integrable system of memory electronics was designed and evaluated. A system power consumption of 1 watt at a 250 kHz read-write cycle was achieved. It is also significant that a high degree of modularity was achieved within this design so that a basic circuit module is used for each function. This permits redundancy techniques to be employed in fabrication of the ultimate memory plane and thus provides for a potentially high yield. The fabrication effort was responsible for developing the techniques of multilayer evaporation necessary to fabricate the memory array plane. This involved the selection of a combination of materials that were chemically and thermally compatible and could be evaporated to large thickness. One of the major problems solved in this phase was that of achieving stable insulating layers of SiO over relatively large planar areas. A new type of evaporation source was conceived and developed during the contract for this purpose.

Because of time limitations an operable system was not attained. Peeling problems associated with the permalloy-SiO interface within the film array prevented a completely satisfactory plane from being constructed. There is little doubt, however, that this problem can be solved with additional future effort. All other major fabrication problems have been solved and a compatible system developed. It is believed that the results of this research do indicate the feasibility of the proposed thin magnetic film integrated memory concept. Using the techniques developed a memory of 10^6 bits can be packaged in a volume of approximately 10^3 cubic inches thus providing future space probes with a highly sophisticated computer memory with high reliability and low power consumption.

II. MEMORY SYSTEM DESIGN

A. INTRODUCTION

The design of the overall memory system involves trade-offs between physically realizable fabrication parameters and electronics capabilities. As an overall goal, drive currents of less than 200 ma and sense signals out of the transmission line of approximately 2 mv are desired. Although this particular program required a design operating at 100 kc repetition rate, all work is being carried out with a 200 ns cycles time as a basic goal. This small system is directed toward studying the fabrication and electrical constraints for an all evaporated memory of this type with all integrated circuits. Satisfactory achievement of such a system should provide future space craft with main processor memories of high reliability, low power consumption and small physical size.

B. BASIC MEMORY PLANE

The basic memory plane consists of the array of magnetic bits and all associated drive and sense lines plus word selection buss lines and selection diodes. The configuration is shown in Figure 2.1. The magnetic film storage media consists of strips located under every other sense line with the easy axis along the length of the strips. In this arrangement, there is no critical alignment of the word line mask since the film is continuous in the easy axis direction. Bit isolation along the strip is effected by domain walls. Such walls have been shown to be stable under pulse conditions in previously published systems. A ferrite keeper covers the entire array.

Structurally the array consists of a substrate with successive layers evaporated to form a ground plane, magnetic film, bit-sense lines and word lines. Intermediate layers of insulation are also evaporated. A vertical cross-section is shown in Figure 2.2. A keeper over the entire array minimizes demagnetizing fields, and eddy current spreading effects in the ground plane.

System analysis and design can be broken down into the areas of magnetic film properties, transmission line effects, keeper effects, and circuits.

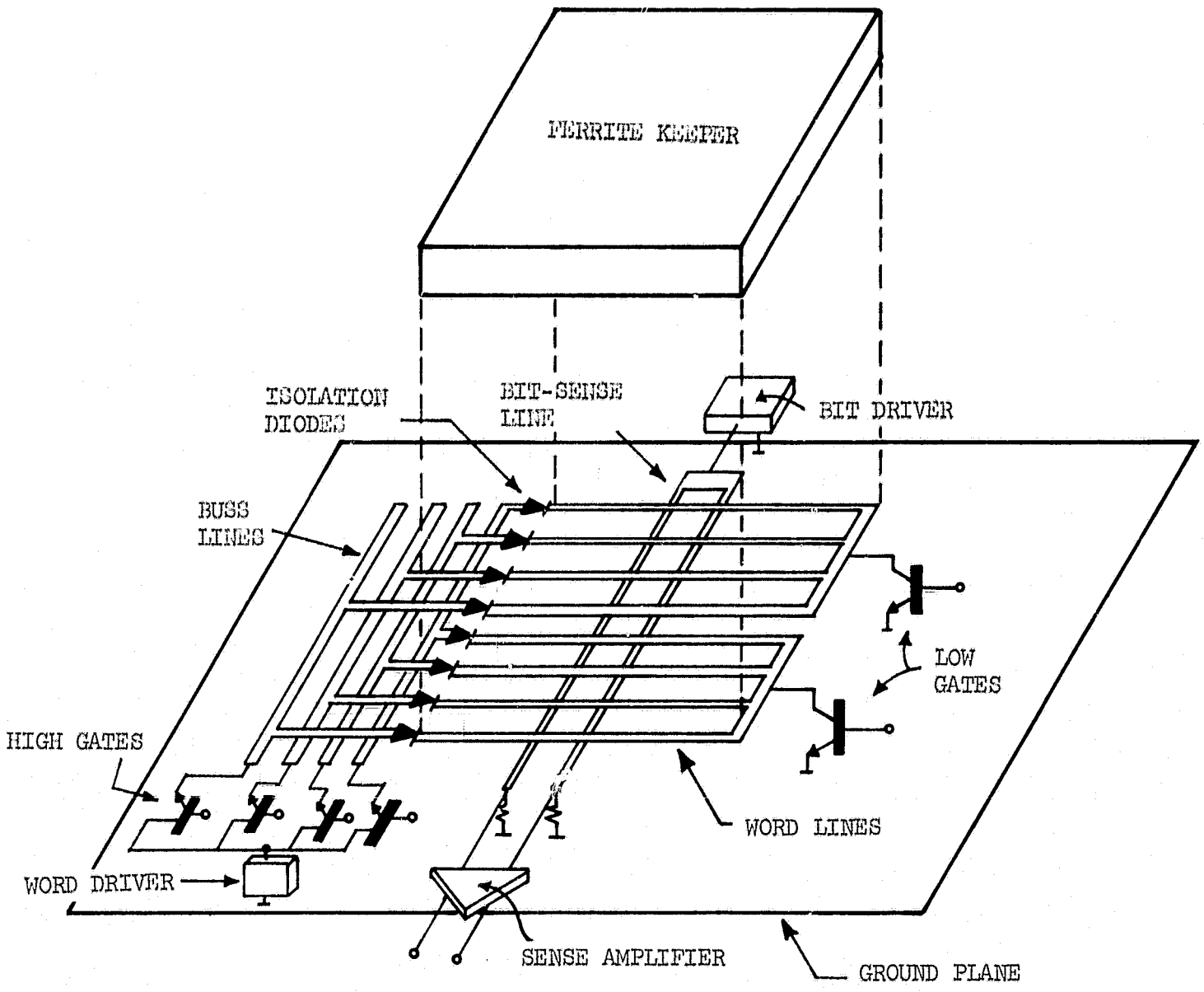


Figure 2.1 Representation of Memory System Structure

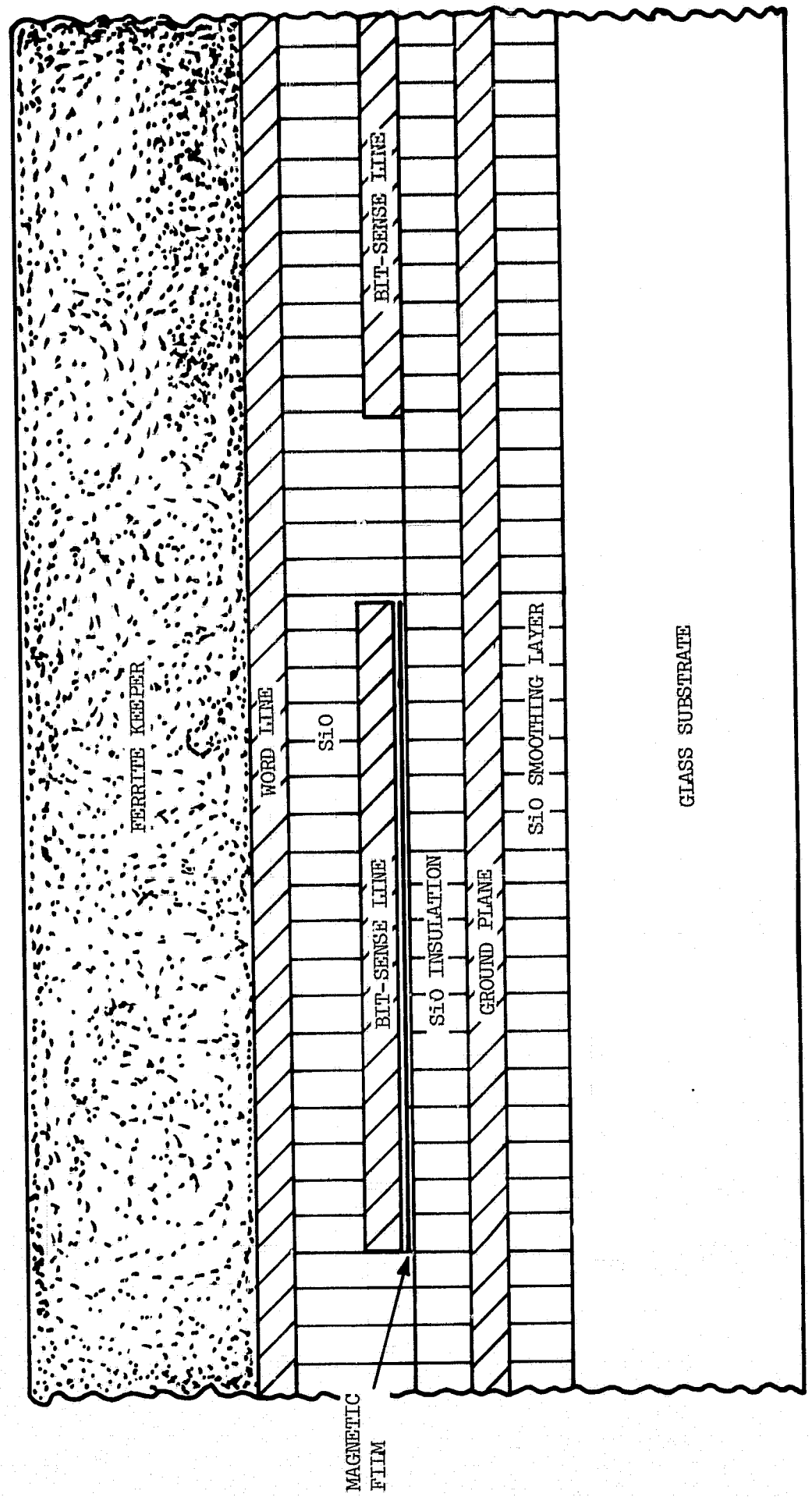


Figure 2.2 Cross-Sectional Representation of Memory Plane (Not to Scale)

C. MAGNETIC FIIM

Although there are various materials which can be employed for the storage, film Ni-Fe has been chosen because of previously demonstrated capability.

From a system design point of view, geometry must be chosen to achieve as much stored flux as possible, consistent with stability from creep and low dispersion. In the structure chosen for this system, the film is continuous in the easy axis, i.e., there is no physical point of discontinuous $\bar{M}$. Although rigorous analytical treatment is impossible with nearly any practical geometry, it should be reasonable to assume an oblate spheroid approximation for demagnetizing calculations. This approximation has been shown reasonable by a number of experimenters and is employed here.

For calculation the bit size is assumed equal to the bit line-word line intersection. Assuming the word line is 10 mil wide and the bit line 20 mil, the magnetic storage location is then rectangular with dimensions of 10 mil x 20 mil. Thickness is chosen to be a compromise of creep sensitivity and stored flux. Middelhoek[1] has shown a maximum in stability occurs at approximately 750 Å which is the thickness corresponding to the transition from cross-tie to Block wall structures. This thickness is chosen in this system. The demagnetizing field is approximated (as an open flux element) by the expression

$$H_d \text{ (oersted)} = \frac{c}{b} (4\pi M) A_d \qquad (2.1)$$

where

- c = film thickness
- b = length in hard direction
- M = discontinuity in magnetization at film edge
- A_d = demagnetizing factor which is a function of the ratio of easy axis length/hard axis length

A plot of A_d is included as Appendix A of this report. If the film is considered to have no keeper then M is equal to M_s, the saturation magnetization, or approximately 800 gauss. For c = 750 Å = 75 x 10^{-8} meter,

b = 10 mil = 2.5×10^{-4} meter and a, the easy axis length, of 5×10^{-4} meter the calculation yields

$$H_d = 0.96 \text{ Oersted} .$$

If the film is 10 mil x 10 mil, the demagnetizing factor from Appendix I is 0.79 and the open flux structure demagnetizing field becomes

$$H_d = 2.37 \text{ Oersted} .$$

This shows the effects of changing the easy axis length, i.e., the width of the bit line. Since the dispersion is very sensitive to easy axis demagnetizing field strength and disturb margin is decreased with increasing demagnetizing field, the value of 2.37 Oersted is probably impractical. However, it will be shown later that the keeper affects a flux closure of approximately 80%. Thus, with a keeper, $M \approx 80$ gauss and H_d reduces to

$$H_d = 0.57 \text{ Oersted (with keeper, 10 x 10 mil film)}$$

$$H_d = 0.2 \text{ Oersted (with keeper, 10 x 20 mil film)}$$

In either case, this is small with respect to normal values of H_c and the film should be quite stable on a dc basis. Demagnetization effects on write currents will be discussed later.

The film properties we are then aiming for are these values:

Thickness = 750 Å
H_k = 4 Oersted
$H_c \geqq 2$ Oersted
dispersion + skew $\leqq \pm 3^\circ$

D. KEEPER EFFECTS

A magnetic keeper closely situated to the memory array provides significant improvement in a number of ways. With respect to the magnetic film itself it decreases the demagnetizing field, as previously discussed, and it permits nearly 100% flux linkage to the bit line by providing a low reluctance flux path around the film. It is well-known that the flux penetrating into the ground plane causes a damping effect of eddy current origin as the film is switched. With a keeper this effect is nearly eliminated.

It can also be shown that the keeper plays a significant role in minimizing the reduction of the H field due to eddy current decay when currents are passed down the drive lines. These effects can all be analyzed by straightforward image techniques which are developed in Appendix B. From the derivations in Appendix B it is found that the effect of the keeper is to produce a magnetostatic image of a magnetic film equal to

$$M_i = \left(\frac{1 - \mu_r}{1 + \mu_r}\right) M_f \quad , \tag{2.2}$$

and an image of a current carrying conductor equal to

$$I_i = \left(\frac{\mu_r - 1}{1 + \mu_r}\right) I \tag{2.3}$$

where

M_i = magnetization of the film image
I_i = amplitude of current image
M_f = magnetization of the actual film
I = amplitude of the actual source current
μ_r = relative permeability of the keeper

With these image solutions it is possible to estimate the effect of the keeper on demagnetization fields and current spreading effects.

The effectiveness of the keeper in reducing demagnetizing fields and increasing bit line flux linkages can be illustrated by the following example. If the relative permeability of the keeper is $\mu_r = 10$ then the material

creates an effective magnetic image of the film magnetization of 0.8 M_f. Within the film itself, the total internal field is the algebraic sum of its own demagnetizing field and the external field of the image. Since the film-to-image separation is very small this external field is approximately equal to the image demagnetizing field, which is in turn 0.8 times that of the actual film. Thus, the effective demagnetizing field is only 20% of what it would be without the keeper.

Similarly, the flux linkage to a bit-sense line located between the film and image is the sum of the linkages due to the image and actual film. In the case described:

$$\lambda_T \approx \tfrac{1}{2}\Phi_f + \tfrac{1}{2}\Phi_i = \tfrac{1}{2}(\Phi_f + 0.8\,\Phi_f) = 0.9\,\Phi_f \qquad (2.4)$$

where

λ_T = total flux linkages
Φ_i = total flux in film
Φ_f = total flux in image

thus, nearly complete flux linkage may be realized with the keeper.

In the ground plane below the film the flux from the image is oppositely directed to that from the film, thus causing a canellation. This nearly eliminates eddy current braking of magnetization rotation which normally occurs with films over conducting ground planes.

With these considerations of keeper effects in mind, it is seen that a keeper with $\mu_r \approx 10$ is desirable. Higher permeabilities are not necessary. From a practical point of view we have specified for this program the development of a keeper materials with $\mu_r \cong 8$ and made in such a way that separation between line and keeper should be approximately 2 μ or less.

E. WORD LINE AND DRIVE FIELD ANALYSIS

In considering operation of a memory system, transmission characteristics into and out of the array are of prime importance. In a memory of the type being developed here, word line and bit-sense line characteristics are different and must be analyzed and designed separately. Computer programs have been developed to aid in the analysis of the transmission system.

While the numerical examples in this report are directly related to the system under contract, it should be emphasized that the programs and techniques are completely general. Thus, a wide variety of memory problems can be analyzed with these techniques.

There are two basic problems to consider when designing the word drive line system. First, the drive efficiency, i.e., the resulting H field per ampere of current in the line, and secondly, the pulse attenuation along the line length must be determined.

1. Line Efficiency

The problem of determining the field for a given current through a word line can be broken up into three parts. These are the field due to the drive current in free space, the field due to the magneto-static effects of the keeper, and finally the field due to eddy currents in the ground plane. All three effects can be calculated from the basic equation of the field generated from a current carrying flat strip. The derivation for this equation is carried out in Appendix C, yielding the result

$$H = \frac{I}{2\pi w}\left[\tan^{-1}\left(\frac{\ell + w/2}{h}\right) - \tan^{-1}\left(\frac{\ell - w/2}{h}\right)\right] . \qquad (2.5)$$

In this expression:

H = horizontal component of the total field

w = width of the current carrying strip

h = vertical separation from strip to point of field calculation

ℓ = horizontal distance from center of strip to point of field calculation

1.1 Field From Actual Current. Note that for the case where $\ell = 0$, i.e., directly beneath the current carrying strip, the above expression reduces to

$$H_{11}\ (\text{center}) = \frac{I}{\pi w}\tan^{-1}\left(\frac{w}{2h}\right) . \qquad (2.6)$$

From this expression it is easy to see that the ratio of w/h must be as

large as possible and w as small as possible in order to maximize the field. Note, however, that because of the shape of the $\tan^{-1}$ function, no appreciable increase in field strength occurs for $w/h > 12$. At this width to separation ratio the resulting field is approximately 90% of its maximum attainable value of $H_{11}(max.) = I/2w$. In design of the line system then we strive for a geometry where

$$.12 \leqq w/h \quad .$$

To achieve maximum drive fields it is desirable to reduce w. It was previously shown, however, that the stored flux in the film is directly proportional to w, assuming the film to be the same width as the drive line. Therefore, the final dimensions chosen must be a compromise so as to yield a satisfactorily large sense signal at drive current compatible with integrated circuit electronics.

1.2 Field From Ground Plane Currents. The field resulting from eddy currents in the ground plane is difficult to determine in general. Recently Liniger and Schmidt[2] have presented a completely general solution to a single filamentary current over a ground plane of finite resistivity. The resulting equations must be solved by numerical techniques of an extensive nature. Fortunately under limiting conditions of either a very thin ground plane or a very thick one, the calculations are considerably simplified. In this report only the case of a very thin ground plane is described. This is the condition existing with an evaporated conducting layer.

Smyth[3] shows that for a thin ground plane the field resulting from induced currents can be accounted for by an image of the original source. The polarity of the image is such that the vector potential $\bar{A}$ at the conducting surface does not change instantaneously. The decay of the eddy currents is accounted for by letting the image recede with a velocity governed by the resistivity and permeability of the ground plane.

For example, consider the case of a current carrying strip at height h above a thin ground plane. The vector potential at the surface of the ground plane is zero. Now if a current step $I = o,\ t < o;\ I = 1,\ t \geqq o$ is applied to the strip an image will appear at a height h below the ground plane such that $I = o,\ t < o;\ I = -1\ t \geqq o$. Thus, the image is a negative

current, i.e., oppositely directed from the original source. The H field on the positive side of the ground plane due to this image can be calculated directly from the previous equation as

$$H_{lli} = \frac{I_i}{2\pi w}\left[\tan^{-1}\left(\frac{t + w/2}{h_i}\right) - \tan^{-1}\left(\frac{t - w/2}{h_i}\right)\right] \qquad (2.7)$$

where now I_i is the image current, i.e., $I_i = -I$ and h_i is negative. It can, therefore, be seen that since both I_i and h_i are negative numbers the resulting image field adds to the field of the strip which would exist if the ground plane were not present.

Since ground plane eddy currents are transient in nature H_{lli} is time dependent. Smyth shows that this can be taken into account by letting the image recede from its initial t = o position of -h, with a velocity of

$$v = \frac{2\rho_s}{\mu} \qquad (2.8)$$

where ρ_s is the sheet resistivity of the ground plane. Thus for an applied current step at t = o, the H field resulting from ground plane currents is

$$H_{lli}(t) = \frac{-I}{2\pi w}\left[\tan^{-1}\left(\frac{t - w/2}{h + vt}\right) - \tan^{-1}\left(\frac{t + w/2}{h + vt}\right)\right] . \qquad (2.9)$$

The velocity associated with a 2 micron aluminum ground plane can be shown to be

$$v = 2.2 \times 10^{4} \text{ m/sec}$$

since $\rho_s = 1.41 \times 10^{-2}$ and $\mu = \mu_o$. This means that in only 10 ns the image will have moved 220 microns.

To determine the field for an arbitrary current pulse shape a computer program was written. For this program, an arbitrary pulse shape is approximated by a sequence of positive and negative steps. Up to twenty

steps may be used to approximate a pulse. The actual program and operating instructions are not given in this report; however, complete information can be obtained at any time by contacting the Solid State Circuits Lab at Georgia Tech. Some selected results obtained from this program during the system design phase of this contract are shown in the following four figures. In these computer runs the total field under a strip line, with a thin ground plane present, is calculated. Thus, the computer program calculates the sum of the fields due to the current in the strip line and the induced ground plane currents.

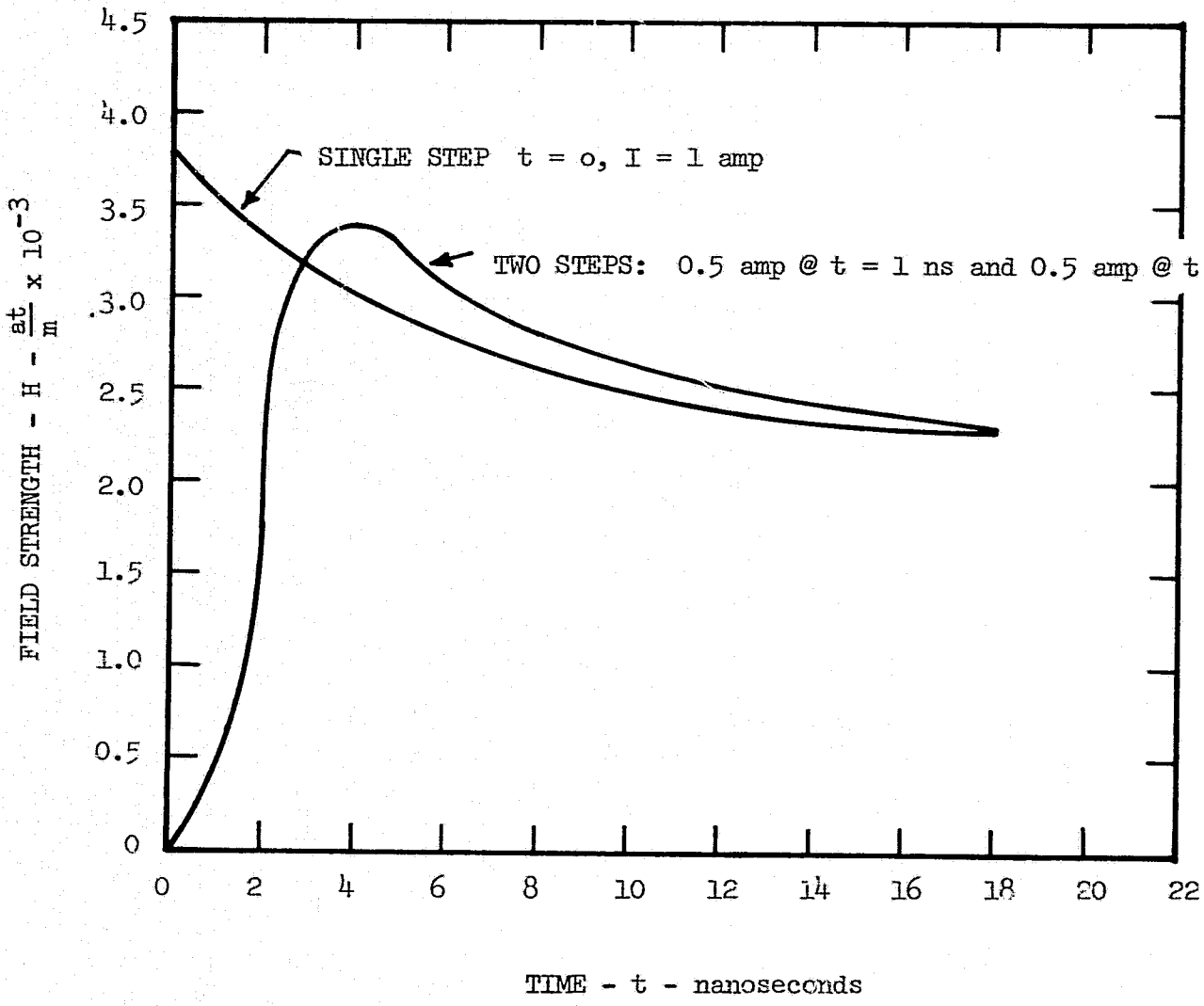
Figure 2.3 shows the effect of approximating a finite rise time current with a single step and a combination of two steps. It is seen that a single step approximation is optimistic at very small time periods but pessimistic at extended times. The difference in peak amplitude of fields predicted is less than 10% in this case. The fields were calculated for a 10 mil wide strip line located 10 μ above a ground plane. The sheet resistivity of the ground plane is assumed to be 0.014 ohm per square. Note how rapidly the field decreases from its peak value.

Figure 2.4 shows the field resulting from a 1 amp, 10 ns wide current pulse. Four steps have been used to approximate the leading edge and three have been used at the trailing edge. Note that the peak field calculated is identical to that previously obtained with a two-step approximation. This indicates that rather crude approximations can be used with little loss in information. The interesting aspect of this calculation is the observance of a negative H field at the trailing edge of the current pulse. While such a reverse hard axis field might aid the writing process of a film element, it is undesirable as a disturbing influence since bipolar hard axis disturbs create worst case creeping.

Figure 2.5, however, illustrates that adjacent word line disturb fields are of negligible amplitude for a thin film structure. In this figure the drive current is identical to that used in Figure 2.4. The fields calculated are at three different horizontal distances along the ground plane. These are (1) directly under the center of the 10 mil drive line, (2) directly under the edge of the line, and (3) 20 mil from the center of the drive line. From this data two features are apparent. First, the drive field under the line is non-uniform, falling to half amplitude at the edge. It can be shown, however, that the field under the line

FIELD STRENGTH vs. TIME

COMPARISON OF CALCULATIONS FOR FIELD DIRECTLY
UNDER CENTER OF STRIP LINE FOR APPLIED STEP AT t = o
AND TWO-STEP APPROXIMATION WITH EFFECTING t_p = 4 ns.



WD = 250 μ

HT = 10 μ

R_s = .014 Ω/square

Figure 2.3 Calculated Field Under Strip Line with Thin Film Ground Plane for Single and Double Step Approximations of Rise Time

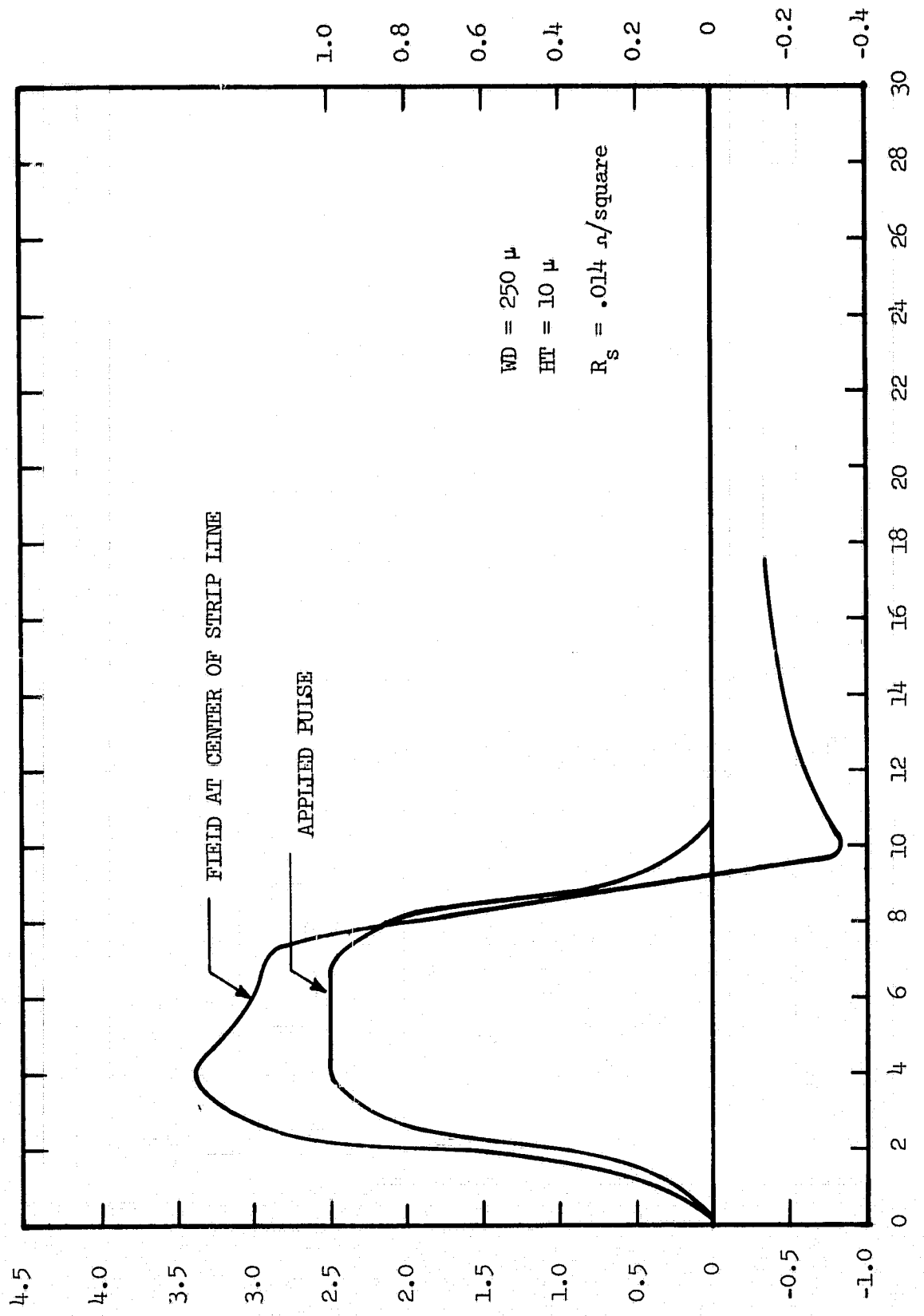


Figure 2.4 Calculated Field Under Strip Line with Thin Film Ground Plane for 10 Nanosecond Wide Current Pulse

FIELD STRENGTH vs. TIME

FIELD STRENGTH AT THREE LOCATIONS ALONG
GROUND PLANE FOR DRIVE PULSE OF 1 amp @ t_p = 3 ns

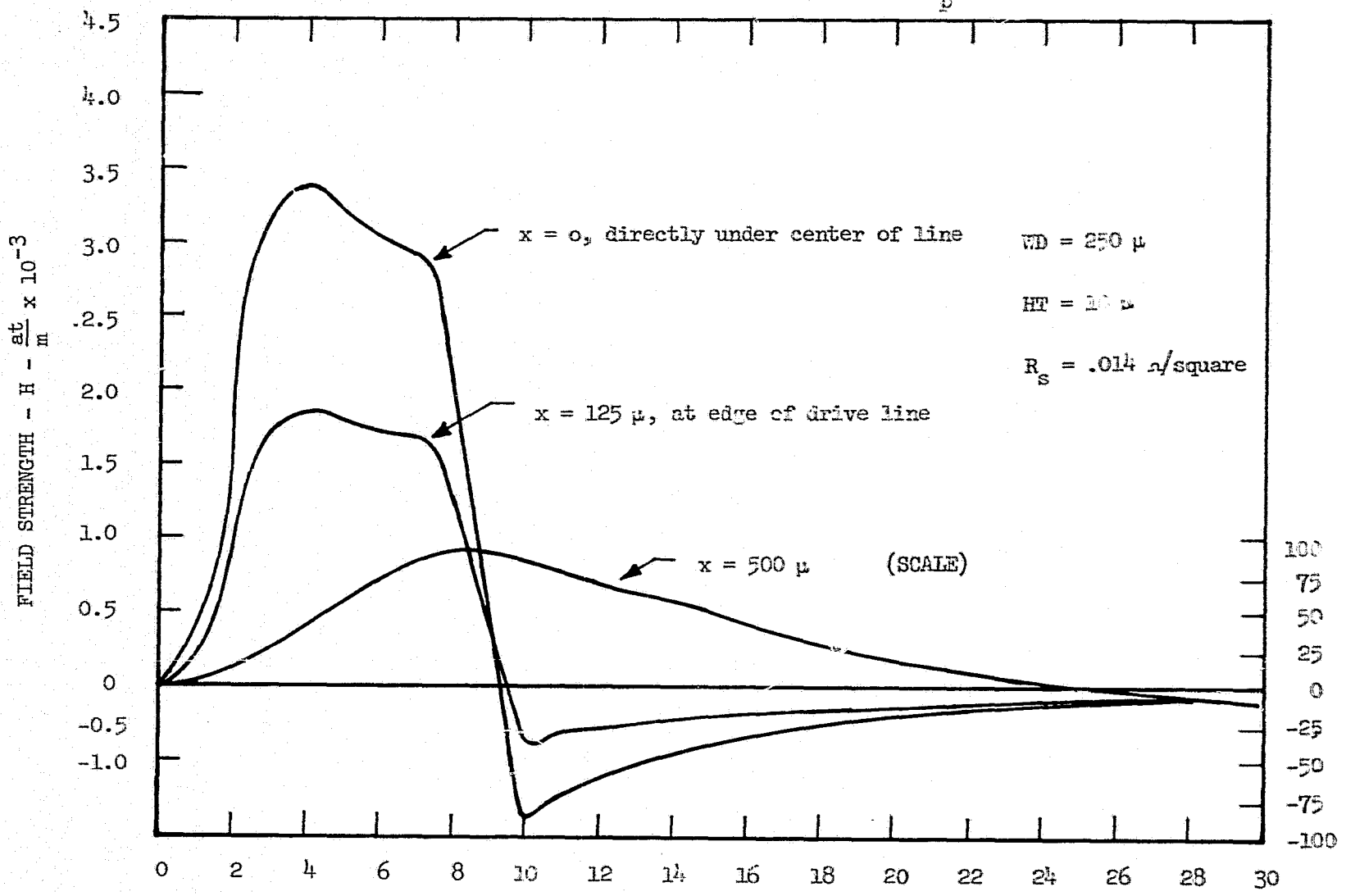


Figure 2.5 Calculated Strip Line Field at the Ground Plane for Three Horizontal Locations

decreases only about 15% over the center 80% of the strip width. Secondly, it is important to note the drastic drop in field outside the strip line. Note also the reduction in negative field. Thus, the integrated drive line structure is well suited for film memory application because of the ability to confine the fields to the vicinity directly beneath the drive lines. This is not generally true for plated wire or mylar sheet systems.

Finally, Figure 2.6 shows the effects of a leading edge peak of the applied current. This is a normal characteristic of actual drive currents, resulting from the reactive impedance of the line. Note that the peaked current provides a significant increase in field during the time when read out would occur in a memory. Thus, some overdrive is provided for the read field and a larger peak sense signal will be obtained. Of equal importance is that the field at the trailing edge of the pulse is not affected, hence the write operation is not hindered in any way by the leading edge peaking.

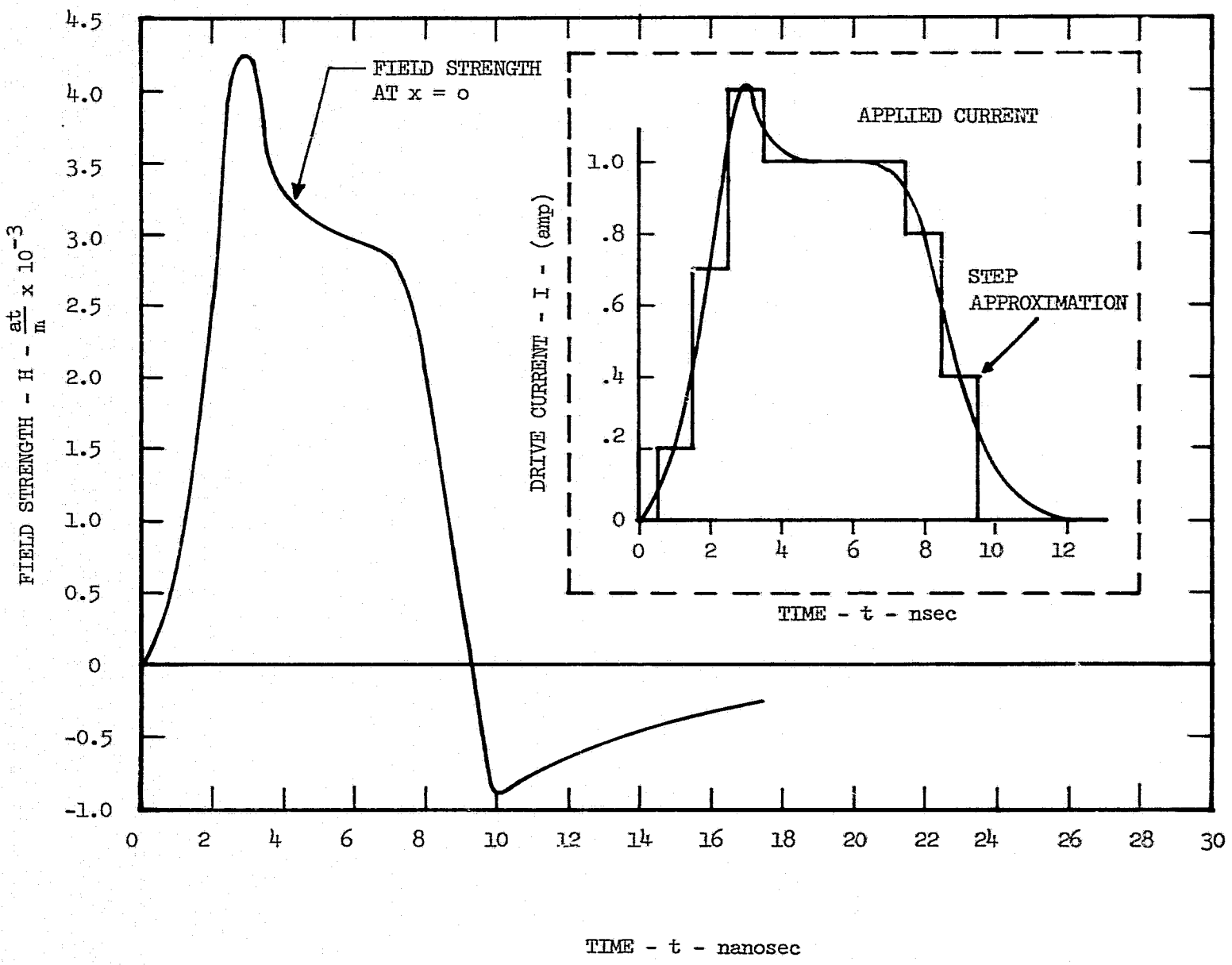
1.3 Field From Keeper Images. The previous calculations are based on fields resulting from drive line and ground plane currents only. The results are somewhat discouraging since the effective field drops so rapidly with time. Thus, where it was anticipated that the ground plane currents would create an effective field doubling it has instead been found that the time constants are so short that a 20% increase at best, occurs for practical pulse widths. It is at this point that the effect of a good magnetic keeper becomes important.

Consider now the resulting field under the strip line resulting from the sum of the drive current, ground plane currents, and magnetostatic image currents in the keeper. Recall from the derivation of keeper properties that the effect of a keeper can be taken into account by imaging every external current with one symmetrically located and of magnitude

$$I_i = \left(\frac{\mu_r - 1}{\mu_r + 1}\right) I \quad .$$

Consider a strip transmission line 250 μ wide situated $h_s = 10\ \mu$ above a ground plane of $\rho_s = 0.014$ ohm per square. In addition, we locate a keeper of $\mu = 10$ a distance $h_k = 2\ \mu$ above the strip line. Assume the dimensions are referenced to the center of the strip line thickness. If we now assume a current step is applied to the drive line a first order

EFFECT OF LEADING EDGE OVERSHOOT
ON APPLIED CURRENT PULSE



WD = 250 μ
HT = 10 μ
R_s = .014 Ω/square

Figure 2.6 Calculated Strip Line Field Showing Effect of Leading Edge Peaking on Drive Current

approximation of the resulting field can be obtained by considering the following sources:

1) Strip line alone,
2) Magnetostatic image of strip line current in the keeper,
3) Eddy current image of the strip line from the ground plane receding with velocity $v = 2\rho_s/\mu$,
4) Magnetostatic image in keeper of 3) which also recedes with velocity v.

A diagram of these is shown in Figure 2.7.

The total field as a function of time can be approximated by summing the contributions of each current source shown. The current strength in each source is:

(1) I

(2) $\left(\frac{\mu - \mu_o}{\mu + \mu_o}\right) I$

(3) $-I$

(4) $\left(\frac{\mu - \mu_o}{\mu + \mu_o}\right)(-I)$

Note that at $t \to \infty$ images (3) and (4) are at $h = \pm\infty$, respectively and contribute nothing to the resulting field. Thus, the steady state field value is given simply as

$$H_{11}(s.s.) = \frac{I}{2\pi w}\left[\tan^{-1}\left(\frac{t + \frac{w}{2}}{h_s}\right) - \tan\left(\frac{t - \frac{w}{2}}{h_s}\right)\right]$$

$$+ \frac{(\mu_r - 1)I}{(\mu_r + 1)\,2\pi w}\left[\tan^{-1}\left(\frac{t + \frac{w}{2}}{h_s + 2h_k}\right) - \tan^{-1}\left(\frac{t - \frac{w}{2}}{h_s + 2h_k}\right)\right]. \qquad (2.10)$$

Recall in the above equation t is the horizontal distance from the strip line center to where the field is to be determined. See Figure C.1. For design purposes of a memory system, one needs no more than the steady state equation. However, to illustrate the effect of the keeper more fully we have calculated the time varying field at the center of a strip line with

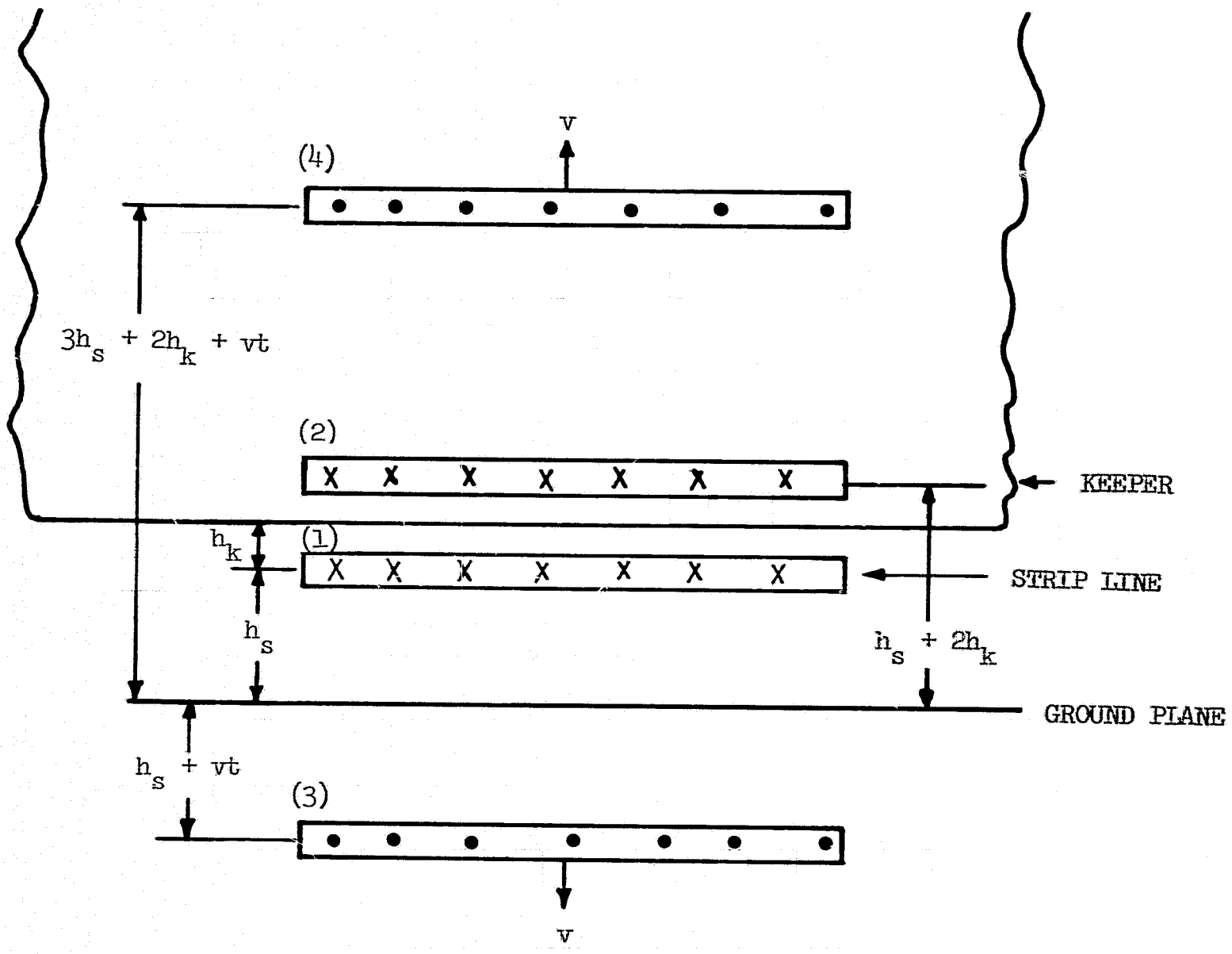


Figure 2.7 Diagram Showing First Order Field Sources in Relative Spacial Distribution

and without the keeper. This is shown in Figure 2.8. Both calculations are based on a single step of current at t = o. The geometry is a 10 mil line 10 μ above a 0.014 ohm per square ground plane. In the case where a keeper is present μ_r = 10. The keeper solution is based on the 4 image approximation of Figure 2.7. Word line to keeper separation was assumed to be 2 μ. From this it is observed that a good keeper can offset many of the limitations of a poor ground plane.

As a result the studies carried out on field efficiency as a function of line geometry we have chosen a drive line 250 μ wide with up to 12 mil line to ground plane separation. In addition, we specify a magnetic keeper with relative permeability equal to or greater than 8. While a narrower line would allow lower drive currents the stored flux would also be proportionately smaller. However, since the greatest single source of power dissipation in a memory is associated with the sense amplifiers it is desirable to keep them as simple as possible. The decision then is based on the criteria of achieving maximum stored flux and still maintaining drive currents of under 200 ma. The 200 ma limit is somewhat arbitrary but experience shows it to be a practical rule of thumb value. The dimensions chosen result in a drive system requiring approximately 150 ma for a film with H_k = 4 Oersted. Detail calculations of this will be shown in Section II-H.

2. Pulse Shape Distortion

Having studied the field efficiency aspects of an evaporated transmission line the second important consideration is the lines effect on pulse shape.

2.1 Fourier Analysis Concept. In the small memory structure to be fabricated the lines are electrically short, i.e., the delay from one end to the other is much shorter than a period of the shortest component wavelength in the pulses. Thus, a lumped circuit approximation can be used for the line parameters. Even with the simplification afforded by using lumped equivalent circuits, however, pulse analysis by hand calculation is too complicated to be practical. A Fourier analysis computer program was therefore developed which not only allowed pulse analysis of the word line system but is also used for sense line and sense amplifier design analysis. The program is completely general and can be used in any analogous pulse transmission problem.

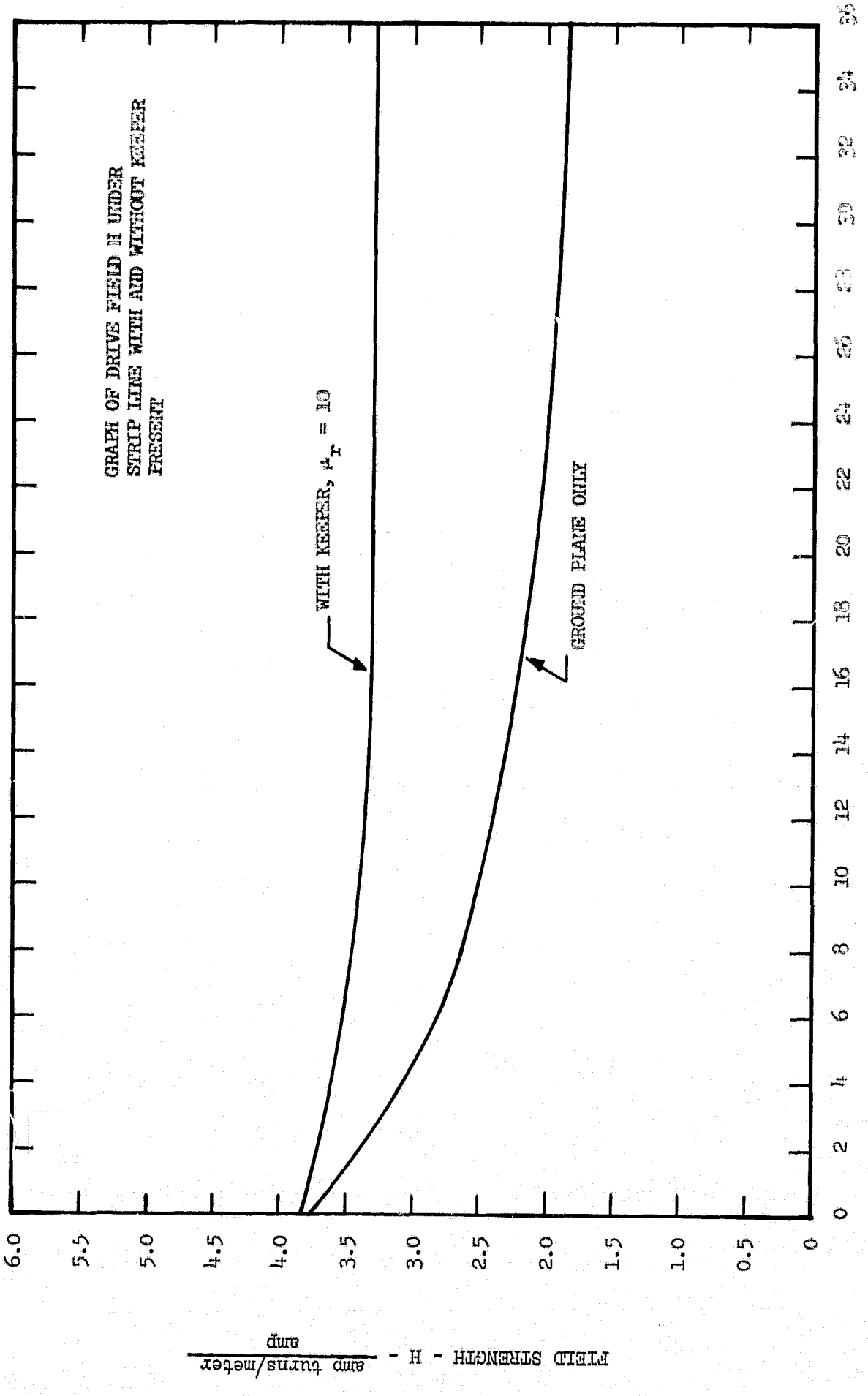


Figure 2.8 Field Directly Beneath Center of Strip Line With and Without Keeper

The concept of the analysis is that the signal under investigation is decomposed into a series of sinusoidal Fourier components. Then, knowing the gain-phase characteristics of the transmission path each component is attenuated and phase shifted accordingly. The resulting components are subsequently reassembled and the resulting waveform is the desired output signal. The information which must be given to the computer is a set of sample points on the input waveform and the gain-phase characteristics of the transmission network (transmission lines, amplifier, two port network, etc.). Appendix D gives a complete description of the operation of the program including details for coding the required information on punched cards.

2.2 Calculation of Line Parameters. For transmission line analysis it is thus necessary to calculate the gain-phase characteristic of the line. The information required for such calculations is the resistance, inductance and shunt capacitance of the transmission lines. Since the lines in an integrated film configuration are wide with respect to the separation from ground, reasonably accurate results can be obtained by neglecting fringing fields.[4] Thus the basic transmission line parameters are given as

$$C = \frac{\epsilon_o \epsilon_r w}{h} \quad \text{farad/meter} \tag{2.11}$$

$$L = \left(\frac{\mu_o h}{w} + \frac{\mu_o \mu_r \delta}{w} \right) \text{hy/meter} \tag{2.12}$$

$$R = \frac{2R_s}{w} \quad \text{ohms/meter} \tag{2.13}$$

where

w = line width in meters
h = line height above ground plane in meters
R_s = sheet resistivity of conductors
δ = thickness of any magnetic film between the line and ground
μ_r = relative permeability of magnetic film

The line and ground plane resistivities are assumed equal. Also since the

conductor thickness is less than a skin depth, even at 200 mc, the dc sheet resistivity is used.

The word line alone is assumed to be 10 mil wide located 10 μ above the ground plane. Intervening dielectric is SiO with a relative dielectric constant of approximately $\epsilon_r = 5$. Line and ground plane conductors are assumed deposited to a sheet resistivity of $R_s \approx 0.014$ ohm per square. In addition, the line is loaded with a permalloy film 800 Å thick. If $B(max) \approx 0.8$ weber/m^2 and $H_k = 320$ amp · turn/meter the relative permeability is $\mu_r = 2{,}000$.

From these data we obtain the word line parameters as

$$R = 110\ \Omega/\text{meter}$$

$$C = 9 \times 10^{-10}\ \text{farad/meter} \quad ,$$

$$L = (49.5 \times 10^{-9} + 9.4 \times 10^{-7})\ \text{hy/meter} \quad .$$

The word line in the memory system proposed is approximately 1 inch long. Thus, with a lumped parameter model the total R, L, and C, become

$$R = 2.8\ \Omega$$

$$C = 22.8 \times 10^{-12}\ \text{farad} \qquad \text{Word Line}$$

$$L = 5 \times 10^{-9}\ \text{hy} \quad .$$

Note that in the calculation for L the term corresponding to magnetic loading was multiplied by (8) · (5×10^{-4} meter) since each word line contains 8 bits each 500 μ long. A word line is thus electrically characterized by the circuit shown in Figure 2.9.

Carrying out the same type of analysis for the buss lines, i.e., the selection lines connected to the high gates, we obtain lumped element values of

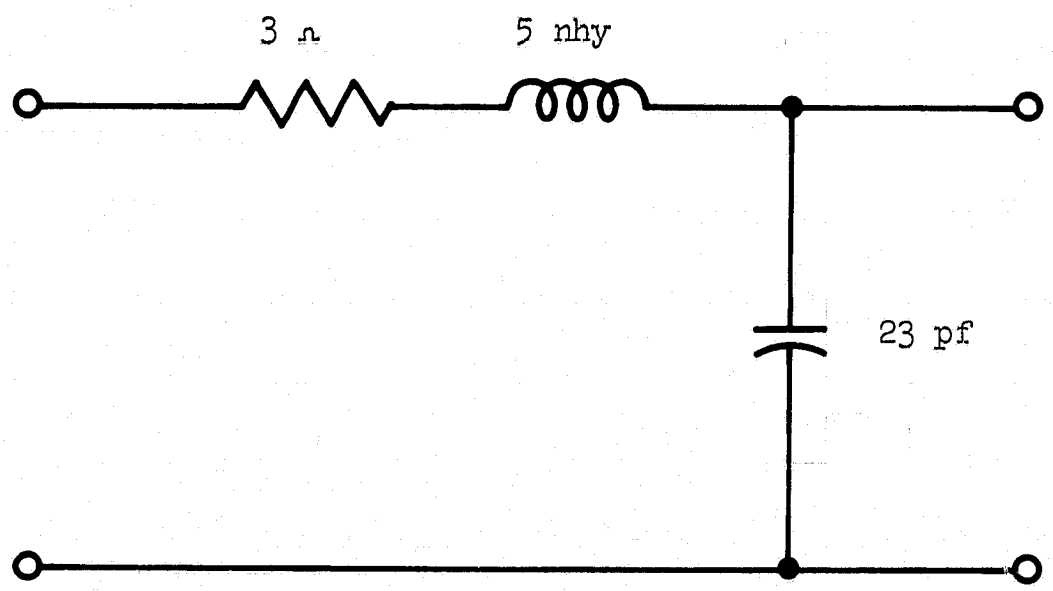


Figure 2.9 Equivalent Circuit Diagram of Word Line Over a Thin Film Ground Plane

$$R = 2\ \Omega$$

$$C = 17 \times 10^{-12} \text{ farad} \qquad \text{Buss Lines}$$

$$L = 1 \times 10^{-9} \text{ hy}$$

Here we have assumed 20 mil wide lines separated 10 μ above the ground plane. The line is approximately 4×10^{-2} meters lone.

2.3 Equivalent Circuit Pulse Analysis. It is now possible to construct a network representing the path of current flow down a selected word line in the memory. The result is shown in Figure 2.10. The 25 pf capacitor represents the effects of the remaining 7 lines connected to the buss via back biased selection diodes, plus the capacitance to ground of the high gate transistor. Each back biased diode has a capacitance of approximately 2 pf and the output capacitance of the high gate transistor is assumed to be 10 pf. The 2 ohm resistor is the buss line resistance; the inductance is considered negligible. The 17 pf capacitor represents the total buss shunt capacitance to ground. The 5 ohm resistor is the sum of the selection diode forward resistance, 2 ohm, and the 3 ohm word line resistance. We previously calculated the word line inductance as 5 n hy and this is included in the diagram. The 184 pf capacitor at the end represents the total shunt capacitance of eight word lines since each line is connected into a group of eight. Finally, the 5 ohm terminating resistor represents the saturated low gate transistor. The current I_w is the word current flowing down the word line. We want to determine the waveshape of this current. The approach to the problem will be to obtain the gain-phase characteristic, of the network of Figure 2.10, i.e., the transfer ratio

$$\frac{I_w}{E_i}(\omega) = A(\omega)\ \underline{|\theta(\omega)} \qquad (2.14)$$

Rather than calculate the above relationship for the three loop network, it was measured.

Note that direct measurement of a bread board circuit of Figure 2.10 is impractical in practice because of the small component values. However,

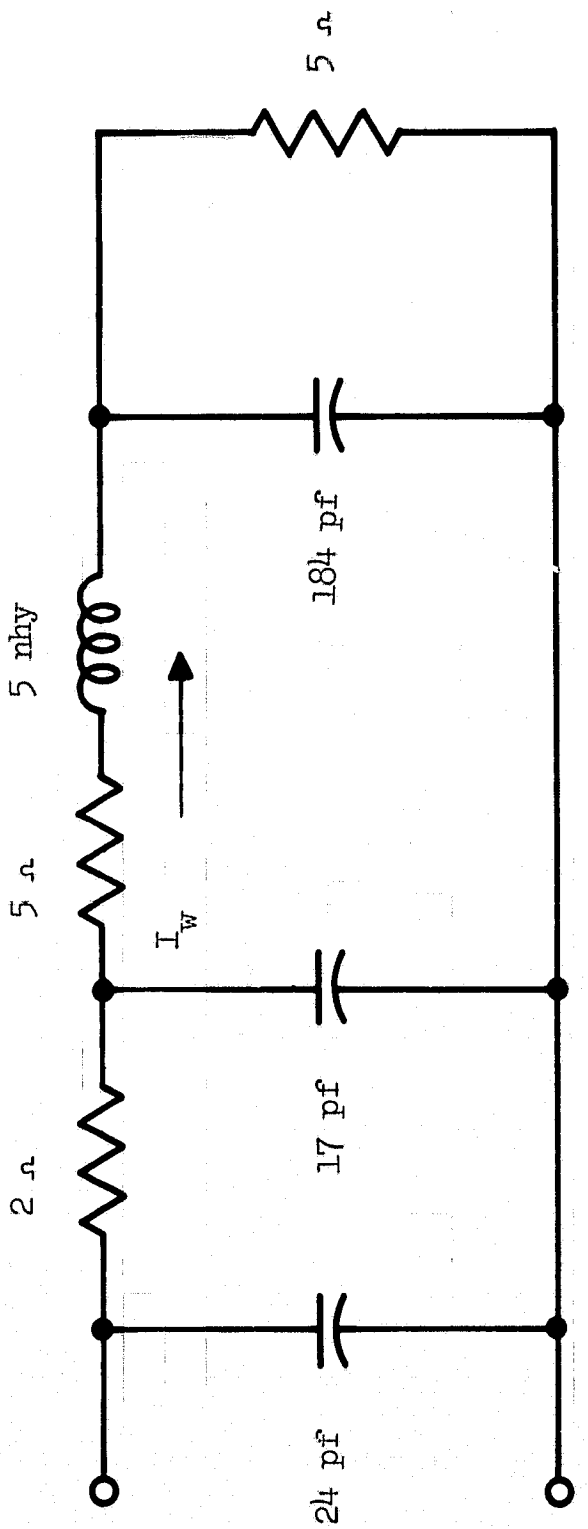


Figure 2.10 Equivalent Circuit Diagram of a Driven Word-Buss Line Path Including Parasitic Effects of Entire Array

by performing a simple frequency transformation practical values can be obtained and measurements can be performed at much lower frequencies. To take the required data we let $\omega(\text{meas}) = 10^{-3}\omega(\text{actual})$, where $\omega(\text{meas})$ is the experimental measuring frequency and $\omega(\text{actual})$ is the corresponding frequency for the actual memory. The capacitors for the bread board are then 0.024 μf, 0.017 μf and 0.184 μf and the inductor becomes 5 μ hy. The resistors are unchanged.

In the actual memory system the drive supplied to the network is essentially a step voltage through a current limiting resistance. For the gain-phase measurements a sinusoidal voltage source with a 50 Ω source impedance was used. At each frequency the current I_w was measured, both amplitude and phase, and the transfer ratio, equation (2.14) was calculated. Here E_i was the internal source voltage. The results, plotted in terms of actual frequency are shown in Figure 2.11.

Using this gain-phase data in the Fourier series program, and applying a flat top voltage pulse with 3 ns rise time the resulting current in the word line was computed. The result is shown as Figure 2.12. Note that the rise time of the current is only slightly increased. This is a result of the shunt capacitance but at worst it is now only 4 ns. There is some slight current peaking but because of the low inductance it is nearly negligible. Additionally, it is observed that the dc current level is approached within 10-12 ns. Thus, we have shown that system calculations can be made on the basis of dc impedances, for the word line, with confidence that the resulting current pulse will not be materially distorted. Note, however, that this is not generally true and each line system under study must first be analyzed in detail before such simplifying assumptions can be made.

F. ESTIMATE OF SWITCHING SIGNAL

With the knowledge that the word current rise time will be approximately 4 ns it is possible to estimate the peak sense signal to be expected. A reasonable first order approximation for the switching waveform is a sine-square function. Thus assuming

$$e_s = E_m \sin^2 \frac{\pi t}{T_s} \qquad o \leqq t \leqq T_s \qquad (2.15)$$

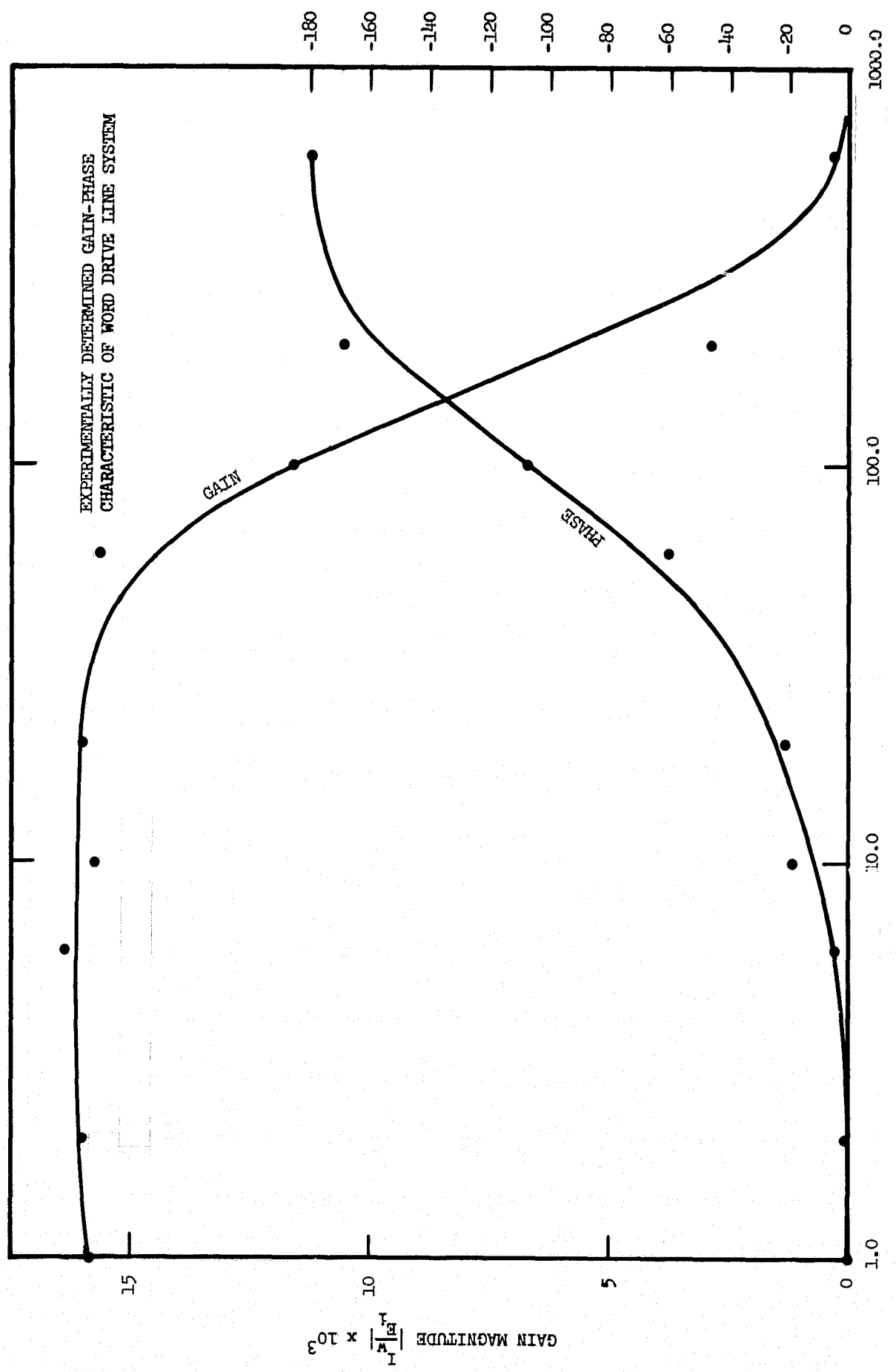


Figure 2.11 Measured Gain-Phase Data on Frequency Scaled Equivalent Circuit of Driven Word-Buss Line

OUTPUT WORD CURRENT

RESULTING FROM

ONE VOLT APPLIED PULSE @ t_r = 3 ns

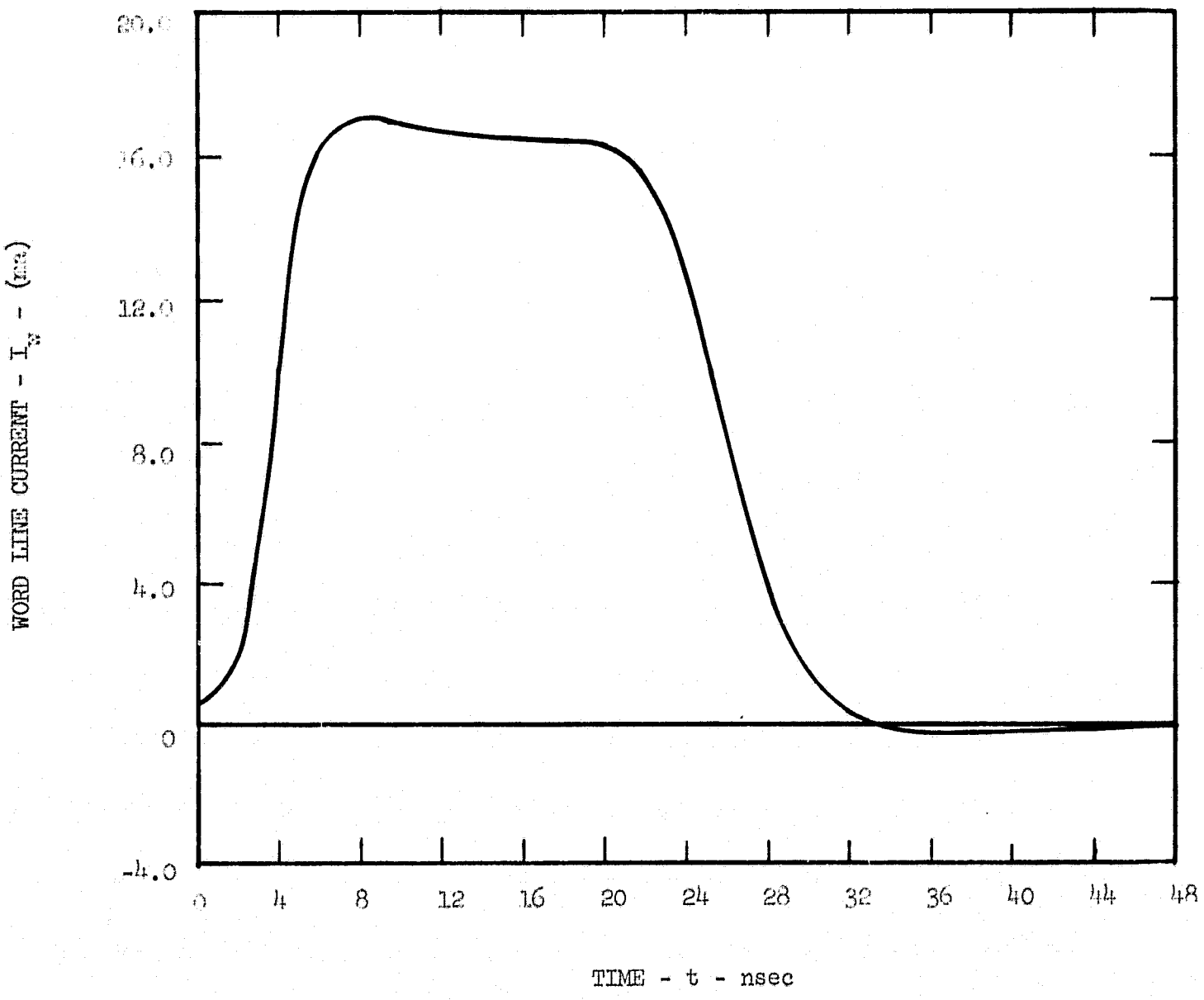


Figure 2.12 Current In Word Line for 3 ns Rise Time Applied Voltage Pulse as Calculated By Fourier Series Program

where

T_s = switching time

it is easy to show that the area under the $e_s(t)$ curve is equal to $\frac{1}{2}(E_m T_s)$. Since the area under the voltage-time curve is also equal to the total flux switched we have

$$\Phi = \tfrac{1}{2} E_m T_s \quad . \tag{2.16}$$

The film is 750 Å thick and 10 mil wide, and for permalloy $B_s \approx 0.8$ weber/m^2; thus, the total stored flux is found to be

$$\Phi_s = 15 \times 10^{-12} \text{ weber} \tag{2.17}$$

The switching time will be slightly larger than the drive current rise time because of shielding due to the intervening bit-sense line and some flux trapping in the ground plane. As a worst case estimate assume $T_s \leqq 6$ ns. Using this value for switching time we estimate the peak sense voltage to be

$$E_m \geqq 5 \text{ mv} \quad .$$

This value agrees well with actual measurements made by Reardon on thin film structures.[5]

G. BIT-SENSE LINE SYSTEM

In order to design the bit-sense line system properly it is necessary to first study the interrelationships between line parameters and:

Demagnetization of Film
Drive Current Requirement
Capacitively Coupled Noise
Distortion and Attenuation of Sense Signal.

The following paragraphs present these considerations independently and a line geometry is then specified.

1. Demagnetization Effects

Probably the greatest deterent to reducing bit-sense line width is the increasing apparent dispersion which accompanies higher demagnetizing fields. This in turn results in higher bit write fields and thus lowers the disturb threshold ratio H_c/H_B.

It was previously shown that with a keeper the demagnetizing field could easily be much less than the coercive force. Thus, no dc stability problems enter the considerations. However, the increase in effective dispersion is not insignificant. Crowther[6] has shown the relationship between demagnetizing field and dispersion to be

$$H_d = H_k(\sin \alpha' - \sin \alpha_o) \qquad (2.18)$$

where

α' = effective dispersion which must be overcome to store information

α_o = intrinsic dispersion in the absence of demagnetizing fields

Since the bit field required during the write operation is

$$H_B = H_k \sin \alpha' \qquad (2.19)$$

we see then that

$$H_B = H_k \sin \alpha_o + H_d \quad . \qquad (2.20)$$

It is therefore necessary to deliver an "excess" bit field equal to the demagnetizing field.

Thus, for an eighty percent efficient keeper, i.e., $\mu_r \approx 10$, the required bit field for 10 mil and 20 mil lines can be found using the demagnetizing fields calculated in the section on film properties. We

assume H_K = 4 Oersted and $(\alpha_o + \beta) = 3°$. Then

$$H_k \sin \alpha_o = 0.21 \text{ Oersted}$$

and

$$H_B(10 \text{ mil}) = 0.57 + 0.21 = 0.78 \text{ Oersted}$$

and

$$H_B(20 \text{ mil}) = 0.2 + 0.21 = 0.41 \text{ Oersted} \quad .$$

The respective H_c/H_B ratios, which indicate creep stability, are

$$(H_c/H_B)_{10 \text{ mil}} = 2.56$$

$$(H_c/H_B)_{20 \text{ mil}} = 4.9$$

assuming a film with H_c = 2 Oersted. Thus, the 20 mil wide line provides for much greater stability of the stored state.

2. Drive Field Considerations

We have previously developed the expressions for field-current relationships of integrated film transmission lines. For a line with a perfect keeper, the maximum field attainable is simply

$$H_{max} = \frac{I}{W} \text{ amp/meter} \quad . \qquad (2.21)$$

Using the previously derived values of required bit field the minimum possible bit currents for 10 mil and 20 mil lines would be

$$I_b \text{ (10 mil)} = 15.5 \text{ ma}$$

and

$$I_B \text{ (20 mil)} = 16.4 \text{ ma} \quad .$$

Therefore, the reduction in bit current is negligible for the narrow line. In fact, for a given height above the ground plane the efficiency of a narrow line is somewhat less, thus tending to equalize the actual currents required.

3. Induced Noise Configurations

One of the major problems in any memory system is noise on the sense line induced by capacitive and inductive coupling to the word drive line. In a word organized memory, the orthogonality of the word line and bit-sense line eliminates any significant inductive coupling. However, in an intetrated film system capacitive coupling is relatively large.

Using a lumped parameter model for the lines involved it is easy to see the effect of line to line and line to ground separations. Consider a word line crossing a single sense line as shown in Figure 2.13a. Figure 2.13b shows the equivalent circuit of the noise producing components. The voltage source represents the voltage rise of the word line as word current is transmitted. The output terminals represent the voltage between a single sense line and ground.

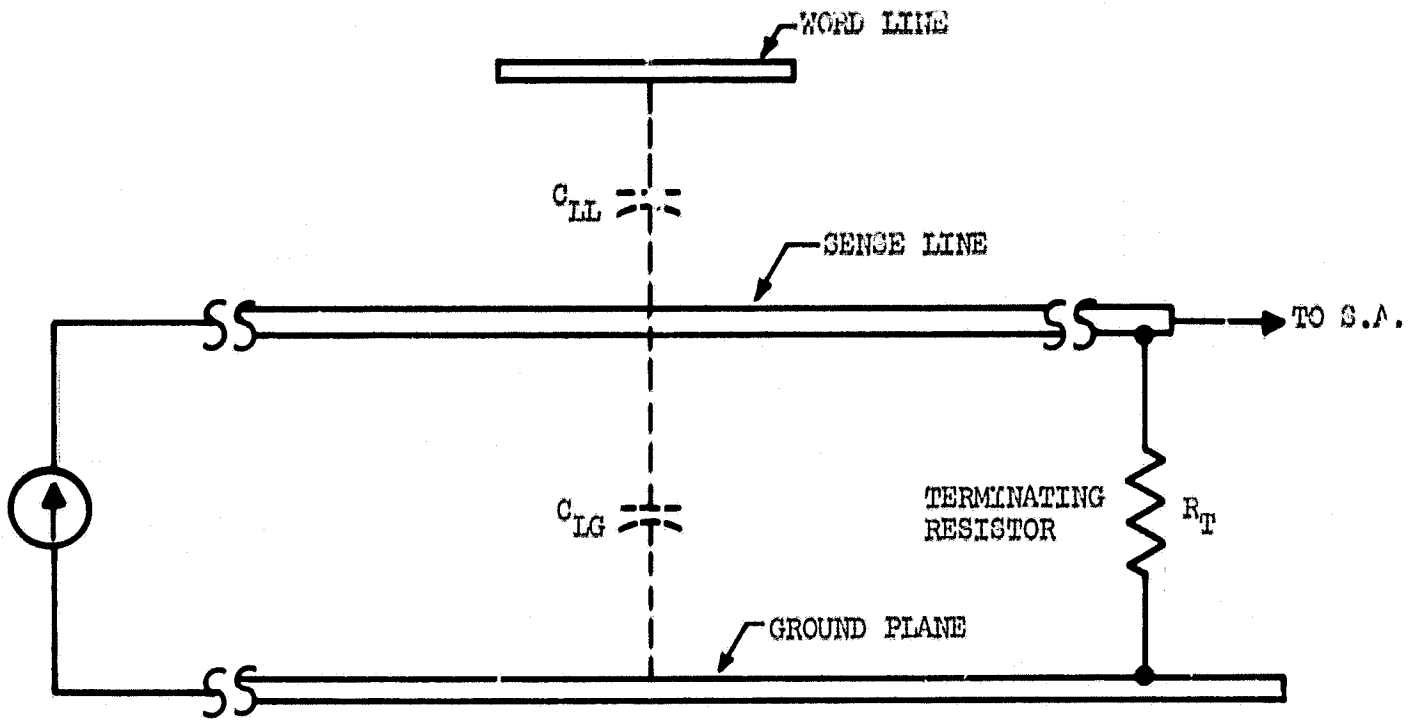
The Laplace transform of the noise voltage is found to be

$$E_o(s) = \frac{E_i(s)\, S \left(\frac{C_{LL}}{C_{LG}}\right)}{\left(1 + \frac{C_{LL}}{C_{LG}}\right)\left[S + \frac{1}{RC_{LG}\left(1 + \frac{C_{LL}}{C_{LG}}\right)}\right]} \quad . \qquad (2.22)$$

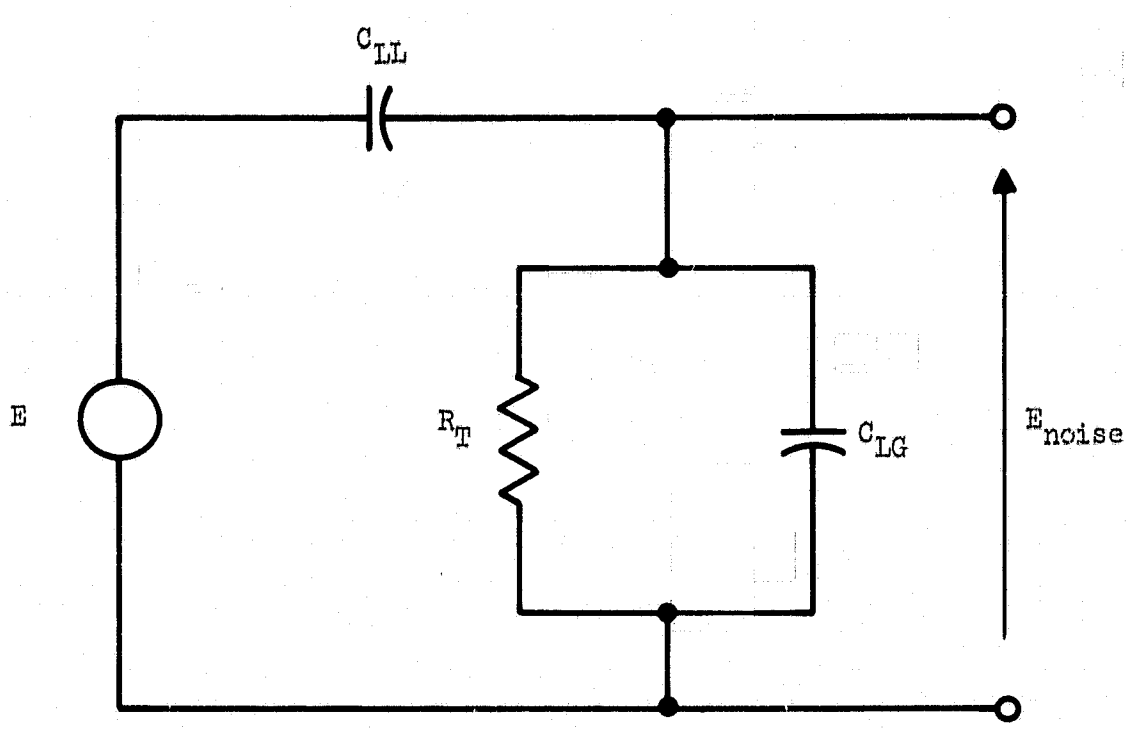
For a word line voltage which rises approximately linearly such that

$$E = Kt \qquad o \leqq t < T_r$$

$$E = KT_r \qquad T_r \leqq t \quad ,$$



(a)



(b)

Figure 2.13 Capacitive Noise Coupling
(a) Physical Geometry
(b) Equivalent Electrical Circuit

the noise voltage peak becomes

$$e_{noise}\ (peak) = KR_T C_{LL}\ (1 - e^{-\frac{T_r}{\tau}}) \qquad (2.23)$$

where

$$\tau = RC_{LG}\ (1 + \frac{C_{LL}}{C_{LG}}) \quad . \qquad (2.24)$$

It is apparent, therefore, that to minimize noise the line to line capacitance C_{LL} should be as small as possible and the sense line to ground capacitance should be as large as possible. In terms of physical separation we should evaporate the sense line close to ground and provide thick insulation between sense and word lines. Fabrication problems govern what minimum and maximum thickness of dielectrics are practical to consider. Experience has shown that 3 to 4 μ is probably a minimum thickness to assure no shorts occur.

To appreciate the size of the noise voltage consider a sense line 20 mil wide located 4 μ above ground. The word line will be 10 mil wide separated from the top of the sense line by 4 μ. In this memory the bit-sense line is about 4.4×10^{-2} meters long. The insulation is SiO with $\epsilon_r \approx 5$. With these dimensions we obtain

$$C_{LL} = 1.4 \text{ pf}$$

and

$$C_{LG} = 242 \text{ pf} \ .$$

If the word line voltage rises 2 volts in 4 ns, then $K = 5 \times 10^8$. For a sense line terminating resistor of 10 ohms the peak noise voltage is then calculated to be

$$e_{noise}\ (peak) \approx 6 \text{ mv; (20 mil sense line)}.$$

For a 10 mil wide sense line, other dimensions being held constant, the induced noise is reduced to approximately 3.5 mv. In either case, the signal is approximately equal to the expected sense signal. This shows the necessity for the balanced sense line incorporated in the memory. With the balanced line the noise is coupled into each half and hence is rejected with a differential sense amplifier.

From a system point of view then we would like to have line to line separations around 4 μ or larger, yet not so large as to reduce field generation efficiency. With a balanced sense line the width is not a critical factor; however, if one considers a single bit-sense line system a narrow line is desirable.

4. Frequency Response

Design of the sense line must also take into account attenuation of the induced sense signal. Since the lines are thin the resistance is relatively high and the close spacing to ground creates large values of shunt capacitance. This results in high attenuation per unit length. In general then we desire a wide line to minimize resistance and inductance and large separation to reduce shunt capacitance. Actual evaluation of pulse degradation, however, can best be done with computer analysis. During this contractural effort both the Fourier digital program and an analog computer approach were used to obtain this information. It has been found possible to generalize the results in terms of the effective 3 db frequency associated with the sense line. This is illustrated in the following paragraphs.

4.1 Sense Line Equivalent Network. The worst case situation for attenuation is where maximum line length separates the induced voltage and the sense amplifier terminals. Thus for the following analysis we assume a bit switches at the exact center of the balanced sense line. Due to the symmetry of the line structure, and the location of the assumed induced voltage, the equivalent circuit is as shown in Figure 2.14. The elements shown represent total line parameters as previously discussed in connection with the word line. Thus R_1 and R_2 are the total sense line plus ground plane resistance of one leg of the U shaped line. The same holds for L_1 and L_2, and C_1 and C_2. R_T is the sense line terminating resistor.

Due to the geometry of the lines the inductive reactance at all frequencies of interest is negligible compared to the series resistance. It is therefore possible to characterize each leg as a simple R-C low pass

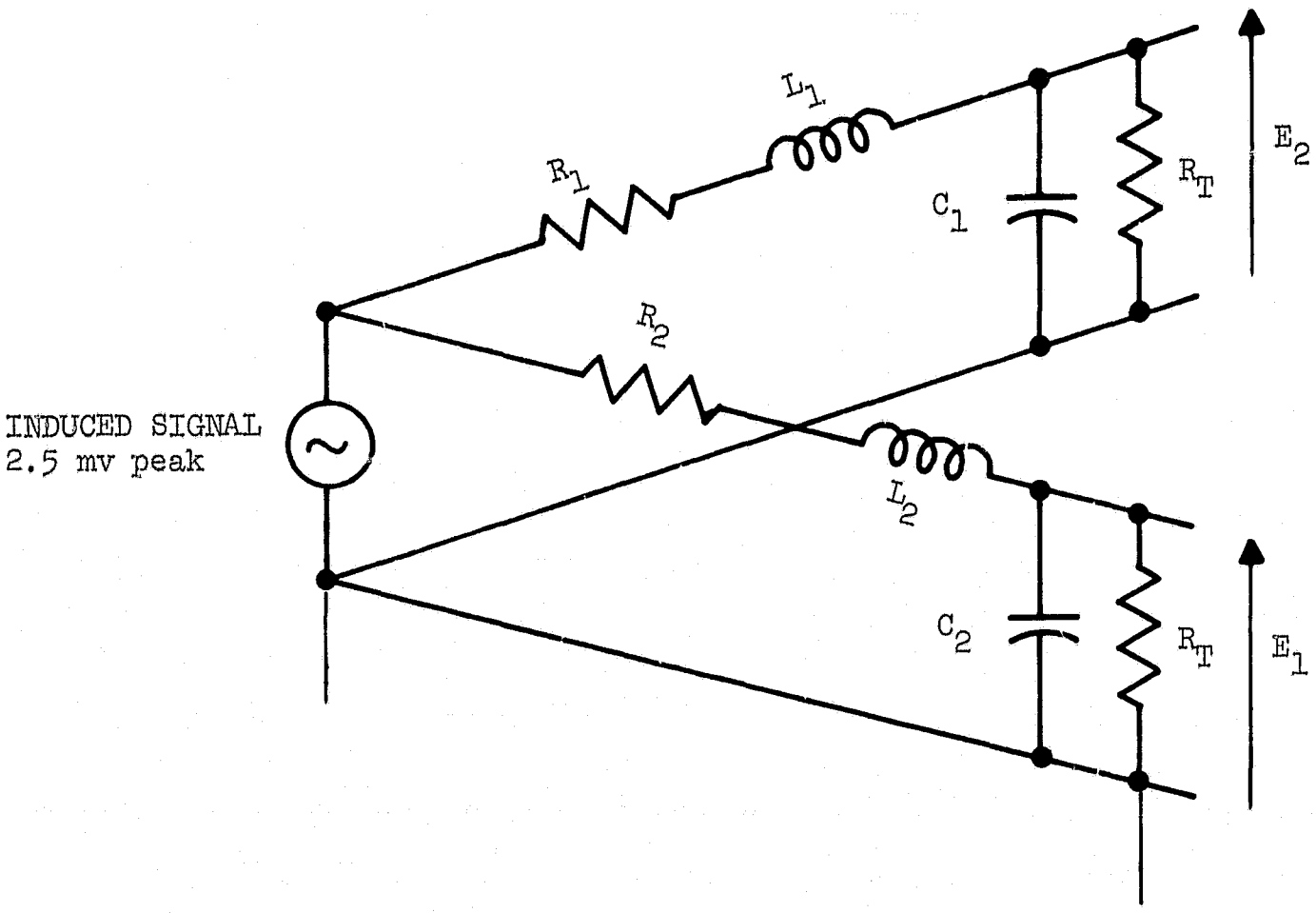


Figure 2.14 Equivalent Circuit of Worst Case Sense Line System

filter where the 3 db frequency is given simply as

$$f_c = \frac{1}{2\pi RC_1}$$

where

$$R = \frac{R_1 R_T}{R_1 + R_T}$$

4.2 Computer Analysis. Using the gain-phase data for this type of network the Fourier series program can be used to determine the pulse distortion of the sense line. For this analysis we have used a switching waveform representative of an actual film output.

Figure 2.15 shows the differential output signal for a 50 mc line, i.e., f_c = 50 mc, with a 5 mv peak switching voltage induced at the far end. Note the large attenuation in peak signal and the broadening effects resulting from the limited bandwidth of the transmission line. Taking this type of data for lines of different bandwidths we can plot graphs of attenuation and peak time delay as a function of f_c. This data is shown in Figure 2.16. The upper curve of Figure 2.16 shows a plot of the ratio of sense line output peak voltage to switching peak voltage. Note that even with a 100 mc bandwidth line the signal is attenuated by a factor of two. It is seen here that very high bandwidths are required to obtain low peak attenuations.

The line parameters for a bit-sense line 4 μ above the ground plane and deposited to a sheet resistivity of 0.014 ohm/square are:

10 mil line:

$R = 110$ ohm/meter

$C = 2.25 \times 10^{-9}$ farad/meter

20 mil line:

$R = 55$ ohm/meter

$C = 5.5 \times 10^{-9}$ farad/meter

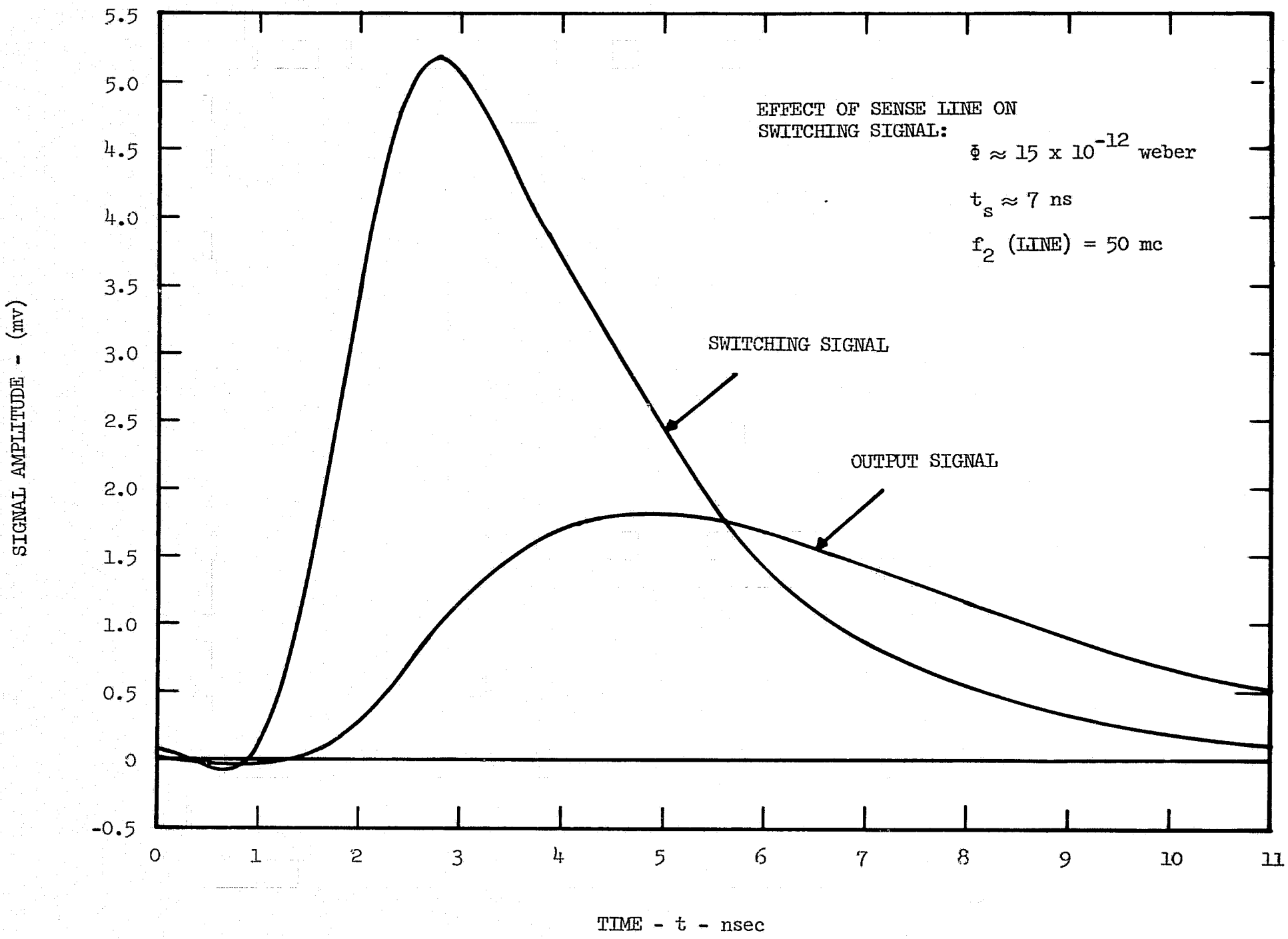
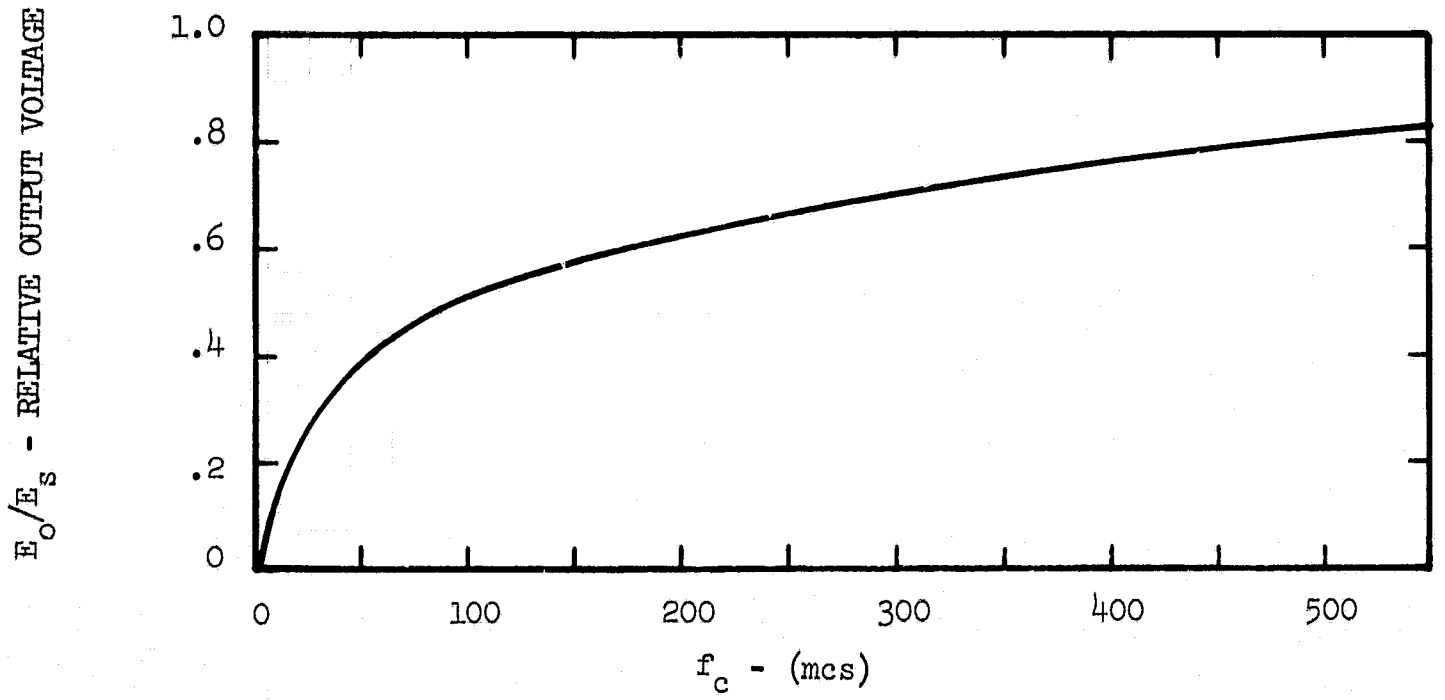


Figure 2.15 Signal at Terminals of 50 MHz Bandwidth Sense Line for 5 mv Peak Switching

GRAPHS SHOWING CALCULATED SIGNAL ATTENUATION
AND DELAY AS A FUNCTION OF SENSE LINE BANDWIDTH



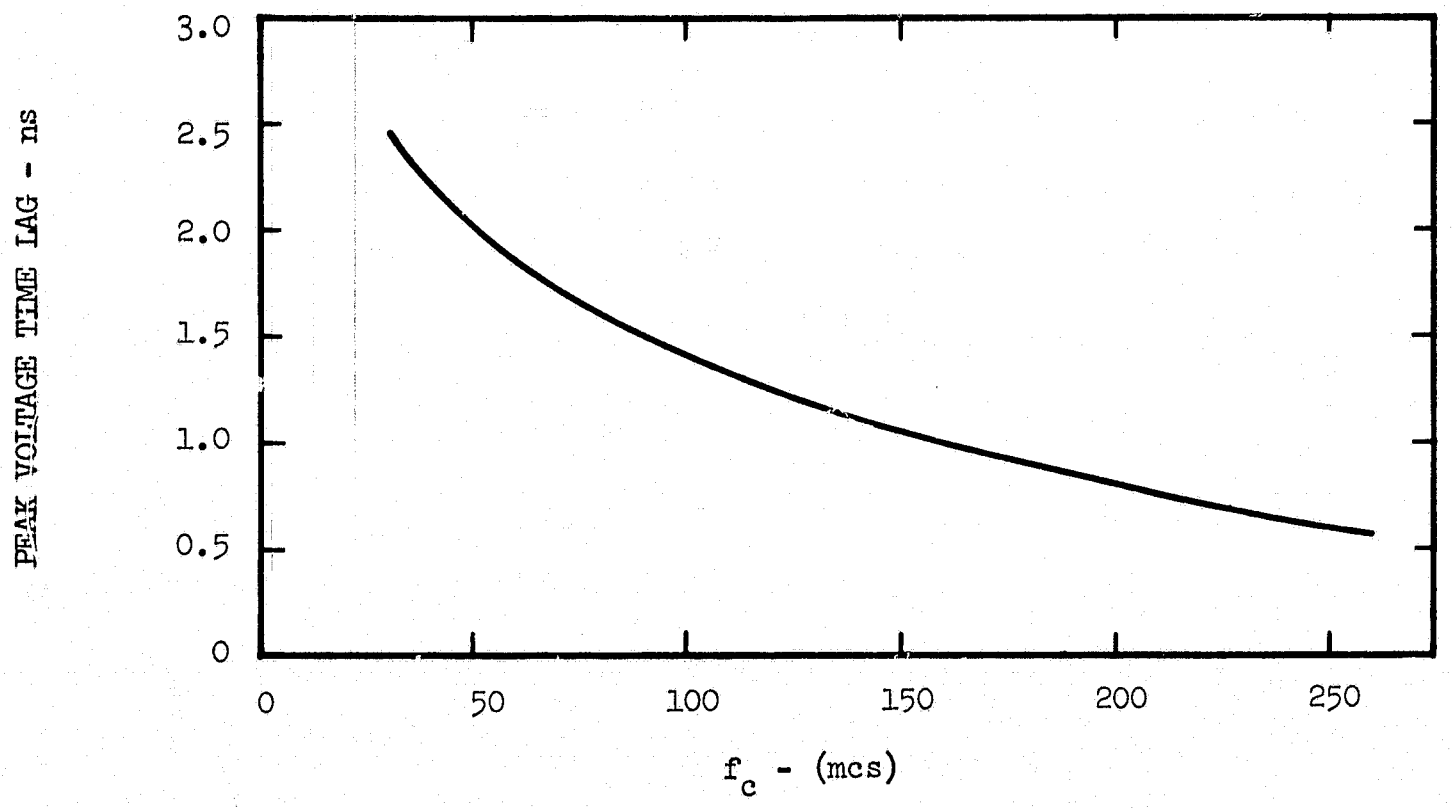


Figure 2.16 Attenuation and Delay Characteristics of Sense Line System as a Function of Line Bandwidth

For the 4.4×10^{-2} meter bit-sense line of this memory and a 10 ohm termination resistor the bandwidths of 10 mil and 20 mil lines are found to be

$$f_c \text{ (10 mil)} = 485 \text{ mc}$$

$$f_c \text{ (20 mil)} = 400 \text{ mc}$$

In either case the bandwidth of the line is sufficiently large that terminal voltages should be approximately 80% of the switching signal.

5. Conclusion

The bit-sense line design problem has been analyzed considering four prime limiting effects. These are:

1) Demagnetization
2) Drive Current Requirements
3) Capacitively Coupled Noise
4) Pulse Distortion .

Demagnetization considerations provide a strong impetus to choose wide bit-sense lines. The other three areas produce a tendency to go to narrower lines but the benefits gained are minor. Since creep has been such a significant problem in magnetic film memories in the past, achieving maximum stability by system design is of the greatest importance. For this reason 20 mil wide bit-sense lines have been selected for use in this memory.

H. SYSTEM DESIGN PARAMETERS

In this final section on system design the decisions of the previous sections are brought together and the predicted characteristics of the array are calculated.

1. Array System Specifications

Planar Line Dimensions

Word Lines -- 10 mil wide on 20 mil centers

Bit-Sense Lines -- 20 mil wide on 30 mil centers

Bit line pairs are therefore 50 mil wide on 60 mil centers.

Vertical Dimensions (Referenced to Ground Plane)

Bit Sense Line -- 4 μ

Word Line -- 10 μ

Keeper Surface -- 12 μ

These dimensions assume insulation layers of 4 μ and conductor thickness of 2 μ.

Film Characteristics

$H_k \leqq 4$ Oersted

$H_c = 2$ Oersted

$(\alpha_{90} + \beta) \leqq 3^\circ$

Thickness 750 Å

Keeper Characteristics

$\mu_r \geqq 8$ for $o \leqq f \leqq 200$ mc

2. Predicted Characteristics

From the previous specifications the following system characteristics are calculated.

Stored Flux

$$\Phi_s = 15 \times 10^{-12} \text{ weber}$$

Flux Linking Sense Line

$$\Phi = \frac{15 \times 10^{-12}}{2} \left[1 + \frac{(8 - 1)}{(8 + 1)}\right] = 13.3 \times 10^{-12} \text{ weber}$$

Peak Induced Switching Voltage

$$E(\max) = \frac{2\Phi}{T_s} = 4.4 \text{ mv for } T_s = 6 \text{ nsec} .$$

Peak Output Voltage of Sense Line

$$E_o = 0.8\, E_{(\max)} = 3.5 \text{ mv}$$

This is for sense line bandwidth of 400 mc.

Word Line Efficiency (H/I)

We calculate only the field directly beneath the center of the line, i.e., $\ell = 0$.

$$\frac{H_w}{I} = \frac{1}{\pi w}\left[\tan^{-1}\left(\frac{w}{w \cdot h_s}\right) + \frac{\mu_r - 1}{\mu_r + 1} \cdot \tan^{-1}\left(\frac{w}{2(h_s + 2h_k)}\right)\right]$$

where

$w = 250\ \mu$

$h_s = 10\ \mu$

$h_k = 2\ \mu$

$\mu_r = 8$

$$\frac{H_w}{I} = 3.3 \times 10^3 \frac{\text{at/m}}{\text{amp}}$$

Bit Line Efficiency

Using the same equation as for the word line efficiency but with

$w = 500\ \mu$

$h_s = 4\ \mu$

$h_k = 8\ \mu$

$\mu_r = 8$

$$\frac{H_B}{I} = 1.73 \times 10^3 \frac{\text{at/m}}{\text{amp}}$$

Required Word Field

$$H_w = H_k + H_{S.A.}$$

where

$H_{S.A.}$ = Shape Anisotropy Field .

From Appendix I

$$H_{S.A.}\ \text{(No Keeper)} = (A_b - A_a)\left(\frac{c}{b} 4\pi M\right)\ \text{Oersted}$$

and with

$a = 500\ \mu$

$b = 250\ \mu$

$c = 750$ Å

$4\pi M = 8{,}000$ gauss

$$H_{S.A.} \text{ (No Keeper)} = 1.5 \text{ Oersted} .$$

With the keeper the total required word field becomes:

$$H_w = 4 + 1.5 \left[1 - \frac{\mu_r - 1}{\mu_r + 1} \right] = 4.33 \text{ Oersted}$$

or

$$H_w = 346 \text{ a.t/m} .$$

Required Bit Field

$$H_B = H_k \sin (\alpha_o + \beta) + H_d$$

where

H_d is the easy axis demagnetizing field. From Appendix I, using the film parameters listed in the previous calculation we find

$$H_d \text{ (No Keeper)} = A_a \ (4\pi M_s) \text{ Oersted}$$

and since $A_a = 0.32$

$$H_d \text{ (No Keeper)} = 0.77 \text{ Oersted} .$$

With the keeper then, the required bit field is

$$H_B = 4 \sin(3^\circ) + 0.77 \left[1 - \left(\frac{8 - 1}{8 + 1} \right) \right] ,$$

$$H_B \approx 0.4 \text{ Oersted} = 32 \frac{\text{at}}{\text{m}} .$$

From the line efficiencies calculated and the drive fields estimated

the minimum required word and bit drive currents can be determined. These are found to be:

Required Word Current

$$I_W = \frac{346}{3.3 \times 10^3} = 105 \times 10^{-3} \text{ amp}$$

Required Bit Current

$$I_B = \frac{32}{1.73 \times 10^3} = 18.5 \times 10^{-3} \text{ amp/line}$$

Since the bit generator must also supply current down the balance line the total current required is:

$$I_B(\text{total}) = 37 \text{ ma}$$

Realizing that these are minimum currents the driver circuits for the system should be capable of delivering 150 ma of word current and approximately 60 ma of bit current. These magnitudes are within the present state of the art of monolithic integrated circuits.

I. CONCLUSIONS

In this section on system design, the significant design parameters have been discussed and general approaches to the required analysis have been illustrated. The results demonstrate that a thin film memory compatible with integrated circuit drivers is feasible. The features of high density, nearly ideal transmission line characteristics, and high reliability are inherent in the approach. It seems likely that systems of this type will find applications in a variety of space missions in the future.

III. KEEPER FABRICATION AND ANALYSIS

A. INTRODUCTION

The feasibility of operating a high density, low power magnetic film memory depends upon utilization of a keeper. The keeper consists of a relatively thick plane of high permeability material adjacent to the plane of the magnetic bits and drive lines.

One of the purposes of the keeper is to provide a flux closure path for the magnetic bits. This path reduces the demagnitization or stray field of the bit, thereby increasing the bit stability and reducing interference between bits. The keeper also causes more of the external flux to close about the bit-sense line thereby increasing the output efficiency.

Another major beneficial effect is to provide enhancement of the drive currents by the magnetic image of the drive currents. This image also reduces the stray field interference of the drive currents.

In order to perform these essential functionsit is necessary that the keeper have reasonable permeability, low electrical conductivity and losses, and retain these parameters from static conditions up to frequencies commensurate with the memory cycling time. In addition, it is necessary to assure that a close proximity of keeper to memory plane is achieved without damage to the memory and that adhesion and dimensional stability be sufficient to maintain good contact between the surfaces.

B. FABRICATION

Commercially available ferrites have many of the properties desired for a keeper. However, the difficulty with using these materials in their bulk, sintered form is manifold. Ferrites do not have linear frequency characteristics or a linear magnetization curve. They also have considerable remanence and consequently, high losses at large fields. They are also hard and abrasive and cannot be machined with ease to fit closely and mate well with the surface of the memory plane without the danger of scratching or puncturing the memory structure. Ferrite powders in some form of binder have been used with success in keeper applications.[7]

Three samples of ferrite powder were obtained from the Indiana General Corporation in Keasbey, New Jersey. Their designations and descriptions

of the materials in bulk form are as follows:

Type	Initial Perm.	at Freq.	Max. Freq.
T-1	2000	100 kHz	400 kHz
H	850	1 MHz	1 MHz
Q-2	40	1 MHz	50 MHz

As received, all powders were screened to -60 mesh (250 μ). However, the H and Q-2 powders appeared to be much finer than the T-1. The T-1 powder was the most dense, about 3.10 gm/cm^3, and also had the highest permeability in powder form as well as in bulk. Due to the higher permeability, the T-1 powder was used extensively to the exclusion of the other two.

Three binder materials were investigated. All three were supplied by the Dow Corning Corporation and are designated as follows:

RTV 3110	Silicone Rubber	Low Viscosity
RTV 3120	Silicone Rubber	High Viscosity
Sylgard 184	Silicone Resin	Low Viscosity

Associated with each is a particular curing and thinning agent. Working time of the RTV rubbers can be adjusted from a few minutes to several hours by the selection of proper amounts and types of curing agents. The addition of thinning agents generally increased curing time and reduced mechanical properties.

Test samples for determining the permeability were made by molding a mixture of RTV 3120 and T-1 powder. A toroidal mold with a rectangular cross-section was used. This configuration was used to correspond with the form used to measure inductance on the loose powders. The mold was machined from brass. No release agents were used when molding the samples.

The density of the powder within the sample was determined from the mix ratios and the final weight and size of the finished test sample. Four powder-bearing toroids were made with powder densities as follows:

(1) 1.15 gm/cm^3
(2) 1.43 gm/cm^3
(3) 1.94 gm/cm^3
(4) 2.36 gm/cm^3

Torroid No. 5 was fabricated as a standard and contained no ferrite.

A sixth toroid was constructed using a different method. Ferrite powder was packed lightly in the mold and a thinned mixture of Sylgard 184 was poured over the powder. The resin, however, did not completely penetrate the mold and only about two thirds of the sample could be removed intact. Thin sections of keeper were also fabricated by the same method. However, the resin tended to channel through the powder and create a non-uniform structure. Keeper sheets were also made by mixing powder and rubber as in the electrical samples, and pressing the mixture between microscope slides. The mixed material was difficult to remove from the glass slides, and later teflon blocks were used to reduce sticking; however, this was still unsatisfactory. Keepers were made from Sylgard 184 with and without 10% thinner and also RTV 3110 with and without thinner. The T-1 powder was dry-sieved through a 320 mesh screen (50 μ) for the keeper so that the particle size would be small with respect to the bits and lines.

The final process evolved from the trials consisted of mixing the ingredients under vacuum. The vacuum typically measured about 29 in. Hg. After mixing, the paste was pressed into sheets between two teflon blocks also under the same vacuum. One side of the sheet was cast very smooth by placing a sheet of 0.001 in. stainless steel foil against one of the blocks. The keeper was allowed to cure in atmospheric pressure at about 40° C for 12 hours or longer. The mixture decided upon for the final material was a compromise between high density and ease of mixing in the vacuum. The ratios by weight were: 5 parts T-1 powder, 1 part RTV 3110, 0.1 part thinner, and 0.1 part standard curing agent.

The test samples No. 2 and No. 4 were examined after testing by sectioning. Both were found to have a great number of air bubbles. It is not unlikely that the rest were similar to these. In order to successfully eliminate these bubbles in the thin keeper, it was necessary to mix under vacuum and cure at atmospheric pressure. This was not done with the samples. Keepers made by vacuum mixing had a higher density than the test samples and showed no evidence of air holes.

The mixing process consists of placing the ingredients in a cup which is cemented to the bottom of the vacuum chamber. The vacuum is slowly applied to prevent boil-over of the liquid. The vacuum is held for about 30 minutes, then the ingredients are mixed. The mixture is then removed

from the chamber and placed on the stainless foil. The foil is placed between the teflon blocks and the press is put back in the vacuum chamber. The vacuum is applied for about 15 minutes, then the blocks are pressed together to form the sheet. The sheet is allowed to cure as stated above while the blocks remain over it.

The purpose of the stainless foil is to form a very smooth surface to place against the memory plane. It is also necessary to provide a flexible form which could be easily peeled away from the keeper without damaging the surface. Both the RTV and the Sylgard adhere strongly to most surfaces and it is impossible to break apart a large surface at one time without damage to the keeper.

The resulting sheet was then cut to the desired size and pressed gently over the memory plane. This pressure is sufficient to cause a slight adherence of the keeper to the memory and when removed some days later, the keeper face clearly showed the impression of the memory plane face. This indicates that the keeper flows slightly on prolonged contact with an uneven surface. This flow is fortunate in that it improves the closeness of contact essential to good keeper performance.

C. PERMEABILITY MEASUREMENTS

1. Inductance Technique

The first series of electrical measurements to determine the permeability of the ferrite powders involved measurements of inductance of a toroid of rectangular cross-section. The powder was contained in a plexiglas form which had the windings fixed to it. The relationship of the measured inductance to the permeability can be computed if one considers the toroid to be a long narrow solenoid bent around upon itself. The flux density of such a solenoid is given by

$$B = \mu NI/l$$

For the toroid, the length l is given by the average circumference of the toroid which is $2\pi(r_i + r_o)/2$. The total flux in the toroid is given by $\Phi = BA$ where $A = (r_o - r_i)t$. The inductance is the number of flux linkages

divided by the current or

$$L = \frac{\mu N^2 (r_o - r_i) t}{\pi (r_o + r_i)} \quad . \tag{3.1}$$

The above solved for μ_r gives

$$\mu_r = \frac{\pi L (r_o + r_i)}{\mu_o N_2 (r_o - r_i) t} \quad . \tag{3.2}$$

A similar calculation using slightly altered assumptions yields a similar result and has the advantage that it may be applied to the later measurements directly. One may assume that the toroid behaves as though a single wire carrying a current of NI passes through the center and that the flux in the toroid is a function of the radius from the wire only. Then, by using Ampere's Law

$$\oint \vec{H} \cdot \vec{dl} = NI \quad .$$

The left side = $2\pi r H$, therefore

$$B = \frac{\mu NI}{2\pi r} \quad . \tag{3.3}$$

The total flux within the toroid is then easily computed as

$$\Phi = \frac{\mu NIt}{2\pi} \int_{r_i}^{r_o} \frac{1}{r} \, dr = \frac{\mu NIt}{2\pi} \ln r_o/r_i \quad . \tag{3.4}$$

The expression for L then becomes

$$L = \frac{N\Phi}{I} = \frac{\mu N^2 t \ln r_o/r_i}{2\pi} \tag{3.5}$$

and solving for μ gives

$$\mu_r = \frac{2\pi L}{\mu_o N^2 t \ln (r_o/r_i)} \quad . \tag{3.6}$$

Thus under these assumptions μ_r may be directly determined by a measurement of the inductance.

The inductance of such a toroid containing the ferrite powder as a core was measured initially by using the toroid in a series L-R circuit. As oscilloscope was used to measure the voltage across the resistor and across the series pair. By measuring the ratio of applied voltage to the voltage drop across the series resistor the inductance can be calculated as

$$L = \frac{R}{\omega}\left[\left(\frac{E}{E_R}\right)^2 - 1\right]^{\frac{1}{2}} \quad . \tag{3.7}$$

E and E_R are taken directly from the oscilloscope. Since the ratio is all that is important, the absolute accuracy of the oscilloscope is unimportant (see Figure 3.1a).

The above method is incomplete since it does not account for the errors due to dissipation in the inductor or stray capacitance. To eliminate the effect of dissipation, an L-C series resonant technique was adopted. It may be shown by a straightforward calculation that for parallel resonance

$$\omega = \sqrt{\frac{1}{LC} + \frac{R^2}{L^2}}$$

where R is the series equivalent loss resistance of the coil. For series resonance, the resistive term disappears. In the series resonant circuit the effect of the stray shunt capacitance may be readily computed. The resonant frequency is

$$\omega = \sqrt{\frac{1}{L(C + C_S)}}$$

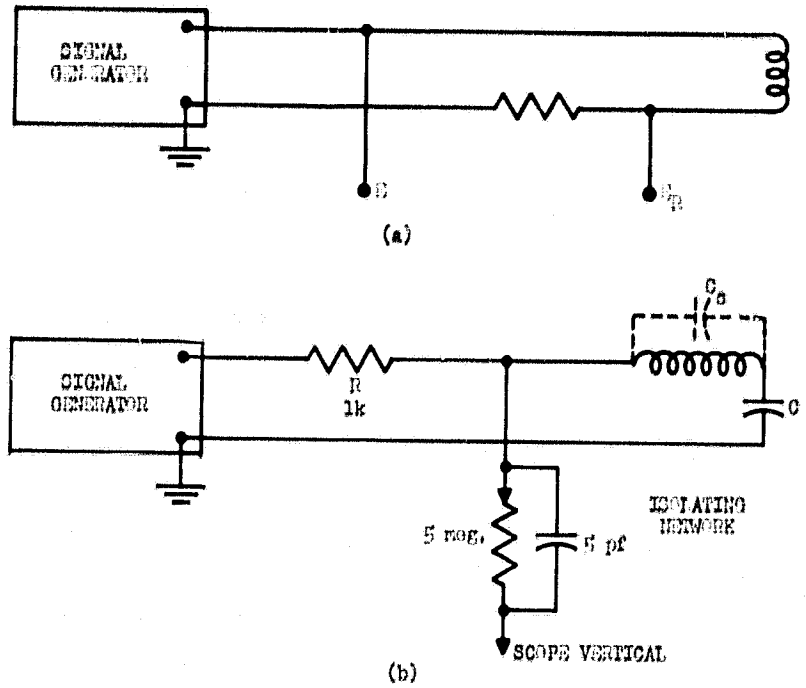


Figure 3.1 Relative Permeability Measurement Techniques
(a) Determination of Inductance by Voltage Ratio Measurement
(b) Determination of Inductance by L-C Resonance Measurement
(c) Measurement of Induced Voltage Resulting From Field of Long Straight Wire
(d) Measurement of Relative Induced Voltage Resulting From Field of Shorted Coaxial Test Line
(e) Measurement of Resonant Line Length Change Associated With Specimen In Shorted Coaxial Section

where C_s is the stray capacitance. In our experiment, C_s was determined to be about 5 pf by the following method. The resonant frequency was measured by observing the null on an oscilloscope across the circuit. Silver-mica capacitors of known value were used to resonate the toroid. At the three lowest values of C corresponding to the three highest frequencies, three equations of the form

$$\omega_i = \sqrt{\frac{1}{L(C_i + C_s)}} \tag{3.8}$$

were solved simultaneously in pairs for C_s. The average value was then used to compute the inductance (see Figure 3.1b).

The inductance of the toroid with varying densities of the ferrite powders was measured at frequencies from about 0.7 MHz to about 35 MHz. These frequencies varied because for a given toroid, the same set of known capacitors was used. The density of the powders was varied by mixing the ferrites in varying amounts of baby powder.

The same test was applied to the first of the toroids which was made from the silicone rubber and ferrite powder. Duplication of the same winding geometry as on the powder core was attempted. However, it was not possible to correlate the results with those obtained from the powders because any variation in the placement of the windings caused large changes in the inductance of the toroid. The rubber toroid was then wrapped uniformly with 174 turns of wire so that the conditions previously described in the calculations would be more nearly met. This toroid was then measured with a standard impedance bridge and the result compared to the measurement by the series resonant method. In this case the inductance did agree fairly well; however, the permeability indicated by this value of the inductance did not agree with that for the same density of powder in the previous measurements.

2. Long Wire Comparison Technique

The previous methods of measuring permeability have the disadvantage that the computation of inductance from the geometry is very inaccurate unless the toroid has a very large number of closely wound turns. In such a case, the losses and stray capacitance are quite large as is the inductance. Therefore, only measurements taken at relatively low

frequencies would have any chance for accuracy. An alternate method was developed in which the field configuration could be controlled. The geometry which produces fields having a symmetry compatible with the toroid is a long straight wire. Near the center of the wire the B and H fields are concentric about the wire and given very nearly by

$$H = \frac{I}{2\pi R} \quad \text{and} \quad B = \frac{\mu I}{2\pi R} \tag{3.9}$$

where I is the current in the wire and R is the distance from the wire. Since the boundary of the magnetic material of the toroid is always tangent to the fields if the toroid is concentric with the wire, the flux Φ in the toroid is computed as in the calculation for the case above except that N = 1.

$$\Phi = \frac{\mu I t}{2\pi} \ln (r_o/r_i) \tag{3.10}$$

Faraday's Induction Law states

$$\oint \vec{E} \cdot \vec{dl} = - \frac{d}{dt} \int \vec{B} \cdot \vec{ds}$$

and

$$\int \vec{B} \cdot \vec{ds} = \Phi$$

if the surface of integration contains the cross-section of the toroid. If

$$I = I_{peak} e^{-j\omega t}$$

then N turns of wire about a section of the toroid will develop a voltage

$$E = jN\omega\Phi, \text{ where } \Phi = \Phi_p e^{-j\omega t}$$

Here Φ_p corresponds to $I = I_{peak}$. Working now only with peak values

$$E_{peak} = \omega \frac{I_{peak}\mu tN}{2\pi} \ln(r_o r_i) \quad , \tag{3.11}$$

and solving for μ_r gives

$$\mu_r = \left(\frac{E_{peak}}{I_{peak}}\right) \frac{1}{\mu_o N f t \ln(r_o/r_i)} \tag{3.12}$$

Both E and I were measured on an oscilloscope. I was measured using a Tektronics PC-1 current probe (see Figure 3.1c).

This method had the advantage that the system could be calibrated with an absolute standard. A toroid was made containing no ferrite so that the permeability was known to be unity, and the performance of the apparatus could be determined through the use of this standard sample. The system was continuously improved. The wire was replaced by a long aluminum rod which supported the sample on a plexiglas centering guide. Various coil configurations and measuring instruments were tried. The most satisfactory arrangement consisted of using a short piece of coaxial cable, the center conductor of which formed a single turn pickup coil and the other end connected to a Tektronics high impedance oscilloscope such as the Tektronics 545-A with type CA dual trace amplifier.

At frequencies above about 5 MHz standing waves on the line create variations in current at different positions along the line. By necessity, the current probe was located about 2 feet from the position of the sample making it desirable to measure the current at the same position as the toroid. At this point it was decided that instead of relocating the current probe, the all-rubber toroid alongside the ferrite-bearing toroid being measured would serve as a direct comparison. In fact, the output voltage from each toroid is directly proportional to its permeability. Thus, the permeability of the sample being measured is just the ratio of the output voltages. These voltages are readily compared on a dual trace oscilloscope.

The above method greatly improved the effectiveness of the permeability measurements. However, considerable R.F. noise was encountered

using an open line at frequencies above 15 MHz. The reason for this is that the output of the signal generator is very low and the inductance of the line limits the current to a low value. Thus, the useful signal is of the same order as stray R.F. fields in the vicinity. To eliminate this problem it was decided to enclose the experiment in a large diameter coaxial line. Such a line was constructed from hard copper tubing. The outer conductor was 2.45 in. I.D. and the inner conductor 1.125 in. O.D. Using the well-known relation for an air dielectric line

$$Z_o \approx 60 \ln r_o/r_i = 47 \text{ ohms} \quad .$$

The length was 57 in. Reducing cones were used to match the large diameter line down to a standard BNC connector. A 50 ohm and a shorting termination were made so that full advantage of the generator power was possible. A narrow slot was cut along the outer tube to allow exit for the RG 58A/U cable from the toroids under test. The all rubber toroid and the toroid under test were placed side by side on a plastic guide near the shorting termination. Using six inch cables on the toroids, the coaxial line allowed permeability measurements up to 50 MHz (see Figure 3.1d).

The useful frequency range of the measurements above described was actually limited to about 35 MHz because of the support equipment. The output from the rubber toroid was quite small due to the small driving power available. In order for the measurements to be meaningful, no current must flow in the pickup coils. These currents are difficult to eliminate at high frequencies. Even the short lengths of connecting cables, combined with the capacitance of the oscilloscope input create considerable leading of the pickup coils. A technique for high frequency measurement was adapted to our equipment which enabled measurements to be made up to 250 MHz.

3. Resonant Line Techniques

Method cited utilized a length of coaxial line as a resonant cavity. When a coaxial line is resonant at a quarter wavelength from a shorting termination, the line may be thought of as a lumped L-C parallel circuit. The same is true for the section of the line nearest the short when the resonances are at 3/4, 5/4, etc. That is, one may neglect the

portion of the line ahead of the last quarter wavelength. The resonant frequency and the inductance of a line are related by

$$\omega_r^2 = \frac{1}{LC}$$

and hence differential changes in line inductance can be related to changes in resonant frequency as

$$2 \frac{d\omega}{\omega_r} = - \frac{dL}{L} \qquad (3.13)$$

Near the end of the line, the flux density as a function of position along the line may be considered constant over distances small compared to a quarter wavelength. Also, the E field is very nearly zero so that loading the line in this region does not alter the lumped capacitance of the line. If the length of the line is changed slightly the change in lumped inductance is very nearly linear with this change due to the increased number of flux linkages there. If, however, the frequency is held constant, the effect of moving the shorting termination merely moves the position of the null. If the end of the line is loaded with a permeable material the increase in flux in the material has the same effect as lengthening the line. In order to return the current null to its original position, the line may be shortened by moving the sliding termination toward the source an amount to equalize the inductance in the last quarter wavelength of the line. Thus, a simple measurement of the length of the line, the interior dimensions of the line, and the dimensions of the toroid, will suffice to determine the permeability of the toroid. However, a simpler technique is to construct a toroid of aluminum or copper identical to the ones to be measured. At high frequencies, the surface currents induced in the metal toroids completely shield the interior of the toroid from magnetic flux and the line must be accordingly lengthened to restore the position of the null. Thus, the metal toroid behaves as though it had a permeability of zero.

Let l_o, l_m, and l_f, be the length of the line at resonance with the line empty, the metal sample in the line, and the ferrite sample in the

line respectively. It is understood that $\ell_m > \ell_o > \ell_f$. The relative permeability is then simply

$$\mu_R = \frac{\ell_m - \ell_f}{\ell_m - \ell_o}$$

or factoring the above expression

$$\mu_r = 1 + (\ell_o - \ell_f) \; / \; (\ell_m - \ell_o) \qquad (3.14)$$

Actually, the line length is not measured but, as shown, only the changes in length when the appropriate loading is inserted. The resonance is measured by observing an input current null with a current probe in the feed line at the connector end of the large coaxial line. If desired, a length of ordinary 50 ohm coaxial cable can be added to increase the effective line length and lower the fundamental quarter wavelength frequency. However, below about 50 MHz the null point is quite broad and the accuracy of the experiment becomes poor. Detection was made using a Telonic R.F. Detector and a Hewlett-Packard D.C. VTVM with 1 mv full scale sensitivity (see Figure 3.1e).

The upper limit of frequency occurs when the circumference of the toroid is about one wavelength for a wave in the material of the toroid. Assuming that $\mu_r = 8$ and $\epsilon_r = 3$, which is the value given for the rubber alone, this occurs at $f \approx 300$ MHz. A smaller sample and line might be used to even higher frequencies. A further discussion is contained in the references.[8, 9]

4. Torque Magnetometer Technique

The methods of permeability measurement described above utilize a large toroidal shaped sample. The finished keeper is a thin flat sheet not amenable to measurement by these means. It was considered necessary to make some sort of measurement on the actual keeper material to assure its conformity with the results of measurements on the toroidal samples. A static torque test was developed for this purpose.

A uniform field was obtained by incorporating the experiment into the Helmholtz coils of the Kerr apparatus. A calibrated 1 mil diameter

Tungsten fiber attached to a rotating holder with suitable indicating apparatus was used for determining torque. A disk 1-1/16 in. diameter was cut from a sample of the keeper sheet. The thin disk is a convenient shape for the calculations of demagnetizing factors. The disk was suspended by the fiber over a line drawn 45° to the applied field. The field was increased in small steps and the torque required to hold the disk at 45° was measured.

The measured torque can be directly related to the susceptibility. The relationship, derived in detail in Appendix E, is found to be

$$X \approx \tfrac{1}{2}\left[A + \sqrt{A^2 + (A/\pi)}\ \right] \qquad (3.15)$$

where

$$A = \frac{2T}{VH_o^2 \sin\theta} \qquad (3.16)$$

In this expression

T = measured torque
V = sample volume
H_o = applied field
θ = angle between field and sample plane.

An expression taking into account the exact demagnetizing factors of an ellipsoidal sample shape is given in Appendix E.

Using this technique it has been possible to show that the permeability, given as

$$\mu_r = 1 + 4\pi X \quad \text{(egs units)} \qquad (3.17)$$

is independent of field strength up to 5 Oersted and the material exhibits no appreciable remnant magnetization for fields of practical interest in memory operation.

D. QUANTITATIVE RESULTS

The keeper material made by vacuum mixing and pressing was determined to have a density of T-1 powder of 2.36 gm/cm^3. This is approximately 85% of the maximum attainable density of 2.77 gm/cm^3 for the T-1 powder which has passed through the 50 μ sieve. The permeability of the powder is approximately 10.4 and that of the finished keeper, measured statically, is 9.5.

Inductance measurements on the ferrite powders in varying densities indicated that the permeability of the powders is nearly independent of the initial permeability of the corresponding bulk materials. It was indicated that the permeability was also independent of the frequency over the range from about 1 to 50 MHz. The permeability was, however, very much related to the packing density of the powder. Unfortunately, the inductance experiment did not allow calculation of the permeability and the above conclusions were based on the behavior of the inductance for a fixed geometry, which is only some undetermined function of the permeability of the powder. The relation of inductance to frequency and density is shown in Figures 3.2 and 3.3.

The actual magnitude of the permeability of the powders was determined by the Faraday Induction Law method described above. The frequency range for these measurements was from 1 to 50 MHz. The results of these measurements on the four test toroids confirm the general results of the inductance measurements. The highest permeability measured was about 7.5 for 2.36 gm/cm^3 of T-1 powder. The results of these measurements are shown in Figures 3.4 and 3.5.

The frequency range of the permeability measurements was extended to VHF frequencies as described above. Again, the powdered ferrite showed no significant change in permeability due to frequency.

Finally, the finished keeper sheet was tested for static permeability. The permeability was determined to be 9.5. The torque test confirmed that the keeper material had a linear magnetization versus applied field relation at least up to about 5 Oersted applied field. Also there was no indication of remanence in a field up to 8 Oersted. The magnetization curve is shown in Figure 3.6.

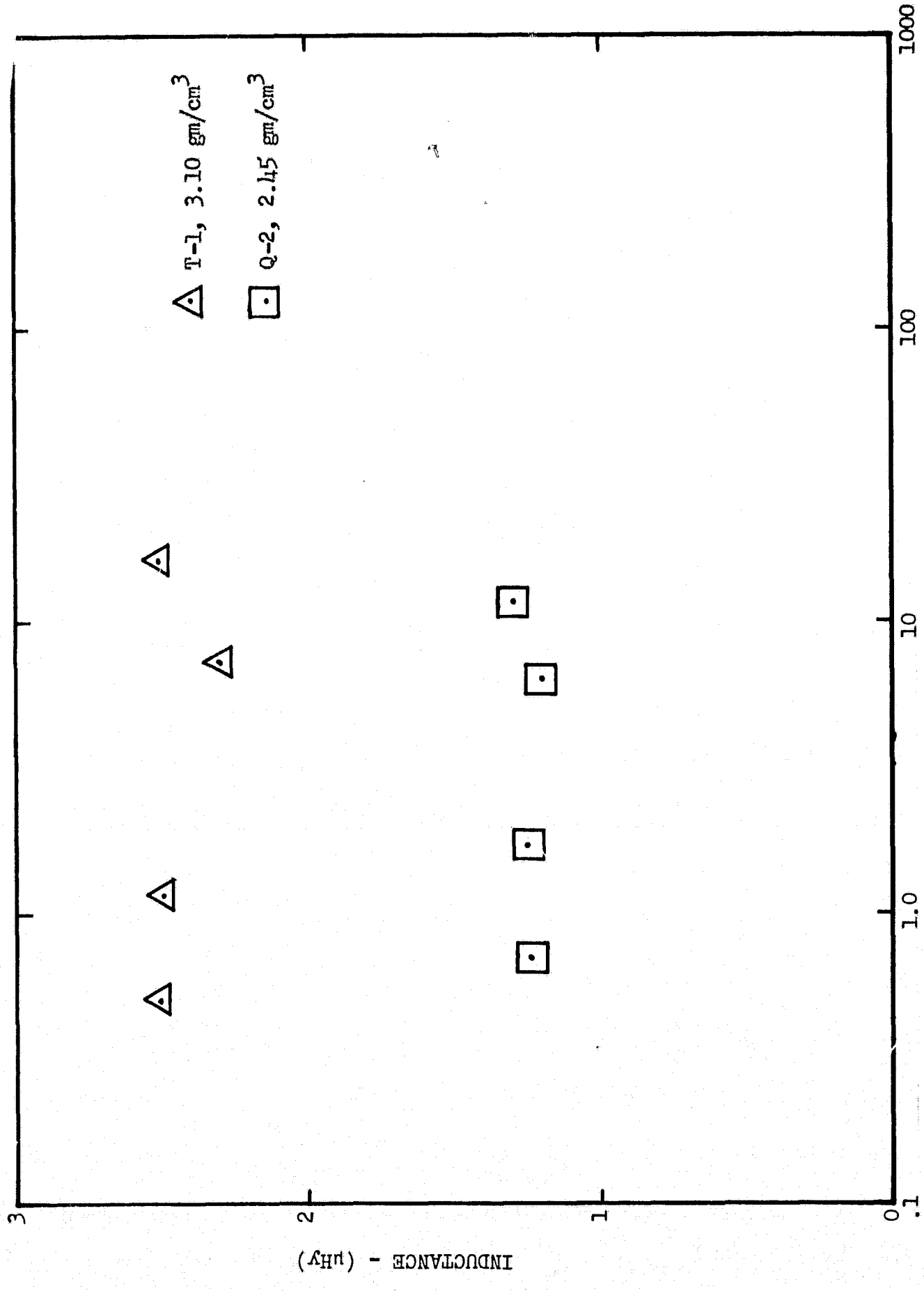


Figure 3.2 Inductance of Powder Core Coil vs. Frequency For T-1 and Q-2 Materials, Using the Technique of Figure 3.1b

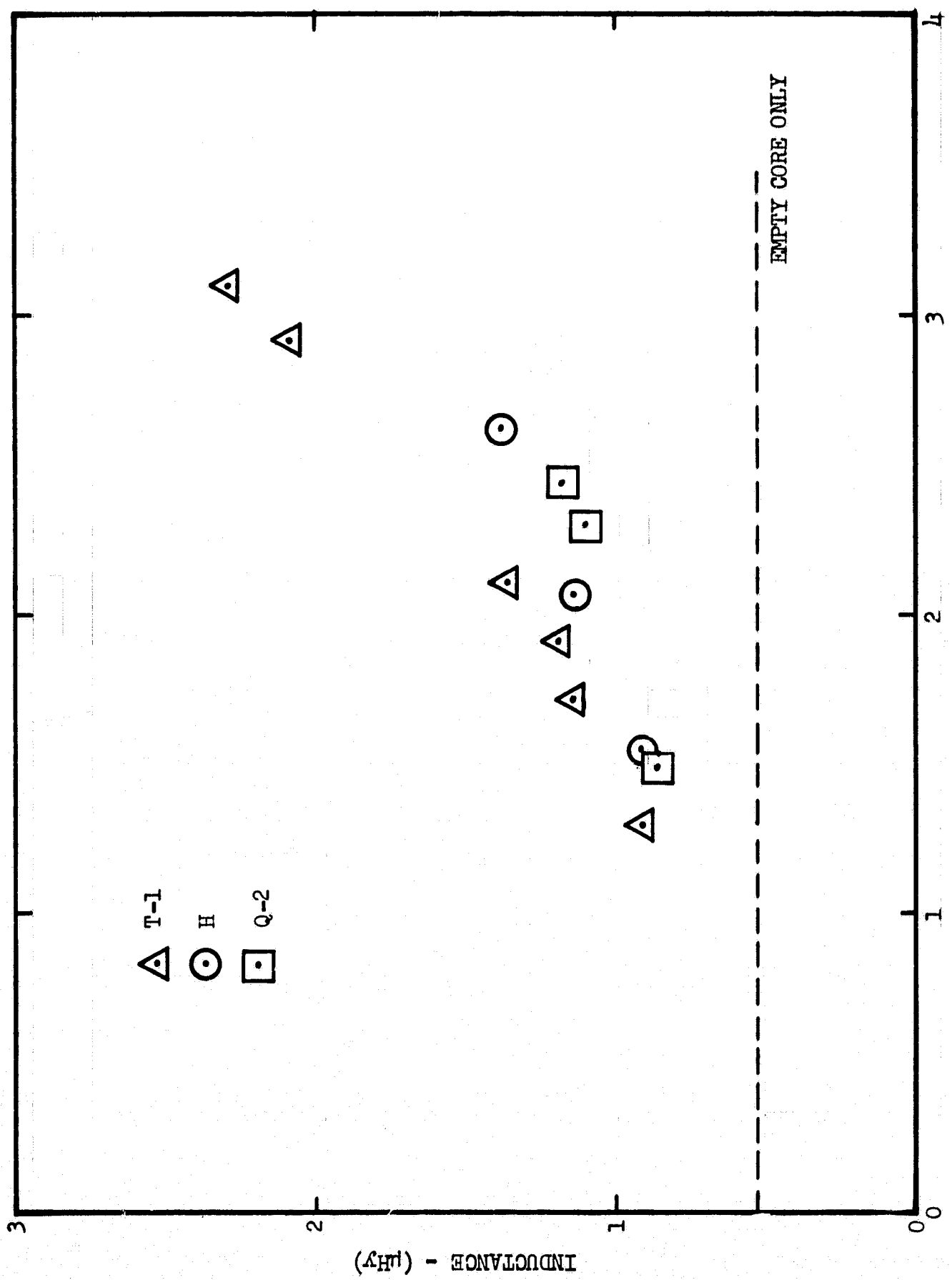


Figure 3.3 Inductance of Powder Core Coil vs. Powder Density For T-1, Q-2, and H Materials, Using the Technique of Figure 3.1b

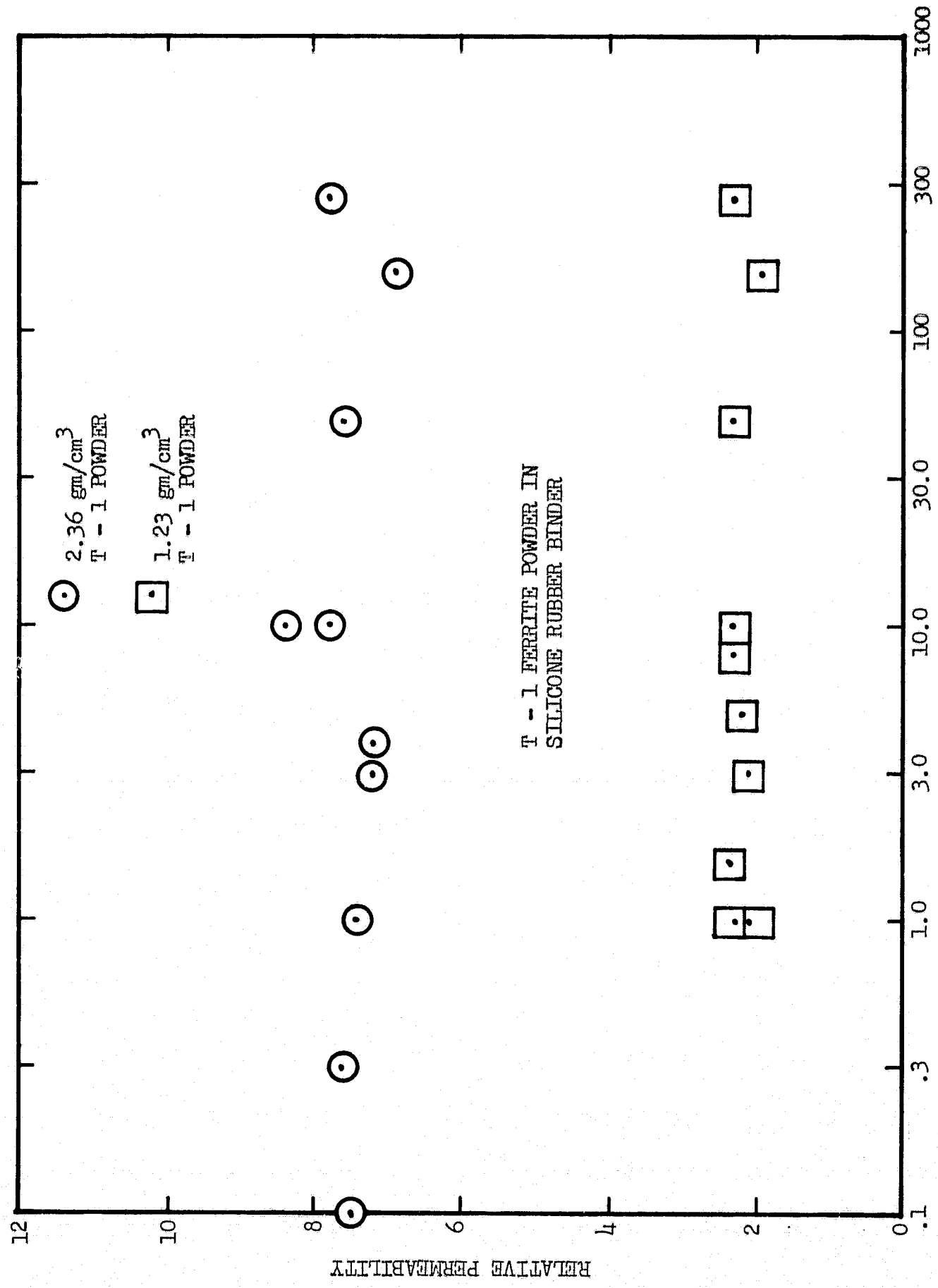


Figure 3.4 Relative Permeability of Silicone Rubber and T-1 Ferrite Powder Mixture as a Function of the Ferrite Powder Density Using Method of Figure 3.1d

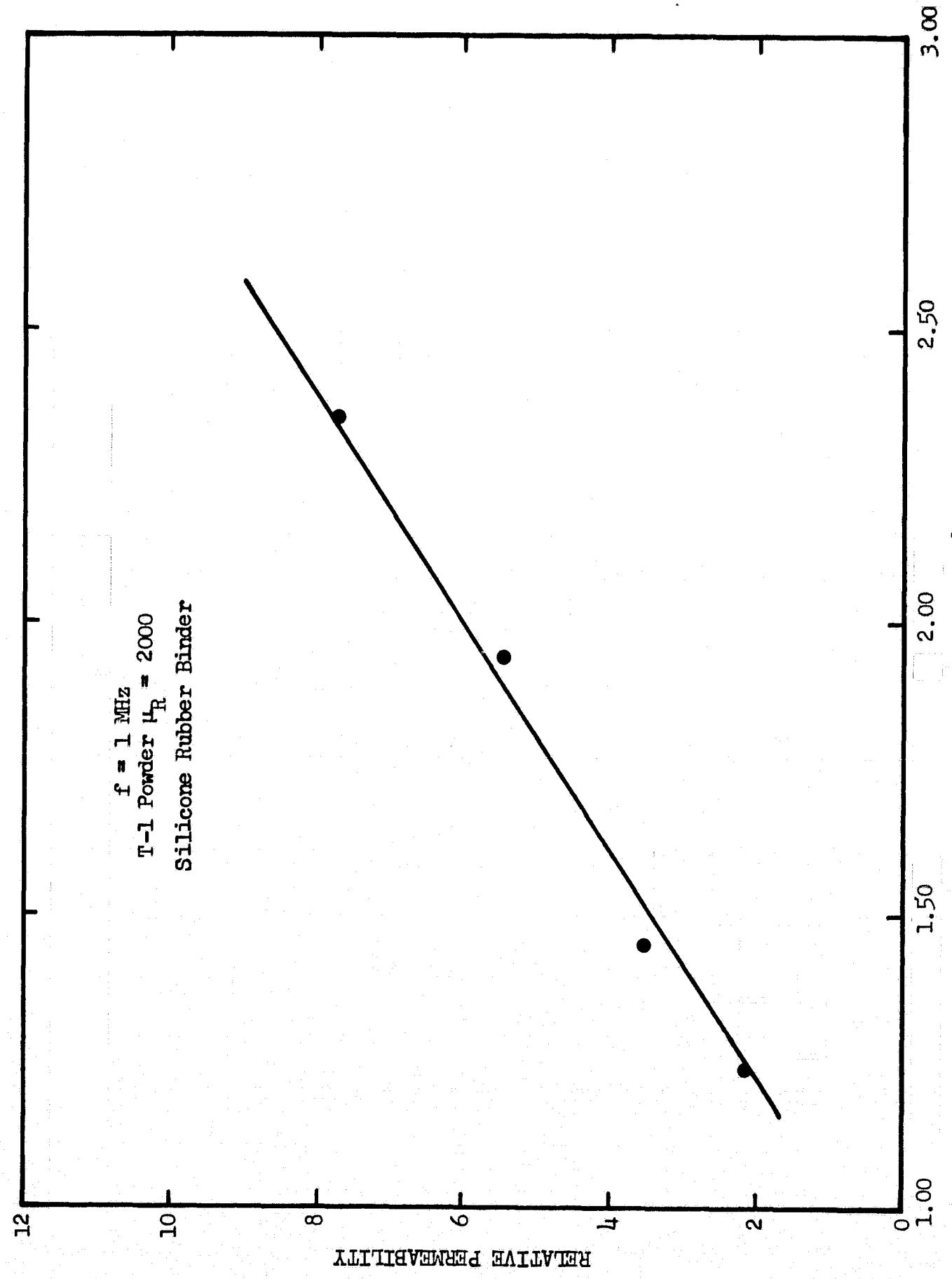


Figure 3.5 Relative Permeability of Silicone Rubber and T-1 Ferrite Powder Mixture as a Function of Frequency for Two Powder Densities Using Method of Figure 3.1e

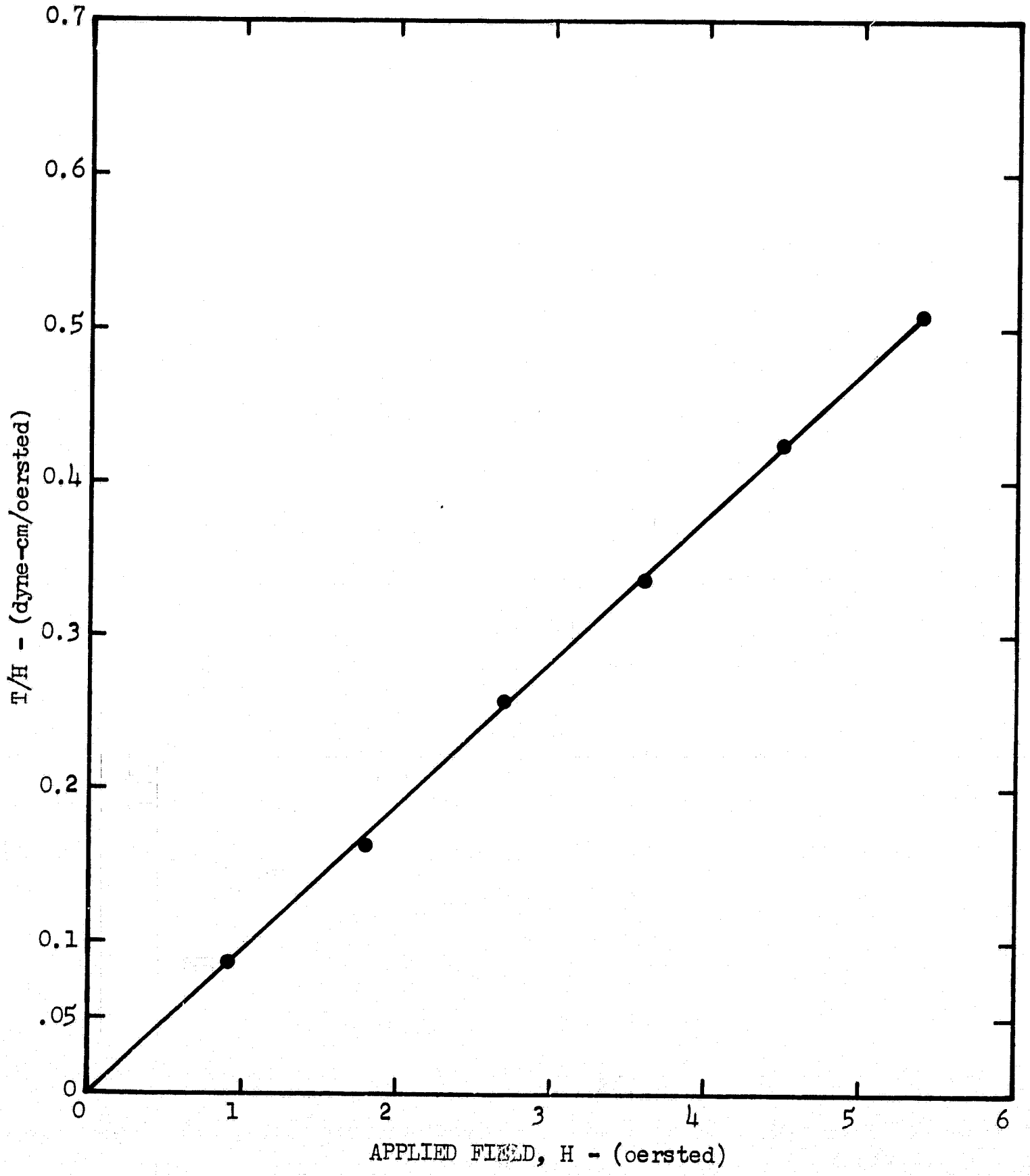


Figure 3.6 T/H vs. H for Final Keeper Material as Obtained From Torque Magnetometer Measurement

E. DISCUSSION

The keeper must be an integral part of the design of any magnetic memory system which utilizes open flux elements such as thin films. In particular, if the storage density of the array is to be large enough to be useful, the stray fields from the elements are certain to interfere with each other as will the driving fields.

In order to construct a suitable keeper for the all evaporated memory plane, it was decided to utilize the favorable properties of the ferrites while hopefully eliminating their disadvantages. It was decided to use finely crushed ferrite powder held in a flexible binder so that the keeper might be molded against the memory surface or at least molded against a very smooth surface and then applied to the memory. At the same time, it was hoped that the powder would yield sufficient permeability.

The question of the permeability is basic to the keeper since it has been shown that the expressions for both image strength and current enhancement contain the factor $\frac{\mu - 1}{\mu + 1}$. Thus an efficiency of greater than 80% is attainable with a relative permeability of only 10. In the present work a permeability of 8 was projected from the experimental results. This figure gives an efficiency of 76%. In order to gain a much greater permeability other characteristics might be sacrificed.

1. Theoretical Model for Permeability

A calculation was made to estimate the attainable permeability with a powdered material. This calculation is similar to Lorentz' calculation for the electric polarizability. The keeper is assumed to be made of discreet, spherical particles which occupy some fraction of the volume of the material. The rest is filled with a non-permeable substance. The field inside of a given particle is computed as though the particle were interior to a large spherical cavity in the material. The other particles in the cavity are assumed isotropically located so as not to affect the particle of interest. Quite naturally, this last assumption is not wholly valid. In particular, if several particles happen to touch, the demagnetizing fields of the particles will be greatly disturbed. There is no doubt that such effects occur. However, the important features of the keeper are predicted by the simpler assumption.

Let M_o, χ_o and μ_o denote the magnetic quantities associated with the

keeper and M', χ', and μ' denote those of the particles. On a macroscopic scale $M_o = F_p M'$ where F_p is the fraction of the total volume occupied by the particles. The field H' within the particles has three components; H_o the applied field, $4\pi/3\ M_o$ the demagnetizing field due to the imaginary cavity, and $4\pi/3\ M'$ the demagnetizing field due to the particle itself.

$$H' = H_o + \frac{4\pi}{3} (M_o - M') \ . \tag{3.18}$$

Then since $M = \chi H$,

$$M' = \frac{3\chi' H_o}{3 + 4\pi\chi' (1 - F_p)} \tag{3.19}$$

From this we obtain

$$\chi_o = \chi' \left[\frac{3F_p}{3 + 4\pi\chi' (1 - F_p)} \right] \tag{3.20}$$

and recalling that $\mu = 1 + 4\pi\chi$ we can solve for the permeability

$$\mu_o = 1 + \frac{3F_p(\mu' - 1)}{3 + (\mu' - 1)(1 - F_p)} \tag{3.21}$$

The family of curves generated by this relation for differing values of F_p are shown in Figure 3.7. These curves approach the value

$$\mu_o = 1 + \frac{3F_p}{1 - F_p}$$

for large values of μ'. This behavior is similar to that in Figure 3.3 which shows the resultant permeability much more strongly dependent on density than on the bulk permeability of the powder. The fact that the permeability of the keeper does not seem to be affected by the frequency may also be explained by the results of this calculation. The permeability of the T-1 ferrite is known to decrease sharply at frequencies above 1 MHz yet the permeability of the T-1 powder and the keeper made from it does not change appreciably with frequency even up to 250 MHz.

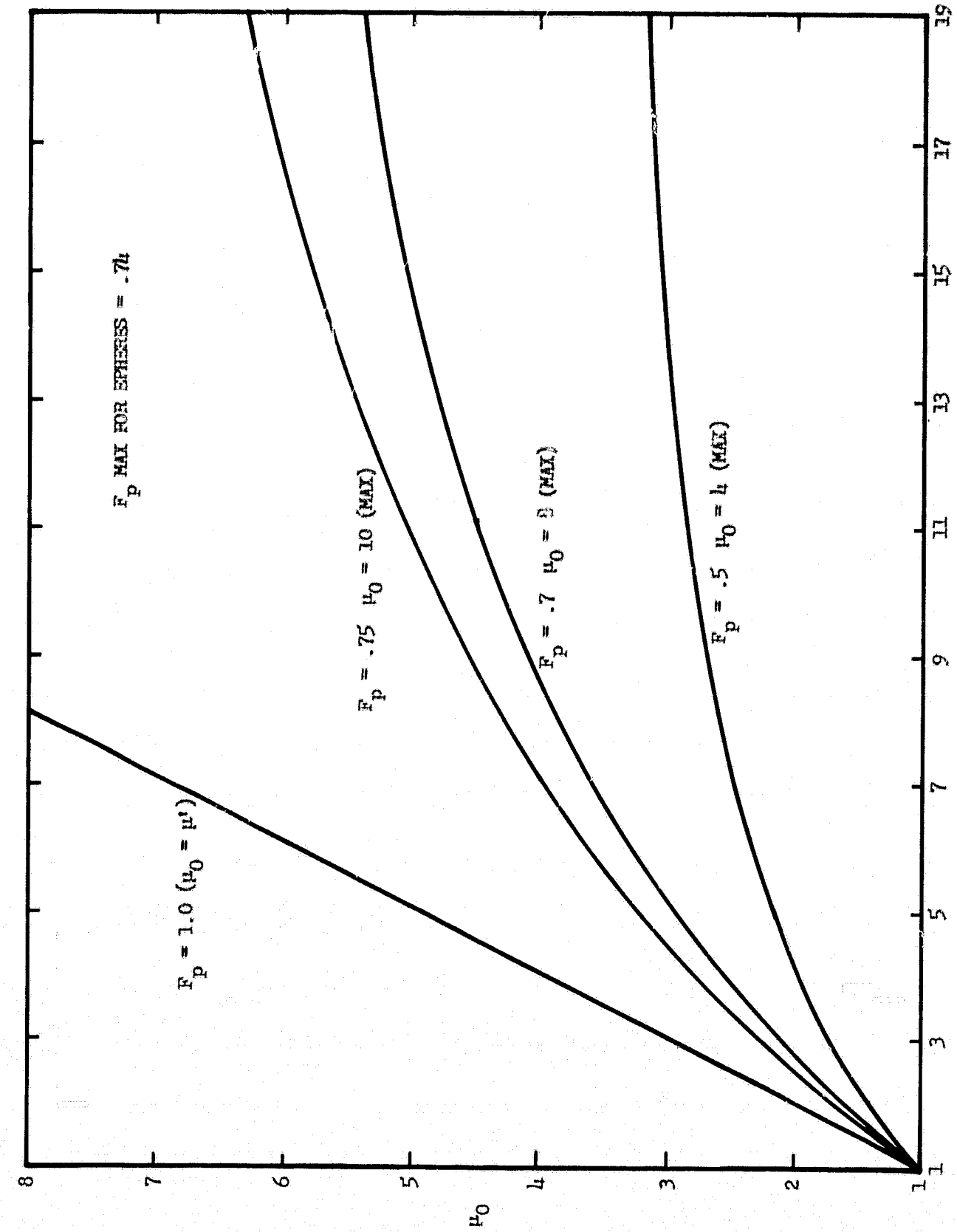


Figure 3.7 Theoretical Prediction of Relative Permeability of Keeper Material vs. Permeability of Bulk Ferrite for Three Different Packing Factors

The one quantity which does not agree too well with the calculation is the magnitude of the permeability. The volume fraction of the fabricated keepers is considered to be no greater than 0.6 for which the predicted maximum permeability is 5.5. The measured permeability, however, has been found to be 7.5 in the toroidal samples. This would indicate that assumptions made in the calculation of the permeability are not so simple. The assumption of no interaction between near particles is probably the greatest source of error.

The fact that the magnetization curve, as shown by the static torque data, is quite linear is undoubtedly due to the large demagnetizing fields acting on each particle. Thus, the magnetization of each particle is still in the linear region. This also gives a good explanation why there was no detectable remanence.

2. Accuracy of Measurements

Very little has been done to ascertain the losses in the keeper. As noted, the keeper does not appear to have any remanence in static tests. It must be assumed that the losses in the keeper could be compared with those of the bulk material when the latter is subjected to time varying fields of the same magnitude as the internal field of the particles in the keeper. However, the presence of high frequency losses due to the keeper were noted in the resonant cavity permeability measurements. The indications were a decrease in the sharpness of the current null. Unfortunately, the equipment was not calibrated for qualitative measurement of losses.

The methods developed for permeability measurements are considered to be much more reliable than ordinary inductance measurements. If the material is isotropic, the use of a toroidal test sample greatly simplifies the test geometry. The Faraday Induction Law method is much simpler to implement and interpret than inductance measurements because the effects of losses and stray capacitance are eliminated. By maintaining careful dimensional tolerances and obtaining sufficient driving power and detection sensitivity, it is estimated that 5% accuracy is easily obtainable up to about 10 MHz. As the materials were soft and difficult to instrument, our accuracy is probably no better than 7% to 10% up to 10 MHz and probably decreases at higher frequencies due to limitations in the driving and detecting apparatus. In any case, it is difficult to provide a sufficiently high impedance for accurate measurement at frequencies much above 10 MHz. Although a few

measurements were made up to 50 MHz, due to very low output from our standard sample, it is doubtful that better than 20% accuracy could be obtained.

For measurement at high frequencies, up to microwave regions, the resonant cavity measurements of one type or another provide the only reasonable way to obtain permeability data. Accuracies of ± 5% are attainable with this technique. As discussed, our own equipment limited us to about 300 MHz because of the size of the coaxial line used and the samples employed. For measurements above this range the slotted line method is perhaps the most accurate and has the added advantage that loss factors are readily obtained. For memory applications, it is usually not necessary to extend permeability much beyond the 200 MHz covered adequately by the methods described in this report.

3. Physical Properties

Once it was determined that the ferrite powders mixed in a binder of silicone rubber would meet the electrical needs of the keeper material, it was necessary to form a sheet of this composite suitable for application to the memory surface. The electrical test samples were sectioned and examined under low power magnification. They were found to have large numbers of sizeable air holes. The literature from the supplier of the silicone rubber indicated that the rubber alone should cure in deep sections free from air holes. However, the addition of the ferrite powder greatly increases the viscosity of the mixture. Attempts to cure a mixture of powder and rubber in vacuum in order to reduce the number of air bubbles revealed that quite a large amount of air was trapped in the mixture presumably by the mixing process. Therefore, it was decided to attempt to mix the substances in vacuum and to cure them at atmospheric pressure. This resulted in sheets of a very uniform internal structure and free from air holes.

The maximum density of the ferrite powder obtainable from this type of combination seems to be limited to about 2.5 gm/cm^3. The maximum density of the powder is nearly 3.1 gm/cm^3. If the powder is mixed with less of the binder the two will not mix well and dry spots will occur resulting in pitting of the surface of the sheets when they are peeled from the forming blocks.

The silicone rubbers and resins used have a good adherence to most surfaces when cast against them. This was particularly true of the Sylgard 184 resin. For this reason the sheets were cast against a stainless steel

foil which could be peeled back more easily. This method worked particularly well with the RTV 3110 rubber. The silicone rubbers have the added advantage that they will continue to flow for some time after curing and the very smooth cast surface did flow about the crevices and depressions on the surface of the memory when held against it for about two days.

F. SUMMARY

A suitable keeper can be readily fabricated from finely ground ferrite powder and a silicone rubber binder pressed into a sheet and applied to the memory plane. The magnetic properties of such a material are well suited for keeper applications. The material retains its permeability for very high frequencies, at least up to 250 MHz, and does not demonstrate any significant remanence. The permeability of the material depends strongly upon the density of the powder in the material. A permeability of 7 to 8 is readily obtained and is sufficient for a keeper. It is not likely that significantly higher permeabilities can be obtained in this manner and, in fact, it would not be to any great advantage to increase the permeability to a much higher value since other undesirable effects might be introduced.

Several methods of permeability measurement were investigated. Methods involving the measurement of the inductance of fixed geometries encounter many problems at high frequencies. These measurements are much more easily made by utilizing the compatible symmetry of a toroid and the fields about a long straight wire or internal to a coaxial line and applying Faraday's Induction Law. At frequencies between 0.1 and 1.0 GHz permeability measurements are probably best made by resonant cavity methods. One such method is described in this work. Loss measurements can also be obtained directly from this type of measurement.

The permeability of powdered ferrites can be estimated by assuming that the model of a particle in a cavity is applicable and that nearby particles do not strongly interact, or that effects of nearby particles cancel each other. The result indicates that for spherical particles, the maximum attainable permeability is about 10.

This investigation of keeper materials for a thin film magnetic memory has accomplished the purpose of producing an adequate material for this application. It would be desirable to continue the study of the relation of the keeper properties to memory operation parameters. There are,

also, several variables whose effect has not been investigated. Among these is the effect of particle size and keeper sheet thickness.

Techniques should be investigated for the experimental determination of the effect of the keeper on the stability, shape anisotropy, and dispersion of the magnetic films. It is likely that the Kerr Effect Apparatus would be useful in this purpose. In addition, the beneficial effects of the keeper as described above should be verified experimentally in the operation of a memory test plane.

IV. ELECTRONIC CIRCUITS EFFORT

Several goals were outlined in the original proposal. These included development of analytical techniques to study the response of the integrated array, design of drive and sense circuits, study of the possibility of using field effect devices, and the protection of circuit performance at higher repetition rates. Essentially the circuits effort was a study of the feasibility of an all integrated electronics system. It was hoped to define the problems associated with the use of integrated circuits in drive and sense applications with thin film memories.

The following basic results were achieved. Analytical techniques for studying transmission lines of the system were developed. These are detailed in Section II. A Fourier series computer program for studying the response of amplifiers in the time domain was developed. This program is discussed in Appendix D. Performance of the integrated circuit amplifiers can be predicted with the aid of simple models and this computer program. Circuit designs which are compatible with the limitations of integrated circuits were developed and tested. Not only are these circuits easily integrated, but they are all very similar and make use of a "basic circuit module" which will simplify the completed system. A design technique for solving the coupling problem in multistage amplifiers is outlined. This problem deserves more attention in the future. The relationship between power consumption, circuit speed or frequency response, and pulse amplification is detailed. This relationship could make optimization with respect to chip area and power consumption a tractable problem. The possibility of using field effect devices was studied briefly but was rejected because of the limited number of complete linear functions (such as differential amplification) available with field effect devices in integrated form. This does not rule out their use in the future, but means only that it was more convenient at the time to work with monolithic bipolar circuits.

The circuits effort is explained in the following six sections. These sections describe

A. The basic circuit module, common to all circuit design,
B. The sense amplifier,
C. The word line driver,
D. The bit line driver,

E. The gates,

F. The timing chart, power consumption chart and the mother board.

A. BASIC CIRCUIT MODULE

It was desired to obtain as much similarity between the circuits as possible. This makes the task of integration simpler and means that once the basic circuit is understood and optimized, design of the various circuit functions is a routine matter. Optimization can be made with respect to a variety of performance indices, e.g., power consumption, chip area of the circuit, frequency response, radiation resistance, cost, and any other attribute of a circuit design. The danger of standardization is that when the basic circuit is optimized with respect to some arbitrary performance index, it does not do the particular job at hand in the best possible manner. For example, a circuit which makes a good sense amplifier may not make a good word driver. Fortunately this is not true in the present case. When compatibility with emitter coupled logic and the limitations of monolithic circuits are considered, the basic circuit module is a best choice for both the sense amplifier and the gates and drivers.

One of the greatest problems facing the digital circuit designer has always been the achievement of high speed with low power consumption. This basic challenge continues into the integrated circuit era. The over-riding factor in the choice of circuits was the voltage gain/power consumption factor.

Reference to Figure 4.1 will show some of the general aspects of the problem. The active element, the transistor configuration, is represented as a voltage controlled current source. Equivalent input, output, and feedback impedances are shown for the device. It should be noted that these capacitances and resistances are normally themselves functions of frequency. The current source has a response characteristic which can be represented in the frequency domain by a simple pole.

One immediately sees the possibility of Miller effect capacitance adding to the input capacitance C_i. This Miller effect capacitance, essentially C_f multiplied by the voltage gain for the circuit, is typically several times greater than C_i. To prevent loading of the preceding stage, then, it is necessary that the preceding stage have a low output impedance.

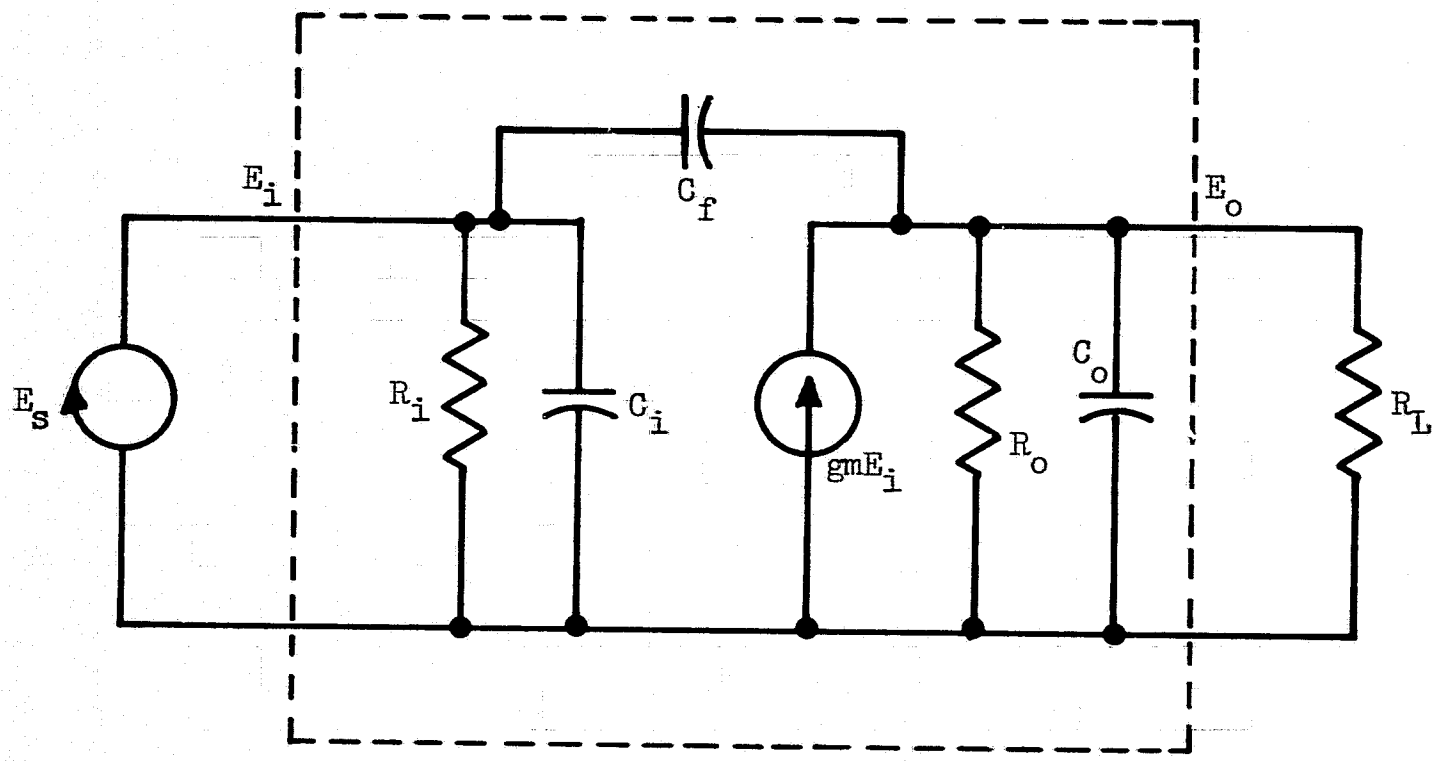


Figure 4.1 Model for a general amplifier stage showing input, output, and feedback impedances

This is provided by emitter followers in the final circuit design. Therefore the driving source is represented as a voltage source.

The output resistance R_o of the amplifier is typically many times higher than the load R_L. Thus the low frequency voltage gain is given by $g_m R_L$. The frequency response of the amplifier is not determined by the frequency response of the current source, but rather by the pole of impedance of the R_L - C_o parallel combination. For example, the devices chosen for the basic amplifier have output capacitances of about 7 picofarads. Add 3 picofarads of stray capacitance and a load resistance of 1000 ohms, and the parallel combination has a pole at 16 MHz. This is in comparison with the pole at about 50 MHz in the frequency characteristic of the current source. The relationship between voltage gain and frequency response is thus established. The first break in the frequency characteristic is inversely proportional to the voltage gain of the circuit, for a fixed g_m.

The relationship between frequency response and voltage gain may be extended to include power consumption. Most devices show an increase in transconductance as the quiescent current is increased, at least to a point. The integrated circuit devices chosen for this work show a direct increase in transconductance as the current level is increased. For these particular devices, the proportionality constant is 8 millimhos per milliamp of quiescent current. This relationship is not affected by the quiescent collector voltage.

These conclusions may be drawn. The gain-bandwidth product for the circuit is $g_m R_L \omega_c$, but since $\omega_c = 1/R_L C_o$, the product is simply g_m/C_o. The gain-bandwidth product is thus directly proportional to the quiescent current consumption. The small signal characteristics of the amplifier are not affected by collector voltage if it is above 700 millivolts. Since collector power, collector to emitter voltage times collector current, is in a sense "wasted" power, it is desirable to operate the transistors in a low voltage configuration. The most desirable configuration seems to be a low voltage, high current circuit with small collector load resistors. Operation with low collector voltages will require precise control of collector quiescent current. Typically the circuits chosen operate with 2 volts dropped across the load resistor and one volt collector to base.

The greatest signal amplification takes place in the sense amplifier. Since standardization of circuit types is helpful in integrated circuits work, the requirements of the sense amplifier have heavily influenced the

choice of circuits for the various drivers and gates. A differential amplifier pair was chosen for the basic module in the design of the sense amplifier. This choice was obvious for the input stage, since the bit line is balanced. However the advantages of the differential pair led to its use in all of the circuits.

The advantages of the differential pair as a basic building block are listed in Reference (10). The use of a balanced configuration allows many ambient effects, such as power supply variations and temperature changes, to be cancelled out. No capacitors are normally needed and the resistance values are relatively low. Operation of the unit depends on resistance ratios rather than absolute values. With the addition of output emitter followers, the quiescent output voltage can be the same as the input voltage. Stages may thus be directly cascaded. This is an important consideration if only one type of transistor, e.g., the NPN, is allowed on the chip. Quiescent current levels may be strictly controlled with resistor ratios.

Two other advantages are particularly important. These are the differential amplifier's ability to reject common mode signals at the two input terminals and the natural limiting ability of the amplifier. Suppose two differential amplifiers are cascaded in a direct coupled circuit and the quiescent current of the first amplifier changes. Both collector voltages of the first amplifier then change and change the input voltages to the second amplifier. But since this change is a common mode signal the output levels of the second amplifier change little, if at all. The natural limiting ability of the differential pair enables its use as a non-saturating switch. This is the principle of emitter coupled logic, for example, Motorola's MECL. The total collector current through the pair is determined by a constant current source in the emitter lead of the differential pair. The load resistors are selected so that when all of the collector current flows through one load resistor, the transistor is still not saturated. Thus there exists the possibility of using the same circuit module for both logic and amplification in a digital system.

The basic module consists of a differential pair operating with low collector voltages and with emitter followers on each collector load resistor. This configuration is shown in Figure 4.2. The differential amplifier is the R.C.A. type CA3005. The emitter followers are type 2N918 discrete

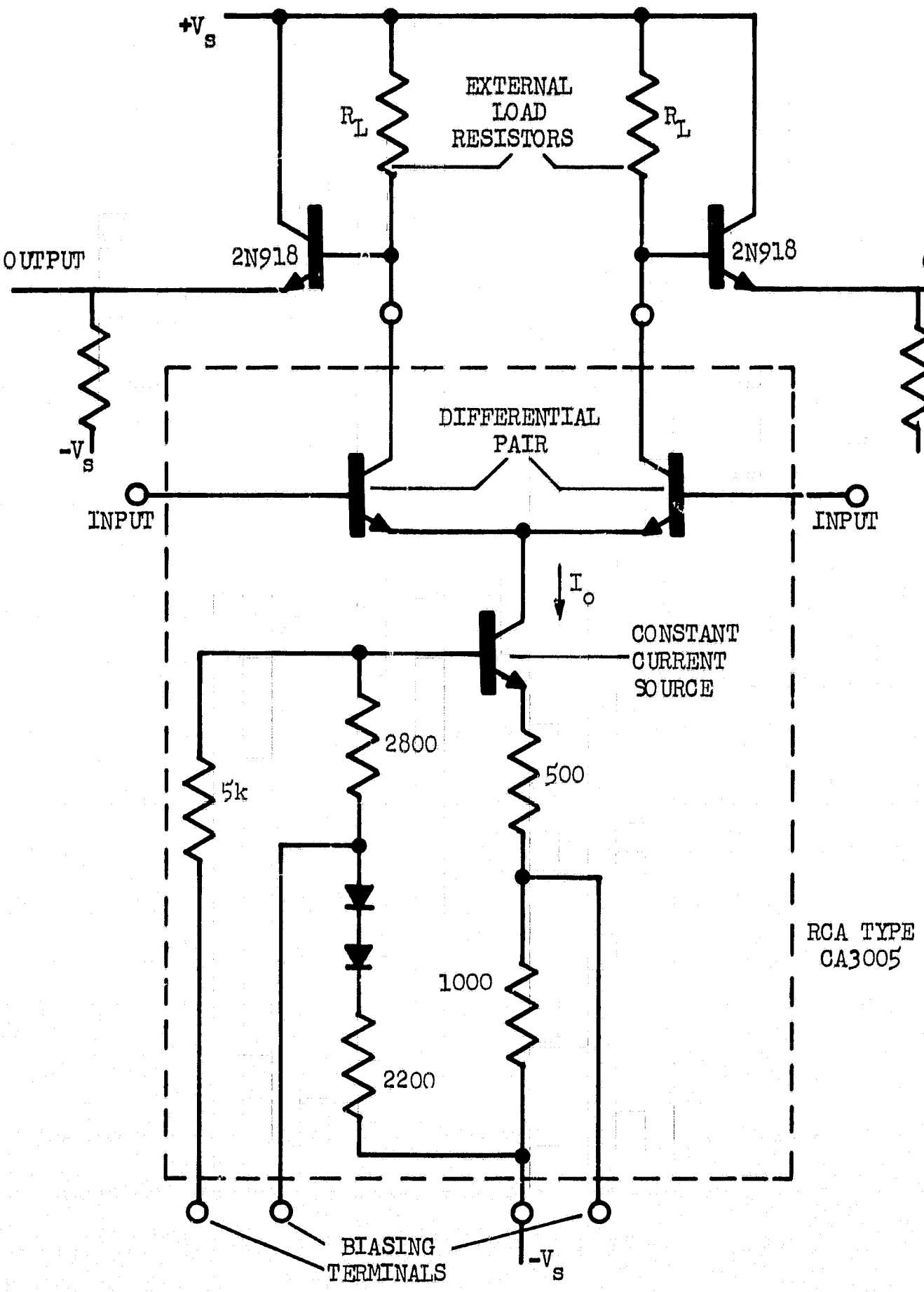


Figure 4.2 Circuit diagram of the basic circuit module

transistors. The 2N918 is a passivated epitaxial transistor that is very similar to a non-gold-doped monolithic transistor. Such a transistor is used in high frequency linear amplifier applications. The 2N918 is also used for gating applications in the final circuits. Separate chips would allow the use of PNP transistors or gold-doped-collector transistors for these saturated switching jobs. Much progress is being made in placing PNP and NPN transistors on the same chip, but at the beginning of the program few satisfactory high frequency combinations had been reported in the literature.

The choice of the R.C.A. type CA3005 monolithic integrated circuit was based on the versatility, availability and economy of the unit rather than on its absolute performance. The transistors in the CA3005 are not the state of the art. This is reflected in its unit retail price of less than three dollars. On the other hand, the CA3005 is very versatile for broadband amplification work since no collector load resistors are included. The user adds his own loads. Secondly, a variety of biasing networks is included and are selected by shorting certain of the TO-5 can's pins together. Four different combinations are available and complete specifications are given by the manufacturer for operation of each mode at three different supply voltage levels. This variety of biasing modes was important since it was desired to operate into specific load resistors and at the same time have low collector to emitter voltages.

Operation of the differential pair is described both from an analytical and from an empirical viewpoint in Reference (10), the RCA Linear Integrated Circuits Manual. These results may be summarized. The small signal, single-ended transconductance of the pair is 8 millimhos/milliamp at low frequencies. The current level referred to is the total current following through the pair, i.e., the current through the current source in the emitter leg. The current consumed in the biasing network for the current source is less than 1/2 milliamp and varies with the biasing mode. If the quiescent current through the emitter followers is added to these currents, total power consumption is obtained by multiplying by the supply voltage. The transconductance of the differential pair starts to fall off at a -6 db/octave above 50 MHz. The input and output impedances in the model of Figure 4.1 are frequency dependent. The output resistance R_o is typically 10,000 ohms at 1 MHz but falls to 2800 ohms at 40 MHz.

C_o is 4 picofarads at 1 MHz but rises to 7.6 picofarads at 40 MHz. All of these data are developed in the reference.

B. SENSE AMPLIFIER

The sense amplifier must amplify induced signals from the magnetic film to the logic levels employed in the system. The sense signal is in a noisy environment; thus strobing of the sense amplifier output is a necessity. The sense signal is induced in a balanced bit line and appears as a differential signal at the input terminals to the sense amplifier. Most noise, however, appears as a common mode signal and is rejected by the sense amplifier. Important design criteria for the amplifier are that the amplifier have a differential input, have good common mode rejection, and have the ability to strobe the output signal. Choice of system logic levels sets the required output levels for the amplifier.

Design criteria set by the requirement of limited power dissipation were the most challenging. Additional requirements are that the noise level of the amplifier be much less than the sense signal level and that the amplifier have adequate frequency response. The frequency response of the unit is important from two aspects. First, time delay of a signal passing through the amplifier is related to the phase shift of the amplifier. For a network characterized by poles and zeros in only the left half plane, phase shift β is directly related to the gain-frequency characteristics. Group delay for the network is $-d\beta/d\omega$. For example, if the amplifier frequency response falls off rapidly about some ω_o, then phase shift will change rapidly about ω_o also. The resulting time delay will increase. The net effect for a signal possessing frequency components up and above the break frequency of an amplifier is that the output waveform will be distorted due to dispersion. One effect of distortion is that the output peak will occur later in time than the input peak and the amplifier output will tend to "hang up" after the input has returned to zero. Phase shift is reduced by wide frequency response. Given an amplifier with a fixed gain-bandwidth product and characterized by a simple pole, the tradeoff is between a low dc gain, wideband amplifier which gives a certain peak output signal with little time delay, and a high gain, low bandwidth amplifier with a slightly greater peak output but much longer time delay. Slightly greater output is

obtained in the second case since the low frequency components dominate in the typical input waveform.

A second motivation to have a wideband, or flat, amplifier response is to prevent excessive amplification of low frequency noise signals. Most common mode signals present at the amplifier input will have lower frequency components than the sense signal. The base of the sense signal is about 10 nanoseconds long, whereas a typical common mode noise signal, the bit line drive pulse, will last 20-30 nanoseconds. Excessive response of the amplifier to low frequency signals makes the noise rejection problem more difficult.

Some circuits in the final design have their power supplies turned on and off to limit total dissipation, but it was not possible to do this with the sense amplifier. Thus power dissipation in the sense amplifier is a critical factor. There are eight sense amplifiers and each amplifier uses 80 milliwatts. The total power consumption is then 640 milliwatts for sense amplifiers alone. This is an appreciable portion of the 1000 milliwatt total dissipation allowed for the memory. Three stages are normally required for sense amplifiers of this general class. This means about 27 milliwatts per stage is allowed. Since the minimum reasonable voltage supply is ± 3 volts, 4.5 milliamps per stage is allowed. At this point the importance of logic levels can be seen. High logic levels require much more dissipation in the sense amplifier. Perhaps the lowest standard levels are those of emitter coupled logic. These levels are separated by the drop across the emitter-base junction of a silicon transistor, or, about 750 millivolts. The absolute magnitude of the levels depends on the supply voltage levels to a logic gate. If 0 and -5.2 are used with Motorola's MECL logic, -750 millivolts and -1.55 volts are typical logical levels. These levels were used throughout the circuit design for this program.

1. Bit Line

The bit line is the transmission line which carries the induced voltages from the switched film to the terminals of the sense amplifier. The attenuation in this transmission line should be small since signal levels are very low and induced noise can become a problem. Design of this line must take into consideration fabrication problems. Typically there must be a compromise between low loss characteristics and ease of fabrication.

A first order analysis has been made of typical transmission lines in evaporated film structures. When discrete transistors are used for the sense amplifier, the physical size of the amplifier will be too large for the amplifier to be mounted close to the bit line. Some fan out of the transmission lines will be necessary. In the present system, this fan out was accomplished on the printed circuit board rather than inside the evaporated structure. Thus there are two transmission lines between the induced signal and the sense amplifier. The line on the printed circuit board is characterized by low loss but a relatively high characteristic impedance. The evaporated lines are low impedance, lossy lines. These differences result from the greatly different dimensions of the two lines. The differences in characteristic impedance will result in some reflection of the high frequency components of signals traveling down the lines. These reflections will be ignored since they are characteristic of the prototype design only and not of an all evaporated and integrated structure. Complete analysis of the bit line is carried out in Section II.

Analysis of the bit line indicates that, as far as the induced sense signal is concerned, the line can be represented as having a frequency dependent transfer characteristic and a certain output resistance. The output resistance is a function only of the resistivity and size of the bit line conductors. It represents a loss at all frequencies. Above the cutoff frequency of the line there is additional loss expressed by the declining magnitude of the transfer function. The transmission line can thus be characterized as a 3 ohm, 400 MHz line, for example. The output resistance of the line will form a voltage divider with the input resistance of the sense amplifier. The input resistance to the amplifier happens to be 22 ohms. Thus $3/(22 + 3) = 12\%$ of the sense signal is lost to conductor resistivity. Additional portions of the signal are lost to the finite bandwidth of the line. Design of the sense amplifier is based on an input signal at the amplifier terminals of 2.5 or 3 millivolts peak and lasting about 10 nanoseconds. This is approximately 88% of the 3.5 mv peak induced switching voltage estimated in Section II. For actual evaluation of the amplifier, such a signal is easily obtained by differentiating the rising edge from a fast rise time pulse generator. The actual signal used is shown in Figure 4.3.

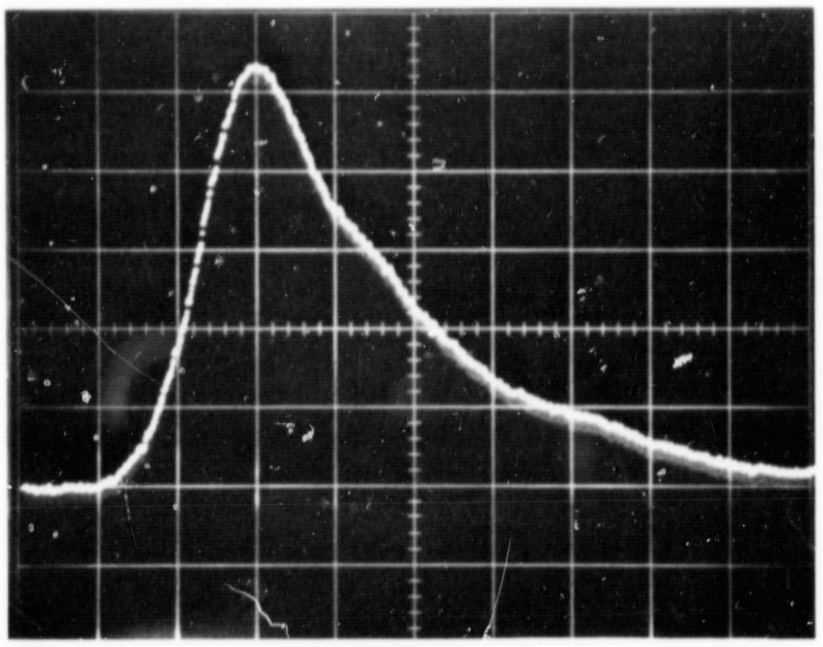


Figure 4.3 Excitation signal for sense amplifier. Horizontal scale: 2 nanoseconds/division; vertical scale: arbitrary units.

2. Offset Problem

The general requirements of the sense amplifier have been outlined in the preceding paragraphs. Another problem, peculiar to integrated circuits operating with strict power requirements, is low frequency noise or drift. This problem is important because the traditional solutions of coupling capacitors, or large collector to emitter voltages to absorb changes in operating point, can not be easily applied. Extensive use of coupling capacitors is ruled out by chip area limitations. Relatively large capacitors would be needed to couple stages without excessive signal loss. Large collector to emitter voltages (say, three or four volts) would solve the problem at the expense of wasted power.

The magnitude of the problem can be easily demonstrated. The first two stages of the sense amplifier have a pulse gain of 200 and a low frequency gain of about 1000. These are typical numbers for a variety of circuits considered. The sense signal at the input terminals is 3 millivolts, giving a 600 millivolt output swing. However, offset between the base-emitter voltages of the input differential pair is typically 3 millivolts. Thus the differential output signal due to offset is 3 volts, or five times that of the sense signal. This could not be tolerated in a direct coupled system.

Plausible solutions include a better match between the input transistors, applying an external bias signal which cancels the offset, and use of capacitors. Since offset is a function of manufacturing tolerances as much as temperature differences, and these tolerances are constantly being improved, it was felt reasonable to use selected integrated circuits for the input stages. The manufacturer, R.C.A., markets a device identical to the CA3005 except for tighter offset tolerances. This device, the CA3006, was used for the input stages. It has a typical offset voltage of 1 millivolt, compared to the 3 millivolts typical of the CA3005.

Cancellation of the offset voltage by an external bias signal was not felt to be reasonable in a large system and, in addition, would be difficult since the offset varies with time. The offset voltage can be represented as a generator attached to the input of an ideal amplifier. This generator would have strong frequency components up to several hertz.

The only complete solution to the offset problem involves the use of capacitors. Capacitors may be used as coupling elements between stages or as feedback elements. When used as a coupling element the capacitor

reduces the low frequency gain of the amplifier. An equivalent circuit is shown in Figure 4.4. Resistor R_b is the biasing resistor for stage N + 1 and offers a dc return path to ground for any bias currents. R_o and R_i are the small signal output and input resistances of the amplifiers. Let the parallel resistance of R_b and R_i be represented by R. Then,

$$R = R_b R_i / (R_b + R_i)$$

and the transfer ratio E_o/E_s is easily shown to be

$$\frac{E_o}{E_s} = \frac{R}{R + R_o} \quad \frac{s}{s + 1/C(R + R_o)} \; .$$

The representation of the amplifier as a voltage source is reasonable since the output stage of the module shown in Figure 4.2 is an emitter follower. The output impedance R_o of the emitter follower is essentially the base resistance of the 2N918 - several hundred ohms - since the collector load resistor is about 2000 ohms and the emitter resistor is several kilohms. R_i for the CA3005 is about 2000 ohms and it is reasonable to assume that the equivalent resistance of the biasing network, i.e., R_b, can be made large compared to 2000 ohms. The low frequency pole is thus located at about

$$s = - 1/2000\ C \quad .$$

If C is chosen as 100 picofarads, the pole is at 800 kHz. A gain-frequency plot is sketched in Figure 4.5 for the coupling network.

If capacitors are used to couple stages, two resistors, shown simply as R_b above, are needed for each side of the differential amplifier in addition to those shown in Figure 4.2. These are used to correctly bias the differential pair of stage N + 1. If direct coupling could be used, the input to one stage would be tied directly to the output from the preceding stage.

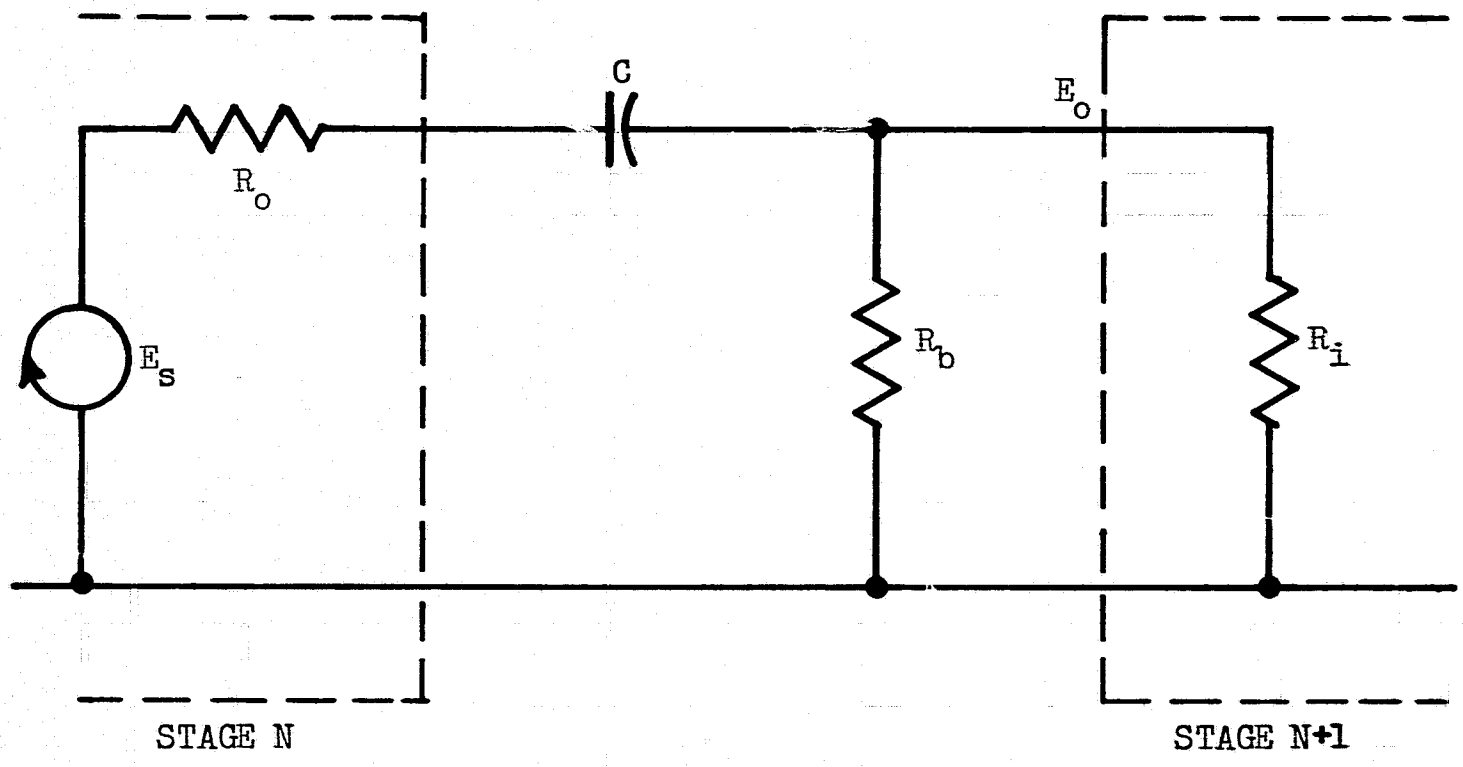


Figure 4.4 Equivalent circuit for capacitor coupled amplifier stages

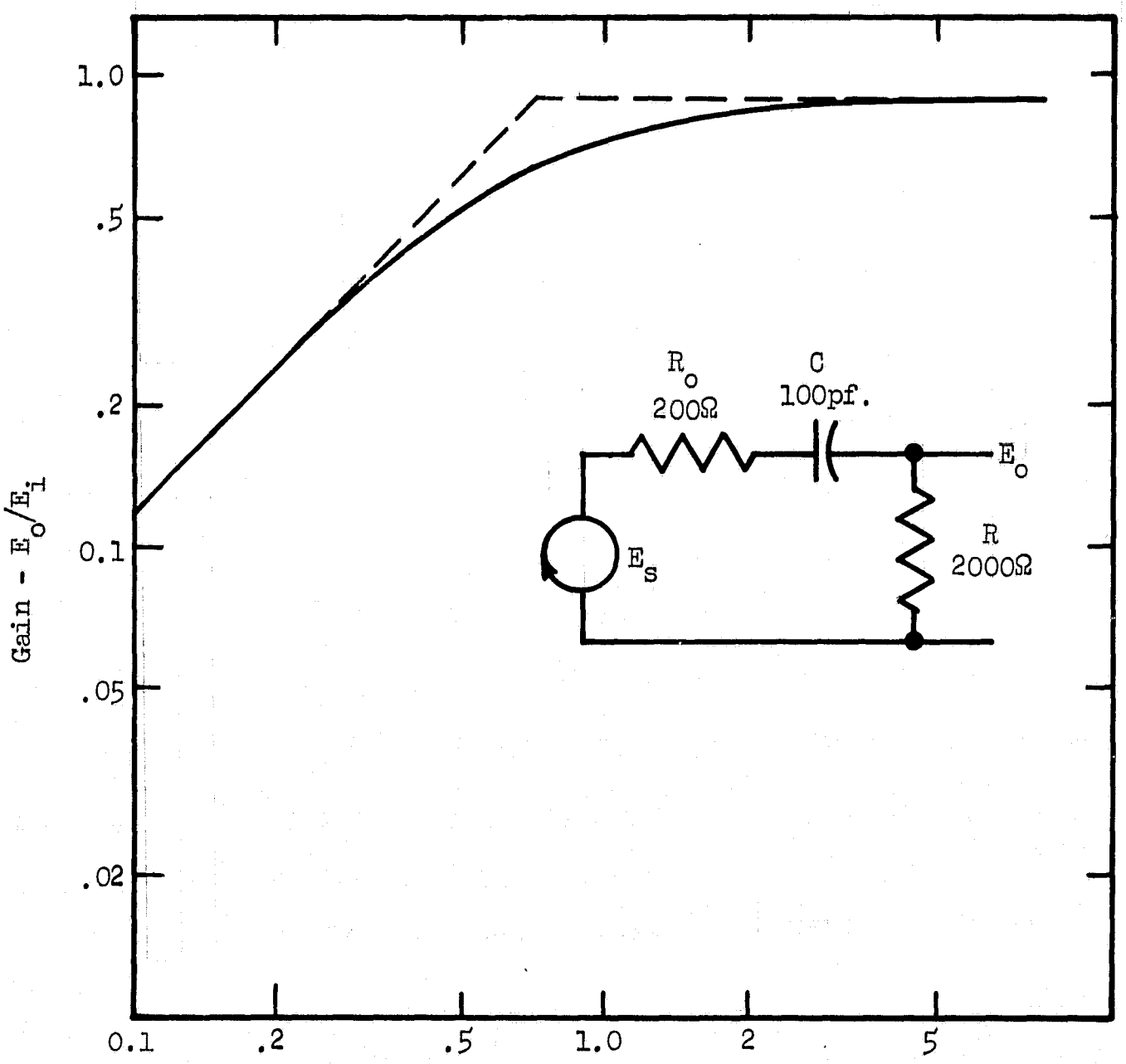


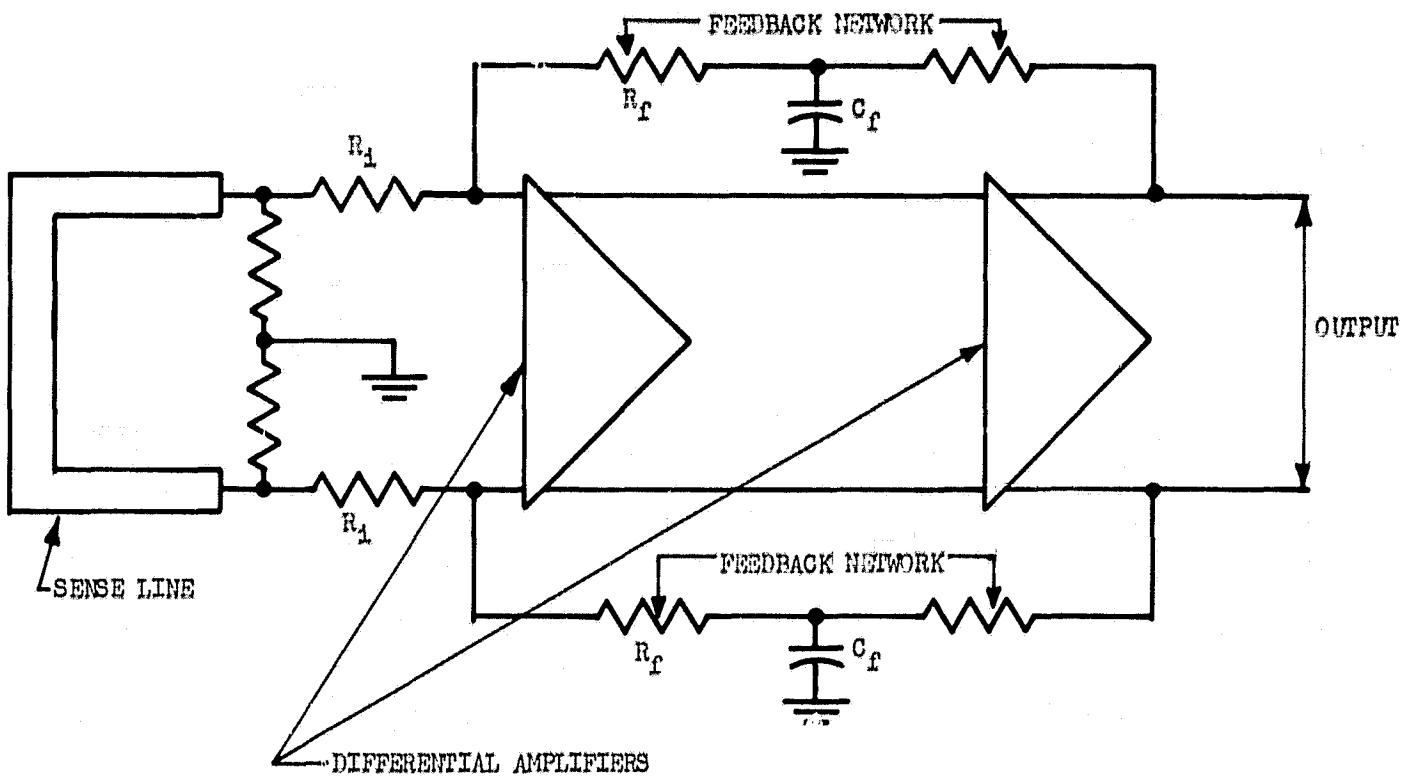
Figure 4.5 Gain-frequency plot for capacitor coupling network

A series R, shunt C, type of feedback network can be used around the direct coupled amplifier to solve the offset problem. The cutoff frequency of the network would be relatively low so that the mid-band gain of the amplifier would not be affected. A schematic representation of the scheme is given in Figure 4.6 which shows representative gain-frequency plots for the open and closed loop amplifier. It is seen that the pole of the feedback network introduces a dipole in the closed loop response. The exact magnitude and location of the dipole, i.e., the feedback ratio and the location of the feedback pole, will be discussed later.

The significant factor is that the feedback network is easier to fabricate than the coupling capacitor network and will likely occupy less chip area. Reference (11) gives models for typical monolithic capacitors. These models show stray capacitances from each terminal to ground. It is these parasitic capacitances which cause signal losses in coupling applications, but which are unimportant in the feedback application since one terminal of the capacitor is grounded. The feedback network is easier to fabricate in the sense that the losses normally encountered in monolithic capacitors do not adversely affect performance.

Design of the feedback network in monolithic form is outlined in Appendix F. The transfer characteristics of a typical line 50 mil long and 3 mil wide have been computed for several excitation frequencies. These are shown in Figure 4.7. The distributed line does not behave like a simple R-C network; yet it is still useful as a feedback element. Care needs to be taken in the design of the feedback loop, but once the loop is designed, the fabrication problems should be less since parasitic capacitances are unimportant.

There exists another possible use of capacitors in a feedback scheme. This involves the use of active elements to multiply the apparent value of a capacitor so that the time constant in the feedback network is more easily achieved. The advantage of this method is that the resulting transfer function is characterized by a rational expression in the complex frequency variable s. This is in contrast to the previous method using a distributed R-C transmission line. The disadvantage is that the capacitor must have both terminals above ground. This type of capacitor is more difficult to fabricate than the capacitor with one terminal grounded; that is, the resulting capacitor differs from the ideal more when both terminals are above signal ground.



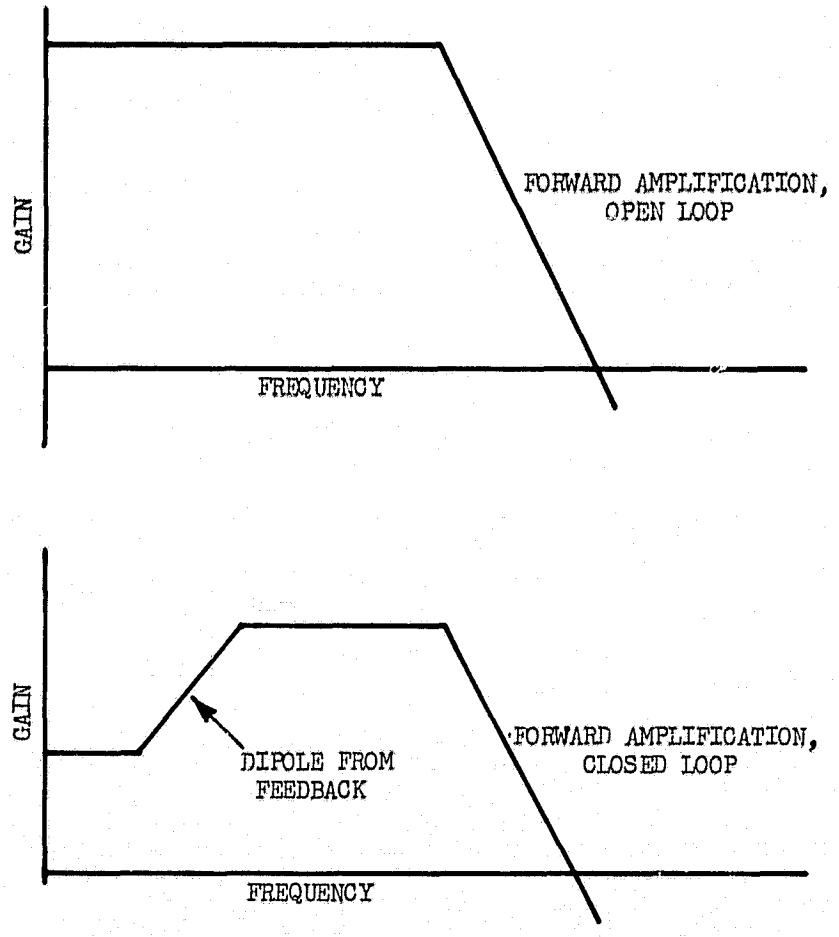


Figure 4.6 Block diagram and gain-frequency plots for direct coupled feedback amplifier

Figure 4.7

Summary of Calculations for a Typical Lossy Line

Radian Excitation Frequency	Characteristic Impedance	$\alpha = \beta$	Wavelength in Line	V_{out}/V_{in}
0				0.0385
10^6	10,700 @ -45°	0.0132	475 mils	0.027 @ -56°
10^7	3,380 @ -45°	0.0418	150 mils	0.019 @ -80°
10^8	1,070 @ -45°	0.132	47 mils	0.0003 @ -730°

Consider the schematic of Figure 4.8. The circuit would be constructed as a differential pair; here only one side of the pair has been shown. The differential input impedance of the amplifier is shown as R_2. The output admittance of the amplifier has been ignored. Straightforward node analysis yields the voltage transfer function e_o/e_i.

$$\frac{e_o}{e_i} = \frac{-g_m R_3}{R_1} \frac{\frac{1}{C(1 + g_m R_3)}}{s + \frac{R_1 + R_2}{R_1 R_2} \frac{1}{C(1 + g_m R_3)}}$$

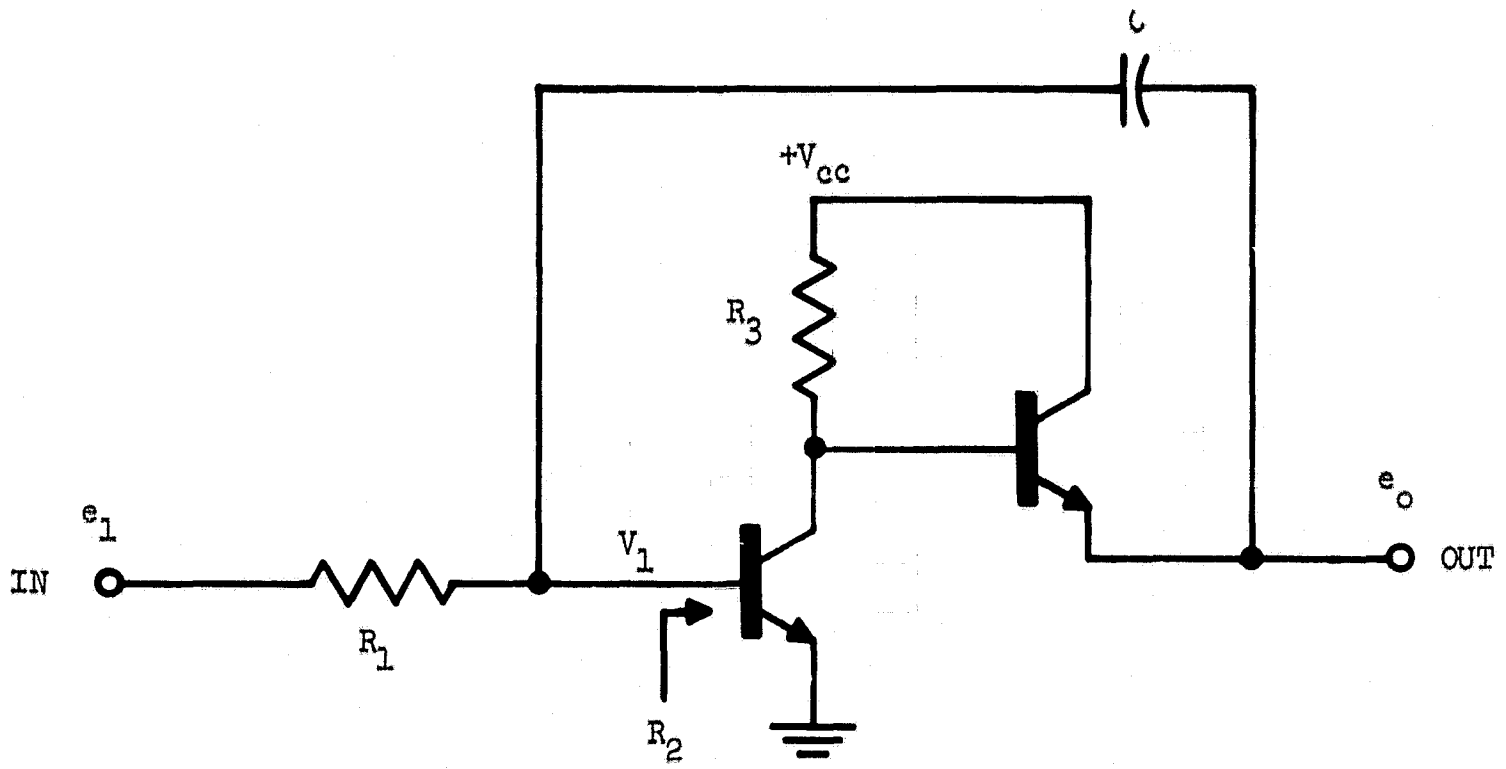
It is seen that the apparent value of the capacitance has been increased by the factor $(1 + g_m R_3)$. To give some feeling for the numbers, assume that g_m = 40 millimohos, R_1 = 10 kilohms, R_2 = 10 kilohms (this is easily achieved using input emitter followers), R_3 = 5 kilohms and C = 20 picofarads, a very reasonable value. The equivalent time constant of the network is then

$$RC = (5 \times 10^3)\ (20 \times 10^{-12})\ (1 + 200) = 20 \times 10^{-6} \quad .$$

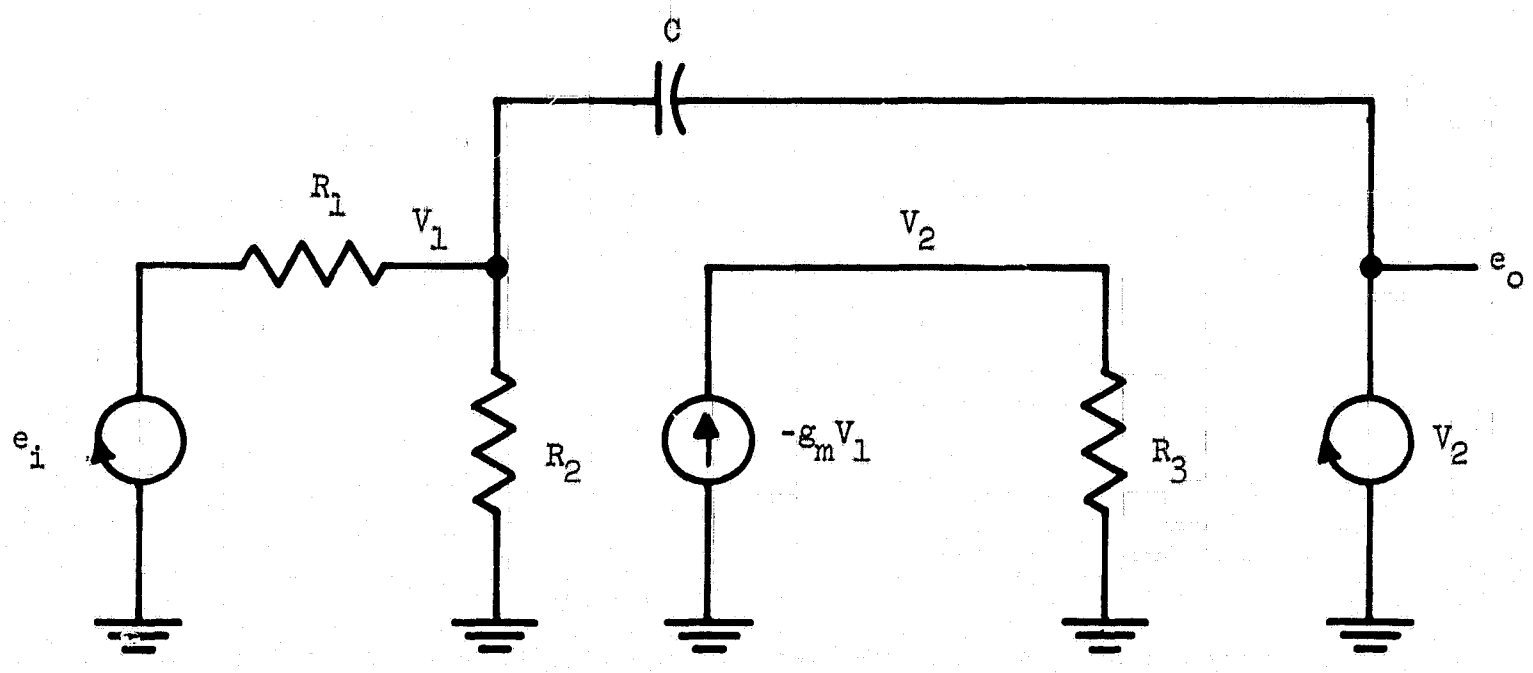
The corresponding cutoff frequency is only 8 kHz. This scheme was not used in the prototype because of the additional complexity of the circuitry. This would not be the case when an all integrated structure is used.

3. Small Signal Performance

The requirements for the small signal performance of the sense amplifier will be briefly reviewed. The sense signal amplitude at the input terminals is about 2.5 millivolts. The logic levels of emitter coupled logic differ by 750 millivolts. It follows that a pulse gain of roughly 300 is needed. Pulse gain is specified rather than mid-band gain since the sense signal spectrum is far wider than the bandpass of the amplifier. Thus the pulse gain is far less than the mid-band gain of the amplifier, typically by a factor of 5-10 for the particular sense signal and the CA3005. Analysis of a two stage amplifier employing CA3005's was made using the Fourier series computer program, described in Appendix D. A computer run was made with each stage characterized by a simple pole at 10 MHz and a dc gain of 40. The output from a 5 millivolt switching signal into a 100 MHz bit line was



(a)



(b)

Figure 4.8 A method to increase effective capacitance. Part (a) is a circuit which increases the effective value of C in the transfer function. Part (b) shows an equivalent circuit for computing the transfer function

2.47 millivolts peak. The peak output from the two stage amplifier was 450 millivolts. The pulse gain was 180 whereas the dc gain was 1600, about nine times greater. The pulse gain per stage was a factor of three lower than the dc gain. Actual pulse gains measured are about 20% lower than the predicted gains.

When the bandpass of the amplifier and the signal spectrum are compared, it is somewhat surprising that anything is obtained from the amplifier. The signal has significant frequency components up to ten times the cutoff frequency of the amplifier. The primary effects of this narrowband amplification are that the pulse gain is less than the low frequency gain and the output peak appears to be delayed considerably from the input peak. For the present system, this delay is about 30 nanoseconds. The output appears to be an integration of the input, with the output "hanging up" for some time after the input signal has returned to zero. These characteristics will be seen in the actual waveforms of the amplifier. Again it should be emphasized that the R.C.A. CA3005 is not the most sophisticated integrated circuit on the market. It was used in this design because of its flexibility and economy. Improved frequency response of the integrated circuits would allow more freedom in the design of the feedback network.

The total amplification needs of the sense amplifier are easily satisfied by a three stage amplifier. It would be difficult to accomplish the amplification and the necessary level shifting in only two stages. The sense amplifier may be divided into two parts, the preamplifier and the output stage. The output stage can also include any strobing circuitry necessary. The preamplifier has a pulse gain of 150-200, with the output stage adding the additional factor of two. The output stage is similar in design to a standard MECL logic gate. It was not constructed but a typical design is illustrated later. The output stage was not considered to be the difficult portion of the sense amplifier.

The preamplifier was constructed and evaluated. It will be described completely. The output swing of the preamplifier is several hundred millivolts, so the signal is easily observed on an oscilloscope. In the present system, the output stage would be constructed on separate printed circuit cards from the preamplifier and would be connected by coaxial cable. Therefore a low impedance output was accomplished with double emitter followers. Were a complete system to be built, the output stage would be constructed as

an extension to the preamplifier and the additional emitter followers could be omitted. In the present system the output stage must be coupled through capacitors since the offset stabilizing loop only extends around the preamplifier. In a complete system, however, the stabilizing loop would be carried around the output stage also, and the coupling capacitors eliminated. These differences are sketched in Figure 4.9. The remainder of the discussion will be devoted to the two stage preamplifier with feedback, but the principles of design apply also to a complete three stage amplifier with feedback.

The small signal performance for the individual stages is most easily described in the frequency domain. The measured response for the circuit of Figure 4.2 is given in Figure 4.10. It agrees essentially with the response predicted by the model of Figure 4.1 with C_o = 8.8 picofarads, a g_m of 21 millimhos, and a load resistance of 1800 ohms. The output resistance and feedback capacitance of Figure 4.1 can be ignored. This model gives a low frequency gain of 37.8 and a pole at 10 MHz. The measured response also showed a second pole in the neighborhood of 50 MHz due to roll-off of the transconductance.

The open loop performance of the preamplifier is the product of two of these stages. The closed loop performance will now be described. A glance at the frequency response of the individual stages indicates that very little resistive feedback can be applied around the preamplifier. In terms of gain-frequency plots, stability is assured if the slope of the gain plot at 0 db is equal to or less than -6 db/octave. The total open loop gain, the preamplifier in series with the feedback element, must satisfy this criterion. It is easily seen that the amount of feedback is limited. An even more serious objection is that the mid-band closed loop gain of the amplifier is reduced by the feedback. A simple way to assure maximum mid-band gain, and stability at the same time, is to reshape the gain-frequency plot for the open loop by a dominant low frequency pole in the feedback loop. This new pole rolls off the open loop gain at a low frequency, giving the gain-frequency plot a -6 db/octave slope at 0 db. Furthermore the mid-band gain of the closed loop amplifier is not seriously affected since the feedback ratio, β, is now small at these frequencies. A sketch of the gain-frequency relationship for the forward amplifier and for the open loop system is given in Figure 4.11. It is seen how the feedback pole dominates the open loop gain-frequency characteristic.

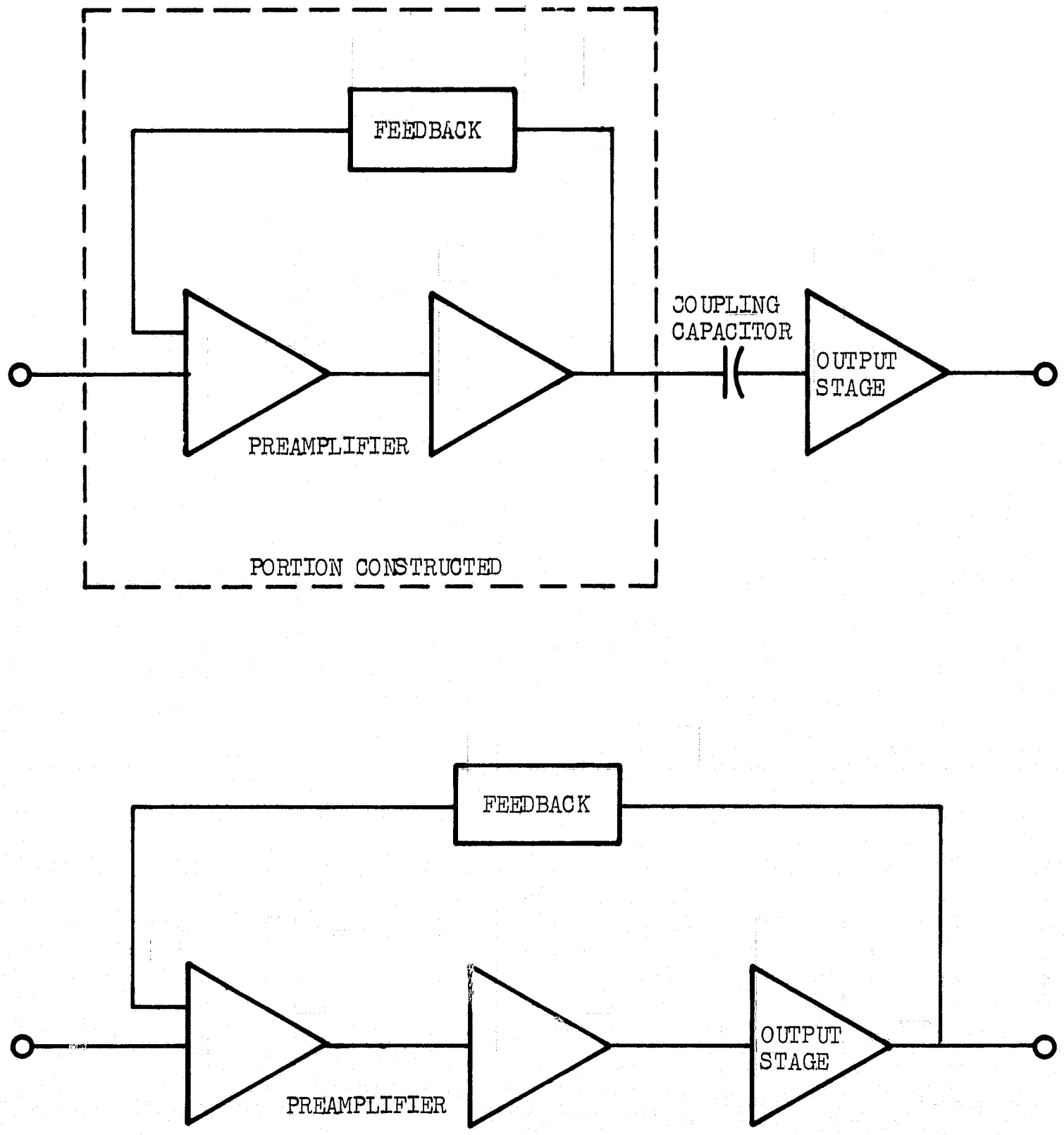


Figure 4.9 Comparison of sense preamplifier constructed (upper), and a complete amplifier as would be used in an operating system (lower). Each stage is a basic circuit module

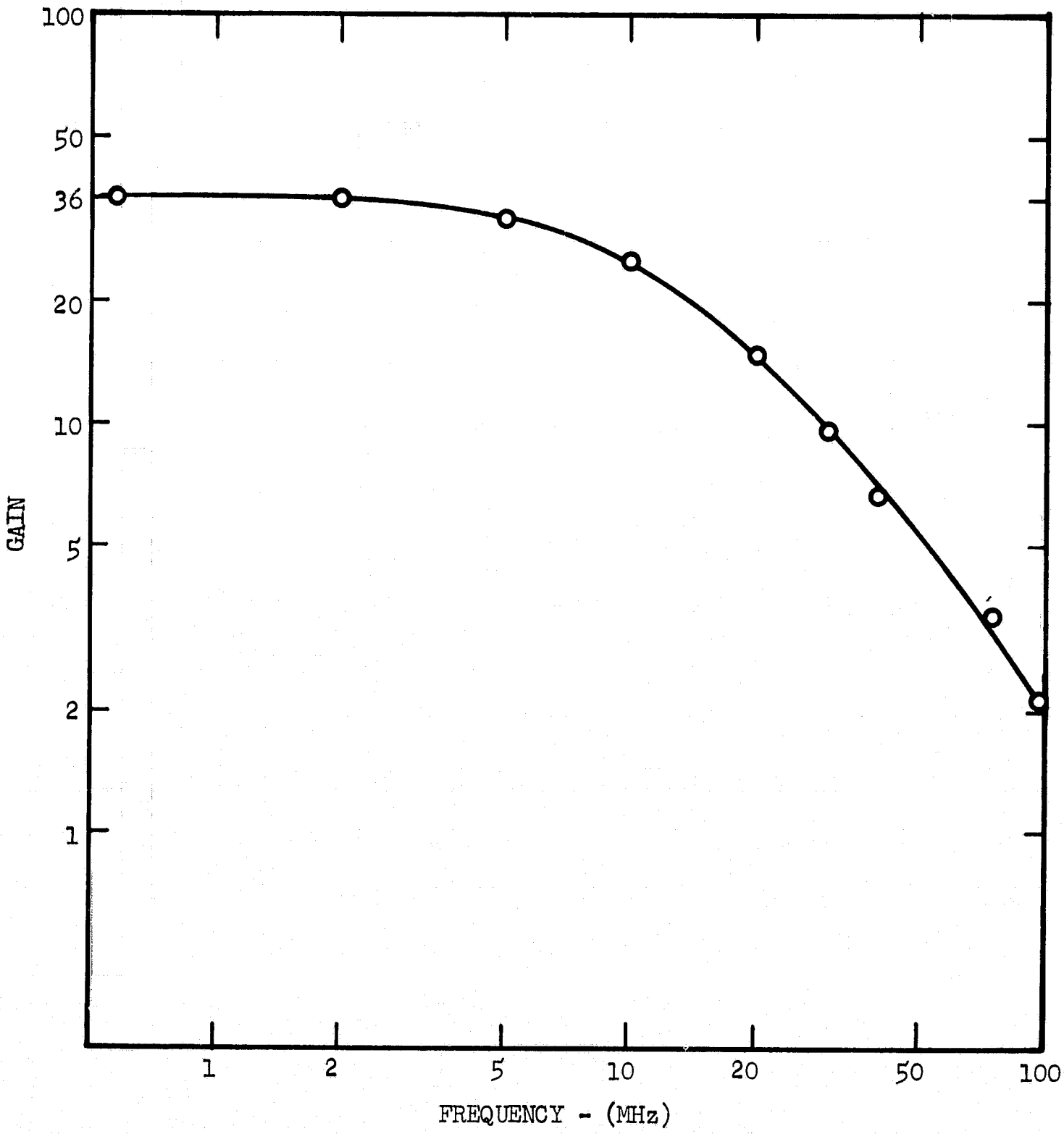


Figure 4.10 Measured response for the basic circuit module with 2.7 milliamps total current, 1800 ohm load resistors, and ±3 volt supplies

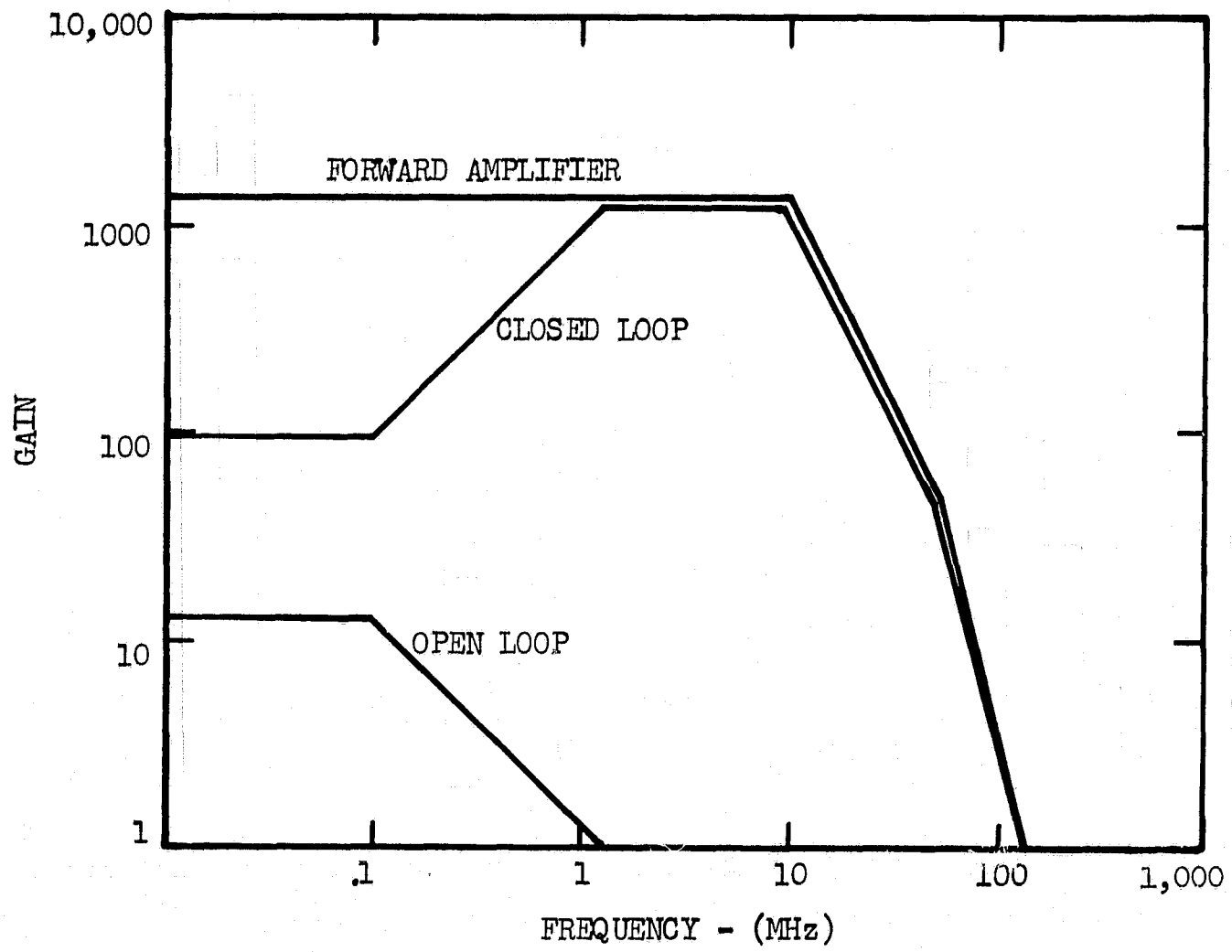


Figure 4.11 Asymptotic gain-frequency plots for the sense preamplifier with feedback dominated by a pole at 100 kHz. The two basic circuit modules comprise the forward amplifier. The feedback cascaded with the forward amplifier yields the open loop. When the loop is closed, the output/input response is the closed loop

This scheme is completely general and may be used around any amplifier. Success depends on the ease of fabrication of the low frequency pole in the feedback element. Given a maximum R-C product which can be fabricated, it is necessary that the pole synthesized with this R-C be at a much lower frequency than the first pole of the forward amplifier. In the present case this means the feedback pole must be at a much lower frequency than 10 MHz. Thus, the wider bandwidth amplifier will require a lower R-C product in the feedback loop to insure stability. In general, the greater the reduction in gain at dc because of the feedback, i.e., the greater the loop gain, the greater the R-C product required. Once stability is assured, the resulting closed loop gain-frequency characteristic can be examined. The closed loop frequency response will have a zero at the location of the feedback pole and will rise at a 6 db/octave rate until it intersects the forward gain of the amplifier. If the feedback pole is too close to the first pole of the forward amplifier, some peaking may occur in the closed loop response. Both the stability and the frequency response of the closed loop amplifier are most easily determined from a root-locus plot. The plot for the preamplifier constructed is given in the next section (Figure 4.14). The only generalization that may be made is that this feedback scheme is useful when the R-C product, which can be easily fabricated, results in a pole lower than the required low frequency cutoff of the closed loop and considerably lower than the first pole of the forward amplifier.

4. Circuit Details and Performance

A circuit diagram for the preamplifier is given in Figure 4.12. Each differential amplifier is an integrated circuit; the remaining components are discrete. Each component is identified on the photograph in Figure 4.13. The feedback network is the R-C "T" formed by C_1, R_5, R_{17}, and by C_2, R_6, R_{18}. Each "T" serves one side of the differential amplifier. The feedback ratio at dc is determined by

$$\beta = \frac{R_{15}}{R_{13}} \quad \frac{R_3}{R_5 + R_{17}} \quad .$$

In the present case this is 0.0055 = 1/180. The dc gain of the amplifier is about $1/\beta$, so any voltage offset appearing at the input terminals will be multiplied by 180. The observed offset at the output was between 200

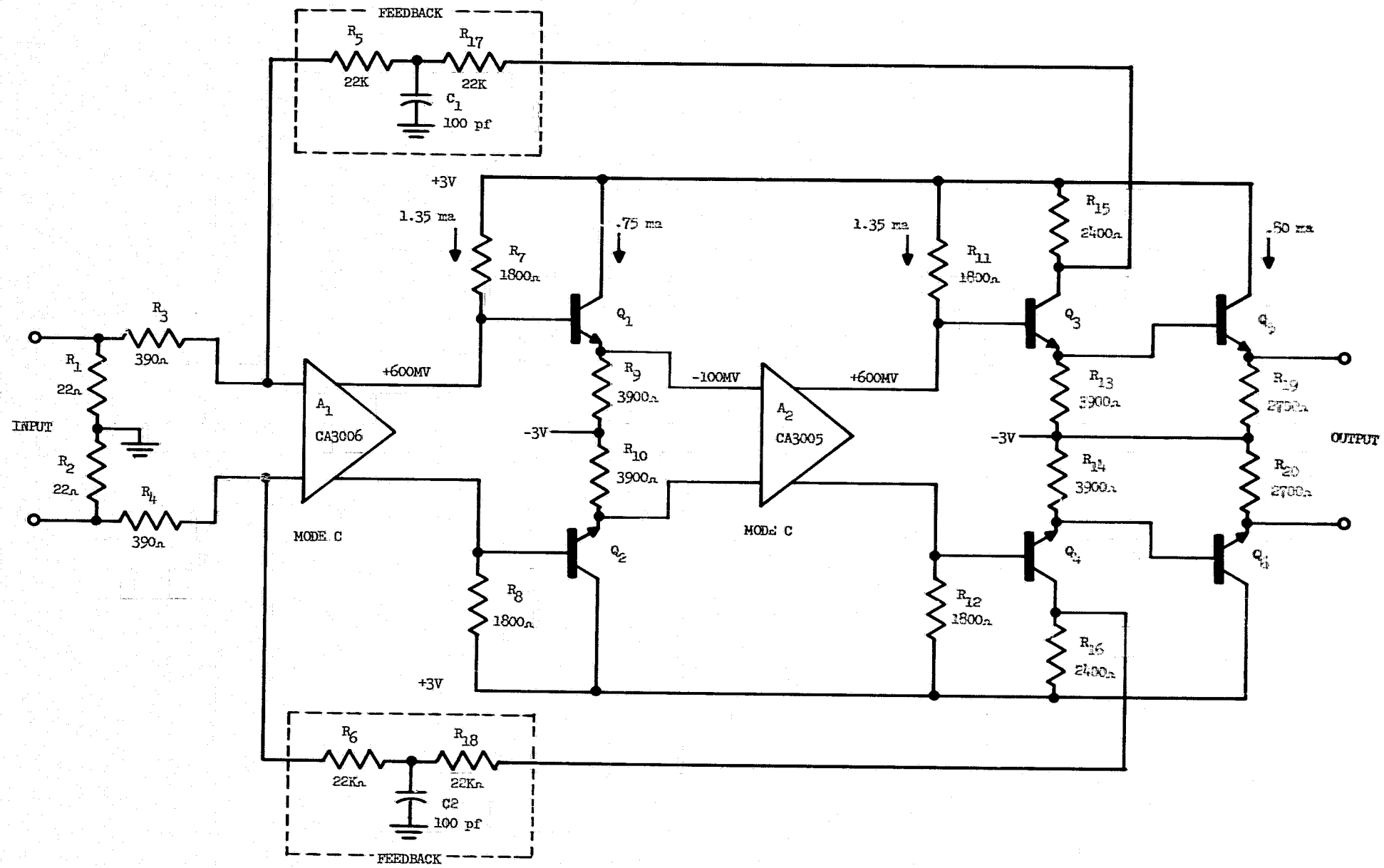


Figure 4.12 Schematic for sense preamplifier. Currents and voltages are quiescent levels

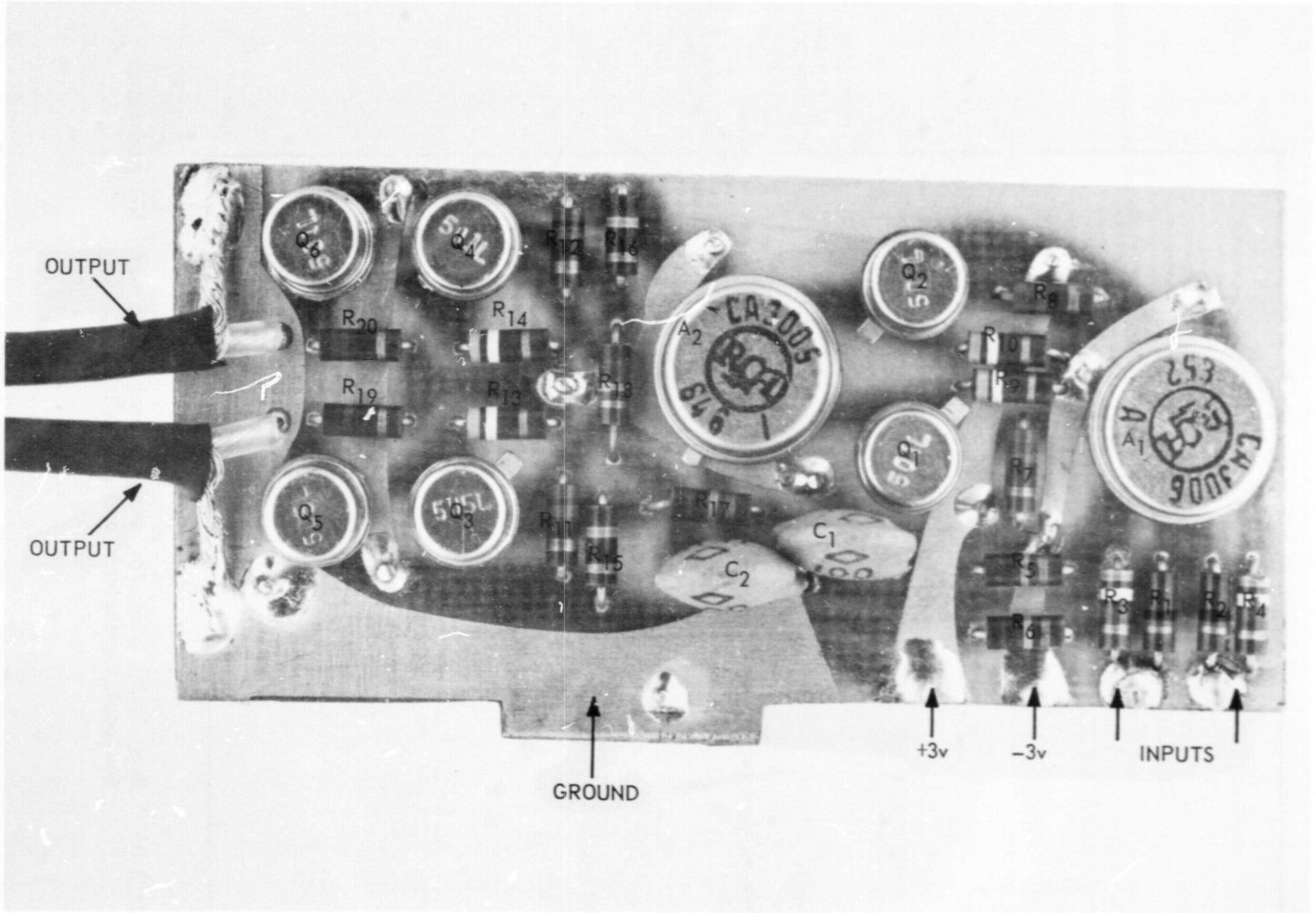


Figure 4.13 Parts identification for sense preamplifier board

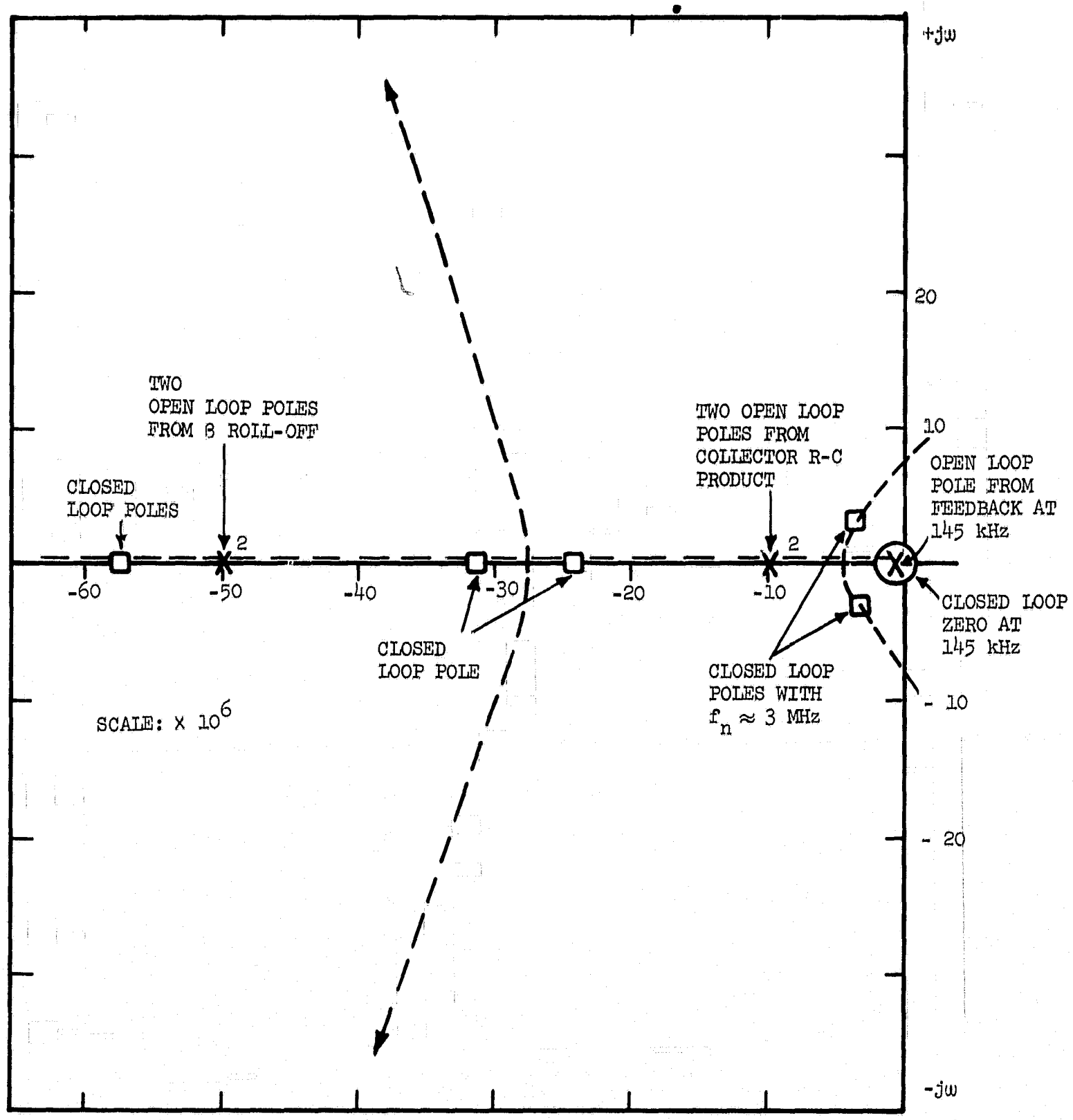


Figure 4.14 Root locus plot for sense preamplifier with 100 picofarad feedback capacitors and $\beta = 1/180$

and 300 millivolts, indicating that the offset of the CA3006 was a little over 1 millivolt.

The design of the amplifier is very straightforward. R_1 and R_2 are terminating resistors for the bit line. The value of these resistors is limited by the common mode voltage developed across them by the bit current during the WRITE operation. The amplifier can only stand a few hundred millivolts of common mode voltage since the collector-base quiescent voltage of the input stage is 600 millivolts. R_5 and R_{17} were chosen to give the desired low frequency pole with C_1. The value of C_1 was arbitrarily set at 100 picofarads. Larger values for C_1 would result in a lower frequency pole for the feedback. The location of the feedback pole is given by the parallel resistance of R_5 and R_{17} combined with C_1.

$$f_c = (R_5 + R_{17})/2\pi R_5 R_{17} C_1$$

This is the pole of the voltage transfer ratio. R_3 is then chosen to give the desired feedback ratio.

Once the open loop characteristics of the forward amplifier are known, the feedback loop is designed with the lowest frequency pole allowed by the fabrication process. The evaluation of the closed loop amplifier may be made with either Bode plots or with root locus plots. The root locus plot for the present amplifier is given in Figure 4.14. The feedback pole is at 145 kHz. The open loop gain of the forward amplifier is 1200. The location of the closed loop poles is given for $\beta = 1/180$. It is seen that the amplifier constructed has complex poles with rather light damping. This was done to check the design method since relatively small errors or parasitic feedback would lead to instability. No instability was observed.

The quiescent voltages and currents are given on the schematic of Figure 4.12. The total power consumption for the preamplifier is 6 volts x 10 milliamps, or, 60 milliwatts. The emitter followers are operated at about the minimum current without excessive signal loss. Since the current gain for the transistors falls off for quiescent currents less than 1 milliamp, the emitter follower becomes less effective at low quiescent current levels. The integrated circuit amplifiers are operated at 2.7 milliamps total collector current in what the manufacturer refers to as "Mode C"

biasing. This biasing mode has the advantage of maintaining constant the total collector current over the temperature range from -55 degrees C to +125 degrees C. This is achieved through the use of temperature compensating diodes in the constant current sink for the amplifier. An additional advantage of this particular biasing mode is that the transconductance per milliwatt of dissipation is one of the highest available. This ratio of transconductance per milliwatt is a useful figure of merit. For Mode C biasing with ±3 volt supplies, it is 1.25 millimhos per milliwatt. It is desirable to have a high transconductance to dissipation ratio at a relatively high current level. This will be explained in the following discussion.

Direct coupling between the stages requires a fixed quiescent drop across the collector load resistors. This drop is the supply voltage minus the desired output quiescent level, plus the emitter-base drop of the emitter followers. Refer to Figure 4.2 again. The quiescent collector voltage level is $V_s - I_o R_L/2$, for a balanced amplifier. Let this fixed quiescent drop be V_d.

$$V_d = I_o R_L/2$$

The power consumption for the circuit, neglecting the power consumption of the constant current sink biasing network, is

$$P = 2 I_o V_s$$

for balanced voltage supplies. The voltage gain of the circuit at low frequencies is

$$V.G. = g_m R_L \quad .$$

Substituting,

$$V.G. = g_m(2V_d/I_o) = 2V_d g_m(2V_s/P)$$

$$V.G. = 4V_d V_s (g_m/P)$$

Given a supply voltage, the drop V_d is fixed in order to achieve coupling. These results follow. Given a supply voltage, choose the biasing mode with the highest g_m/P ratio, if the resulting gain-bandwidth product is satisfactory. Remember that the gain-bandwidth product is g_m/C_o for these units. Since g_m is related to I_o by the constant 8 millimhos/milliamp, it is desirable to have a good g_m/P ratio at a high current level.

If the supply voltage is to be chosen, the voltage gain is merely

$$V.G. = 4\ V_d V_s (g_m/2\ V_s I_o) = 16\ V_d$$

since $g_m = 8\ I_o$ millimhos, where I_o is expressed in milliamps. This expression has been verified since the measured dc gain is 36 and the voltage drop across the load resistors is about 2.25 volts. The choice of supply voltage was made on the basis that since three stages were necessary, and the total gain required is known, the voltage gain per stage can be determined. This fixed the supply voltage at 3 volts, the nearest "standard" voltage. If the supply voltage can be chosen at random, the choice should be studied with great care using the above principles. Total amplifier voltage gain could be expressed as a function of total power consumption for amplifiers consisting of one, two, three, ... stages. For most realistic conclusions, the voltage gain used should be the pulse gain rather than the low frequency gain. Thus each possible amplifier would have to be evaluated using the Fourier series program. Weighting could be given to the increase in delay caused by low bandwidths. If this study were made, a truly "optimum" selection of operating points could be made.

The procedure for selecting the operating point can be summarized as follows:

1. On a supply voltage versus supply current graph, plot constant power consumption hyperbolas.

2. For a single stage amplifier determine the pulse gain with the Fourier series program for a variety of supply voltages and currents. The pulse gain alone, or in combination with signal delay, can be used as an

an index of performance.

3. For selected points on the supply voltage - current graph note the index of performance and connect similar indices, thus forming contours of the index.

4. Form similar graphs for two stage amplifiers, three stage amplifiers, etc. From the entire set of graphs select that operating point (supply voltage, supply current, and number of stages) which meets the minimum performance requirements with a minimum of power dissipation.

The measured gain-frequency characteristic of the closed loop amplifier is shown in Figure 4.15. The resonant peak at 3 MHz is the result of the feedback path. A lower frequency pole in the feedback path would remove this peak. The primary effect of this peak is undershoot in response to the impulse-like sense signal. The response of the amplifier for a typical excitation signal is given in Figure 4.16. The excitation signal was that of Figure 4.3 with an amplitude of 2 millivolts. This signal is formed by differentiating a pulse from a standard pulse generator. This differentiation results in a positive going signal at one edge of the pulse and a negative going signal at the other edge. Thus Figure 4.16a shows the amplifier response to both a negative and a positive signal. Figure 4.16b shows the same amplifier and excitation signal but with the 100 picofarad feedback capacitor replaced by a 300 picofarad capacitor. The improvement in undershoot is obvious. In all other tests the 100 picofarad capacitor is used. Figure 4.17 gives a detail view of one of the output signals from the preamplifier. Figure 4.18 shows the output when the amplifier is overdriven. It is seen that the amplifier limits for inputs slightly greater than the expected sense signal.

Besides differential amplification, the other important criterion for the preamplifier is common mode rejection. This is necessary because the bit current and induced noise from the word current will result in a common mode voltage at the input terminals. The bit current will result also in a differential voltage due to any unbalances in the bit lines or the terminations, but the differential signal should be relatively small. The word current also introduces a common mode signal. Whereas the bit current interference can be eliminated by strobing the amplifier output, the word current signal cannot, since it occurs at essentially the same time as the sense signal (the sense signal is the induced signal from the magnetic film switching under the influence of the word current). Ideally

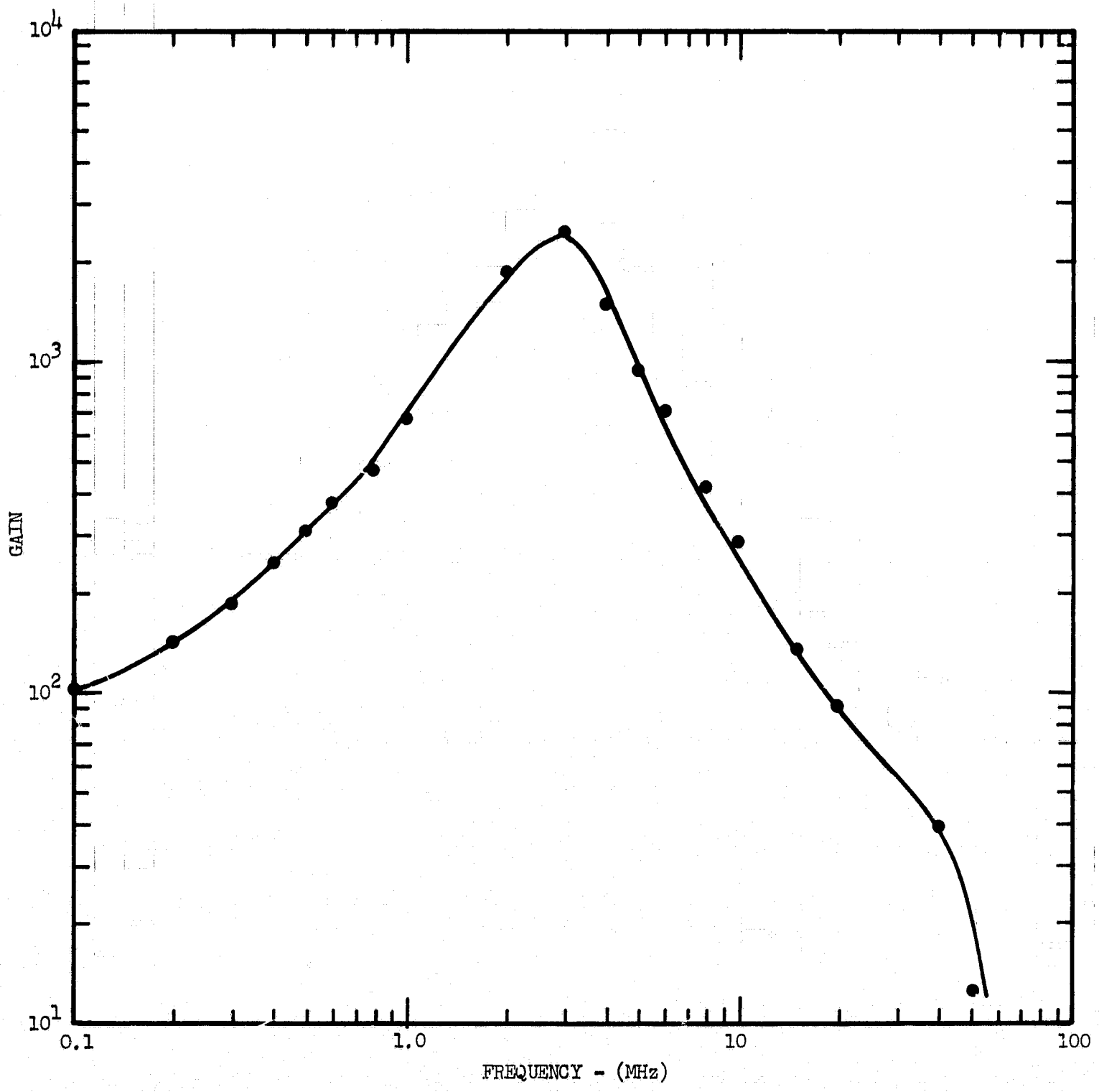
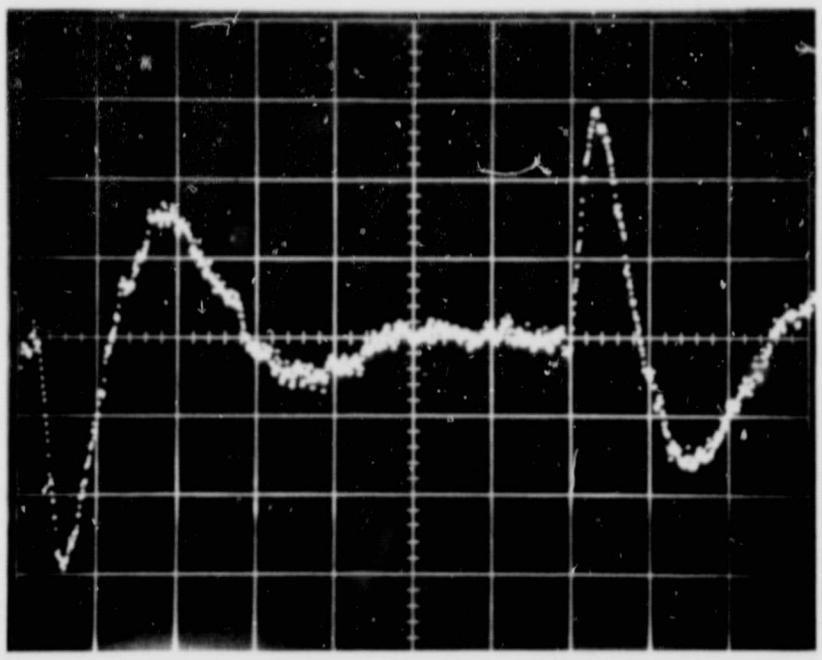
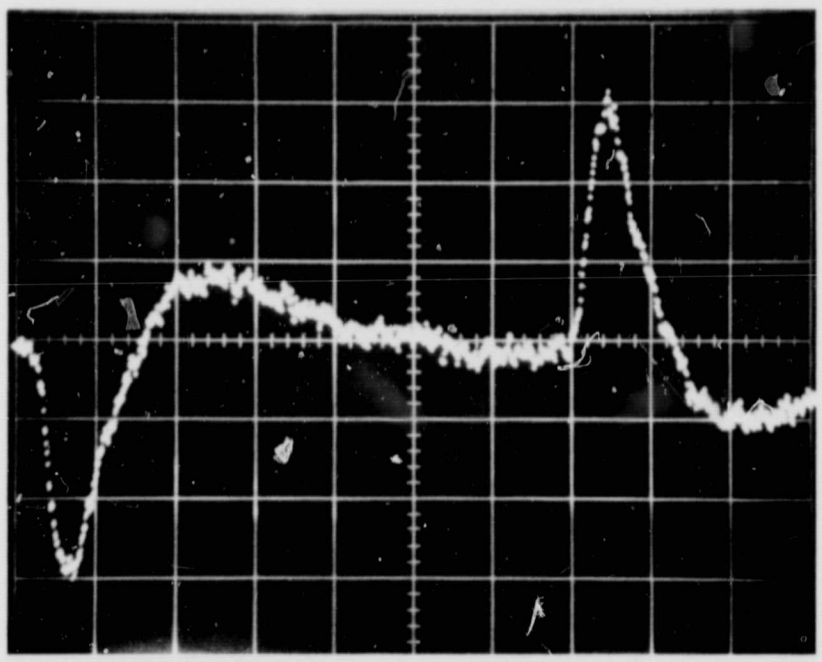


Figure 4.15 Measured gain-frequency characteristic of closed loop sense preamplifier



(a)



(b)

Figure 4.16 Output of sense preamplifier. Part (a) shows output with respect to ground for negative and positive 2 millivolt input pulses. Pulse amplification is 150. Feedback capacitor is 100 picofarads. Part (b) shows same response but with 300 picofarad feedback capacitors. Horizontal scale: 100 nanoseconds/division; vertical scale: 100 millivolts/division.

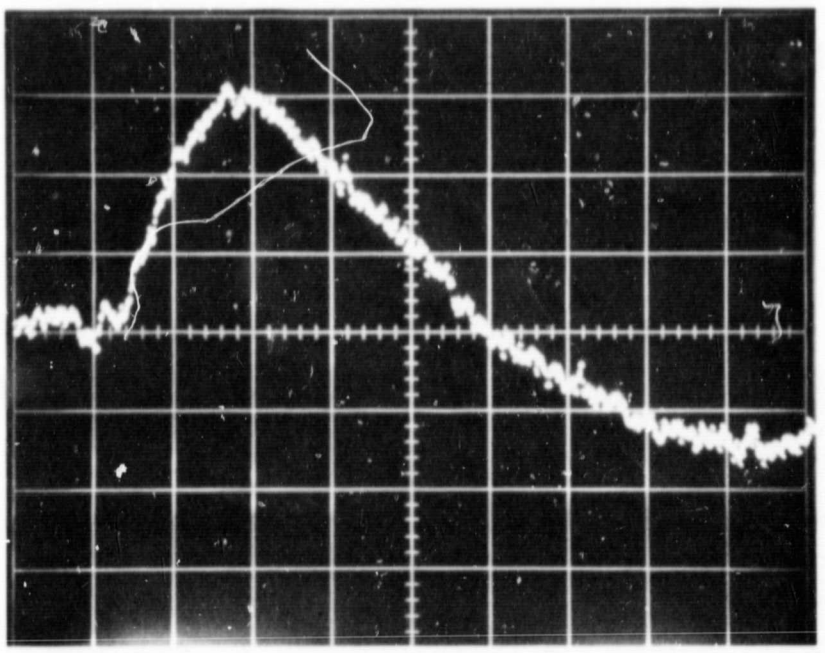
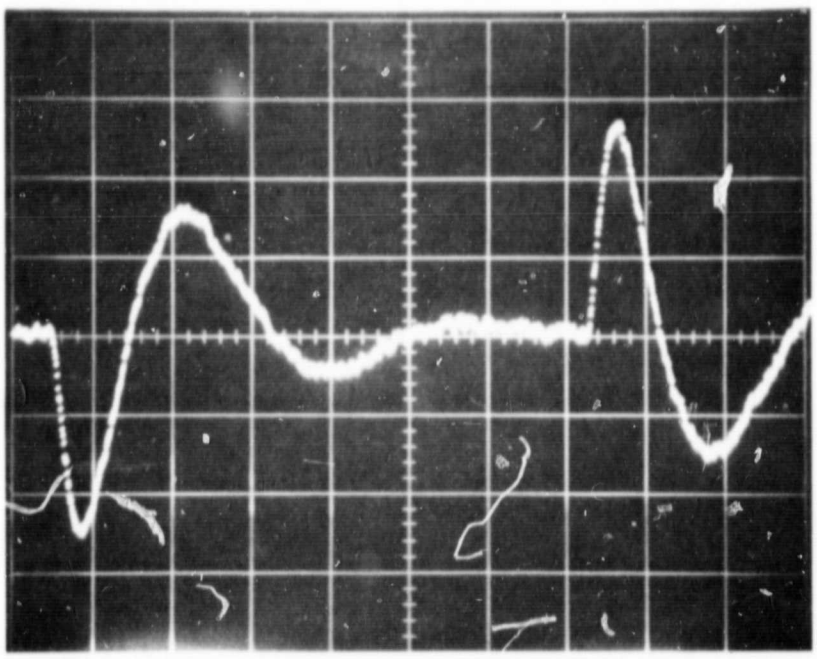
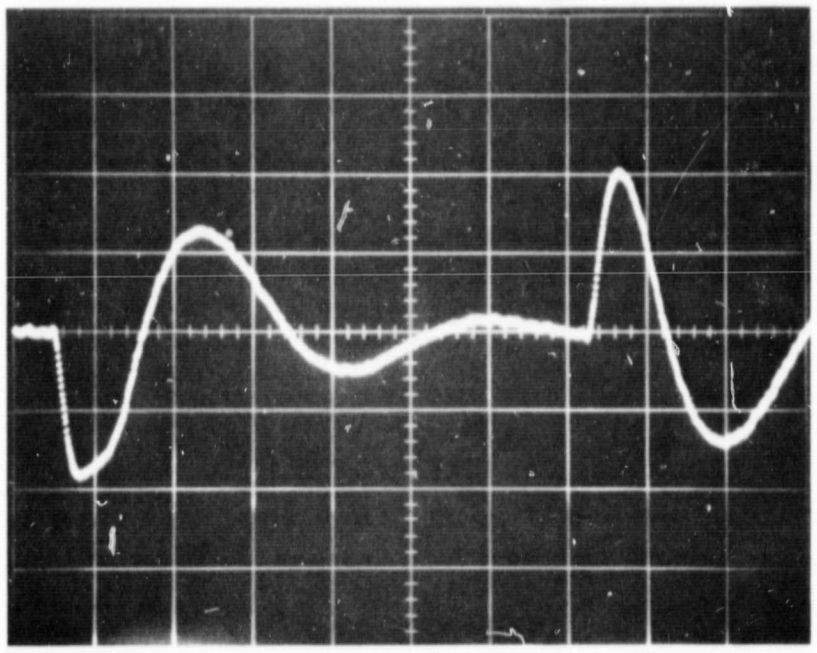


Figure 4.17 Detail of positive output pulse. Horizontal scale: 20 nanoseconds/division; vertical scale: 100 millivolts/division.



(a)



(b)

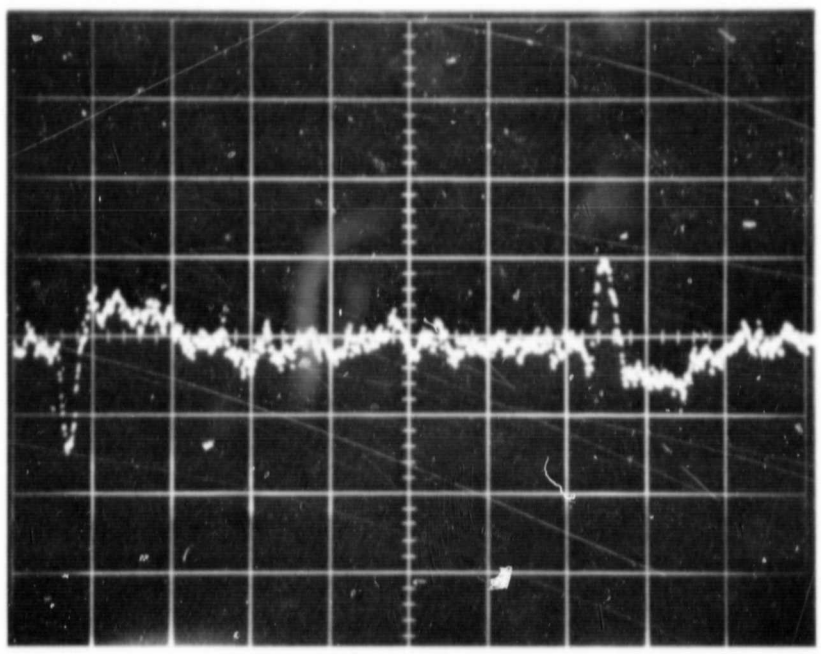
Figure 4.18 Response of amplifier when overdriven with differential signal. Input for (a) was 4 millivolts. Amplification is 125 and vertical scale is 200 millivolts/division. Input for (b) was 10 millivolts. Amplification is 100 and vertical scale is 500 millivolts/division. Horizontal scale is 100 nanoseconds/division.

the word current will result in common mode noise only, and no differential signal will be induced. Any unbalances in the bit lines or terminations will cause a differential signal. Response of the amplifier to two levels of common mode signal is shown in Figure 4.19. The common mode gain of the amplifier is less than one in both cases. The excitation signal in both cases was the sense signal waveform. The differential inputs were tied together to give a common mode input. The common mode gain is relatively independent of signal frequency since the common mode rejection increases at lower frequencies, but so does the differential gain of the amplifier. At higher frequencies the common mode rejection decreases but so does the differential gain.

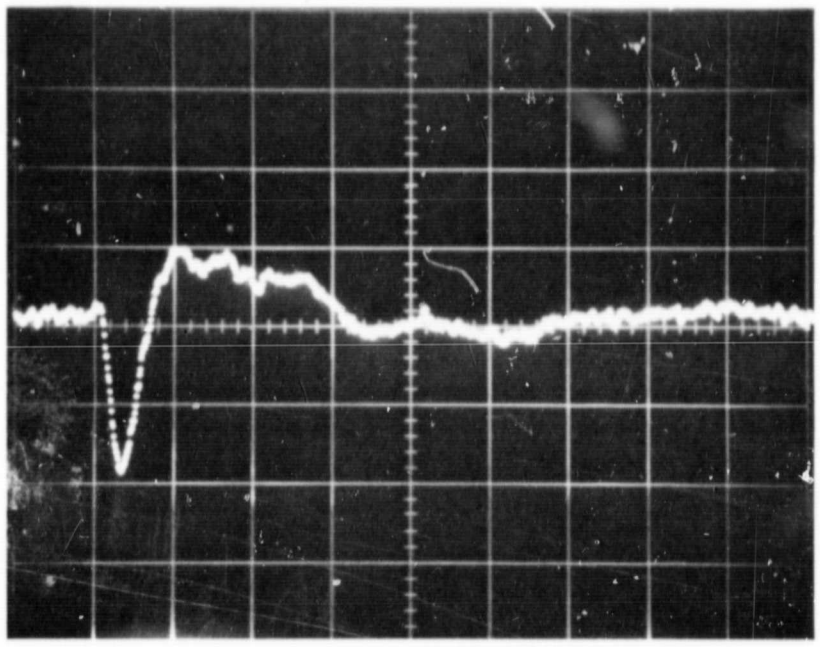
5. Output Stage and Strobing Circuit

A proposed output stage is shown in Figure 4.20. It is similar to the basic circuit module except for the addition of a strobing circuit and emitter followers on the input. This circuit was not actually constructed but is similar to other circuits employed in the sense amplifier. It would be normally directly coupled to the preamplifier and the offset stabilization loop would be taken from the collector load resistors. The stage has a low frequency gain of 16 and the output levels are those of emitter coupled logic. With this gain any signal loss in the input emitter followers is of no consequence. Two strobing transistors, Q_1 and Q_2 of the diagram, are provided. These are held in the saturated mode by a positive true logical ONE from the central processor. Note that the emitter of each of these transistors is returned to the reference voltage, -1.15 volts, of MECL logic. The bases of the output emitter followers, Q_3 and Q_4, are held at about -1.0 volts when Q_1 and Q_2 are ON. The output would be about -1.7 volts in this case, or below the logical ZERO level. The saturation characteristic for a non-gold-doped monolithic transistor is given for moderate base drives by the Motorola reference as 100 millivolts in series with a 75 ohm resistor. It is seen that the collector current of the strobe transistor will always be a small fraction of a milliamp. The base of the output emitter follower will never rise above -1.0 volts when strobed off and, in addition, the collector voltage of the differential pair will not be affected. Thus the integrity of the feedback loop is not damaged by the strobing transistor.

Typical operating waveforms are sketched in Figure 4.21. These show that the differential amplifier is actually switched hard over to one side



(a)



(b)

Figure 4.19 Common mode rejection of sense preamplifier. Output with respect to ground is shown. Inputs for (a) were 125 millivolt sense signals with input terminals tied together. Horizontal scale: 100 nanoseconds/division; vertical scale: 100 millivolts/division. Input for (b) was a 400 millivolt common mode sense signal. Horizontal scale: 50 nanoseconds/division; vertical scale: 200 millivolts/division.

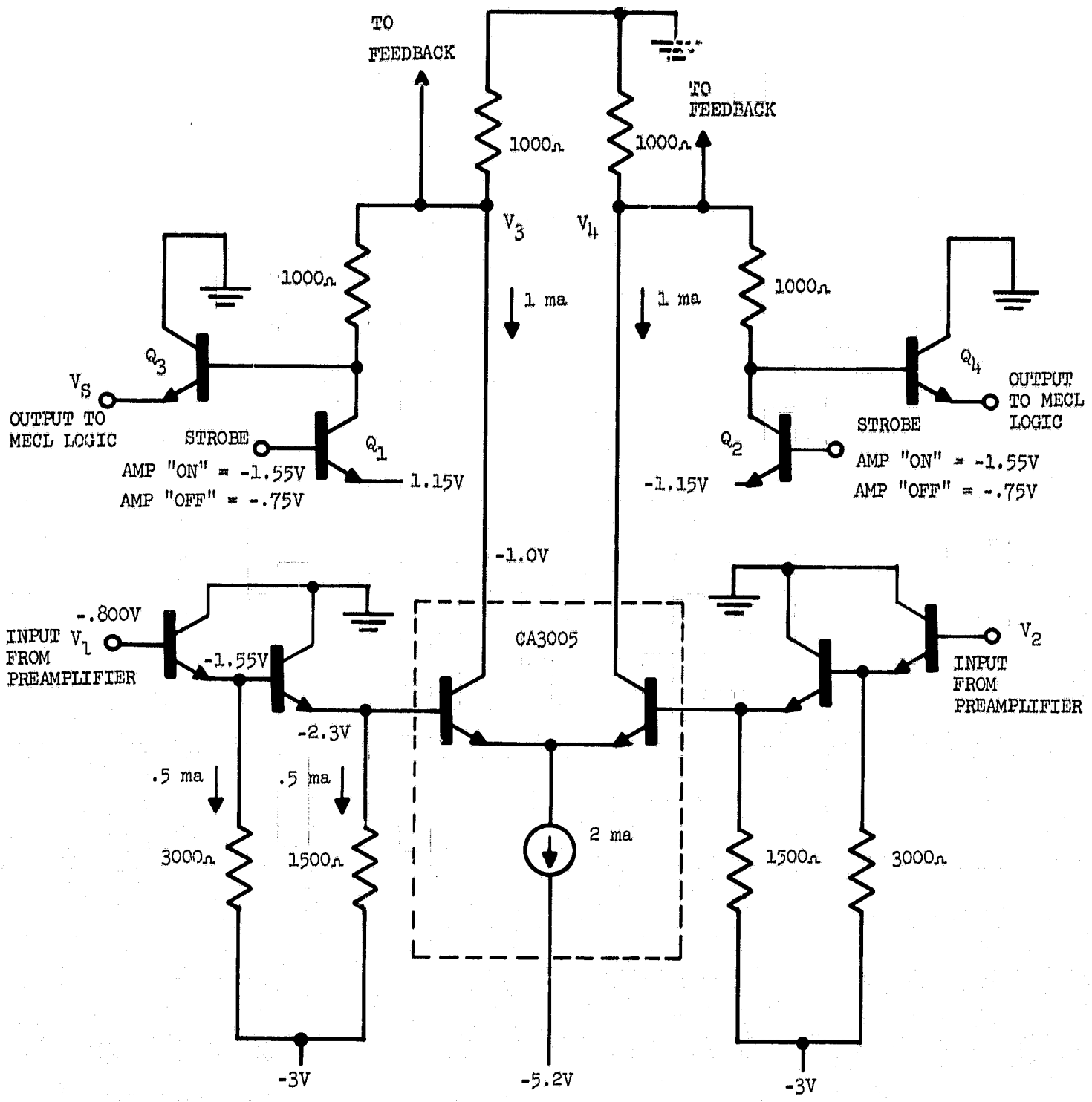


Figure 4.20 Circuit diagram for a typical output stage for sense amplifier. Quiescent voltages and currents are shown

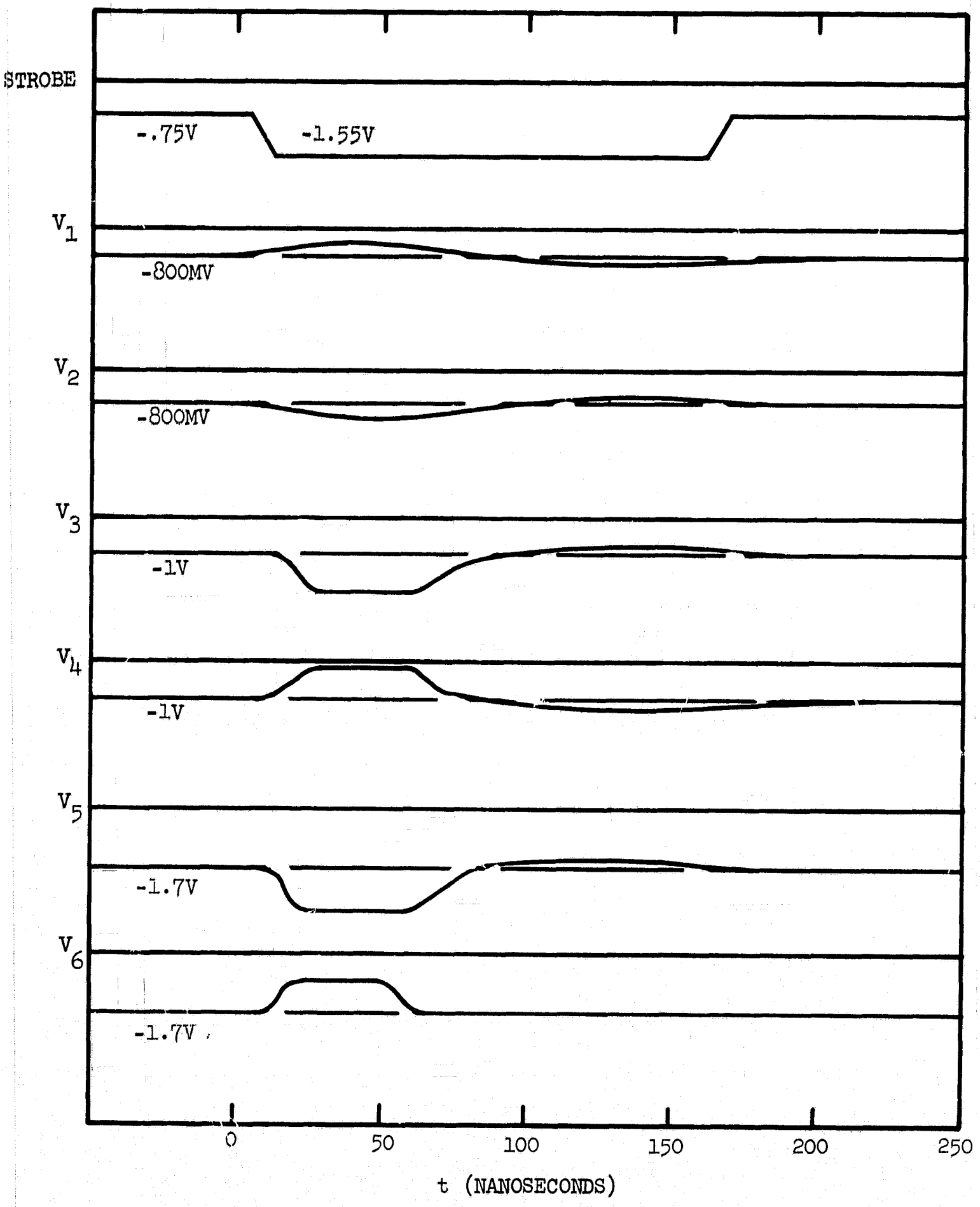


Figure 4.21 Waveforms for sense amplifier output stage. Voltages refer to those shown in the circuit diagram of Figure 4.20

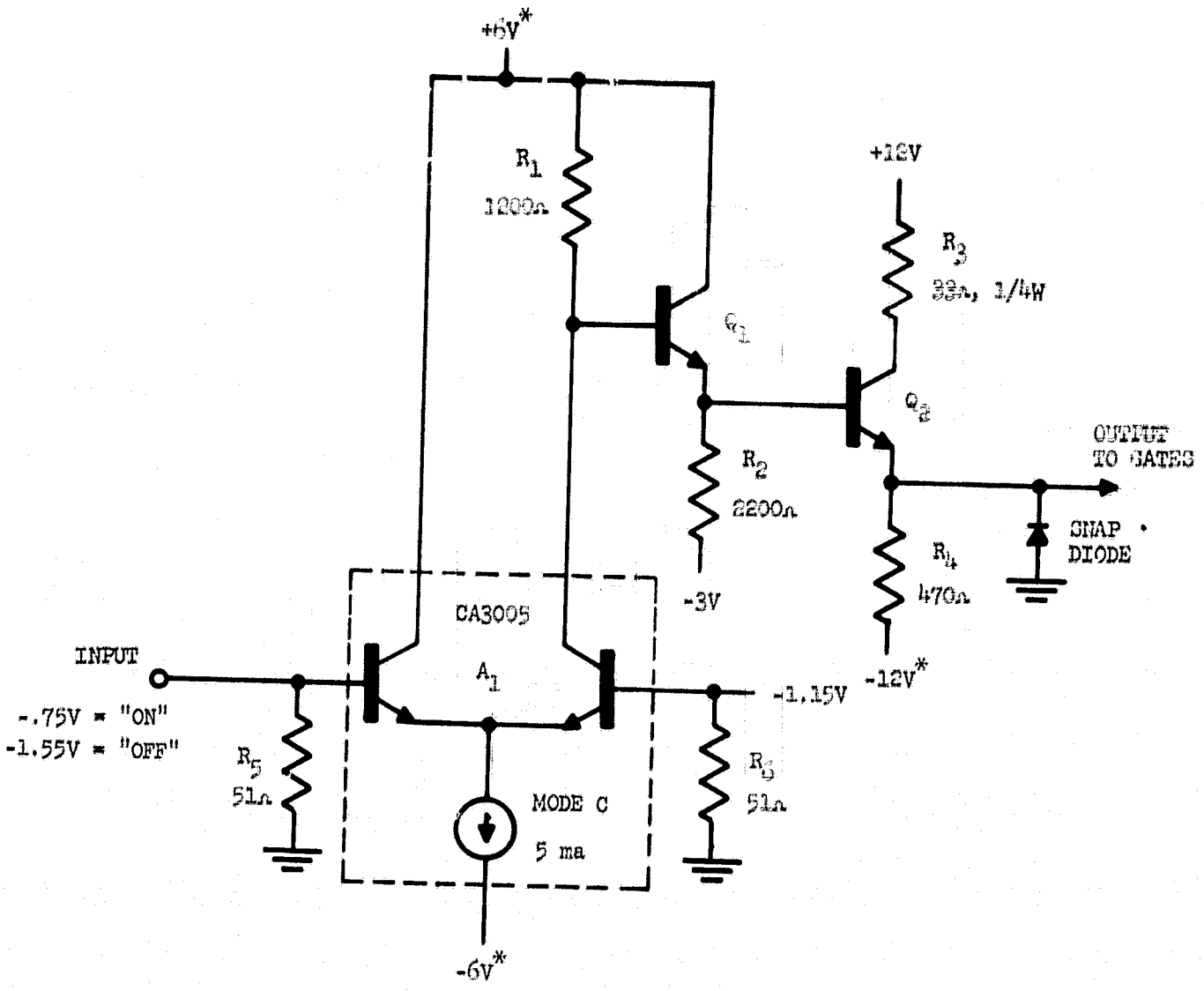
by the sense signal. Thus the cutput waveform and levels are standardized by this stage. Discrimination between a sense "1" and a sense "0" is accomplished since only one side will rise to the "1" level of -.75 volts. This side will set the associated R-S flip-flop which serves as the output register. The other side will actually drop below the "0" level of -1.55 volts, but this will have no adverse effect on the flip-flop.

Power consumption is easily determined and is essentially the same as a single stage of the preamplifier. It is approximately 20 milliwatts. Frequency response of the stage should extend out to about 20 MHz because of the low collector load resistors (1000 ohms). This will mean that the open loop forward amplifier will be characterized by two poles at 10 MHz and one pole at 20 MHz. This is a much better situation than three poles at 10 MHz.

C. WORD DRIVER

The purpose of the word driver is to deliver positive pulses of current with very fast rise times to the word line. The input signal is a logical ONE which, with emitter coupled logic, corresponds to a shift from -1.55 volts to -.75 volts. The word driver uses a basic circuit module, similar to that shown in Figure 4.2, to amplify and level shift the input waveform. One load resistor and emitter follower is omitted since it is not needed. The output emitter follower of the basic circuit drives another emitter follower which acts as the output stage. This single emitter follower can deliver up to 160 milliamps into the word line. If additional current is needed, two such emitter followers can be used in parallel.

The circuit schematic is given in Figure 4.22. A photograph of one such circuit is given in Figure 4.23 and the various components are identified. A single 2N918 discrete transistor is used as the output stage. This transistor must be operated with a very low duty cycle in order to withstand such high current levels. Paralleling two such transistors, or using a gold-doped-collector transistor, would provide a more sophisticated output stage. The final design would depend on the exact current level required and the capabilities of the monolithic transistors. The salient point of the design is that the basic circuit module can conveniently amplify and level shift the emitter coupled logic signals and drive a simple output stage. This same circuit topology can easily deliver 250 milliamps with different supply



* INDICATES POWER SUPPLY VOLTAGE WHICH IS SWITCHED ON DURING MEMORY CYCLE

Figure 4.22 Circuit diagram for word line driver

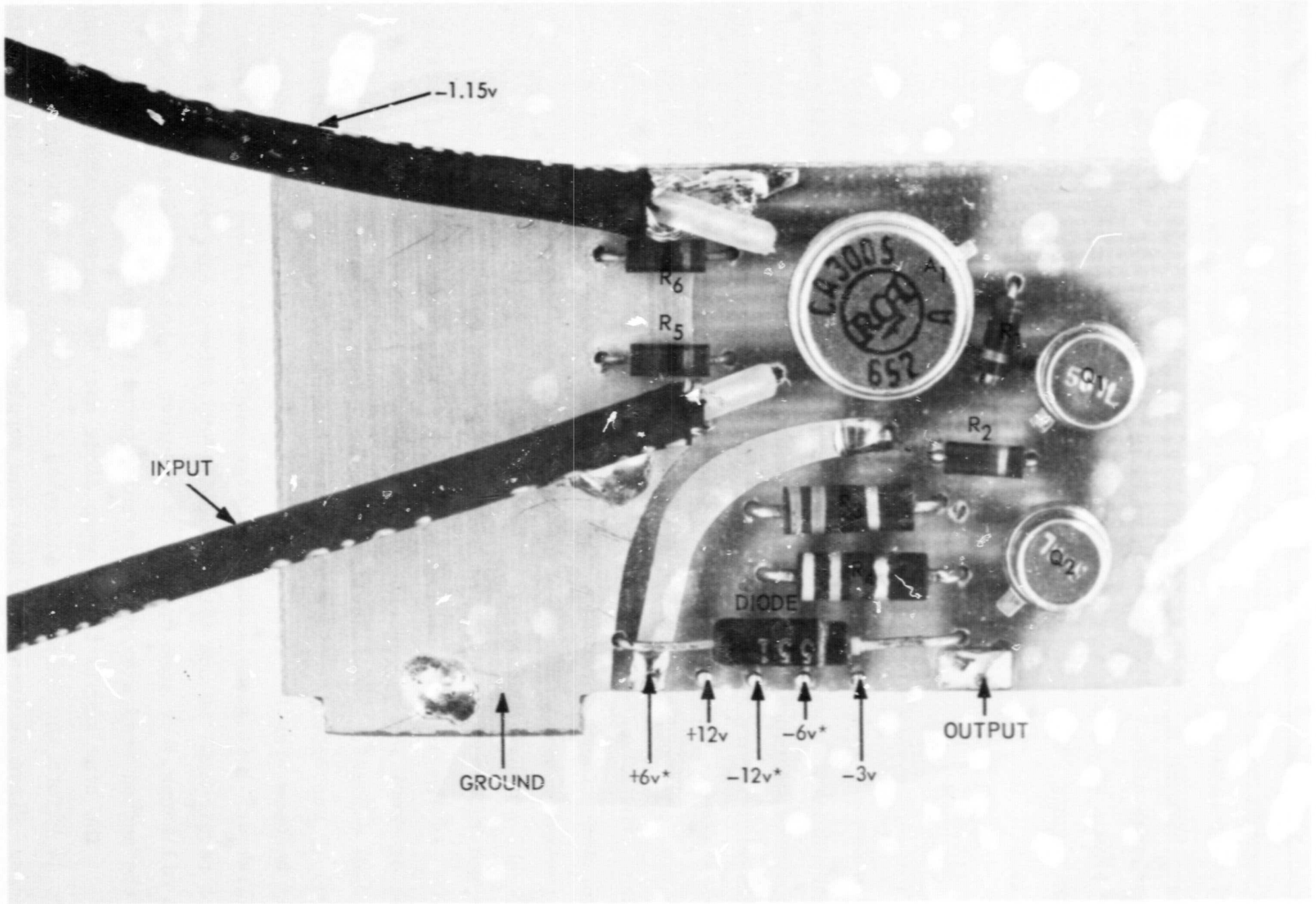


Figure 4.23 Parts identification for word line driver board

voltages and a different output stage (a higher capacity transistor or two paralleled transistors).

A one nanosecond rise time is achieved with the use of a snap diode. The operation of recovery snap diodes is adequately explained in Reference (12), the General Electric Transistor Manual. The diode is first forward biased through R_4. A certain amount of charge is stored in the junction. The charge stored is a function of the bias current and the recombination lifetime τ of excess carriers. If the charging current is i_d, then the stored charge is

$$Q_f = i_d \tau (1 - e^{-t/\tau})$$

where the charging current is turned on for t seconds. If the rise time of the driver is much less than the recombination time, essentially all of the stored charge is recovered. By recovered it is meant that the snap diode will remain forward biased until the driver has delivered to it this much charge in the form of reverse current through the diode. Thus when the time integral of output current from the driver has depleted all stored charge, the diode will "snap" off and the voltage across the input to the word line will rise rapidly. If the output current from the driver can be approximated as a ramp, then the snap diode must store at least $I_{max}/2T$ coulombs of charge, where I_{max} is the maximum output current from the driver and T is the rise time of this current pulse.

In the present design the HPA type 0114 diode has a recombination time of about 125 nanoseconds. This value is actually a function of the forward current. The effective rise time of the driver current pulse is about 15 nanoseconds (since the driver output voltage must rise considerably to back bias the diode), and the maximum output current is about 160 milliamps. This gives a stored charge requirement of 2.4 nanocoulombs. This requirement is met with a 25 milliamp forward current. Q_2 switches 200 milliamps, but some current is absorbed in the diode biasing network, so the actual word line pulse is only 160 milliamps.

The bias supply to the snap diode must be turned on about 150 nanoseconds before the driver is activated in order to store the required charge. Since it is assumed that the supply voltages can be turned on at

the initiation of a memory cycle, this is a simple arrangement. The delayed input to the driver stage could be furnished by the central processor. One disadvantage of the simple resistor biasing network is that it absorbs some of the driver output current. The input voltage to the word line is several volts during the word pulse. Thus the driver must furnish enough current to drop about 12 + 3 = 15 volts across R_4. A much more efficient method would be to have a common emitter driver to bias the snap diode rather than R_4. The arrangement would be similar to the bit line driver. The common emitter stage could be driven from the unused side of the differential amplifier. This circuit modification is sketched in Figure 4.24. Rather than return to -12 volts, as in the present driver, the emitter can be returned to -3 or -6 volts, thus saving power. The return is to -12 volts in the present circuit so that R_4 can be maximized and thus minimize the driver output absorbed in R_4. When the memory cycle is initiated with the modified circuit, the bias driver would come on and charge the diode. The output driver would then be activated by a delayed pulse. As the driver came on, the bias driver would turn off. Operation of both the original and the modified circuit is explained by the chart of Figure 4.25. It is seen that R_3 limits the maximum output current from the driver since Q_2 is operated in a saturated mode when ON. Choice of R_3 selects the word pulse amplitude.

The rise time of the output driver is important in that a faster rise time will require less charge stored in the snap diode. The differential amplifier is never saturated, so the rise time can be estimated accurately from small signal performance. From the discussion of the sense amplifier it is known that typical bandwidths for the basic circuit module with resistive loads between 1000 and 2000 ohms are between 10 and 20 MHz. From the well-known relation between rise time and bandwidth for systems with little overshoot (systems characterized by a dominant simple pole),

$$B_w T_r = 0.3$$

we have for a circuit with a 10 MHz bandwidth,

$$T_r = 0.3/10^7 = 30 \text{ nanoseconds}$$

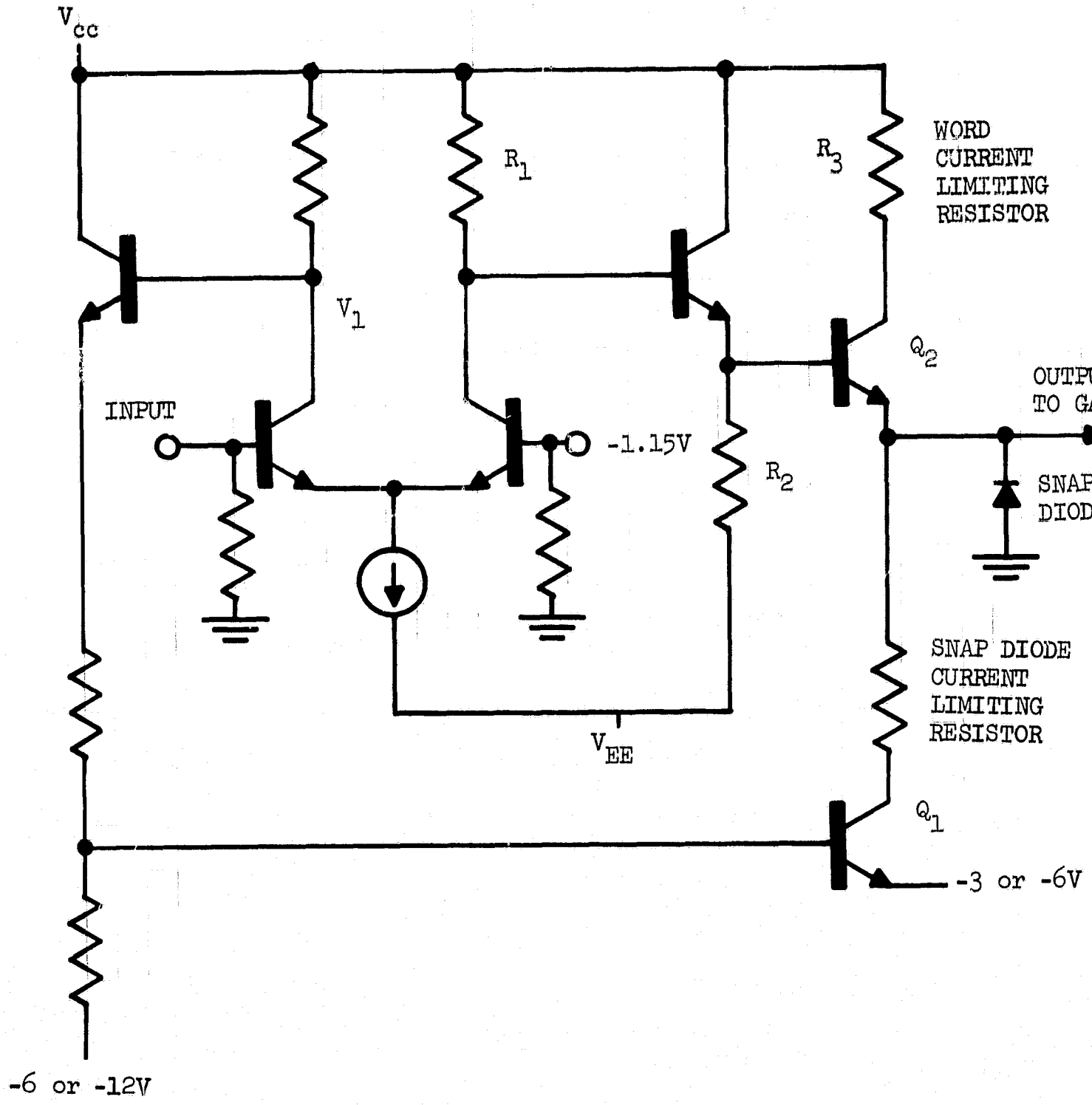


Figure 4.24 A modified word line driver

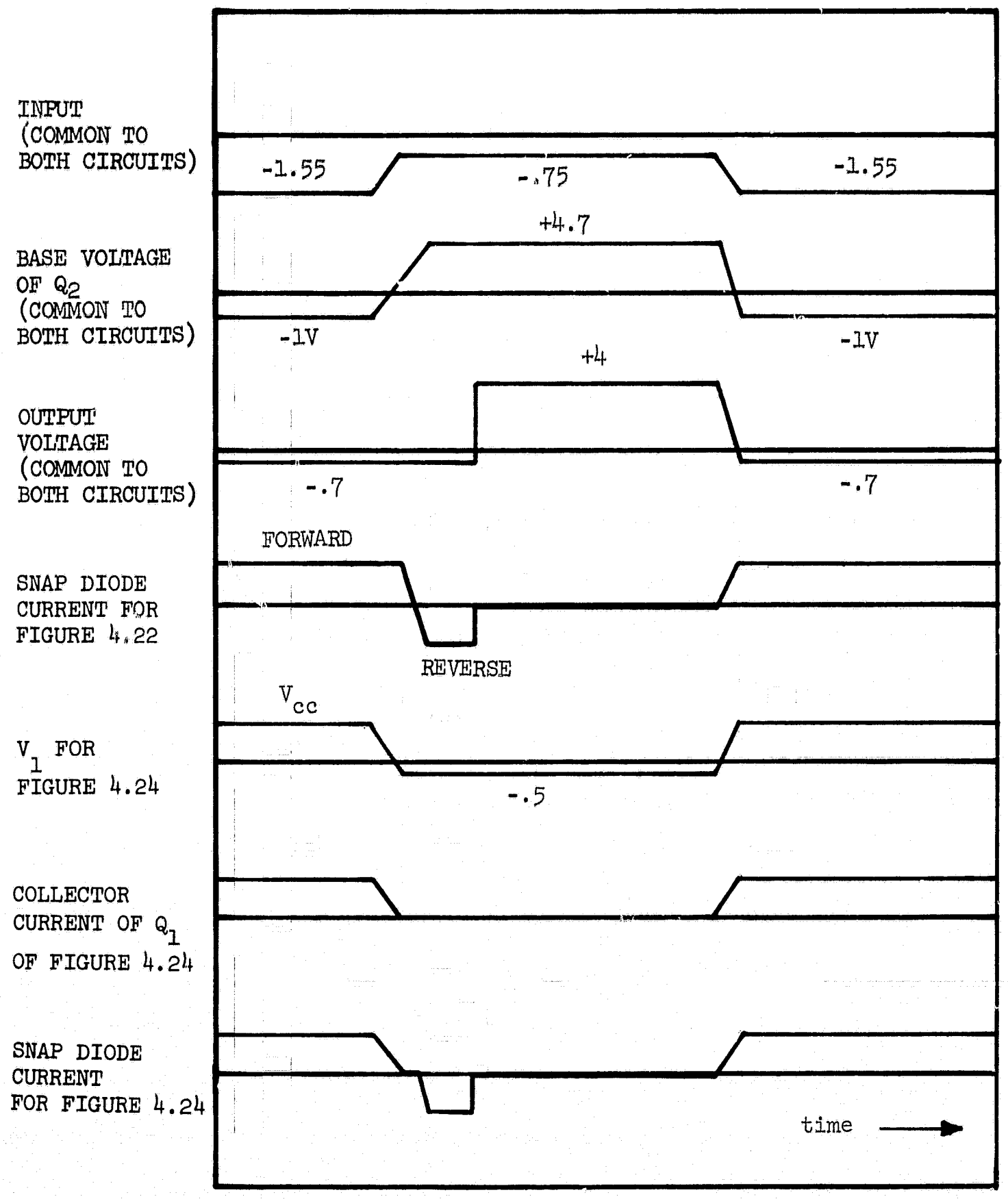


Figure 4.25 Comparison of waveforms in the two word line drivers

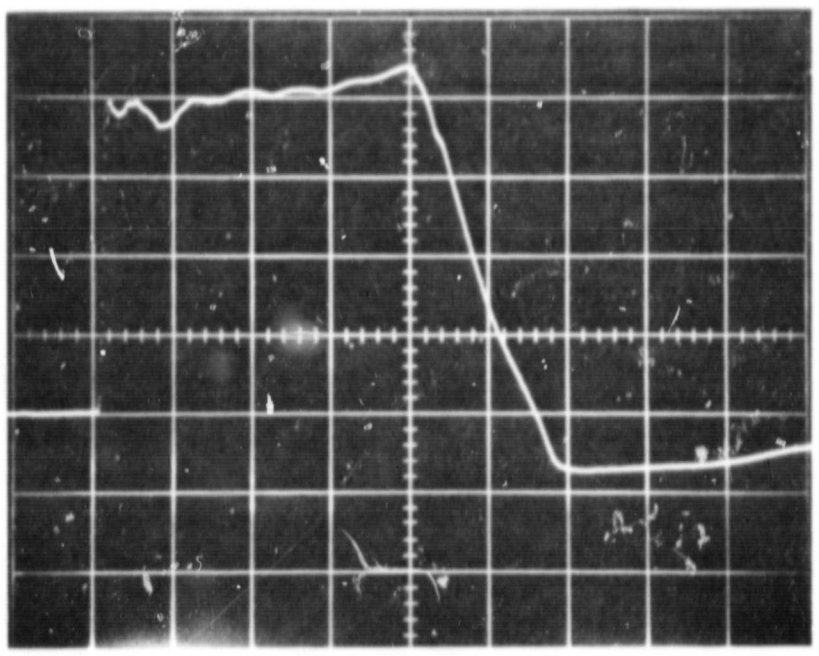
Similarly, a 20 MHz bandwidth circuit will have a rise time of about 15 nanoseconds. These figures agree with the observed rise time of 20 nanoseconds for the base waveform of Q_1. The fall time of the output stage will show the effects of base charge storage since the transistor is saturated when ON. The storage time can be minimized by providing a low impedance path to the base of the output transistor. This is provided by the emitter follower output of the basic circuit. The maximum discharge current that Q_1 can handle is limited by R_2. Fall time is thus minimized by small values of R_2. On the other hand, R_2 absorbs current from Q_1 when the driver is ON. This current would otherwise be base drive to Q_2. Thus small values of R_2 limit base drive to Q_2. A compromise value for R_2 must be chosen.

Circuit performance is shown in the photographs of Figure 4.26. A one nanosecond rise time is achieved with an output amplitude of 160 milliamps. The load for this test was a 1N55 diode in series with a 15 ohm resistor and a two inch wire loop to simulate the word line.

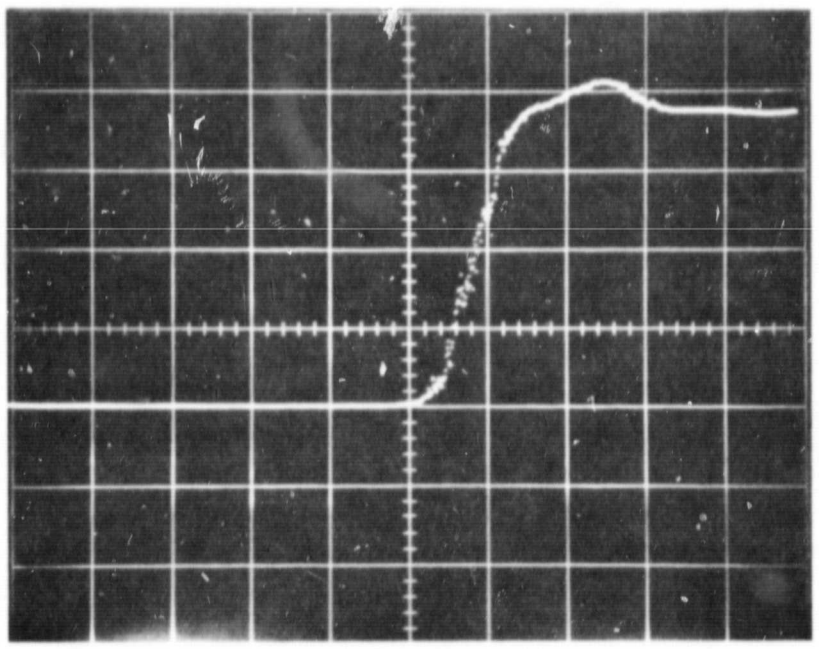
D. BIT DRIVER

The bit driver must furnish either a positive or negative output pulse of about 25 milliamps. The exact level is set by the characteristics of the magnetic films and the transmission lines. The particular circuit shown in Figure 4.27 delivers 20 milliamps but the circuit topology can easily deliver 50 milliamps. That is, if resistor values are changed slightly and power supply levels are increased, more output current is available. Figure 4.28 shows a photograph of an actual circuit board. The exact output level is set by R_1 (for the positive driver) and by R_7 (for the negative driver). These would be precision resistors in an operating system. Circuits delivering larger currents will likely be slightly slower since larger resistor values have to be used.

Circuit operation will be briefly explained with the aid of the schematic. As in the case of the word driver, a basic circuit module drives an output stage. A logical ONE at the input of either differential amplifier will turn the corresponding driver ON. The second side of the differential amplifier is taken to -1.15 volts, the reference voltage for emitter coupled logic. A logical ONE turns the right hand side of the differential



(a)



(b)

Figure 4.26 Output current from the word line driver of Figure 4.22. Part (a) shows the 160 milliamp pulse. Horizontal scale: 20 nanoseconds/division. Part (b) shows the leading edge. Horizontal scale: 1 nanosecond/division. Vertical scale: 40 milliamps/division.

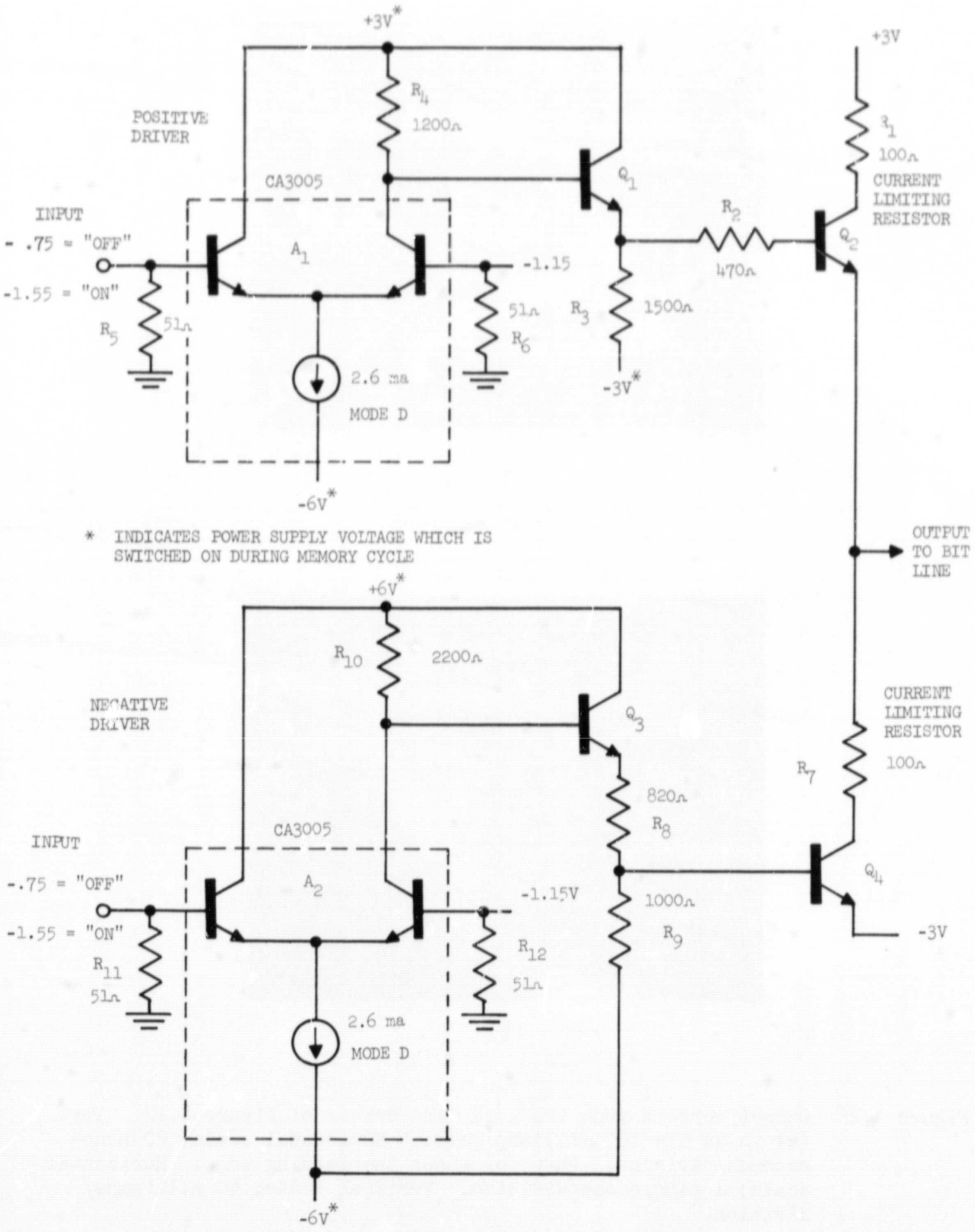


Figure 4.27 Circuit diagram for bit line driver

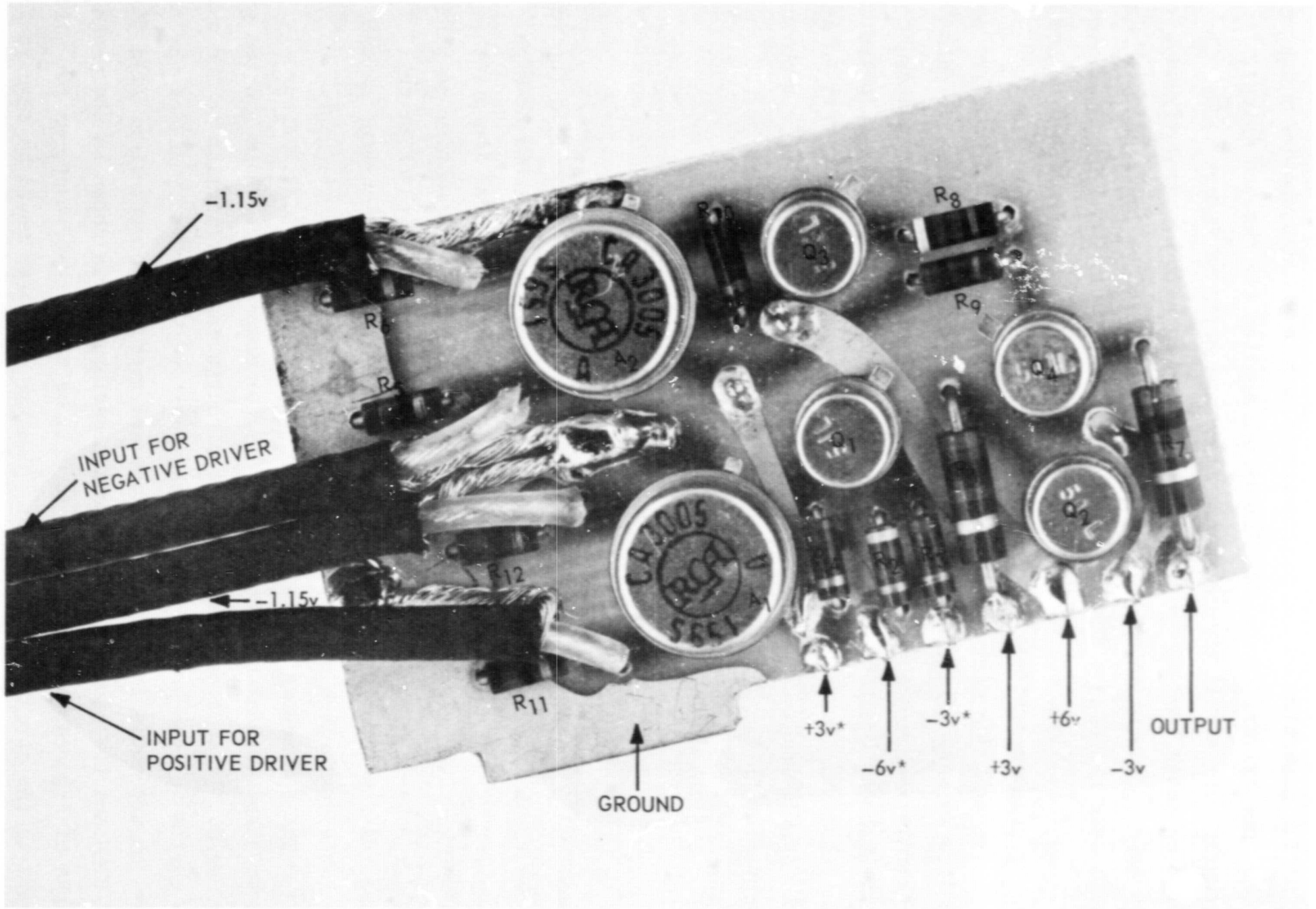


Figure 4.28 Parts identification for bit line driver board

amplifier off and Q_1 or Q_3 on. In turn, either Q_2 or Q_4 is turned on and a current pulse appears on the bit line.

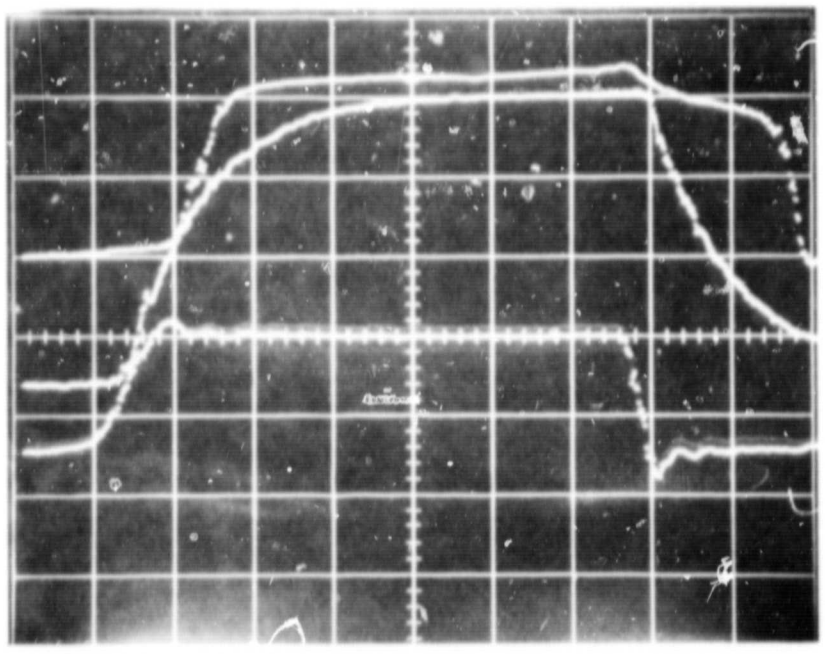
The rise time of the basic circuit module was discussed for the case of the word driver. A similar discussion applies for the bit driver. Photographs of actual circuit performance are given in Figure 4.29. It should be noted that the supply voltages must be well bypassed at the circuit card. This is accomplished on the mother board by low impedance supply busses over a ground plane. If these supplies are not well bypassed, the rise and fall times of the circuits will be longer because of the increased load impedances. In addition there will be more noise on the lines.

The bit driver is capable of delivering closely spaced positive and negative pulses. Figure 4.30 shows a negative and then a positive pulse. By bringing the excitation pulses closer together in time, the pulses shown can be brought together until they cancel each other. No loss in pulse fidelity occurs. This is useful in the case of the word driver if it is desired to eliminate the bias resistor for the snap diode. This is a possible improvement in the word driver and is discussed in the section on the word driver.

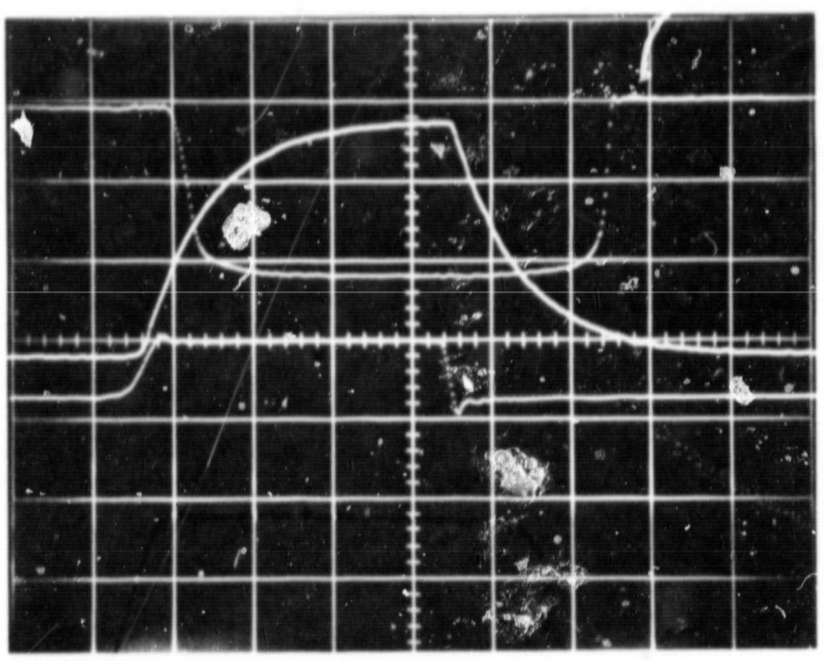
E. HIGH AND LOW GATES

The purpose of the gates is to switch the output pulse from the word driver to the appropriate word line. The HIGH gates select one of eight groups of word lines and the LOW gates select the individual lines within the groups. The input to the gates is a logical ONE from emitter coupled logic. A basic circuit module is used to amplify and level shift this pulse. A common emitter output stage is then used as a saturated switch. The gates can switch up to 200 milliamps.

The schematics for the gates are shown in Figure 4.31. Figures 4.32 and 4.33 show actual boards and identify the components. There are two gates per board. It will be noted that the circuits are very similar to the driver portion of the word driver and the positive bit driver. All of the comments on tradeoffs for resistor values and rise time computations hold for the HIGH and LOW gates. Actual circuit performance is shown in the photographs of Figures 4.34 and 4.35. It will be noted that waveforms for various points in the circuit are included. Similar waveforms would be seen in the word driver and the bit driver.



(a)



(b)

Figure 4.29 Circuit waveforms for bit line driver. Part (a) shows the positive driver. Uppermost is the output current at 10 milliamps/division. Next is the base voltage waveform of Q_2, at 1 volt/division, and lowermost is the input signal. Horizontal scale: 10 nanoseconds/division. Part (b) shows the negative driver. Uppermost is the output current at 10 milliamps/division. Next is the base voltage waveform of Q_3, at 2.5 volts/division, and lowermost is the input signal. Horizontal scale: 20 nanoseconds/division.

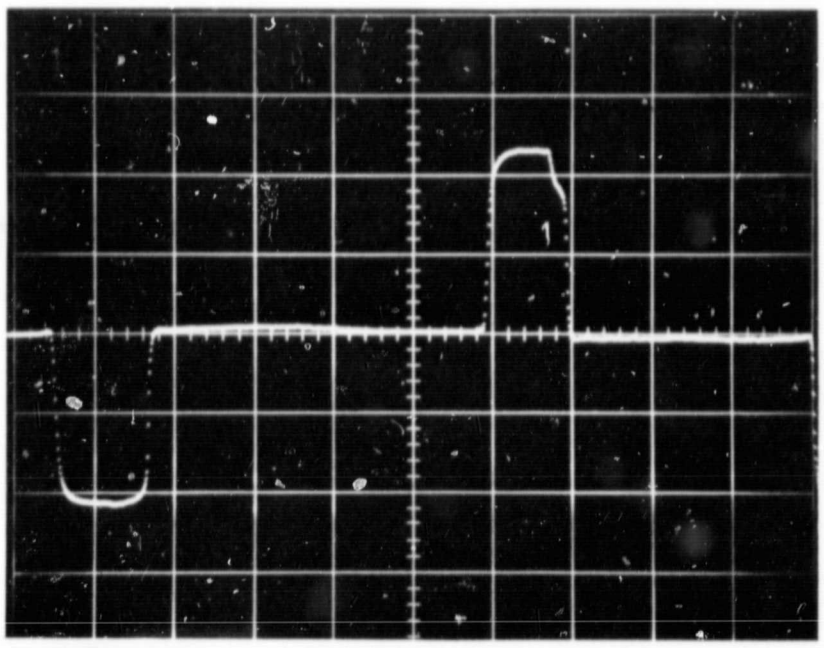
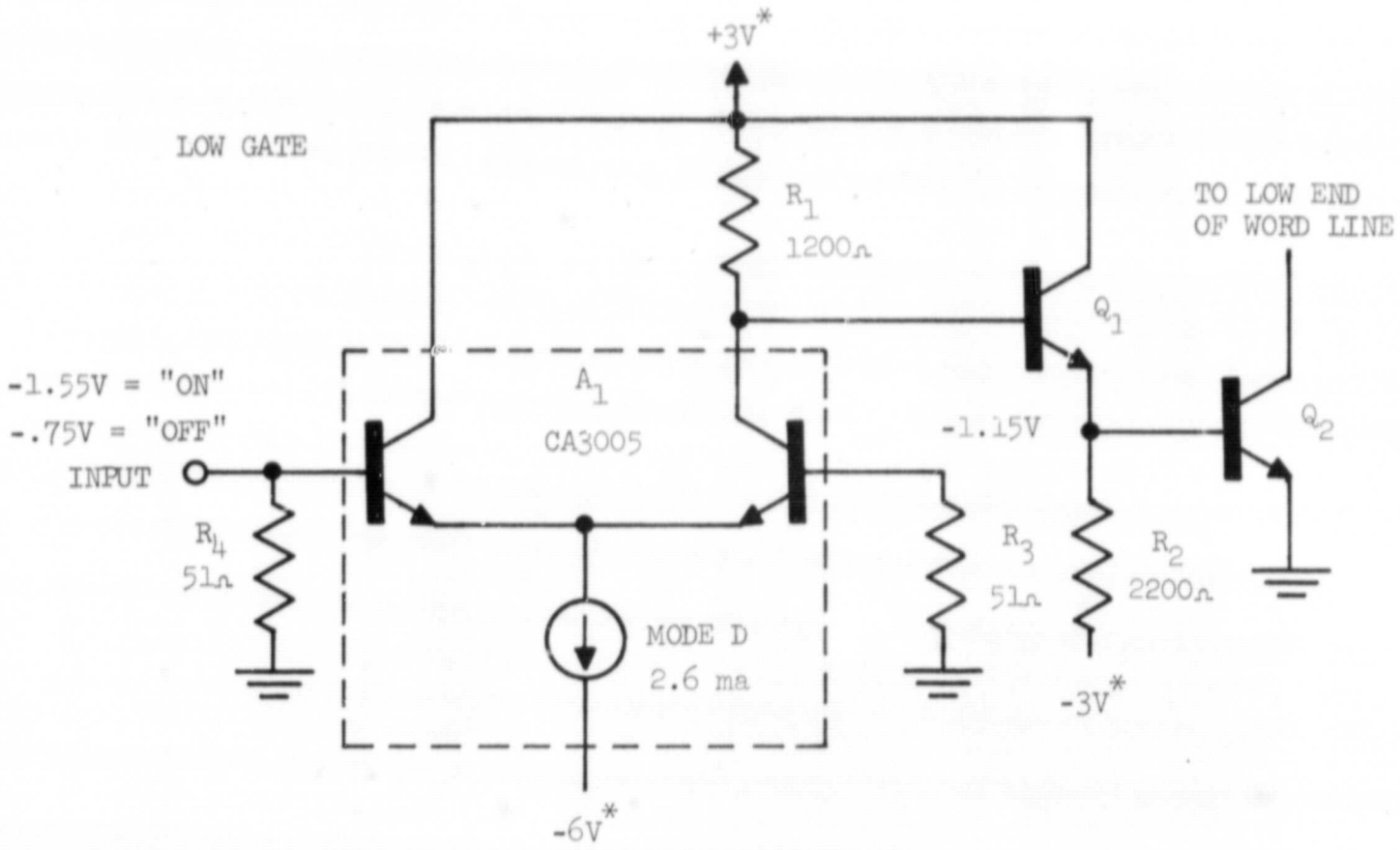


Figure 4.30 Negative and then positive outputs from the bit line driver. Horizontal scale: 100 nanoseconds/division; vertical scale: 10 milliamps/division.



* INDICATES POWER SUPPLY VOLTAGE WHICH IS SWITCHED ON DURING MEMORY CYCLE

Figure 4.31 Circuit diagram for HIGH and LOW gates

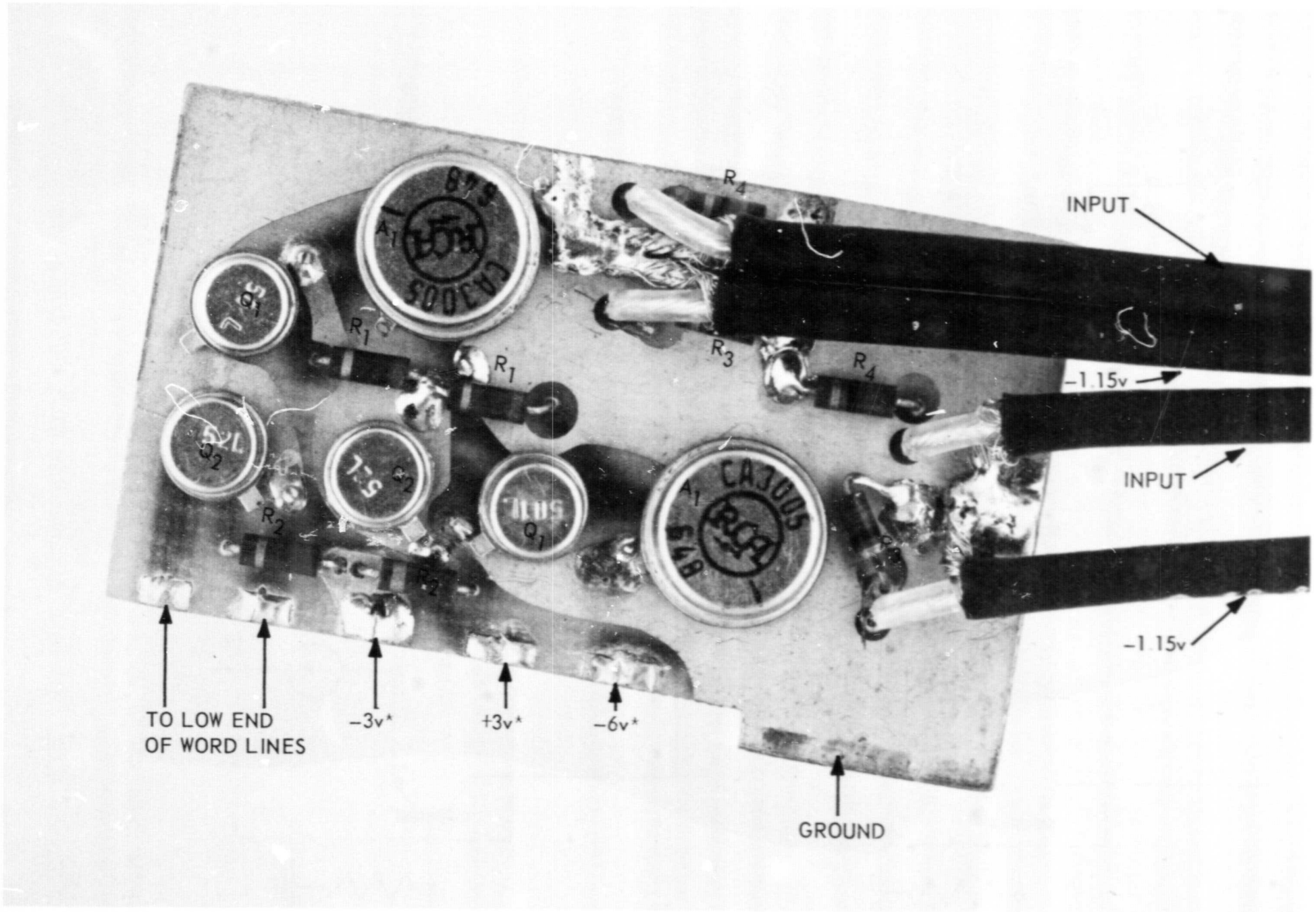


Figure 4.32 Parts identification for LOW gates board. There are two gates per board

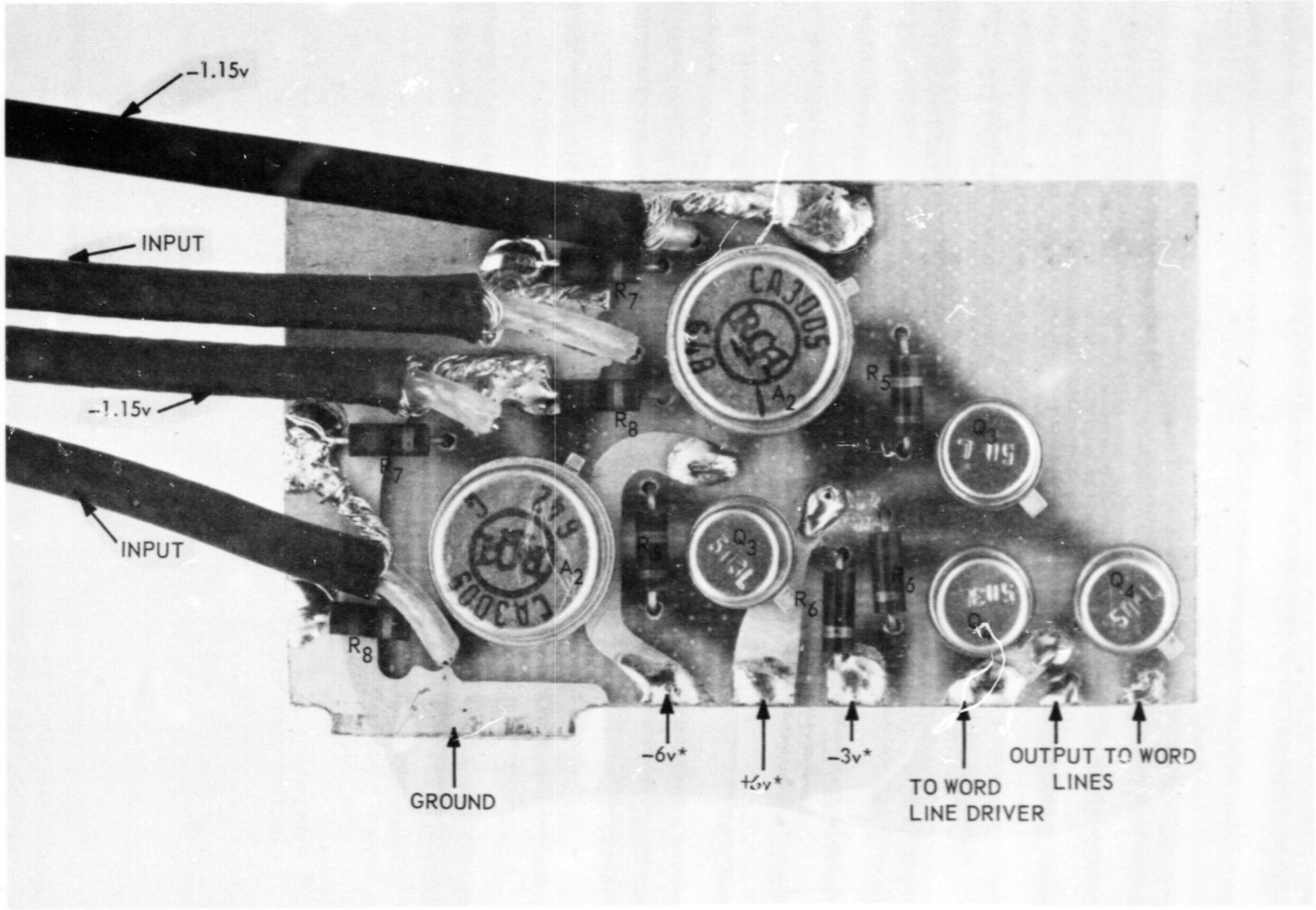


Figure 4.33 Parts identification for HIGH gates board. There are two gates per board

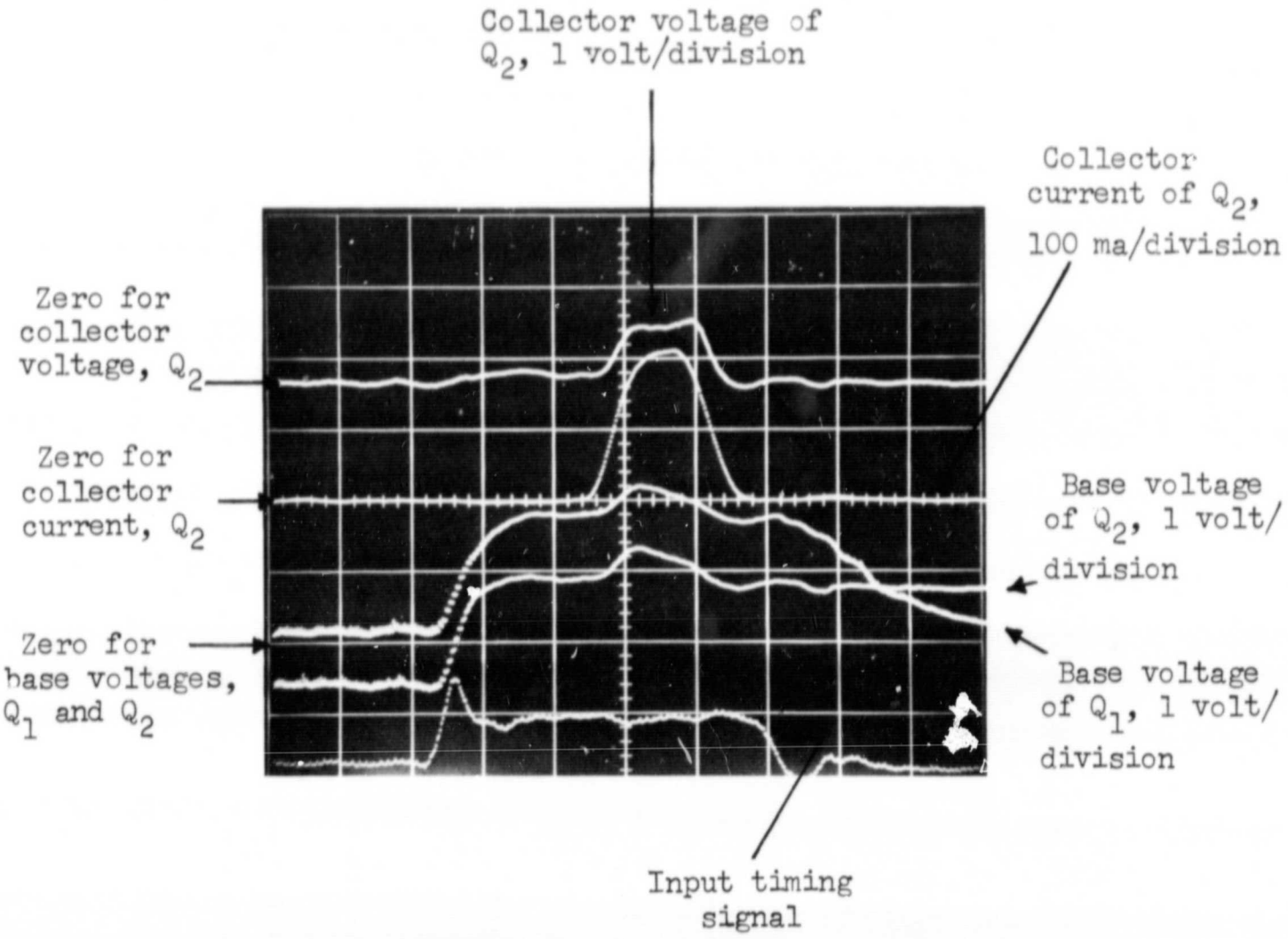


Figure 4.34 Operation of LOW gates when switched on. Horizontal scale: 10 nanoseconds/division.

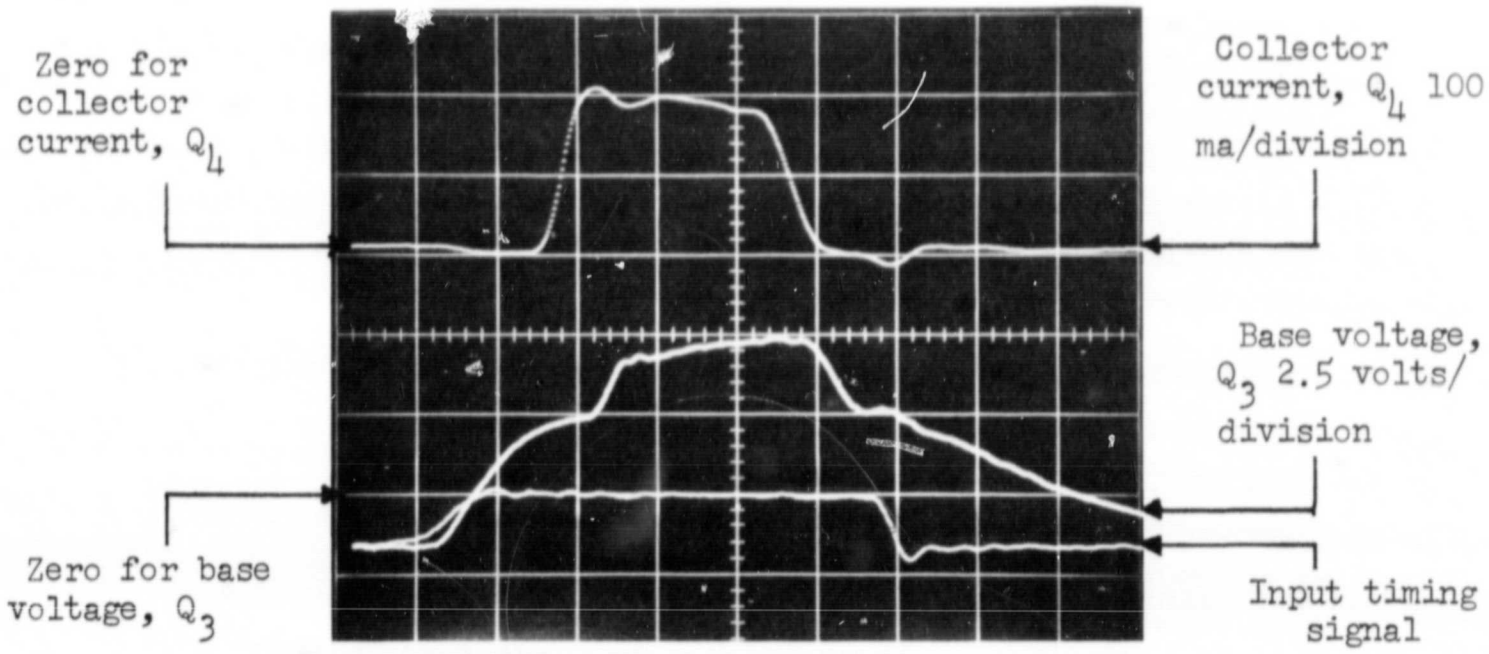


Figure 4.35 Operation of HIGH gates when switched on. Horizontal scale: 10 nanoseconds/division.

F. TIMING CHART, POWER CONSUMPTION TABLE, AND MOTHER BOARD

The timing chart for memory operation is a direct consequence of the performance capabilities of the individual circuits. Based on the performance shown in the figures of this report, the timing chart of Figure 4.36 can be constructed. The length of time that power must be turned on to the circuits is determined by the biasing requirements of the snap diode in the word generator. If this diode were driven by a transistor, as suggested in the word driver section, this biasing period could be reduced to about 50 nanoseconds. This would include the rise time of the snap diode bias driver. On the other hand, if the memory were to be operated continuously, or in bursts with many consecutive cycles, it would be more economical to use resistive biasing for the snap diode.

The maximum repetition rate is set by the settling time of the sense amplifier. This settling time can be minimized by lowering the frequency of the feedback pole. The waveform drawn is based on the performance of the circuits delivered (with 100 picofarad capacitors).

In summary, the power must be turned on from the time bias is applied to the snap diode until the bit current has written information back into the memory. The maximum repetition rate is set by the time from the initiation of the word pulse to the settling of the sense amplifier. Thus the maximum rate is set by the 225 nanosecond time from word pulse to settling of the sense amplifier. Power must be supplied for about 250 nanoseconds. Both of these times can be reduced by the measures indicated above.

A power consumption table is given in Figure 4.37. The average power consumption is 900 milliwatts at a 200 kHz repetition rate. This is below the maximum of 1000 milliwatts allowed. The additional 100 milliwatts could be easily "spent" to lower the rise times of the various generators by lowering resistance levels and increasing current levels. Some thought has been given to the problem of turning on and off power to the various gates and drivers. Because of the fast response time of the circuits, no problem will be experienced with ringing or instability. One set of circuits, the LOW gates, was tested with the power switched on just before the circuit was activated by the signal pulse. Performance of the low gates is shown in the photograph of Figure 4.38. There is no difference between the observed circuit performance under these conditions and under steady state power

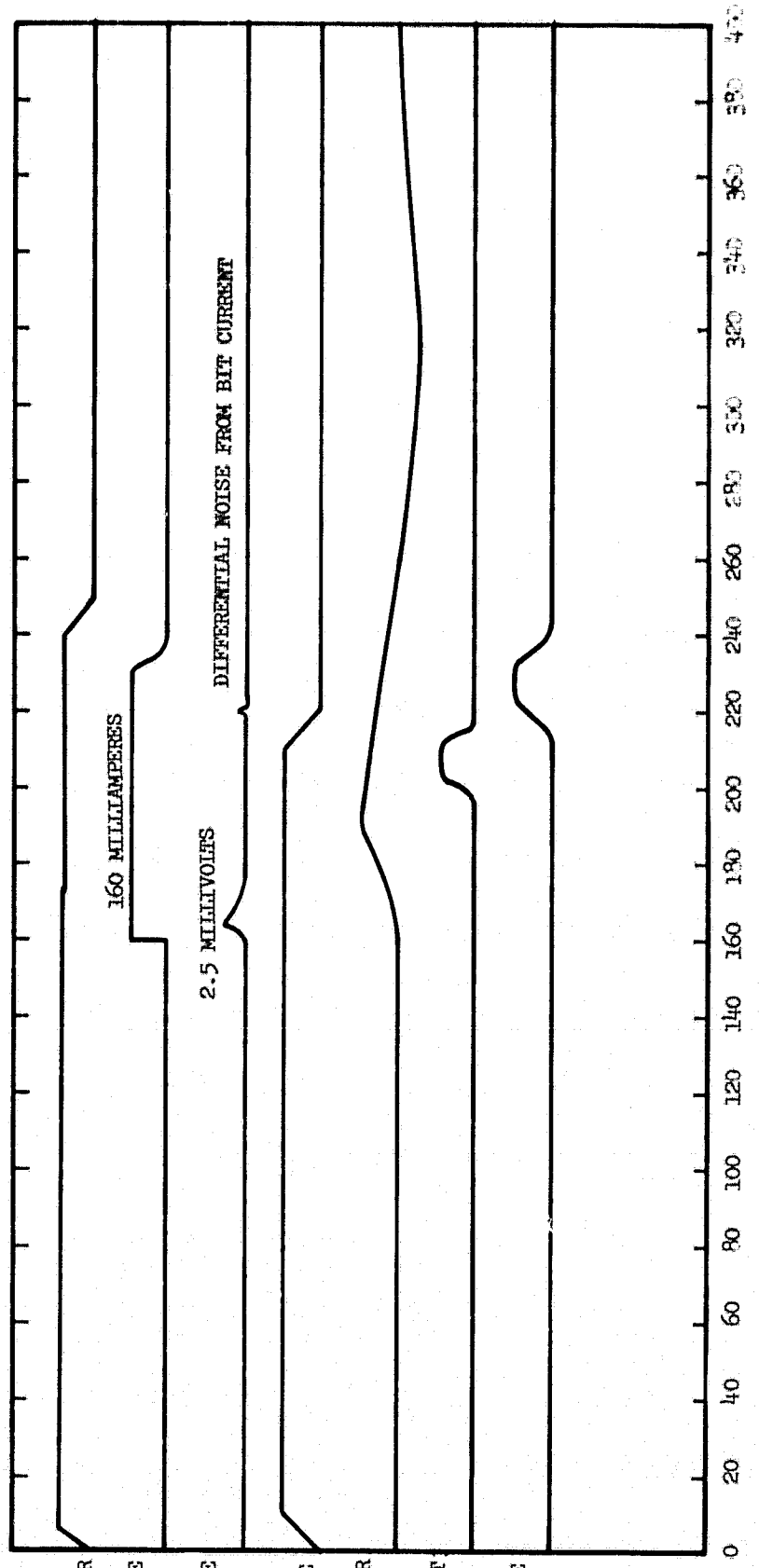


Figure 4.36 Timing chart for memory

Figure 4.37

POWER CONSUMPTION

Duty cycle is computed on the basis of a 200 kHz repetition rate. Since power is on for 250 nanoseconds per cycle, the duty cycle is 0.05 or 5%. Only the sense amplifiers and power gates are not switched on and off.

Circuit Function	Number in Memory	Consumption per Circuit	Total Consumption
Power Gate (±3 volts, ±6 volts, -12 volts)	5	25 milliwatts	125 milliwatts
Sense Preamplifier	8	60	480
Sense Amplifier Output Stage	8	20	160
Word Line Driver	1	0.05 x 1200 = 60	60
Bit Line Driver	8	0.05 x 100 = 5	40
HIGH Gates	8	0.05 x 42 = 2.1	17
LOW Gates	8	0.05 x 35 = 1.75	14
			896 milliwatts

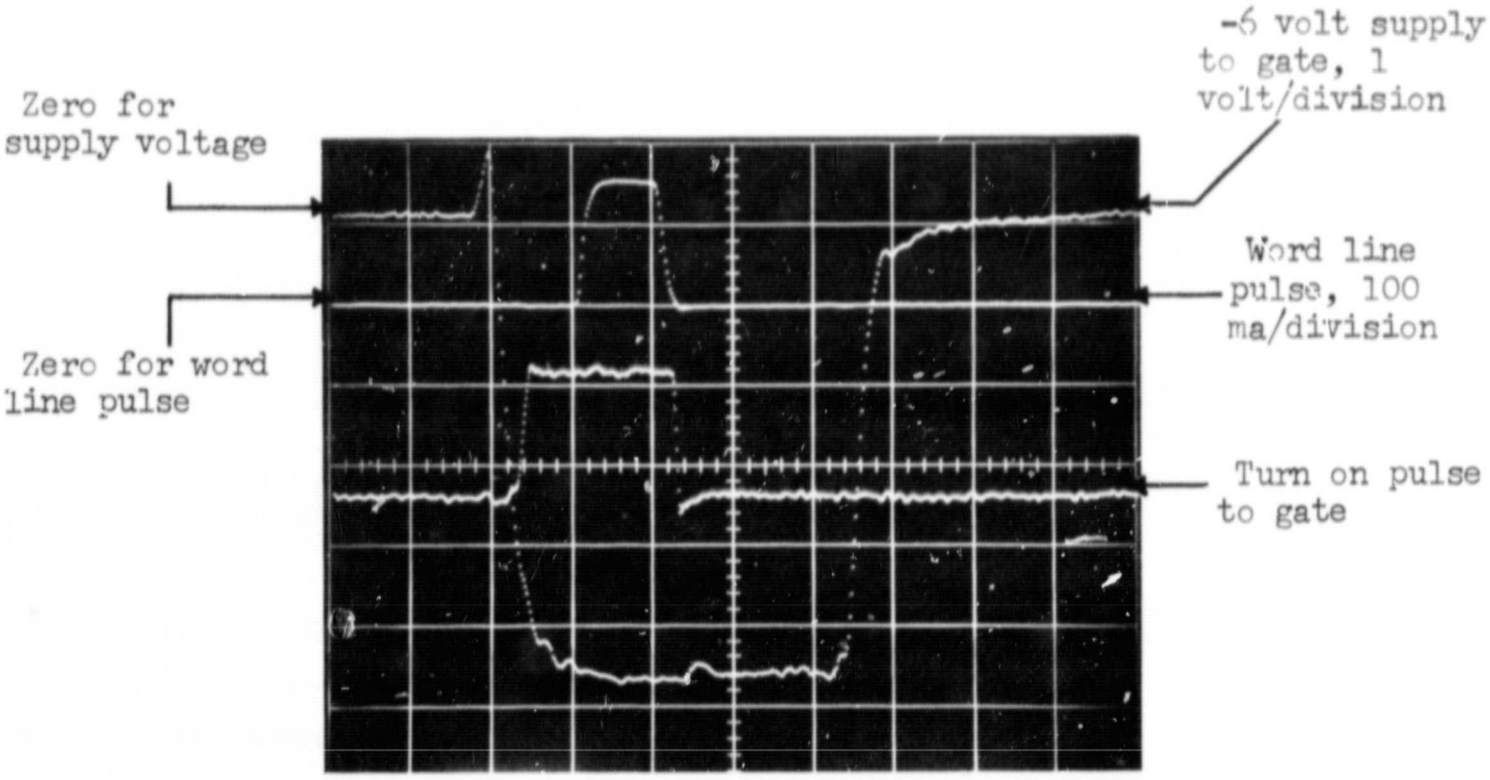


Figure 4.38 Performance of LOW gates under pulsed power conditions. Horizontal scale: 50 nanoseconds/division.

conditions. The 25 nanoseconds between when the power is applied and when the circuit can be switched by logical signals can be used to charge the snap diode.

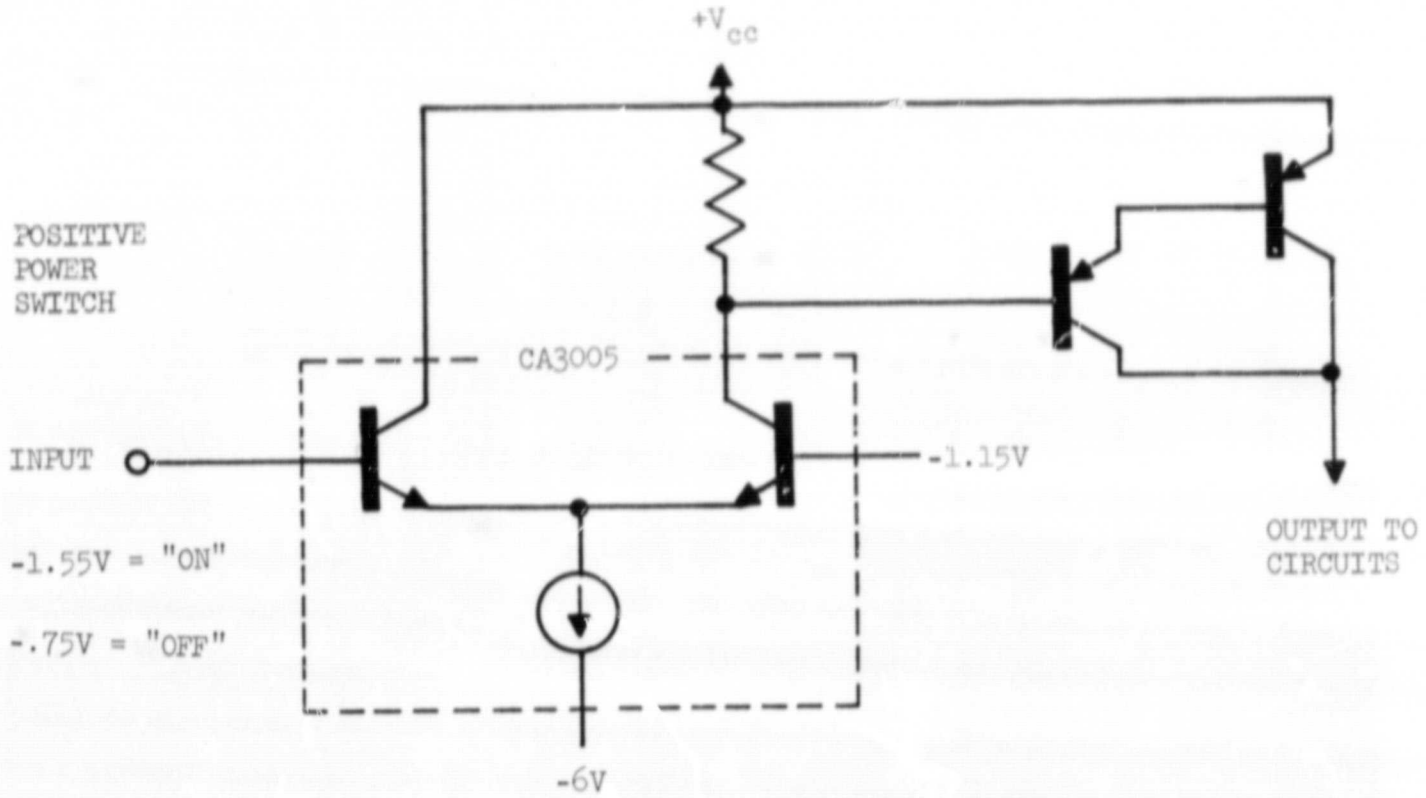
Typical power switches are shown in Figure 4.39. The design assumes that it would be permissible to use PNP transistors for this switching application since only a few are required and they could be fabricated on separate chips or in a separate isolation region of the chip. Furthermore, the performance of these transistors is not critical and low β transistors would be acceptable. The primary requirement of these transistors is the ability to handle relatively large currents. Fortunately none of the supplies which directly furnish output current from the drivers has to be switched.

Commercial integrated circuits were used as much as possible in this design. Even so, because of the number of extra discrete transistors and resistors required, the circuits for a completed memory will occupy about 46 square inches of printed circuit board surface. This may be compared to about 1.8 square inches of memory plane. It should be noted that if all circuits were monolithic, as they may be, they would occupy less room than the memory plane. Although 46 square inches of printed circuit board surface is not excessive (approximately 7" x 7"), problems of fan-in and fan-out from the memory plane suggested using small circuit boards mounted perpendicular to the mother board. If all circuits are on small, secondary boards the design is modular and can be changed without changing the large mother board.

The layout of the mother board is shown in Figure 4.40. Regions are indicated for each of the circuit types, i.e., LOW gates, HIGH gates, bit drivers, word driver and sense amplifiers. Each secondary board fits in a milled slot in the mother board and is held firm by epoxy cement. Tabs are placed on both sides of the small boards for soldering to the lines of the mother board. These solder filets offer additional mechanical support. The entire reverse side of the mother board is a ground plane to keep the impedance of the lines on the mother board low.

G. SUMMARY

The purpose of the circuits effort was to investigate the feasibility of using an all integrated structure for a thin film memory. It has been shown that an all integrated circuit is indeed feasible. Circuits



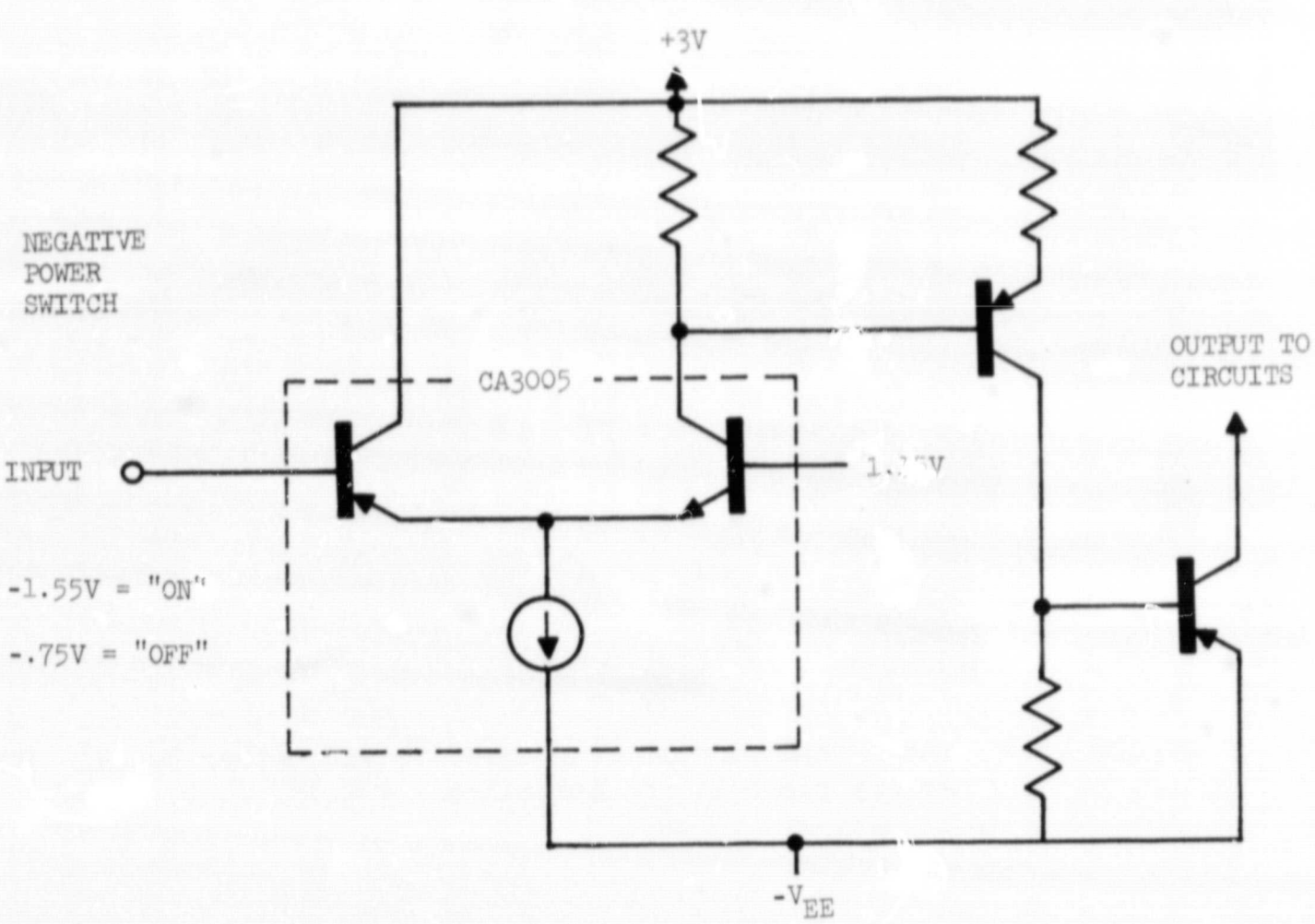


Figure 4.39 Typical positive and negative power switches

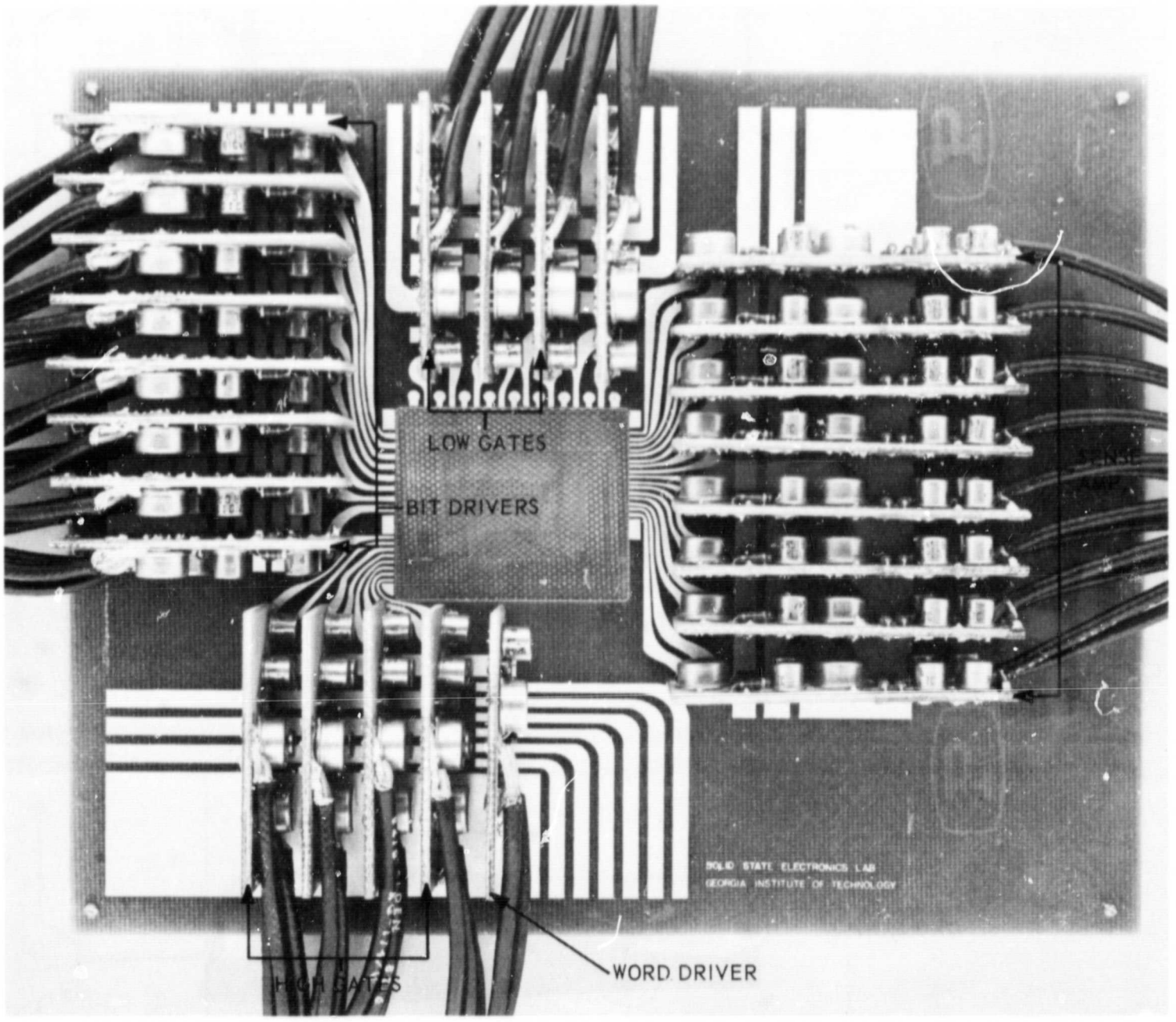


Figure 4.40 Photograph of completed circuits and mother board. The memory plane is not installed

have been demonstrated which perform all required tasks. The power gain-bandwidth relation for the circuits has been demonstrated. A method of optimizing the circuits with respect to amplification, power consumption, and chip area is explained. Possible methods of solving the coupling problem in multistage linear amplifiers have been listed. The general technique of using frequency dependent feedback is a powerful method of handling offsets. Finally, the entire circuit design makes use of a basic circuit module. It was interesting to note that this module can handle both linear and switching operations.

V. THIN FIIM MULTILAYER FABRICATION

A. APPARATUS AND PROCEDURES

1. Film Deposition and Apparatus

Film deposition by evaporation in high vacuum was employed exclusively in this study. Major apparatus and accessories are discussed.

1.1 Vacuum Evaporation System. The primary vacuum system was a Veeco model VE-775 automatic evaporator. The vacuum chamber is constructed of type 304 stainless steel and is 26 inches in diameter. The system is adapted to conventional evaporation methods using filaments, boats, or crucibles. In addition, an electron beam power supply and gun, Veeco model VeB-6-C, is incorporated for evaporation by electron beam techniques. Helmholtz coils are positioned outside the vacuum chamber for applying constant magnetic fields up to 60 Oersted during the deposition of magnetic films. An overhead chain hoist is employed to raise and lower the 200 pound coils. Figure 5.1 is an overall view of the vacuum system.

1.2 Accessories and Techniques. During early film depositions, a substrate and mask changer manufactured by Edwards High Vacuum, Inc. was employed. However, several parts associated with the rotational mechanism of this apparatus were magnetic. These had to be removed for this work, and only the basic tripod and top support plate of the original changer were utilized during the major portion of this program. Further modifications included the construction of (1) source compartments that provided vapor shielding between two source positions and two substrate positions and (2) a fixture for supporting, heating, and masking substrates. Insitu substrate or mask changing features were eliminated in the modification. Major features are shown in Figure 5.2. During evaporations from filaments and boats, substrates were supported above the evaporation source at a distance of 6 inches. Electron beam evaporations were made upward from a massive copper crucible positioned 8-1/2 inches below the substrate position.

A fixture was constructed to provide substrate support, substrate heating, and accurate substrate to mask registration. Major details are shown in the sequence of photographs in Figure 5.3. Three precision pins mutually register the substrate and transmission masks. The mask holder mates with a copper plate with the substrate sandwiched in a pressure fit

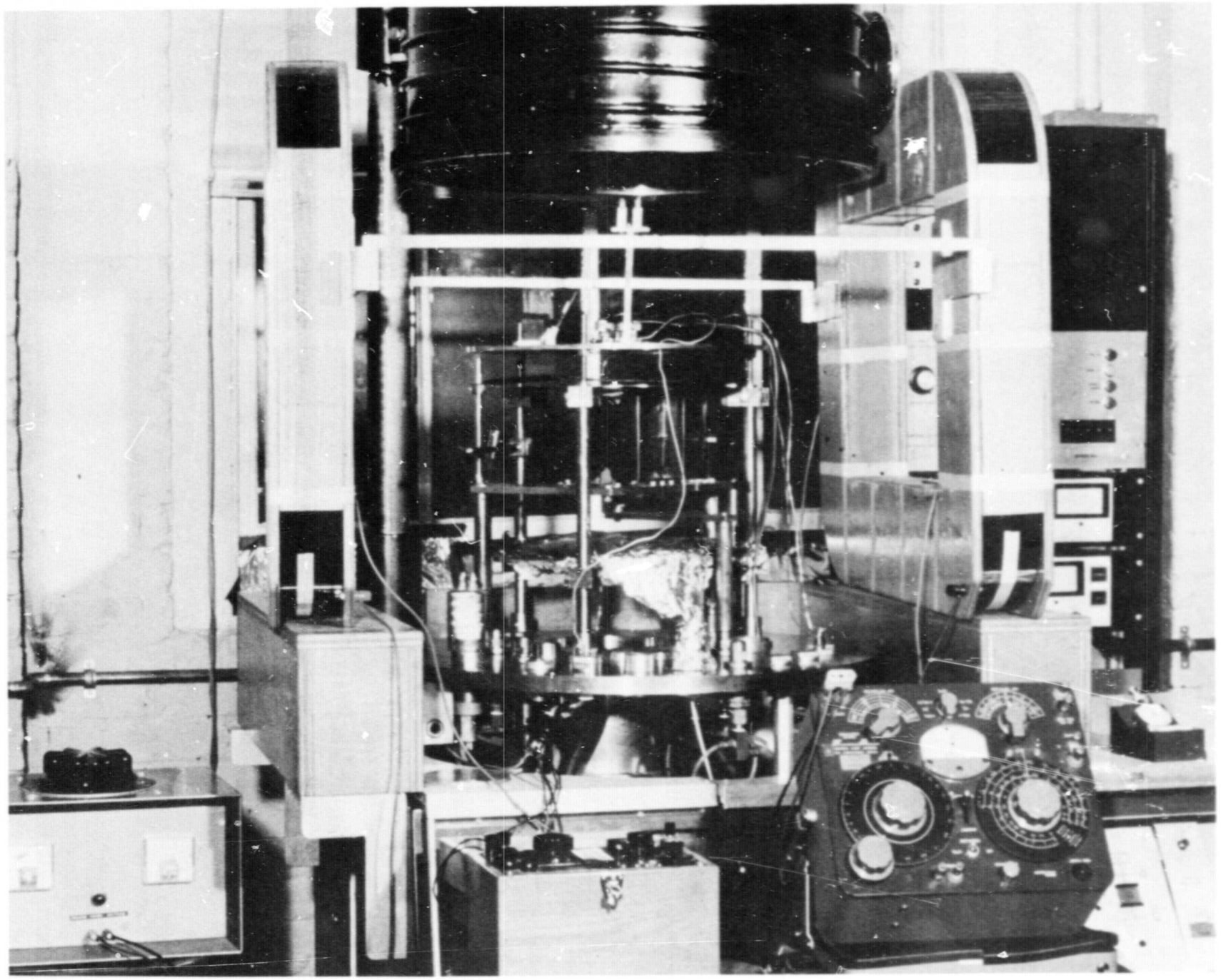


Figure 5.1 Overall View of Vacuum Evaporation Plant

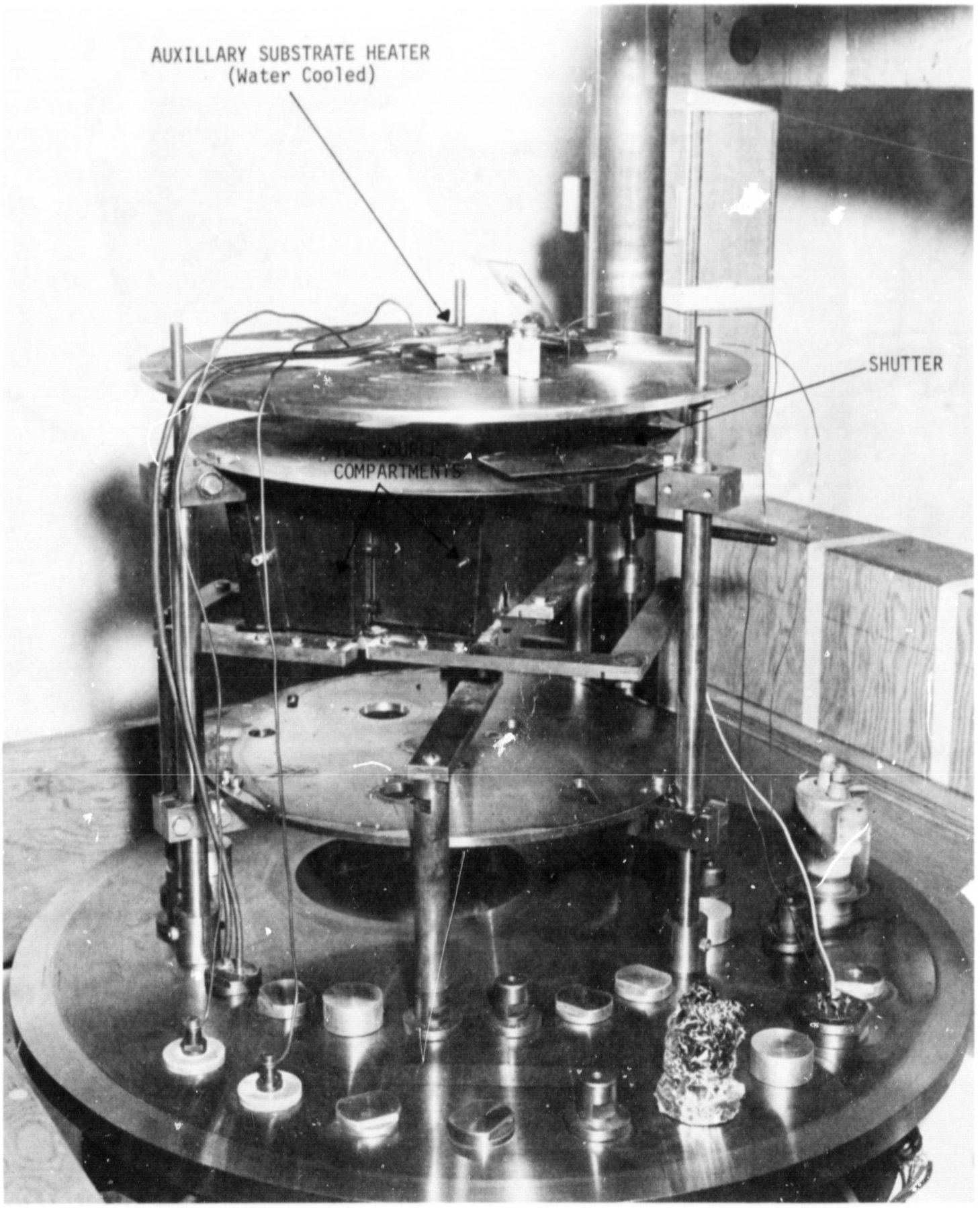
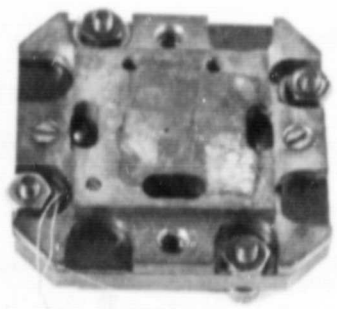


Figure 5.2 Evaporation Apparatus Inside Vacuum Chamber



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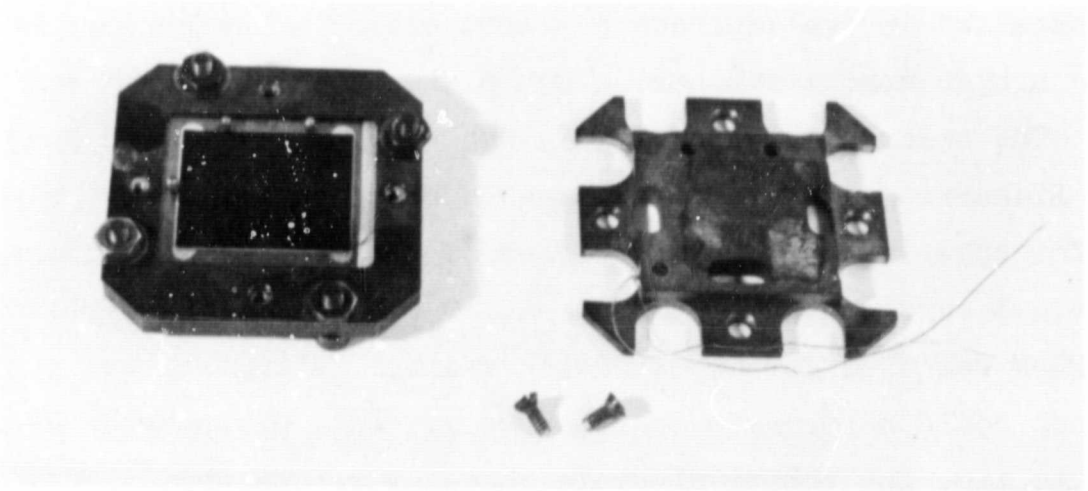

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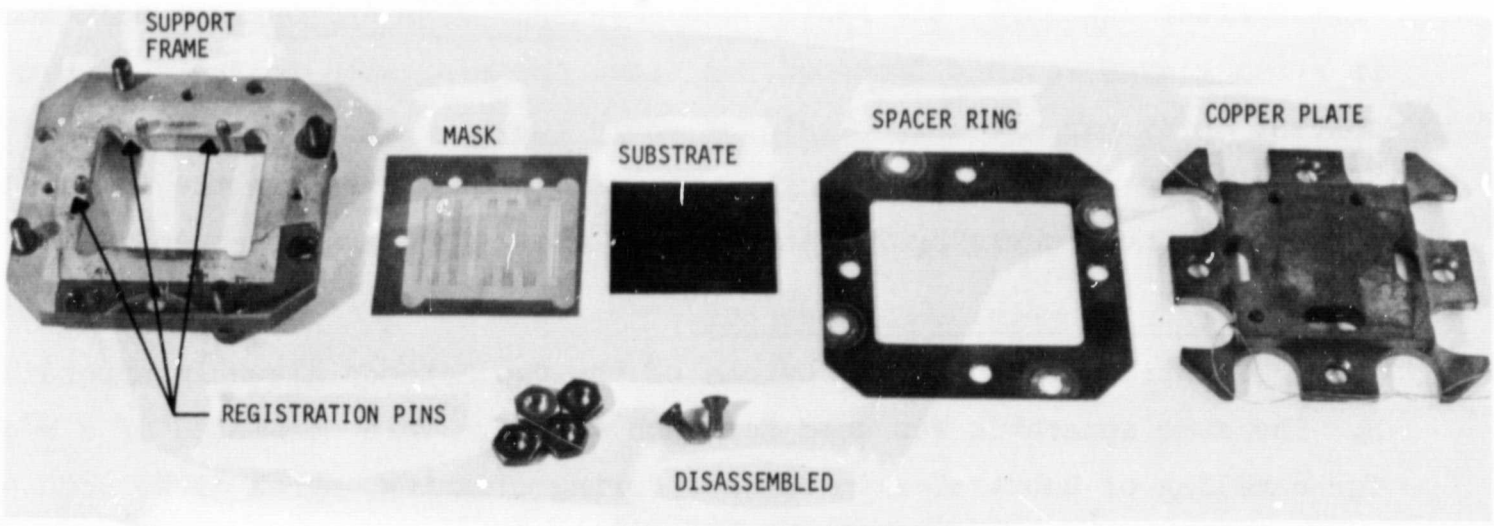


Figure 5.3 Substrate Support Fixture

between the plate and mask. A spacer ring limits the pressure on the substrate to minimize breakage. Heating of the substrate is accomplished by heating the copper plate with an auxiliary heater. Rapid cooling is provided by water flow through a cooling coil attached to the auxiliary heater. A thermocouple was fixed to the copper plate for continuous monitoring of the plate temperature during substrate baking and film deposition. While the copper plate theoretically contributed to uniform substrate heating,[13] its temperature is not necessarily an accurate indication of substrate temperature. As discussed in Section V-B-2.2 for the deposition of Cr-Au films, there can be a considerable difference between the actual substrate temperature and that of the copper plate in contact with the substrate.

2. Photo Resist Processing and Apparatus

Equipment for applying, curing, and exposing photosensitive resists was installed in two separate compartments of an ultraclean box. This included a high torque spinner, a hot plate, a vacuum frame and an exposure lamp. The spinner, model AHT2A-T, was manufactured by Headway Research, Inc., Richardson, Texas and is capable of speeds to 10,000 r.p.m. It was used for applying thin uniform coats of resist. After application, the resist was cured on a hot plate. A 100 watt mercury vapor flood lamp, G.E. type H4JM was used for exposing the resist. A shutter was employed so that the lamp could be operated continuously. At a distance of 24 inches, the exposure time for relatively thin coats of resist varied from 1 to 10 minutes, depending primarily on the type of resist. A vacuum frame was used to maintain intimate contact between photomasks and substrates during exposure.

After exposure, the resist was developed with appropriate solutions in pyrex glassware in a fumehood. A final spraying with solvents with a solvent spray gun aided in obtaining sharp images. Etching of the films and stripping of the resist images were also accomplished in the fumehood. Details of the processing for the resists used are given in Appendix G.

3. Substrate Cleaning and Apparatus

Substrate cleaning was by one of the two methods given in Appendix H. The same apparatus was used for each method. This consisted of a rack for handling of substrates in batches during cleaning, pyrex jars, hot plates, blow bottles, a filtered demineralized water rinse, and a trichloroethylene vapor degreaser. The final cleaning station is shown in Figure 5.4.

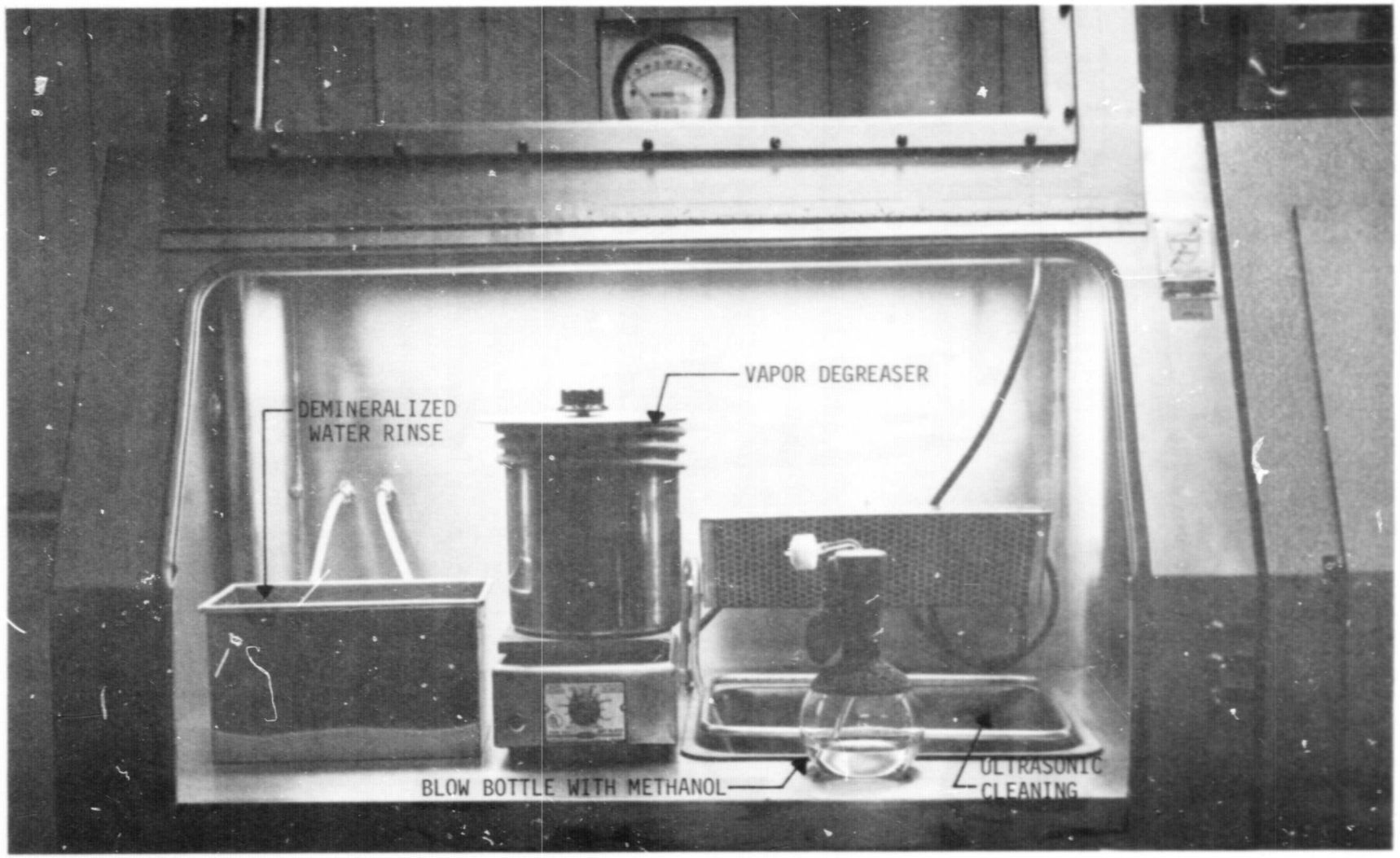


Figure 5.4 Final Cleaning Station for Substrates

The demineralized water rinse contained a Barnstead demineralizing loop, Model PL-1-C. To this a centrifugal water pump was added for circulating a supply of water through a stainless steel rinse tank. The system was charged with distilled water, U.S.P. grade. The rinsing tank was installed in a clean box and was covered with a lid when not in use. After operating for a few minutes, the resistivity of water reached a level of 15 to 18 megohms.

4. Bonding and Micromanipulating Apparatus

Two bonders were available for small lead bonding. One was for ultrasonic welding and the other for thermocompression bonding. The ultrasonic welder is the Model W-260-A manufactured by the Sonobond Corporation. The thermocompression bonder was constructed by Georgia Tech. A micromanipulator, Dumas Instrument Company Test Station Model D-300, was used for micropositioning in testing and bonding.

5. Measurements and Measurement Apparatus Employed in Memory Fabrication

Discussed are the measurements, techniques, and apparatus used for establishing process control in the deposition of films and routine measurements used during the fabrication of multilayer film structures.

5.1 Film Thickness Measurements and Apparatus. A constant deviation spectrometer, Hilger and Watts model D-186, was used in conjunction with an interferometer to measure film thickness. The interferometer is equipped with a white light source and operates on the prinicple of multiple beam interferometry[14] to produce fringes of equal chromatic order. Design is based on that described by Scott, McLauchlan and Sennett.[15]

Thickness measurements were made to establish deposition rates of SiO evaporation sources so that timed depositions at predetermined rates could be made to evaporate to a desired thickness. Also, thickness measurements were made to calibrate sources for the evaporation of permalloy films to know thickness.

5.2 Routine Fabrication Measurements. In the fabrication of multilayer film memory structures, resistance, capacitance, and magnetic measurements were made to determine the electrical and magnetic parameters of deposited films; these were made selectively at successive stages of development and aided in making corrective adjustments in the overall experimental process of building a complete memory. During the evaporation of

metal films, resistance monitoring was used to deposit to designed resistivity values. In addition to electrical and magnetic measurements, specimens were optically examined with stereomicroscopes during routine inspections of the fabrication process.

The resistance and capacitance measurements were made with an impedance bridge, General Radio Model 1650-A.

5.3 Memory Plane Test. The concept of the memory plane test is to measure the electrical characteristics of a variety of film and strip line configurations and fabrication parameters in actual memory pulse operation. Simple memory planes are fabricated by multilayer deposition in an identical sequence to the final memory. The patterns for this program consist of a series of 3 sizes of word lines and bit lines. There are three sets of word lines; the first consists of three 5 mil lines with 5 mil separation; the second has three lines 10 mil wide with 10 mil separation; and the third has three 20 mil lines with 20 mil separation. The array has three sets of bit lines as follows: 10 mil wide with 10 mil separation, 20 mil wide with 10 mil separation, and 40 mil wide with 20 mil separation.

The simple memory plane is important to the work of this contract since it provides data on creep stability, signal levels, and drive requirements for a wide range of geometric configurations. It is also a simpler structure than the final memory plane and, hence, serves as an evaluation platform for fabrication studies. In fact, most of the fabrication work done under this contract was with this simple plane structure.

The test equipment, specially designed for pulse test of the simple memory, are a test fixture and a logic generator.

Test Fixture: In this apparatus, the simple memory plane is placed into a recessed substrate holder and a special printed circuit overlay is positioned to make contact with tabs on the substrate. Current pulses and sense signal are transmitted to and from the substrate via transmission lines on the overlay. The original copper overlay was gold-plated to decrease contact resistance between transmission lines and tabs on the substrate. Tests showed that all 18 contacts between the substrate and the overlay can be simultaneously electrically connected with each contact resistance less than 0.1 ohms. By using this test fixture a simple memory plane can be pulse tested without a single soldering operation.

Logic Generator: The logic generator, which develops programmable sync pulses for memory plane evaluation, was designed and built on Radiation Incorporated's logic simulator kit Model 59105. The clock in the system was designed to operate at a pulse frequency of 100 kHz. The logic generator contains eight sequentially pulsed channels, any two of which can be expanded to have more than one pulse in each cycle. The advance of channel sequence can be controlled either automatically or manually. When automatically controlled, the number of pulses in each expanded channel in each cycle is also automatically controlled. In the manual mode, the number of pulses in each expanded channel is manually controlled.

The eight channels are sufficient to program any sync pulses required to test the simple memory plane. The output pulses from the simulator kit are amplified by a set of transistor line drivers and then connected to the sync input terminals of current pulsers. These pulsers in turn supply the drive currents to the memory plane test fixture. Figure 5.5 shows the setup of the simple memory plane test equipment.

B. FABRICATION OF MULTILAYER THIN FILM MEMORY PLANES

The studies discussed in this section were directed toward the primary objective of developing a process for fabricating a multilayer film memory plane. Two potentially feasible processes were initially designed. These differed primarily in choice of materials. Before examining the processes, certain preparations and preliminary studies were made to establish a starting point. Major efforts were then directed to adapting the processes to fabricating a memory. Several major problems ensued; most of these were systematically solved or eliminated so that much general progress was made toward meeting the objective. It is expected that the few remaining problems can be solved with minimal effort.

1. Initially Proposed Processes for Fabricating Memory

Design and the functional characteristics of the multilayer film memory plane are discussed in Section II. The word lines are 0.010" wide and on 0.020" centers, and the bit sense lines are 0.020" wide on 0.030" centers. These were arrayed in a common plane at right angles to each other to provide a total of 512 bits with 0.060" centers along the word lines and 0.020" centers in the direction of the bit lines. It was desirable that a process for fabricating the memory meet the following general

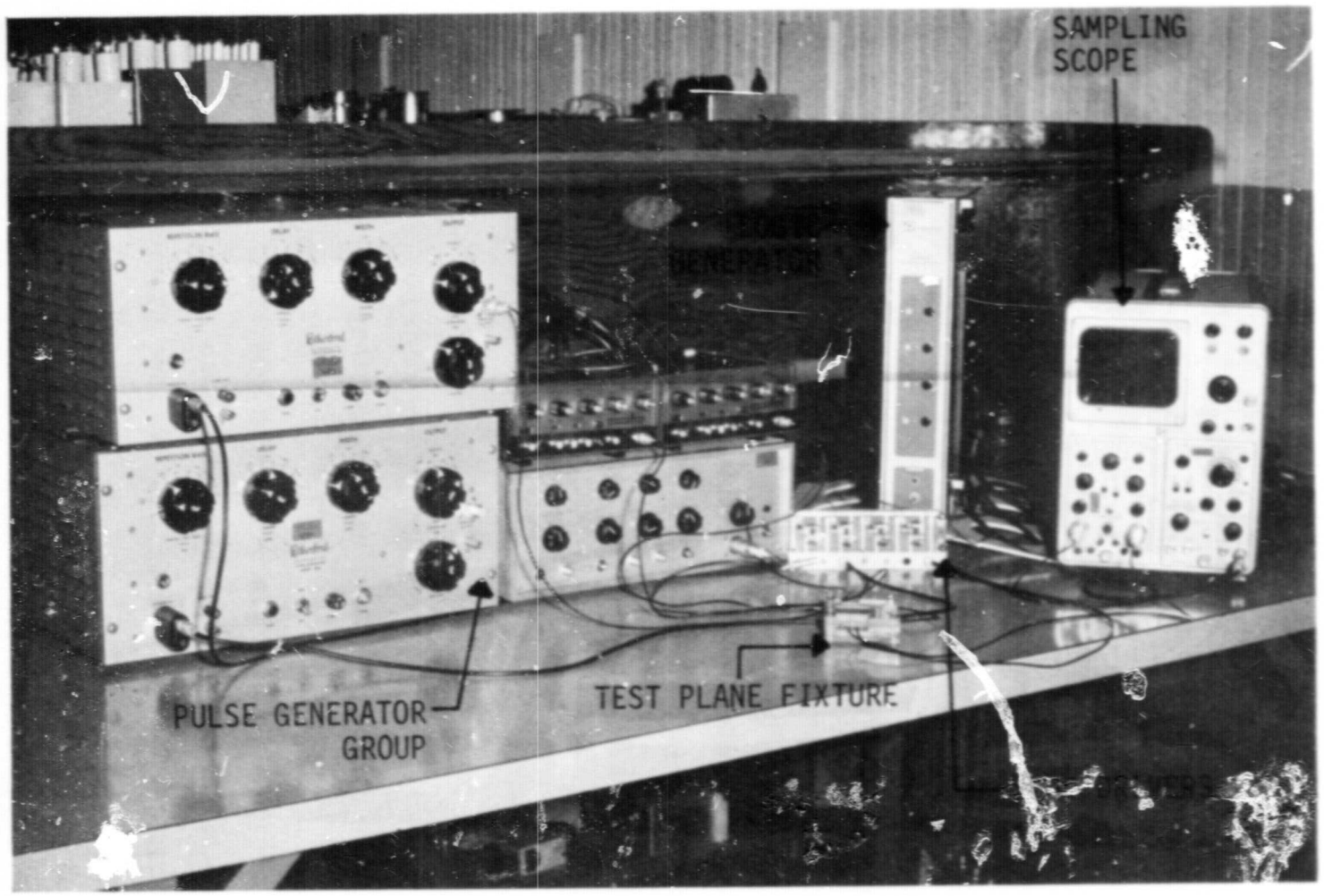


Figure 5.5 Pulse Test Facility for Simple Memory Plane

criterion:

(1) Be economical,
(2) Be capable of immediate application,
(3) Be capable of attaining the greatest feasible storage density with permalloy or similar films in a planar array of storage elements, and
(4) Be compatible with monolithic integrated circuit technology.

1.1 Substrate Materials and Other Design Features. To support the film memory, four materials were considered for substrates. These were doped silicon, fused quartz, Corning type 7059 glass, and non-corrosive soft glass microscope slides. Silicon was selected as a first choice of substrate materials for the final memory model so that memory fabrication would be most compatible with monolithic integrated circuit technology. Silicon substrates with chemically polished surfaces and doped for a low resistivity in the range 0.0004 to 0.001 ohm-cm were ordered. At first, it was thought that possibly the low resistivity silicon wafer could serve as a ground plane for the memory. Subsequent theoretical analysis however indicated the desirability of a low resistance metal film ground plane. This was included in the processes designed for experiment. It so happened that the vendor failed to supply the silicon wafers on schedule, and the order had to be cancelled. Other substrate materials were then selected in order to pursue process development. Polished fused quartz was selected as the second choice for substrate material because of its similarity to passivating films of SiO_2 on silicon and its resistance to breakage with extensive handling during fabrication. Glass substrates, Corning type 7059, were obtained as a third choice. All of the process studies were made with fused quartz and glass substrates; and, in the final process analysis, glass was actually selected over fused quartz due to certain difficulties experienced with the quartz. These difficulties are discussed subsequently.

substrate size of 1.5" x 1.25" x 0.025" was selected for the memory. This size was slightly larger in width than that needed for the actual storage matrix. The extra substrate area was for film buss lines and selection diodes. General Instrument type 10-XH100 beam lead diodes were used. These are bonded to the mating buss and word lines. Figure 5.6 shows one of the diodes bonded to mating lines. Inclusion of the buss lines and selection diodes on the substrate with the memory resulted in a neat

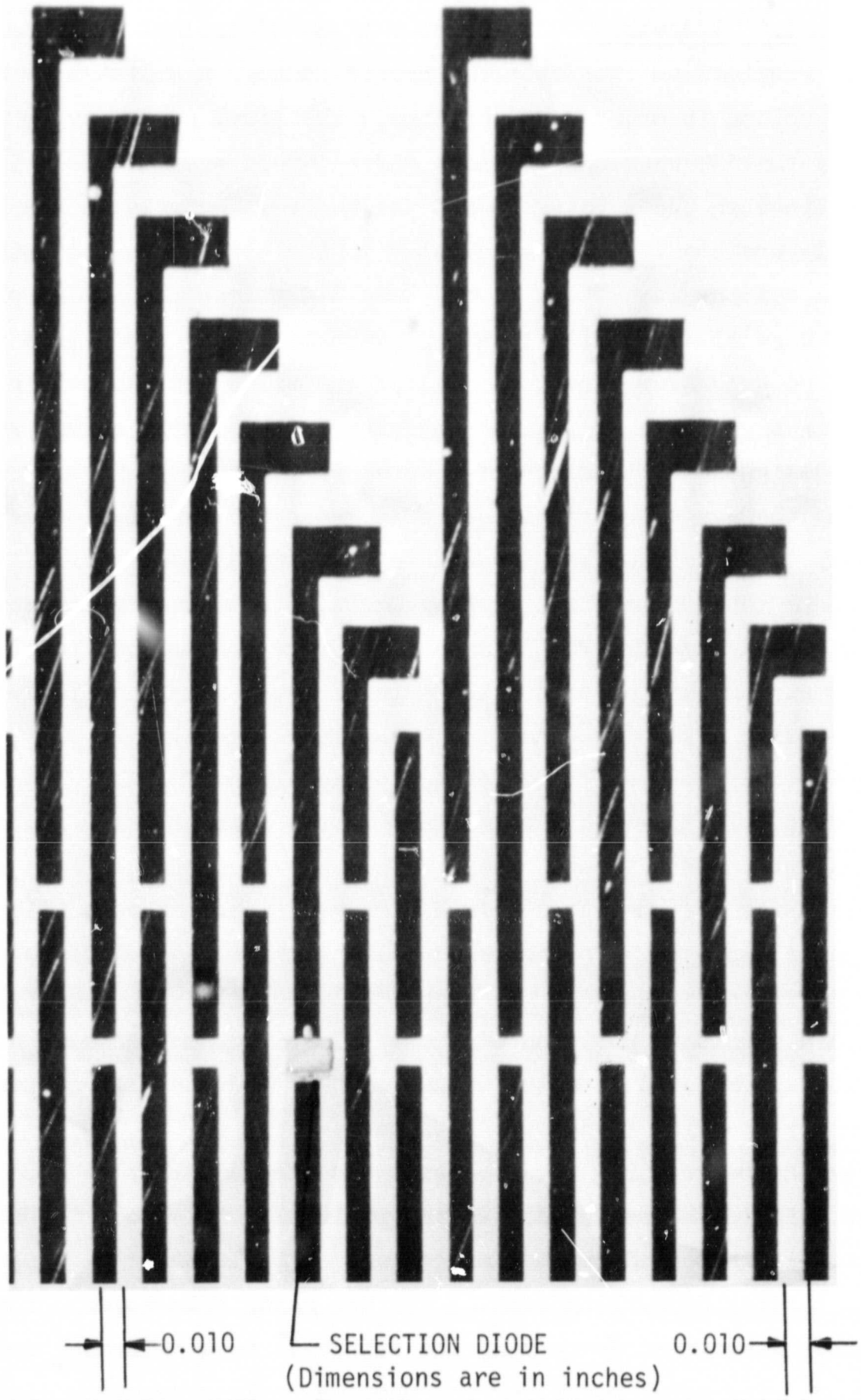


Figure 5.6 A Partial View of Word Line Pattern of Model Memory with Selection Diode Bonded to Gold Over Chromium Film

hybrid package that simplified interconnections from the memory to the driving and sensing electronics.

1.2 Process A. A general outline of process A appears in Table 5A. Films required to fabricate the hybrid package are listed in the first vertical column in order of deposition. The first seven layers make up the memory matrix; whereas, the last three layers resulted from including the buss lines on the substrate with the memory. Details on the respective film layers are listed horizontally in the table. As indicated in the material column, insulating layers were SiO films; the ground plane and bit lines were aluminum films; and the word lines and buss lines were bilayer films of gold over chromium. All of the films were deposited by evaporation in high vacuum. This is indicated in the third column where the general design specifications of the respective film properties are given also. During the evaporations of each film, contact transmission metal masks were employed to restrict the deposit to definite areas or to define a line pattern. A total of eight difference metal masks were required to deposit all of the film layers. The film patterns were defined completely with the contact metal masks for six of the layers; these were the SiO layers, the 8th or adhesive layer (Cr), and the buss lines (Cr-Au). However, the dimensional tolerances and line resolution specified for the ground plane, storage film, bit lines, and word lines in the memory design could not be obtained with contact metal masks. This was demonstrated in a series of experiments designed to determine transmission mask resolution for the type of masks employed. To insure adequate dimensional tolerance and resolution, the decision was made to use high resolution glass photomasks and to photoengrave precision patterns of these films. To photoengrave a film, the substrate was removed from the vacuum system, and the film pattern was etched before proceeding to deposit subsequent films in the layered structure. After photoengraving, the substrate was cleaned prior to deposition of the next film in the sequence. Where applicable, this post deposition fabrication is indicated in the last column of Table 5A.

After depositing each of the ten major film layers, the vacuum chamber was opened for moving the substrate to a different source position, for changing metal masks, or for photoengraving; however, cleaning of the substrate was not required unless photoengraving was involved. These interruptions in the vacuum processing were advantageous in many respects

TABLE 5A

Process A

	Film Layers in Order of Deposition	Material	Film Deposition	Post Deposition Fabrication
1.	Insulation and/or Smoothing	SiO	Evaporate thru transmission metal mask #1 to coat entire substrate surface to a thickness of 2 to 3 μ for smoothing and/or insulation.	NONE
2.	Ground Plane	Al	Evaporate thru transmission metal mask #1 to a sheet resistivity ≦ 0.015 ohm per square	Photoengrave Ground Plane
3.	Insulation	SiO	Evaporate over ground plane thru transmission metal mask #2 to a minimum thickness of 2 μ for d.c. insulation between ground plane and subsequent metal films.	NONE
4.	Storage or Magnetic Film	Permalloy	Evaporate Ni-Fe (81-19) thru transmission metal mask #3 to a thickness of 750Å with magnetic parameters of $H_K \leqq 4$ oe, H_c/H_k = 0.5 to 1, and dispersion plus skew not more than ± 3 degrees.	Photoengrave Storage Film
5.	Bit Sense Film	Al	Evaporate thru transmission metal mask #4 to a sheet resistivity ≦ 0.015 ohm per square or less.	Photoengrave Sense Lines
6.	Insulation	SiO	Evaporate over bit lines and ground plane thru transmission metal mask #5 to a minimum thickness of 2 μ for d.c. insulation between bit lines and subsequent metal films and for additional insulation between ground plane and subsequent metal films.	NONE

TABLE 5A (Continued)

Process A

	Film Layers in Order of Deposition	Material	Film Deposition	Post Deposition Fabrication
7.	Word Film	Cr-Au	Evaporate a bilayer film of gold over chromium thru transmission metal mask #6 to a resistivity ≦ 0.015 ohm per square with the initial Cr film thickness equal to 500 to 1000 Å.	
8.	Adhesive Layer	Cr	Evaporate thru transmission metal mask #7 (same mask as for film No. 9) to a thickness of 500 to 1000 Å over area of film #7 to be coated with insulating film #9.	Photoengrave Word Lines
9.	Insulation	SiO	Evaporate thru transmission metal mask #7 for selective d.c. insulation between word lines and buss lines.	NONE
10.	Buss Lines	Cr-Au	Using transmission metal mask #8 to define buss line pattern, evaporate film of gold over chromium as for word lines.	Bond selection diodes to word lines

since each film could be inspected before proceeding to deposit subsequent films in the sequence.

1.3 Process B. The general procedures for process B were similar to process A. The primary difference in the two processes was that in process B the ground plane and bit lines were trilayer metal films of Cr-Au-Cr instead of aluminum films as in process A. The notation Cr-Au-Cr is used to indicate that a gold film was sandwiched between two films of chromium. Deposition was similar to that of the Cr-Au for word lines in process A; that is, the chromium films were from 500 to 1000 angstroms thick, and the gold was deposited for a sheet resistivity of about 0.015 ohm per square. The chromium and gold were deposited successively from independently controlled sources in juxtaposition.

1.4 Comments on the Proposed Processes. At this point, there may be some questions with regards to the materials and methods that were selected for the proposed processes, and some explanation is in order. It was stipulated that vacuum evaporation techniques would be employed to fabricate the film layers of the memory. From a fabrication standpoint, several problem areas were anticipated. Paramount among these were (1) mechanical instability of the differing materials combined in a multilayer structure of so many film layers, and this being compounded because of the relatively large thickness of eight out of ten layers to be deposited by evaporation, (2) shorting between the extensive area of metal films and the numerous metal film crossovers to be insulated, (3) the possibilities of destroying magnetic properties of the storage film during the film processing following its deposition, and (4) interconnections between the memory and its driving and sensing electronics. There was considerable conflict in making a selection of materials. Hardly any one metal film could be selected for the conductive films with properties that satisfied best the conditions presented by all four problem areas; as a consequence, considerable compromising between these problems and other desired features was made with near certainty that some modifications of the processes would be required.

Several properties of silicon monoxide make it nearly an ideal choice for the insulating films in the memory. The most attractive of these are its ease of evaporation, its superior adherence to most metals and to glass and quartz, its dramatic smoothing effects on surfaces when deposited sufficiently thick, its potentially high dielectric strength, its relatively

low dielectric constant, and its anhydros nature and general inertness. A minimum thickness of about 2 μ was required for the SiO films in order to limit the capacitance between the various metal films. To provide uniform dielectric films especially with reliable d.c. insulation at the numerous conductor crossover points by evaporation was considered a major problem, and to a large extent this would determine the necessary thickness regardless of the dielectric material selected. The problem was complicated by the fact that the conductive films were relatively thick and their edges were sharply defined as a result of photoengraving. To mask these effectively, it appeared desirable to design a broad evaporation source. This was done with apparent success. The source is discussed subsequently in the section on incidental studies.

The selection of aluminum for conductive films in process A was based upon several factors, the most important being its low resistivity, good adherence to SiO, and relatively low stress on the SiO films. The latter feature was considered important for minimizing shorts between metal films. Since aluminum can be anodized, anodization of aluminum films before deposition of the SiO in order to improve d.c. insulation at crossovers was an alternate choice; however, this was not resorted to in the subsequent work. Gold was selected for the word line in order to assure a reliable bond between the diode beam leads and the line. The choice of gold also eliminated the possibility of contact resistance at points of direct contact between the successively deposited films for word and buss lines that would unavoidably occur with surface oxide formation on aluminum word lines. The adherence of gold to SiO was considered insufficient to meet stability requirements and the stresses of bonding, and a thin layer of chromium was used to provide adequate adherence at gold to SiO interfaces. This resulted in the bilayer Cr-Au films and trilayer Cr-Au-Cr films in processes A and B.

There were some reservations concerning process A where the aluminum film bit lines are in direct contact with the permalloy storage films. It was feared that the two films would alloy and destroy the magnetic properties of the permalloy, and this did occur in subsequent work. This was the primary reason for designing two processes. Cr-Au-Cr films were selected for bit line in the second process, and in order to minimize the number of different materials, chromium and gold were selected for all of the metal film layers. Choosing the chromium-gold system for all of the conductive

layers also resulted in a greater flexibility for making connections from terminals of the hybrid memory package to the mother board since soldering as well as ultrasonic or thermal compression bonding techniques could be employed. In addition, hot sulfuric or chromic acid could be used to obtain superior cleaning of chromium-gold films after photoengraving.

Primarily, the discussions so far have pertained to processing the 512 bit memory. Actually masks were prepared for two different planes. The pulse test plane of 27 bits was designed for determining preferred line widths and spacings for the bit and word lines and dielectric film thickness; this is referred to as the Simple Test Plane to make distinction between it and the more complex 512 bit array. It has been previously described in Section A-5.3. Besides bit density, the basic difference between it and the larger memory was that the simple plane consisted of only the first seven film layers of process A as described in Table 5A. The buss lines and switching diodes were not included on the simple test memory. Most of the process development was done using the simple memory structure following the procedures outlined for fabricating the 512 bit memory.

An "insitu" process would be ideal for fabricating such a complicated film structure. In such a process, the vacuum apparatus would be designed to interchange contact masks and substrates and select evaporation sources so that the memory could be fabricated by successively depositing the various film patterns in registration in a single evacuation of the vacuum chamber. The complications introduced by the photoengraving in the proposed processes would be eliminated resulting in a cleaner process requiring less time for completion. However, the feasible bit density attainable with transmission metal masks in an insitu process was considered to be too low. It thus seemed profitable to pursue the more complicated process which ultimately will allow for a much greater bit density.

Certain general principles were considered necessary to fabricate a reliable multilayer film memory; these guided the approach to effecting the processes. It was decided that all film evaporations would be made at pressures in the 10^{-5} to 10^{-7} torr range. Substrate temperatures during deposition had to be sufficiently high to relieve as much stress within and between the various film layers as possible. This was particularly true for SiO films which will reticulate if deposited at temperatures much below 250° C. It was known that the desired magnetic properties for the permalloy

films could be obtained for films deposited on substrates at some temperature in the range of 300° C to 450° C. Thus, the plan was to establish a preferred substrate temperature for the particular vacuum apparatus used to deposit the permalloy film. All film depositions before the permalloy would be made at or above this substrate temperature; all film depositions after the permalloy would be made at substrate temperatures equal to or preferrably below the permalloy temperature. It was not known for sure if applied magnetic fields would be required to prevent excessive degradiation of the magnetic parameters with heating during the film depositions following the permalloy. Among other things, post-deposition annealing effects on the permalloy had to be determined. High rate evaporation sources were desirable for depositing the thicker films, and considerably attention was given to source designs for evaporating the various materials. Preferred photoengraving techniques for the particular combinations of films had to be developed also. Thus, many details had to be resolved in order to develop a satisfactory process; the results of these studies are discussed in the following paragraphs.

2. Incidental Studies and Preparation for Multilayer Film Memory Fabrication

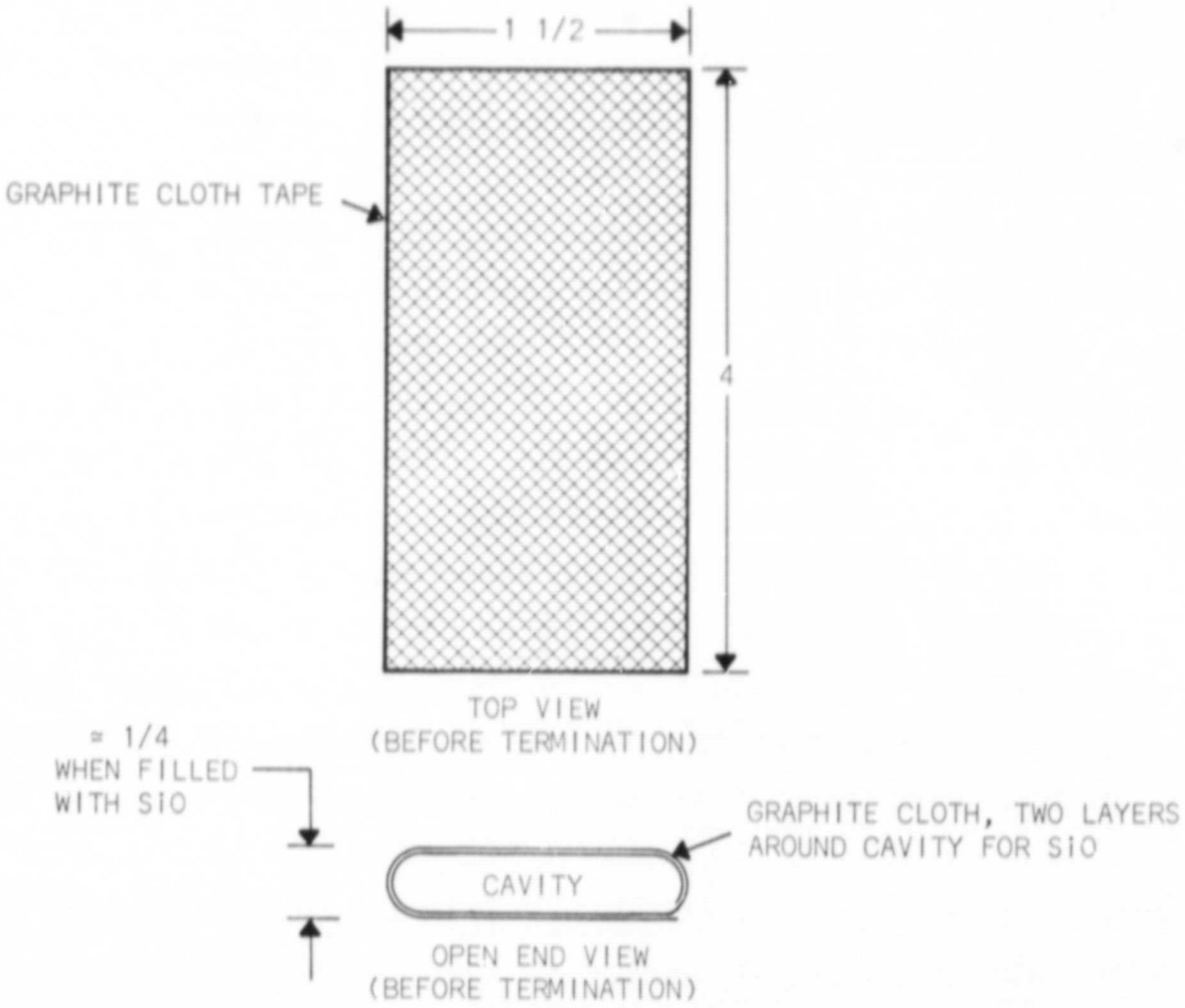
The apparatus and general procedures for film fabrication are discussed in Section V-A. In this section, vacuum evaporation and other process studies preceding efforts to fabricate a complete memory with the proposed processes are discussed in detail. Included also are discussions on the artwork and masks for memory fabrication and a study on the resolution of transmission metal masks. Glass substrates were used for all of the exploratory film studies in this section.

2.1 Development of Evaporation Source for SiO. The metal films of the memory requiring insulation were about 2 μ thick, and the edges of the numerous crossing paths (crossovers) that required d.c. insulation were sharply defined as a result of photoengraving. As discussed previously, evaporated SiO films were selected for insulation. Highly directional sources are unsatisfactory for evaporating the SiO on stationary substrates since shadowing effects occur at the steep edges of the metal films. Hence SiO films of excessive thickness, on the average, are required to obtain adequate insulation at the crossovers. Since deposition apparatus was designed to accommodate a stationary substrate, the easiest method of minimizing the shadowing effects was to design a sufficiently broad source to evaporate the SiO from a fixed position.

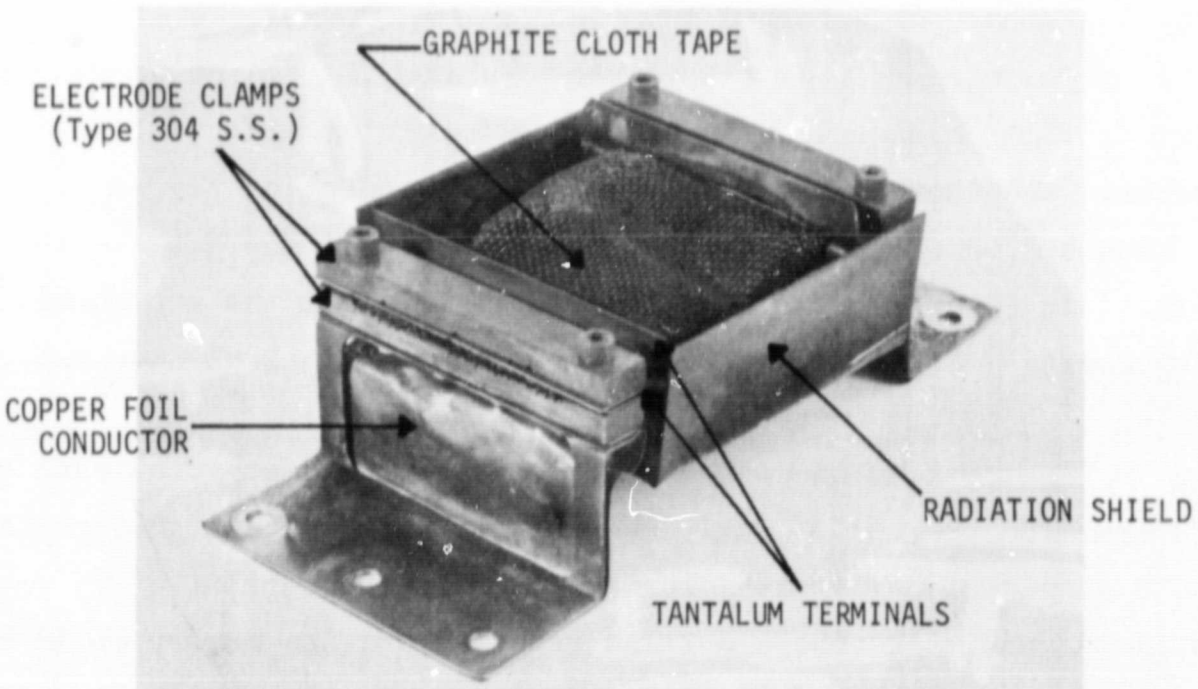
Graphite cloth was used to construct a broad source for evaporating SiO. Its resistivity is high compared to suitable refractory metals; thus, relatively low currents were required for I^2R heating and a broad source can be operated without overloading the current feedthrus of the vacuum system. In addition, the well known ejection ("spitting") of the SiO particles during heating is eliminated by enclosing SiO particles within densely woven cloth. Union Carbide grade WCB graphite tape 4 inches in width was selected for constructing the source. The sheet resistivity of this grade is approximately $\frac{1}{2}$ ohm per square. A length of 7 inches was folded as indicated in Figure 5.7a to form a cavity. This was filled with SiO particles, and the two open ends were terminated with electrodes so that the planar area of the source exposed to the substrate was 1.5" x 1.5". Tantalum terminations were used since the graphite cloth operates at near full temperature right up to the electrode connections. A molybdenum radiation shield limited heat radiation from the sides and bottom of the source. Figure 5.7b is a photograph of the completed source structure. When fully loaded, the source held about 20 grams of SiO particles ranging in size from 20 mesh to $\frac{1}{4}$ of an inch in breadth, and a new graphite element was installed with each new charge or renewal of the SiO charge.

Evaporations of SiO were made with the two source to substrate geometries of Figure 5.8 to compare the uniformity of films deposited. Substrate temperatures ranged from 300°C to 450°C and all of the films were strongly adherent. For both of the "A" and "B" source to substrate geometries, film thickness varied 20 percent over an area of 1.5 inches in diameter. The variation in each case was dependent on the radius with respect to the center of the substrate but in an almost opposite sense as illustrated in Figure 5.9. The primary difference in the geometries was that for source "B" the source to substrate distance is shorter and the 1-5/8" x 1-5/8" aperture introduced a stopping effect.

Figure 5.10 shows the dependence of the deposition rate on source current for source "B" fully charged with SiO. The high deposition rate of 4000 angstroms per minute obtained at a source current of 75 amps was very satisfactory since the 2 μ films required for the memory could be deposited in 5 minutes. Most of the literature reports much lower deposition rates for high quality SiO films. To insure that the insulation quality of the SiO was satisfactory at the higher rate of deposition, a few thin film capacitors were fabricated with aluminum film plates. The SiO dielectric

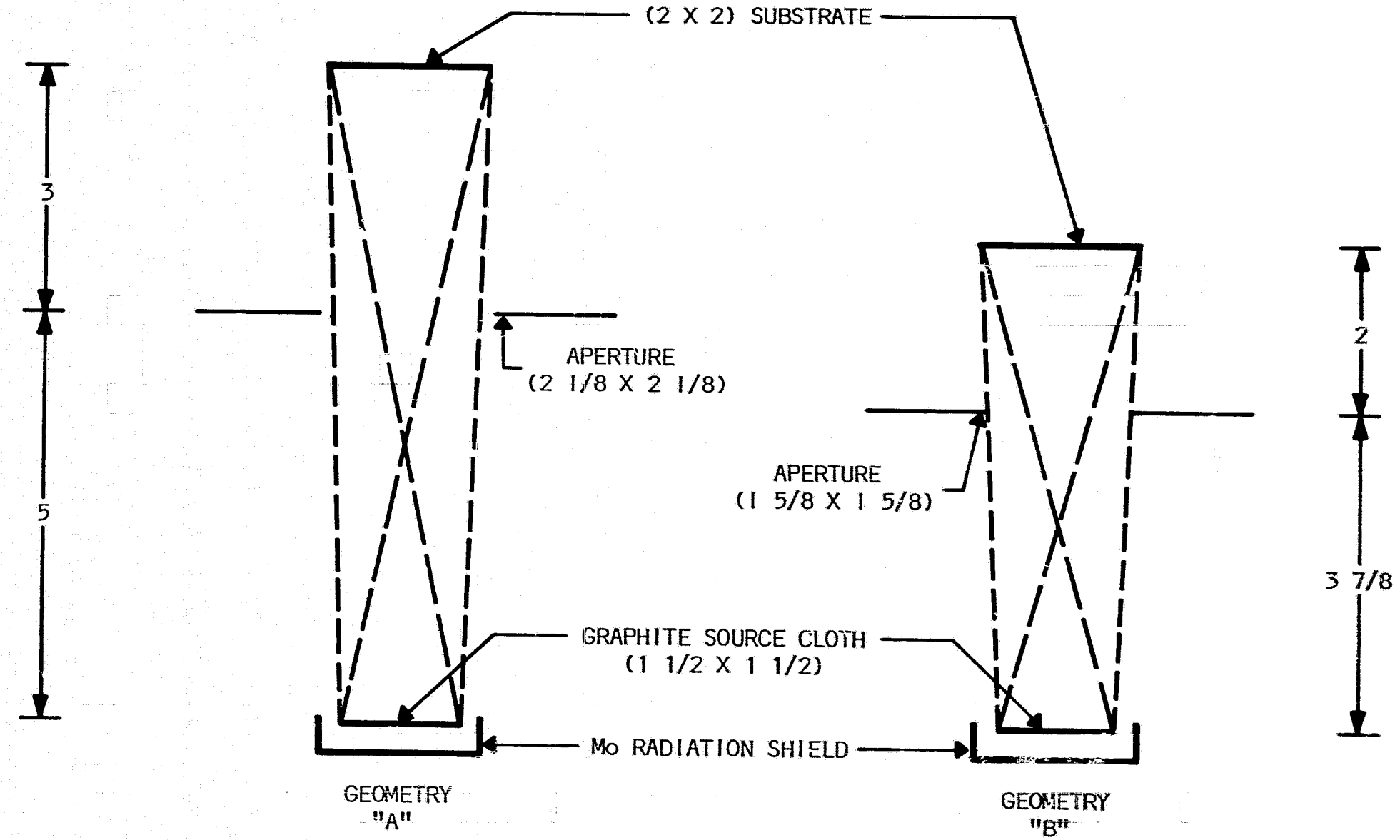


(a) Folding of Graphite Cloth Tape



b. Photograph of SiO Source

Figure 5.7 Broad Source for Evaporating SiO



(Dimensions are in inches)

Figure 5.8 SiO Source to Substrate Geometries for Film Uniformity Studies

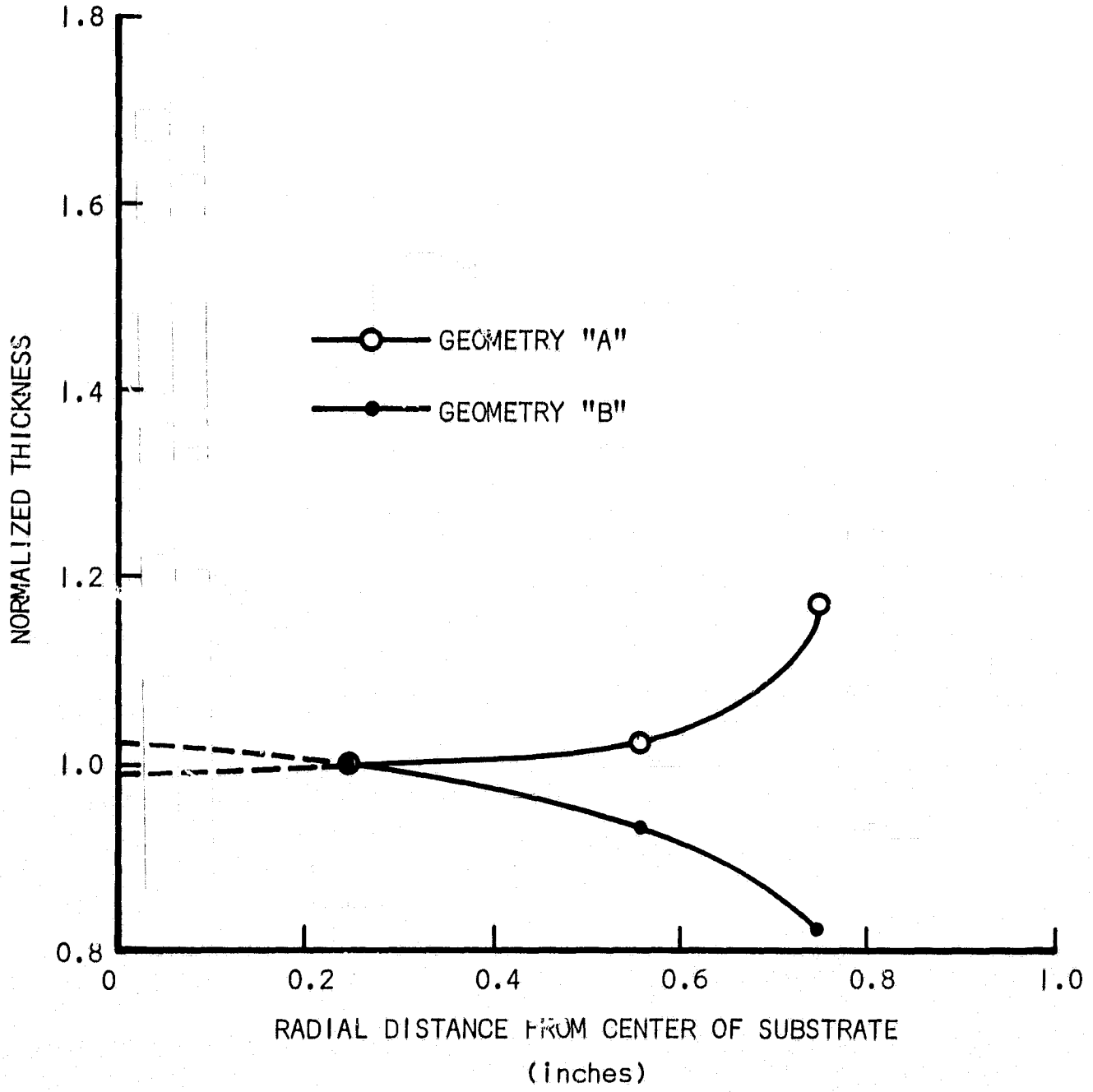


Figure 5.9 Uniformity of SiO Films for Source to Substrate Geometries "A" and "B"

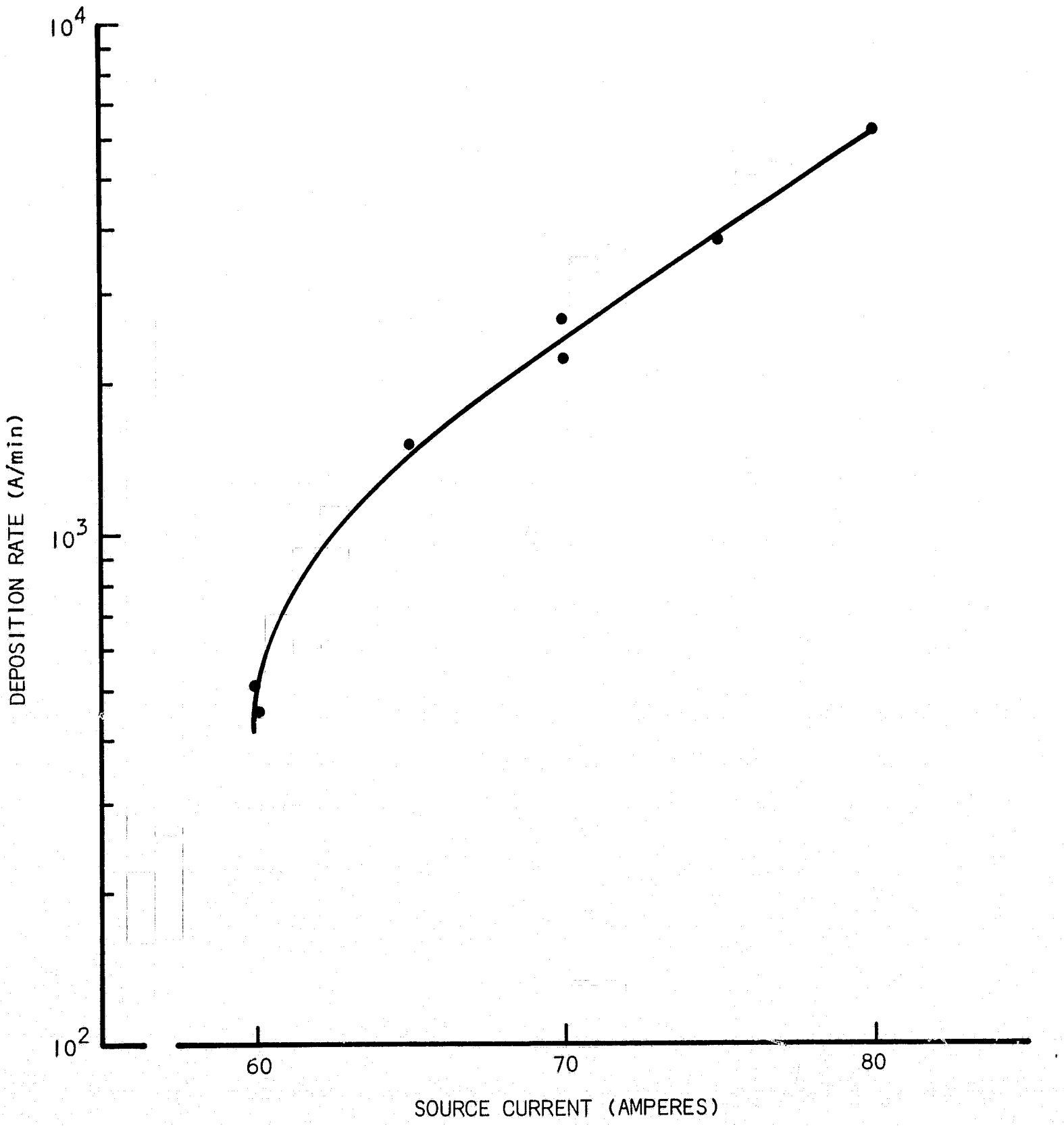


Figure 5.10 Dependence of Deposition Rate on Source Current for SiO Source

was evaporated at the 4000 angstroms per minute rate at a substrate temperature of about 350° C. Each capacitor had an area of one square centimeter, and the dissipation factors ranged from 0.01 to 0.02 for capacitance values of about 0.01 mf. This was considered quite good so the source was considered satisfactory to evaporate SiO films for the memory.

A load of 20 grams of SiO was depleted in a time equivalent to about 2.5 hours of operation at 75 amps. An accurate calibration of the change in evaporation rate with extended use was not obtained. However, it was determined that the rate after evaporating for the equivalent of 1 hour at 75 amps was about double that obtained initially at full load. In actual use, timed evaporations could be made to deposit to an approximate desired thickness until the thicknesses of the films deposited totaled about 70 to 90 μ with the Source "B" geometry. Thereafter, the evaporation rate of the source dropped sharply, and a new graphite element and SiO load were required.

2.2 Evaporation Sources and Methods for Aluminum and Chromium-Gold Films. Except for the ground plane, all of the conductive films (bit, word, and buss lines) crossed the edges of previously deposited films. In order to minimize shadowing effects at the edges of previously deposited films, broad evaporation sources were desirable. This condition was simulated during memory fabrication by evaporating simultaneously from two tungsten basket or three tungsten boat sources, respectively, for aluminum and chromium-gold. Other methods of evaporating aluminum were tried and rejected. A sheet resistivity in the range of 0.01 to 0.015 ohms per square was desired for the conductive films. The manner in which this was achieved for the aluminum and chromium-gold films is discussed in the following paragraphs.

Several attempts were made to evaporate aluminum from a copper crucible with a broad beam electron beam gun. This proved to be difficult. Before reaching the evaporating temperature range, outgassing of the aluminum jettisoned the melt from the crucible. This occurred even after long periods of outgassing so other methods of evaporating aluminum were sought.

It was desirable that the aluminum source have a large capacity so that successive depositions could be made without reloading or changing sources after each deposition. Other work[16] at Georgia Tech indicated that boron nitride crucibles could be used for large capacity aluminum

sources. Several crucibles were machined from 3/8" O.D. boron nitride rod. The overall length of these was 1.5 inches, and a 3/16 inch diameter center bore to a depth of 1.25 inches formed the cavity. The outside of the crucibles were threaded for a helical tantalum wire heater. A few turns of the helix extended above the mouth of the crucible to minimize migration of molten aluminum over the mouth of the crucible. A rather complex procedure had to be followed during melting and evaporating the aluminum to prevent migration of the aluminum out of the crucible mouth and over the outside walls; even then, the maximum deposition rate that could be obtained from a single crucible was 1000 angstroms per minute for a source to substrate distance of 8 inches. In addition, the life of the crucibles were shorter than expected due to the occurrence of cracks in the walls after a few evaporations. This permitted molten aluminum to migrate through the walls and destroy the tantalum helix. In general, the crucibles were unsatisfactory for the intended purpose.

The evaporation source finally selected for aluminum was a pair of commercially available stranded tungsten baskets, R.D. Mathis type B12A-3X .025W. These were installed in the vacuum chamber at a distance of 6 inches below the substrate with the two baskets connected in parallel across a current source and physically separated approximately 1.75 inches. To calibrate the source, a series of films were deposited by completely evaporating various lengths of 0.010 inch diameter aluminum wire (99.999% purity) and determining the sheet resistivity of the films. The wire length was equally divided between the two baskets. For these films, the copper plate substrate heater discussed in Section V-A-1.2 was maintained at 350° C. A film resistivity of 0.013 ohms per square was obtained for the complete evaporation of 20 feet of wire for an evaporation time of 2 to 3 minutes. In evaluating process A, all of the aluminum films were deposited by evaporating 20 feet of 0.010 inch diameter wire.

Tungsten boats, R.D. Mathis type S8A-.005W, were selected for evaporating chromium-gold films. For the gold, two of the boats were installed in the vacuum chamber at a distance of 6 inches below the substrates. The sources were connected in parallel across the current source and physically separated 1.75 inches. A third boat for evaporating chromium was centered about 1 inch below these and connected to a second current source.

To establish the rate of deposition for the chromium source, the boat was filled with vacuum outgassed chromium granules (99.9%) of

approximately 3 to 4.5 mm in breadth. Thickness measurements indicated that a deposition rate of 600 angstroms per minute was obtained at a source current of 150 amps. In subsequent work, evaporations were made at this source current using the established rate to determine the time for depositing to a desired thickness.

For gold over chromium films, the thin chromium film was deposited first to a thickness in the range of 500 to 100 angstroms, and after a brief interruption of about 30 seconds the gold was evaporated. Resistance monitoring was used to make controlled depositions to the target resistivity of 0.010 to 0.015 ohm per square. The contribution of the relatively thin chromium film to the resistivity of the bilayer film was insignificant. A series of gold over chromium films were deposited to the target resistivity with the copper substrate heater maintained at 350° C and the source current adjusted for an evaporation period of 12 minutes. However, the temperature of the source was too high, and excessive outgassing caused some spitting of the melt. In addition, the surface of these films were dull in appearance (agglomerated) which indicated that the substrate temperature was considerably higher than that of the copper substrate holder.

To eliminate spitting of the gold the source temperature was decreased for an evaporation time of about 25 minutes for film resistivities in the range of 0.010 to 0.015 ohm per square. With the copper substrate holder (see Figure 5.3 and Section V-A-1.2) maintained at 350° C during these longer depositions, the outer surface of the gold was agglomerated to the extent that in some instances it appeared black. For this to occur, the substrate temperature was probably near or in excess of 500° C. Thus, the temperature of the copper plate heater in contact with the substrate could not be depended on for an accurate indication of substrate temperature during the extended gold evaporations. Reducing the temperature of the copper plate to 200° C during gold evaporations eliminated the agglomeration. The procedure followed in practice was to heat the substrate to 450° C or 350° C for cleaning and then cool to 200° C for depositing the Cr-Au.

2.3 Permalloy Film Studies. One of the first objectives was to determine the evaporation method and optimum evaporation parameters for the permalloy films since these would limit to some extent the deposition parameters, especially substrate temperature, of other films of the memory. As evidenced by the variation of data found in the literature, it is necessary

to optimize deposition parameters according to a particular system since temperature measuring and evaporating techniques differ from one installation to the next. In these studies the vacuum apparatus of Figure 5.1 was employed. The Helmholtz coils used for applying a magnetic field during film fabrication were positioned outside the vacuum chamber so that the direction of the applied field was approximately parallel with the earths field. All magnetic data on the films were taken on the Kerr effect hysteresograph, and dispersion measurements were made by the conventional cross field technique.

Electron beam evaporation was the first method examined to evaporate permalloy. In these experiments, the permalloy was evaporated from a cool copper crucible with a crucible to substrate distance of 8.5 inches. The first difficulty experienced was nonuniformity of the films due to electron and/or ion charge effects at the substrate surface during evaporation. The nonuniformity was observable as a characteristic spot pattern of greater transparency than remaining portions of the films with size and shape that were dependent on the geometry of the transmission metal mask used during evaporation. These effects were eliminated by positively biasing a collector ring positioned near the front surface of the substrate. Uniform films were obtained with the ring biased at +300 to +600 v.d.c. with respect to the substrate holder and baseplate. At elevated substrate temperatures near 450° C, spot patterns did not occur in the absence of the biased collector ring. At these temperatures, apparently the resistance of the soft glass substrates was sufficiently low to prevent the surface from becoming charged.

The maximum deposition rate obtained during the electron beam studies was 300 to 500 angstroms per minute at the stated crucible to substrate distance. Increasing the beam power to increase the rate was unsuccessful due to excessive outgassing which caused spitting or ejection of the melt from the crucible. Higher rates of deposition were desirable; therefore, this method of evaporating the permalloy was eliminated from further consideration.

A series of permalloy films was fabricated with tungsten basket sources (R.D. Mathis type B12A - 3 X .030 W). The source to substrate distance was 6 inches and glass substrates were used. Measurements of H_c, H_k, 50% dispersion angle (α_{50}), and skew (β) as a function of substrate temperature and applied field strength were made. The effect of SiO smoothing

layers was also investigated. Included in these studies were some 23 film samples. These were fabricated before the substrate holder of Figure 5.3 was available, and some difficulty was experienced in accurately reproducing substrate temperatures. As a result, the data were scattered; nevertheless a number of valid conclusions were obtained.

First, a substrate temperature corresponding to that of a substrate in contact with a metal plate at 425° C appeared desirable in order to achieve low dispersion with reasonable H_c/H_k ratio. At this temperature, typical values of H_c, H_c/H_k, and α_{50} were 2 oe, 0.6, and 0.7°, respectively.

A second conclusion drawn from these data was that an applied field during deposition of 27 Oersted was satisfactory. The data, taken for an applied field range of zero to 60 Oersted showed increasing dispersion with decreasing field and very large data spread at or below 13.5 Oersted, indicating poor reproducibility. As the field was increased to 60 Oersted the dispersion decreased, but the H_c/H_k ratio also decreased. A satisfactory compromise between low dispersion and high H_c/H_k was obtained for a field strength of 27 Oersted.

Evaporation history of a basket had a significant influence on film properties. After 4 or 5 evaporations in succession from the same basket, the film dispersion increased to undesirable large values. It was observed that the rate of evaporation increased as the number of evaporations were made from a single basket increased. The cause for this was that during each evaporation a small portion of the permalloy charge alloyed with the basket. This caused the surface of the tungsten to increase in roughness with successive evaporations. Accordingly, the basket temperature had to be increased above the melting point of the permalloy before melting occurred. The evaporation rate of permalloy increases rapidly at temperatures above its melting point, and the temperature required after about 5 evaporations was so much greater than the melting point that once the permalloy began to melt the whole charge was essentially flash evaporated. However, with an unused basket, the permalloy was melted at a basket temperature near its melting point. A somewhat slower wetting action occurred, and the basket temperature was then raised slightly to complete the evaporation in about 1 minute. It was not determined whether the effect on the dispersion was one of changing film composition or the result of an evaporation rate change; however, in subsequent work, a maximum of two evaporations were made from a single basket to avoid the effects.

Remarkable effects of an aluminum ground plane and SiO smoothing on H_c and dispersion were also noted in these data. A composite structure was formed where part of the permalloy film was on SiO over glass and the rest was on SiO over aluminum on glass. H_c values of 1.4 and 1.8 Oersted were obtained, respectively, for permalloy on substrates of SiO over glass and SiO over aluminum on glass; the corresponding dispersion (α_{50}) was 0.5° and 0.9°. Hence, the dispersion for the SiO over the aluminum ground plane was approximately twice that for substrates of SiO on glass. The value of 1.4 Oersted for the permalloy on substrates of SiO on glass was also lower than the value of 2 Oersted obtained for plain glass substrates. For these conditions, H_k remained constant at about 3.6 Oersted. In this experiment, the thickness of the aluminum and the SiO were about 2 μ each. Eventhough the surface of the ground plane was rougher than that of plain glass, it was apparent that with sufficient SiO over the ground plane, magnetic parameters equal to or better than those for permalloy on plain glass substrates were feasible.

Magnetic properties of permalloy films deposited with a tungsten basket source and the substrate holder-heater-masking fixture of Figure 5.3 as a function of the temperature of the copper plate in intimate contact with the substrate were determined. These results verified those previously discussed. The characteristics observed are plotted in Figures 5.11 and 5.12, respectively, for constant applied fields during deposition of 27 Oe and 40 Oe. Immediately following the evaporations, the applied field was reduced to zero and the specimens were annealed 15 minutes at their respective deposition temperature. They were then cooled to room temperature in about 10 minutes. Thus, there was no applied field during annealing or cooling. Corning type 7059 glass substrates were employed. The films were deposited to a thickness of about 525 angstrom units by evaporating a permalloy composition of 81% nickel and 19% iron at a pressure of about 1×10^{-6} torr. Rectangular in shape, each film measured 1.5 inches by 1.25 inches. The area of each film was scanned with the Kerr apparatus to determine minimum and maximum values of H_c and H_k.

The first series of permalloy films prepared with the substrate holder of Figure 5.3 are represented in Figure 5.11. For the temperature range of 30 to 500° C, H_c values ranged from 2.4 to 6 oe; H_k values ranged from 4.5 to 6.2 oe. Typically H_c varied by as much as a factor of 2 over

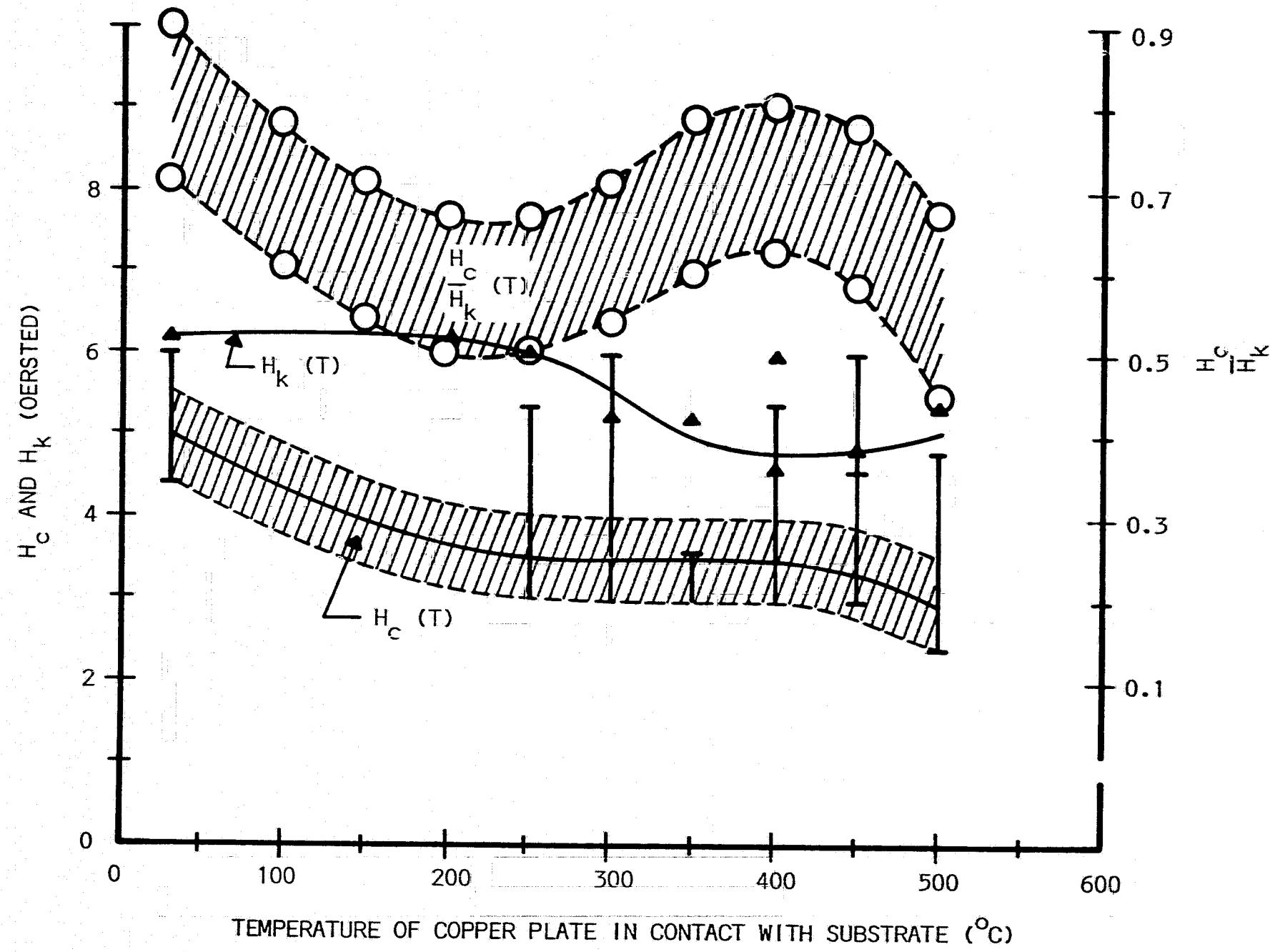


Figure 5.11 Magnetic Properties of Permalloy Films as a Function of Substrate Temperature with Constant Applied Field of 27 oe

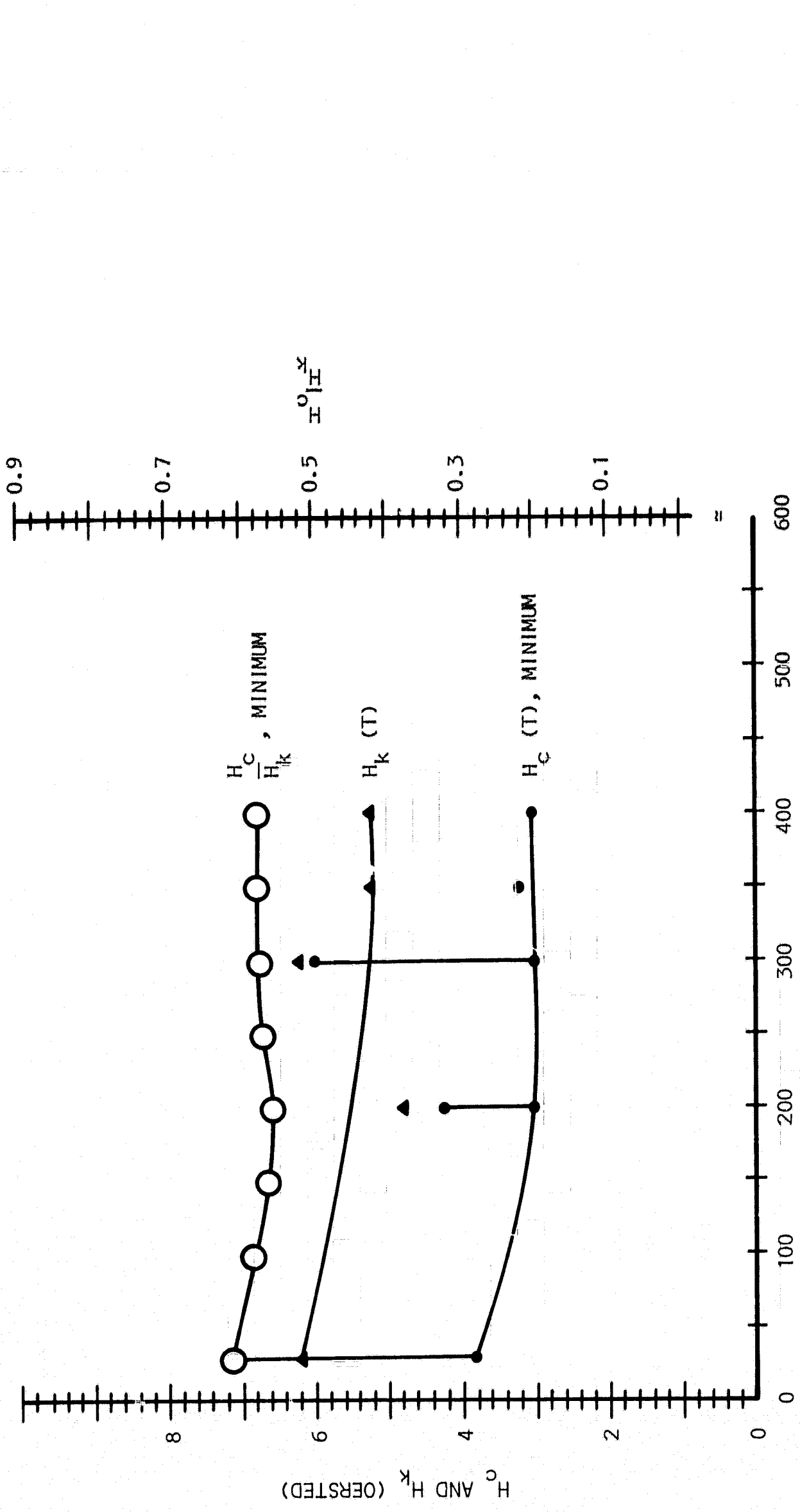


Figure 5.12 Magnetic Properties of Permalloy Films as a Function of Substrate Temperature with Constant Applied Field of 40 oe

the film area. However, for the greater portion of the film area, H_c values were within the hashed area of Figure 5.11. It can be noted that minimum H_c values decreased in a smooth manner with increasing temperature for the temperature range tested; whereas, the maximum H_c values did not behave as orderly. Minimum H_k values occurred near 400° C. The H_c/H_k ratio of Figure 5.11 is plotted for the corresponding hashed H_c region.

For the specimens of Figure 5.11, a definite pattern in the variation of H_c was noted. This pattern persisted in a film deposited without an applied field. It appeared that somehow an extraneous magnetic field was affecting H_c during deposition. The Edwards microcircuit jig used to support the substrate during deposition was examined thoroughly to determine if any parts in the vicinity of the substrate were magnetic. A few parts were found to be slightly magnetic. The apparatus was stripped of all such parts. After this, measurements of magnetic field strength in the substrate position with a Gauss meter indicated no significant extraneous fields and that the applied field was uniform over the substrate area. Subsequently, another series of permalloy films were prepared. These are represented in Figure 5.12 and were fabricated similarly to those of Figure 5.11, except, the applied field was 40 oe. Specimens deposited at 350 to 400° C had only a small variation in H_c. Those films deposited at lower temperatures had variations similar to the earlier films. An H_c/H_k ratio of about 0.6 was obtained at substrate temperatures in the range of 350 to 400° C, and the corresponding sum of the dispersion and skew was less than ±3 degrees.

The permalloy studies permitted certain definite conclusions for testing the initially proposed processes. These were that satisfactory permalloy films could be fabricated by evaporating from a tungsten basket on SiO coated substrates heated to 450° C with an applied magnetic field of 40 Oersted, and that during a 15 minute annealing period at this temperature and a subsequent cooling period of 10 minutes an applied field was not necessary. The inference from the latter was also that a field need not be applied during subsequent film fabrication if the substrate holder temperature was maintained below 450° C.

For memory fabrication, a permalloy film thickness of 750 angstroms was selected. A series of evaporations was made to calibrate the tungsten basket for the substrate distance of 6 inches. Since the permalloy in stock was in the form of 0.020 inch diameter wire the calibration was made

for film thickness per unit length of wire evaporated. The result was 230 Å/in. for the evaporation of 1 to 4 inches of wire. From this calibration, the thickness of the previously discussed permalloy films was estimated at 525 angstroms.

2.4 Photoengraving of Films. Photo resist processing apparatus that was available for photoengraving are discussed in Section V-A-3. The equipment was set up for this program; suitable photo resists, techniques of processing the resists, and etching solutions were determined for photoengraving films of aluminum, permalloy, and chromium-gold.

The Eastman Kodak Company, in Kodak Publication No. P-7, recommends KMER for use on nickel-base magnetic alloys, stainless steel, and steel. Thus, initial efforts were devoted to photoengraving of all the metal films using KMER as the resist.

KMER is a negative working resist. The process empirically arrived at for the processing apparatus available for applying, curing, exposing, developing, and removing KMER is discussed in detail in Appendix G. It was tested and found satisfactory for aluminum and chromium-gold films; however, difficulty was encountered in effectively using KMER for photoengraving permalloy. The J-100 stripping solution, used to remove the resist after etching, dissolved the permalloy films. Of the more effective solvents and commercial solutions available for removing the resist, it was feared that these too, if effective, would probably attack the permalloy. Thus, the most promising approach appeared to be to select a different resist for permalloy.

Resist type AZ-111, a product of Shipley Company, Inc., was purchased for testing. It is a positive working resist so that exposed resist is dissolved in the developer. Also the unexposed resist is readily removed with acetone. Thus, either of these two methods can be used to remove the resist after etching; that is, the resist image, which is unexposed resist, can be removed with acetone or it can be exposed after etching and removed with developing solution. Processing techniques recommended by the vendor were followed to develop an empirical procedure for using the resist. The developed procedure is discussed in detail in Appendix G. The resist proved to be very satisfactory for masking permalloy films during etching, and both methods of removing the resist were effective and nondestructive.

The primary advantage of KMER is its superior resistance to attack by strong acids and bases. Probably for the same reasons it is very difficult to completely remove remnants of cured and exposed images, see photo

resist processing in Appendix G. Meticulous inspections and stripping procedures had to be followed or the remnant components interferred with obtaining sufficient adherence between film layers in the memory; even then, considerable difficulty was experienced in this respect. In comparison, the AZ-111 resist was easy to remove after etching. From this standpoint, it is more satisfactory for application where successively deposited film layers are photoengraved between deposition cycles. However, efforts to etch chromium-gold films in the 2 to 3 μ thickness range with AZ-111 masking were unsuccessful because the resist would not withstand the etching solution for a sufficient length of time. Thus, to evaluate the memory processes, KMER was selected for image masking to etch aluminum and chromium-gold films and the AZ-111 resist was selected for image masking to etch the permalloy films.

There are several basic and acidic formulations that will etch aluminum. However, with many of these, a smut is left on the aluminum surface. Also, basic solutions such as dilute sodium hydroxide and acidic solutions containing hydrofluoric acid that were first tried attacked glass and quartz substrates and SiO insulation layers. An improved etching solution for aluminum films was developed that did not etch the substrates or SiO. The formulation was by volume 2 parts HNO_3, 1 part "Hi-Speed Circuit Etch", and $\frac{1}{2}$ to 3/4 parts HCl. The "Hi-Speed Circuit Etch" is sold by the Philip A. Hunt Chemical Corp. for etching copper circuit boards. The primary ingredient is FeCL. Addition of the HNO_3 in the formulation eliminated smut formation. Etching speed is adjusted by varying the amount of HCl. With $\frac{1}{2}$ to 3/4 parts HCl, aluminum films with a thickness of about 2.5 μ were etched in 1 to 2 minutes at room temperature. This etching time is sufficiently long to make a visual observation of the engraving process and is short enough that the KMER will not break down before the completion of the engraving. With shorter times, it was easy to over-etch and, hence, difficult to maintain dimensional tolerances.

The "Hi-Speed Circuit Etch" solution was used satisfactorily for etching permalloy films at room temperature. A permalloy thickness of about 750 angstroms was etched within one second.

The solution used for etching gold was 2 parts by volume of concentrated HNO_3 to 1 part "Hi-Speed Circuit Etch". This solution etched gold films in the thickness range of 2 μ in two minutes at room temperature.

A solution of 1 part by volume of concentrated HCl to 1 part water was used to etch chromium films. The substrate was placed in a beaker of this solution and zinc powder was added to catalyze the reaction.

The bilayer films of chromium-gold were etched selectively since neither of the respective etching solutions for chromium and gold etched the other. When etching gold over chromium films, the gold was etched first, leaving the underlying chromium intact. The substrate was then rinsed with water to remove the gold etching solution before etching the chromium. Quite frequently a clean etch could not be obtained on the bottom layer of chromium with the HCl solution. The very thin layer of material that remained appeared to be chromium oxide. A dip in fresh chromic acid heated to 125 to 150° C was effective in removing the chromium oxide. When required, this was done during cleaning of the substrate after stripping of the photo resist (KMER). This trouble was not encountered with the top layer of chromium in trilayer films of Cr-Au-Cr.

2.5 Artwork, Transmission Metal Masks and Glass Photomasks. Master artwork for the production of the various masks was prepared in the laboratory at 20 times actual mask size on Ulano Rubylith (a product of Graphic Arts Supplies, Inc.). Precision photoreduction of the master copies and mask fabrication services were obtained from Electromask Inc., Van Nuys, California. Both metal transmission masks and high resolution glass photomasks were purchased for memory fabrication. A few replacement metal transmission masks were fabricated in the laboratory from original glass photomasks. There were three sets of masks - one set each for the model memory, the simple test memory, and metal mask resolution studies.

The initial metal masks were fabricated of 0.003 inch thick type 304 stainless steel. Because of magnetic effects the stainless steel was unsatisfactory for masking during deposition of the permalloy film and copper masks were fabricated for this deposition. The initial glass photomasks for the memory fabrication were prepared on Kodak High Resolution Plates for negative working photo resist (KMER). A negative of the original glass mask for the permalloy was fabricated in the laboratory for the positive working photo resist (AZ-111).

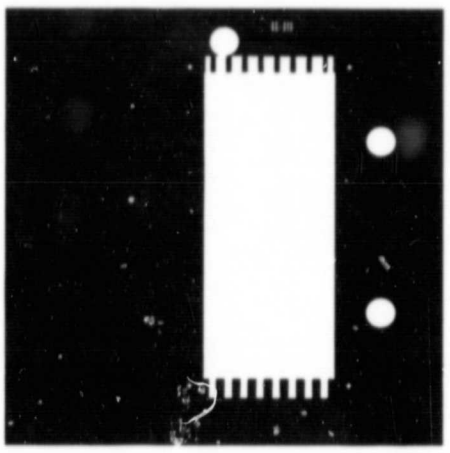
The two masks used for fabricating the bit lines of the model memory are shown in Figure 5.13. The transmission metal mask shown in Figure 5.13a for the bit sense film is typical of the type of metal masks designed for

all of the films to restrict deposition to the general area desired. The one exception is the metal mask for the buss lines which defines the line pattern during film deposition. Figure 5.13b shows the glass photomask for photoengraving the precision sense line pattern. The masks for the permalloy film were similar to those for the bit sense film. The major differences were that the aperture of the metal mask for the permalloy was slightly smaller and the glass mask had only one line per pair of sense lines. Photographs of the bottom and top sides of a model memory structure is shown in Figures 5.13c and 5.13d. Note the holes etched in the ground plane in Figure 5.13c. These are located directly below the position for the selection diodes. The holes are to prevent the possibility of short circuiting the buss and word lines to the ground plane during bonding of diode leads. The sequential use and number of masks for memory fabrication is given in Table 5A.

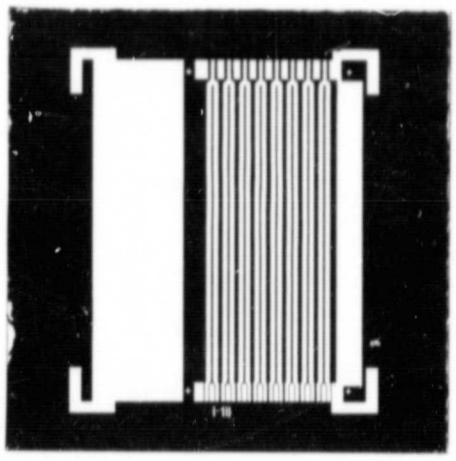
Patterns of the simple test memory were designed to determine operational characteristics of a variety of film and strip line configurations in an actual multilayer memory structure. The masks were fabricated for the deposition of films in an identical sequence to the model memory. The patterns consisted of a series of 3 sizes of word lines and bit lines as illustrated in the photographs of a completed specimen in Figure 5.14.

Mutual registration of the substrate and contact metal masks was accomplished with three precision pins in the substrate holder, see Figure 5.3. Registration marks (4 crosses) were provided on the high resolution glass photomasks to facilitate pattern registration during photoengraving of the films.

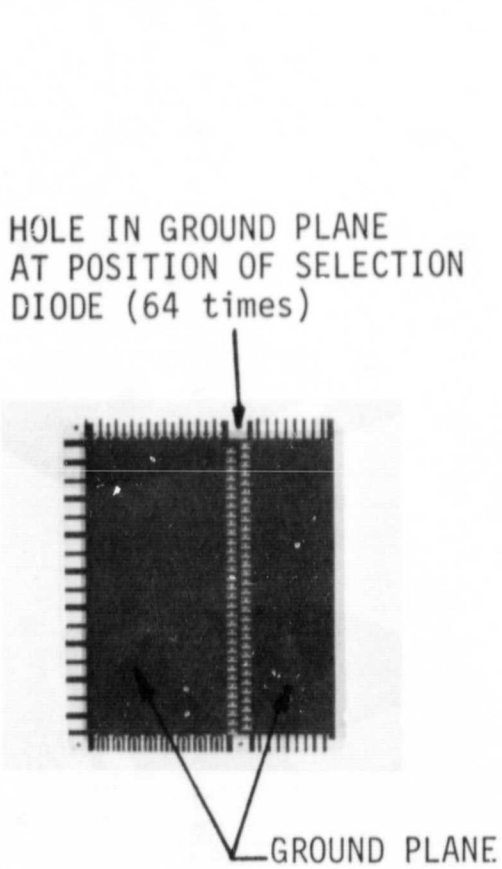
2.6 Resolution Study of Transmission Metal Masks. Two contact transmission metal masks were fabricated for resolution studies. The primary objective in this study was to determine the feasibility of defining all of the line patterns in the model memory with transmission metal masks. This would eliminate the required photoengraving steps, and permit an all-insitu process. Photographs of these masks are shown in Figure 5.15. One of the masks, Figure 5.15a, was designed for constant line lengths of one inch. Line widths of 5, 10, and 15 mil and spacings of 5, 10, 15, and 20 mil were grouped for constant width and constant spacing with the various width and spacing combinations delineated in the figure. The second mask shown in Figure 5.15b was designed to determine the effect of length on



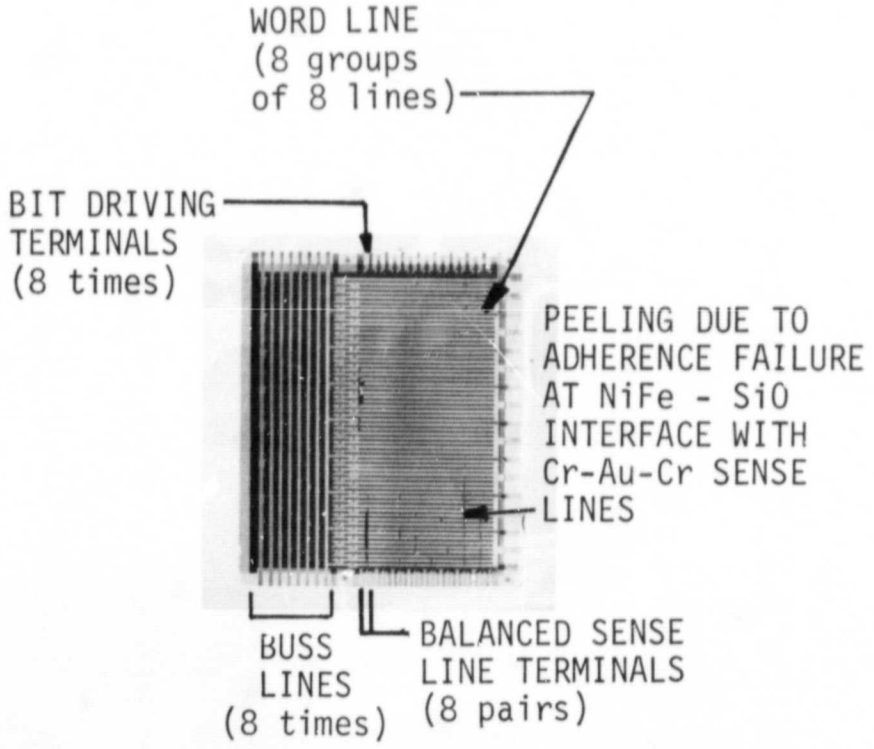
a. Transmission Metal Mask for Deposition of Bit Sense Film



b. High Resolution Glass Photomask for Bit Sense Lines

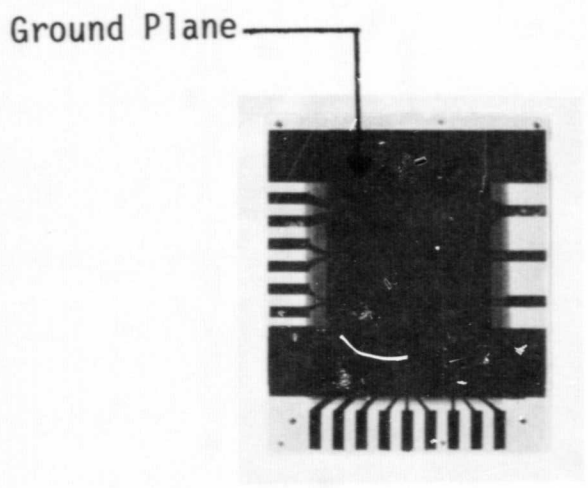


c. Bottom View of Memory Structure Through Substrate

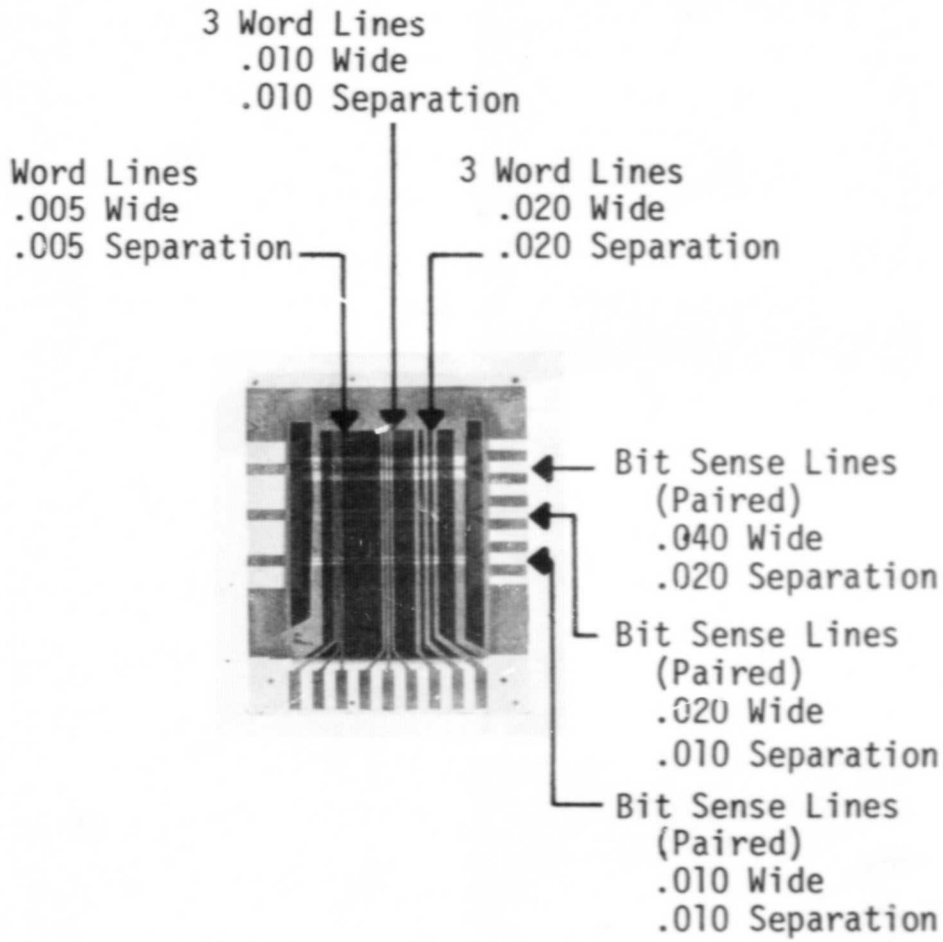


d. Top View of Memory Structure

Figure 5.13 Model Memory Specimen and Typical Masks



a. Bottom View Thru Substrate

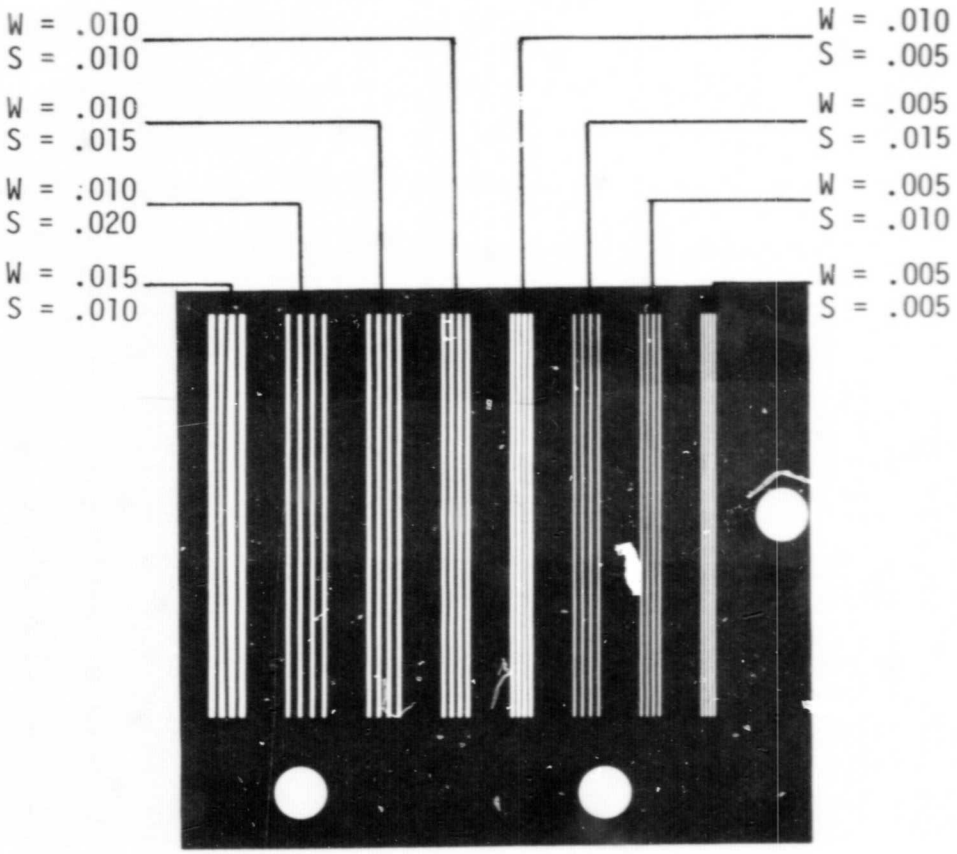


b. Top View

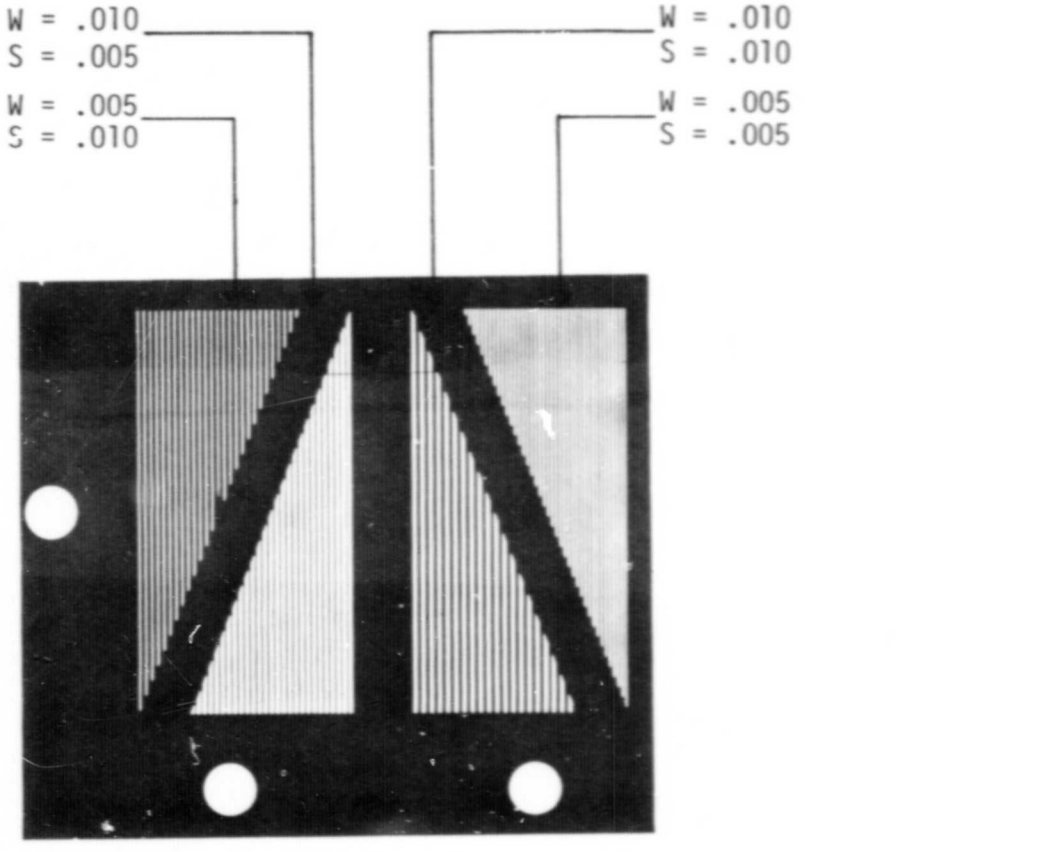
Figure 5.14 Simple Test Memory Specimen

W denotes width of window mask in inches

S denotes width of metal spatial member in inches



a. Constant Length Lines
(L = 1-inch)



b. Variable Length Lines
(1/32 to 1 inch)

(Magnification: 1-3/4X)

Figure 5.15 Transmission Metal Masks Used for Resolution Studies

resolution. For this mask, the line length was varied from approximately 2 squares for the line widths and spacings indicated to a maximum length of one inch.

To determine the resolution of the masks for relatively thick and thin films, two depositions of gold over chromium films were made for each mask. In each case, the substrates were heated to about 350° C and the first bilayer film was deposited to a thickness in the range of 1000 to 2000 angstroms and the second bilayer film was approximately one micron thick. The film patterns were examined visually with a stereomicroscope, and d.c. resistance measurements between adjacent lines were made with an ohmmeter.

From the resistance measurements, it was determined that the line widths had little effect on the occurrence of shorts between adjacent lines. It was found that for lines of appreciable length the borderline between shorted and open conditions occurred at a line-to-line separation of about 10 mil; this was essentially true for both film thicknesses, although the occurrence of shorts between adjacent lines was slightly less for the thinner films. For lengths of 3/8 of an inch or shorter there was a slight improvement in line separation, but no significant dependence of separation on length was observed for longer lengths. However, no shorts were obtained between any of the lines with spacings equal to or greater than 15 mil.

The microscopic examination revealed considerable shadowing at the film edges as a result of paralax between the evaporation source and masks. The sets of longer lines with 5 mil spacing were completely run together for the one micron thick films. For the 5 and 10 mil wide lines, the width at the center of the one inch long lines was about double the width at the ends. Some of the narrower spatial members became warped. Obviously, warped members did not lay flatly against the substrates so that this contributed to the paralax. Undoubtedly, the broad evaporation source arrangement, see Cr-Au source of Section V-B-2.2, contributed to the paralax. To eliminate sufficiently the paralax due to the broad source condition, however, a point source would have to be located at such a great distance from the 1.5 inches x 1.5 inches substrates that the deposition rate would be impractical for evaporating the 2 μ thick gold films required for the memory. Also the advantages previously discussed for the broad source design would be lost with a point source.

These observations demonstrated rather convincingly that to obtain the desired line density and resolution of the word and bit lines of the

512 bit model memory with transmission metal mask would be highly improbable. The desire and need to fabricate memories of even greater densities has been expressed; hence, there appeared to be little to gain by pursuing the improvement of metal masking techniques.

2.7 Initial Multiple Layer Film Studies. During the period of preparing artwork and masks for the memories, some elementary masks were fabricated for fabricating multilayer structures simulating that of the memories. A structure was fabricated that consisted of a glass substrate and the following films in sequence of deposition: 1μ SiO smoothing layer, 2.5μ Al ground plane, 2μ SiO insulation, 2μ Al bit sense lines, 2μ SiO insulation, and 1.5μ Al word lines. No permalloy film was included because the main purpose of the experiment was to evaluate ability to satisfactorily evaporate the thick insulating and conducting layers. The line patterns were photoengraved and consisted of one each of 40 mil, 20 mil, and 10 mil wide bit lines and 3 each of 20 mil, 10 mil, and 5 mil wide word lines.

Low dissipation factors of about 0.02 were obtained for measurements of capacitance between the metal films. This indicated satisfactory insulation. The stability of the films was very good. There were no peeling tendencies, even during ultrasonic cleaning. To achieve satisfactory film adherence, a minimum substrate temperature of 250° C was required for each of the films.

The excellent stability of the films indicated low intrinsic stress in the SiO films and low stress between the substrate and various films. This experiment was very significant in interpreting the film instability experienced subsequently with fused silica substrates during memory fabrication efforts.

2.8 Determination of Bonding Methods. Both ultrasonic and thermal compression bonding of the gold foil leads of the selection diodes to gold over chromium films were tried. Reliable bonding was obtained much more readily for these gold to gold bonds by thermal compression techniques. Figure 5.6 shows one of the diodes bonded in a typical word line pattern at one of the 64 locations for the diodes. (Note the staggered positions for the diodes on adjacent lines. This was done to make room for the full width of the diodes).

The fabrication did not progress to the point of connecting the memory to the circuits board; however, it was planned that flying gold

leads would be used for this purpose. All of the ground plane, drive, and sense terminals of process B were gold or chromium over gold, and soldering of the flying gold leads to the film terminals and circuits board was planned. On the other hand, the bit line and ground plane terminals for specimens of process A were aluminum. Ultrasonic bonding of the gold leads to the aluminum films was considered the most likely of methods that would be used.

3. Adaptation of the Proposed Processes

The two processes designed for memory fabrication were discussed in Section V-B-1. The studies discussed in Section V-B-2 led to several specific conclusions implemental to the general plan of attack. Efforts were then devoted directly to fabricating memory specimens to effect or adapt these initially proposed processes. By concentrating the fabrication efforts mostly on a complete process, attention was directed to vital problems as they occurred in the sequential build-up of the multiple film structures. These efforts were conducted primarily on the simple test memory structure. Fabrication details, difficulties encountered, and progress made toward effecting the processes are discussed in this section.

3.1 Reticulation of SiO Films on Fused Silica Substrates and the Selection of Glass Substrates to Eliminate the Problem. Memory fabrication was begun on fused silica substrates. Several simple test memory specimens were fabricated by process A to the point of photoengraving the permalloy storage film. At this point, examination with a stereomicroscope revealed that the second SiO film was reticulating, see Table 5A. Initially, the crazing of the SiO layer occurred only in areas where it was over the first SiO smoothing layer on the substrate. Figure 5.16 is a photograph showing an advanced stage of reticulation in areas of SiO over SiO. The gross reticulation shown in Figure 5.16 occurred with time. At first, only a few cracks were in the SiO; however, the crazing increased with time, and it could be promoted by probing along the edge of the ground plane with a steel scribe or by ultrasonic vibrations. During the probing, cracks would originate in the second SiO layer at the edge of the aluminum ground plane and progress outward from the ground plane to the edge of the second SiO film. This indicated that the points of highest stress were along the edge of the ground plane. It was difficult to cause the SiO over the aluminum to craze by probing; however, ultrasonic cleaning in water produced crazing

throughout the second layer of SiO. For these specimens, the SiO was deposited at a rate of about 4000 angstroms per minute, and the temperature of the copper plate substrate holder (hereafter referred to as the substrate temperature) was 350° C and 400° C, respectively, for the aluminum and SiO depositions. The films were then annealed to 450° C during subsequent substrate heating for the permalloy deposition.

Experiments were conducted by process A to determine if a slower SiO deposition rate and higher substrate temperatures for the aluminum and SiO would eliminate the reticulation. No improvements were obtained for variations in the substrate temperatures or for the slower SiO deposition rate.

Next, specimens were fabricated by process B with deposition parameters similar to those for process A, and the reticulation problem remained. Thus, substitution of Cr-Au-Cr for the aluminum did not eliminate the problem.

The occurrence of reticulation was unexpected since it did not occur in the earlier preliminary studies. In those studies, glass substrates were employed. Specimens were fabricated similar to the previous specimens by both of the hypothetical processes substituting Corning type 7059 glass substrates for the fused silica. No reticulation occurred in any of the SiO films even after subjection to ultrasonic cleaning for periods of 15 minutes.

It was concluded that fused silica substrates were not compatible with the memory structure of either process and that glass substrates were satisfactory. In addition, it appeared that ultrasonic vibration was a method that can be possibly developed for testing the adherence qualities of films. Corning 7059 glass substrates were used for all of the subsequent memory fabrication.

3.2 The Elimination of Three Sources of High Skew and Dispersion in Permalloy Films. During memory fabrication, the permalloy films were examined with the Kerr Effect apparatus before and after photoengraving. This was done to determine if the magnetic properties were satisfactory before continuing with the photoengraving and also to detect any changes in the magnetic properties as a result of engraving. These measurements aided in detecting three sources of excessive skew and dispersion in the permalloy films.

The first transmission metal masks used during the evaporation of

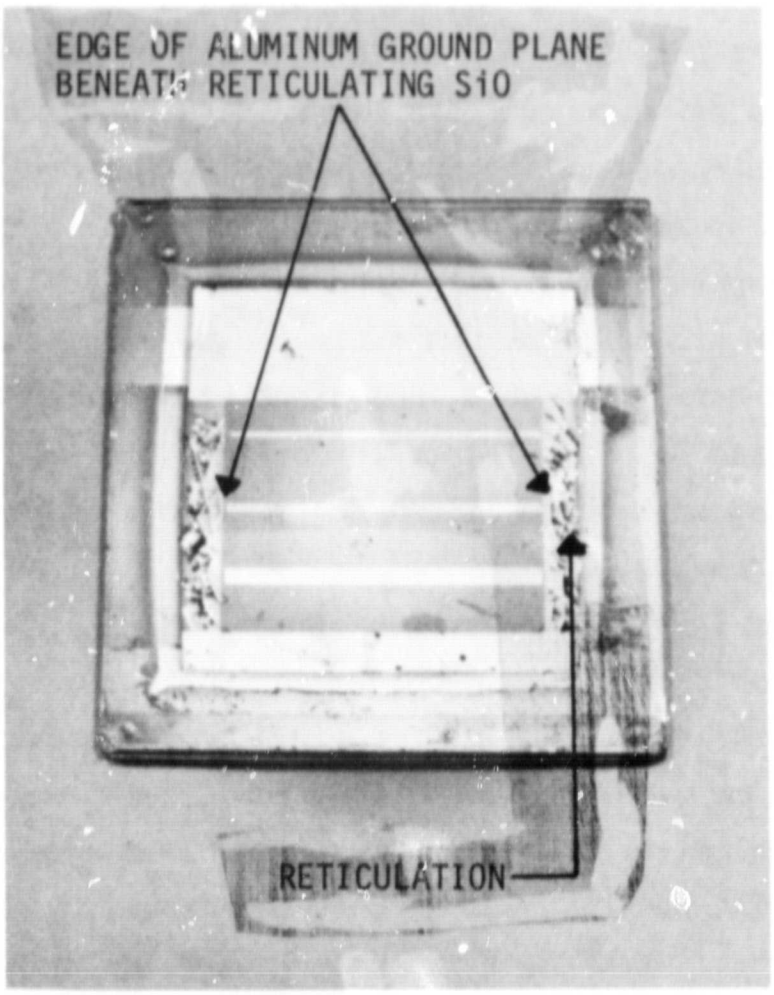


Figure 5.16 Photograph Showing Reticulation of Second Layer of SiO on Fused Silica Substrate

the permalloy films for fabricating the simple test memory were fabricated of type 302 stainless steel. This type of stainless steel is supposedly nonmagnetic when fully annealed; however, films fabricated during the use of these masks were highly skewed. The skew appeared to increase with repeated use of the masks. Measurement of the residual magnetic field on one of the masks indicated a field strength of 5 Oersted. The effects were eliminated by using copper masks in subsequent permalloy film depositions.

The thickness of the insulating SiO film over the ground plane also influenced dispersion and H_c values obtained for permalloy films. Usually excessive dispersion ($\alpha_{90} > 1^\circ$) was obtained where the thickness of the SiO film over the ground plane was estimated to be substantially less than 2 μ. On the other hand, minimum H_c and dispersion values were obtained for SiO films exceeding 3 μ in thickness. For the thicker SiO films, H_c and dispersion values of 1 oe to 1.5 oe and 0.5° to 1° were typically obtained before photoengraving.

During initial fabrication efforts the AZ-111 resist used for masking permalloy films during etching was applied in two successive spin coats at 2500 r.p.m. Occasionally, the permalloy films were highly dispersive after the films were etched and the photo resist was removed. Further examination revealed large holes in the films that were not present before etching. This condition was corrected by applying dip coats of the resist to obtain better masking of the permalloy film.

3.3 Shorting Between Metal Films and Methods Used to Eliminate Shorts. To determine insulation quality of SiO films in the memory structures, measurements of capacitance, dissipation factor, and d.c. resistance were made between the various metal films after each film was etched. These measurements were made with an impedance bridge, General Radio Type 1650-A. From the capacitance values, the average SiO thickness was calculated by assuming a relative dielectric constant of 6 and using the known film area. For an SiO thickness in the range of 1 to 4.4 μ, only an occasional short occurred between the permalloy lines and the ground plane for either of the initially proposed processes. On the other hand, pronounced shorting occurred between the bit sense line and the ground plane. The shorting of the sense lines to ground occurred for both of the processes; however, the shorts were more numerous for metal films of Cr-Au-Cr than for aluminum. A similar situation existed between the bit sense and word lines for the SiO thickness range of 1 to 4.4 μ.

To locate position of shorts, test specimens were placed in a petri dish of methanol and observed with a stereomicroscope while a d.c. potential was applied across affected lines. As the voltage was increased, the shorted points became hot and caused local boiling of the methanol. It was surprising that the hot spots did not appear first at suspected points such as crossovers, surface defects, and film edges. At applied voltages above 20 volts, the shorting began to occur more regularly at film edges and points that might be suspected.

Shorting between aluminum films could be readily eliminated by discharging a one microfarad capacitor, charged to 5 to 10 volts, between affected films. It was more difficult to eliminate shorting between Cr-Au-Cr films. For the latter films, the capacitor had to be charged to about 40 volts.

Several specimens were fabricated by depositing the SiO at 500 Å/min instead of the 4000 Å/min used for the previous films. In addition, the deposition cycle was interrupted to complete the depositions in two successive evaporations. During the interruption, air was admitted to the vacuum chamber and the specimens were rotated 90 degrees in the plane of the evaporation source before depositing the second half of the film. No significant improvement in the occurrence of shorts was noted in these experiments; however, numerous authors have reported improvements by using extremely low deposition rates or by interrupting the deposition cycle and exposing the film to air.

Increasing the thickness of the SiO appeared to be most significant in reducing shorts and dissipation factors. The model memory specimen of Figure 5.13d was fabricated by process B. The insulating SiO films between the buss lines and word lines were evaporated at a rate of about 6000 Å/min. to a thickness of about 8 μ in an uninterrupted deposition. The buss lines overlap the word lines a total of 274 times where insulation is required. None of these crossovers were shorted. Also, there were no shorts between the buss lines and ground plane; however, in the latter case, the thickness of the SiO was from 16 to 24 μ as a result of the multiple SiO layers in the memory structure. The capacitance and d.f. values of each pair of sense lines to the ground plane was 210 ± 10 pf and 0.01, respectively. The total absence of shorts in these cases indicated that 8 μ thick SiO films would essentially eliminate shorting problems. No SiO insulating films were deposited in the thickness range from 4.4 to 8 μ; therefore, the

minimum thickness required to eliminate excessive shorting was not established. From the few shorts obtained for thicknesses of 3 to 4 μ, however, it is expected that satisfactory SiO insulation can be obtained at film thicknesses of 5 to 6 μ for either of the processes or either memory structure.

Possibly improved SiO insulation can be obtained by operating the broad SiO source at a reduced source to substrate distance. This will increase the average angle of incidence of the SiO atoms arriving at the substrate, and the source temperature could be lowered to reduce any disassociation of the SiO at the source while maintaining a high rate of deposition. Both effects should be beneficial and examined in the future.

3.4 Diffusion of Permalloy and Aluminum Bit Sense Lines; A Method of Eliminating the Aluminum - Permalloy Diffusion; and a Short Study of Diffusion of Permalloy with SiO, Cr-Au, and Cu. When the first simple test memory was processed to the point of completing the bit sense lines by process A, it was noticed that in every case the resistance of the aluminum line over the permalloy was higher by about 10 percent than their respective mating balance lines which did not have permalloy beneath them. This difference in resistance was an indication that the aluminum and permalloy had alloyed; nevertheless, the specimen was completed with aluminum word lines to see if the memory would function. No semblance of a switching signal could be detected during a performance test.

No previous tests were made to determine the diffusion properties of aluminum and permalloy films; however, a diffusion possibility had been anticipated. A permalloy film previously prepared on glass during the preliminary studies was selected to determine the effects of deposition aluminum films on permalloy films at the 350° C substrate temperature. The magnetic properties of the permalloy were measured with the Kerr Effect apparatus at the substrate-permalloy interface from the substrate side before and after depositing an aluminum film over the permalloy. These measurements indicated that the magnetic properties of the permalloy were completely destroyed. This experiment demonstrated the incompatibility of aluminum films in direct contact with the permalloy.

It was decided then to determine if a thin SiO film over the permalloy would prevent the occurrence of diffusion between the permalloy and a subsequently deposited aluminum film. In the same manner of testing used before, it was first determined that a 2000angstrom thick SiO film did not

adversely affect the permalloy and secondly that a subsequently deposited aluminum film over the SiO did not adversely affect the permalloy.

A simple test memory was fabricated by process A modified to include an additional thin layer of SiO (500 to 1000 Å) between the permalloy and storage film. It was operationally tested; however, the switching signal levels were below the noise level of the test fixture. Signals ≧ 1 mv are observable in this apparatus. It is believed that the low signal level was a result of overetching of the permalloy film. Large and numerous holes were observed in the permalloy after etching (see the discussion on overetching with spin coats of resist AZ-111 in Section V-B-3.2). Another possible reason for the poor performance is local diffusion of the aluminum bit lines with the permalloy through pinholes in the thin SiO film between them.

It can be safely assumed that SiO films can be deposited sufficiently free of pinholes to prevent any adverse diffusion effects between the permalloy and aluminum films of process A. However, from a standpoint of system performance the extra separation between bit line and ground is not desirable. For this reason, work on process A was terminated and attention was directed fully to effecting process B.

Before going directly to memory fabrication with process B, it was determined that the Cr-Au sense lines of process B would not adversely affect the magnetic properties of permalloy; this was done in the same manner previously used to detect the effects of aluminum on permalloy. In additional tests, copper in the thickness range of one micron was observed to destroy the magnetic properties of permalloy films (700 Å thick) at 350° C.

3.5 Adhesion Failure at the Permalloy-SiO Interface with Cr-Au-Cr Bit Sense Lines. Several simple test memory structures were satisfactorily processed by process B until the Cr-Au-Cr bit sense lines were photoengraved and cleaned. At this point, it was observed that the sense lines were peeling. It was discovered that the peeling occurred only for that portion of the Cr-Au-Cr lines over the permalloy and that the adherence failure was at the permalloy-SiO interface. An example is shown in Figure 5.17.

A sample of peeled film was taped to a glass slide with the permalloy side up for examination with the Kerr apparatus. These measurements indicated that the magnetic properties of the permalloy film were still satisfactory. This bit of information was encouraging since it proved that the Cr-Au film deposition did not adversely affect the magnetic properties of the permalloy.

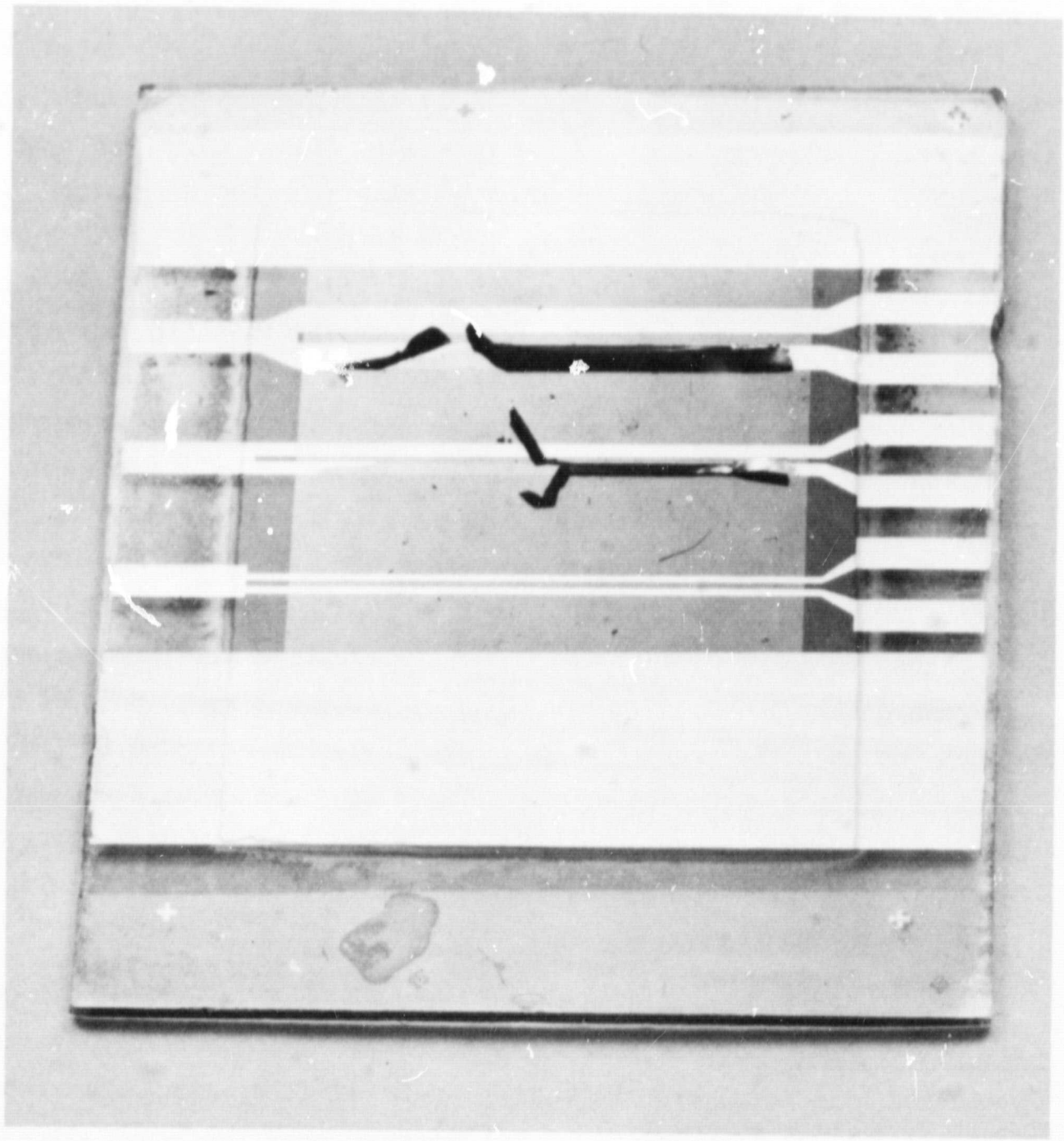


Figure 5.17 Photograph Showing Peeling of Bit Sense Line Resulting from Adhesion Failure at Permalloy-SiO Interface

Before depositing these Cr-Au-Cr sense films, the substrate was outgassed by baking at 350° C for about 15 minutes. To deposit the Cr-Au-Cr the substrate was cooled to 200° C. The evaporated sense line film was then post-annealed in the vacuum chamber at 350° C for about 15 minutes. It is possible that annealing of the Cr-Au at temperatures in the range of 400 to 450° C will eliminate stresses that caused the peeling, but there is a possible danger that the chromium will alloy or diffuse with the permalloy at the higher temperature, so another method to eliminate the peeling was tried.

It was decided first to deposit a thin film of SiO over the permalloy before depositing the Cr-Au-Cr sense lines. Two simple test structures were fabricated by process B with this modification. On one of these the SiO was deposited to a thickness of about 1500 Å and on the other specimen the thickness was 3000 to 4000 Å. The bit sense lines did not peel on either specimen. Both of these specimens were completed for an operational test, and during the subsequent fabrication no peeling occurred. In the operational tests, peak switching signals of about ± 2 mv were obtained. The film dispersion was so large however that a stored bit was not stable under any disturb pulses. The pulse program was modified to directly measure the write mode switching astroid and the single pulse disturb astroid. From this data it was observed that no combination of word and bit write currents existed such that the bit current alone would not disturb the film. Measurements with and without the keeper present indicated a keeper efficiency of only 40%. The keeper used in this fixture was not fabricated by the finalized process developed and had a high percentage of bubbles and voids. This low keeper efficiency would increase the bit current required to write by at least a factor of two and probably accounts for a significant part of the poor observed test characteristics. However we also observed that the amount of flux linking the sense line was a factor of 2.5 smaller than predicted. With a film 800 Å thick and keeper efficiency of 40% the flux linkage should be approximately 10×10^{-12} weber. By integrating the observed switching signal we measured 4×10^{-12} weber. There is the possibility that the Ni-Fe film was adversely affected during photoengraving. Time did not permit detailed investigation of this anomoly.

Since there was only enough time left on the contract to fabricate one or two more memory structures, it was decided to use this time to fabricate a 512 bit model memory by process B, modified to include an SiO

layer between the Cr-Au-Cr bit sense film and the permalloy. This film was deposited to about 3000 angstroms in thickness for the memory fabricated. The SiO film did not prevent the peeling in the more complex line structure, but a significant reduction in peeling tendencies was obtained compared to the earlier films where the extra SiO layer was not used. The peeling was sufficiently restricted that the remaining films of the memory structure could be fabricated. This specimen is shown in Figures 5.13c and 5.13d where the peeling is noted. The reduced peeling compared to the specimen in Figure 5.17 is apparent. The latter case was typical of the extent of peeling that occurred immediately after etching the sense lines when SiO was not used between the permalloy and Cr-Au sense film.

It appears from these studies that an SiO film in the thickness range of 0.5 to 1 μ will eliminate the permalloy adherence failure at the SiO interface. However, for the same reasons expressed previously for process A, this is not the most desirable approach; it is recommended that other methods of eliminating the problem be investigated. The first measure recommended is to deposit the initial chromium layer at the highest possible temperature that can be used without adversely affecting the magnetic properties of the permalloy. For the previous specimens, this temperature was 200°C, but it was determined in the diffusion experiments that this can be increased to 350°C. The maximum temperature that can be used can be just as simply determined. The gold deposition temperature can be increased in like manner. Annealing effects at higher temperatures would result in minimum intrinsic stress for the Cr-Au film. This in turn will possibly result in less strain on the permalloy film.

A second measure that would shorten the process and possibly eliminate peeling is to deposit the permalloy through a transmission metal mask that roughly defines the permalloy lines. Following the permalloy deposition, the sense line film layer is then deposited and the precision line pattern of the permalloy and sense lines is etched in a common engraving step.

In the event that these measures do not eliminate the problem, another metal such as molybdenum, tantalum, or platinum might be substituted for the chromium.

3.6 Minor Difficulties Common to Processes A and B. The difficulties discussed in this section were of a minor nature, in that, solutions were not required to realize the primary objective of fabricating a working

memory by either of the processes. Solutions to the problems would, however, result in overall improvements in the fabrication processes. There were three difficulties or problem areas of this nature. These were: skew and variation in H_c values over the permalloy film area, the method of measuring substrate temperature during film deposition, and stripping of KMER. To some extent, the latter two problems have been discussed.

In general, H_c values and dispersion varied over the permalloy film area. This variation was within the specified limits; however, the variations did follow a characteristic pattern. While the shape of the permalloy possibly contributed to the observations, it appeared that the film deposition apparatus was a significant influence on the pattern shape in this work. As discussed in Section V-B-3.2, stainless steel transmission masks had to be eliminated for masking during the deposition of the permalloy because of its contribution to high H_c and dispersion. In the latter instance, the variations in H_c and dispersion were greater but followed the same general pattern. Inspection of the deposition apparatus revealed that all of the type 303 and 304 stainless steel parts such as the screws, mask support, and spacer ring of Figure 5.3 and the tripod and top support plate of Figure 5.2 possessed a small amount of residual magnetism. The square holes in the top support plate of the tripod, where the substrate was located during film deposition, and the stainless steel frame section of the substrate support fixture are of the same general shape (rectangular) as the stainless steel mask, but further removed from the film. Hence, due to the similarity in pattern shapes observed with and without the metal mask it is believed that when the Helmholtz field was applied during film deposition the field induced in the stainless steel parts contributed to the pattern of variation in H_c and dispersion. It is suggested that in the future nonmagnetic and nonferrous materials such as aluminum-titanium alloys, aluminum, copper, tantalum, and ceramics be used for constructing vacuum tooling to eliminate any possibility of adverse tooling influence on the magnetic properties of the films.

The difficulty of removing KMER remnants after engraving is discussed in the photo resist processes, Appendix G. Poor removal, in a few cases, caused peeling of subsequently deposited films. It is suggested that another type of resist be tried that is easier to remove. The AZ-111 resist is easy to remove, but for the process developed, it would not withstand the etching solution for Cr-Au films. To etch the thick Cr-Au films

used in the memory with the AZ-111 resist a different etching solution or improved application and curing procedures will be required.

The method of heating and measuring the temperature of substrates was discussed. The method permitted consistent reproduction for a given set of conditions but was not an accurate indication of the actual temperature of the substrate, in particular for the Cr-Au and SiO evaporations. In these evaporations, the high intensity of heat radiation from the sources caused the substrate temperature to rise above that of the copper heater, and the temperature of the latter was measured. The disadvantage was the extra time required to emperically establish a set of conditions for depositing films that otherwise could have been established more readily with an accurate measurement of substrate temperature.

3.7 Typical Magnetic and Electrical Parameters of Films in the Memory Structures. The magnetic properties of the permalloy films in Figures 5.11 and 5.12 were for large area continuous films on glass substrates. For memory fabrication, the permalloy (81-19) was evaporated at a source to substrate distance of 6 inches from a tungsten basket on substrates at 450° C to a thickness of about 750 angstroms with a constant applied field of 40 Oersted. They were annealed at this temperature for 15 minutes and subsequently cooled to room temperature in 10 to 15 minutes with no applied field. The H_c, dispersion (α_{90}), and skew (β) values varied some with the thickness of the SiO film over the ground plane, i.e., lower values of all three parameters were obtained as SiO thickness was increased.

H_k values of the permalloy films in the memory structures were typically in the range of 3.5 to 4.5 oe before and after etching. Where thicker SiO films in the 3 to 8 μ range were used, H_c = 1.2 to 2 oe, $\alpha_{90} = 0.5°$ to 1°, and $\beta = \pm 1.5°$. After etching α_{90} and H_c usually increased showing a dependence on line width with typical average values of $\alpha_{90} = 4°$, 6°, and 12° and H_c = 1.5, 1.6, and 2 oe, respectively, for 40, 20 and 10 mil wide lines. H_c showed somewhat less tendency to increase during etching after introducing the dipping technique of applying the AZ-111 resist. For SiO films of about 1 to 2 μ in thickness over the ground plane and before etching, the magnetic parameter of the permalloy were more scattered ranging from values as low as those for the thicker SiO films to excessively high values but typically H_c = 1.5 to 2.5 oe, $\alpha_{90} = 1°$ to 2°, and $\beta = \pm 2°$.

Capacitance measurements between the metal films were made to have a record for subsequent electronic testing and evaluation. Also, the d.f. values of the capacitance was an indication of the insulating quality of the SiO. For the model memory specimen of Figure 5.13d, the capacitance and d.f. values of each pair of sense lines to the ground plane was 210 ± 10 pf and 0.01, respectively. From the film area and average capacitance value, the average SiO thickness was calculated to be 8.6 μ. After the deposition of the word lines, the word lines, bit lines, and ground plane were shorted due to the peeling of the bit lines and further measurements were not made.

For the simple test memory shown in Figure 5.14 the capacitance of the bit sense lines to the ground plane was 455, 233, and 123 pf, respectively, for the 40, 20, and 10 mil lines, and the corresponding d.f. values were 0.12, 0.01, and 0.012. After depositing the word lines, the respective bit line to ground plane capacitance and d.f. values were 493, 255, and 146 pf and 0.015, 0.022, and 0.025. From these capacitance values, the SiO insulating films were about 4 μ thick. The respective average sheet resistivity of the bit and word lines were calculated as 0.016 ohms per square and 0.02 ohms per square; however, the actual resistance per square was somewhat lower than this since the contact resistance between the metering probes and films was not eliminated from the measured resistance values in making the calculations. The d.f. values obtained for this specimen were typical of memory structures fabricated by both processes with SiO films ranging from 3 to 8 μ in thickness and metal films having sheet resistivities in the range of 0.01 to 0.02 ohms per square.

3.8 Comparison of the Processes After Optimization. With substrate temperatures measured as discussed previously, the permalloy films were deposited at temperatures of 450° C in both processes. Substrate temperatures of about 450° C, 350° C to 400° C, and 200° C were used, respectively, for SiO, Al and Cr-Au film evaporations before the permalloy deposition. For the Cr-Au depositions, 200° C was the initial temperature and this increased to an unknown value in the range of 300° C to 450° C. After the permalloy was evaporated, substrate temperatures of about 350° were used for all film depositions. Copper transmission masks were used satisfactorily in both processes for permalloy film depositions, and type 304 or 302 stainless steel masks were used for the remaining films of the structures. Except for the etching solution, the photoengraving processing was basically

common to both processes. Corning type 7059 glass was selected over fused silica for the substrate in each process. Cleaning processes are given in Appendix H. In general, hot chromic acid cleaning was used after photoengraving the Cr-Au films in process B, but it was not used for direct cleaning of the permalloy film. Hot chromic acid attacks aluminum films, and was not used in any of the cleaning steps for process A.

It was determined that a thin film of SiO (2000 to 3000 Å) between the permalloy and aluminum prevented the diffusion. Similarly, it appeared that an SiO film in the thickness range of 0.5 to 1 μ can be used between the permalloy and Cr-Au-Cr to possibly eliminate the adhesion failure in process B. However, for both processes, it is more desirable, though not necessary, to have the sense lines in direct contact with the permalloy. Possibly, this can be achieved for both processes by evaporating a refractory metal film between the sense lines and permalloy. Also, for process B, optimum annealing conditions for the Cr-Au films may eliminate the peeling. For both processes, SiO insulation of 8 μ essentially eliminated shorting between the various metal films of thickness in the range 1.5 to 3 μ. It appears that somewhat thinner SiO films in the thickness range of 5 to 6 μ will be satisfactory.

Film structure of the simple test memory planes fabricated by process A exhibited excellent mechanical stability. The mechanical stability of the structures of process B with Cr-Au-Cr, SiO, and Ni-Fe films was excellent, except for the adhesion failure of the bit sense lines.

As mentioned above, chromic acid cleaning was used after photoengraving of the chromium-gold films in process B. The acid will slowly attack permalloy. It was assumed that the permalloy was adequately protected by the thick chromium-gold and SiO overlayers. A thorough proof of this assumption was not made, but supporting evidence was obtained when the peeled sense lines were examined with the Kerr apparatus. In these instances, the chromic acid cleaning was used on the Cr-Au-Cr sense lines before peeling and the magnetic properties of the permalloy on the peeled sense lines were good.

The one model memory film structure completed was known to be bad when the sense lines began to peel after they were etched. The subsequent film processing was completed to determine if all of the various masks were correct and in proper registration.

During the course of working with the two processes, a slight preference was developed for process B. This was due primarily to the more rigorous cleaning procedures that could be employed with the Cr-Au films compared to that for the aluminum films of process A. Also the gold terminations for all of the lines were considered an advantage for subsequent connections to the circuits board. In this preference, it is assumed that the peeling of the sense lines can be eliminated by one of the suggested methods. Process A appears to be a satisfactory approach also and has some advantages over process B. It is expected that either process can be developed for memory fabrication. However, considerable additional efforts will be required to make either process effective for pilot production and to prove them compatible with silicon substrates.

In view of the considerable progress made during this report period, it is estimated that the fabrication efforts required to obtain a satisfactory process will be about equal to that devoted to fabrication during this program which was the combined efforts of one research physicist and one assistant research engineer to the total of about 1.5 man-years.

C. CONCLUSIONS AND RECOMMENDATIONS

The objective of this study was to develop an all-evaporation process for fabricating a multilayer film memory plane compatible with integrated circuit technology. It was proposed that fabrication of a 512 bit hybrid memory circuit on a single substrate to include not only a thin film memory matrix but also the selection diodes and buss lines be considered first as an intermediary step to fabricating a memory matrix on a silicon wafer with diffused electronics. Considerable progress was made toward effecting two proposed processes A and B. In process A, films of SiO, Al, SiO, Ni-Fe (81-19), Al, SiO, Cr-Au, Cr, SiO and Cr-Au were successively evaporated. In process B, successively evaporated films of SiO, Cr-Au-Cr, SiO, Ni-Fe (81-19), Cr-Au-Cr, SiO, Cr-Au, Cr, SiO, and Cr-Au were used. The simple test memory consisting of a film memory matrix of 27 bits with a film deposition sequence identical to the first seven films of processes A and B proved to be a useful tool for examining the proposed processes.

Multiple tungsten boats and baskets physically separated to simulate a broad source condition proved to be satisfactory, respectively, for evaporating Cr-Au and Al films of the memory plane. Values of sheet resistivity

of 0.010 to 0.015 ohm per square were obtained.

A broad source with a graphite cloth element to evaporate SiO proved capable of deposition rates to about 100 Å/sec. An SiO film thickness of 8 μ essentially eliminated shorting between the various metal films 1.5 to 3 μ thick. It appeared that somewhat thinner SiO films in the thickness range of 5 to 6 μ will give satisfactory insulation. Investigations to determine optimum source temperature for the graphite cloth source and to adjust the source to substrate geometry for maximum possible average angle of incidence for atoms arriving at the substrate will possibly permit the use of thinner SiO films.

A single tungsten basket was found satisfactory for evaporating permalloy films to a target thickness of 750 angstroms, but the number of evaporations from a single basket was restricted to two to avoid excessive skew and dispersion of the easy axis of the films that occurred with more extensive use of a basket. Of the ranges of substrate temperature (25° C to 500° C) and intensity of an applied magnetic field (zero to 60 oe) examined for the deposition of permalloy, the most satisfactory compromise between low dispersion and high H_c/H_k was obtained for a constant applied field strength of 40 oe at a substrate temperature of 450°C. It was determined that an applied magnetic field was not necessary during post deposition annealing at 450° C for 15 minutes and subsequent cooling. The latter inferred that a field need not be applied during subsequent film fabrication if the substrate temperature was maintained below 450° C. H_k values of the permalloy films in the memory structures for these conditions ranged from 3.5 oe to 4.5 oe or close to the target value of 4 oe or less before and after etching the bit lines. Additional variables affecting H_c, α_{90}, and β, were the thickness of the SiO over the ground plane and line width of the permalloy. It was found that before etching the permalloy that values of H_c = 1.2 to 2 oe, α_{90} = 0.5° to 1°, and $\beta = \pm 1.5°$ were consistently obtained for an SiO film thickness of 3 to 8 μ over the ground plane. After etching the permalloy, H_c and α_{90} usually increased showing a dependence on line width with typical values of H_c = 1.5, 1.6, and 2 oe, and $\alpha_{90} = 4°, 6°$, and 12°, respectively, for 40, 20, and 10 mil wide lines.

For multilayer film memory fabrication, experiments indicated that transmission metal masks were unsatisfactory for resolving film line patterns with separations of less than 15 to 20 ten thousandths of an inch.

Except for the permalloy, stainless steel type 304 and 302 transmission metal masks were found satisfactory for defining the large area deposits and buss lines of the 512 bit model memory. It was found that highly dispersive permalloy films were obtained with repeated use of stainless steel masks to define large area permalloy deposits; on the other hand, copper proved to be satisfactory for masking large area permalloy deposits. Photoengraving techniques using high resolution glass photomasks proved to be satisfactory for fabricating the precision patterns of the ground plane, storage film, sense lines, and word lines.

Shipley's resist, type AZ-111, proved to be satisfactory for masking permalloy during photoengraving. Kodak-Metal-Etch-Resist (KMER) masking was found satisfactory for engraving metal films of Al and Au-Cr, but it is recommended that improved methods of removing the KMER or other resist materials more easily removed after engraving be investigated. Solution formulations by volume of 2 parts HNO_3, 1 part "Hi-Speed Circuit Etch", and 1/2 to 3/4 parts HCl; 2 parts HNO_3 to 1 part "Hi-Speed Circuit Etch"; 1 part HCl to 1 part water with a zinc catalyst; and "Hi-Speed Circuit Etch" were found satisfactory for etching, respectively, films of Al, Au, Cr, and permalloy.

Of the two substrate materials examined (fused silica and Corning type 7059 glass), the glass substrates gave the most consistent mechanical stability of the multilayer film memory structures.

It was determined that the method of heating the substrate with a contact copper plate and measuring the temperature of the plate as an indication of substrate temperature was sufficiently reproducible but that this method of specifying the substrate temperature was not necessarily an accurate measurement of temperature of the substrate perse.

As specified, substrate temperatures during film deposition of 400° C to 500° C, 450° C, and 350° C, respectively, for films preceding the permalloy, the permalloy, and films succeeding the permalloy gave consistently excellent adherence of films in the multilayer structures fabricated by process A. For similar substrate temperatures in process B, there was an adherence failure at the permalloy-SiO interface with adhesion of the remaining films being excellent. In process A, alloying of the aluminum sense lines with the permalloy at 350° C destroyed its magnetic properties. It was determined that a thin film of SiO (2000 to 3000 Å) deposited between the permalloy and aluminum prevented the diffusion and concurrent adverse effects on the

permalloy. Similarly, it appeared that an SiO film in the thickness range of 0.5 to 1 μ can be used between the permalloy and Cr-Au-Cr to eliminate the adhesion failure in process B. However, for both processes it was concluded that direct contact between the sense lines and permalloy is more desirable though probably not necessary. To achieve direct contact, an examination to use evaporated films of metals such as molybdenum, tantalum, platinum, or palladium between the permalloy and sense lines of both processes is recommended as a profitable future course. Also, for process B, a study of optimum annealing conditions for the Cr-Au sense lines to eliminate the Ni-Fe adherence failure is suggested. A third method recommended is that the precision etching of the permalloy lines can be delayed for a common photoengraving step with the sense lines by using a trasmission mask to roughly define the permalloy line pattern.

Simple test memory specimens fabricated by processes A and B modified to include a thin SiO film between the permalloy and sense lines did not meet the expected functional characteristics. It was concluded that damage to the permalloy film occurred during fabrication subsequent to that of the permalloy film. Time did not permit a detailed investigation of the anomolous behavior. It is expected that either process can be developed for memory fabrication; however, the answers obtained pointed to a considerable amount of further engineering development to fabricate reliably multilayer film memories by either process or to prove either process compatible with silicon substrates.

VI. CONCLUSIONS AND RECOMMENDATIONS

The work carried out under this contract indicates that the proposed integrated thin film memory system is indeed feasible. A detailed system analysis has shown that word drive current requirements will be approximately 150 ma and sense signals at the array terminals of 3 mv to 4 mv can be expected. Integrated circuit drivers and sense amplifiers capable of operating to these specifications have been designed, fabricated, and evaluated. To eliminate demagnetizing effects and increase drive line efficiency, a ferrite keeper material has been developed which provides a relative permeability of nearly 10 over a wide frequency range. This material also possesses the mechanical compliance necessary to permit it to conform to all surface variations thus providing high efficiency flux closure. The keeper is instrumental in achieving the low drive currents and high signal levels of this design.

Because of an adherence problem at one interface in the 10 layer film array structure, an operable memory system was not achieved during this contract period. It has been possible, however, to identify and solve the vast majority of fabrication problems, and there is little doubt that this one remaining can be solved with additional time. The significance of the fabrication problem can be appreciated when considering the fact that the array consists of ten individual film layers each having a thickness of 20,000 Å to 60,000 Å. As a result of the work done under the fabrication effort, a compatible material system has evolved and detailed process techniques have been developed. Significant among these was the development of a new evaporation source to deposit thick SiO insulating layers at high rates and free of high stress regions near conductor edges. A patent application has been filed on the development of this source because of the importance of sound insulating layers in thin film circuitry of all types.

It is recommended that additional fabrication effort be extended to complete the processing of the complete memory system. Following evaluation of this completed system, a development effort directed toward increased density would be a logical successive program. From the system analysis performed, it is predicted that a scaling of one-half is easily attainable. Using the photo-lithographic processes herein developed, high tolerance line dimensions of a half scale system can be produced in a straightforward

manner. The work performed under this contract, therefore, provides the basic foundation upon which a highly sophisticated space oriented memory system can be developed.

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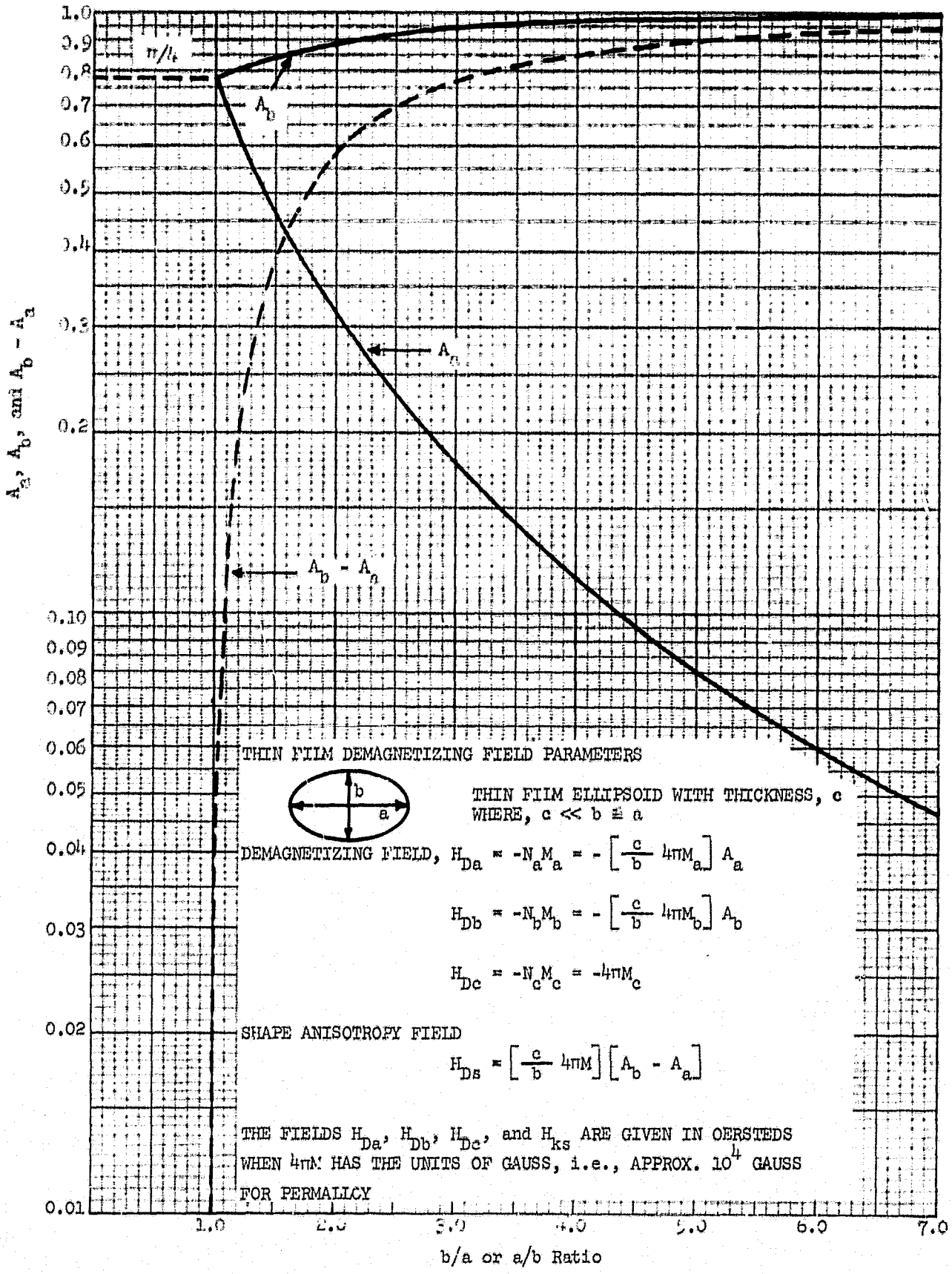
APPENDICES

APPENDIX A

DEMAGNETIZING FACTORS OF THIN FILM ELLIPSOID



APPENDIX B

DERIVATION OF KEEPER EFFECTS

Magnetostatic Fields From Film Edges

Whenever a discontinuity of magnetization occurs due to either a film edge or a domain wall, a magnetic surface charge distribution is established such that

$$\bar{n} \cdot \bar{M} = \sigma \qquad \text{(B.1)}$$

where

σ = surface charge density in poles per m^2

$\bar{M}$ = discontinuity in magnetization

$\bar{n}$ = outward normal unit vector at the surface.

If these charges act entirely in an isotropic uniform median, the resulting field due to them can be calculated easily from a magnetic scaler potential in an identical manner as electric charge. Hence,

$$U = \frac{1}{4\pi} \iint_{\text{surface}} \frac{\sigma ds}{r} \qquad \text{(B.2)}$$

and from this the magnetic field is calculated as the negative gradient of the potential, i.e.,

$$\bar{B} = -\mu_o \nabla U \quad . \qquad \text{(B.3)}$$

If the charge distribution is in the vicinity of a material boundary of different permeabilities there exists a second surface charge distribution at this boundary surface which alters the potential distribution and in general, requires a solution of Poisson's equation. However, if the boundary is simple, an image solution can often be obtained and such is the case with a magnetic film edge below a permeable keeper.

To demonstrate the effect of the keeper, consider a single point charge located below an infinite slab of material of permeability μ_2 as shown in Figure B.1.

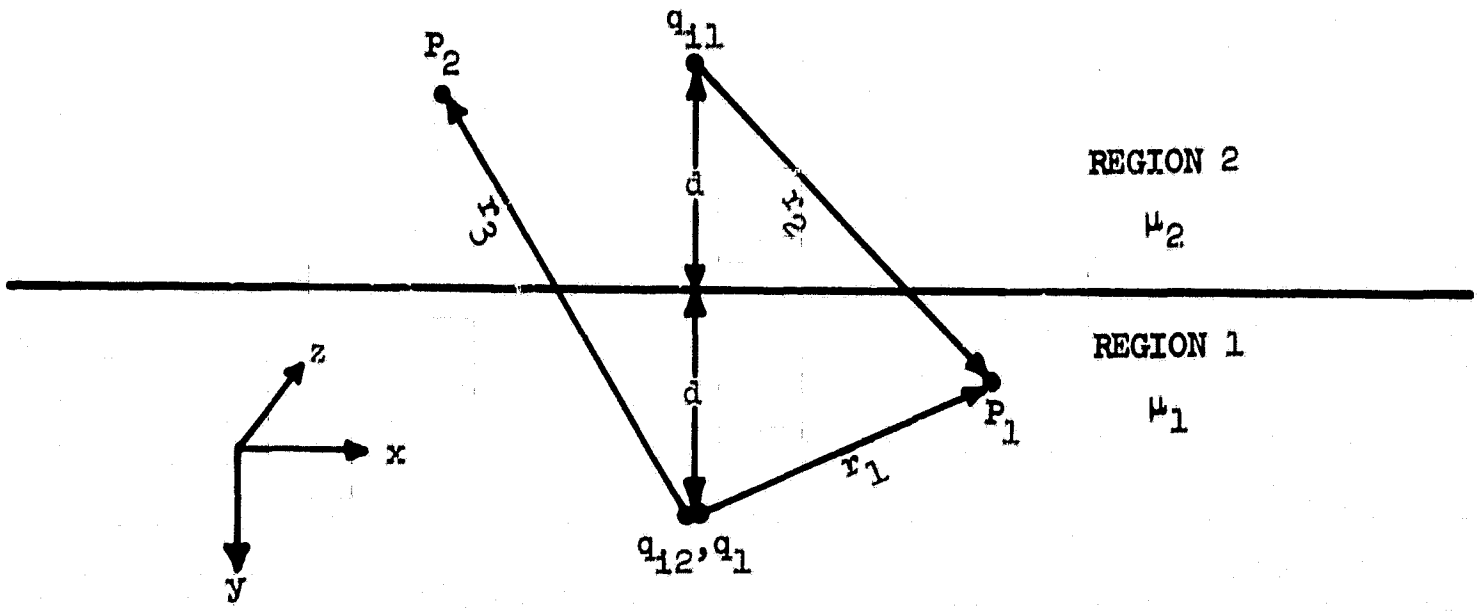


Figure B.1

Establish an image charge q_i at distance d within region 2. In order to determine the potential in region 2, it is necessary to establish an image in region 1. We let it be at the same location as q, but with magnitude q_{i2}. Thus in region 1, the potential at any point P_1 is given as:

$$U_1 = \frac{1}{4\pi}\left[\frac{q_1}{r_1} + \frac{q_{i1}}{r_2}\right] \qquad (B.4)$$

and in region 2 as:

$$U_2 = \frac{1}{4\pi}\left[\frac{q_{i2}}{r_3}\right] \qquad (B.5)$$

In rectangular coordinates:

$$r_1 = \sqrt{(y - d)^2 + x^2 + z^2}$$

$$r_2 = \sqrt{(y + d)^2 + x^2 + z^2} \qquad \text{(B.6)}$$

$$r_3 = \sqrt{(y - d)^2 + x^2 + z^2}$$

Now consider the case where P_1 and P_2 are brought together at any point (X, 0, Z) at the boundary surface. For this case $r_1 = r_2 = r_3 = r_o$ and the boundary conditions to be met are:

$$\text{at } y = o; \quad \mu_1 \frac{\partial U_1}{\partial y} = \mu_2 \frac{\partial U_2}{\partial y} \qquad \text{(B.7)}$$

and

$$\text{at } y = o; \quad U_1 = U_2 \ .$$

Hence,

$$\frac{1}{r\pi 4_o} (q_1 + q_{i1}) = \frac{1}{4\pi r_o} (q_{i2}) \qquad \text{(B.8)}$$

or

$$q_i + q_{i1} = q_{i2} \qquad \text{(B.9)}$$

Since

$$\frac{\partial U_2}{\partial y} = - \frac{1}{4\pi} \left\{ \frac{q_{i2}(y - d)}{\left[(y - d)^2 + x^2 + z^2\right]^{3/2}} \right\} \tag{B.10}$$

and

$$\frac{\partial U_1}{\partial y} = - \frac{1}{4\pi} \left\{ \frac{q_1(y - d)}{\left[(y - d)^2 + x^2 + z^2\right]^{3/2}} + \frac{q_{i1}(y + d)}{\left[(y + d)^2 + x^2 + z^2\right]^{3/2}} \right\} \tag{B.11}$$

Then at y = o

$$\mu_1 \frac{\partial U_1}{\partial y} = \mu_2 \frac{\partial U_2}{\partial y} \tag{B.12}$$

yields:

$$- \mu_1 q_1 d + \mu_1 q_{i1} d = - \mu_2 q_{i2} d \tag{B.13}$$

Solving the two resulting B.C. equations simultaneously gives:

$$- \mu_1 q_1 + \mu_1 q_{i1} = - \mu_2 q_1 - \mu_2 q_{i1} \tag{B.14}$$

or

$$q_{i1} = \left(\frac{\mu_1 - \mu_2}{\mu_1 + \mu_2} \right) q_1 \, . \tag{B.15}$$

Since we are seldom interested in the field in region 2, q_{i2} is unimportant. The result obtained then is that if $\mu_2 > \mu_1$ the field in region 1

can be found by replacing region 2 with a charge distribution identical to the original, symmetrical to the boundary, opposite in sign, and of 1 magnitude $|(\mu_1 - \mu_2) / (\mu_1 + \mu_2)|\ |q_1|$. Note if $\mu_2 \gg \mu_1$ the image becomes simply the negative of the original.

Effects of Current Distribution

If a current carrying conductor is located in close proximity to a boundary of two different permeabilities, a magnetic charge distribution will occur as a result of a discontinuity of M at the surface. Thus, consider a conductor in air $\mu = \mu_o$ located over an infinite plane slab of permeability μ as shown in Figure B.2. In the absence of the magnetic material the H field from the conductor would be uniform and by Amperes law equal to

$$\bar{H}_A = \hat{\theta}\left(\frac{I}{2\pi r}\right) .$$

The components of H normal to the surface, i.e., $H_\perp$ create a net vertical component of M in the material according to:

$$M_\perp = \chi H_\perp \qquad (B.16)$$

resulting in a discontinuity of M at the boundary since M(air) = 0.

Note it is only the vertical components of the external field which create a charge distribution. Thus, our image system must be configured to satisfy the requirements associated with this component.

Consider a small pill box region at the surface such that the field distribution is uniform over the area of the region as shown in Figure B.3. In the absence of the material boundary the original field at that location due to a current carrying conductor is simply

$$H_A = \hat{\theta}\left(\frac{I}{2\pi r}\right) = H_{11}x + H_\perp y . \qquad (B.17)$$

With the boundary, however, the resulting surface charge will modify the field both external and internal.

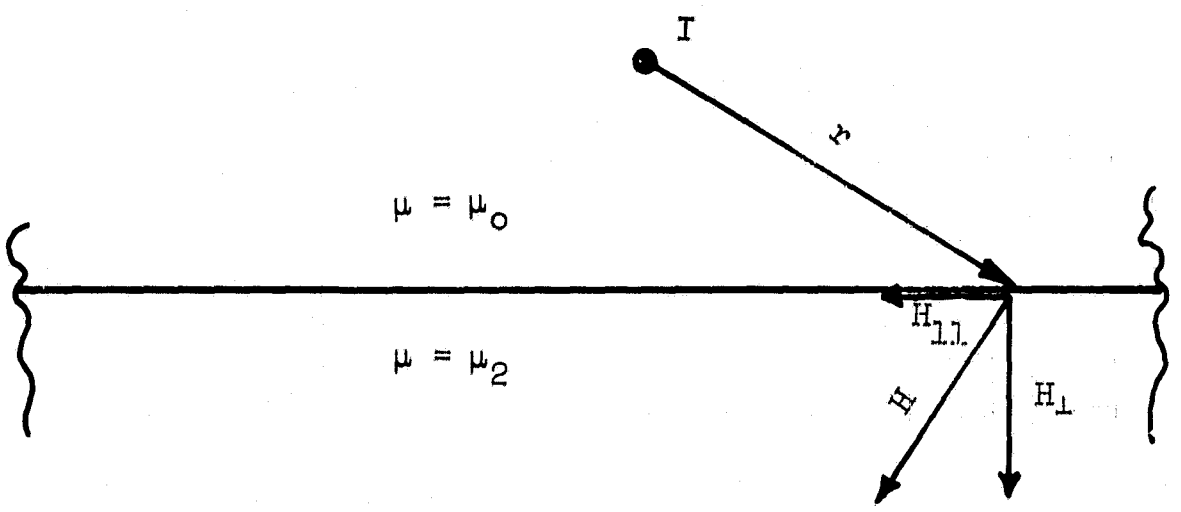


Figure B.2 Current Carrying Conductor Above a Keeper Surface

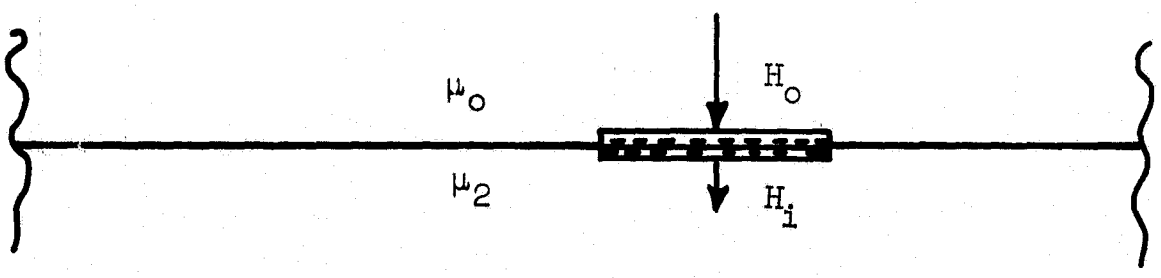


Figure B.3 Pill Box Construction Showing Field Distribution Above and Below the Keeper Surface

The surface charge within the infinitesimally thin box causes a field normal to the surface. By Gauss's law, this is simply

$$H_{\sigma\perp} = \frac{\sigma}{2} \tag{B.18}$$

The two net fields external to the box are then

$$H_i = H_\perp - H_\sigma \tag{B.19}$$

$$H_o = H_\perp + H_\sigma$$

where $H_\perp$ is the applied field in the absence of a material boundary. Since the surface charge is due simply to the discontinuity in magnetization at the boundary we have:

$$\sigma = M_2 = \chi_2 H_i \ . \tag{B.20}$$

Thus

$$2H_\sigma = \chi_2 H_i = \chi_2 (H_\perp - H_\sigma) \tag{B.21}$$

or

$$H_\sigma = \left(\frac{\chi_2}{2 + \chi_2}\right) H_\perp \ . \tag{B.22}$$

Since $\chi = \left(\mu/\mu_o - 1\right)$ the equation B.22 becomes:

$$H_\sigma = \left(\frac{\mu_2 - \mu_o}{\mu_2 + \mu_o}\right) H_\perp \tag{B.23}$$

Thus the effect of the boundary is to create a field at every point along the surface directly proportional to the applied field H_A at that point. With the plane boundary existing in this problem, the effect of the charge distribution can be accounted for simply by placing a current image on the opposite side of the boundary from the true source. The magnitude of this image current should be

$$I_{image} = \left(\frac{\mu_r - 1}{\mu_r + 1}\right) I_A \,. \qquad \text{(B.24)}$$

Here the image is a positive image as contrasted to the case where the source is a magnetic pole distribution.

APPENDIX C

DERIVATION OF FIELD FROM A THIN CURRENT CARRYING STRIP

The field resulting from a thin conducting strip is readily calculated to the first order as shown below. Consider the geometry of Figure C.1.

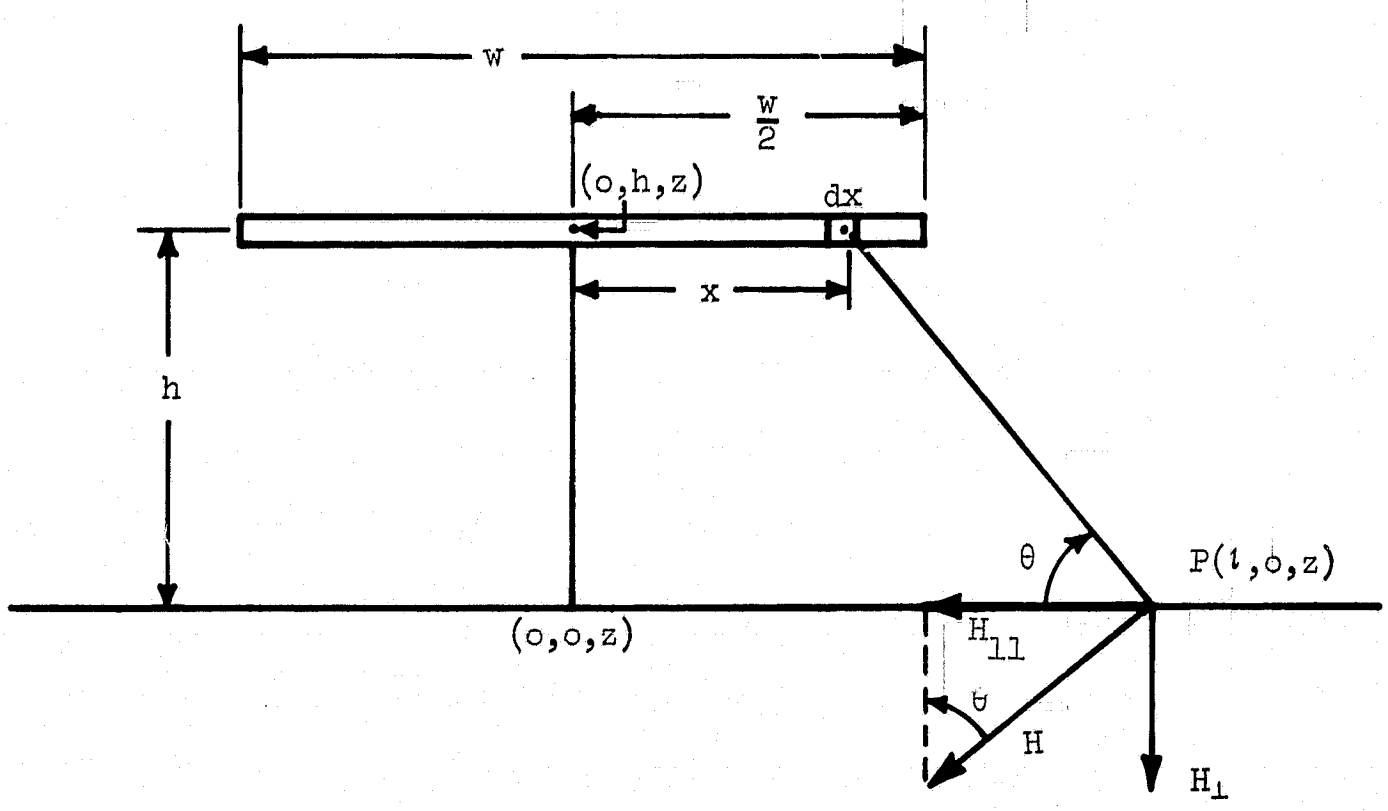


Figure C.1

Here we calculate the field at any point P resulting from a current I in the conductor. The conductor is w meters wide, and the point is located on a plane h meters below the line and at a distance ι meters from the line center. The line, i.e., the current carrying conductor, is assumed to extend to infinity in the directions perpendicular to the paper.

For a total current flow I amperes, uniformally distributed across the conductor, the current in an incremental element dx meters wide is simply

$$dI = \frac{Idx}{w} \tag{C.1}$$

and the incremental resulting field at point P is

$$dH = \frac{Idx}{2\pi rw} \tag{C.2}$$

In thin film work we are concerned only with the component of H parallel to the plane or

$$dH_{ll} = \frac{I \sin\theta \, dx}{2\, rw} \tag{C.3}$$

From the figure it is readily seen that

$$\sin\theta = h/r \tag{C.4}$$

and

$$r^2 = (\ell - x)^2 + h^2 \tag{C.5}$$

Thus carrying out the integral

$$H_{ll} = \int_{w/2}^{-w/2} dH_{ll} \tag{C.6}$$

we obtain the desired field as

$$H_{ll} = \frac{I}{2\pi w}\left[\tan^{-1}\left(\frac{\ell + w/2}{h}\right) - \tan^{-1}\left(\frac{\ell - w/2}{h}\right)\right] . \tag{C.7}$$

APPENDIX D

USING THE FOURIER SERIES PROGRAM

The Fourier program allows any periodic waveform or any waveform which can be forced into a periodic cycle to be decomposed into its Fourier series components. It then permits a component by component operation by any specified gain-phase versus frequency transfer function and recombines the resultant series into an output waveform.

Very basically, consider the following waveform to be analyzed.

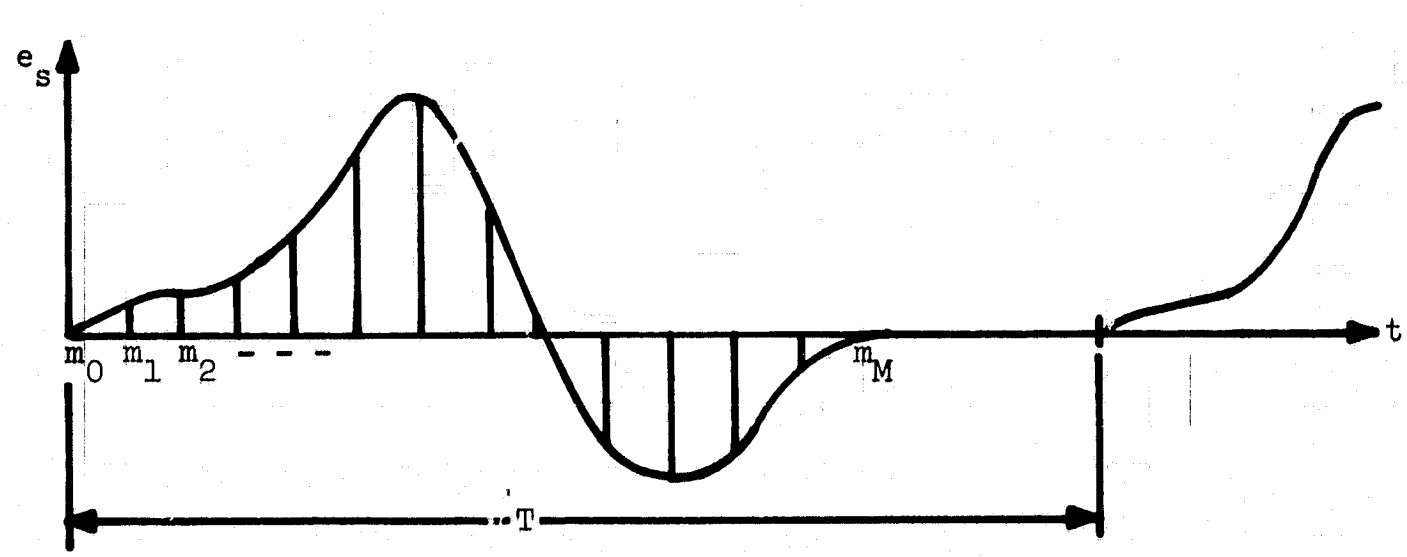


Figure D.1

The period of the waveform is shown as T seconds, corresponding to 2 π radians. The actual signal may cover any portion of the period T. The signal is sampled at M + 1 points and this provides the required input data.

The Fourier coefficients are calculated by the following sums:

$$A_n = \frac{1}{\pi} \sum_{m=0}^{M} \left[e_s(m) \cos \left(nm \frac{K\pi}{m} \right) \right] \frac{K\pi}{m} \qquad (D.1)$$

$$B_n = \frac{1}{\pi}\sum_{m=o}^{M}\left[e_s(m)\ \sin\ (nm\ \frac{K\pi}{M})\right]\frac{K\pi}{M} \qquad (D.2)$$

And yield a series of:

$$e_s(t) = \frac{A_o}{2} + \sum_{n=1}^{MAXC} A_n \cos\ (n\frac{2\pi}{T}\ t) + \sum_{n=1}^{MAXC} B_n \sin(n\ \frac{2\pi}{T}\ t) \qquad (D.3)$$

In the expression for the coefficients, the term $\frac{K\pi}{M}$ is the number of radians per interval, (region between samples). Thus if the M + 1 samples extended through total 2 π radians $\frac{K\pi}{M} = \frac{2\pi}{M}$ radians/interval. If the signal only existed for an equivalent of 200 degrees and was zero for the last 160 degrees, then taking M + 1 samples over the 200 degree interval would yield:

$$\frac{K\pi}{M} = \frac{(200/180)\pi}{M} = \left(\frac{200}{M}\right)\frac{\pi}{180}\ \frac{\text{rad}}{\text{interval}} \qquad (D.4)$$

The feature of sampling over only the region where the signal is significant with respect to zero permits maximum accuracy with reasonable size values of (M + 1), i.e., reasonable number of samples.

The previous equations include all the necessary information required by the program. A list of the specific information required is given below.

The first data card supplies:

(1) Number of intervals taken on the waveform. Equivalently, the number of total sample points less one. The program calls this JMM.

(2) Number of harmonics to be calculated. The program calls this JMAXC.

(3) Number of degrees per sample interval. This is calculated by the programmer as number of degrees over which samples were taken divided by the number of intervals. It is the

bracketed quantity in the right most factor of equation (D.4). Note the information is fed in as degrees per interval, not radians per interval. The program subsequently converts the number inputted to radians per interval. The computer calls this JDT.

(4) Period of one cycle in seconds. This is illustrated in Figure D.1 as T. The computer calls it JCAPT.

Following the first data card is a sequence of cards inputting the values of the sample amplitudes for each point. Each card contains four sample points. There must be JMM + 1 values sequentially given. The program calls these data JES [I].

With this information the computer calculates the Fourier coefficients specified, i.e., A_o, A_1, A_2, ... A_{JMAXC}, B_1, B_2, ... B_{JMAXC}. It prints out the following:

(1) Frequency of fundamental harmonic in cycles per second.

(2) Sample interval in radians/interval. (This is simply as a check for the programmer).

(3) List of Fourier coefficients.

The next data card inputted contains information allowing the program to construct the approximate waveform employing the previously generated coefficients. This card contains:

(1) Number of harmonics to be employed in the approximation. This value can be equal to or less than JMAXC. The program calls this JNH.

(2) Number of 2 π periods to be included in the output. The program calls this JNOP.

Using this data the program calculates the approximation to the input waveform and prints the output amplitudes at the same sample points used for input data. The format is:

$E_o(o)$	$E_o(1)$	$E_o(2)$	$E_o(3)$
$E_o(4)$	$E_o(5)$	$E_o(6)$	$E_o(7)$
$E_o(8)$	.	.	.
.	.	.	.
.	.	.	.
.	.	.	.
.	.	.	.
$E_o(M-1)$	$E_o(M)$	$E_o(M+1)$	.

Figure D.2

and continues in this manner until the number of periods specified by JNOP is complete. This output data can be punched on cards so that an automatic plot can be made. This is done by calling the PLOT procedure with a card added into the deck. This will be discussed later.

The last part of the program accepts as input, data specifying a gain-phase transfer characteristic, and calculates the effect of this on the Fourier approximated waveform. From some specified gain-phase plot, the programmer selects a set of samples which the program can use as data. The program performs linear interpolation between sample points and hence the data must be selected with this in mind. As an example consider the following gain-phase characteristics. Samples are taken at frequencies intersected by the dotted lines.

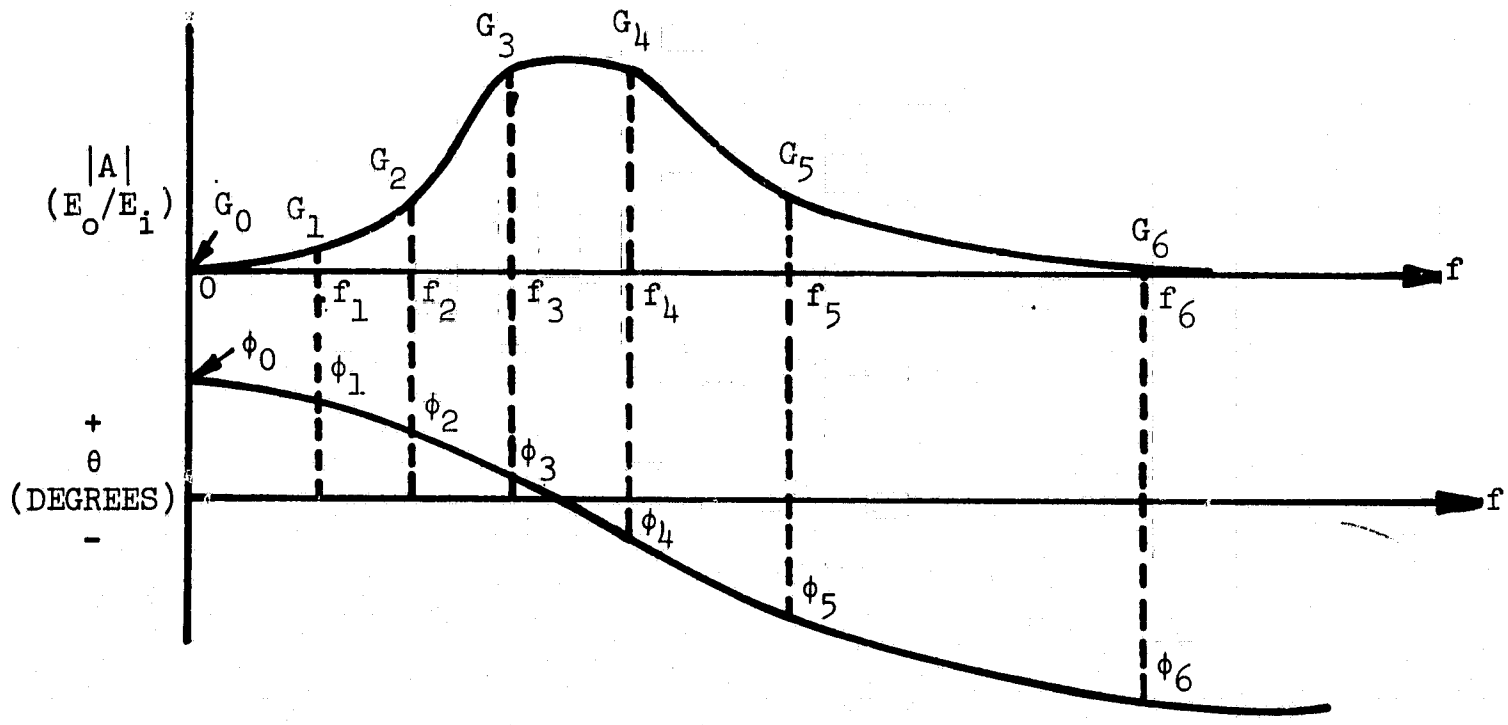


Figure D.3

The samples can be taken at any frequency desired and the sample intervals are completely independent. Only the following two restrictions hold:

(1) $|A|$ (n) and θ(n) must be taken at the same frequency.

(2) The frequency of the last point must be equal to or greater than the highest Fourier component to be employed.

Note $|A|$ is given simply as a number $\frac{E_o}{E_i}$ and <u>not</u> in db. Phase is given as degrees, <u>not</u> radians.

The data for this part of the program is supplied to the computer with the following cards:

(1) Card specifying number of gain-phase sample points to be supplied. This is simply a single integer number and is called <u>NUMPTS</u>.

(2) Next a sequence of cards containing the actual gain-phase data. Each card represents one sample frequency and contains three numbers in the following order:

(a) Frequency at which sample is taken; this is called <u>FREQ</u>.

(b) Gain magnitude at the sample frequency; this is called <u>GAIN</u>.

PROGRAM TITLE: INPUT DATA CARDS FOR FOURIER PROGRAM [SEQUENC

PROGRAMMER: _____ DATE: _____ PROBLEM NO.: _____

1st
nnn nnn ±n.ddde±ee ±n.ddde±ee
JNM JMAXC JDT JCAPT

2nd
±n.dd±ee ±n.dd±ee ±n.dd±ee ±n.dd±ee JES WITH E OPTION
±nnn.dd ±nnn.dd ±nnn.dd ±nnn.dd JES WITH F OPTION

3rd
nnn nnn
JNH JNOP

4th
nnn
NUMPTS

5th
n.dd±ee n.dd±ee ±n.dd±ee
FREQ GAIN THETA

PAGE _____ OF _____

220

(c) Phase shift in degrees at sample frequency; this is called THETA.

Using this data the program calculates a new set of Fourier Coefficients (the original set modified by gain specifications) and calculates a new Fourier series including the appropriate phase shifts. The number of harmonics employed is that previously specified as JNH. From this new series the program prints out data points corresponding to the waveform of the output function. The format is identical to that shown in Figure D.2. As before, the data may be punched out with the proper format to allow automatic plotting by calling the PLOT procedure.

Following is a summary of the sequence of input data and format required by the program:

ORDER	No. of CARDS	DATA	FORMAT
1st	One Card	JMM, JMAXC, JDT, JCAPT	2I5, 2E20.3
2nd	(JMM+1) Cards	JES [I] I=0, JMM	4R 12.2
3rd	One Card	JNH, JNOP	2I5
4th	One Card	NUMPTS	I3
5th	(NUMPTS) Cards	FREQ[F],GAIN[F],THETA[F] F=0,(NUMPTS-1)	3E12.2

The following page illustrates the formats in detail.

PLOT ROUTINE:

The PLOT routine is a procedure which punches tubular data in a format to be acceptable to the Mosley x-y plotter. In some programs where fine detail is desired and many points are calculated this procedure can save much time. The procedure is simply called by inserting a card with the following data punched:

PLOT (Identifier of Variable, Number of Data Points, File ID of Printer);

The procedure normalizes the entire list of data so the minimum value becomes 0 and the maximum becomes 100. It then punches a set of cards, each card being one data point, with an x coordinate, (0, 1, 2, 3, ...), and a y coordinate, ($0 \leq Y \leq 100$). From these cards a plot is made of Y vs. X on the plotter.

Renormalization to real values is effected by the programmer with the aid of a print out supplied by the procedure. This produces a set of

actual values at every 10 intervals from Y=0 to Y=100, i.e., Y(0), Y(10), Y(20) ... Y(100). In addition it also prints out the value of Y at which the zero axis occurs. A typical print out which was obtained during an actual program is shown below.

THE ZERO AXIS IS LOCATED AT Y = 7

VERTICAL AXIS SCALE IS AS FOLLOWS:

Y	VALUE
0	-8.729 @ -02
10	3.058 @ -02
20	1.484 @ -01
30	2.663 @ -01
40	3.842 @ -01
50	5.021 @ -01
60	6.199 @ -01
70	7.378 @ -01
80	8.557 @ -01
90	9.735 @ -01
100	1.091 @ +00

Since frequency techniques are a powerful approach to many system analysis problems it is believed that this program will find application in a variety of problem studies.

APPENDIX E

DERIVATION OF MAGNETIC SUSCEPTIBILITY FROM TORQUE MEASUREMENT

The torque on a magnetized sample in a uniform field H is given simply as

$$\bar{T} = \bar{M} \times \bar{H} \quad . \tag{E.1}$$

Assume the sample is planar in shape, i.e., a flat disk, hanging on a fiber which is along the Z axis. If the field has no Z directed component, then defining the i vector normal to the plane of the disk, and the j vector as tangent to the plane of the disk the following equations can be written.

$$\vec{H}_o = iH_{oi} + jH_{oj} \tag{E.2}$$

$$H_{oi} = \vec{H}_o \cdot i = H_o \cos\theta$$

$$H_{oj} = \vec{H}_o \cdot j = H_o \sin\theta$$

$$\vec{M} = iM_i + jM_j \,, \quad M_i = \chi H_i, \quad M_j = \chi H_j$$

$$H_i = H_{oi} + H_{di} \,, \quad H_j = H_{oj} + H_{dj}$$

$$H_d = -4\pi N M \qquad 1 > N > 0$$

$$\therefore H_i = H_{oi} - 4\pi N_i M_i, \quad H_j = H_{oj} - 4\pi N_j M_j$$

$$H_i = H_{oi} - 4\pi N_i \chi H_i \quad , \quad H_j = H_{oj} - 4\pi N_j \chi H_j$$

$$H_i = \frac{H_{oi}}{1 + 4\pi N_i \chi} \quad , \quad H_j = \frac{H_{oj}}{1 + 4\pi N_j \chi}$$

$$M_i = \frac{\chi H_{oi}}{1 + 4\pi N_i \chi} \quad , \quad M_j = \frac{\chi H_{oj}}{1 + 4\pi N_j \chi}$$

$$(\vec{M} \times \vec{H}_o)_z = k\,(M_i H_j - M_j H_i) = T_z$$

$$T_z = k\chi\left(\frac{H_{oi} H_{oj}}{1 + 4\pi N_i \chi} - \frac{H_{oj} H_{oi}}{1 + 4\pi N_j \chi}\right)$$

$$T_z = \tfrac{1}{2}\chi H_o^2 \sin 2\theta\left(\frac{1}{1 + 4\pi N_i \chi} - \frac{1}{1 + 4\pi N_j \chi}\right) \qquad \text{(E.3)}$$

Let $4\pi N = D$. Then replace T by T/V where V = the volume of the disk.

$$A = \frac{2T}{VH_o^2 \sin 2\theta} \quad , \quad A = \chi\left(\frac{1}{1 + D_i \chi} - \frac{1}{1 + D_j \chi}\right) \qquad \text{(E.4)}$$

Solving for χ gives:

$$\chi = \frac{-A(D_i + D_j) \pm [A^2(D_i - D_j)^2 - 4A(D_i - D_j)]^{\frac{1}{2}}}{2[AD_iD_j + D_i - D_j]} \qquad \text{(E.5)}$$

where in this case $A < 0$. Now for a flat disk, $D_i \approx 4\pi$, and $D_j = 0$. Replacing A by its magnitude and solving again for χ gives:

$$\chi = \frac{A \pm [A^2 + A/\pi]^{\frac{1}{2}}}{2} \qquad \text{(E.6)}$$

Obviously, only the positive root is meaningful here. Now, recall that in

the CGS system of units $\mu_R = 1 + 4\pi\chi$ and the calculation is complete. Following the method of Osborne and assuming the disk to have an elliptical cross-section, a suitable correction was applied to the value of χ by using the more exact relation.

APPENDIX F

CHARACTERISTICS OF DISTRIBUTED R-C TRANSMISSION LINES AS FEEDBACK ELEMENTS

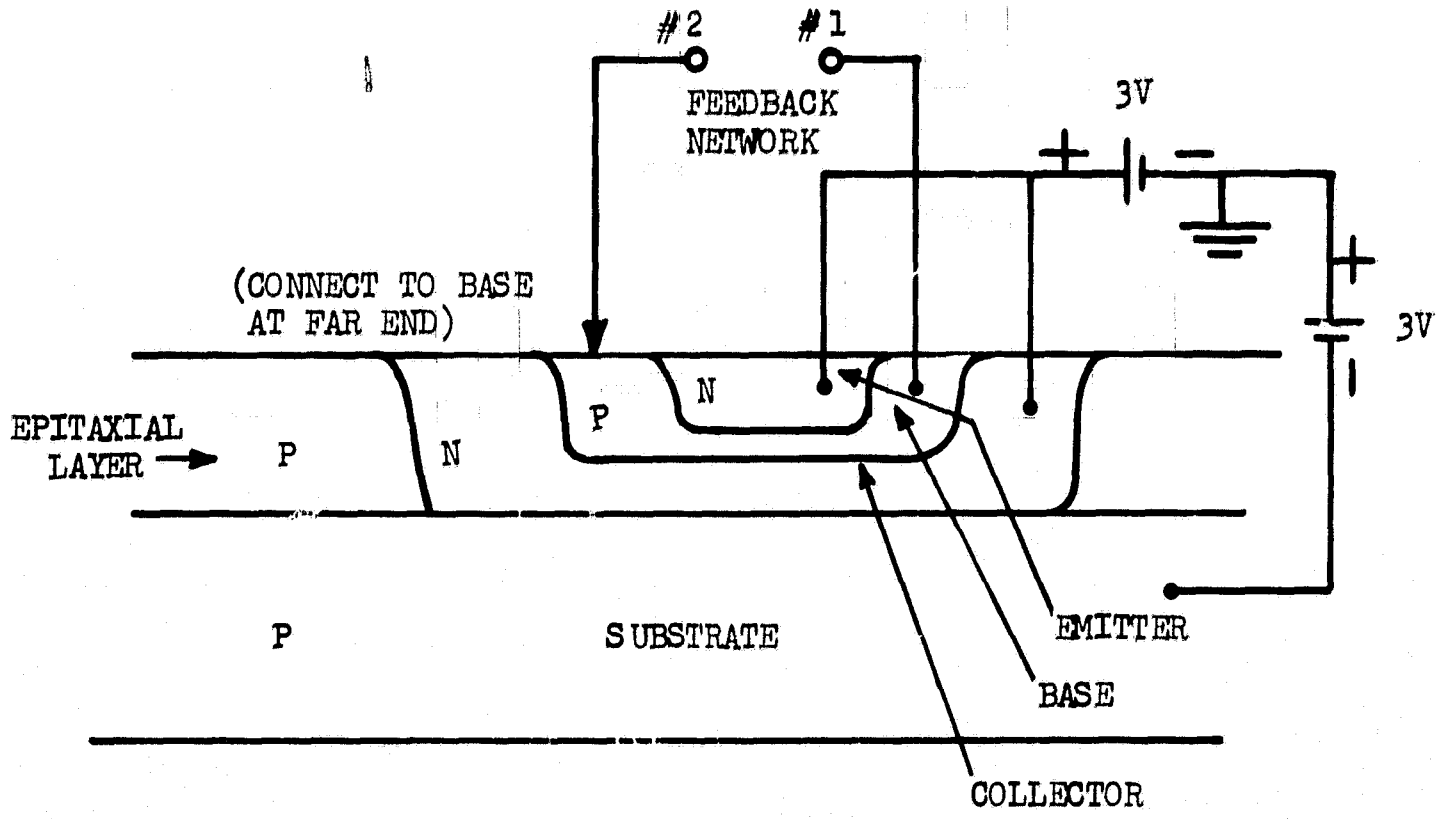
The comparative ease of fabrication of capacitors in a monolithic structure and the performance of the two schemes (coupling capacitors or feedback elements) will be compared. Most of this discussion is based on material in Reference (11), the text Integrated Circuits by the Motorola staff. Comparison of the coupling capacitor scheme with the feedback scheme is difficult in multi-stage amplifiers since the low frequency roll-off is 6 db/octave for each stage in a capacitor coupled amplifier whereas it is 6 db/octave for the entire amplifier with the feedback scheme. Moreover, for the model of Figure 4.5 the resistances are fairly well fixed so that only increasing the capacitance will lower the roll-off frequency in the capacitor coupled circuit. In the feedback circuit the time constant of the network is most important. Reference to Figure 4.6 will show the limitations on the R and C of the network. The dc gain of the amplifier is R_f/R_i, where R_f is the total series resistance of the feedback network. The input signal from the sense line is divided between R_i and the differential input impedance of the amplifier. Thus the maximum value of R_i is limited by signal attenuation. The input impedance of a typical stage is roughly several thousand ohms, so R_i is limited to values less than 1000 ohms for minimum signal attenuation. The amount of feedback, and hence the reduction of dc gain from mid-band gain, is limited by stability requirements. Thus the minimum value of the R_f/R_i quotient is limited by amplifier stability. Comparison and choice between the schemes depends on the high frequency roll-off of the differential amplifiers, the amount of initial offset and the offset which can be tolerated at the output collectors, and on the total forward gain of the amplifier under consideration. Since these characteristics of the amplifier are determined by the necessary small signal performance, the design of the feedback loop must be discussed after the small signal performance has been determined. For the amplifier under consideration, it turned out that the feedback capacitor C_f of Figure 4.6 needed to be about the same size as the coupling capacitor of Figure 4.5 in order to achieve a low frequency roll-off at about 800 kHz in both cases. This capacitance value was 100 picofarads. The feedback

series resistance can be fabricated in the same region of the chip as the capacitor. Thus the chip area occupied by the feedback network is no larger than the area required for the capacitor.

Figure F.1 shows a typical cross-section of an epitaxial-diffused monolithic structure. The various N and P regions can be connected together with ohmic contacts (not shown in the drawing) as indicated by the schematic. This interconnection scheme reverse biases each P-N junction and at the same time maximizes the capacitance between the series R element, the base diffusion, and signal ground. Here signal ground is not circuit ground but rather is the +3 volt supply. Knowledge of the sheet resistivity of the base diffusion, and typical junction capacitances as a function of biasing voltage, enables one to model the structure as a series R - shunt C transmission line. This structure results in a lossy transmission line, which is exactly what is needed as a feedback element. Because the base region of the monolithic transistor is shallow compared to the base diffusion depth, the conductivity of the line per unit length is determined by that portion of the base diffusion not under the emitter. The region under the emitter can be ignored not only because it has a small cross-section area, but also because the diffusion impurity level is typically an order of magnitude less there than at the top of the base diffusion region. This order of magnitude drop in impurity level makes the resistivity about an order of magnitude greater.

The resistance per unit length of line is easy to compute since the resistivity per square of the base diffusion is known. The unit of length for the line will be a mil since the width of each side of the base is 1/2 mil. Here the portion directly under the emitter diffusion is not considered to carry any appreciable current. The sheet resistivity of the base diffusion is typically 200 ohms/square. The resistance per unit length (one mil) of line is then 200 ohms.

The capacitance per unit length is more difficult to compute. Two junctions, base-emitter and base-collector, yield capacitance to signal ground. The effective capacitance of a reverse biased junction is a strong function of applied voltage. The emitter-base junction offers the greatest capacitance per unit area, but is rather lossy due to the high resistance of the region directly under the emitter. The Motorola staff implies that the base-collector junction is normally used for coupling applications even though the capacitance per unit area is less. For a coupling capacitor



TYPICAL DIMENSIONS:

Junction Depths - Emitter-base, 2.0 microns
Base-collector, 2.7 microns
Collector epitaxial width-25 microns thick
Minimum emitter width-1 mil
Clearance between emitter-base and base-collector junctions on surface-0.5 mil

Figure F.1 Cross-section of a typical monolithic structure showing junctions biased for use as a feedback element for the sense amplifier. The feedback element would be long and narrow, so terminal No. 2 would connect to base at the far end

application, series resistance such as that with the emitter-base junction results in direct signal losses and must be avoided. However, for applications such as a feedback network this series resistance is less important. Thus the shunt element of the transmission line model is a simple capacitor, rather than a capacitor and resistor in series. To take into account the isolation of the capacitor by the base resistance, one might use a lower figure of capacitance per unit area. Rather than attempt to simplify a complex problem, the capacitance figures listed in Table 10-1 of Reference (11) will be used directly. If such a network were to be constructed, actual measurements would be far more meaningful than calculations. The purpose of this section is not to design a working network, but rather to point out that the feedback network takes advantage of the distributed capacitance and resistance inherent in a monolithic structure, whereas a coupling capacitor has losses due to the distributed nature of the structure. In this particular application both the coupling capacitors and the feedback network will occupy about the same chip area, but given different, improved performance of the differential amplifiers, the feedback network would offer advantages with respect to the chip area occupied.

Two possible models for the feedback element are shown in Figure F.2. Since the feedback structure will be long and narrow, it will be treated as a transmission line. The models are for an incremental length of this line. As discussed above, the model of Figure F.2a is accurate but the element values are hard to estimate. The model of Figure F.2b is simplified in that the series resistance of the shunt leg is ignored and the capacitances are lumped together. The values shown are for a line with a 2 mil wide emitter diffusion and a 3 mil base diffusion. These are arbitrary, but reasonable, dimensions. The base diffusion sheet resistivity was assumed to be 200 ohms/square before the emitter diffusion.

The general transmission line is considered in many texts, e.g., Reference (18), Ramo, Whinnery, and Van Duzer's Fields and Waves in Communication Electronics. If a line has a distributed series impedance Z per unit length and a distributed shunt Y per unit length and the line is excited by a steady state sinusoid, the voltage and currents can be expressed as:

$$V(z,t) = \left(V_+ e^{-\gamma z} + V_- e^{\gamma z}\right) e^{j\omega t}$$

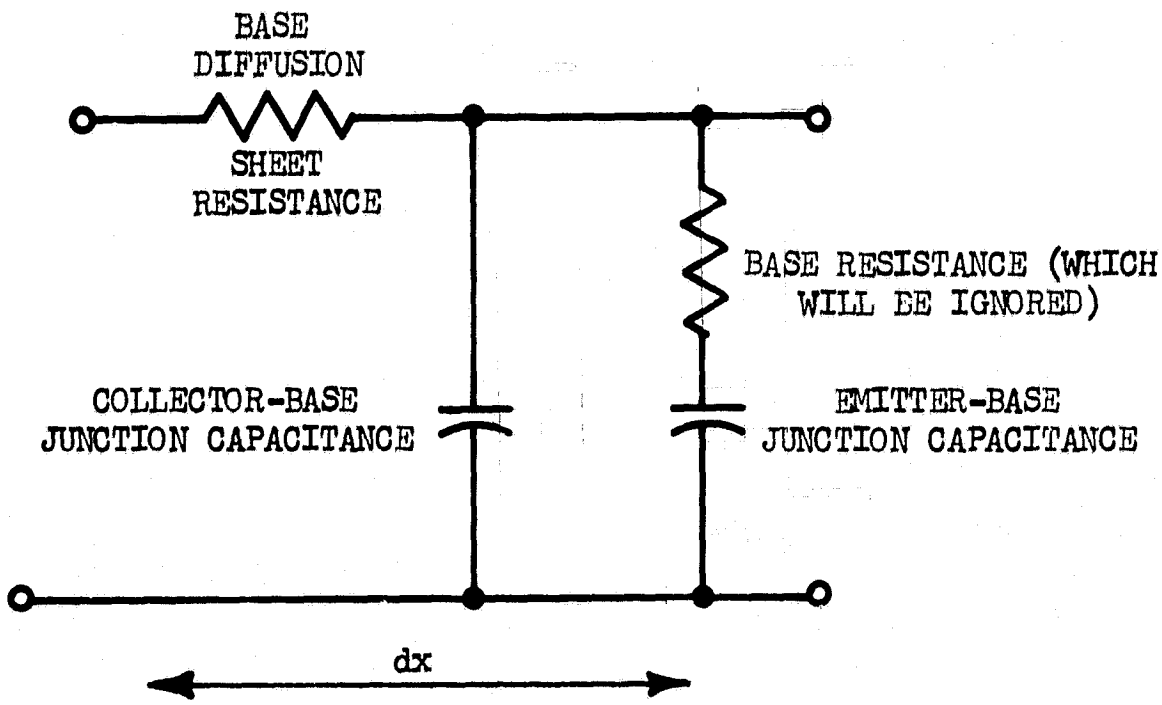


Figure F.2 Models for R-C transmission lines. Part (a) shows exact model for transmission line. Part (b) is a simplified model for a line with a 2 mil emitter and a 3 mil wide base

$$I(z,t) = \frac{1}{Z_o}\left(V_+ e^{-\gamma z} - V_- e^{\gamma z}\right)e^{j\omega t}$$

where V_+ and V_- are complex coefficients determined by the boundary conditions on the line, ω is the excitation frequency and γ and Z_o are determined by the line parameters. The propagation constant γ is given by

$$\gamma = (ZY)^{1/2}$$

Since Z = R and Y = $j\omega$C for the model of Figure F.2b,

$$\gamma = (\omega RC/2)^{1/2} + j(\omega RC/2)^{1/2} .$$

Here the real and imaginary parts have been explicitly shown. Taking the values shown in Figure F.2b for R and C, we have

$$\gamma = (175 \times 10^{-12}\omega)^{1/2} (1 + j)$$

The propagation constant is seen to be a function of frequency, as expected for a lossy line. The characteristic impedance is also a function of frequency and is given by

$$Z_o = (Z/Y)^{1/2} = (R/2\omega C)^{1/2} (1 - j) = (57.1 \times 10^{12}/\omega)^{1/2} (1 - j)$$

The coefficients V_+ and V_- are determined by considering the termination at each end of the line. An equivalent circuit is shown in Figure F.3. The line is shown as 50 units in length, which corresponds to a base diffusion 50 mil long in the integrated circuit.

The solution of the line equations for the voltage transfer ratio $V_o/V_i = V(0,t)/V(z,t)$ is a function of frequency and line length. The general procedure will be given here and the transfer ratic V_o/V_g will be

computed for a line length of 50 mil and for several excitation frequencies. The magnitude and phase of the transfer ratio may be recorded on a Bode plot and a smooth curve drawn through the points. This curve will allow the transmission line to be replaced by an equivalent lumped circuit.

Given a line length and an excitation frequency, the procedure is as follows:

1) R_L and Z_o are known. Form the voltage reflection coefficient

$$\rho(0) = \frac{V_-}{V_+} = (R_L - Z_o)/(R_L + Z_o) \quad .$$

The reflection coefficient is a function of z. In general

$$\rho(z) = (V_-/V_+)\, e^{2\gamma z} \quad .$$

The reflection coefficient gives the ratio between the incident and reflected waves at any point on the line.

2) Use the Smith chart to compute the reflection coefficient at the input to the line, that is, $\rho(-50)$.

3) The input impedance to the line may also be determined.

$$Z_i = Z_o \frac{1 + \rho(-50)}{1 - \rho(-50)}$$

4) The voltage at the input terminals to the line may now be computed. Reference to Figure F.3 will show that $V_i = Z_i V_g/(Z_i + R_g)$.

5) There are now two equations for V(-50).

$$Z_i V_g/(Z_i + R_g) = V_+ e^{50\gamma} + V_- e^{-50\gamma}$$

$$\rho(-50) = (V_-/V_+) e^{-100\gamma}$$

Remember that both ρ and Z_i are functions of frequency. These equations may be solved for V_+ and V_-.

6) The output voltage may now be written as

$$V_o = V_+ + V_- \ .$$

The complete expression is

$$V_o(t) = e^{j\omega t}(V_+ + V_-) \ .$$

Several transfer ratios have been worked out for the line described. A load resistance of 500 ohms and a generator resistance of 2500 ohms were assumed as typical. The results are tabulated in Figure 4.7.

The distributed line does not behave like a simple R-C network; yet it is still useful as a feedback element. Care needs to be taken in designing the feedback loop, but once the loop is designed, the fabrication problems should be less with the feedback system than with coupling capacitors since stray losses are unimportant. Loop design will proceed in a conventional fashion once the small signal characteristics of the amplifier are known.

APPENDIX G

PHOTO RESIST PROCESSING

Kodak-Metal-Etch-Resist (KMER) and AZ-111 resists were used for photoengraving metal films in multilayer film structures. Specimens were placed in a clean covered petri dish and stored in a desiccator when the photoengraving of films did not follow immediately the vacuum deposition process; hence, they remained dry and reasonably clean before application of the respective photo resists. In general, process procedures recommended by the vendor of each resist were followed. Specific processing details are given below for each resist, and processing apparatus are discussed in Section V-A-3.

Processing of KMER

KMER, KMER Developer, and KMER Thinner are products of the Eastman Kodak Company. KMER was used effectively for masking in the precision etching of both aluminum and chromium-gold films. For spin application, the resist was thinned by mixing one volume of resist with one volume of thinner. The resist was filtered during application by applying it with a 20 cc hypodermic syringe fitted with a micro-syringe filter holder (Millipore Filter Corporation Cat. No. XX30 025 00). A 14 μ filtering membrane was used. The stepwise process was as follows:

(1) Place substrate on spinner,
(2) Spin substrate at 2000 r.p.m. for a few seconds to remove dust particles,
(3) Stop spinner and cover substrate surface with 1:1; KMER:KMER Thinner,
(4) Spin at 1500 r.p.m. for 2 minutes,
(5) Apply a second coat by repeating steps (3), and (4),
(6) Place on hot plate at a regulated temperature of 110°C and bake for five minutes,
(7) Mask substrate with appropriate contact photomask in vacuum frame,
(8) Expose with exposure lamp for 1 minute,
(9) Develop in dish of KMER Developer for 1-1/2 minutes - mildly agitate solution,

(10) Remove from KMER Developer and while still wet, spray with reagent grade xylene for 1 minute (a solvent spray gun was operated at 20 to 40 psi and held at a distance of about 12 inches from specimen),

(11) Dry with jet of dry air or nitrogen from spray gun,

(12) Examine the developed image with a stereomicroscope. Usually the best development resulted by repeating steps (9) thru (11) with a development period of 30 seconds in the KMER Developer.

After etching of the metal film, the KMER image was stripped or removed. A commercial stripping solution, Resist Strip J-100, of the Indust-Ri-Chem Laboratory, Richardson, Texas was used in this process. The procedure was as follows:

(1) Place substrate on the bottom of a 1 litter beaker with the film side up,

(2) Add 50 ml of concentrated Resist Strip J-100,

(3) Heat solution to 100°C and leave in solution at this temperature for three to five minutes,

(4) Spray film surface vigorously with the J-100 solution using a hypodermic syringe,

(5) Remove from stripping solution and spray with reagent grade Xylene at 40 psi to remove J-100 solution,

(6) Dry with jet of dry air or nitrogen,

(7) Inspect and repeat if necessary.

In the inspection of step (7), a stereomicroscope was employed at magnifications ranging from 3X to 60X. To aid in the detection of remnant resist, the substrates were placed on a clean piece of blue cobalt glass. A directional microscope lamp was held so that the light intercepted the surface at a large angle of incidence while the surface was viewed from near normal direction with the microscope. This technique permits the detection of surface particles that are not ordinarily seen with full field illumination. It is very difficult to remove completely the remnants of KMER with commercially available stripping solutions. The remnant material is a slimy scum-like substance that is extremely adherent to metal and glass surfaces. In fact, this laboratory has been unable to completely remove the scum even by cleaning in hot sulfuric acid. Better stripping of KMER can be had by ultrasonically cleaning in hot J-100 stripper. Ultrasonic cleaning

was used quite satisfactorily on single layer aluminum, gold over chromium films, and multiple layers of aluminum or Cr-Au-Cr with silicon monoxide; however, permalloy films were damaged with the ultrasonic technique; hence the technique could not be used after the permalloy film was deposited in the multilayer memory structures. Where excessive damage to metal films or the substrate does not occur, cleaning in hot (150°C) chromic acid or sulfuric acid is very effective in removing the scummy remains of KMER. These acids can be used for cleaning chromium - gold films quite satisfactorily.

Processing of Type AZ-111 Resist

Type AZ-111 photo resist and its developer were obtained from the Shipley Company, Inc. The resist was used primarily for masking to photoengrave permalloy films. Spin application similar to that for the previously discussed KMER was employed at first. However, the resist mask had too many pin holes when applied in double coats at a spin speed of 2500 r.p.m. Eventhough a clean box was used for applying the resist, the laboratory was not a clean room, and dust collection on the substrate surface was probably the main source of trouble. To eliminate the pin hole problem, the substrates were dip-coated by submerging them in the unthinned resist and slowly withdrawing to form a uniform film of the resist. The thicker coatings of resist obtained in this manner eliminated the pin hole problem. The remainder of the processing was as follows:

(1) Lay resist coated substrate on a level surface and dry in air at room temperature for 15 minutes,
(2) Place on a hot plate regulated at a temperature of 90°C and bake for 20 minutes (15 minutes of baking was satisfactory for thinner films applied by spinning),
(3) Mask substrate with appropriate contact photomask in vacuum frame,
(4) Expose with exposure lamp for 10 minutes,
(5) Develop in dish of solution consisting of 4 volumes of deionized water to one volume of AZ-303 developer - mildly agitate solution,
(6) Remove from developer and while still wet, rinse well with tap water using considerable pressure,
(7) Dry with hot air gun (do not heat resist above 95°C),

(8) Examine the developed image with a stereomicroscope. Usually the best development resulted by repeating steps (5) thru (7) with a development period of 30 seconds.

After etching of the permalloy film, the resist image was stripped. Since AZ-111 is a positive working resist it can readily be removed by exposing the image and removing in the regular developer; this method was used primarily. The unexposed resist can be removed in acetone. Thus, to insure complete removal of the resist, acetone was used in subsequent cleaning processes before additional films were deposited over the permalloy films.

APPENDIX H

SUBSTRATE CLEANING METHODS

The following are stepwise descriptions of the two substrate cleaning methods used at various stages of fabricating multilayer film structures. Reagent grade chemicals were used in both methods. In the performance of these cleaning procedures, the substrates were not allowed to dry between successive baths. The methanol rinse of step 5, method 1, was used primarily to remove water from the substrates and rack before degreasing since water and trichloroethylene do not mix very well. The trichloroethylene degreaser was used primarily as a storage point immediately before film deposition and as a technique of drying the substrates to obtain a streak-free surface rather than for any unique cleaning or degreasing property of the tricholoroethylene vapor. Cleaning method number 1 was used for initial cleaning of substrates and for cleaning chromium-gold films after photoengraving and stripping of photo resist (KMER). For the latter cleaning, the acid temperature was increased to 125 to 150°C for more effective removal of remnants of KMER. Method number 2 was used for cleaning permalloy films after photoengraving and stripping of photo resist (AZ-111). Cleaning apparatus is discussed in Section II-A-4.

Cleaning Method 1

(1) Scribe code numbers on back of substrates and arrange in deposition order in substrate cleaning rack,

(2) Place racked substrates in a fresh hot chromic acid bath, about 100°C, for 5 minutes (chromic acid formed by saturating concentrated sulfuric acid with chromium trioxide at room temperature -- keep acid dish covered to minimize oxidation at elevated temperatures),

(3) Remove from the chromic acid and rinse away gross acid with flowing demineralized water,

(4) Submerge racked substrates in high purity water rinse, Figure 5.4, leave in recirculating bath a minimum of 10 minutes after resistivity returns to a minimum of 15 megohms,

(5) Remove racked specimens from water rinse and rinse with methanol from a blow flask,

(6) Place racked substrates in trichloroethylene degreaser for a minimum of 10 minutes or until ready to place in vacuum deposition apparatus,

(7) Slowly remove substrates from degreaser,

(8) Use cleaned tweezers to remove substrates from cleaning rack and position in holders in the vacuum deposition apparatus.

Cleaning Method 2

(1) Place racked substrates in a beaker of boiling acetone for three to five minutes,

(2) Rinse with methanol from a blow flask,

(3) Continue with steps (4) thru (9) of Method 1.