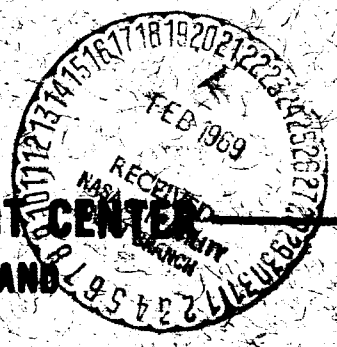
X-616-68-455

NASA TM X- 63452

DIGITAL PRE-FILTERED ADAPTIVE DELTA MODULATION APPLICATION TO MAGNETIC FIELD EXPERIMENT

CHARLES V. MOYER

DECEMBER 1968



GSFC

GODDARD SPACE FLIGHT CENTER
GREENBELT, MARYLAND

X-616-68-455

DIGITAL PRE-FILTERED ADAPTIVE DELTA MODULATION APPLICATION TO MAGNETIC FIELD EXPERIMENT

Charles V. Moyer
Laboratory for Space Sciences

December 1968

NASA GODDARD SPACE FLIGHT CENTER
Greenbelt, Maryland

DIGITAL PRE-FILTERED ADAPTIVE DELTA MODULATION APPLICATION TO MAGNETIC FIELD EXPERIMENT

Charles V. Moyer
Laboratory for Space Sciences

ABSTRACT

This document describes a digital high pass filter and an adaptive delta modulator to be used for on board data compaction of satellite-acquired magnetic field data.

The high pass digital filter removes the spin modulation from the magnetic field data. The adaptive delta modulator provides a four to one bit rate reduction compared to straight PCM encoding.

A feasibility model of the filter and adaptive delta modulator working in conjunction has been built and tested. Development of a flight quality unit for IMP H and J is in progress at this time.

PRECEDING PAGE BLANK NOT FILMED.

CONTENTS

	Page
ABSTRACT	iii
INTRODUCTION	1
ADAPTIVE DELTA MODULATION	2
DIGITAL HIGH PASS FILTER	12
Overflow and Saturation of the Digital Filter	14
Amplitude and Phase Transfer Functions of the Low Pass Digital Filter	19
High Pass Filter Transfer Function	22
Multiplication	27
Addition and Subtraction	28
SUMMARY	28
ACKNOWLEDGMENT	30
REFERENCES	30
APPENDIX	31

ILLUSTRATIONS

Figure		Page
1	Linear Delta Modulation Boundary Curve	3
2	Increase in Sampling Rate to Cover Signal Spectrum	4
3	Attenuation of Signal to Fit Within Delta Modulation Boundary	5
4	Two Bit Per Sample Adaptive Delta Modulator Reproducing a dc Signal and the Nyquist (Two Samples Per Cycle) Frequency	6

ILLUSTRATIONS (Continued)

Figure		Page
5	Two Bits Per Sample Adaptive Delta Modulator Following dc Signal	8
6	Three Modes of Operation — One Bit Adaptive Delta Modulator Following dc Signal	9
7	Block Diagram Two Bit/Sample Adaptive Delta Modulator	10
8	Block Diagram — Digital High Pass Filter	13
9	Logic Diagram — Single Stage of Low Pass Filter	15
10	Low Pass Filter	16
11	Low Pass Filter Transfer Characteristics	23
12	Calculated Values of Attenuation vs Multiples of Spin Frequency from Equation (28)	26
13	Multiplication by a Constant	28
14	Addition and Subtraction with a Serial Full Adder	29
A-1	One Bit Adaptive Delta Modulator with Oscillation Suppression	33

TABLES

Table		Page
1	Delta Modulation/Picture Parameters	7
2	Adaptive Delta Modulator Truth Table	11
3	Calculated Values of Attenuation and Phase For the Low Pass Filter, Calculated From Equations (21) and (22)	22
4	Calculated Values of Attenuation vs Multiples of the Spin Frequency, Calculated From Equation (28)	27
1A	One Bit Adaptive Delta Modulator Truth Table	31
2A	Truth Table for One Bit Adaptive Delta Modulation with Oscillation Suppression	32

DIGITAL PRE-FILTERED ADAPTIVE DELTA MODULATION

APPLICATION TO MAGNETIC FIELD EXPERIMENT

INTRODUCTION

Magnetic field measurements in space are often made on spinning satellites, the spin period being in the range 1 to 15 seconds. The magnetic field is measured by 3 magnetometers oriented in three mutually perpendicular axes. Two (A and B) of the three magnetometers measure fields normal to the spin axis. The magnetometers A and B have spin modulated data while magnetometer C measures the component of the magnetic field parallel to the spin axis of the satellite and is not spin modulated. It follows that the output of magnetometers A and B, while in a stable and non-changing magnetic field, will be in the form of a sinusoid whose period is equal to the spin duration.

The magnetometer signal can be sampled at any rate, limited only by the digital logic speed, but the telemetry space available limits the amount of information which can be transmitted.

Imposed on the spin modulated signal will be fluctuations due to intercepting the magnetosheath of the earth, crossing the earth's magnetic tail as well as intrinsic fluctuations in separate regions of cislunar space. Some of the transients in the measured magnetic field may be quite abrupt, i.e., when crossing the bow shock or magnetic tail there might be field reversals and the encountering of high (relative to the spin frequency) frequency variations in the field.

Much of the data contained in a spin modulated sinusoid is redundant. Thus the telemetry channel assignment is used inefficiently unless data compaction is attempted.

Information about the direction, strength and time variations of the magnetic field is of interest. At this time the following question should be answered: Should data compaction be of the form that allows some calculated quantities of interest to be transmitted, i.e., spectrum analysis data, or statistical data; or should the data compaction be of the form which allows the raw signal data to be transmitted in its minimal form (with respect to the total number of bits required to convey a given piece of information).

The writer has chosen the latter of the two approaches in order to preserve a maximum amount of raw data. The data compaction unit for use on IMP H and J magnetic field experiment is an adaptive delta modulator preceded by a digital high pass filter.

The function of the high pass filter is that of removing the satellite spin-generated sinusoid which modulates the magnetic field signal, thus easing the requirements imposed on the adaptive delta modulator.

Magnetic field data signals with frequencies lower than the spin frequency, which would otherwise be lost due to filtering, are recovered by transmitting complete field strength values at appropriate sampling rates. Data on magnetic field fluctuations at or above twice the spin frequency, and up to 16 times (IMP H) or 32 times (IMP J) the spin frequency will be transmitted by delta modulation.

The hardware for the analog to digital convertor, digital filter and adaptive delta modulator is low power TTL logic. Feasibility models of both the digital filter and the adaptive delta modulator have been tested and found satisfactory.

ADAPTIVE DELTA MODULATION

Adaptive delta modulation is a method of removing some of the redundancies found in PCM data. The redundancy removal is accomplished by predicting the signal, based on its past performance, and transmitting information which indicates the difference between the predicted value and the actual value.

The adaptive delta modulation, described in this document, is used to gain a 4 to 1 bit rate reduction in the transmission of magnetic field data. The 4 to 1 data compaction ratio is defined by the comparison of bits required, for two bits per sample adaptive delta modulation or 8 bits per sample, straight PCM encoding.

Since linear delta modulation is slope rather than amplitude limited, constraints are imposed on the signals which can be transmitted by linear delta modulation. The spectrum which can be transmitted by linear delta modulation is shown in the amplitude vs frequency plot of Figure 1. As long as the signal spectrum remains inside the shaded area in Figure 1 it can be transmitted by linear delta modulation. When a signal, not fully contained within the boundaries described, is to be transmitted by delta modulation, one or more of the following approaches may be taken:

1. Increase the sampling rate as shown in Figure 2 which shifts the boundary curve from position A to position B thus accommodating the signal spectrum described by curve C. This method is generally wasteful of bandwidth, though usually the most readily implemented.

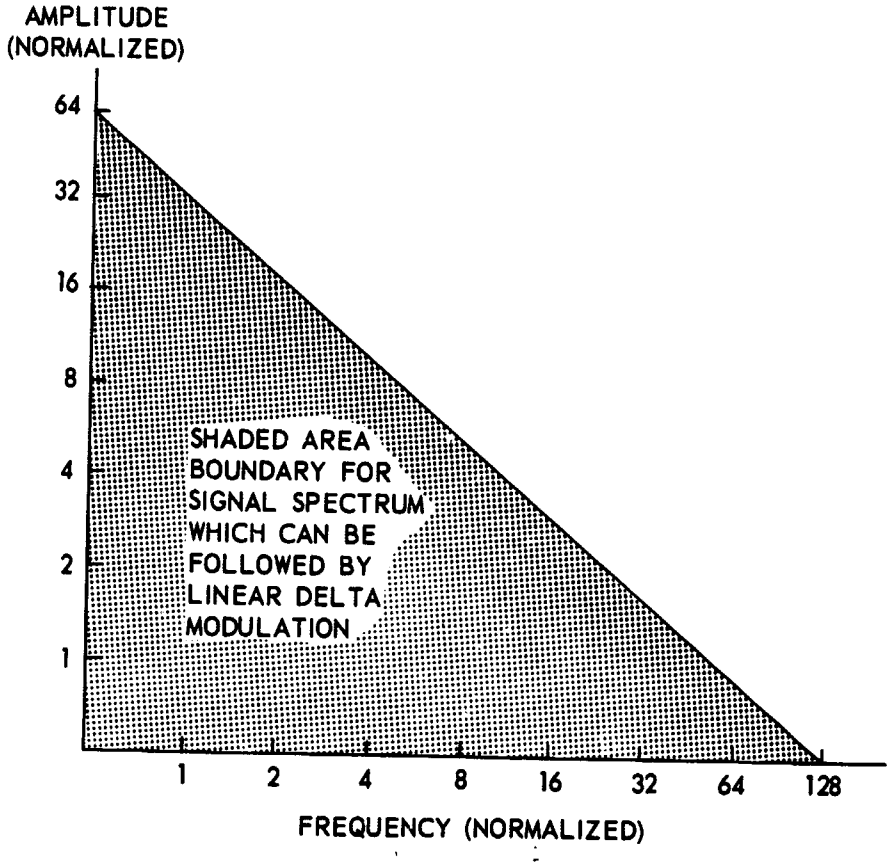


Figure 1. Linear Delta Modulation Boundary Curve

2. Attenuate those frequencies which do not fit within the boundaries of the curve, as shown by point A in Figure 3, to position A' well within the boundary of the delta modulation curve. When the signal has a particular frequency, or frequencies, attenuated a fixed and known amount by a linear filter, the signal can be reconstructed at the receiving end by amplifying those frequencies which had been attenuated.

3. Implementing adaptive modes to accommodate steep slopes. Adaptive delta modulation is also called variable slope, and variable increment delta modulation.

4. Use of multibit (more than one bit per sample) delta modulation.

Inherent with delta modulation is a tendency towards oscillatory modes. The oscillations are within the signal spectrum being transmitted and can appear

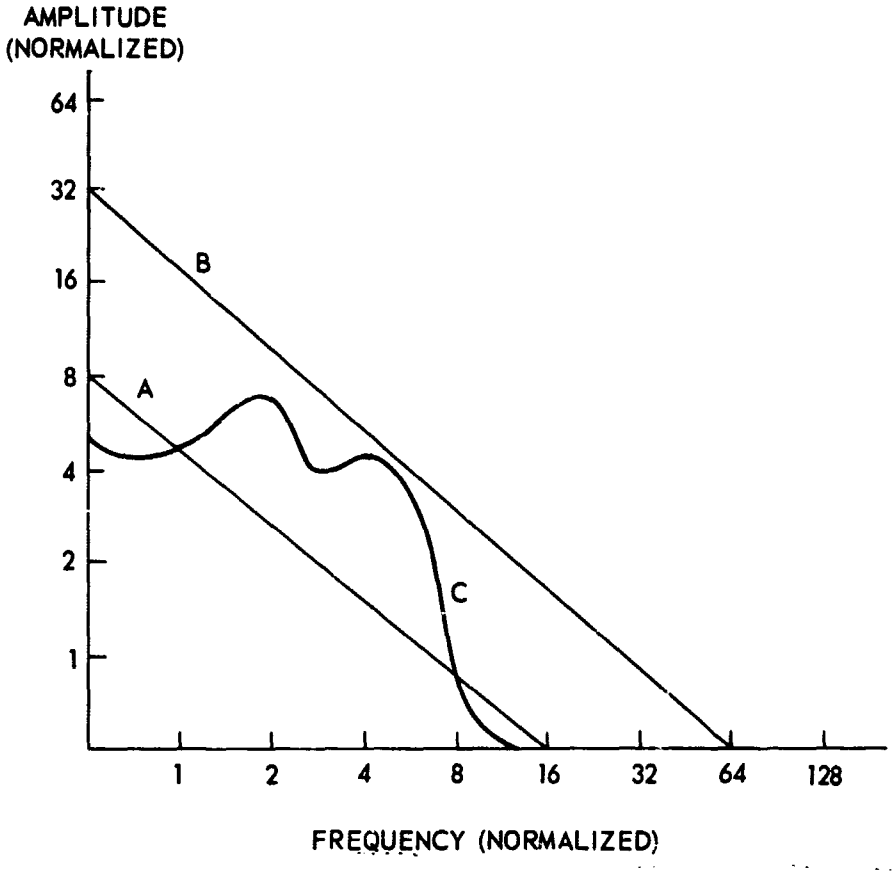


Figure 2. Increase in Sampling Rate to Cover Signal Spectrum

as false signals. In television pictures being transmitted by delta modulation these oscillations may appear as a herringbone or similar type patterns superimposed on the picture.

In practice, in the case of 6 to 8 bit quantization of the signal, one or two bits per sample delta modulation is reasonable. Three or more bits per sample becomes wasteful of bandwidth because:

1. The highest frequency which can be transmitted is limited by the Nyquist sampling rate which requires a minimum of two samples per cycle.

2. A two bit per sample delta modulator (requiring twice the bit rate of one bit per sample delta modulator) can transmit, as the highest frequency twice the frequency of a one bit delta modulator (both having the same sampling rate), and thus not be wasteful of bandwidth. Figure 4 shows the

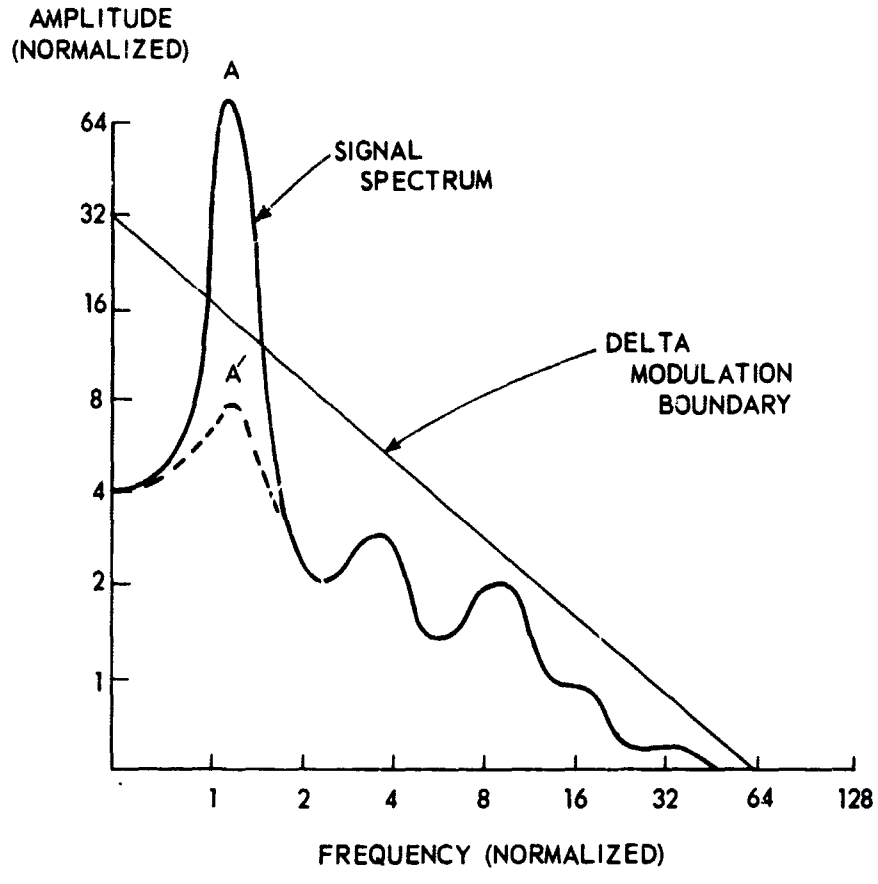


Figure 3. Attenuation of Signal to Fit Within Delta Modulation Boundary

reproduced samples of a two bit per sample adaptive delta modulator for both a dc signal and the highest transmittable signal frequency. From the diagram it can be seen that the two bit per sample approach does not waste bandwidth, since the highest frequency which may be transmitted is double that of the one bit per sample approach.

3. Three or more bits per sample does not increase the maximum frequency which can be transmitted over the one or two bit per sample adaptive delta modulator (which both require the same number of bits for the same maximum frequency). Hence any increase in bits per sample over two consumes excess bandwidth for a given maximum frequency.

Two significant advantages are present in the two bits per sample over the one bit per sample adaptive delta modulator.

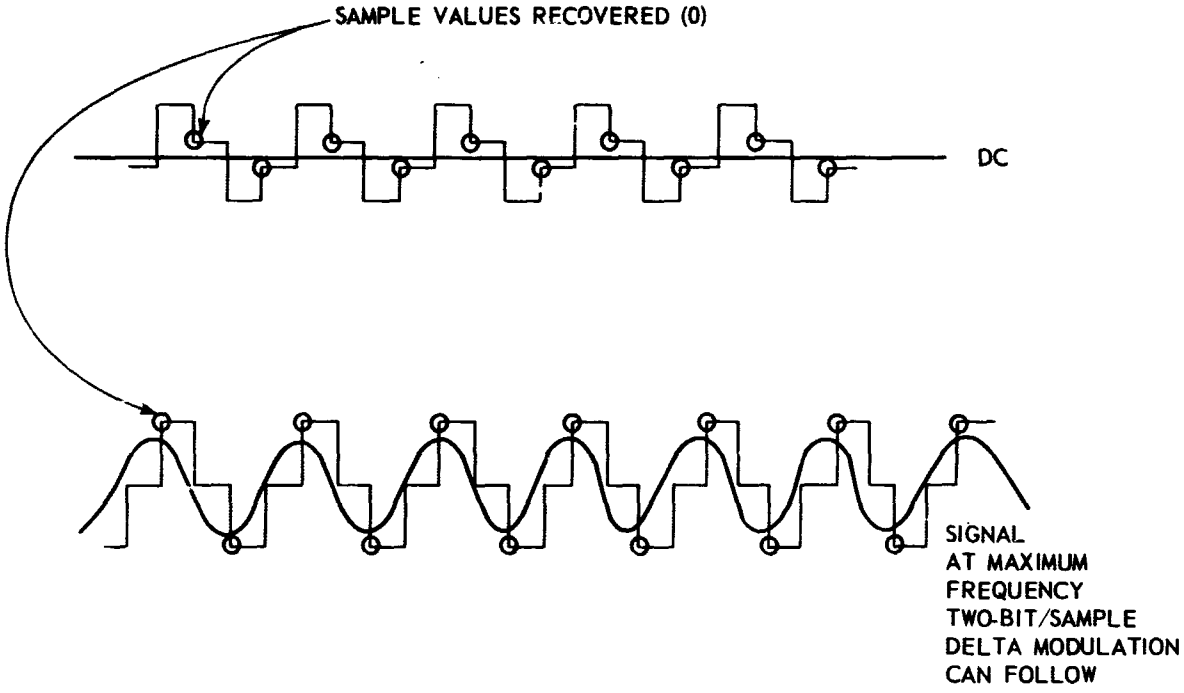


Figure 4. Two Bit Per Sample Adaptive Delta Modulator Reproducing A DC Signal and the Nyquist (Two Samples Per Cycle) Frequency

1. The sampling rate is compatible with the digital filter sampling rate.

2. The two bits per sample adaptive delta modulator cannot oscillate in the presence of a dc signal. A one bit per sample adaptive delta modulator can have several modes of oscillations in the presence of a dc signal.* Figure 5 shows three modes of operation for a one bit adaptive delta modulator of a particular type (±1, ±2, ±4 adaptive). It can be seen that two modes of operation in the presence of a dc signal yield oscillations not readily discernable from real signals. Figure 6 is a two bit per sample adaptive delta modulator of the type to be used for magnetic field data compaction on IMPs H and J. It can be seen that it is impossible for oscillations to exist in the presence of a dc signal, which would be the normal, low activity output of the digital high pass filter.

As a point of related interest it may be noted that there is much difficulty in comparing and evaluating large numbers of combinations of sampling rates,

*See the Appendix of this report for one bit delta modulator oscillation suppression details.

adaptive modes and number of bits per sample. One method of comparison which has been used extensively[1] is television picture quality for various delta modulation methods. Table 1 shows some delta modulation characteristics and some related picture quality characteristics. This method of evaluation and comparison shows the immediate results of all conceivable input signals.

Table 1

Delta Modulation/Picture Parameters

Delta Modulation Parameters	Related Picture Parameters
Quantization Noise	Narrow Horizontal Streaks
Phase Distortion Slope Response Transient Response	Vertical Wiggle
Frequency Response	Washed Out Picture, Fuzzy Picture
Amplitude Resolution	Contouring of Grey Levels
Oscillations	Superimposed Patterns
Integrator Time Constant	Black and White Saturation

The costs of bandwidth reduction by adaptive delta modulation are:

1. Loss of resolution when following steep slopes.

2. Oscillations at critical slopes.

The design of the two bit adaptive delta modulator used the same adaptive modes as an adaptive delta modulator[2] flown on AIMP-D and which was used for picture transmission. The hardware used, and the design for the magnetic field data delta modulator is significantly different. The hardware design for the magnetic field data delta modulator uses low power TTL logic and is completely digital. Comparisons, additions and subtractions are all performed in serial arithmetic. Figure 7 is a block diagram of the adaptive delta modulator to be

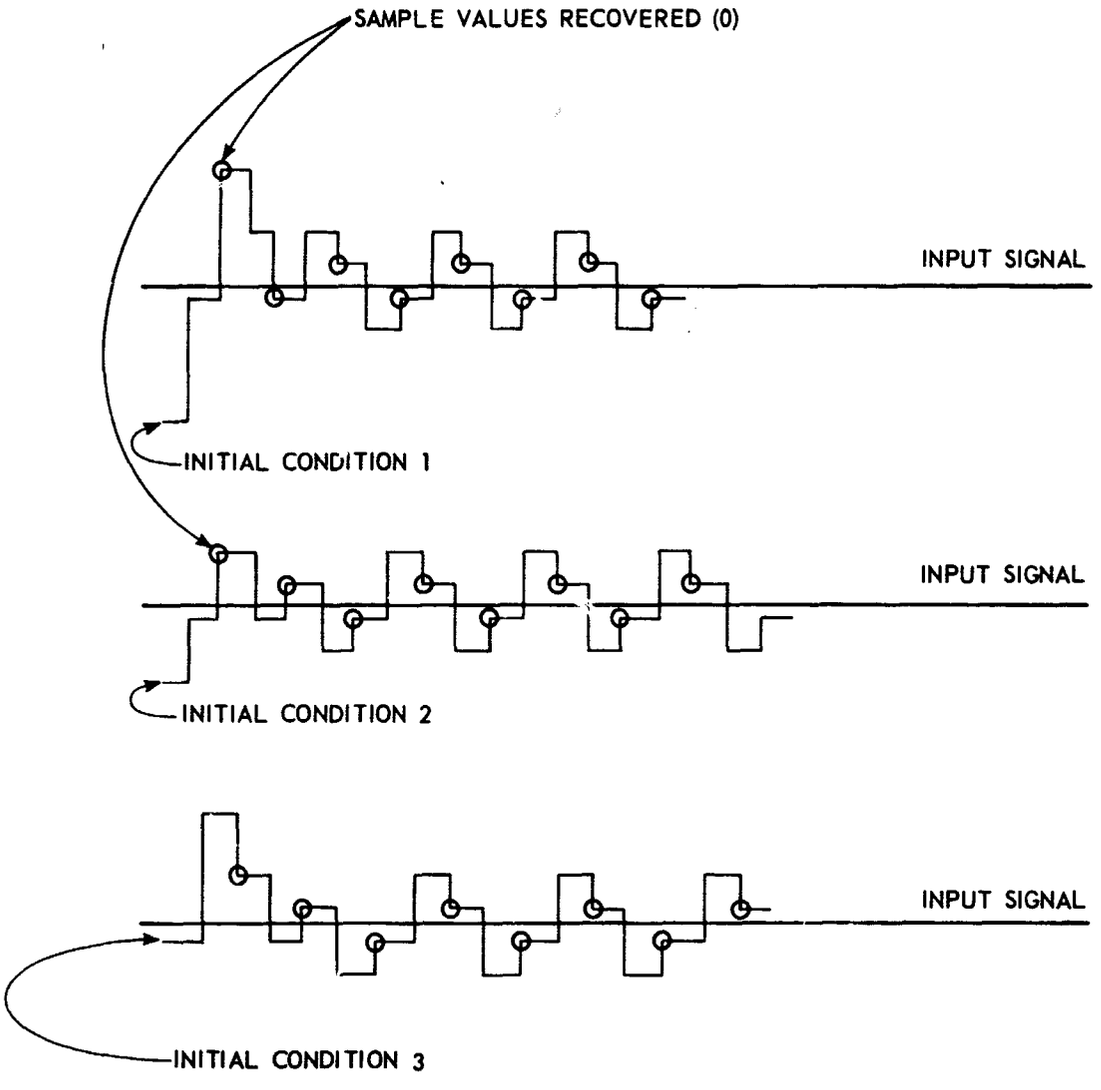


Figure 5. Two Bits Per Sample Adaptive Delta Modularor Following DC Signal

flown on IMPs H and J. In operation, a data sample is serially compared to the contents of the Integrator Register. The comparison 1 or 0 corresponding to plus or minus is then transferred to the State Register. This information plus 3 previous comparisons and the step number 1 or 0 corresponding to Step 1 or 2, determine the number ± 1, ± 2, or ± 4 to be placed in the Increment Register. The contents of the Increment Register is then added to the contents of the Integrator Register with the sum being placed in the Integrator Register.

The second step is similar to the first, using the same sample, which had been stored in the Sample Register. The only difference between the step one

and the step two operation is the number placed in the Increment Register for a given number in the State Register. The number placed in the Increment Register is a function of the step number and the last 4 comparisons (states). The bits transmitted by the delta modulator are the states (two bits per sample). Table 2 is a truth table of the step sizes and polarities.

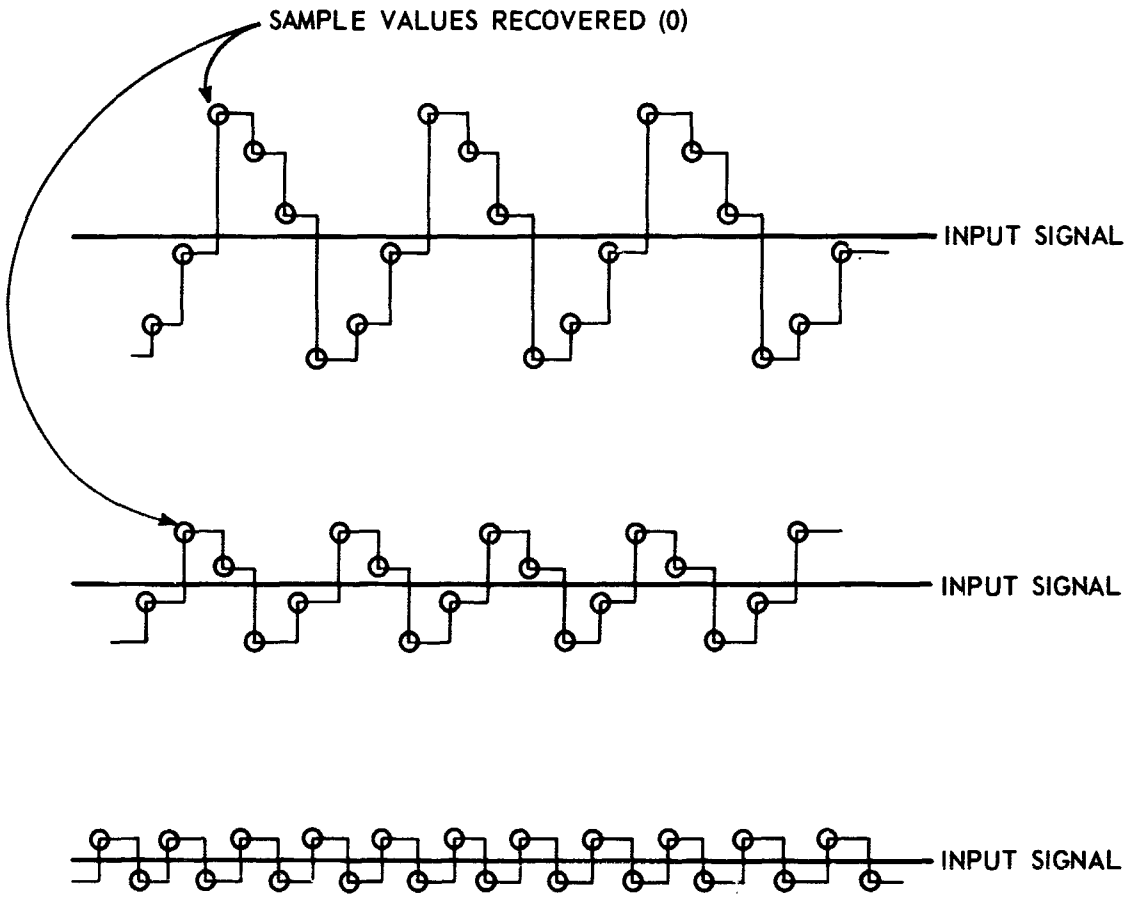


Figure 6. Three Modes of Operation – One Bit Adaptive Delta Modulator Following DC Signal

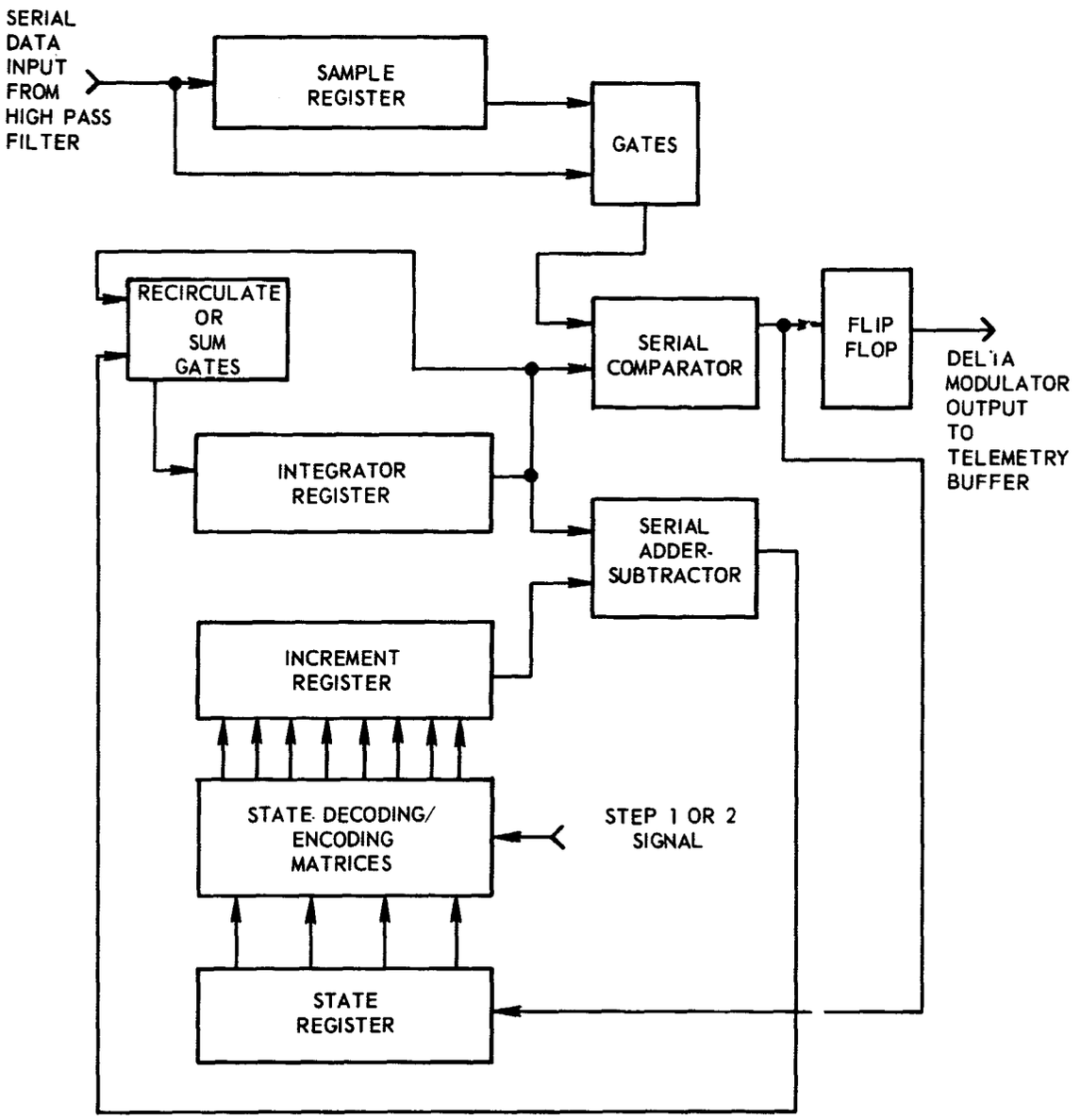


Figure 7. Block Diagram Two Bit/Sample Adaptive Delta Modulator

Table 2

Adaptive Delta Modulator Truth Table

Step Size and Sign	Step Per Sample 1 = 1st 0 = 2nd	Comparator Outputs			
		Present At Time	Past 3 Decisions At Times		
		t	t - 1	t - 2	t - 3
+4	1	1	1	1	1
+4	1	1	1	1	0
+2	1	1	1	0	1
+2	1	1	1	0	0
+2	1	1	0	1	1
+2	1	1	0	1	0
+2	1	1	0	0	1
+2	1	1	0	0	0
-2	1	0	1	1	1
-2	1	0	1	1	0
-2	1	0	1	0	1
-2	1	0	1	0	0
-2	1	0	0	1	1
-2	1	0	0	1	0
-4	1	0	0	0	1
-4	1	0	0	0	0
+4	0	1	1	1	1
+2	0	1	1	1	0
+2	0	1	1	0	1
+2	0	1	1	0	0
+1	0	1	0	1	1
+1	0	1	0	1	0
+1	0	1	0	0	1
+2	0	1	0	0	0
-2	0	0	1	1	1
-1	0	0	1	1	0
-1	0	0	1	0	1
-1	0	0	1	0	0
-2	0	0	0	1	1
-2	0	0	0	1	0
-2	0	0	0	0	1
-4	0	0	0	0	0

DIGITAL HIGH PASS FILTER

The digital high pass filter removes the spin modulation from the magnetic field signal. A high pass filter is used in preference to a band reject filter for the following reasons:

1. A very narrow band reject filter would pass both upper and lower sidebands of the magnetic field signal (when its frequency is lower than the spin modulation) and the spin frequency. The sidebands would so closely resemble the spin modulation that the slope limited capabilities of the adaptive delta modulator would be exceeded.

2. Broadening the band reject filter to eliminate the side bands associated with magnetic field signals lower than the spin frequency, in effect, makes the band reject filter similar to a high pass filter.

3. Using a high pass filter instead of a broad band reject filter results in:

    a. The loss of very little information because of the lower skirt of the broad band reject filter extending down to the region of dc, noting that this information (contained in the upper and lower sidebands around the spin frequency) can be efficiently recovered by taking absolute samples (prior to filtering) at the low sampling rates required.

    b. Elimination of ambiguities resulting from having pass bands above and below the spin frequency.

    c. Elimination of a hardware two-variable multiplier.

    d. Ease of quick graphical analysis of transient responses.

A digital filter is used in preference to an analog signal filter because:

1. The capacitors required for the low (less than 1 Hz) frequency would be too large and/or unstable with respect to the capacitance tolerance required for the filter.

2. The digital filter will shift its characteristics, i.e., cutoff point, to accommodate a varying spin rate, because the filter characteristics are sample rate dependent and the sample rate is in synchronism with the spin.

Figure 8 is an elementary block diagram of the high pass filter. The filter will first be described in general terms to be followed by a detailed description.

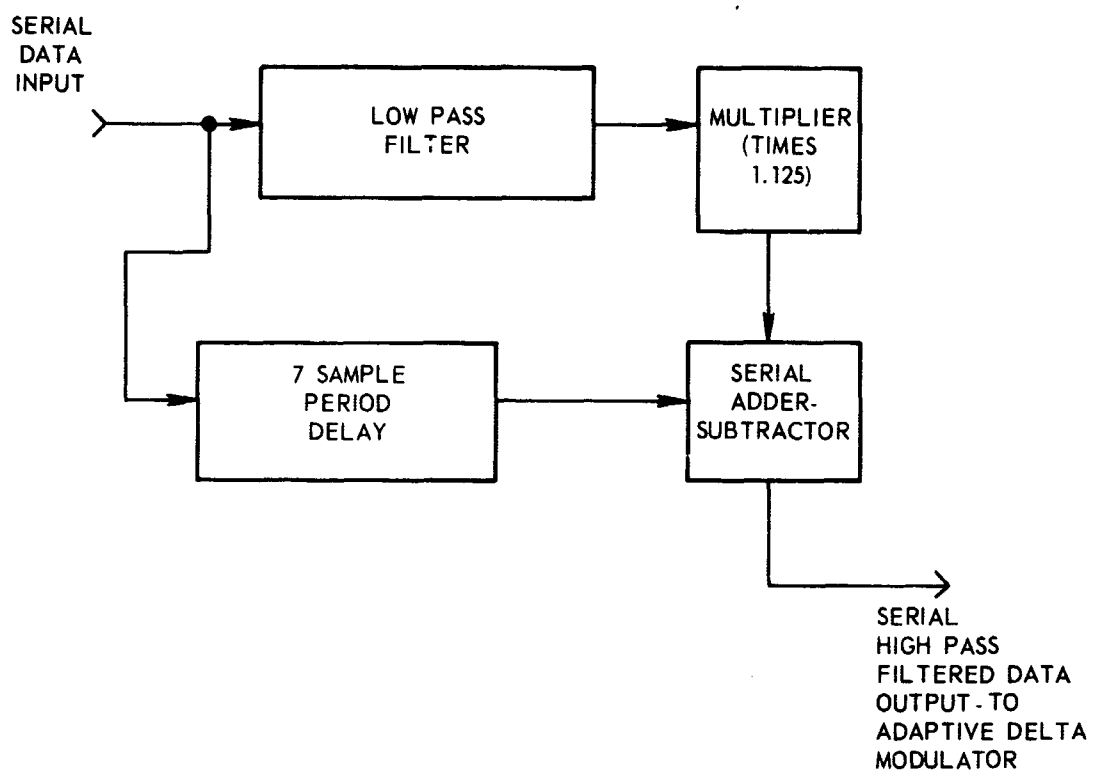


Figure 8. Block Diagram – Digital High Pass Filter

The data coming from the experiment is in the form of positive numbers. In the presence of a uniform magnetic field the spinning magnetometers with their 8 bit digital outputs describe a sinusoid symmetrical about the positive number 128 plus or minus the zero level offset. The difference between the number 128 being the axis of symmetry of the sinusoid and another number i.e., 135 is due to the offset of the zero level of the magnetometers. Thus, if the maximum reading is 173 and the minimum reading is 73 and the magnetic field is unchanging then the true zero point is 123 instead of 128. In practice the zero point might have a maximum offset of 20 out of a full scale reading of 256.

In order to place the data into a usable format as easily as possible, the most significant bit is inverted so that the sinusoidal data is now in two's complement form when the count is less than 128. With the most significant bit of the data word inverted (and now being the sign bit, minus = 1, plus = 0) and negative numbers in two's complement the data is now in a form conducive to arithmetic operations.

The data is first low pass filtered digitally, and in addition to going to the filter also goes to a delay so that the delayed incoming data is in phase with the filtered data. Since the low pass filtered data is slightly attenuated at the spin frequency, it is multiplied by a factor of 1.125 for restoration to its original value.

With the low pass filtered data now in phase (at the spin frequency) with the delayed incoming data and amplified to be the same magnitude (at the spin frequency), the only difference in the two signals is any high frequency information on the original signal.

One stage of the low pass filter is shown in Figure 9. Figure 10 shows three stages of the filter cascaded. This filter is similar in characteristics to a low pass RC analog filter, with interstage isolation. The operation of one stage of the filter is as follows:

1. An incoming word (LSB first) is added to the contents of the shift register.

2. When the addition has been performed, one extra clock pulse shifts out the last bit of the sum thus implementing a divide by two operation.

3. This operation is then repeated for eacn incoming word.

4. The contents of the shift register and the incoming data are in normal form when positive and in two's complement form when negative. Hence when the contents of the register is positive and the incoming data is negative a subtraction is performed by the serial full adder.

Overflow and Saturation of the Digital Filter

Figure 10 is three stages, or the entire low pass filter. It can be seen that there is no feedback from one stage to another. Because there are no feedback paths, one stage of the filter can be treated separately, and the combined effects of three stages may readily be calculated by adding stage attenuation and phase shifts.

Figure 9 is one stage of the filter and employs:

a. One 8 bit shift register

b. One full adder

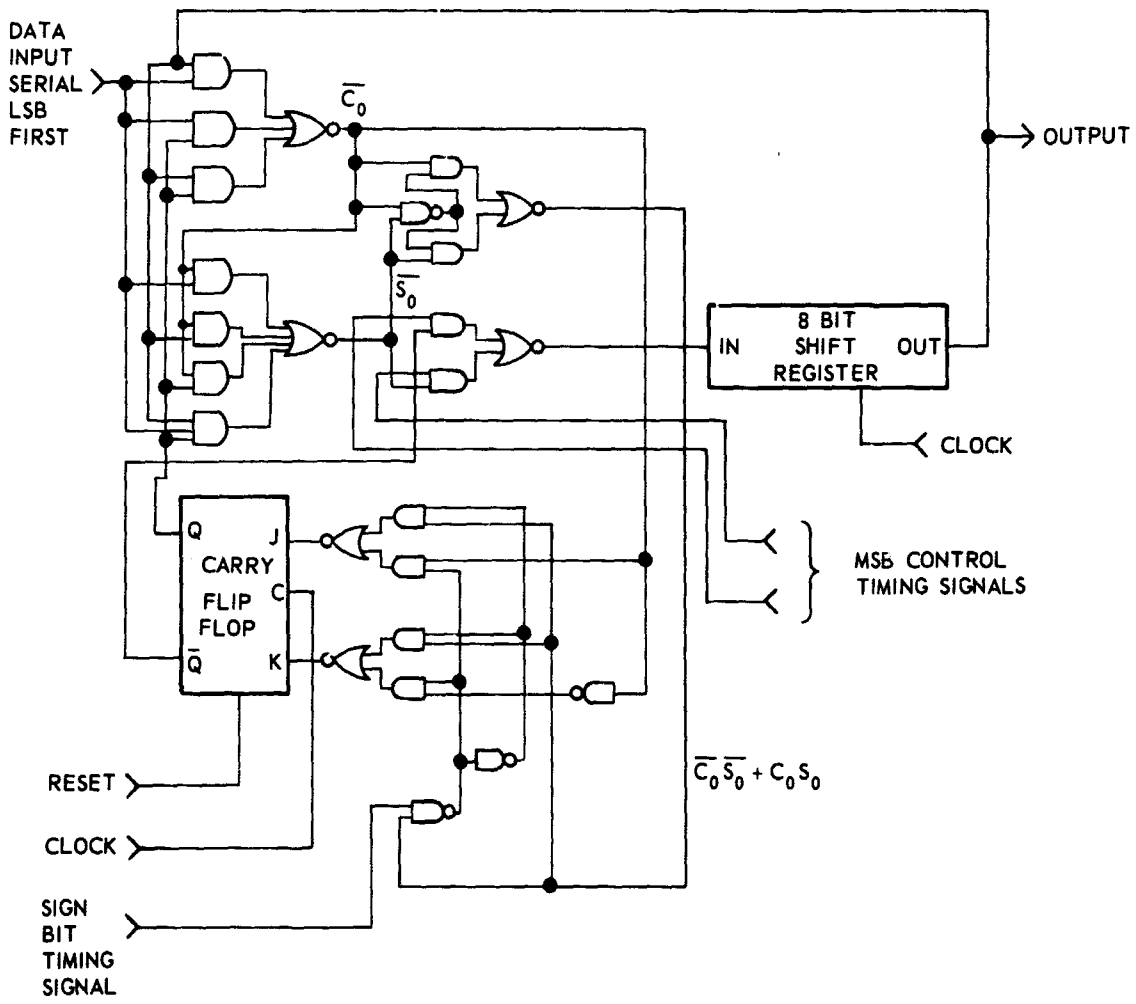
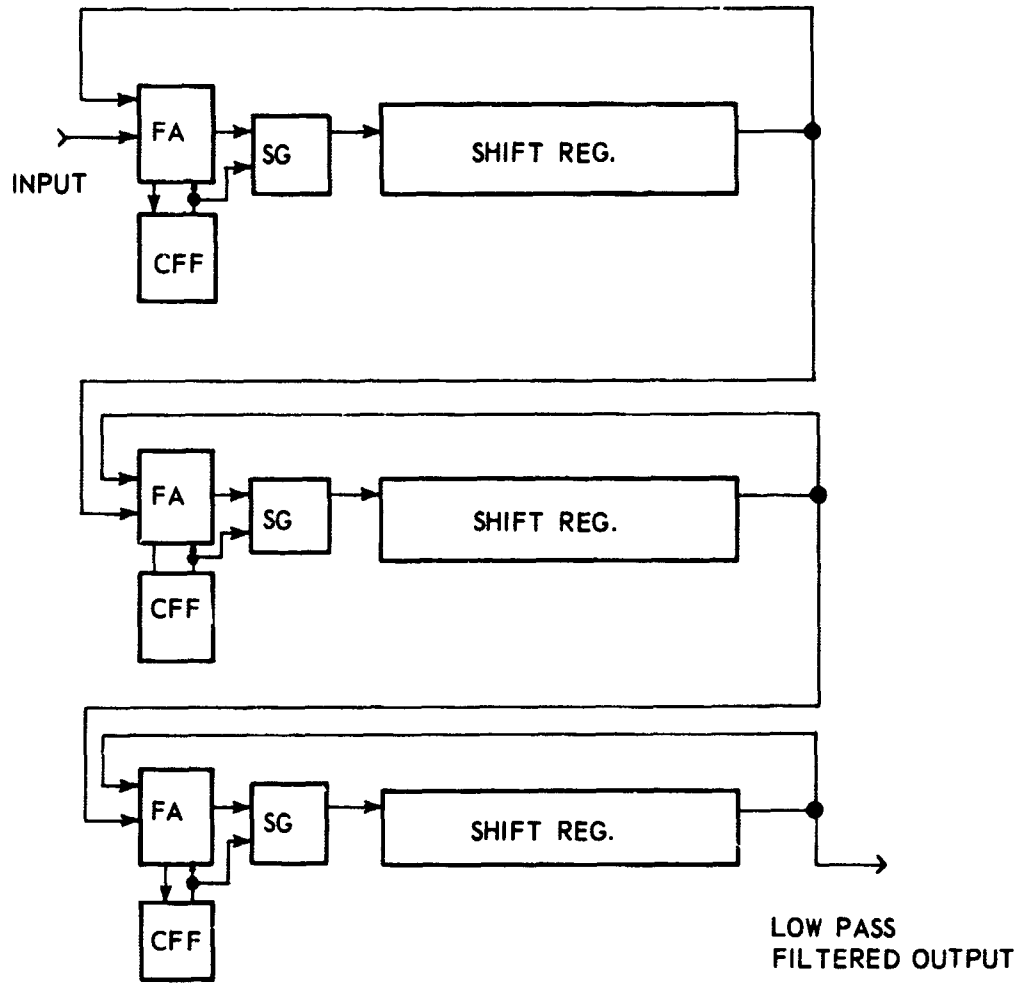


Figure 9. Logic Diagram – Single Stage of Low Pass Filter



FA: Full adder
CFF: Carry flip-flop
SG: Steering gates

Figure 10. Low Pass Filter

c. One flip-flop for the serial carry

d. Gating for the MSB.

Input to the filter stage is the serial incoming data which comes in LSB first. When the data is positive it is in normal form with the MSB a zero; when negative it is in two's complement form with the MSB a one. The incoming data has a total of 8 bits with the MSB always denoting sign.

The operation of the filter stage adds the LSB of the contents of the register to the LSB of the incoming data and the summing operation continues in serial mode until the LSB of the sum is in the last position of the register. At this time an extra clock pulse goes to the register dropping off the LSB thus implementing a divide by two operation, i.e.,

let E_d = the data word

E_r = the contents of the register

t = time

τ = a sample period

then

$$E_{r(t)} = \frac{E_{d(t)} + E_{r(t-\tau)}}{2} \tag{1}$$

From this it can be seen that the contents of the register must be smaller than the larger of the two values $E_{d(t)}$ and $E_{r(t-\tau)}$ unless both are the same value, in which case: $E_{r(t)} = E_{d(t)} = E_{r(t-\tau)}$. It is not possible for $E_{r(t)}$ to be larger than the larger of the two so that if neither $E_{r(t-\tau)}$ nor $E_{d(t)}$ is over eight bits then $E_{r(t)}$ cannot be over 8 bits, hence it is impossible for the filter stage to saturate or overflow. The state of the carry flip-flop is not the true carry after the 8th clock pulse. After the 8th clock pulse and prior to the 9th (divide by 2) clock pulse, the flip-flop serves as temporary storage for the sign bit.

The information needed to determine the sign bit is contained in the 8th Sum Out bit position and the 7th and 8th Carry Out bit positions. This information then determines the state of the carry flip flop after the 8th clock pulse. The 9th clock pulse then transfers the carry flip flop contents into the MSB of the shift register. The case of the carry flip flop having a one in it, which is routed to the MSB bit position of the register during the divide by two operation, occurs when the contents of the register are to be negative and in two's complement form.

Consider the overflow and saturation for the worst possible case

let: $E_{(t-n\tau)}$ = the data word at time $t - n\tau$

$E_{r(t)}$ = the contents of the register at time t

n = the number of sample periods

For one sample period:

$$E_{r(t)} = \frac{1}{2}\left(E_{(t)} + E_{r(t-\tau)}\right) \tag{2}$$

For two sample periods:

$$E_{r(t)} = \frac{1}{2}\left[E_{(t)} + \tfrac{1}{2}\left(E_{(t-\tau)} + E_{r(t-2\tau)}\right)\right] \tag{3}$$

For three sample periods:

$$E_{r(t)} = \frac{1}{2}\left\{E_{(t)} + \frac{1}{2}\left[E_{r(t-\tau)} + \frac{1}{2}\left(E_{r(t-2\tau)} + E_{r(t-3\tau)}\right)\right]\right\} \tag{4}$$

For n sample periods:

$$E_{r(t)} = \frac{E_{(t)}}{2} + \frac{E_{(t-\tau)}}{4} + \frac{E_{(t-2\tau)}}{8}\,\frac{E_{(t-3)}}{16} + \cdots + \frac{E_{(t-n\tau)}}{2^{n+1}} \tag{5}$$

$$E_{r(\ )} = \frac{E_{(t)}}{2} + \sum_{n=1}^{n=\infty} \frac{E_{(t-n\tau)}}{2^{n+1}} = \sum_{n=1}^{n=\infty} \frac{E_{[t-(n-1)\tau]}}{2^{n}} \tag{6}$$

let $E_{[t-(n-1)\tau]}$ be a maximum of 1 for all values of n,

$$E_{1(t)} = \frac{1}{2} + \frac{1}{4} + \frac{1}{8} + \frac{1}{16} + \frac{1}{32} + \frac{1}{64} + \cdots + \frac{1}{2^{n}} \tag{7}$$

$$E_{[t-(n-1)\tau]} = 1 \quad \lim_{n\to} \sum_{n=1}^{n} \frac{E_{(t-n\tau+1)}}{2^n} = 1 \qquad (8)$$

Hence the contents of the register cannot exceed the maximum value of the input data word.

Amplitude and Phase Transfer Functions of the Low Pass Digital Filter

Figure 9 is one stage of the low pass filter with the inputs in serial LSB first form.

$E_{i(t)}$ is the input data word

$E_{o(t)}$ is the output data word

τ is a sample period.

One stage of the filter, in terms of inputs and outputs is described in Equation (9).

$$E_{o(t)} = \frac{E_{i(t)} + E_{o(t-\tau)}}{2} \qquad (9)$$

Rewriting the equation in Z transform notation where:

$$Z^{-k} \equiv (t-k\tau) \qquad (10)$$

$$E_o Z^{-0} = \frac{E_i Z^{-0} + E_o Z^{-1}}{2} \qquad (11)$$

$$E_o = \frac{E_i + E_o Z^{-1}}{2} \qquad (12)$$

$$2E_o - E_o Z^{-1} = E_i \tag{13}$$

$$\frac{E_o}{E_i}(z) = \frac{1}{2 - Z^{-1}} \tag{14}$$

where

$$\frac{E_o}{E_i}(z) = \frac{E_o}{E_i}$$

as a function of Z

$$Z^{-k} \equiv e^{-ks\tau} \tag{15}$$

$$\frac{E_o}{E_i}(s) = \frac{1}{2 - e^{-s\tau}} \tag{16}$$

where

$$\frac{E_o}{E_i}(s) = \frac{E_o}{E_i}$$

as a function of S

$$S \equiv j\omega \tag{17}$$

$$\frac{E_o}{E_i}(j\omega) = \frac{1}{2 - \cos\omega\tau + j \sin\omega\tau} \tag{18}$$

where

$$\frac{E_o}{E_i}(j\omega) = \frac{E_o}{E_i}$$

as a function of $j\omega$

$$\frac{E_o}{E_i}(j\omega) = \frac{2 - \cos \omega\tau}{5 - 4 \cos \omega\tau} - j \frac{\sin \omega\tau}{5 - 4 \cos \omega\tau} \tag{19}$$

where

$$\omega\tau = 2\pi f_1 \tau = 2\pi \frac{f_1}{f_2}$$

and f_1 = input signal frequency in cycles per unit time

f_2 = sampling frequency in samples per unit time

$$\frac{2\pi f_1}{f_2} = \frac{2\pi}{\frac{f_2}{f_1}} = \frac{2\pi}{\frac{\text{samples/unit time}}{\text{cycles /unit time}}}$$

$$= \frac{2\pi}{\text{samples/cycle}}$$

Amplitude transfer function per stage

$$\left|\frac{E_o}{E_i}\right| = \left|\sqrt{(\text{Reals})^2 + (\text{imag})^2}\right| \tag{20}$$

$$\left|\frac{E_o}{E_i}\right| = \left|\sqrt{\frac{1}{5 - 4\cos\frac{2\pi}{\text{samples/cycle}}}}\right| \qquad (21)$$

Phase shift transfer function per stage

$$\phi = \tan^{-1}\left[\frac{-\sin\frac{2\pi}{\text{samples/cycle}}}{2 - \cos\frac{2\pi}{\text{samples/cycle}}}\right] \qquad (22)$$

Figure 11 shows the curves for the transfer functions and Table 3 shows the calculated values for the curves.

Table 3

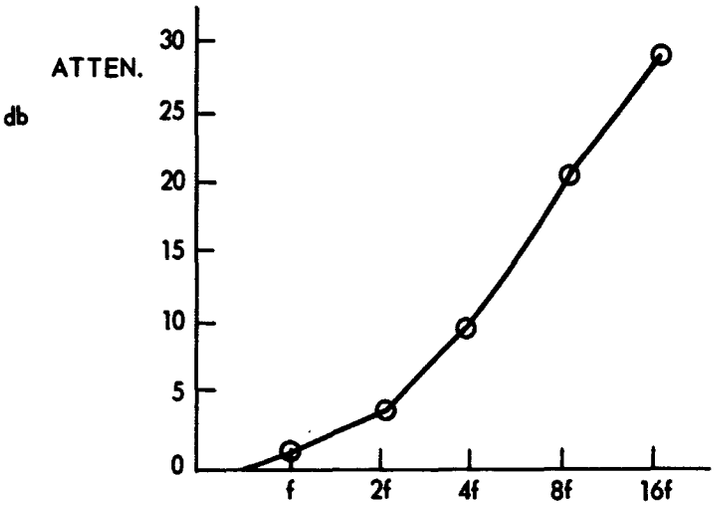
Calculated Values of Attenuation and Phase Shift for the Low Pass Filter, Calculated from Equations (21) and (22)

Samples Per Spin	Atten. 1 Stage	Atten. 3 Stages	Phase Shift 1 Stage	Phase Shift 3 Stages	Atten. 3 Stages db
32	.96	.88	10.6	31.8	1
16	.87	.68	19.7	59.1	3.5
8	.67	.305	28.6	86	10
4	.445	.088	—	—	21
2	.333	.0371	—	—	29

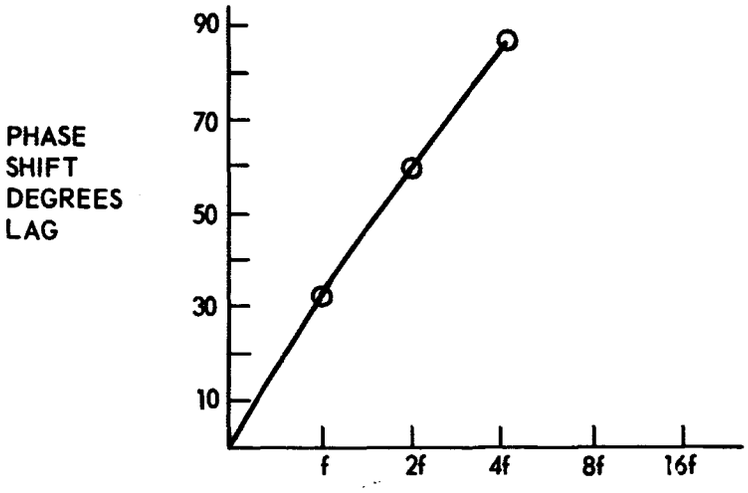
High Pass Filter Transfer Function

Let: E_o = output of the high pass filter

f = spin frequency with 32 samples/spin



Attenuation vs frequency, 3 stage low pass filter



Phase shift vs frequency curve

Figure 11. Low Pass Filter Transfer Characteristics

E_i = input to the high pass filter

k = multiplication constant (1.125)

$\left\{\frac{E_{o(\ )}}{E_{i\ LP}}\right\}^3$ = transfer function of one stage of the low pass filter cubed to get the transfer function of 3 stages

The equation for the high pass filter is

$$E_o = E_{i(t-3\tau)} - E_i k \left\{\frac{E_{o(t)}}{E_{i\ LP}}\right\}^3 \tag{23}$$

$$\frac{E_{o(z)}}{E_i} = z^{-3} - k \left\{\frac{E_{o(z)}}{E_{i\ LP}}\right\}^3 \tag{24}$$

$$\frac{E_{o(s)}}{E_i} = e^{-3s\tau} - k \left\{\frac{E_{o(s)}}{E_{i\ LP}}\right\}^3 \tag{25}$$

$$\frac{E_{o(j\omega)}}{E_i} = e^{-3j\omega} - k \left\{\frac{E_{o(j\omega)}}{E_{i\ LP}}\right\}^3 \tag{26}$$

$$\frac{E_{o(j\omega)}}{E_i} = d - jc - k\ \{a - jb\}^3 \tag{27}$$

where:

$$d = \cos\frac{6\pi}{n}$$

$$c = \sin\frac{6\pi}{n}$$

$$a = \frac{2 - \cos\frac{2\pi}{n}}{5 - 4\cos\frac{2\pi}{n}} \quad \text{(from low pass filter equation)}$$

$$b = \frac{\sin\frac{2\pi}{n}}{5 - 4\cos\frac{2\pi}{n}} \quad \text{(from low pass filter equation)}$$

n = samples per cycle

High pass filter transfer function:

$$\frac{E_{o(j\omega)}}{E_i} = \cos\frac{6\pi}{n} - 1.125\left[\left(\frac{2-\cos\frac{2\pi}{n}}{5-4\cos\frac{2\pi}{n}}\right)^3 - 3\left(\frac{2-\cos\frac{2\pi}{n}}{5-4\cos\frac{2\pi}{n}}\right)\left(\frac{\sin\frac{2\pi}{n}}{5-4\cos\frac{2\pi}{n}}\right)^2\right]$$

$$- j\left[\sin\frac{6\pi}{n} - 1.125\left\{3\left(\frac{2-\cos\frac{2\pi}{n}}{5-4\cos\frac{2\pi}{n}}\right)^2\left(\frac{\sin\frac{2\pi}{n}}{5-4\cos\frac{2\pi}{n}}\right) - \left(\frac{\sin\frac{2\pi}{n}}{5-4\cos\frac{2\pi}{n}}\right)^3\right\}\right] \quad (28)$$

Figure 12 is a curve of attenuation vs multiples of spin frequency, and Table 4 is calculated values for the curve of Figure 12 and calculated from Equation (28).

The total delay of the incoming signal, prior to comparison to the low pass filtered signal is 7 sample periods. Three of the delays in the low pass filter are interstage delays and the fourth is the delay due to the multiplication operation. Since these delays (4 sample periods) are accounted for in four of the seven incoming data delays the remaining 3 delays of the incoming data are the only delays shown in the preceding mathematics. These three delays of the incoming data approximately equal the low pass filter phase shift of the spin frequency.

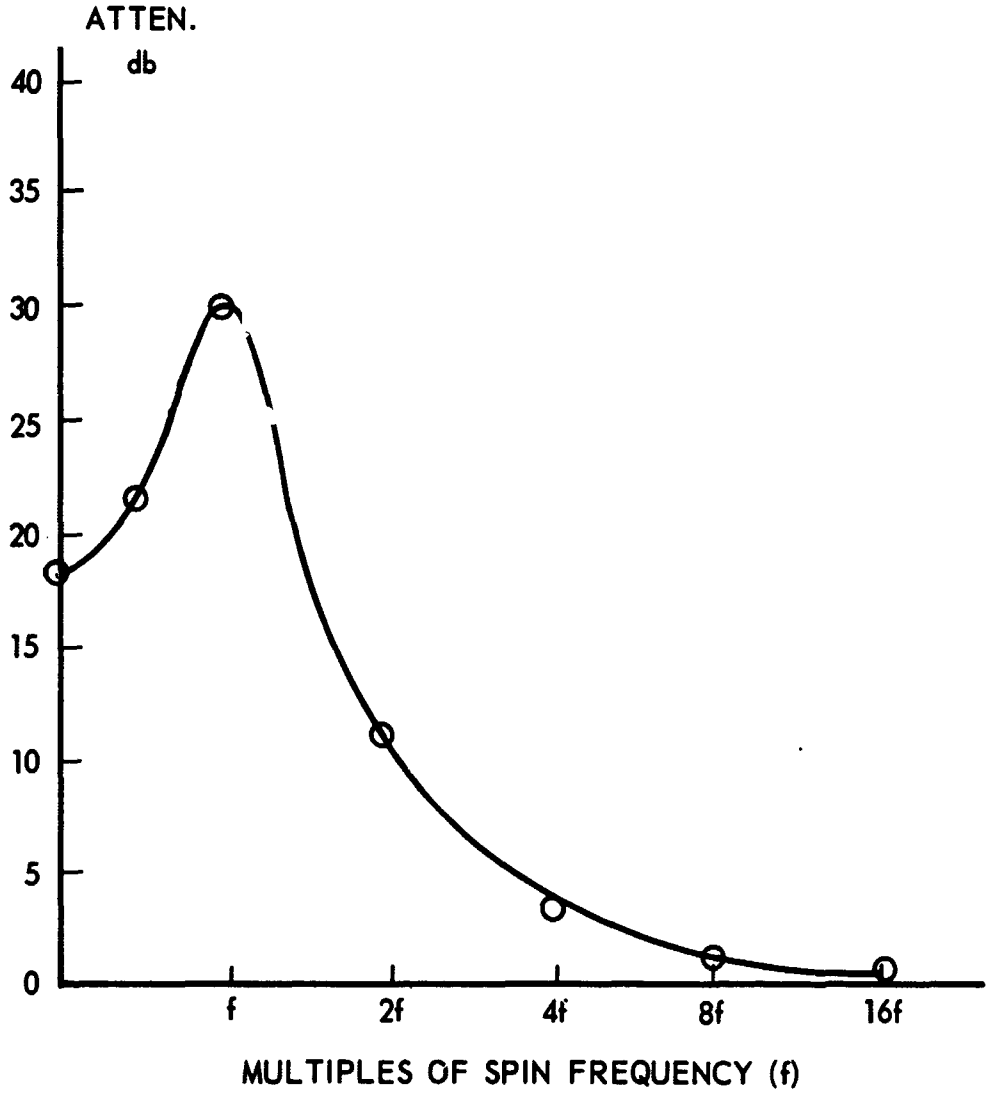


Figure 12. Calculated Values of Attenuation vs Multiples of Spin Frequency From Equation 28

Table 4

Calculated Values of Attenuation vs Multiples of the Spin Frequency, Calculated from Equation (28)

Multiples of Spin Frequency	Attenuation db	n Samples Per Cycle
0	18	∞
1/2	21	64
1	30	32
2	11	16
4	3.6	8
8	0.9	4
16	0.3	2

Multiplication

A multiplication is performed in the digital filter and is the multiplication of a variable times a constant. The multiplication is performed to restore the filtered spin frequency signal to its original amplitude after having been attenuated by the low pass filtering action. The attenuation factor (88%) as well as the phase shift value (3 sample periods) is shown in Figure 11 and Table 3 which were calculated from the low pass filter amplitude and phase transfer functions.

Hence the filtered output must be multiplied by a constant (k) which can be determined by:

$$k = \frac{1}{\sin(w\tau + 3\tau)} = \frac{1}{.88} = 1.136$$

For an approximation of k as 1.125 the multiplication is readily implemented by the block diagram shown in Figure 13.

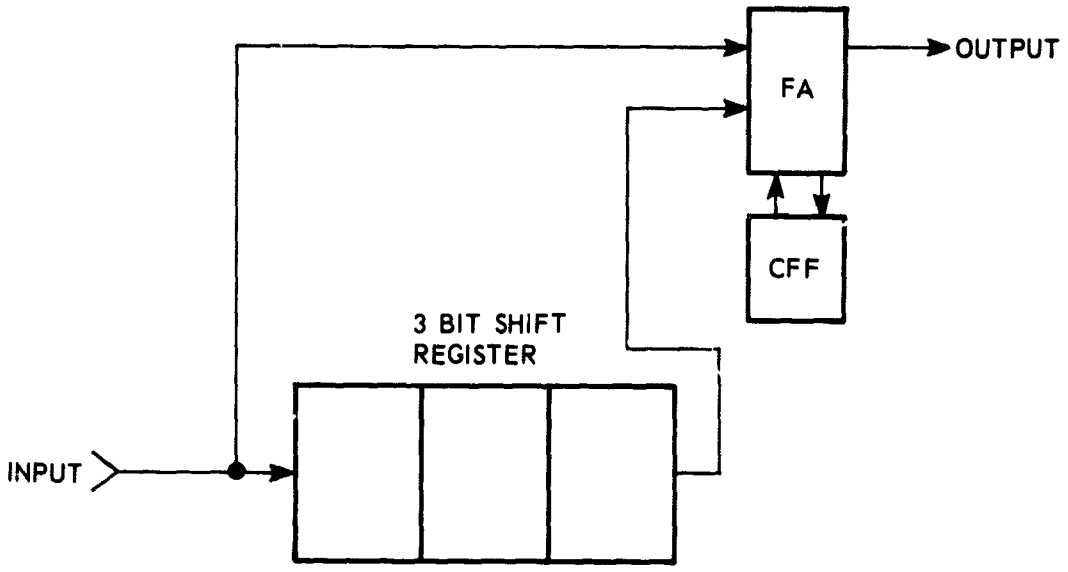


Figure 13. Multiplication By A Constant

Addition and Subtraction

All addition and subtraction is accomplished serially. The serial addition is implemented as shown in Figure 14.

The subtraction of input B from input A using the full adder is performed by two's complementing input B. This is most readily achieved by one's complementing input B and adding one to it by setting a one in the carry flip flop prior to subtraction.

When (1) is added to the one's complement of a number the sum is the two's complement. Setting the carry input to one is equivalent to adding one to the one's complemented input B.

SUMMARY

The digital filter and adaptive delta modulator have been built with commercial quality high power TTL. The feasibility model has been tested and found to perform as anticipated. The design is being converted to flight configuration using low power TTL.

The flight version of the unit will have two filters for the X and Y axes and four adaptive delta modulators. Each axis (X, Y, Z) will have a delta modulator

for information higher than 2 times the spin frequency. In addition the Z axis will have an extra delta modulator for information at frequencies less than 2 times the spin frequency. This same low frequency information on the X and Y axis otherwise not available because of filtering will be recovered by taking four absolute samples per spin to be transmitted along with the filtered-delta modulated data.

In general, on IMP H and J the filtered and delta modulated data will be transmitted during the high bit rate (1600 BPS) telemetry mode only.

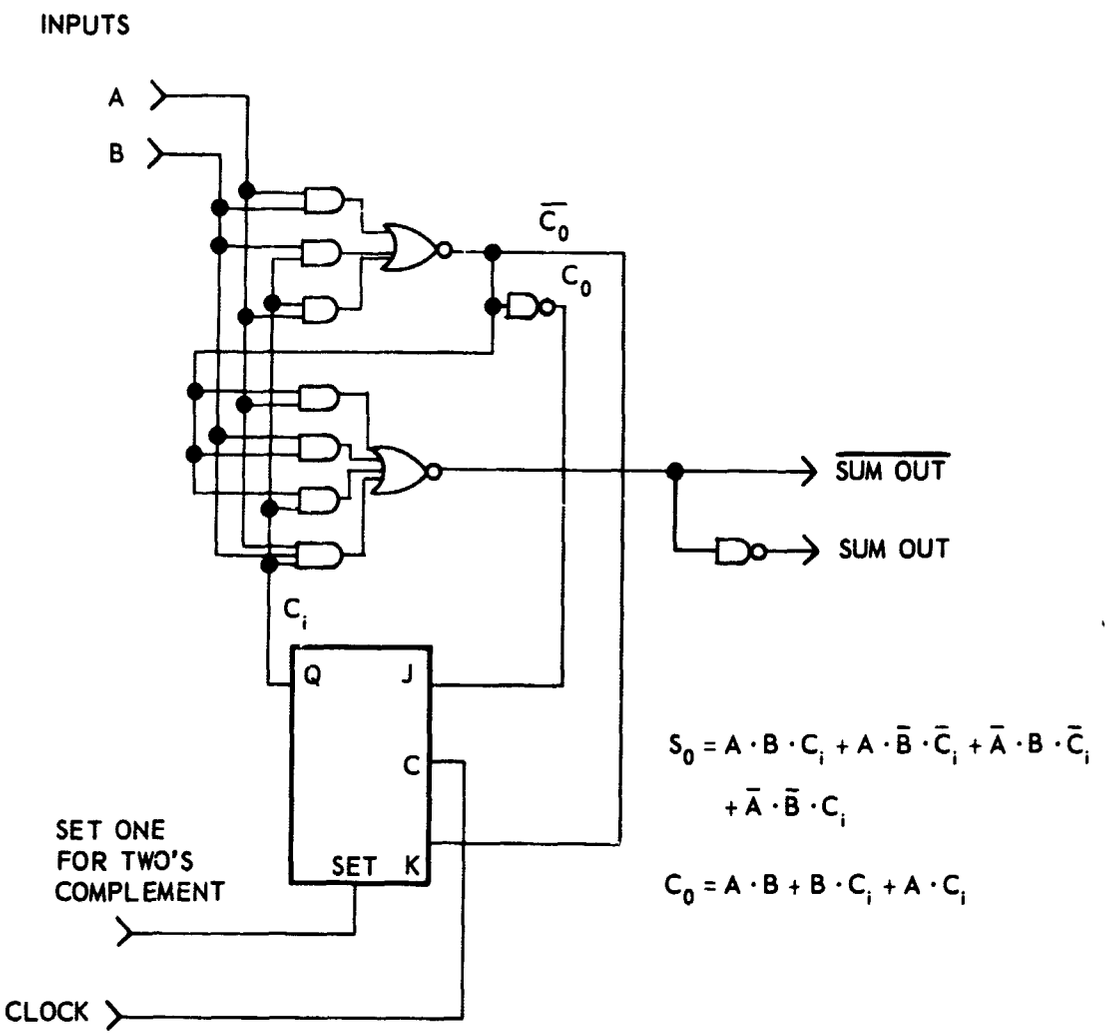


Figure 14. Addition and Subtraction With A Serial Full Adder

ACKNOWLEDGMENT

The writer is indebted to Messrs. Clell S. Scearce, David H. Schaefer and Dennis D. Seekins of Goddard Space Flight Center for their interest and suggestions in this endeavor.

REFERENCES

1. Cotton, R. V. (Philco Corp.), and R. L. Remm (USAF), and Strohmeyer (Philco Corp.), "Analysis of Delta Modulation Encoding Using Computer Simulation", Suppl. to IEEE Trans. on Aerospace and Electronic Systems (Vol. AES.-2 No. 4, July 1966)

2. Albus, J. S. (NASA), Unpublished Communication.

3. Rader, C. M. and B. Gold, "Digital Filter Design Techniques in the Frequency Domain", Proc. of the IEEE (Vol. 55 No. 2, Feb. 1967)

4. Carney, R. (Martin Co.), "Design of a Digital Notch Filter with Tracking Requirements", IEEE Trans. on Aerospace and Electronic Systems, Dec. 1963

5. Tou, J. T., Digital and Sampled Data Control Systems (McGraw Hill Book Co., N.Y., 1959)

6. Breslow, D., "Digital Roads to Analog Functions", Electronic Design (Vol. 15, No. 18, Sept. 1967)

7. Breslow, D., "From Theories to Hardware", Electronic Design (Vol. 15, No. 18, Sept. 1967)

8. Senduk, G. T. and Prince, J. S., "Build Filters with MOS Chips", Electronic Design (Vol. 15, No. 18, Sept. 1967)

9. Moyer, C. V., A Digital Filter for On-Board Data Compaction of Satellite Experiment Magnetic Field Data. Masters Thesis, George Wash. Univ., June 1968

APPENDIX

One Bit Adaptive Delta Modulator

One bit adaptive delta modulators increase their increment size in a 1, 2, 4, 8 . . . . 2^{n-1} ratio when following a signal which is increasing or decreasing at a rapid rate. The limiting value of 2^{n-1} is set by one or more of the following:

1. Signal characteristics
2. Accuracy requirements
3. Hardware constraints.

Table 1A shows a ±1, ±2, ±4 adaptive delta modulator truth table. The one bit adaptive delta modulator defined by Table 1A always makes a unit step (±1) after "catching up" with the incoming signal.

Table 1A

One Bit Adaptive Delta Modulator Truth Table.

Increment Size	Present Decision at Time (t)	Past Decisions at Times	
		(t - 1)	(t - 2)
-4	0	0	0
-2	0	0	1
-1	0	1	0
-1	0	1	1
+1	1	0	0
+1	1	0	1
+2	1	1	0
+4	1	1	1

Suppression of spurious oscillations normally encountered in a one bit adaptive delta modulator, and which would occur in the adaptive delta modulator defined by Table 1A, can be implemented by delaying for one sample period the 2 unit step. Forcing the adaptive delta modulator to take two single unit steps of the same polarity, before taking a 2 unit step prevents oscillations.

Table 2A is a truth table defining the one bit adaptive delta modulator with this type oscillation suppression.

Table 2A

Truth Table for One Bit Adaptive Delta Modulation with Oscillation Suppression.

Increment Size	Present Decision at Time (t)	Past Decisions at Times		
		(t - 1)	(t - 2)	(t - 3)
-4	0	0	0	0
-2	0	0	0	1
-1	0	0	1	0
-1	0	0	1	1
-1	0	1	0	0
-1	0	1	0	1
-1	0	1	1	0
-1	0	1	1	1
+1	1	0	0	0
+1	1	0	0	1
+1	1	0	1	0
+1	1	,0	1	1
+1	1	1	0	0
+1	1	1	0	1
+2	1	1	1	0
+4	1	1	1	1

Figure 6 in the text shows oscillations which can occur without oscillation suppression. Figure 1A shows the same input and initial conditions for the one bit adaptive delta modulator with oscillation suppression.

An advantage of the one bit, over the two bit adaptive delta modulator is that filtering of quantization noise is easier in the one bit delta modulator due to its quantization noise being one octave above the highest recoverable frequency.

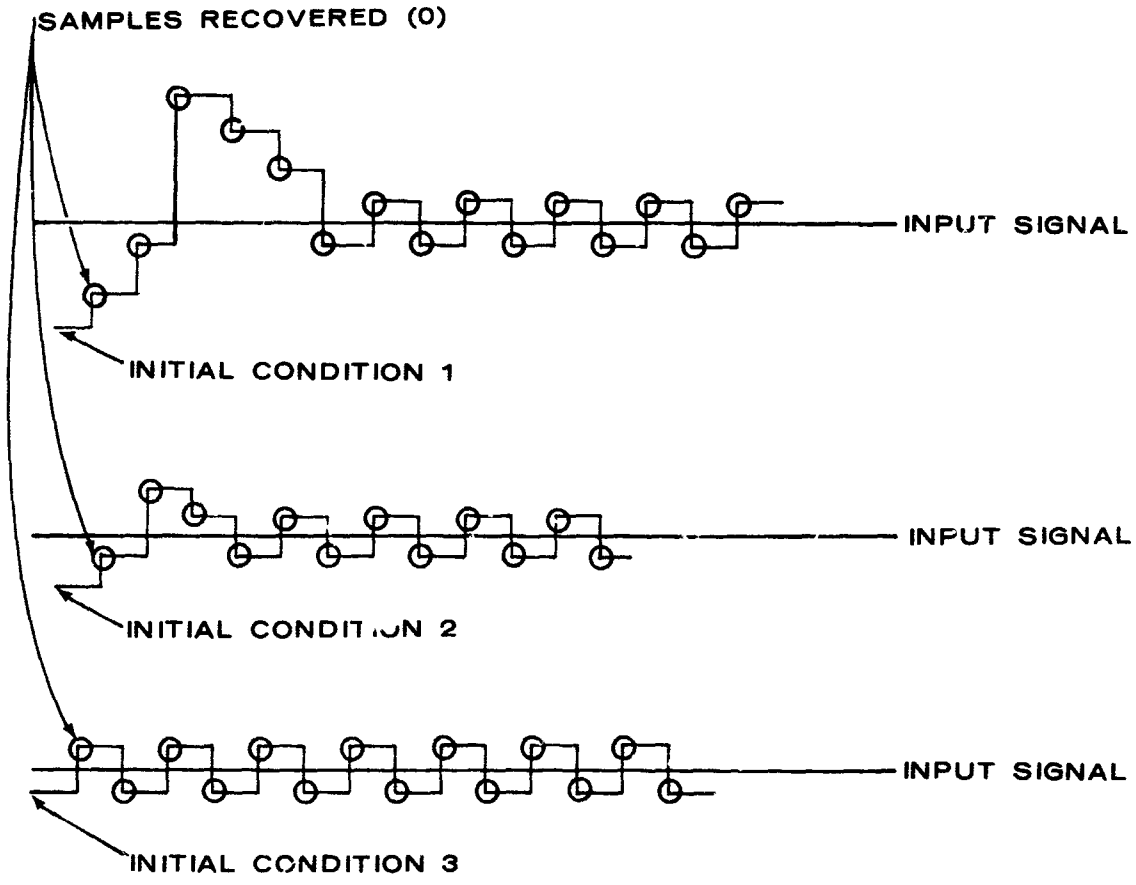


Figure 1A-One Bit Adaptive Delta Modulator with Oscillation Suppression.