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FINAL REPORT

FOR

PCM ENCODER SYSTEM

Submitted To

NATIONAL AERONAUTICS AND SPACE ADMINISTRATION

MANNED SPACECRAFT CENTER

HOUSTON, TEXAS

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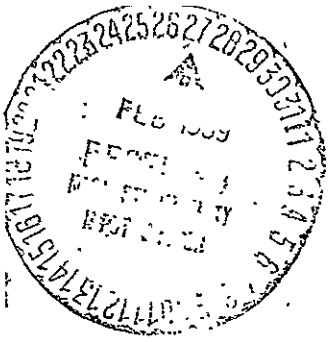

Submitted By

SPACE AND TACTICAL SYSTEMS CORPORATION

ONE GARFIELD CIRCLE

BURLINGTON, MASSACHUSETTS

JANUARY 31, 1969

55 pp.

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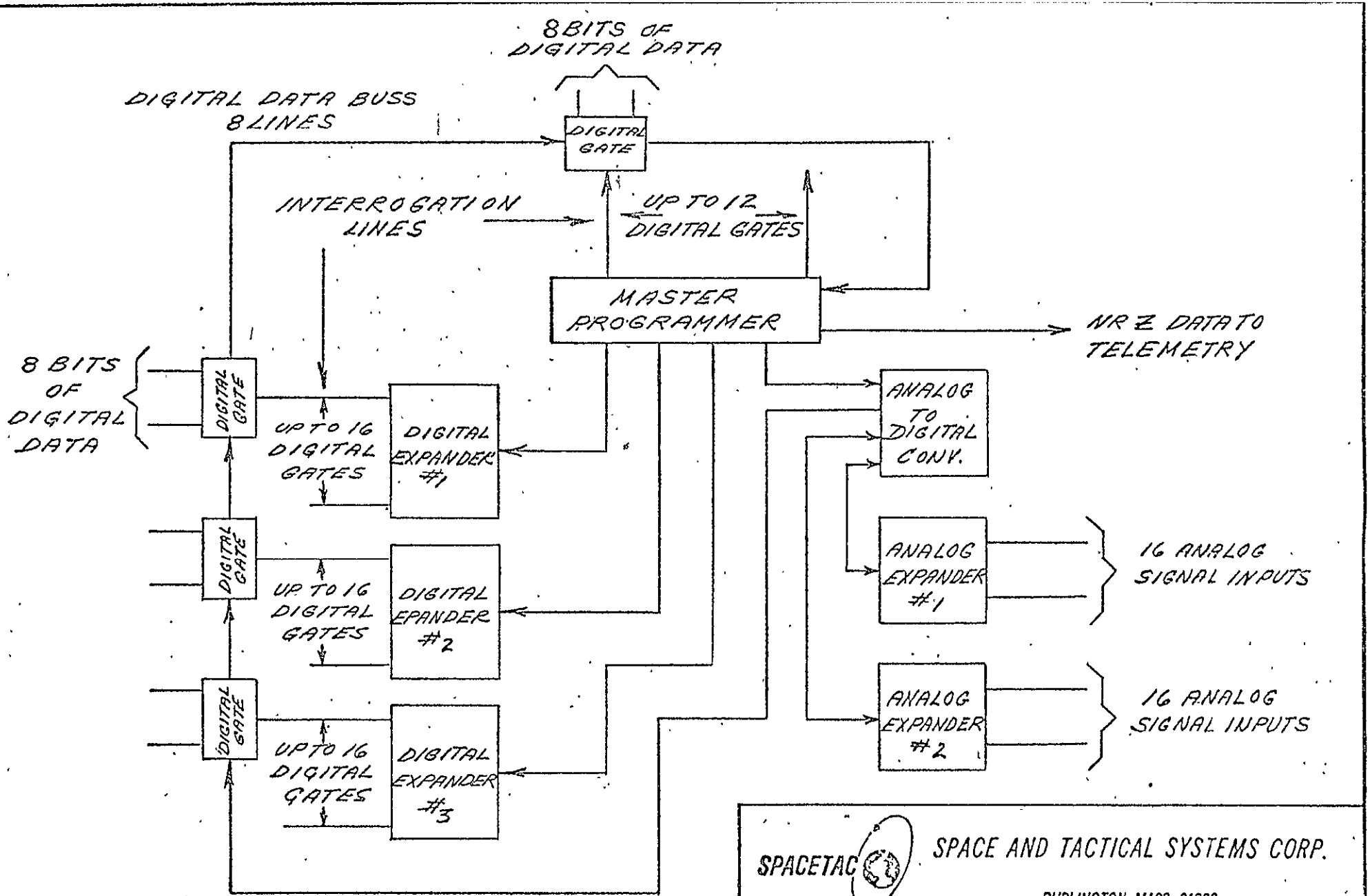
1.0 INTRODUCTION

The overall design philosophy for the PCM encoder system has been to provide a low-power, miniaturized, modular PCM encoder with a flexible frame format, frame size, and sample rate at the lowest possible cost without jeopardizing accuracy or reliability. The general total configuration of the system is shown in Figure 1.0 and discussed in greater detail in the following sections.



SPACETAC

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BURLINGTON, MASS. 01803

TITLE

MAXIMUM CONFIGURATION OF SYSTEM

SCALE	DWG NO. FIG. 1.0	REV

2.0 MASTER PROGRAMMER

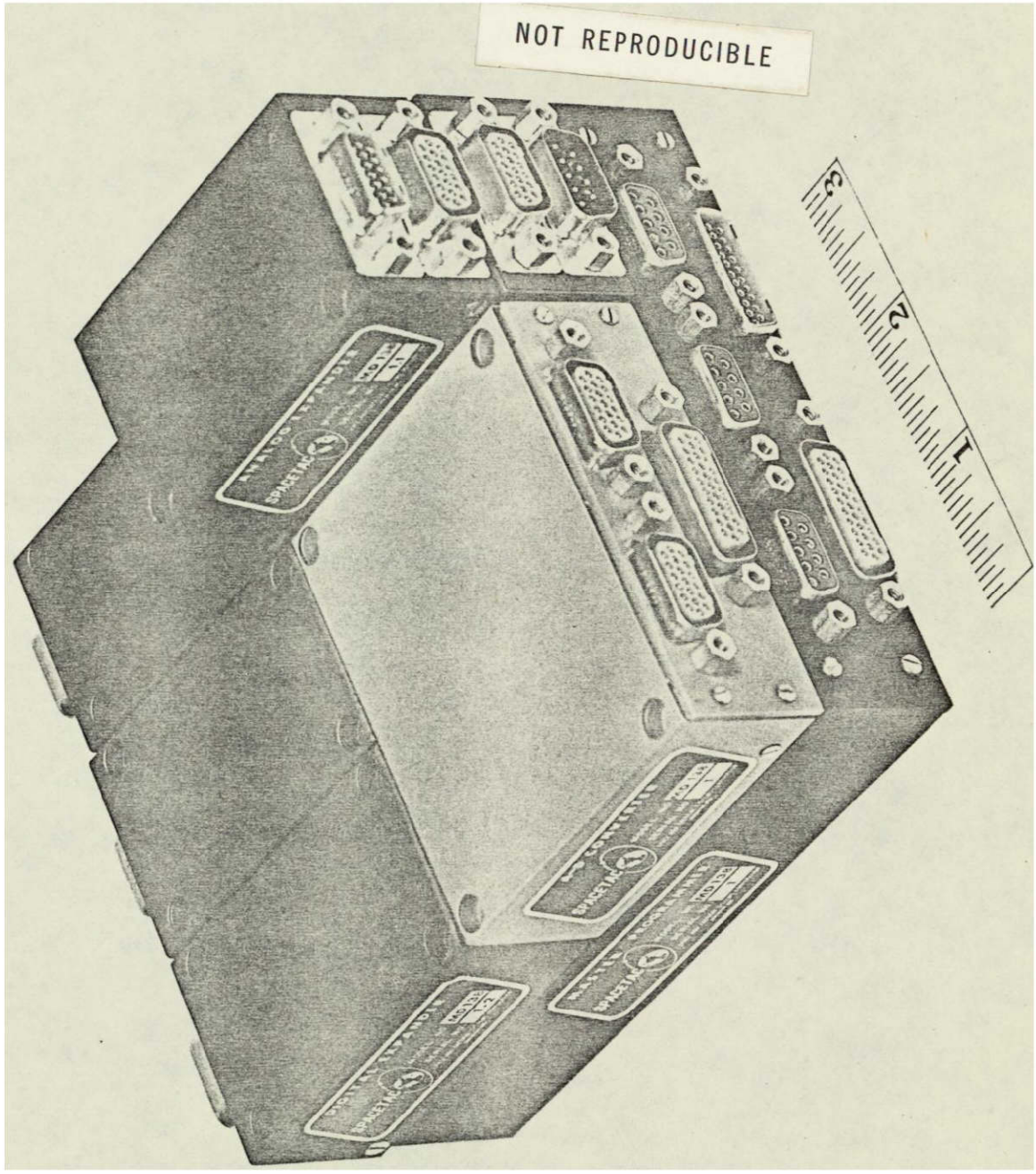
The Master Programmer is the basic building block of the modular encoder system. It is a small PCM encoder system in itself, and by adding the other types of building blocks described in the following sections, a very flexible and powerful data acquisition system can be obtained. The Master Programmer provides all necessary control functions to convert and time multiplex all incoming data into an NRZ serial bit stream that is capable of driving a transmitter.

The Master Programmer consists of three major sections: clock countdown, parallel-to-serial output register, and a 16-channel multiplexer. A logic diagram of the Master Programmer is shown in Figure D4107.

2.1 Clock Countdown

Timing for the Master Programmer is derived from a 256 KHz crystal-controlled oscillator. A 256 KHz crystal has been selected because it is the nearest binary frequency to the required maximum operating frequency of 64 KHz, where the size and operating parameters of the crystal are suitable. Two stages of countdown provide 64 KHz timing signals for the system. An additional four stages of countdown can be added, one stage at a time, to the countdown chain so that there are a total of five selectable clock frequencies available (64 KHz, 32 KHz, 16 KHz, 8 KHz, and 4 KHz).

The countdown chain is designed so that any one of the five clock frequencies can be chosen by adding a small jumper to terminals on the printed circuit motherboard which contains the modules that make up the Master Programmer.



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The countdown chain is designed so that any one of the five clock frequencies can be chosen by adding a small jumper to terminals on the printed circuit motherboard which contains the modules that make up the Master Programmer.

The clock is also used to generate the shift pulses used throughout the system and is, therefore, the bit rate (BPS) of the overall system. It will be assumed, for the remainder of this discussion, that the bit rate used will be the maximum specified - 64 K BPS.

Following the clock there is a three-stage counter that provides timing for an eight-bit-per-word format. The output of the bit counter is used to drive the word counter. Since the format calls for eight words per line, a three-stage counter is used to generate word timing signals. The output of the word counter is used to drive a psuedo variable modulus line counter.

The line counter modulus will be determined by whatever format has been chosen. That is, if the frame consists of only two lines, a modulo two counter is selected. If the format selected consists of eight lines, then the line counter will be a three-stage binary counter (modulo eight).

Timing and control signals from the word counter and the line counter, shown in Figure B4120, are brought out to connectors through buffers to operate up to three digital expander subsystems that will increase the format from eight words by two lines to eight words by eight lines.

2.2 Parallel-to-Serial Output Register

The output register is an eight-bit shift register, whose function is to convert incoming parallel data to a serial data stream with the least significant bit first. The output of the shift register drives a deglitching flip flop, whose buffered output is the NRZ data stream to the telemetry transmitter. A deglitching

flip flop is necessary because data is loaded into the register between two shift pulses, and the last bit shifted out of the register may be split due to the register's being filled with zeros. The register shifts zeros into the most significant bit end of the register with each shift pulse so that when data is loaded into the register, it can be done using a one's transfer method, thereby saving hardware.

A set of transfer gates will accept eight bits of data in parallel and perform the one's transfer of data once each word time, coincident with load pulses.

Pulse generators that are controlled by countdown timing provide the shift and load pulses required for proper operation of the output-shift register.

2.3 Multiplexer, 16-Channel

The Master Programmer will itself provide for a minimum frame format of two lines, each of which is eight words. The telemetry format, in its maximum configuration, is shown in Figure 2.3. The first level of the time division multiplexing operation is performed by decoding the states of the word counter such that one line out of sixteen is enabled for each successive word. The second level of multiplexing groups the enable output lines into the required format. A blanking signal is applied to the control logic to decrease power consumption in the system and to eliminate switching transients.

The outputs of the multiplexer are buffered by line drivers, which supply positive levels to the interrogation lines. The interrogation line will enable an eight-bit digital gate, and the experiment data associated with that gate will appear on the digital data bus.

LINE \ WORD	0	1	2	3	4	5	6	7	
0	0	1	2	3	4	5	6	7	MASTER PROGRAMMER
1	8	9	10	11	12	13	14	15	
2	16	17	18	19	20	21	22	23	DIGITAL EXPANDER 1
3	24	25	26	27	28	29	30	31	
4	32	33	34	35	36	37	38	39	DIGITAL EXPANDER 2
5	40	41	42	43	44	45	46	47	
6	48	49	50	51	52	53	54	55	DIGITAL EXPANDER 3
7	56	57	58	59	60	61	62	63	

RECOMMENDED ALLOTMENT OF DATA CHANNELS

WORDS 0, 1, 2 MAIN FRAME SYNC (24 BITS)
WORD 3 SUB COM. SYNC.
WORD 7 32 CHANNELS SUBCOMMUTATED ANALOG DATA
WORDS 15, 23, 31 FRAME RATE ANALOG DATA.
ALL REMAINING CHANNELS FOR DIGITAL DATA

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TITLE: FRAME FORMAT

SCALE | DWG NO. FIG 2.3 | REV

Control logic for supplying timing levels to format expanding building blocks is derived from the variable modulus line counter, the blanking circuitry, and the word counter. All output levels for control timing functions are appropriately buffered to assure reliable operation.

As set forth in the specifications, up to four of the sixteen data channels provided by the Master Programmer multiplexer can be used to insert eight-bit sync words into the data stream. The selection of a particular sync code is flexible and can be changed easily by either connecting the output of the sync gate to the digital data bus or not connecting it. The interrogation level will place the desired sync pattern on the digital data bus so it can be transferred into the output register.

3.0 DIGITAL EXPANDER

The Digital Expander subsystem is a building block that allows a two-line expansion of the frame format. It expands the digital input capabilities of the system by sixteen eight-bit words. It is designed so that it may be connected directly to the Master Programmer through a connector.

The Digital Expander consists of input buffering circuits, decoding logic, and line drivers. A logic diagram of the Digital Expander is shown in Figure 4078. The input buffers accept timing and control signals from the Master Programmer and re-establish the voltage levels for proper and reliable operation of the sub-system. The decoding logic is done with modules that accept inputs from two flip flops (there are four possible states) and enable each of the four output lines, one at a time in sequence. Two levels of decoding are necessary to perform the time division multiplexing of sixteen channels. The first level of decoding performs the finest time division of sequencing each of the output lines. The second level of decoding controls the actual format in that it divides the sixteen channels into two eight-word lines. The line drivers accept the multiplexed signals from the decoding modules and provide the interrogation levels used to enable the digital gates. With a 64 K BPS rate, the interrogation time will be 125 μs. The blanking circuit discussed in the Master Programmer section will decrease the interrogation time to 62.5 microseconds. The blanking of the interrogation signal is not necessary, but it will serve to reduce overall power consumption and separate each channel in time.

Timing waveforms for the Digital Expander are shown in Figure B4123.

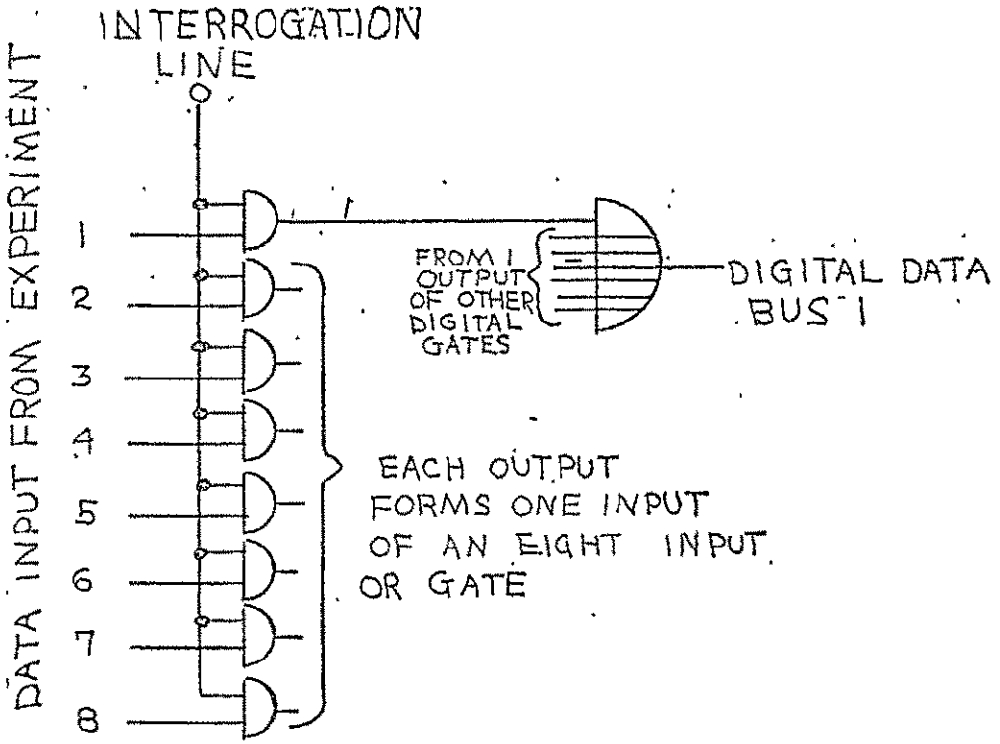
4.0 DIGITAL GATE

The digital gate module accepts up to eight bits of digital data in parallel and transfers this digital data to the digital data bus when enabled by an interrogation signal. Since this module may be an integral part of an experiment, the exact packaging configuration is flexible. The SPACETAC digital gate module size is 1.6" x 0.6" x 0.1". The design is that of a passive circuit which does not require external power.

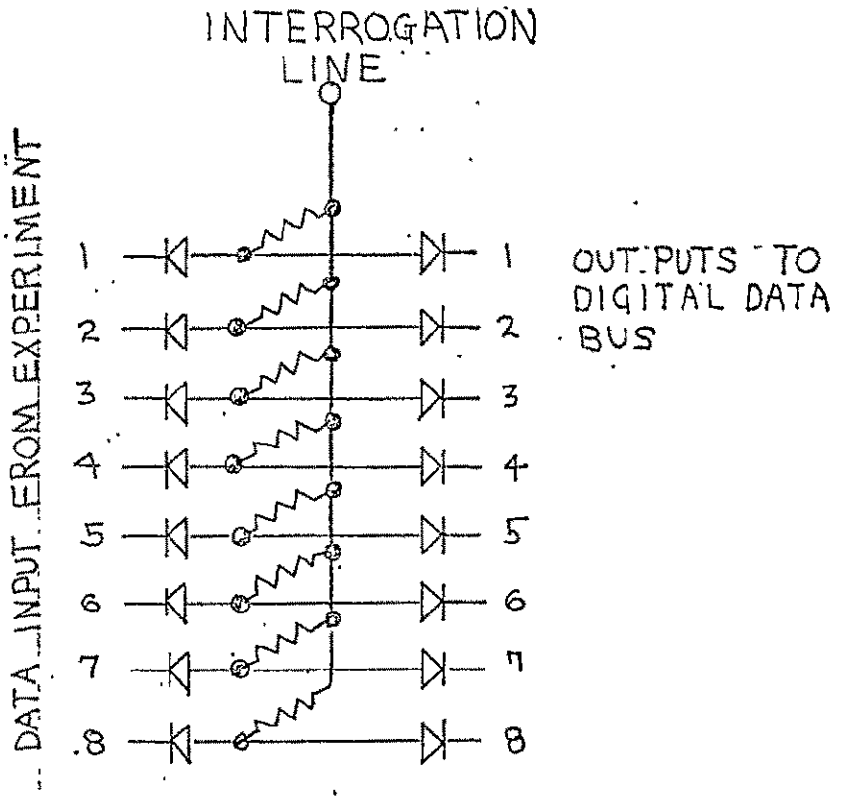
Input levels of greater than +3 volts for a logic one and less than +0.5 volts for a logic zero will be transferred to the digital data bus by the interrogation signal. The interrogate signal will be a level +6.0 volts in amplitude and 62.5μs in duration. The interrogate line forms one input of a two-input AND gate - the other input being the digital data signal. The output of each AND forms one input of a multiple-input OR, whose output is connected to one of the eight digital data bus lines. Figure 4.0 shows the logic and schematic of the digital gate module. The input impedance of the digital gate is 20 K ohms.

The number of digital gate modules for the maximum format configuration would be 64, less the number of sync words and analog channels used.

LOGIC



SCHEMATIC

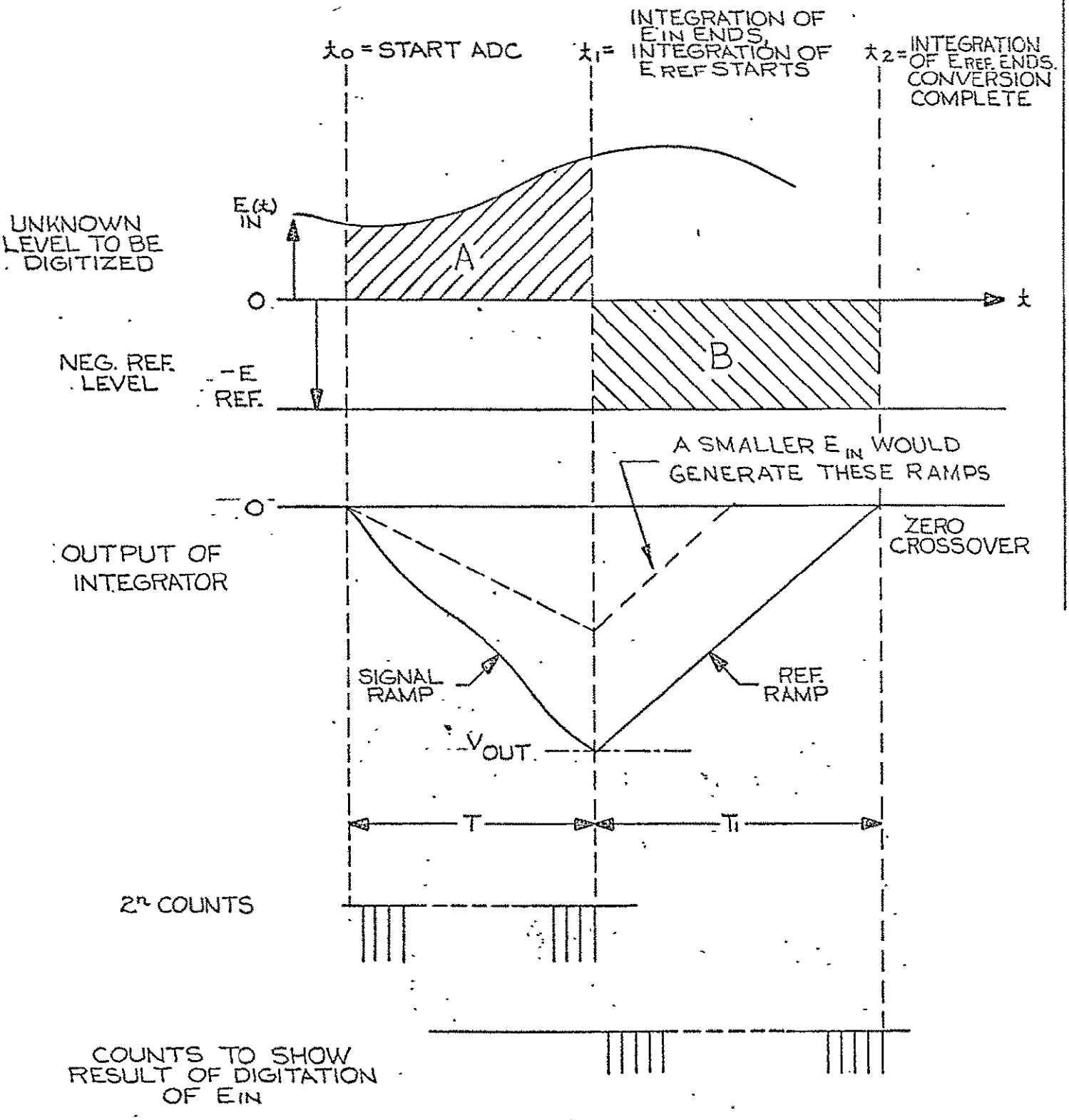


SPACETAC — SPACE AND TACTICAL SYSTEMS CORP. BURLINGTON, MASS. 01803		
TITLE: DIGITAL GATE		
SCALE	DWG NO. FIG 4.0	REV

5.0 ANALOG TO DIGITAL CONVERTER

The 8-bit ADC is a compact unit especially suited for space applications, such as satellites, rockets, or balloons, where reliable performance is required together with low weight and low power dissipation. Because of the dual ramp method of conversion, the ADC is very insensitive to instantaneous noise which may appear on the signal line as pickup from digital circuits, etc. For this reason this unit is a natural for housekeeping applications, where signal lines travel great lengths thru the spacecraft in a noisy environment. The ADC is used with an analog multiplexer unit which has a total input capacity expandable to 35 channels.

The analog-to-digital converter will operate on the voltage-to-time principle in a double integrating ramp configuration. In this configuration the input signal amplitude is changed to a time interval as an intermediate step in obtaining the digital value. During this interval, pulses are counted such that the total pulse count corresponds to the unknown voltage. As shown in Figure 5.0, the input signal is first integrated for a fixed time interval, as denoted by T. This time interval is determined by counting clock pulses from a gated clock source. The integrated voltage at the end of this interval is proportional to the input signal averaged over the integration time. A reference of the opposite polarity to the input signal is then integrated for the time it takes to reduce the integrated voltage to zero, its initial value. During this time the same clock source for integrating the input signal is used to count up to a number which is proportional to the averaged input signal. The advantage of this dual ramp technique is that the overall conversion linearity



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TITLE

BASIC OPERATION
OF DUAL RAMP CONVERTER

SCALE	DWG NO.	REV
#	FIG. 5	

D.L.F. 12-3-68

and accuracy is independent of the integrator's time constant, and precision resistors and capacitors with low temperature coefficients aren't required. Since the same clock source is used for measuring both the first and second integration intervals, a precision clock is also unnecessary. Noise is also minimized because the input signal is integrated, and the actual conversion occurs when the input signal is not connected to the converter.

Logic diagrams of the ADC are shown in Figures B4136 and B4175. A timing diagram is shown in Figure B4209. There is protection for input over-voltage such that the counter will not cycle more than once during the conversion process. The digital conversion is then available for the interrogate lines to strobe out the binary number in the register into the digital data bus and format it within the telemetry frame. The conversion time for the entire analog-to-digital conversion process will be less than one millisecond. However, since the telemetry format may be operating at a reasonably high bit rate, the user of the encoder system must be careful in the selection of analog-to-digital words in the frame format and the rate at which he requires an analog-to-digital conversion, the limitation being that conversions of less than a millisecond are not valid.

6.0 ANALOG EXPANDER

The analog expanders are essentially an extension of the four channel commutator in the ADC. By appropriately extending one output of the commutator 32-channels of subcommutation are obtained. This subcommutator can be used to commutate thirty-two channels into a single word of a frame. Each Analog Expander contains the selection logic and FET switches necessary to accept 16 different analog signal inputs. The Analog Expander receives its power and logic from the Analog-to-Digital Converter subsystem. Each of the 16 signal inputs are switched onto a common analog signal bus through low "ON" resistance FET gates in a sequential manner--one each frame. The analog signal and its datum are sent to the ADC for conversion into an 8-bit digital word which is then formatted into the data frame.

Each of the inputs of the analog commutator will have a leakage not exceeding 10 microamperes from $+60^{\circ}$ to -10°C and will accept inputs from 0 to 5 volts. Since the analog gates are of an FET design, the user of the encoder will find that the signal sources will be loaded by the input of the analog gate when the power is not applied to the encoding system, however it is recommended that any unused analog inputs be grounded.

A logic diagram of the Analog Expander is shown in Figure B4079 and a timing diagram is shown in Figure B4202.

7.0 SUMMARY

The PCM encoder designed and fabricated for NASA -- Houston is a flexible modularized data acquisition system. It is capable of handling data formats in sixteen word increments with a maximum capacity of sixty-four words. It accommodates both digital and analog words with provisions for subcommutating analog data. The system has been tested over a temperature range from $-10^{\circ}C$ to $+60^{\circ}C$ and operates satisfactorily. It is also packaged according to standard SPACETAC packaging techniques and is capable of surviving vibrations from 20 CPS to 2,000 CPS at 15 G's. Its ability to withstand severe environments, its small size and low power dissipation make it particularly suitable for both rocket and spacecraft experiments.

In the design and the use of the PCM Encoder, problems of coupling noise through the cable harness onto the data bus and interrogation lines were encountered. The system has been designed such that the data transfers are integrated by RC networks before being loaded into the paralliel to serial converter, to eliminate the problems of spike noise. It also became necessary to lower the input impedance of the circuitry in the master programmer which accepts the data on the bus. This enabled any coupled spike noise from the interrogation lines to the data bus lines to settle to less than 1/2 volt during the loading of the data into the master programmer. The interrogation lines were meant to provide a level and not for edge coupling control or triggering operations, consequently the interrogation line signals should not be edge coupled for synchronization or timing pulse generation. Sufficient buffering [illegible]ration

is necessary to use this line properly. Otherwise, it is possible to use the interrogation line to strobe or gate the word pulse from the master programmer which is synchronous with the loading of the data into serial converter.

An attempt was made to make the expansion and the interconnect of the boxes in the system as arbitrary as possible. However, it became necessary to specify the ordering of each expander and also the sequencing of the analog input data between the frame commutated and the subcommutated inputs. If the interconnect had been made completely flexible it would have been necessary to increase the cost and the complexity of the electronics.

Additional test data on all the subsystems are available upon request. This includes data on the exact temperatures and conditions of each individual test. It should suffice to say that the system operated over the specified temperature range and within its electrical specifications.

In the future, it is recommended that a couple of additions be made to the set of boxes. One is a faster ADC to eliminate the restriction generated by the long conversion time. Secondly there should be some provision made for power reversal through incorrect connector harnessing, and/or use of another box for power conversion from the +28 volts to provide all the voltages necessary for the PCM Encoder.

APPENDIX

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NASA/MSC ENCODER SYSTEM

MASTER PROGRAMMER SUBSYSTEM

CONNECTOR PIN DESIGNATIONS

(Master Programmer--Digital Expander Connectors)

J1 (.1, .2, .3)
Cannon - DEC9S (Double Density Connector)

Pin No.	Function	Color Coding J1.1	J1.2	J1.3
1	EN (Enable Digital Expander)	Brown	Red	Orange
2	C (W3)	Brown	Red	Orange
3	+6V	Yellow	Yellow	Yellow
4	D (L1)	Brown	Red	Orange
5	GND	Black	Black	Black
6	B (W2)	Brown	Red	Orange
7	A (W1)	Brown	Red	Orange
8	BK (Blank Digital Expander)	Brown	Red	Orange
9	GND (Feedback)	Brown	Red	Orange

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NASA/MSC ENCODER SYSTEM

MASTER PROGRAMMER SUBSYSTEM

CONNECTOR PIN DESIGNATIONS

(Master Programmer--Spacecraft Connector)

J2
Cannon - 2DA31P (Double Density Connector)

Pin No.	Function	lor Coding
1	Interrogate Line 1	Green
2	Interrogate Line 2	Green
3	Interrogate Line 3	Green
4	Interrogate Line 4	Green
5	Interrogate Line 5	Green
6	NRZ-C (Data Out)	Green
7	Digital Data Bus 2	Green
8	Digital Data Bus 5	Green
9	Digital Data Bus 8	Green
10	+12V Input	White
11	Interrogate Line 6	Green
12	Interrogate Line 7	Green
13	Interrogate Line 8	Green
14	Interrogate Line 9	Green
15	Interrogate Line 10	Green
16	Digital Data Bus 1	Green
17	Digital Data Bus 3	Green
18	Digital Data Bus 6	Green
19	-12V Input	Violet
20	N.U.	
21	+6V Input	Yellow
22	Interrogate Line 11	Green
23	Interrogate Line 12	Green
24	Interrogate Line 13	Green
25	Interrogate Line 14	Green
26	Interrogate Line 15	Green
27	Interrogate Line 16	Green
28	Digital Data Bus 4	Green
29	Digital Data Bus 7	Green
30	GND (Input)	Black
31	N.U.	

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NASA/MSC ENCODER SYSTEM

MASTER PROGRAMMER SUBSYSTEM

CONNECTOR PIN DESIGNATIONS

(Master Programmer--Analog to Digital Converter Connector)

J3
Cannon - 2DA31S (Double Density Connector)

Pin No.	Function	Color Coding
1	N.U.	
2	N.U.	
3	N.U.	
4	N.U.	
5	Main Com Sync	Blue
6	W2	Blue
7	L1	Blue
8	Line (0-1) Select	Blue
9	Line (4-5) Select	Blue
10	+12V	White
11	N.U.	
12	N.U.	
13	N.U.	
14	N.U.	
15	Sub Com Sync	Blue
16	SFT (Shift Pulse)	Blue
17	BK (Blank)	Blue
18	W3	Blue
19	-12V	Violet
20	Line (2-3) Select	Blue
21	+6V	Yellow
22	N.U.	
23	N.U.	
24	N.U.	
25	N.U.	
26	N.U.	
27	N.U.	
28	LD (Load Pulse)	Blue
29	W1	Blue
30	GND	Black
31	Line (6-7) Select	Blue

*Indicates connections needed between Master Programmer and ADC. All other functions are for possible future use.

**As a result of negotiations concerning sync acquisition, a 24-bit pattern (NASA standard) appears in words 1, 2, 3 every frame, and the Main Com Sync signal

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NASA/MSC ENCODER SYSTEM

DIGITAL EXPANDER SUBSYSTEM

CONNECTOR PIN DESIGNATIONS

(Digital Expander--Master Programmer Connector)

J1 (.1, .2, .3)
Cannon - DEC 9P (Double Density Connector)

Pin No.	Function	Color Coding J1 (.1, .2, .3)
1	EN (Enable Digital Expander	Blue
2	C (W3)	Blue
3	+6 Volts	Yellow
4	D (L1)	Blue
5	GND	Black
6	B (W2)	Blue
7	A (W1)	Blue
8	BK (Blank Digital Expander,	Blue
9	GND (Feedback)	Blue

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NASA/MSC ENCODER SYSTEM

DIGITAL EXPANDER SUBSYSTEM

CONNECTOR PIN DESIGNATIONS

(Digital Expander--Spacecraft Connector)

J2 (.1, .2, .3)
Cannon - 2DE19P (Double Density Connector)

Pin No.	Function	Color Coding J2 (.1, .2, .3)
1	N.U.	
2	GND	Black
3	Interrogate Line 2	Green
4	Interrogate Line 4	Green
5	Interrogate Line 5	Green
6	Interrogate Line 7	Green
7	Interrogate Line 10	Green
8	Interrogate Line 12	Green
9	Interrogate Line 13	Green
10	Interrogate Line 15	Green
11	N.U.	
12	Interrogate Line 3	Green
13	Interrogate Line 1	Green
14	Interrogate Line 8	Green
15	Interrogate Line 6	Green
16	Interrogate Line 11	Green
17	Interrogate Line 9	Green
18	Interrogate Line 16	Green
19	Interrogate Line 14	Green

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NASA/MSC ENCODER SYSTEM

ADC SUBSYSTEM

CONNECTOR PIN DESIGNATIONS

(ADC--Master Programmer/Spacecraft Connector)

J1
Cannon - 2DA31P (Double Density Connector)

Pin No.	Function	Color Coding
1	Readout Z	Blue
2	Readout S.C	Blue
3	Analog Input Z	Blue
4	N.U.	
5	S1	Blue
6	Digital Data Bus 1	Blue
7	Digital Data Bus 4	Blue
8	Digital Data Bus 7	Blue
9	S5	Blue
10	+12V	White
11	Readout Y	Blue
12	Analog Input Y	Blue
13	N.U.	
14	Digital Data Bus 2	Blue
15	Sub Com Sync	Blue
16	Shift	Blue
17	Digital Data Bus 8	Blue
18	S2	Blue
19	-12V	Violet
20	S3	Blue
21	+6V	Yellow
22	Readout X	Blue
23	Analog Input X	Blue
24	Digital Data Bus 3	Blue
25	Digital Data Bus 5	Blue
26	Digital Data Bus 6	Blue
27	S4	Blue
28	Load	Blue
29	N.U.	
30	GND	Black
31	N.U.	

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NASA/MSC ENCODER SYSTEM

ANALOG EXPANDER SUBSYSTEM

CONNECTOR PIN DESIGNATIONS

(Analog Expander--ADC Connector)

J1 (.1, .2)
Cannon - 2DE19P (Double Density Connector)

Pin No.	Function	Color Coding J1 (.1, .2)
1	EN (Enable Analog Expander)	Blue
2	C (S3B)	Blue
3	+6V	Yellow
4	D (S4B)	Blue
5	GND	Black
6	N.U.	
7	N.U.	
8	N.U.	
9	N.U.	
10	N.U.	
11	BK (Blank)	Blue
12	A (S1B)	Blue
13	B (S2B)	Blue
14	AS (Analog Signal)	Blue
15	+12V	White
16	-12V	Violet
17	N.U.	
18	GND (Signal Datum)	Black
19	N.U.	

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NASA/MSC ENCODER SYSTEM

ADC SUBSYSTEM

CONNECTOR PIN DESIGNATIONS

ADC--Analog Expander Connector

J2(.1, .2)
Cannon - 2DE19P (Double Density Connector)

Pin No.	Function	Color Coding J2.1	J2.2
1	EN (Enable Analog Expander)	Brown	Red
2	C (S3B)	Brown	White
3	+6V	Yellow	White
4	D (S4B)	Brown	White
5	GND	Black	White
6	N.U.		
7	N.U.		
8	N.U.		
9	N.U.		
10	N.U.		
11	BK (Blank)	Brown	White
12	A (S1B)	Brown	White
13	B (S2B)	Brown	White
14	AS (Analog Signal)	Brown	White
15	+12V	White	White
16	-12V	Violet	White
17	N.U.		
18	GND (Signal Datum)	Black	White
19	N.U.		

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NASA/MSC ENCODER SYSTEM

ANALOG EXPANDER SUBSYSTEM

CONNECTOR PIN DESIGNATIONS

(Analog Expander--Spacecraft Connector)

J2 (.1, .2)
Cannon - 2DE19S (Double Density Connector

Pin No.	Function	Color Coding J2 (.1, .2)
1	Analog Input 15	Green
2	Analog Input 13	Green
3	Analog Input 12	Green
4	Analog Input 10	Green
5	Analog Input 7	Green
6	Analog Input 5	Green
7	Analog Input 4	Green
8	Analog Input 2	Green
9	Analog Input 3	Green
10	N.U.	
11	Analog Input 14	Green
12	Analog Input 16	Green
13	Analog Input 9	Green
14	Analog Input 11	Green
15	Analog Input 6	Green
16	Analog Input 8	Green
17	Analog Input 1	Green
18	GND (Signal Datum)	Black
19	N.U.	

SPACETAC PCM ENCODER

An encoder system is an instrument that is used to gather different types of data from various sensors then to process and arrange the information into a specific format for transmission.

The SPACETAC PCM Encoder System has been designed to operate in severe environments such as rocket probes and satellites, where low power, small size, and low weight are important considerations. A modularized subsystem packaging technique has been utilized so that the entire system can be oriented into several different space envelopes. Additional systems' flexibility, such as a variable bit rate, format expansion from 16 to 64 channels, as well as the mix of analog and digital channels has been built into the SPACETAC PCM Encoder System.

The functional flexibility and modularized subsystem approach allows a designer the capability of putting together his own encoder system that is tailored to his own specific requirements.

Overall System Specifications

Power:	180mW Quiescent, 200mW Peak (512μs duration - during A/D conversion)
Volume:	48.75 cubic inches
Weight:	880 grams
Format:	8-bit words, 16 to 64 words/main frame plus 32 sub-commutated data words
Speed:	4 Kbps to 64 Kbps

The SPACETAC PCM Encoder System consists of four types of modular subsystems: Master Programmer, Analog-to-Digital Converter, Digital Expander, and Analog Expander.

Master Programmer

The Master Programmer contains the system clock, and the basic count-down chain consisting of the clock frequency divider, bit counter, word counter, and line counter. In addition, it contains the selection logic for generating the minimum format of 16 channels as well as the drivers to expand the format to 64 channels. The Master Programmer also has an 8-bit parallel-to-serial converter whose NRZ-C output can be used to drive a transmitter:

Specifications

Power:	70mW (11.5ma at +6V)
Size:	1.0" x 4.5" x 5.0" (22.5 cu.in.)
Weight:	350 grams
Environment:	-10°C to $+60^{\circ}$C (spaceflight qualified)
Bit Rates Available:	64Kbps, 32Kbps, 16Kbps, 8Kbps, 4Kbps
Data Channels Available:	16 maximum (depends on number of sync words)
Sync:	32 bits maximum (any pattern)
Word Length:	8 bits

Digital Expander

Each Digital Expander contains the selection logic and drivers necessary to expand the format by an additional 16 channels. The Digital Expander receives its power and logic from the Master Programmer. The 16 "Interrogation Line" outputs are used to interrogate 16 digital gates in sequence. Each digital gate is capable of accepting up to eight bits of information, and when it receives an interrogate signal from a Digital Expander, the eight bits of information are transferred, in parallel, to the serializing register in the Master Programmer via an 8-line data bus.

Specifications

Power:	4.0mW (0.67ma at +6V)
Size:	1.0" x 1.5" x 2.5" (3.75 cu.in.)
Weight:	75 grams
Environment:	-10°C to +60°C (spaceflight qualified)
Data Channels Available:	16 (3 Digital Expanders are necessary to expand the frame format to 64 channels)

Analog-to-Digital Convertor

The ADC is used primarily to convert relatively slow changing analog information, such as temperature, fuel pressure, etc., associated with payload parameters that are of interest into digital data for transmission over a PCM telemetry link. The ADC utilizes the double ramp integrator technique which minimizes errors due to line voltage variations and temperature. The ADC converts high level (0 to +5.10V) signals into an 8-bit digital word that is transferred to the serializer in the Master Programmer upon the receipt of an "interrogation" signal, which also begins the next conversion process.

The ADC time multiplexes 35 different analog signals; three signals are processed within one frame of the format and the remaining 32 analog signals are subcommutated so that one is converted in each frame of the format. The ADC also provides the necessary logic functions to operate two Analog Expanders.

Specifications

Power:	Quiescent; 87mW (6.0ma at +6V, 3.25ma at -12V, 1.0 ma at +12V) Peak; 110mW (11.0ma at +6V, 3.5 ma at -12V, 1.1ma at +12V)
Size:	1.0" x 2.5" x 3.0" (7.5 cu. in.)
Weight:	165 grams
ADC Clock:	1MHz
Conversion Rate:	1KHz max (8-bit words)
Conversion Time:	512μs max
Aperture Time:	256μs
Input Signal Range:	0 to 5.10 vdc
Input Impedance:	$> 1\ m\Omega$
Absolute Accuracy:	±1/2 LSB ±0.2% of full scale
Environment:	$-10^{\circ}C$ to $+60^{\circ}C$ (spaceflight qualified)
Built-in Multiplexer:	4 Channels (plus Analog Expander Control)

Analog Expander

Each Analog Expander contains the selection logic and FET switches necessary to accept 16 different analog signal inputs. The Analog Expander receives its power and logic from the Analog-to-Digital Converter subsystem. Each of the 16 signal inputs are switched onto a common analog signal bus through low "ON" resistance FET gates in a sequential manner--one each frame. The analog signal and its datum are sent to the ADC for conversion into an 8-bit digital word which is then formatted into the data frame.

Specifications

Power:	4.0mW (0.375ma at +6V, 0.05ma at -12V, .17ma at +12V)
Size:	1.0" x 1.5" x 2.5" (3.75 cu.in.)
Weight:	75 grams
Environment:	-10^{o}C to $+60^{o}$C (spaceflight qualified)
Analog Signal Inputs:	16 (0 to +5.10 vdc - full scale)

Two Analog Expanders are necessary to provide 32 channels of subcommutated data.

JAN. 9, 1969.

NASA/MSC ENCODER
ANALOG TO DIGITAL CONVERTER
TEMPERATURE TEST

MAXIMUM TOTAL DEVIATION FROM −12°C TO +54°C IS :−

[A] ZERO DRIFT = 50% OF L.S.B.

OR APPROXIMATELY EQUIVALENT TO $\pm \frac{1}{4}$ L.S.B.

[B] FULL SCALE DRIFT ≅ 0.37 %

[C] DIFFERENTIAL LINEARITY : 6.5 %

[D] INDECISION ZONE IS 0.8 MILLIVOLT

NAST / NLC ENCODER

ANALOG TO DIGITAL CONVERTER

TEMPERATURE TEST

Page A-4

TEMPERATURE: 23°C | DATE: JAN. 9, 1969.

DECIMAL OUTPUT	ANALOG INPUT (mV)	ΔV (mV)
1	20.3	
2	40.6	20.3
3	61.7	21.1
4	82.7	21.0
5	102.7	20.0
6	188.7	20.0
7	143.0	20.3
8	163.9	20.9
15	305.0	
16	325.0	20.0
31	628.7	
32	648.8	20.1
63	1271.0	
64	1281.0	20.0
95	1912.0	
96	1932.0	20.0
127	2552.0	
128	2572.0	20.0
143	2892.0	
144	2912.0	20.0
159	3191.0	
160	3211.0	20.0
191	3828.0	
192	3848.0	20.0
207	4146.0	
208	4166.0	20.0
223	4463.0	
224	4483.0	20.0
253	5056.0	
254	5076.0	20.0
255	5097.0	21.0

REMARKS :

(i) Readings are recorded from Z-Channel.

(ii) DIFFERENTIAL LINEARITY 5.5 %

(iii) INDECISION ZONE IS 0.8 millivolt

NASA/ MSC ENCODER

ANALOG TO DIGITAL CONVERTER

TEMPERATURE TEST

TEMPERATURE: +54°C	DATE: JAN 9, 1969

DECIMAL OUTPUT	ANALOG INPUT (mV)	ΔV (mV)
1	25.0	
2	44.0	19.0
3	64.0	20.0
4	85.0	21.0
5	106.0	21.0
6	126.0	20.0
7	146.0	20.0
8	166.0	20.0
15	307.0	
16	327.0	20.0
31	628.0	
32	648.0	20.0
63	1269.0	
64	1289.0	20.0
95	1909.0	
96	1929.0	20.0
127	2549.0	
128	2569.0	20.0
143	2867.0	
144	2887.0	20.0
159	3186.0	
160	3206.0	20.0
191	3824.0	
192	3844.0	20.0
207	4142.0	
208	4161.0	19.0
223	4458.0	
224	4478.0	20.0
253	5055.0	
254	5074.0	19.0
255	5094.0	20.0

REMARKS:

(i) Readings are recorded from 2-channel

(ii) DIFFERENTIAL LINEARITY IS 5.0%

(iii) INDECISION ZONE IS 0.8 mvolt

NASA / MSC [illegible] TRACK
ANALOG TO DIGITAL CONVERTER
TEMPERATURE TEST

TEMPERATURE: −12°C | DATE: JAN. 9, 1969

DIGITAL OUTPUT	ANALOG INPUT (mV)	ΔV (mV)
1	15.0	
2	36.2	21.2
3	57.2	21.0
4	78.5	21.3
5	99.5	21.0
6	120.0	20.5
7	140.7	20.7
8	161.0	20.3
15	305.0	
16	326.0	21.0
31	631.0	
32	651.5	20.5
63	1277.0	
64	1297.0	20.0
95	1922.0	
96	1942.0	20.0
127	2566.0	
128	2586.0	20.0
143	2886.0	
144	2906.0	20.0
159	3206.0	
160	3226.0	20.0
191	3844.0	
192	3864.0	20.0
207	4163.0	
208	4183.0	20.0
223	4479.0	
224	4499.0	20.0
253	5074.0	
254	5094.0	20.0
255	5113.0	19.0

REMARKS:

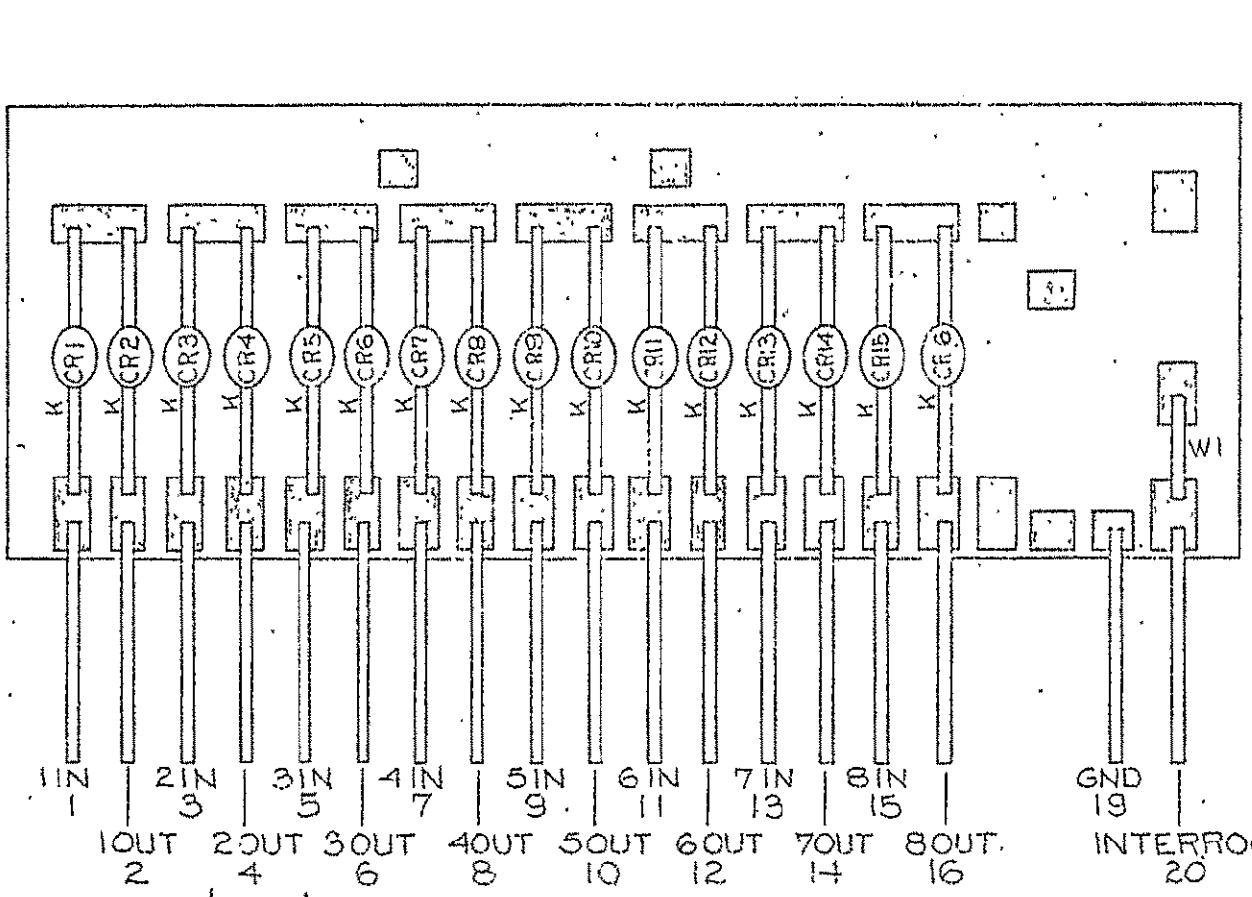
(i) Readings are recorded from 2-channel.

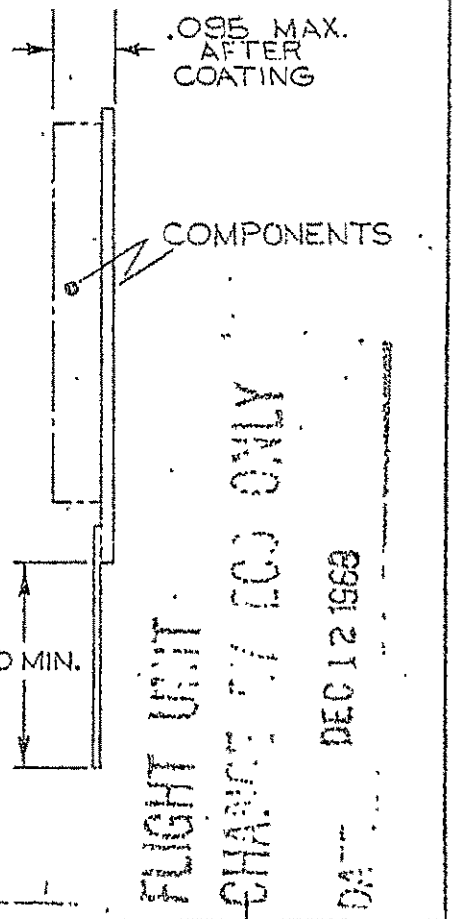
(ii) DIFFERENTIAL LINEARITY 0.5 %

(iii) INDICISION ZONE IS 0.8 MVOLTS

USED ON	NEXT ASSY.

REVISIONS				
REV	DESCRIPTION	BY	DATE	APP'VD

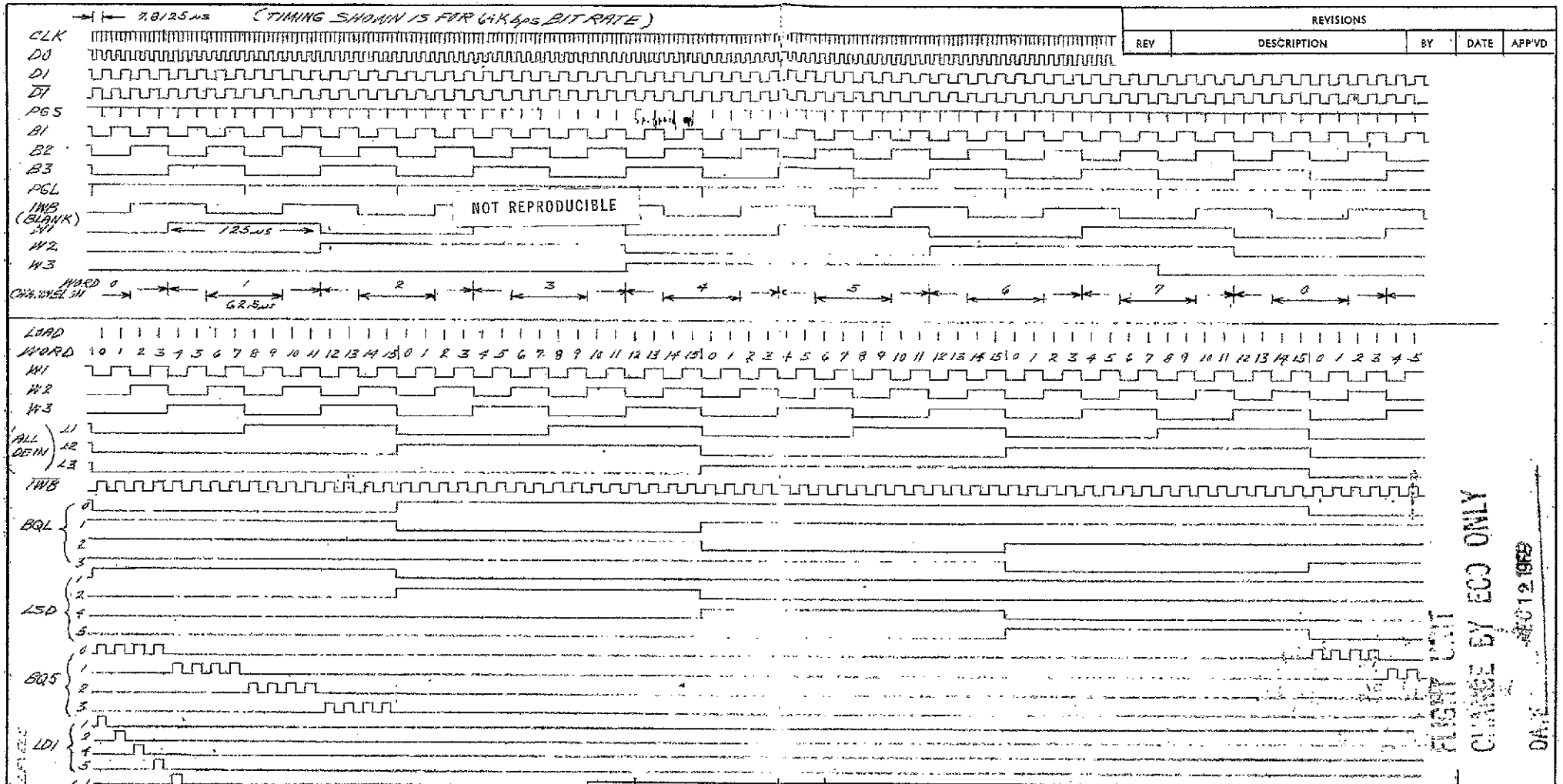




QTY GI	PART NO.	ITEM	DESCRIPTION	REF DES

LIST OF MATERIAL

UNLESS OTHERWISE SPECIFIED	BY	DATE		
FRACTIONS ±1/64	DR D.L. FORRESTER	10-25-68	SPACETAC	SPACE AND TACTICAL SYSTEMS CORP.
DECIMALS .000 = ±.005	CHK R. Vanderwarker	12/12/68		BURLINGTON, MASS. 01803
.00 = ±.010	ENG D.L. Forrester	12/12/68	TITLE	C4094-2. DIGITAL GATE ASSY
ANGLES ±30'	PROD R. Vanderwarker	12-12-68		
REMOVE BURRS & SHARP EDGES			SCALE 4 x 1	DWG NO. A4166 REV —



REVISIONS				
REV	DESCRIPTION	BY	DATE	APP'VD

RELEASED BY ECO ONLY
DATE DEC 12 1968

QTY GI	PART NO.	ITEM	DESCRIPTION	REF DES

LIST OF MATERIAL

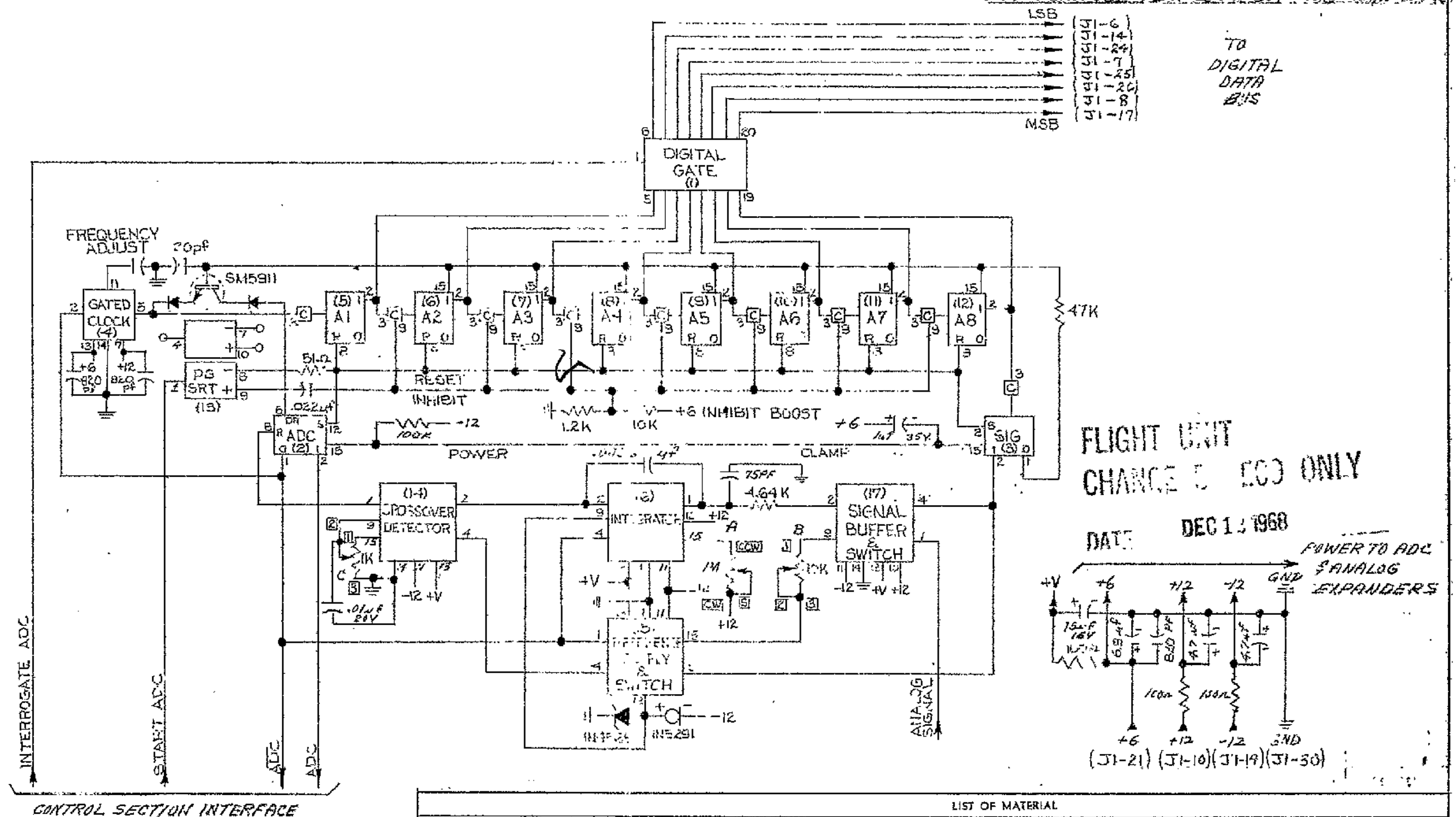
UNLESS OTHERWISE SPECIFIED	BY	DATE
FRACTIONS ±1/64	DR B.M.C.	12/10/68
DECIMALS .000 = ±.005	CHK R. Vaudmarcourt	12/12/68
.00 = ±.010	ENG D A Dalton	12/12/68
ANGLES ±30'	PROD	
REMOVE BURRS & SHARP EDGES		

SPACETAC — SPACE AND TACTICAL SYSTEMS CORP.
BURLINGTON, MASS. 01803

TITLE TIMING DIAGRAM NASA/MSC ENCODER MASTER PROGRAMMER

SCALE NONE | DWG NO. C-41E0 | REV

REVISIONS				
REV	DESCRIPTION	BY	DATE	APP'VD
A	CHANGE PER ECO [illegible]	[illegible]	[illegible]	[illegible]



FLIGHT UNIT
CHANGE [illegible] ECO ONLY
DATE DEC 1 [illegible] 1968

NOTES:

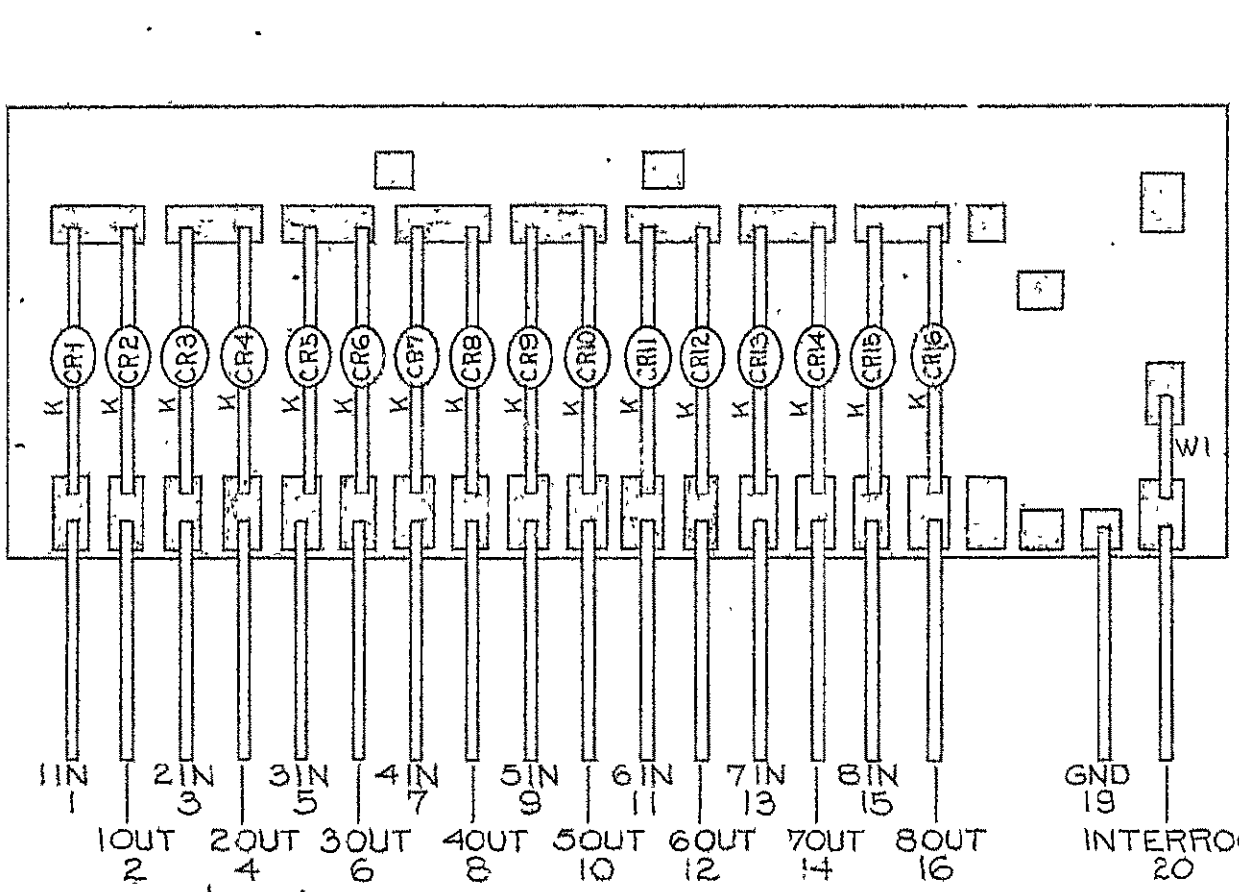
1. ( ) INDICATES B ROW MODULE LOCATION.
2. PWR. ON MODULES (5)-(13): +6, PIN 13, GND, PIN 14
3. PWR. ON MODULES (2),(3): +6, PIN 13, -12, PIN 14

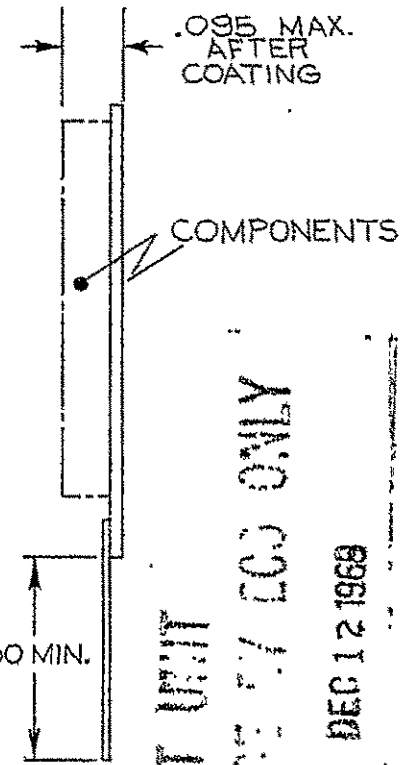
LIST OF MATERIAL

UNLESS OTHERWISE SPECIFIED	BY	DATE	
FRACTIONS ±1/64	DR D.L. FORRESTER	10-18-68	SPACETAC — SPACE AND TACTICAL SYSTEMS CORP. BURLINGTON, MASS. 01803
DECIMALS .000 = ±.005	CHK R. [illegible]	12/12/68	TITLE NAC V MSC ENCODER ANALOG TO DIGITAL CONVERTER SUBSYSTEM (ADC SCHEMATIC)
.00 = ±.010	ENG D.A. [illegible]	12/12/68	
ANGLES ±30'	PROD [illegible]	12-[illegible]-68	SCALE [illegible]
REMOVE BURRS & SHARP EDGES			DWG NO. B4175 — REV A

USED ON	NEXT ASSY.

REVISIONS				
REV	DESCRIPTION	BY	DATE	APP'VD

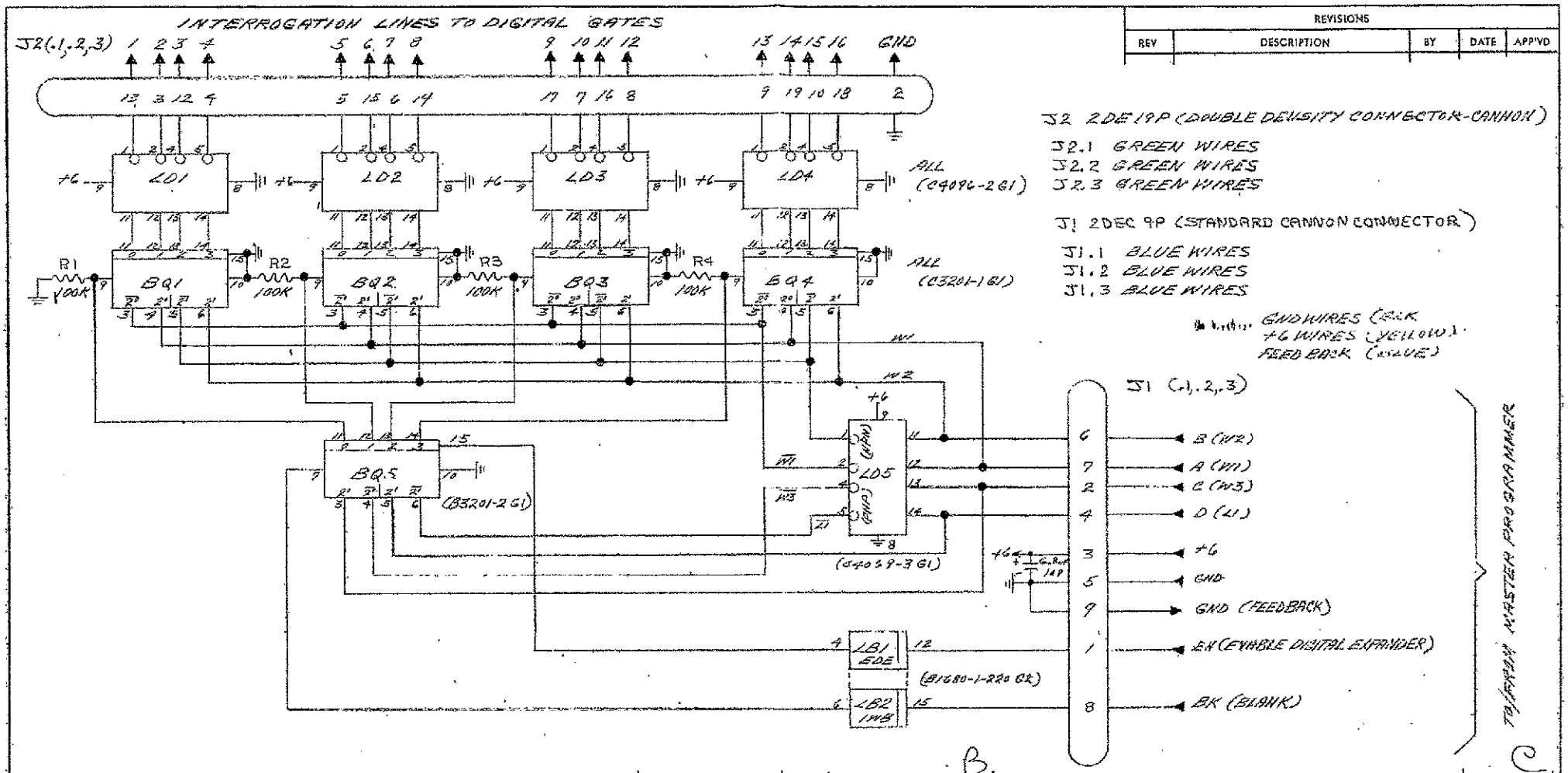




QTY G1	PART NO.	ITEM	DESCRIPTION	REF DES

LIST OF MATERIAL

UNLESS OTHERWISE SPECIFIED	BY	DATE		
FRACTIONS ±1/64	DR D.L. FORRESTER	10-25-68	SPACETAC	SPACE AND TACTICAL SYSTEMS CORP.
DECIMALS .000 = ±.005	CHK R. Vanderwerf	12/12/68		BURLINGTON, MASS. 01803
.00 = ±.010	ENG D.N. Dalton	12/12/68	TITLE	C4094-2 DIGITAL GATE ASSY
ANGLES ±30'	PROD Roy J. Damien	12-12-68		
REMOVE BURRS & SHARP EDGES			SCALE 4×1	DWG NO. A4166 REV —



REVISIONS				
REV	DESCRIPTION	BY	DATE	APP'VD

FLIGHT UNIT
CHANGE BY ECO ONLY
DATE DEC 1, 1968

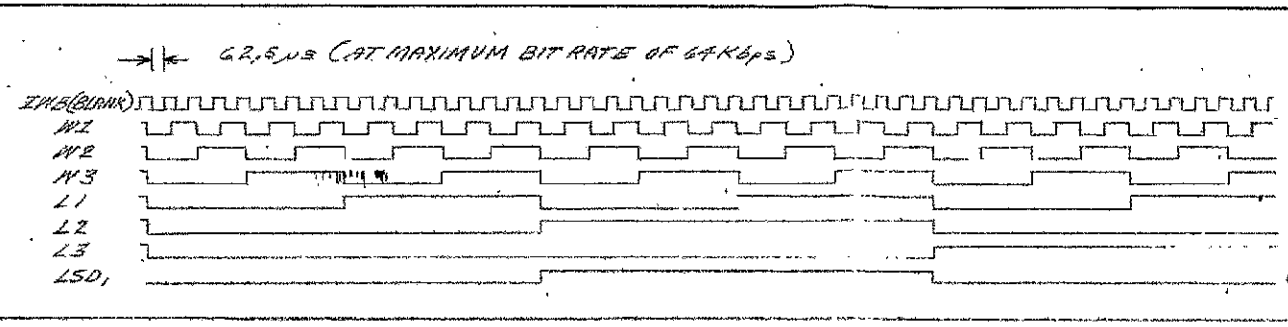
QTY G1	PART NO.	ITEM	DESCRIPTION	REF DES
			LIST OF MATERIAL	

UNLESS OTHERWISE SPECIFIED	BY	DATE
FRACTIONS ±1/64	DR [illegible]	9/5/68
DECIMALS .000 = ±.005	CHK R. V. Hammond	12/2/68
.00 = ±.010	ENG D. L. Dillman	12/6/68
ANGLES ±30'	PROD [illegible]	[illegible]
REMOVE BURRS & SHARP EDGES		

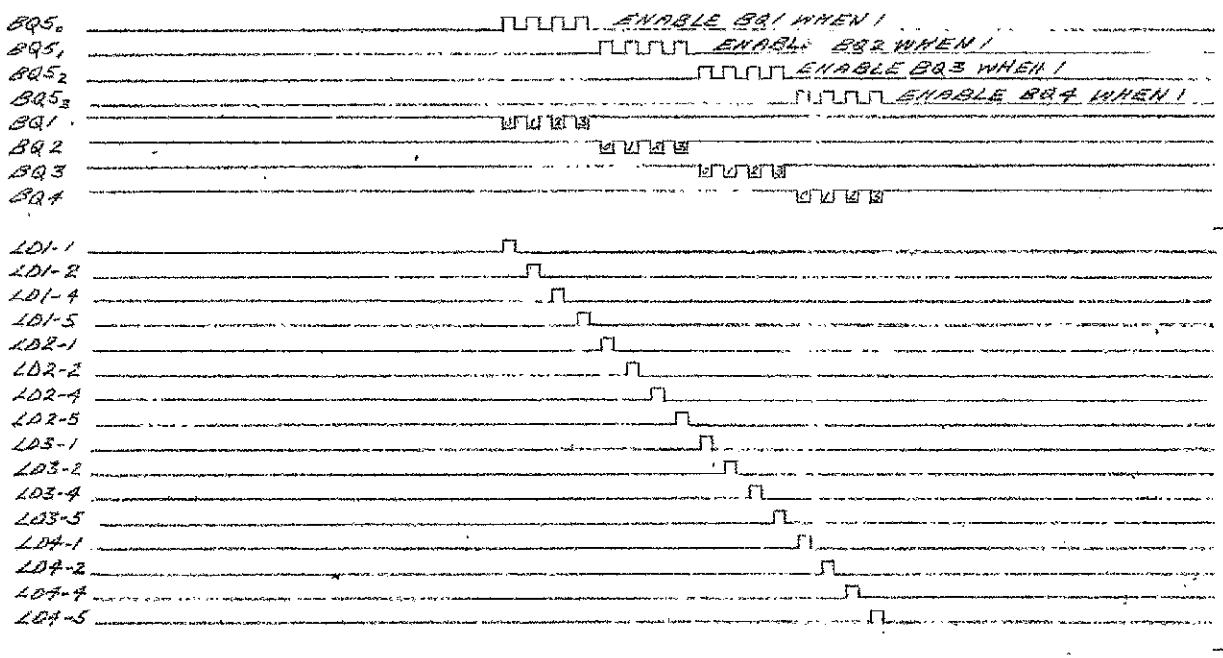
SPACETAC — SPACE AND TACTICAL SYSTEMS CORP.
BURLINGTON, MASS. 01803

TITLE LOGIC DIAGRAM
DIGITAL EXPANDER SUBSYSTEM

SCALE — DWG NO. B40 F 8 REV —



TIMING INPUTS TO EXPANDER SUBSYSTEM - FROM MASTER PROGRAMMER



OUTPUTS OF DIGITAL EXPANDER SUBSYSTEM FORM POSITIVE INTERROGATION LEVELS WHICH ENABLE A DIGITAL GATE TO TRANSFER EIGHT BITS (ONE WORD) OF DATA ONTO THE DIGITAL DATA BUS

FLIGHT UNIT
CHANGE BY ECO ONLY
DATE DEC 12 1969

REVISIONS				
REV	DESCRIPTION	BY	DATE	APP'VD

QTY G1	PART NO.	ITEM	DESCRIPTION	REF DES

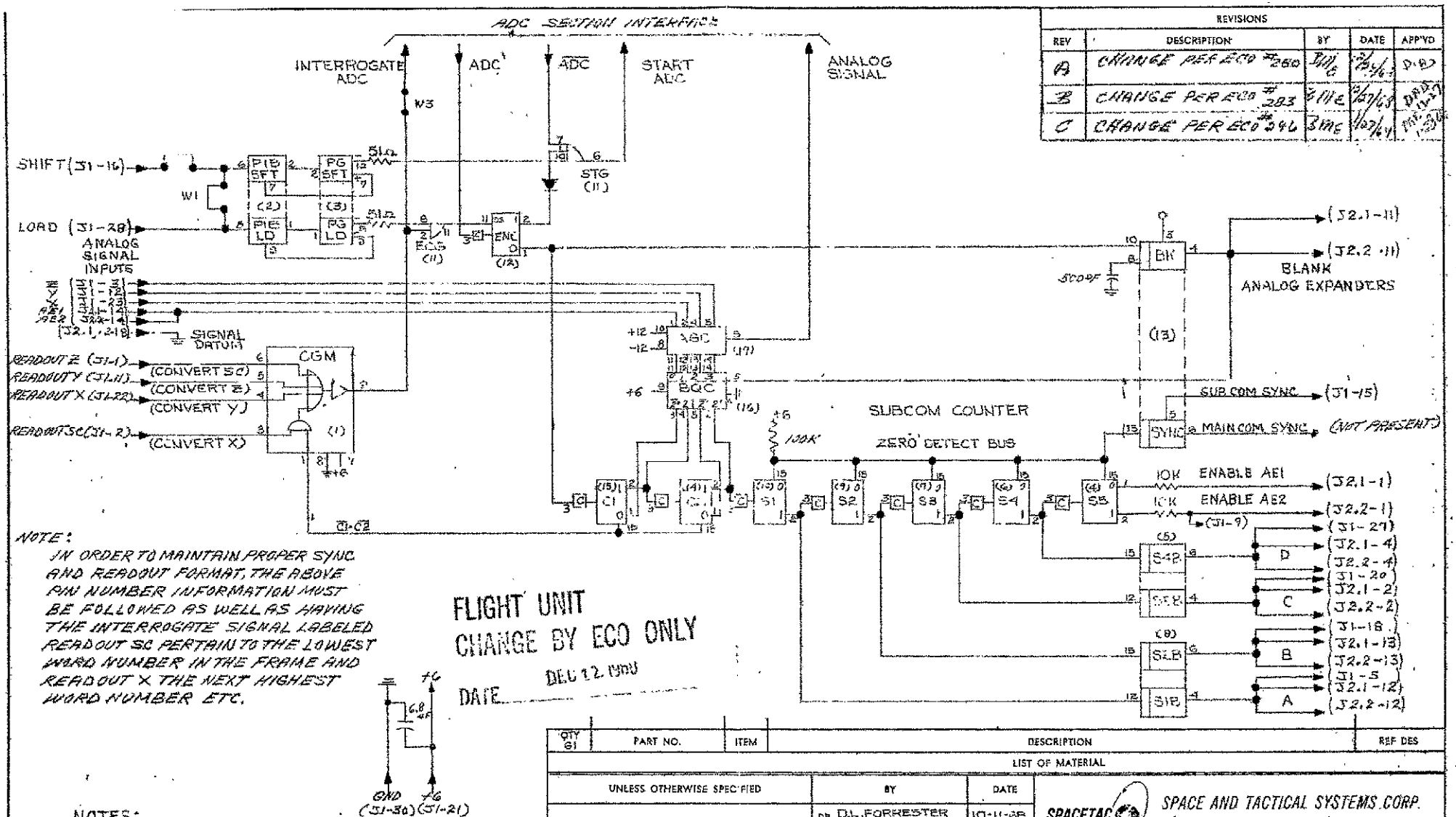
LIST OF MATERIAL

UNLESS OTHERWISE SPECIFIED	BY	DATE
FRACTIONS ±1/64	DR [illegible]	12/1/68
DECIMALS .000 = ±.005	CHK Z. Vartparonian	12/12/68
.00 = ±.010	ENG D.A. Pelletier	12/12/68
ANGLES ±30'	PROD [illegible]	[illegible]
REMOVE BURRS & SHARP EDGES		

SPACETAC SPACE AND TACTICAL SYSTEMS CORP.
BURLINGTON, MASS. 01803

TITLE TIMING DIAGRAM DIGITAL EXPANDER SUBSYSTEM, NASA/NSC ENCODER

SCALE NONE | DWG NO. 84123 | REV —



REVISIONS				
REV	DESCRIPTION	BY	DATE	APP'VD
A	CHANGE PER ECO #260	BME	12/4/68	D.R.D
B	CHANGE PER ECO # 283	BME	12/27/68	D.R.D
C	CHANGE PER ECO #346	BME	1/27/69	D.R.D

NOTE:
IN ORDER TO MAINTRAIN PROPER SYNC. AND READOUT FORMAT, THE ABOVE PIN NUMBER INFORMATION MUST BE FOLLOWED AS WELL AS HAVING THE INTERROGATE SIGNAL LABELED READOUT SC PERTAIN TO THE LOWEST WORD NUMBER IN THE FRAME AND READOUT X THE NEXT HIGHEST WORD NUMBER ETC.

FLIGHT UNIT
CHANGE BY ECO ONLY
DATE DEC 12, 1968

NOTES:
1. ( ) INDICATES A ROW MODULE LOCATION
2. PWR. ON MODULES (2)-(10), (12)-(15): +6 PIN 13, GND PIN 14

QTY	PART NO.	ITEM	DESCRIPTION	REF DES
61			LIST OF MATERIAL	

UNLESS OTHERWISE SPECIFIED	BY	DATE
FRACTIONS ±1/64	DR D.L. FORRESTER	10-11-68
DECIMALS .000 = ±.005	CHK R. VanHorn	12/12/68
.00 = ±.01	ENG D.A. Wilson	12/12/68
ANGLES ±30'	PROD S. Sullivan	12-12-68
REMOVE BURRS & SHARP EDGES		

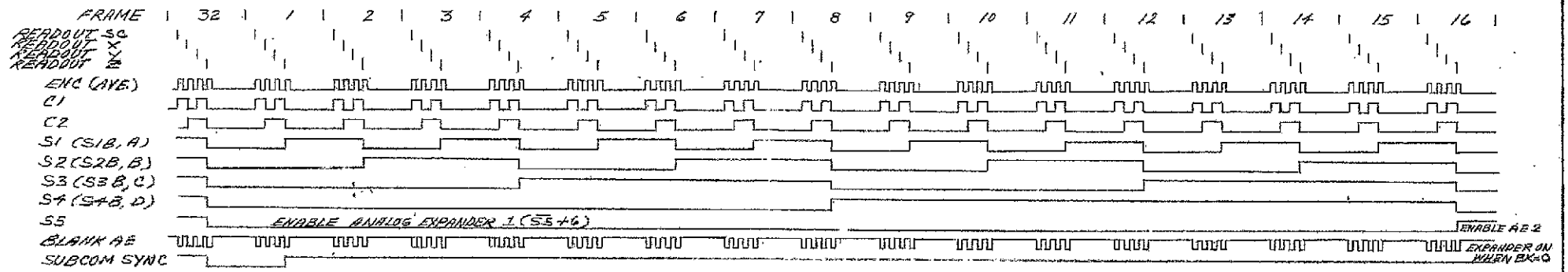
SPACETAC — SPACE AND TACTICAL SYSTEMS CORP.
BURLINGTON, MASS. 01803

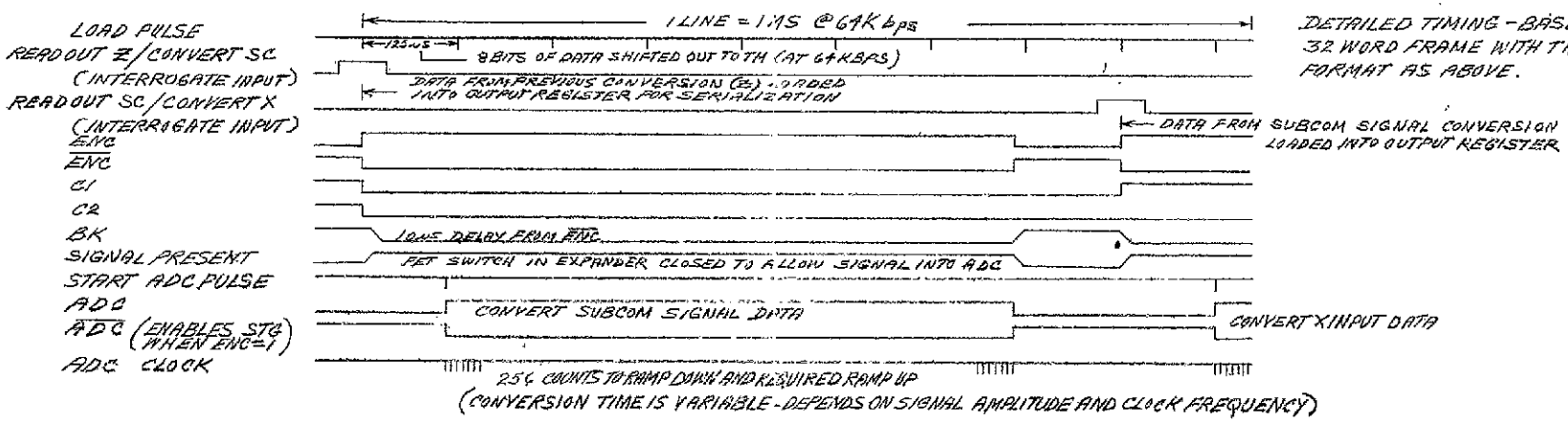
TITLE NASA/MSC ENCODER
ANALOG TO DIGITAL CONVERTER SUBSYSTEM
CONTROL SECTION

SCALE NONE | DWG NO. 84136 | REV C

REVISIONS				
REV	DESCRIPTION	BY	DATE	APP'VD

CONSIDER SAMPLE FORMAT AS: RDOUT S.C. = WORD 8, RDOUT X = WORD 16, RDOUT Y = WORD 24, RDOUT Z = WORD 32, FRAME LENGTH = 64 WORDS ⟷ = 8 WORDS (ONE LINE)





DETAILED TIMING - BASED ON A 32 WORD FRAME WITH THE SAME FORMAT AS ABOVE.

QTY G1	PART NO.	ITEM	DESCRIPTION	REF DES

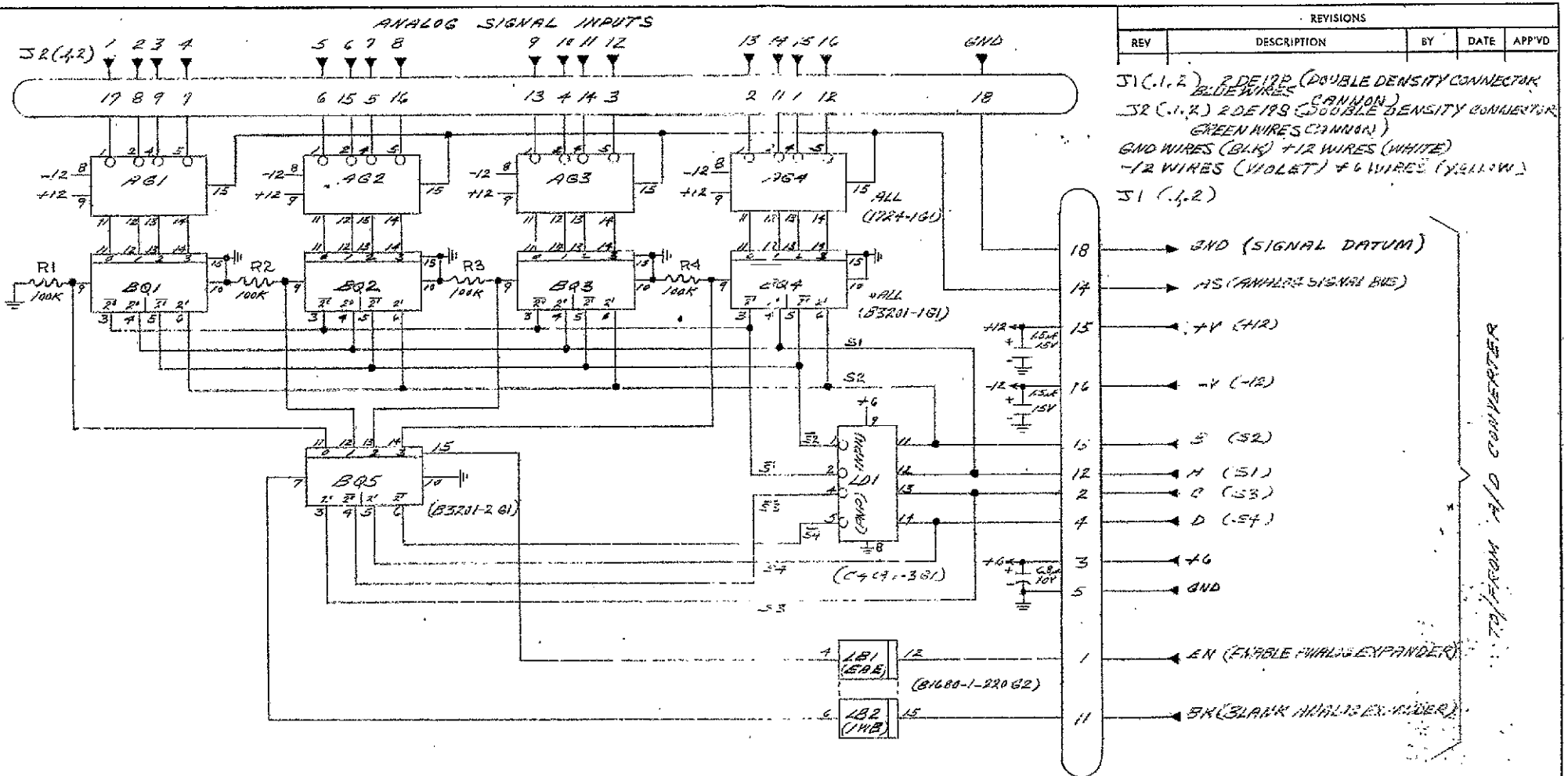
LIST OF MATERIAL

UNLESS OTHERWISE SPECIFIED	BY	DATE
FRACTIONS ±1/64	DR	1/31/69
DECIMALS .000 = ±.005	CHK R. Gallagher	1/31/69
.00 = ±.010	ENG	1/31/69
ANGLES ±30'	PROD	1/31/69
REMOVE BURRS & SHARP EDGES		

SPACETAC — SPACE AND TACTICAL SYSTEMS CORP.
BURLINGTON, MASS. 01803

TITLE: TIMING DIAGRAM NASA/MSC ENCODER A/D CONVERTER SUBSYSTEM

SCALE: NONE | DWG NO. E-4209 | REV



REVISIONS				
REV	DESCRIPTION	BY	DATE	APP'VD

J1 (1,2) 2 DE19P (DOUBLE DENSITY CONNECTOR BLUE WIRES CANNON)
J2 (1,2) 2 DE19S (DOUBLE DENSITY CONNECTOR GREEN WIRES CANNON)
GND WIRES (BLK) +12 WIRES (WHITE)
-12 WIRES (VIOLET) +6 WIRES (YELLOW)

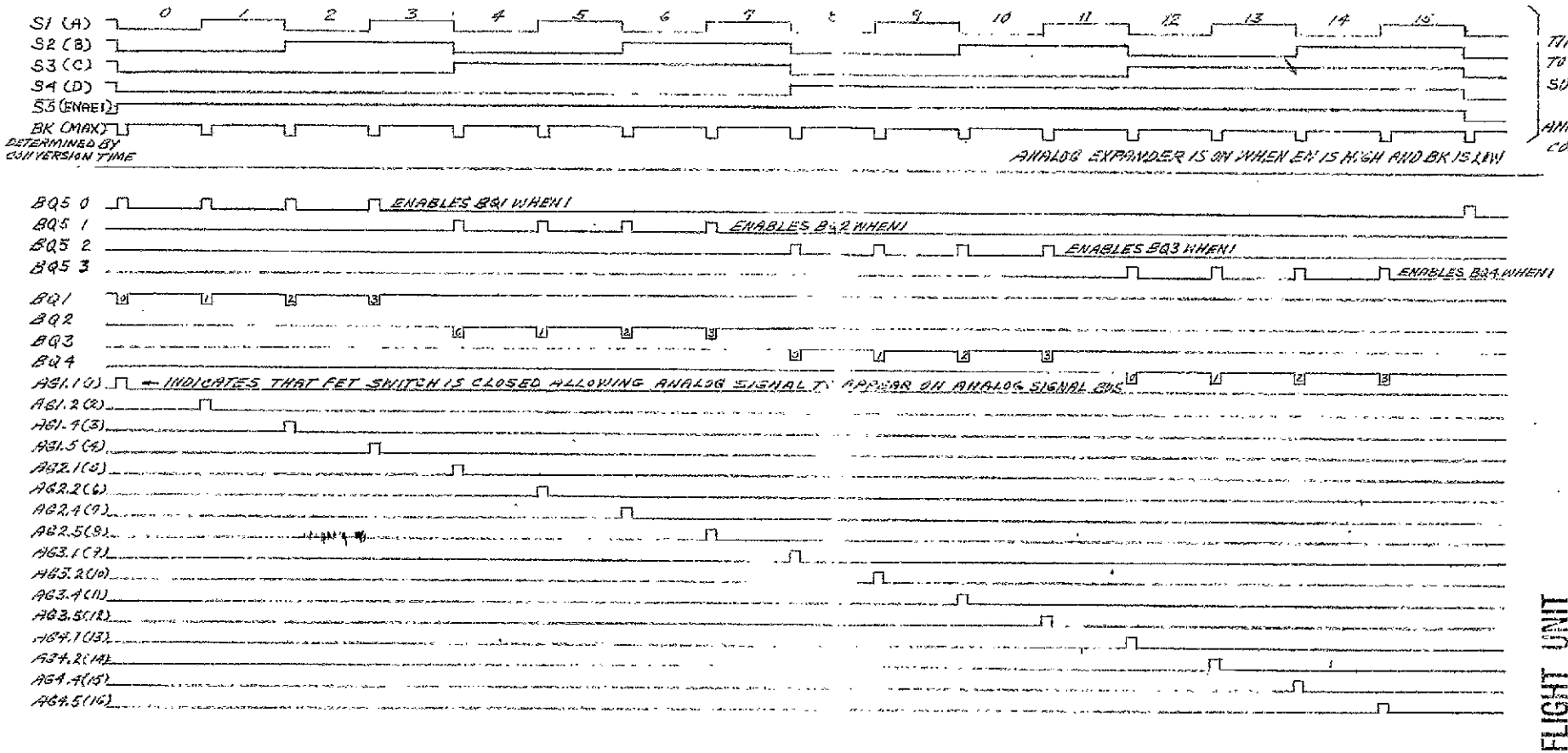
FLIGHT UNIT
CHANGE BY ECO ONLY
DATE REP 12 '68

QTY EI	PART NO.	ITEM	DESCRIPTION	REF DES

LIST OF MATERIAL

UNLESS OTHERWISE SPECIFIED	BY	DATE	SPACETAC SPACE AND TACTICAL SYSTEMS CORP. BURLINGTON, MASS. 01803	
FRACTIONS ±1/64	DR BMC	9/5/68		
DECIMALS .000 = ±.005	CHK R. Vanderhoof	12/12/68		
.00 = ±.010	ENG D.H. Oltman	12/12/68	TITLE LOGIC DIAGRAM ANALOG EXPANDER SUBSYSTEM	
ANGLES ±30'	PROD		SCALE —	DWG NO. 8-319 REV —
REMOVE BURRS & SHARP EDGES				

REVISIONS				
REV	DESCRIPTION	BY	DATE	APP'VD



FLIGHT UNIT
CHANGE BY ECO ONLY
DEC 12 1968
DATE

QTY G1	PART NO.	ITEM	DESCRIPTION	REF DES

LIST OF MATERIAL

UNLESS OTHERWISE SPECIFIED	BY	DATE
FRACTIONS ±1/64	DR [illegible]	9/5/68
DECIMALS .000 = ±.005	CHK R. [illegible]	12/12/68
.00 = ±.010	ENG D. A. [illegible]	12/12/68
ANGLES ±30'	PROD	
REMOVE BURRS & SHARP EDGES		

SPACETAC — SPACE AND TACTICAL SYSTEMS CORP.
BURLINGTON, MASS. 01803

TITLE: TIMING DIAGRAM
ANALOG EXPANDER SUBSYSTEM
5050 MSC EXPANDER

SCALE: NONE | DWG NO. E-7302 | REV

FINAL REPORT FOR PCM ENCODER SYSTEM

Space and Tactical Systems Corporation
Burlington, Massachusetts

31 January 1969