NASA CR 66742-2

STUDY OF IMPROVED PARTS CONTROL TECHNOLOGY FOR ADVANCED PLANETARY MISSIONS

VOLUME II - PART CONTROL PACKAGE

Prepared Under Contract No. NAS1-7259 by

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NATIONAL AERONAUTICS AND SPACE ADMINISTRATION
Langley Research Center

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EXAMPLE (NOT FOR PROCUREMENT)

NSL-A401

GENERAL PROCUREMENT SPECIFICATION FOR NASA SPECIAL LONG-LIFE (NSL) TRANSISTORS

FEBRUARY 1969

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NSL-A401

GENERAL PROCUREMENT SPECIFICATION FOR

NASA SPECIAL LONG-LIFE (NSL) TRANSISTORS

1. SCOPE

1.1 Applicability

This specification is part of the system of Part Control Packages for controlling NASA Special Long-Life (NSL) parts, described in NASA CR-66742-1. This specification is general section A of Part Control Package NSL-401, and defines the general parts procurement requirements for all NSL transistors. This specification and the applicable detail procurement specification, NSL-A401/____, are mandatory whenever NSL transistors are specified.

1.2 Part Identification

Transistors procured under this general specification shall be identified by the NSL part type number defined in the applicable detail procurement specification.

1.3 Part Manufacturer Identification

Transistors procured under this general specification shall be manufactured and obtained directly and only from the part manufacturer identified in the applicable detail procurement specification.

1.4 Deviations

All requirements contained in this general procurement specification and in the applicable detail procurement specification are binding. The part manufacturer shall under no circumstances use the NSL part type number, defined in the applicable detail procurement specification, on a part that deviates in any manner from the requirements herein or in the applicable detail procurement specification. The requirements of this specification cannot be waived or changed by procurement orders, letters, documents, or any other means short of changes to this general procurement specification and/or the applicable detail procurement specification, which have been approved by the prime contractor and the NASA as defined in 1.5 of this specification.

1.5 Revision Verification

Revisions to this specification and/or the applicable detail procurement specification shall not be considered to be valid unless they meet all the following criteria: All changes shall be incorporated into the body of

the specification, and the revised version of the specification shall be marked with the revision letter added after the document number on each sheet. For example, NSL-A401C would designate the third (C) revision of this specification. Each revision shall be defined in a "Revision Record" sheet identifying the section and the change in detail. Each revision shall be approved on the Revision Record sheet, by signature and date, by the prime contractor's parts program manager (or authorized representative) and the designated representative of the NASA. The Revision Record sheet shall be included at the end of each NSL specification, but preceding appendixes.

1.5 Change Notification

In the event of any change in material, design, construction, or process control for this NSL transistor after a purchase order is placed and prior to completion of procurement, the part manufacturer is required to notify the prime contractor, using the "Change Notification" form provided in appendix A to this specification. Unless the prime contractor furnishes written disapproval of the change within 15 days after receipt of change notification, the change will become valid. A disapproval shall constitute a cancellation of the order, in which case recertification shall be required.

Unless the change has only a minor effect on form, fit, function, or reliability, approval of the procurement specification by the NASA shall be considered suspended until the changes are removed or are approved by the prime contractor and the designated representative of the NASA, as evidenced by one of the following actions:

a. In the event that the change is in conflict with specific requirements in this specification and/or the detail procurement specifications, then the specification must be revised to incorporate the change as defined in 1.5 of this specification.

b. In the event that the change is not in conflict with a specific requirement in this specification and/or the detail procurement specification, then the applicable procurement specification must be re-released with a new revision letter as defined in 1.5 of this specification. However, the only physical change to the detail procurement specification shall consist of a description of the change in the Revision Record, with approval by the prime contractor and the designated NASA representative.

2. APPLICABLE DOCUMENTS

2.1 Documents

The following documents form a part of this specification to the extent specified herein. Unless otherwise specified herein, the issue in effect on the date of the part procurement contract shall apply.

STANDARDS

Military

MIL-STD-129	Marking for Shipment and Storage
MIL-STD-202	Test Methods for Electronic and Electrical Component Parts
MIL-STD-453	Inspection, Radiographic
MIL-STD-750	Test Methods for Semiconductor Devices
MIL-STD-1276	Leads, Weldable, for Electronic Component Parts

SPECIFICATIONS

Military

MIL-S-19500	Semiconductor Devices, General Specification for

NASA

NSL-A401/____	Detail Procurement Specification for NASA Special Long-Life (NSL) Transistors

2.2 Conflicting Requirements

In the event of conflict between the requirements of this specification and any of the documents specified herein or in the applicable detail procurement specification, the order of precedence shall be as follows:

a. The applicable NASA Special Long-Life (NSL) detail procurement specification.

b. This general procurement specification.

c. Specifications referenced herein or in the applicable detail procurement specification.

3. PRODUCT REQUIREMENTS

3.1 Electrical Characteristics

The electrical characteristics of the transistors shall be as specified in 3.1 of the applicable detail procurement specification.

3.2 External Physical Characteristics

The external physical characteristics of the transistors shall be as specified in 3.2 of the applicable detail procurement specification. In addition, the following general requirements shall apply:

3.2.1 Lead Materials

Lead materials shall be suitable for both soldering and welding and shall conform to the MIL-STD-1276 type specified in the applicable detail procurement specification. After completion of all specified tests, the leads shall show no evidence of corrosion or degradation that will affect electrical or mechanical performance or reliability. The leads shall be permanently secured internally so that normal movement of the leads will not cause strain, wear, or damage to the transistor die or enclosure.

3.2.2 Case Materials

Materials used for the transistor cases shall be corrosion resistant or shall be plated or treated to resist corrosion. After completion of all specified tests, the finish shall show no evidence of corrosion or degradation that could affect electrical or mechanical performance or reliability.

3.2.3 Fungus Resistance

External parts of the transistors shall be constructed of materials that are inherently non-nutrient to fungus.

3.2.4 Marking Methods

Each transistor shall be marked with the information required in 3.6 of this specification and 3.6 of the applicable detail procurement specification. All markings shall be permanent, legible, and complete at the end of all specified tests, and shall be insoluble in common cleaning solutions. Common cleaning solutions include, but are not limited to, trichloroethylene, freon, and methyl ethyl ketone. The markings shall be either electroetched or printed. Materials shall not be used which will interfere with the fine-leak hermeticity tests specified in this or the detail procurement specification.

3.3 Internal Physical Characteristics

The internal physical characteristics of the transistors shall be as specified herein and in 3.3 of the applicable detail procurement specification. The following general requirements shall apply:

3.3.1 Materials, Design, and Construction

When a definite material, design, or construction is not specified in the applicable detail procurement specification, the material, design, and construction used shall enable the transistor to meet all specified requirements. (See 1.6 herein.)

3.4 Environmental Compatibility[1/]

The transistors, while operating or nonoperating as specified, shall be capable of withstanding the following environmental requirements:

a. Vibration
b. Thermal vacuum
c. Acceleration
d. Temperature
e. Shock
f. Life (operation and storage)
g. Sterilization cycles
h. Acoustic noise
i. Radiation resistance

3.5 Manufacturing Controls

3.5.1 Manufacturing and Inspection Facilities

Manufacturing and manufacturing controls for NSL transistors shall be performed in facilities approved by the NASA prime contractor. The production line used by the part manufacturer for fabricating the NSL transistor will have been certified as eligible to supply transistors to this specification and the applicable detail procurement specification by the prime contractor prior to initiation of procurement. Failure by the part manufacturer to conform to the requirements of this specification or the applicable detail procurement specification shall be grounds for revocation of the line certification (see 6.1.5 herein).

3.5.2 In-Plant Surveillance

NASA-designated representatives may be assigned to the part manufacturer's plant to perform surveillance and monitoring functions in connection with the transistors furnished under this specification. The NASA-designated representatives shall be afforded controlled access to areas involved in the process and fabrication of the transistors. The applicable NASA-designated representatives shall be notified one week before any acceptance testing is to be performed. The NASA-designated representative shall retain the prerogative to monitor inspection and testing in connection with this specification. NASA, the prime contractor, and the procuring activity reserve the

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1/ The actual environmental conditions will be determined by the system or program requirements.

right to perform any of the inspections set forth in this specification or the applicable detail procurement specification, where such inspections are considered necessary to assure that parts and services conform to the prescribed requirements.

3.5.3 Manufacturing Flow Charts

The part manufacturer shall prepare an individual manufacturing flow chart for the NSL transistor controlled by the applicable detail procurement specification. This chart shall identify the production operations, identify in sequence the materials and processes used, and list the document number and revision of the documentation covering these materials and processes. The title, number, release date, and latest revision date of each associated document shall be shown. This chart shall specify each point or location at which an inspection operation is performed and which function is responsible for the inspection. The flow chart shall identify the individual documents that define the plan, sequence, and detailed acceptance criteria for performing all inspections and tests required herein and in the applicable detail procurement specification. The flow chart shall include applicable engineering procedures, process control documents, and process change notices.

3.5.4 Standardization of Design Practices and Processing Procedures

The part manufacturer shall maintain continuous standardization and control of design practices and processing procedures and formalize his results for use by his design, drafting, fabrication, and inspection personnel. The part manufacturer's product assurance organization shall be responsible for reviewing these standards for adequacy in meeting product assurance requirements of purchase orders and for monitoring and assuring that they are being followed. The part manufacturer shall review the specifications of all his subcontractors for compatibility with the requirements of this specification, and all specifications shall be submitted for inspection by NASA or its representatives upon request. Typical areas to be covered in this standardization system include:

a. Process specifications

b. Fabrication, assembly, and machining specifications

c. Drafting practice and drawing specifications.

3.5.5 Process Control Charts

Design and process control shall be monitored by the part manufacturer through control charts on appropriate product and process variables, tolerances, and other control techniques, as necessary.

3.5.6 Process Control Documentation

The part manufacturer shall completely document with specifications and procedures, the procurement of parts and materials, materials

inspection, the transistor manufacturing processes, and the inspections used to control these processes. The documentation shall include internal procedures for the control and revision of all documents. This documentation shall be available for review by the NASA designated representative and the prime contractor.

3.5.7 Design, Material, or Process Change Notification

A listing of all documentation defining the design, material, process, procedure, and control, showing the latest revision letter in effect at the time of manufacture of the procurement lot shall be provided to the NASA prime contractor. No change shall be made to these documents while there is an order in process without the part manufacturer completing the change notification form as shown in appendix A. (See 1.6 herein.)

3.5.8 Specification and Drawing Control

The part manufacturer shall adequately control the issue of new or revised process specifications, inspection procedures, and procurement specifications, and shall provide for the recall of obsolete issues. The specification control shall know the location of all operational issues of specifications. Specification revisions (and new issues) shall require approval by the appropriate levels of production, engineering, and product assurance management. Proprietary process or design specifications shall be handled in the same (or equivalent) formal manner as other specifications, although they need not be made available to the customer nor be given the same distribution as other specifications. However, they shall be identified on product flow charts by title and number. Specification control (or equivalent activity) shall have a record of issue locations and revision history.

Internal process, inspection, and other specifications shall show the customer revision status when customer drawings or specifications provided for contracts are referenced. When changes to customer specifications are received, the impact on active products shall be evaluated by comparison with the prior customer documents; they shall therefore be maintained in a controlled, known location.

3.5.9 Proprietary Processes and Procedures

Documents describing proprietary processes need not be made available to the procuring activity, but upon the specific request of this activity, an official of the part manufacturer shall show the procuring activity that the proprietary operations are completely defined and that the proper controls are specified.

3.5.10 Control of Procurement Sources

The part manufacturer shall exercise control over his sources of supply and contractors to assure the quality and reliability of purchased parts and materials, and shall maintain records of product performance of each sub-tier supplier. Chemical analyses and physical tests necessary to verify

that raw materials conform to design requirements shall be periodically conducted on samples randomly selected from raw material received. Test results shall be incorporated as part of the inspection records for the lot selected.

3.5.11 Part Manufacturer Receiving Inspection

Receiving Inspection shall operate under prescribed procedures and maintain a formal record system. A formal method of handling rejected material shall be in evidence. There shall be a segregation of accepted material, rejected material, and parts being held prior to final disposition by the Receiving Inspection function. The control procedures above shall be implemented for such items as packages, semiconductor material and other types of substrates, piece parts, solder preforms, wire, and pure chemicals.

3.5.12 Nonconforming Materials

The part manufacturer shall provide for the review, control, and disposition of nonconforming materials. Each nonconformance shall be reviewed, a disposition made by personnel vested with this responsibility, and positive corrective action taken to prevent recurrence of similar discrepancies. Pertinent drawings and documentation shall be changed or initiated as necessary.

3.5.13 Measuring and Test Equipment

The part manufacturer shall provide and maintain measuring and testing devices necessary to assure that transistors conform to technical requirements. These devices shall be calibrated against certified measurement standards which have known valid relationships to national standards at established periods to assure continued accuracy. The objective is to assure that inspection and test equipment is adjusted, replaced, or repaired before it becomes inaccurate. The calibration of measuring and testing equipment shall be in conformance with MIL-STD-750. The part manufacturer shall assure the use of only those subcontractors and sources of supply which depend on calibration systems that effectively control the accuracy of measuring and testing equipment.

3.5.14 Identification and Inventory Control

From the time of material receipt, through processing and completion of the transistors, material, parts, and finished products shall be handled and stored in such a way that the identity and quality of such materials will be preserved. All material shall be used on a first-in—first-out basis. Materials and parts shall be transferred and transported in containers or equipment and by methods that will adequately protect quality and identity.

Identification shall be at least a part number, lot number (and/or purchase order), quality status (evidence of acceptability), and operations completed. Rejected material or material awaiting nonconformance review shall be prominently marked, physically isolated from material awaiting inspection or accepted, and locked or otherwise controlled so as to positively prevent loss or substitution. Part numbers and lot numbers shall remain on

products or containers until identity is lost in the next higher level of assembly or batch or until the products are processed with other lots, so as to create a new lot number.

3.5.15 Workmanship

The transistors shall be processed in a manner to ensure freedom of defects and shall be manufactured in facilities that will ensure the proper cleanliness and uniformity. A workmanship program shall be in effect continuously for all personnel involved in the manufacture of transistors, and shall have readily available to operators, detailed written manufacturing procedures and appropriate visual aides for each operation. The methods utilized in handling, storing, and transporting the parts during processing shall minimize contamination and mechanical damage.

Workmanship standards shall be prepared and implemented by the part manufacturer on the basis of the requirements of this and the applicable detail procurement specification.

3.5.16 Internal Contamination

Where material that can introduce solder balls, gold flakes, weld splatter, or other similar contamination into the transistor is used in the manufacturing process, then the part manufacturer shall prepare and implement detailed procedures for process control and inspection to preclude the fabrication of transistors with such contamination. In this area, the process, process control, and inspection shall be continually evaluated by the part manufacturer, the prime contractor, or the designated representative of the NASA. Disapproval of the part manufacturer's process, process control, or inspection shall be cause for suspension of the part manufacturer's line certification until he has taken the proper corrective actions.

3.5.17 Inspection Equipment

Equipment used for inspection shall be recertified at intervals formally established to provide for calibration, replacement, or repair before the equipment becomes inaccurate.

3.6 Identification and Traceability

3.6.1 Maintenance of Traceability

Two-way traceability shall be maintained, that is, from transistor serial number to material acceptance records, and vice versa, from material lot to range of transistor serial numbers.

3.6.2 Marking Information

Each transistor shall be marked, where space permits, in the order of preference shown:

a. NSL part number

b. Serial number

c. Date code

d. Manufacturer's identification.

3.6.3 Date Code

The transistors shall be date-coded immediately after sealing is completed. The date code shall be a three-digit number. The first digit shall be the last number of the year, and the second and third digits shall be the numbers of the week (example: 849 is year 1968, week 49) of sealing.

3.6.4 Serialization

The transistors shall be serialized immediately after internal visual inspection and capping is completed. The serial number shall be a sequential five-digit number. For a given part number, the serial number shall be unique; that is, the part number together with the serial number shall identify one transistor. For each part number, the first serial number assigned shall be 00001, and subsequent serial numbers shall be consecutive within a lot and continue from lot to lot. The part manufacturer shall maintain records of assigned serial numbers so that manufacturing dates and inspection dates can be identified by the part number and a serial number. If a transistor or lot of transistors is rejected, the serial number for that transistor or lot shall not be assigned to another transistor or lot.

3.6.5 Procurement Lot

A procurement lot shall consist of all the parts procured under one order to one NSL detail procurement specification. Every effort shall be made by the part manufacturer to arrange that the parts in one procurement lot are as identical as possible. To the greatest extent possible, all the parts in a procurement lot shall be fabricated:

a. without interference or interruption of any kind, in the minimum time,

b. from the minimum number of diffusion batches,

c. from one lot of each material or part,

d. with unchanging processes, and

e. with a minimum turnover in personnel.

3.7 Product Assurance

3.7.1 Product Assurance Organization

The organization responsible for product assurance shall have access to management. If the product assurance organization is composed of a reliability and a quality assurance function, these shall both have direct access to management. Under no circumstances shall these organizations be under the manufacturing organization. The responsibility and authority assigned to each organization shall be defined and documented in a Product Assurance Plan. Management shall regularly review the status and adequacy of the product assurance program.

3.7.2 Product Assurance Plan

The part manufacturer shall provide a Product Assurance Plan in support of the procurement of NSL transistors for approval by the prime contractor. This plan shall document the product assurance activities with which the part manufacturer intends to support the NSL transistor procurement. The plan shall be submitted to and approved by the prime contractor prior to fabrication. The plan shall identify tasks, and for each task: assignments of responsibility, schedule, controlling procedures, end-items, and criteria for completion. The information in the plan shall not be considered proprietary. The plan shall contain:

a. Part manufacturer's organizational chart.

b. Description of failure analysis capabilities and planning for support of NSL procurements.

c. Description of product-assurance-oriented training, including identification of specific scheduling.

d. Manufacturing flow chart.

e. Description of lot control plan for traceability of materials and processes throughout the manufacturing cycle to and including transistor identification by serial number.

f. Description of procedures and planning for certification of inspectors, fabrication personnel, and test personnel.

g. Description of procedures and planning for calibration and maintenance of test and fabrication equipment.

4. TEST REQUIREMENTS

4.1 Controls Required Over Testing

4.1.1 Facilities

Acceptance testing and qualification testing required by 4.3 and 4.4 of this specification and 4.3 and 4.4 of the applicable detail procurement specification shall be performed in facilities approved by the prime contractor and by the designated representative of the NASA.

4.1.2 Measuring and Test Equipment

The part manufacturer shall provide and maintain measuring and testing devices necessary to assure that transistors conform to the acceptance and qualification test criteria. These devices shall be maintained as required in 3.7 of this specification.

4.1.3 Standard Ambient Test Conditions

Unless otherwise specified, all tests, measurements, and examinations shall be performed under the standard temperature, pressure, and humidity conditions specified in MIL-STD-750.

4.1.4 Test Procedures

The part manufacturer shall prepare, and conform to, test procedures to implement the requirements of 4.3 and 4.4 of this specification and 4.3 and 4.4 of the applicable detail procurement specification. These procedures shall be approved by the prime contractor and by the designated representative of the NASA prior to testing. The procedures shall include, as a minimum, a description of the test equipment, data recording equipment, test sequence, descriptive diagrams, a step-by-step procedure of parameter and environmental testing, acceptance and rejection criteria, part marking, computer-card data format, data sheets, and inspection stamp requirements. In cases where complex automatic test equipment is utilized, the operating manual shall be referenced and be available for review. Test methods covered by military test specifications need only be referenced; however, where a choice of alternative conditions or test levels is required to implement, these shall be defined.

4.1.5 Procedure in Case of Test Equipment Failure or Operator Error

Any part failing as a result of a verified test equipment failure or operator error shall be removed or replaced depending upon schedule, by another part from the same procurement lot. Replacement devices shall be subjected to all required tests.

4.1.6 Test Records

All test measurements and data shall be recorded. (See 5.1.3, 5.1.4, and 5.2 herein.)

4.2 Test Methods and Criteria

In tables I and II of this specification, the column labeled "Methods and Criteria" identifies the sections which define the test methods required for each line item, and the criteria for satisfactory completion of each line item. Test methods and criteria for satisfactory completion, as called out by tables I and II, are provided in the subsections below. These subsections apply to the extent they are called out in table I or II.

4.2.1 Internal Visual

Internal visual examination shall be performed in accordance with appendix C of this specification immediately before the transistors are sealed. (The transistors shall be suitably protected from contamination until sealed.) The examination shall be performed in a controlled clean atmosphere by qualified personnel in the part manufacturer's product assurance or quality assurance department. The transistors shall meet the requirements specified in 3.3 and appendix C of this specification and in 3.3 of the applicable detail procurement specification.

4.2.2 Physical Dimensions

The physical dimensions of the transistors shall be checked in accordance with method 2066 of MIL-STD-750. The dimensions shall be measured with equipment appropriate to verify their conformance to the dimensional figure or figures specified in 3.2 of the applicable detail procurement specification.

4.2.3 External Visual

External visual examination shall be performed in accordance with method 2071 of MIL-STD-750 and the requirements of 3.2 of this specification and 3.2 of the applicable detail procurement specification. There shall be no visible evidence of corrosion, contamination, or damage such as grossly bent or broken leads, defective or damaged plating, or other conditions which could interfere with the application or operation of the transistor. All marking shall be legible and complete.

4.2.4 Electrical Characteristics

Electrical tests shall be performed on the transistors in accordance with the test conditions, methods and parameter limits specified in table II of the applicable detail procurement specification. The transistors shall meet the specified requirements.

4.2.5 High-Temperature Storage

The transistors shall be subjected to high-temperature storage for 48 ±2 hours at the maximum rated high storage temperature specified in table I of the applicable detail procurement specification. There shall be no mechanical damage after completion of the test.

4.2.6 Thermal Shock

The transistors shall be subjected to thermal shock in accordance with method 107 of MIL-STD-202. The temperature extremes shall be the maximum rated low and high storage temperatures specified in table I of the applicable detail procurement specification. The transistors shall remain 15 minutes ±30 seconds at each extreme, and the maximum transfer time shall be 5 minutes. There shall be no mechanical damage or evidence of harmful corrosion after completion of the test.

4.2.7 Reverse-Bias High-Temperature Life

When specified therein, all transistors shall be subjected to the test conditions specified in table III of the applicable detail procurement specification. The bias shall remain applied until the temperature is reduced to specification ambient conditions. The leakage-current parameter specified in the applicable detail procurement specification shall not exceed the specified limit.

4.2.8 Constant Acceleration (for Acceptance Test)

The transistors shall be subjected to a constant acceleration of 20,000 g ±10% for a period of one minute ±5 seconds in the Y_1 orientation, in accordance with method 2006 of MIL-STD-750. There shall be no mechanical damage after completion of the test.

4.2.9 Mechanical Shock (for Acceptance Test)

The transistors shall be rigidly mounted with suitable protection for the leads and shall then be subjected to 10 blows, each with a peak acceleration of 1500 g and a duration of 0.5 (+.25, -0) millisecond, applied perpendicular to the base of the die, in accordance with method 2016 of MIL-STD-750. There shall be no mechanical damage after completion of the test.

4.2.10 Hermeticity

The transistors shall be subjected to the fine leak and gross leak tests below, in the following sequence:

4.2.10.1 Fine-Seal Leak

The transistors shall be subjected to a leakage test in accordance with method 112 of MIL-STD-202, test condition C, procedure IIIa or IIIb, except that the gross-leak portion of the test shall conform to 4.2.10.2 herein.

Conditions for Procedure IIIa - The transistors shall be placed in a sealed chamber, pressurized to 50 psig minimum with helium gas, for a minimum of 4 hours. The transistors shall then be removed from the chamber and within 30 minutes shall be subjected to a helium leak detection test. Transistors shall be rejected that exhibit a leak rate greater than

1×10^{-8} cubic centimeter of helium per second when measured at a differential pressure of one atmosphere.

Conditions for Procedure IIIb - The transistors shall be placed in a sealed chamber which shall be pressurized to 180 psig minimum with Krypton 85 tracer in a nitrogen solution for a minimum of 30 minutes. Within 4 hours after evacuation of the chamber, the transistors shall be tested with a counter capable of detecting leakage at the rate of 1×10^{-8} cubic centimeter per second.

4.2.10.2 Gross-Seal Leak

Each transistor shall be tested for gross leaks by immersing in noncorrosive ethylene glycol at approximately 150° C for a minimum of 15 seconds and observing for bubbles. All devices that bubble shall be rejected.

4.2.11 Burn-In and Parameter Drift Measurements

The transistors shall be operated in accordance with method 1026 of MIL-STD-750 for a period of 500 ±10 hours under the conditions specified in table III of the applicable detail procurement specification. Unless otherwise specified therein, these conditions shall provide for the maximum rated junction temperature. At the start, at 250 ±10 hours, and at 500 ±10 hours, the drift-measurement parameters specified in table III of the applicable detail procurement specification shall be measured and shall not exceed the limits and drift criteria specified therein.

4.2.12 X-Ray

Each transistor shall be photographed in three mutually perpendicular planes and examined as specified in appendix B of this specification. The transistors shall meet the requirements specified in appendix B.

4.2.13 Electrical End Points

The electrical end-point parameters listed in table IV of the applicable detail procurement specification shall be measured at the temperature specified therein. The parametric change (delta) shall be determined by comparison with the initial end-point measurements. The transistors shall meet the limits specified in table IV of the applicable detail procurement specification.

4.2.14 Vibration, Variable Frequency

The transistors shall be tested in accordance with method 2056 of MIL-STD-750, except that they shall be subjected to a constant rms acceleration of 100 g with a frequency range from 20 to 2000 Hz. The sweep rate shall be 1/2 octave per minute and the displacement shall be limited to 0.6 inch double amplitude between 20 and 100 Hz. The transistors shall be subjected to two sweeps up and down along each of three mutually perpendicular

axes (X, Y, and Z). There shall be no mechanical damage after completion of the test.

4.2.15 Constant Acceleration (for Qualification Test)

The transistors shall be subjected to a constant acceleration of 30,000 g ±10% for a period of one minute ±5 seconds in all six orientations (X_1, X_2, Y_1, Y_2, Z_1, and Z_2), in accordance with method 2006 of MIL-STD-750. There shall be no mechanical damage after completion of the test.

4.2.16 Mechanical Shock (for Qualification Test)

The transistors shall be rigidly mounted with suitable protection for the leads and shall then be subjected to 5 blows, each with a peak acceleration of 1500 g and a duration of 0.5 (+.25, -0) millisecond, applied in all six orientations (X_1, X_2, Y_1, Y_2, Z_1, and Z_2), in accordance with method 2016 of MIL-STD-750. There shall be no mechanical damage after completion of the test.

4.2.17 Moisture Resistance

The transistors shall be tested in accordance with method 1021 of MIL-STD-750. There shall be no damage after completion of the test. At least 90 percent of the surfaces shall be unaffected by moisture and show no evidence of harmful corrosion.

4.2.18 Thermal Resistance

The θ_{J-A} thermal characteristics of the transistors shall be tested in accordance with method 3132 of MIL-STD-750. The transistors shall be mounted in free air with no heat sink. The test conditions shall be as specified in table IV of the applicable detail procurement specification. The specified limit shall not be exceeded.

4.2.19 Solderability

The transistors shall be tested for solderability in accordance with method 2026 of MIL-STD-750. The following details shall apply:

a. Number of terminations of each part to be tested: All.

b. Depth of immersion in flux and solder: The leads shall be immersed to within 1/8 inch of the weld, seal, or case, as applicable.

c. Examination with 7X magnification: The transistors shall be examined for wetting and coverage and shall meet the criteria specified.

4.2.20 Terminal Strength

The transistors shall be tested in accordance with method 2036 of MIL-STD-750, test condition E. The following details shall apply:

a. Weight to be attached to lead: 4 ±0.5 ounces.

b. Number of arcs: Three.

c. Examination with 7X magnification: The transistors shall be examined for glass fracture or broken lead and shall meet the criteria specified.

4.2.21 Solvent Resistance

The transistors shall be tested in accordance with method 215 of MIL-STD-202. After completion of the test there shall be no physical or mechanical damage or obliteration of the marking.

4.2.22 Operation Life and Parameter Drift Measurements

The transistors shall be operated in accordance with method 1026 of MIL-STD-750 for a period of 2000 ±24 hours, under the conditions specified in table IV of the applicable detail procurement specification. Unless otherwise specified therein, these conditions shall provide for the maximum rated junction temperature At the start, at 500 ±10 hours, 1000 ±10 hours, 1500 ±24 hours, and at 2000 ±24 hours, the drift-measurement parameters specified in table IV of the applicable detail procurement specification shall be measured and shall not exceed the limits and drift criteria specified therein.

4.2.23 Construction Analysis

The construction analysis shall consist of the examinations described in the following subsections (in the order listed). There shall be no evidence of improper construction, processing, or use of materials.

4.2.23.1 X-Ray

The transistors shall be X-rayed in accordance with 4.2.12 herein and shall meet the criteria specified.

4.2.23.2 Physical Dimensions

The physical dimensions of the transistors shall be measured in accordance with 4.2.2 herein and shall conform to the criteria specified.

4.2.23.3 External Visual

The transistors shall be examined in accordance with 4.2.3 herein and shall meet the criteria specified.

4.2.23.4 Transistor Autopsy

The package shall be opened by a technique that does not damage or contaminate the internal structure or in any way impair the ability to observe defects in the devices or the effects of preceding test exposures.

4.2.23.5 Internal Visual

The transistors shall be examined in accordance with 4.2.1 herein and shall meet the criteria specified. Each transistor shall be fully described, by means of diagrams and photographs, as to product marking, coating, all dimensions of the package, leads, sealing, bonds, and general construction. Topographic maps of the semiconductor die shall be constructed showing a correlation between the various elements on the topographic map and the schematic elements. Either an exploded or a cross-sectional view shall be drawn showing the part construction, materials, type of bonds, dimensions, and sealing surfaces.

4.3 Acceptance Test

4.3.1 General Requirements for Part Acceptance Testing

Part acceptance tests are required to be:

a. Performed by the part manufacturer for each procurement lot.

b. Conducted after successful completion of product requirements for the procurement lot in conformance with section 3 of this specification and section 3 of the applicable detail procurement specification.

c. Performed on all parts in the procurement lot which have passed manufacturing inspection.

d. In conformance with the requirements of 4.3 of this specification and 4.3 of the applicable detail procurement specification.

4.3.2 Acceptance Test Requirements

The acceptance test shall be conducted in conformance with figure 1 and table I herein. Any part failing to meet all the criteria in table I shall be rejected.

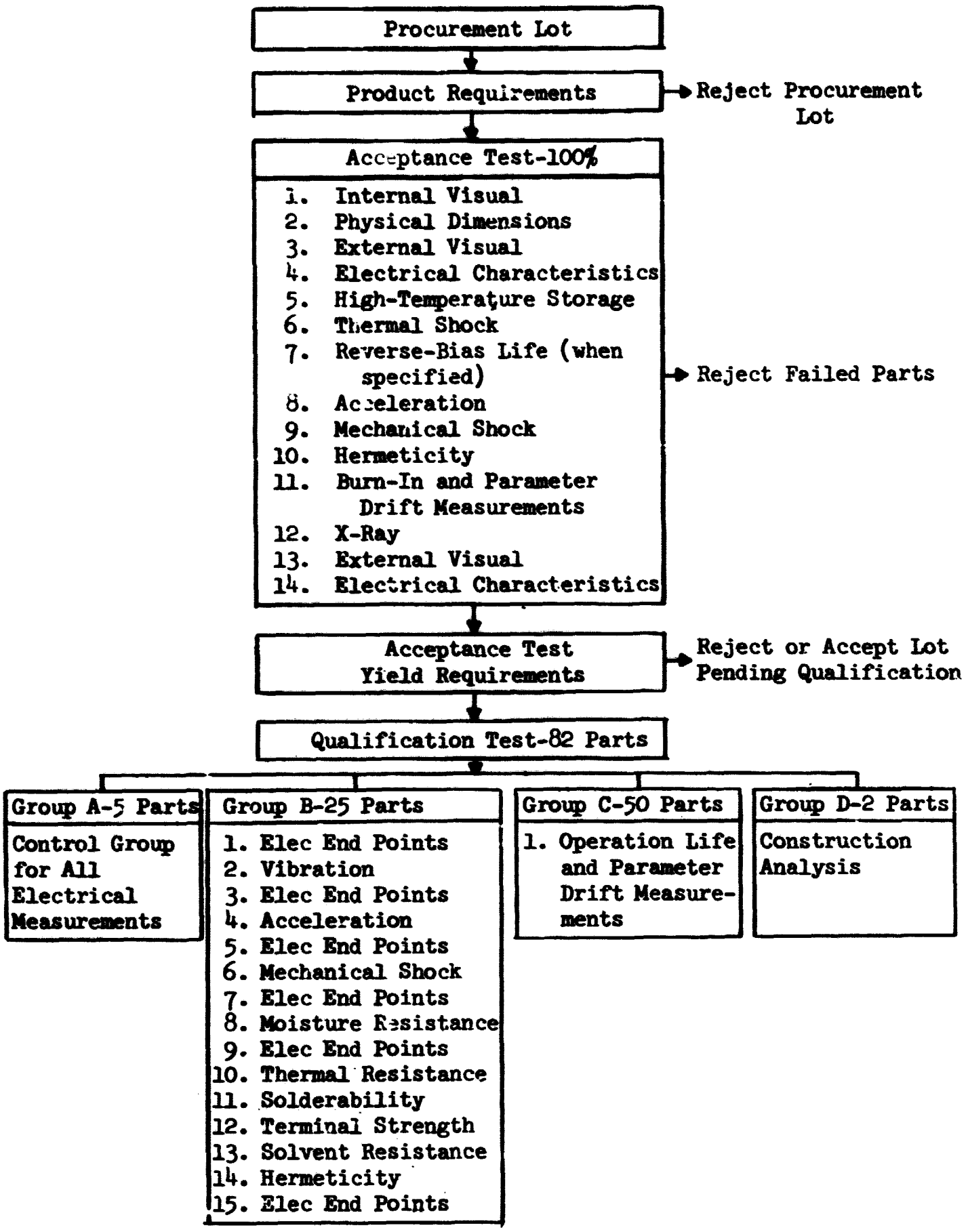

FIGURE 1.- TEST REQUIREMENTS

TABLE I.- ACCEPTANCE TEST

Quantity	Test	Max. Percent Defectives Acceptable	Methods and Criteria	
			Section in This Spec	Section in Applicable Detail Procurement Spec
100%	1. Internal Visual	--	4.2.1	3.3
100%	2. Physical Dimensions	--	4.2.2	3.2
100%	3. External Visual	--	4.2.3	3.2
100%	4. Electrical Characteristics	--	4.2.4	Table II
100%	5. High-Temperature Storage	25%	4.2.5	Table I
100%	6. Thermal Shock		4.2.6	Table I
100%	7. Reverse-Bias Life (when specified)		4.2.7	Table III
100%	8. Acceleration		4.2.8	--
100%	9. Mechanical Shock		4.2.9	--
100%	10. Hermeticity		4.2.10	--
100%	11. Burn-In and Parameter Drift Measurements	5%	4.2.11	Table III
100%	12. X-Ray	5%	4.2.12	--
100%	13. External Visual	5%	4.2.3	3.2
100%	14. Electrical Characteristics	5%	4.2.4	Table II

4.3.3 Acceptance-Test Yield Requirements

If the "maximum percent defectives acceptable" limit specified in table I is exceeded for one or more line items, or if the total part rejects during steps 5 through 14 of the acceptance test exceeds 25 percent of the procurement lot, then this may be grounds for failure and rejection of the entire procurement lot. In either such event, the final acceptance or rejection of the procurement lot shall be made by the prime contractor with approval by the designated representative of the NASA.

4.4 Qualification Test

4.4.1 General Requirements for Part Qualification Testing

Part qualification tests are required to be:

a. Performed by the part manufacturer for each procurement lot.

b. Performed on 82 parts which have been selected in approximately equally spaced intervals throughout the production lot, and have pas the acceptance test in conformance with 4.3 of this specification and 4.3 o the applicable detail procurement specification.

c. In conformance with the requirements of 4.4 of this specification and 4.4 of the applicable detail procurement specification.

4.4.2 Qualification Test Requirements

The qualification test shall be conducted in conformance with figure 1 and table II. Any failure, during part qualification testing, to meet all the criteria in table II may be grounds for failure of the qualification test. In the event of any such failure, the final acceptance or rejection of the procurement lot shall be made by the prime contractor with approval by the designated representative of the NASA.

4.4.2.1 Control Group for Electrical Measurements

Five transistors (group A) shall serve as the control group for all electrical measurements called for in the qualification test of table II. Group A shall be electrically measured before any electrical measurements are performed for any group B or group C tests. Each time a group B or group C electrical test is performed, the five parts in group A shall be subjected to the same electrical test, using the same equipment and procedures.

TABLE II.- QUALIFICATION TEST

Test Group	Quantity	Test	Methods and Criteria	
			Section in This Spec	Section in Applicable Detail Procurement Spec
A	5	Control Group for Electrical Measurements	4.4.2.1	Table II
B	25	1. Electrical End Points (Initial)	4.2.13	Table IV
		2. Vibration	4.2.14	--
		3. Electrical End Points	4.2.13	Table IV
		4. Acceleration	4.2.15	--
		5. Electrical End Points	4.2.13	Table IV
		6. Mechanical Shock	4.2.16	--
		7. Electrical End Points	4.2.13	Table IV
		8. Moisture Resistance	4.2.17	--
		9. Electrical End Points	4.2.13	Table IV
		10. Thermal Resistance	4.2.18	Table IV
		11. Solderability	4.2.19	--
		12. Terminal Strength	4.2.20	--
		13. Solvent Resistance	4.2.21	--
		14. Hermeticity	4.2.10	--
		15. Electrical End Points	4.2.13	Table IV
C	50	1. Operation Life and Parameter Drift Measurements	4.2.22	Table IV
D	2	Construction Analysis	4.2.23	3.2, 3.3

5. DOCUMENTATION REQUIREMENTS

5.1 Documentation Required with Delivery

For all transistors procured under this specification, the documents defined in the subsections below shall be delivered with the transistors to the procuring activity. In addition, a copy of each shall be forwarded to the prime contractor. All such documentation (including data records) shall be contained on sheets 8-1/2 by 11 inches, or standard electronic accounting machine printout. Each of the documents required below shall be signed by the part manufacturer's authorized representative and by his product assurance manager (or quality manager).

5.1.1 Certificate of Compliance

After all the requirements of this specification and the applicable detail procurement specification have been fulfilled and verified, the part manufacturer shall so state in a "Certificate of Compliance."

5.1.2 Fabrication Record Report

A "Fabrication Record Report" shall be prepared by the part manufacturer, defining for the procurement lot:

a. A copy of all nonconformances and waiver/deviations.

b. A copy of all change notification forms submitted (see 1.6 herein).

c. A correlation (tabulation) of individual transistor serial numbers and date codes.

d. A copy of the manufacturing flow chart (see 3.5.3 herein).

5.1.3 Acceptance Test Report

An "Acceptance Test Report" shall be prepared, containing for the procurement lot:

a. All the test data required under 4.3 of this specification and 4.3 of the applicable detail procurement specification.

b. A summary of the acceptance test results, including an itemization by serial number of all failures in each test group and a description of the failed parameters of each failed part.

5.1.4 Qualification Test Report

A "Qualification Test Report" shall be prepared, containing for the procurement lot:

a. All the test data required under 4.4 of this specification and 4.4 of the applicable detail procurement specification.

b. A summary of the qualification test results, including a full description of any test failures and identification of failed parts by serial number.

5.2 Record Retention Required

For all the transistors procured under this specification, the records and documents defined below shall be retained by the part manufacturer, and kept complete and available for a minimum of 5 years after completion of the procurement lot. These records and documents shall be available to the prime contractor and the NASA-designated representative. These requirements apply to both accepted and rejected procurement lots. Where data is recorded, the film, tape, or other media shall be identified with the requirements of this specification or the applicable detail procurement specification. Inspection and test records shall include the NSL part number, part serial numbers, procurement lot number, date code, inspection or test number, and the inspectors' and test operators' identity. The intent is that this data and information should be traceable to the specific part to which they apply.

5.2.1 Copy of Delivery Documentation

A copy of the documentation required for delivery under 5.1 above shall also be retained.

5.2.2 Test Procedures

Procedures for acceptance testing and qualification testing, as required in 4.1.4 herein, shall be retained.

5.2.3 Radiographs

One complete set of radiographs for the procurement lot shall be retained. Each radiograph shall carry a serial number or code letters to identify the radiograph with the specific part shown.

5.2.4 Manufacturing Controls

The manufacturing control records and documents required under 3.5 herein shall be retained.

5.2.5 Traceability

Traceability shall be maintained in conformance to 3.6.1 herein.

5.2.6 Serialization

The records of assigned serial numbers shall be maintained as specified in 3.6.4 herein.

5.2.7 Product Assurance

The product assurance documentation required under 3.7 herein shall be retained.

6. PARTS DISPOSITION

6.1 Disposition of Parts

6.1.1 Acceptable Parts

Parts which have passed the requirements and criteria for acceptance test specified in 4.3 of this specification and 4.3 of the applicable detail procurement specification shall be impounded and placed in bonded storage to await (a) the satisfactory completion of acceptance testing by the entire procurement lot, and (b) the satisfactory completion of qualification testing. Upon satisfactory completion of these two events, the parts shall be packaged and shipped as described in 6.2 and 6.3 herein.

6.1.2 Bonded Storage

The bonded storage area shall provide physical protection from the environment at a room temperature of 25° ±10° C and humidity of 70 percent or less. Transistors stored in the bonded area for more than 6 months shall require satisfactory re-test of the electrical characteristics measurements specified in 4.2.4 herein. Transistors impounded and stored in the controlled storage area shall be removed only for shipment. Transistors shall be removed only under the surveillance of the part manufacturer's product assurance or quality assurance personnel. The transistors, on first entering bonded storage, shall be contained in the individual containers defined in 6.2.1 herein, and except for possible re-test, the transistors shall not be removed from these containers until after delivery.

6.1.3 Disposition of Failed Parts

Transistors that fail during the acceptance or qualification test shall be removed from the lot to be shipped, clearly marked, and retained by the part manufacturer for a minimum of 5 years. Catastrophic failures in the acceptance test, and all failures during the qualification test, shall be subjected to failure analysis. Transistors that are rejected by the prime contractor or any subcontractors for nonconformance and returned to the part manufacturer shall not be resubmitted without prior written approval of the prime contractor and the designated representative of the NASA.

6.1.4 Qualification Samples

Upon satisfactory completion of the qualification test to the requirements of 4.4 of this specification and 4.4 of the applicable detail procurement specification, the qualification sample transistors shall be clearly marked, packaged separately, and delivered to the prime contractor. The individual containers for this application shall be marked as required in 6.2.1 herein, and with the additional identification "QUALIFICATION SAMPLES - NOT FOR FLIGHT USE." This additional information shall also be carried on the shipping container required in 6.2.2 herein.

6.1.4.1 Control Group Samples

The individual containers for the five transistors serving as the control group (see 4.4.2.1 herein) shall be marked with the additional identification "CONTROL GROUP". These parts shall be retained by the part manufacturer for 5 years after completion of the qualification test.

6.1.5 Rejection of Procurement Lot

Any of the conditions listed below may be grounds for the failure and rejection of the entire procurement lot; in such an event, the final acceptance or rejection of the procurement lot shall be made by the prime contractor with approval by the designated representative of the NASA:

a. Change by the part manufacturer in material, design, construction, or process control for the NSL transistor after negotiation and prior to completion of the procurement.

b. Failure to respond to the change notification requirements of 1.6 herein.

c. Failure to successfully complete product requirements for the procurement lot, as defined in section 3 of this specification and/or section 3 of the applicable detail procurement specification.

d. Failure to meet the acceptance-test yield requirements of 4.3.3 herein.

e. Failure of the qualification test as defined in 4.4.2 herein.

f. Nonconformance to the requirements of this specification or the applicable detail procurement specification.

6.2 Packaging of Parts for Delivery

6.2.1 Individual Containers

The lowest level of packaging of the transistors shall have the following characteristics:

a. The individual transistors shall be supported by the case, with the terminals free and protected, in a manner to provide maximum protection from shock and vibration during transit and handling.

b. The parts shall be individually packaged in separate or separable containers, or several to a container provided the parts are isolated from each other within the overall container.

c. The individual containers shall provide full protection from dust, humidity, or gaseous contamination. Placing each individual container in sealed polyethylene bags is preferred.

d. The individual container shall have one or more transparent surfaces to permit visual inspection of the contents and part marking.

e. The individual containers shall be rigid so as to prevent the movement of parts within the container.

f. Each individual container shall be marked with the following information:

Part manufacturer's name
NSL part number (e.g., NSL-401/3)
Lot date code (see 3.6.3 herein)
Serial number (see 3.6.4 herein)
Purchase order number.

g. Marking on the individual container shall conform to the legibility requirement of MIL-STD-129. Printing or stamping may be used, and all information shall be legible on the outside of the container.

h. Parts which may be damaged by electromagnetic or electrostatic effects shall be completely enclosed in a nonmagnetic electrical conducting material, such as lead or aluminum foil. In this event, the case transparency requirements of (d) above do not apply.

6.2.2 Shipping Containers

The individual containers shall be packed in shipping containers of the type, size, and kind commonly used for the purpose. Shipping containers shall comply with the Uniform Freight Classification Rules or regulations of other carriers as applicable to the mode of transportation employed. Individual containers shall be packed within the shipping container in a manner to provide maximum protection from shock, vibration, and weather during transit; and in the order of ascending serial numbers or groups of serial numbers to facilitate and minimize handling subsequent to delivery.

6.2.3 Marking of Shipping Containers

Each shipping container shall be marked with the part manufacturer's name, NSL part number, lot date code, and purchase order number. Each shipping container shall be marked on each surface with the following legend in bold letters: "FRAGILE - NASA SPECIAL LONG-LIFE PARTS - TO BE OPENED BY AUTHORIZED PERSONNEL ONLY."

6.3 Delivery of Parts

For transistors procured under this specification, all the transistors in the procurement lot (defined in 3.6.5 of this specification) shall be

delivered to one address; this address shall be as defined in the procurement order. The shipping containers shall be delivered in the manner which, under the given circumstances, will result in the minimum exposure to shock, vibration, weather, delay, extremes of any kind, or unexpected exigencies. The receiving activity and the prime contractor (if different) shall be notified of the means and time of delivery. If necessary, the part manufacturer shall expedite any problems in transit.

7. ABBREVIATIONS, SYMBOLS, AND DEFINITIONS

7.1 MIL-S-19500 Terms, Abbreviations, and Symbols

Except as indicated in 7.2 below, the terms used herein and in the detail procurement specifications are defined in appendix A, and the abbreviations and symbols are defined in appendix B of MIL-S-19500.

7.2 Definitions of Additional Abbreviations and Symbols

Abbreviations and symbols not covered in MIL-S-19500 are defined below. Other abbreviations and symbols, when used, are defined in the applicable detail procurement specification.

7.2.1 Bipolar Transistors

C_{te}	Emitter transition capacitance
$h_{FE(inv)}$	Inverted static forward-current transfer ratio (same as h_{FE}, except that the transistor is inverted)
P_{in}	Input power
P_{out}	Output power
η (eta)	Collector efficiency, defined as $\frac{\text{rf power out}}{\text{dc power in}}$
Q_s	Stored charge
$r_b'C_c$	Collector-to-base time constant
$r_{ec}(on)$	On-state series resistance (the ratio of ac collector voltage to ac collector current)
$V_{CE}(sus)$	Collector-to-emitter sustaining voltage, open base, measured at a current where the breakdown voltage is a minimum
$V_{CER}(sus)$	Collector-to-emitter sustaining voltage, resistance return, measured at a current where the breakdown voltage is a minimum

7.2.2 Transistor Matched Sets

h_{FE_A}	Forward current transfer ratio, condition A. (Analogous symbols h_{FE_B}, h_{FE_C}, etc., represent conditions B, C, etc.)
$\frac{h_{FE_1}}{h_{FE_2}}$	Matching ratio of forward-current transfer ratios (each side is measured in accordance with MIL-STD-750, method 3076). The lowest of the two h_{FE} measurements is recorded as h_{FE_1} (not necessarily h_{FE} of side 1).
$\lvert V_{BE_2} - V_{BE_1} \rvert$	Absolute value of the difference in base-to-emitter voltages (each side is measured in accordance with MIL-STD-750, method 3026). V_{BE_1} is not necessarily V_{BE} of side 1.
$\frac{\Delta \lvert V_{BE_2} - V_{BE_1} \rvert}{\Delta T_A}$	Change in base-to-emitter voltage differential over the specified temperature range

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REVISION RECORD

REV	AUTHORITY	DESCRIPTION	RELEASE	
			DATE	APPROVAL

APPENDIX A

CHANGE NOTIFICATION

Document (Drawing, Process Specification, Procurement Specification, etc.)

Document Number _____

Revision Change from _____ to _____

Document Title _____

Description of Change _____

_____

_____

_____

_____

_____

Effect of Change on Form, Fit, Function, or Reliability _____

_____

_____

_____

_____

_____

Reason for Change _____

_____

_____

_____

_____

_____

Effectivity Date of Change _____

_____

Evaluation of Change _____

_____

_____

_____

APPENDIX B

X-RAY INSPECTION

10. SCOPE

10.1 This appendix establishes the requirements, test conditions, and methods for X-ray inspection of transistors for verification of physical attributes.

20. TEST METHODS AND CRITERIA

20.1 Acceptance Criteria

Each transistor supplied shall be radiographically inspected in accordance with the test conditions and methods of this appendix and shall meet the criteria specified.

20.2 Abnormality of Construction

Acceptable X-ray lots shall be of a homogeneous construction. Construction shall be as specified in the applicable detail procurement specification, and parts deviating from the specified construction shall be rejected.

20.3 Examination

The transistor examination shall include, but not be limited to, inspection for foreign particles, solder splash, proper bond of lead to semiconductor element and lead to terminal post, and proper semiconductor-element mounting. The transistors shall also be inspected for high-reliability construction and workmanship.

20.3.1 Element Support Posts

Element support posts shall not be bent more than 15 degrees from the vertical and shall be uniform in length and construction.

20.3.2 Lead Wire

The lead wire shall not extend beyond the post by a distance greater than twice the diameter of the wire. Lead wires shall not be pulled tight unless specifically designed in this manner, such as transistors using clips or rigid interconnection leads. However, there shall be no loops or excessive bends in the lead wire. Any bends or curves in the lead wire shall not extend beyond the top of the post more than twice the diameter of the lead wire. (See figures B-1 through B-6.)

20.3.3 Semiconductor Element Mounting

The semiconductor element shall be mounted and bonded so that it is not tilted more than 10 degrees from the normal mounting surface. Where the bonding agent accumulates around the perimeter of the semiconductor element and touches the side of the semiconductor element, it shall not accumulate to a thickness greater than the thickness of the semiconductor element (see figure B-7). Where the bonding agent is built up but is not touching the semiconductor element, the buildup shall not be greater than twice the thickness of the semiconductor element.

20.3.4 Extraneous Material

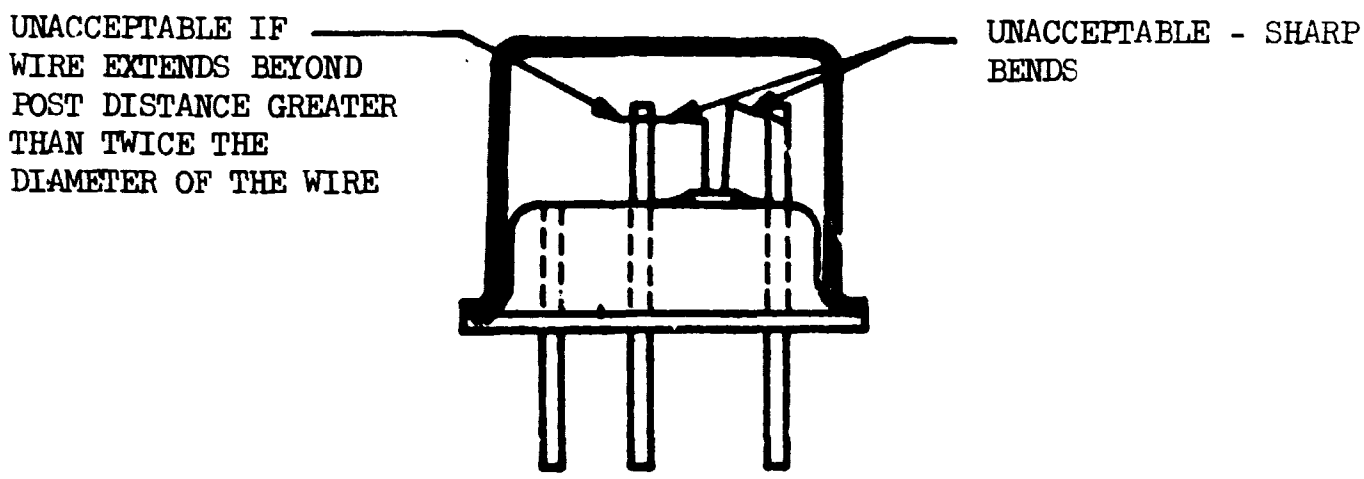
There shall be no visible extraneous material 0.001 inch or larger in the major dimension. Loose bonding material shall be considered extraneous material. Excessive (but not loose) bonding material shall not be considered extraneous unless it fails to meet the requirements of 20.3.3 (see figure B-7), or unless the accumulation of bonding material is in the pedestal form (see figure B-3).

20.3.5 Clearance

Acceptable transistors shall exhibit adequate internal clearances. The minimum distance between electrical connections on the post (or the post proper) and the nearest point on the case or header, as well as the minimum distance between the lead wire and the case or header, shall be equal to the diameter of the element post proper (except for the short distance between the lead and header in the vicinity of the bond of the lead to the semiconductor element). In transistors that have the semiconductor-element mount vertical, the minimum clearance shall be 0.002 inch between the semiconductor-element mount and the header, and between the semiconductor-element mount and the case (see figure B-8).

20.3.6 Extra Wires

There shall be no wires present other than those connecting specific areas of the transistor semiconductor element to the external leads, except where the design of the transistor calls for the use of such additional wires.



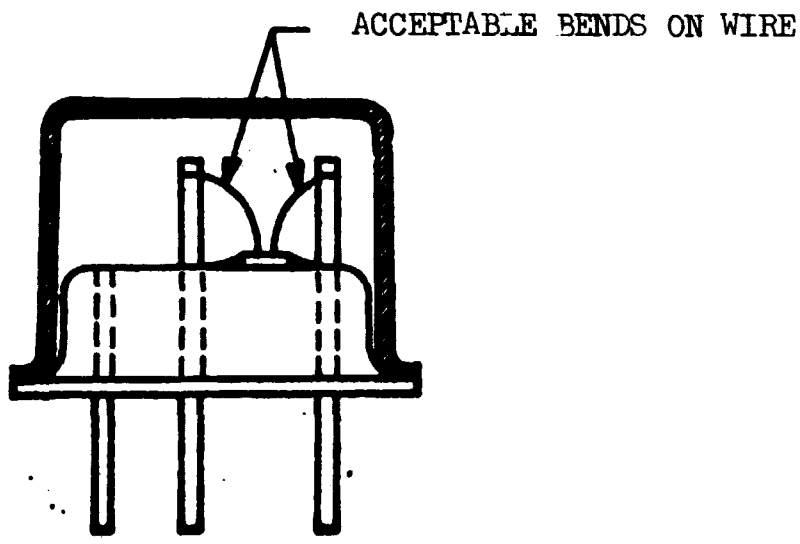
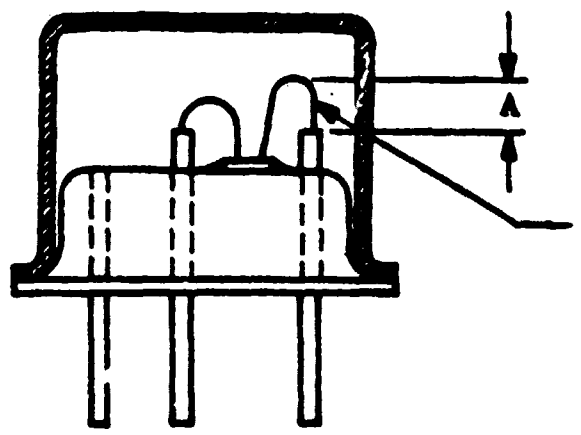
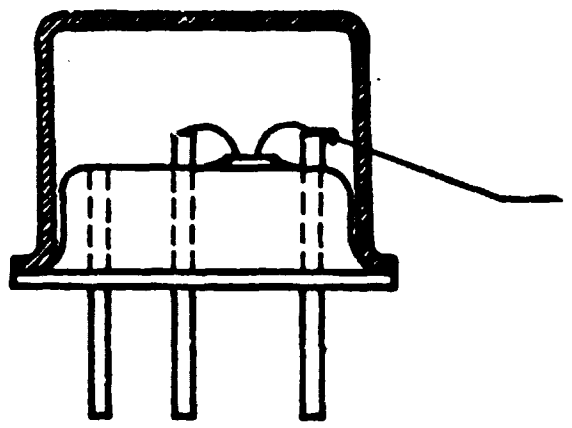


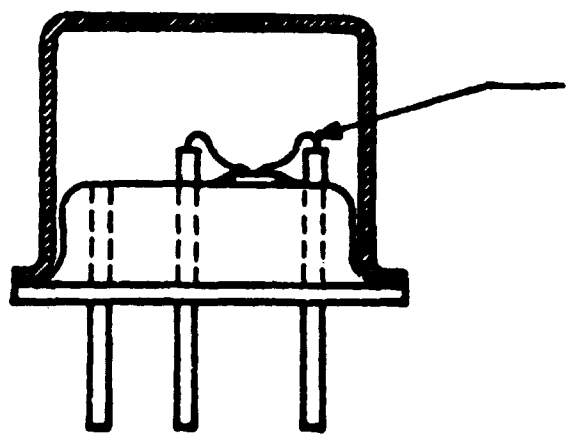
FIGURE B-1. ACCEPTABLE AND UNACCEPTABLE BENDS ON INTERNAL LEADS.



UNACCEPTABLE IF DISTANCE A EXCEEDS TWO TIMES DIAMETER OF WIRE CONNECTING POST TO SEMICONDUCTOR ELEMENT (APPROX 0.005 INCH)



ACCEPTABLE



UNACCEPTABLE - WIRES SAG TOO MUCH AND TOO CLOSE TO SEMI-CONDUCTOR ELEMENT

FIGURE B-2. ACCEPTABLE AND UNACCEPTABLE BENT OF SAGGING INTERNAL LEADS.

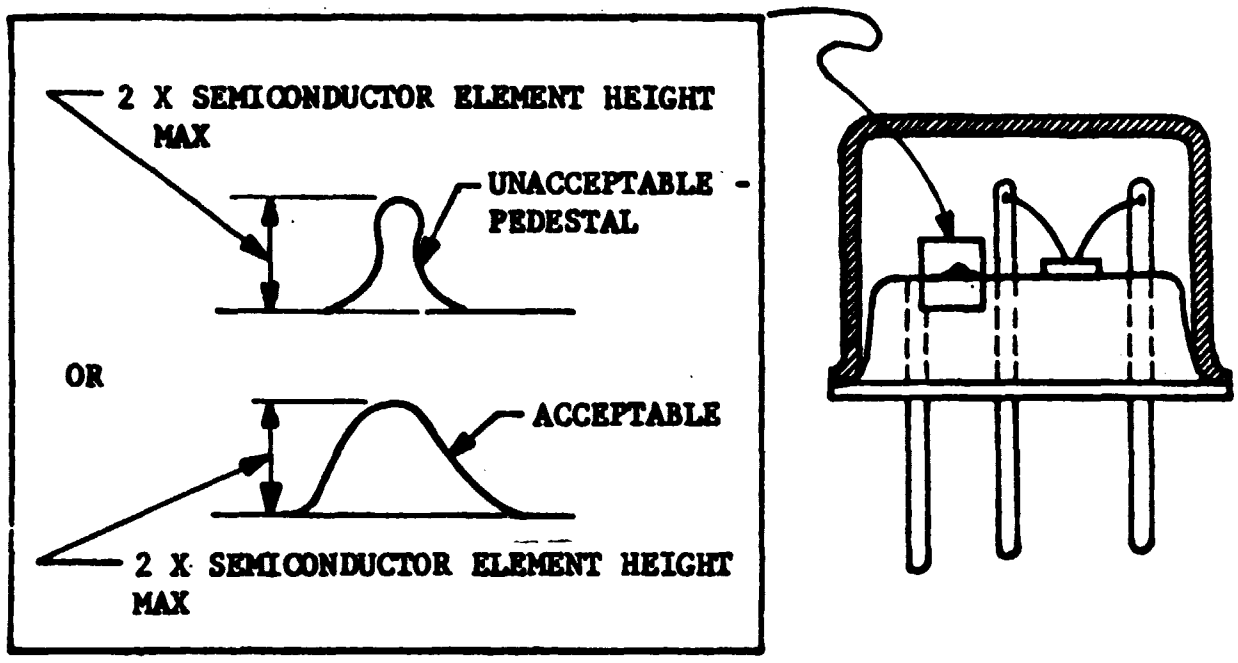
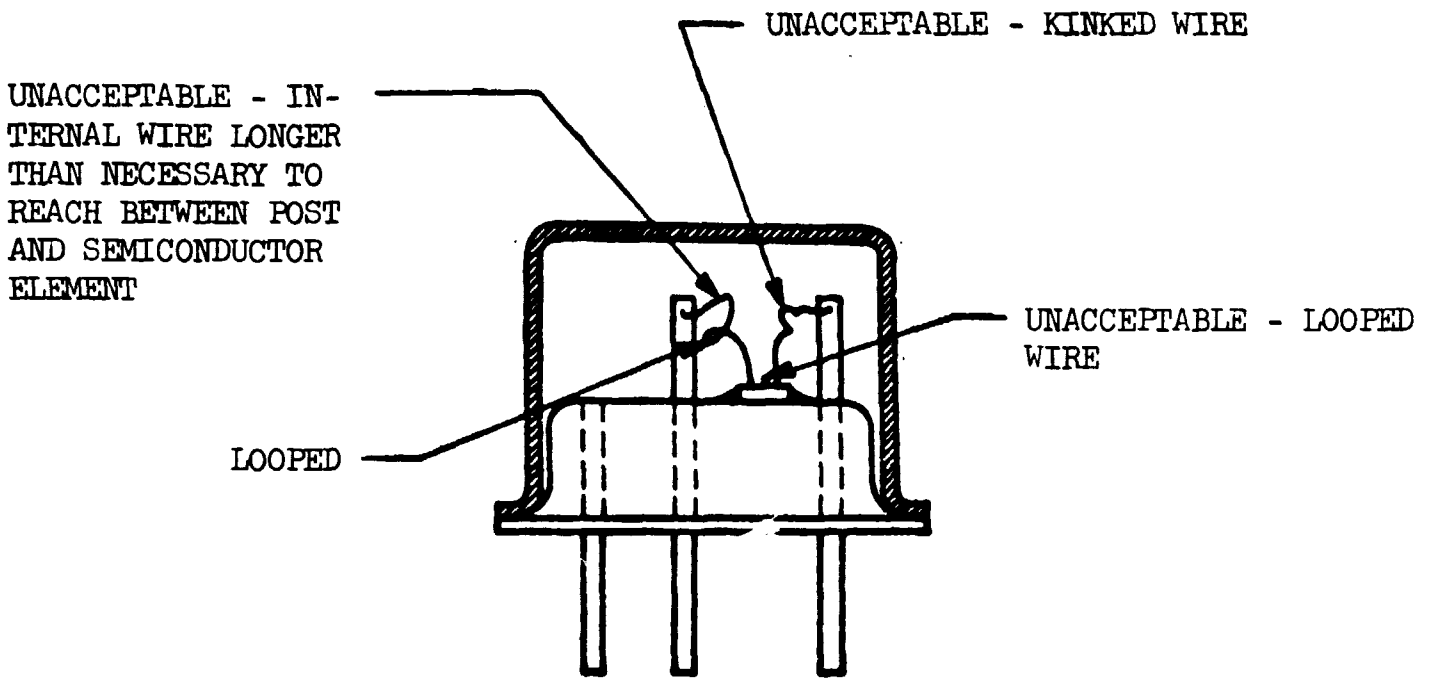


FIGURE B-3. ACCEPTABLE AND UNACCEPTABLE EXTRANEOUS MATERIAL BUILDUP.



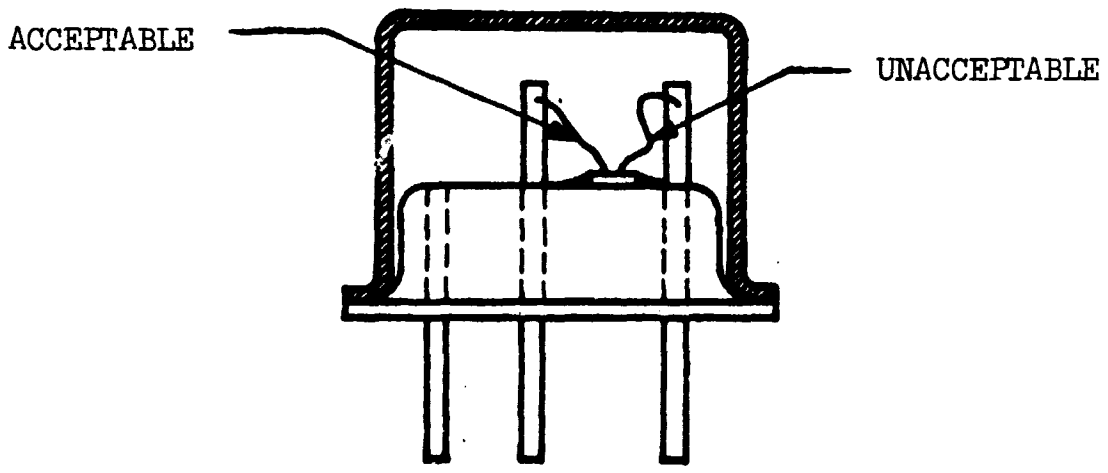


FIGURE B-4. OTHER TYPES OF ACCEPTABLE AND UNACCEPTABLE INTERNAL LEADS.

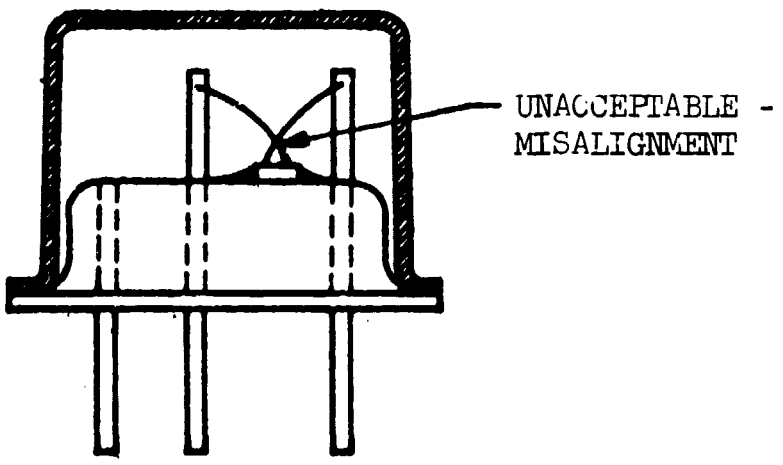


FIGURE B-5. MISALIGNED INTERNAL LEADS.

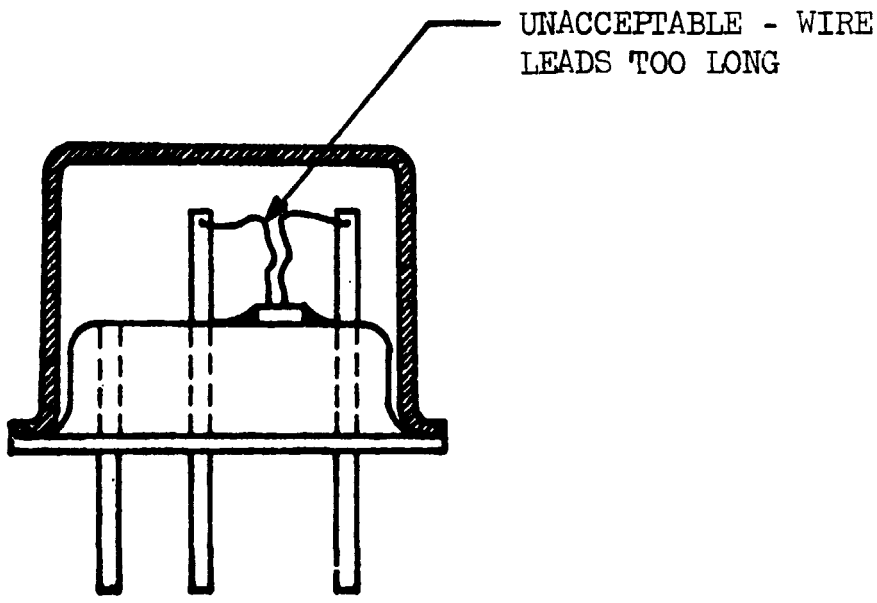


FIGURE B-6. INTERNAL LEADS TOO LONG.

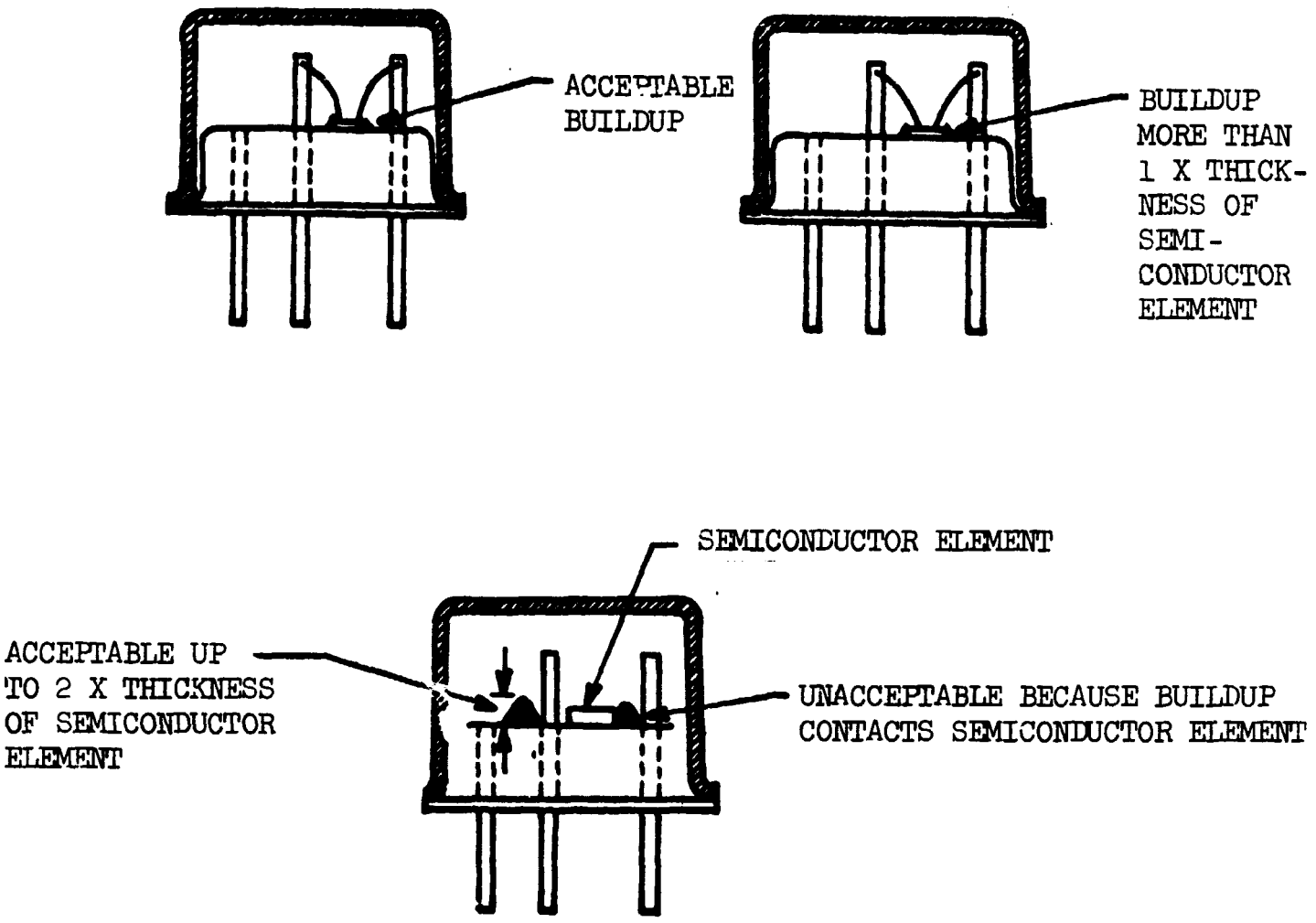


FIGURE B-7. ACCEPTABLE AND UNACCEPTABLE BONDING MATERIAL BUILDUP.

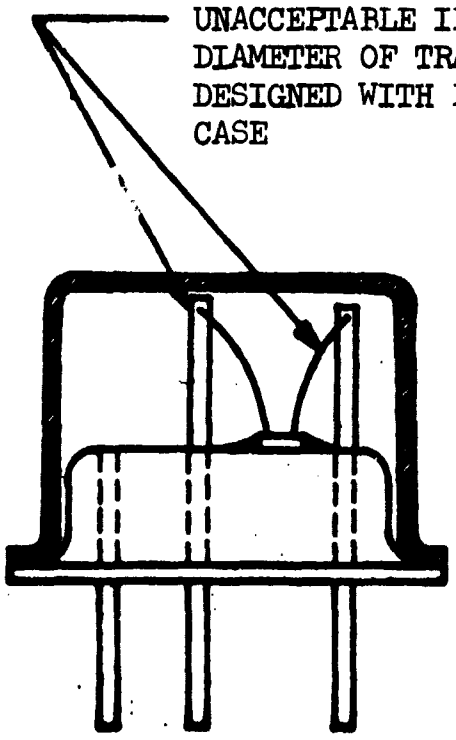


FIGURE B-8. UNACCEPTABLE INTERNAL CLEARANCE.

APPENDIX C

INTERNAL VISUAL EXAMINATION

10. SCOPE

10.1 This appendix contains the methods and acceptance criteria for the internal visual examination of physical dimensions, materials, design, construction, and workmanship of transistors. The examination shall be performed prior to sealing or encapsulation to detect and eliminate transistors with internal defects.

20. APPARATUS

20.1 The apparatus for this examination shall include optical equipment capable of the specified magnifications (see 30.1) and any visual standards (gages, drawings, photographs, etc.) necessary to perform an effective examination.

30. TEST METHODS AND CRITERIA

30.1 Examination

Prior to sealing or encapsulation, all transistors shall be examined with a binocular microscope under 80-power minimum magnification for semiconductor die defects and under 20-power minimum magnification for header, die attachment, bonding, and lead-wire defects. Vertical illumination shall be used when necessary for detection of defects.

30.1.1 Rejection Criteria

Devices that exhibit any of the following defects shall be unacceptable.

30.1.1.1 Semiconductor Die Defects

a. Reduction of metallization width: Voids or scratches through the metallization, causing a reduction in the metallization width to less than one-half of its design width. (See figures C-1 and C-2.)

b. Excess metallization: A reduction in the silicon dioxide width between metallized areas to less than one-half the design width. (See figure C-3.)

c. Contact windows which are not completely covered with metallization.

d. Lifting or peeling of metallization.

e. Localized stains or other evidence of deterioration of die surface or metallization. (See figure C-4.)

f. Exposed silicon: Silicon, not covered by oxide, which exposes a junction or touches metallization (passivated devices only).

g. Gross undercutting: Discoloration of the oxide, indicating areas of gross undercutting caused by lifting of the photo resist.

h. A channel stopper which is not continuous through its normal pattern area. (See figure C-5.)

i. Solidly adhering foreign material which bridges two metallized areas, extends to the edge of the chip, covers more than one-half the metallization width, or covers any part of a junction.

j. Particles of metal or silicon (including potentially loose particles) which exceed 1 mil (0.001 inch) in a major dimension. (See figure C-6.)

k. Lint or other soft nonconducting particles which exceed 1 mil in a major dimension.

l. Cracks and chips: Cracks, chips, or scribe lines which touch or cross a junction or metallization. No chip shall extend over more than 10 percent of the surface of the die. (See figure C-7.)

m. Pinholes in the active area of the die.

30.1.1.2 Header Defects

a. Blistering or flaking of gold plating.

b. Bent header posts, inclined more than 10 degrees from perpendicular.

c. Bent or deformed header flanges.

d. Insulated header post which is off center by more than 25 percent of radius length from center of hole. (See figure C-8.)

e. Pinholes (bubbles). Air bubbles in the glass region which exceed one-fourth the area of the glass region.

30.1.1.3 Die Attachment Defects

a. Die which is not properly oriented and not parallel with the plane of the header within 10 degrees.

b. Eutectic voids: Voids in the eutectic material around the die periphery exceeding 20 percent of a side.

c. Excess solder, eutectic material, or gold (finish) that may break away and become loose particles.

d. Extraneous gold (finish) on the die or header, or gold splashes on glass seals. (See figures C-9 and C-10.)

30.1.1.4 Bonding or Lead Wire Defects

a. Bonds which overlap to adjacent metal or another ball bond, so that no silicon dioxide can be seen between the bond and the adjacent metal when viewed vertically. (See figure C-11.)

b. A bond which has less than 50 percent placement on the bonding pad. (See figure C-12.)

c. Missing or broken bonds: Kinked or broken leads.

d. A ball bond off its pad by more than 50 percent of its diameter or which extends over a junction (except mesa diodes). (See figure C-13.)

e. Ball bond sizes greater than three wire diameters or less than two times the wire diameter.

f. Pigtails which are longer than two wire diameters. (See figure C-14.)

g. More than one bond attempt for each pad.

h. Nicks, crimps, twisting, or scoring, which cut or deform the lead wire or reduce the wire diameter by 10 percent or more.

i. Taut lead between ball bond and post: Maximum permissible lead slack is defined as a chordal distance of three wire diameters from the outside diameter of a wire's point of greatest deviation to an imaginary straight line from bond to weld. (See figure C-15.)

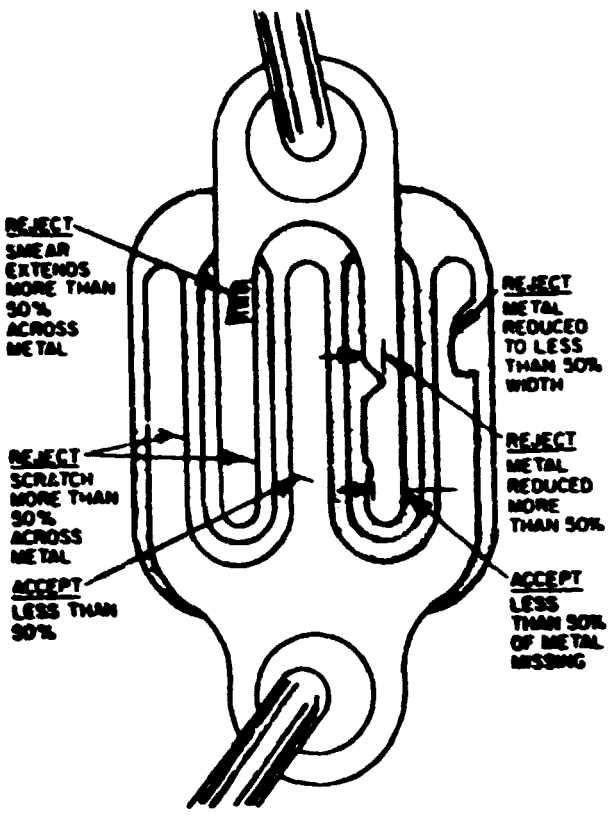


FIGURE C-1. REDUCTION IN METALLIZATION.

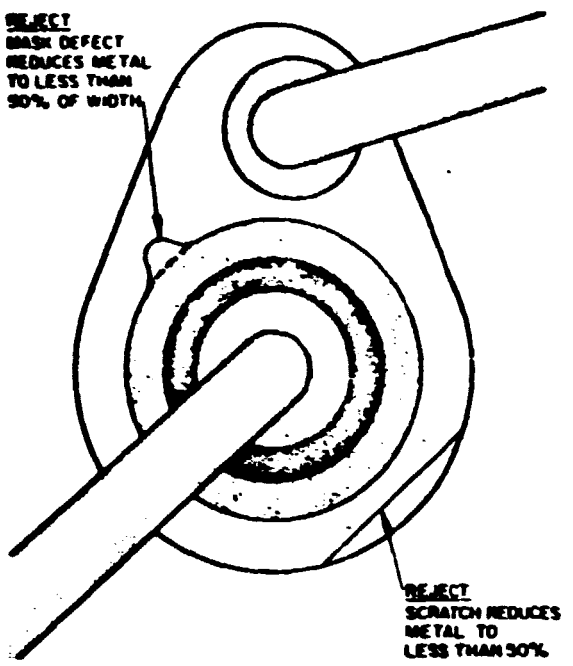


FIGURE C-2. REDUCTION IN METALLIZATION.

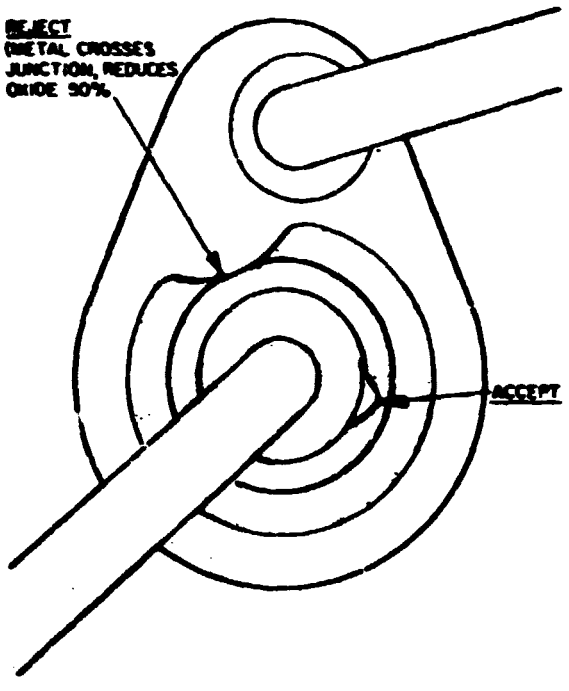


FIGURE C-3. REDUCTION IN METALLIZATION SPACING.

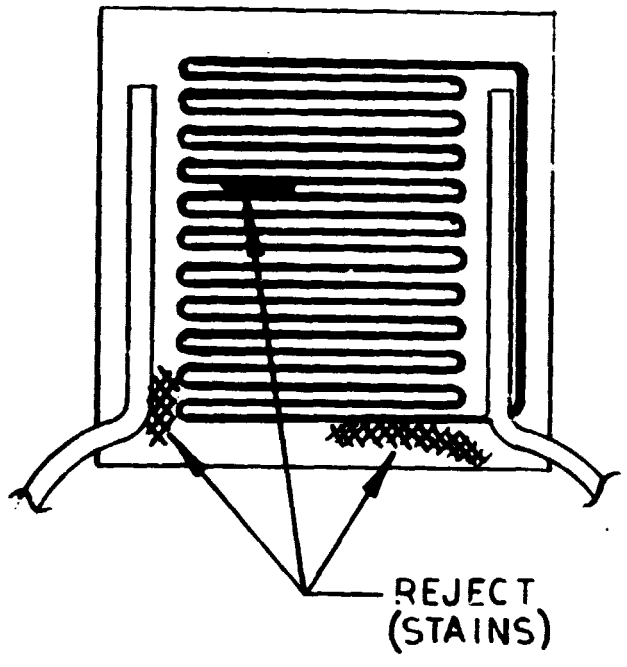


FIGURE C-4. STAINED CHIP AND METALLIZATION.

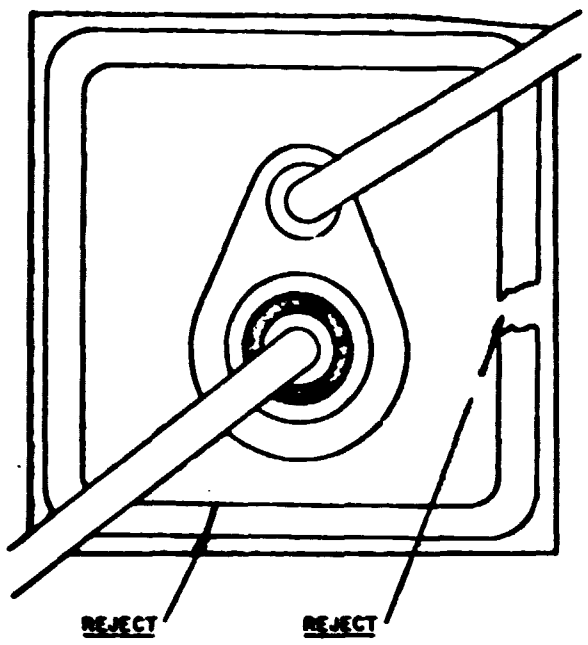


FIGURE C-5. NONCONTINUOUS CHANNEL STOPPER.

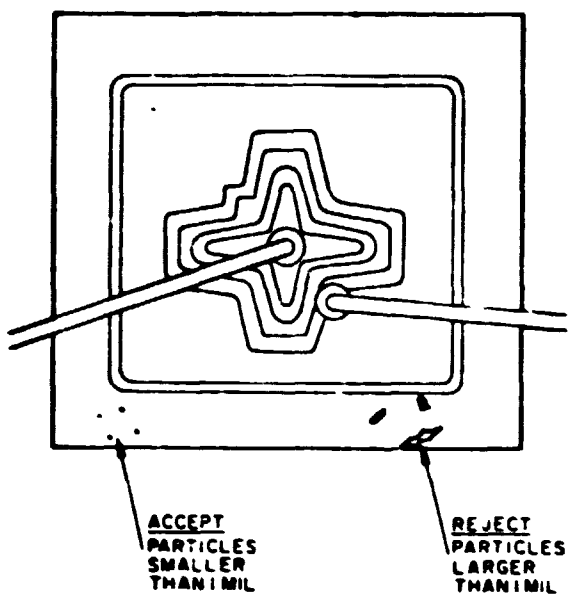


FIGURE C-6. LOOSE PARTICLES LARGER THAN 1 MIL.

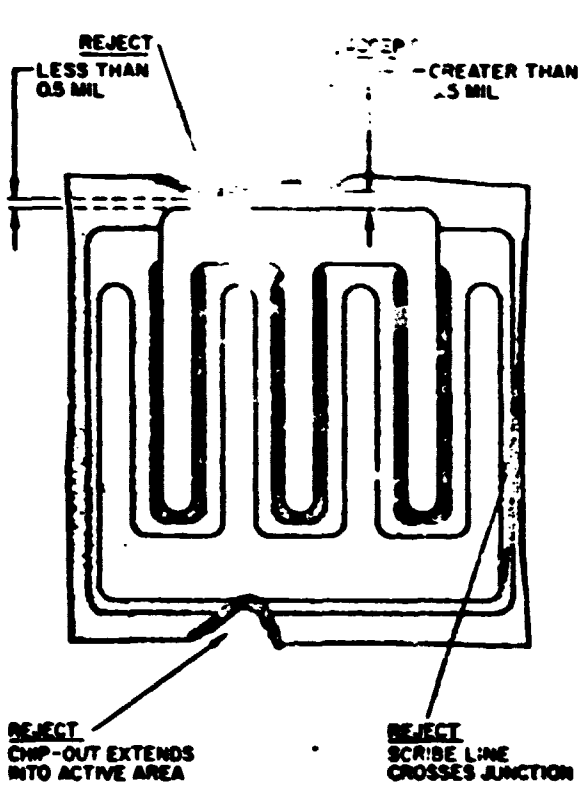


FIGURE C-7. CRACKS, CHIP-OUTS, AND SCRIBE LINES.

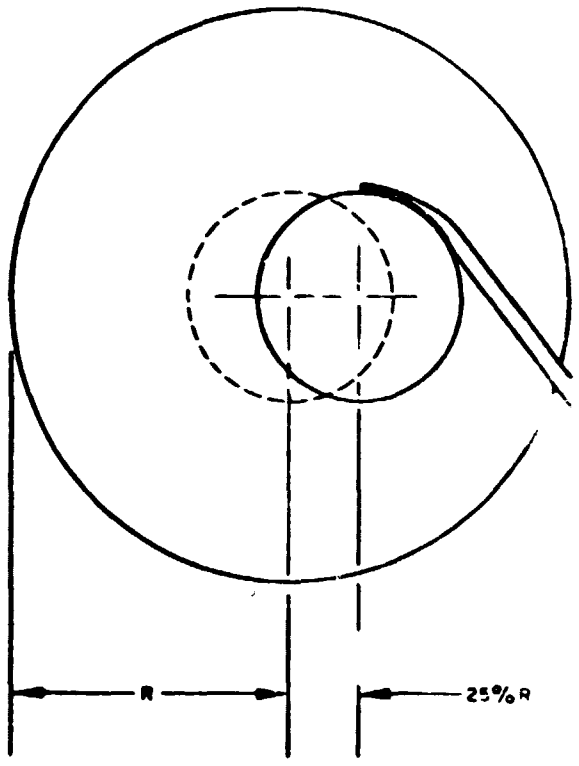


FIGURE C-8. HEADER POST OFF CENTER.

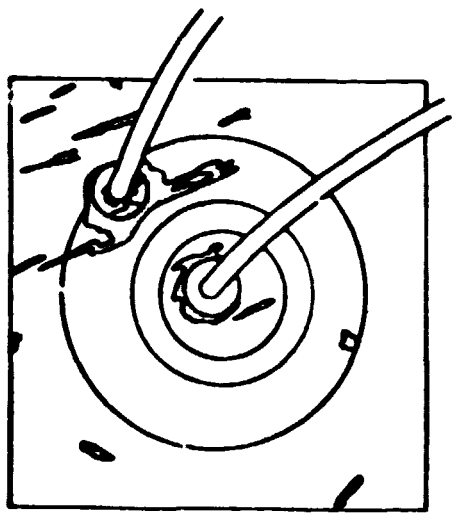


FIGURE C-9. WELD SPLATTERED ON DIE.

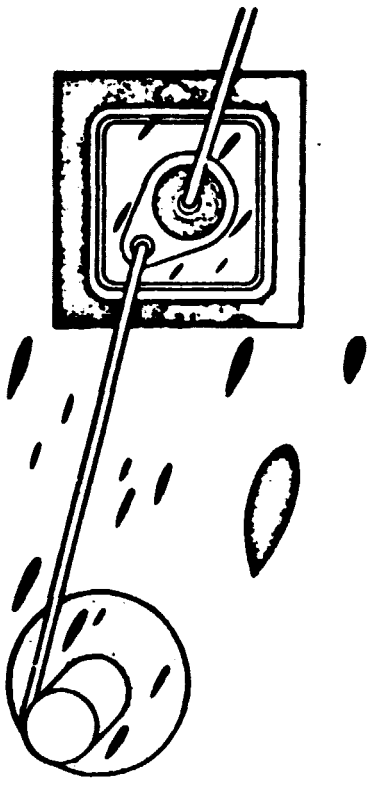


FIGURE C-10. EXTRANEOUS METAL ON DIE, GLASS, AND HEADER.

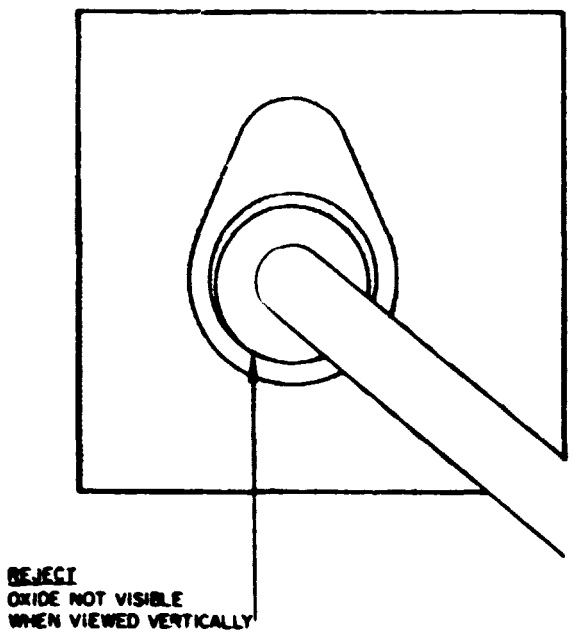


FIGURE C-11. BOND OVERLAPPING THE METAL.

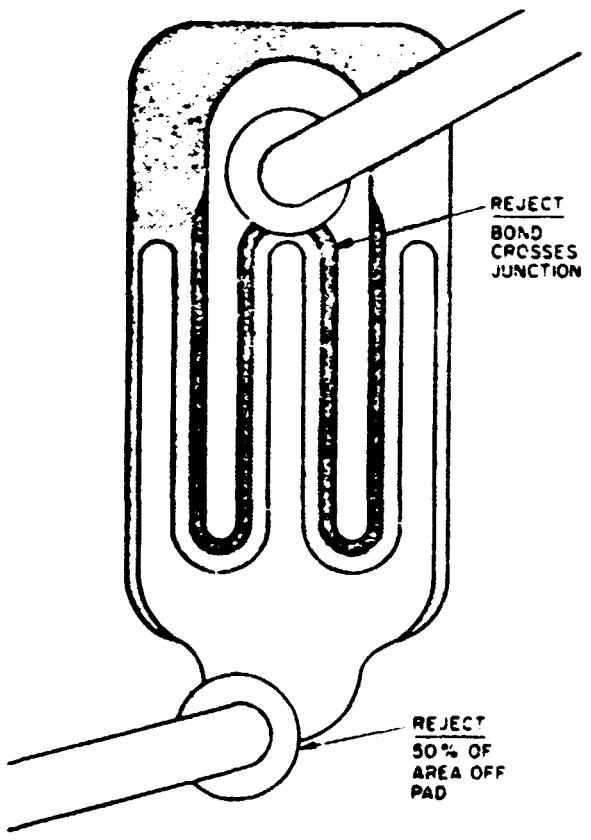


FIGURE C-12. MISPLACED BONDS.

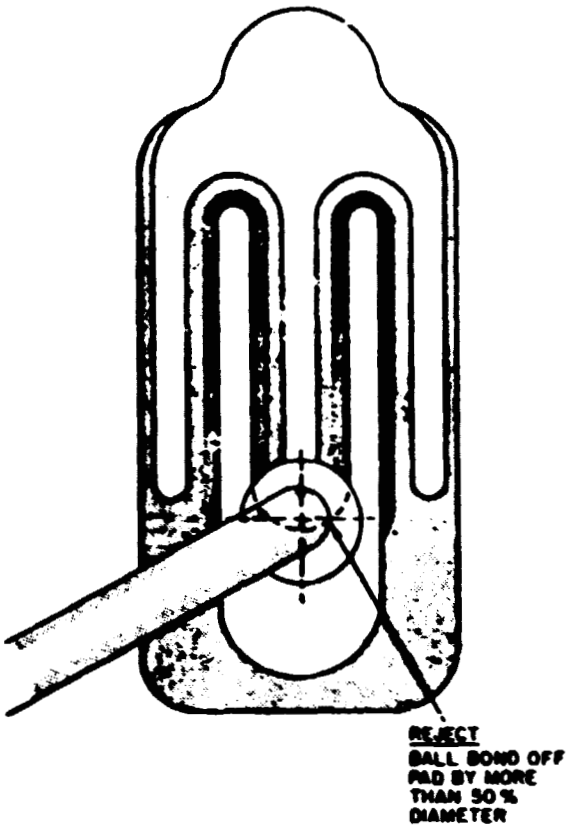


FIGURE C-13. MISPLACED BOND.

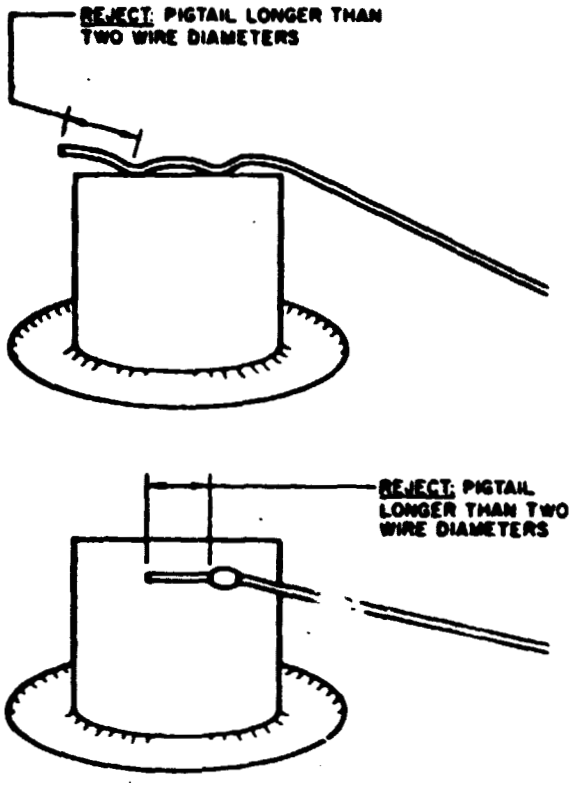


FIGURE C-14. PIGTAILS

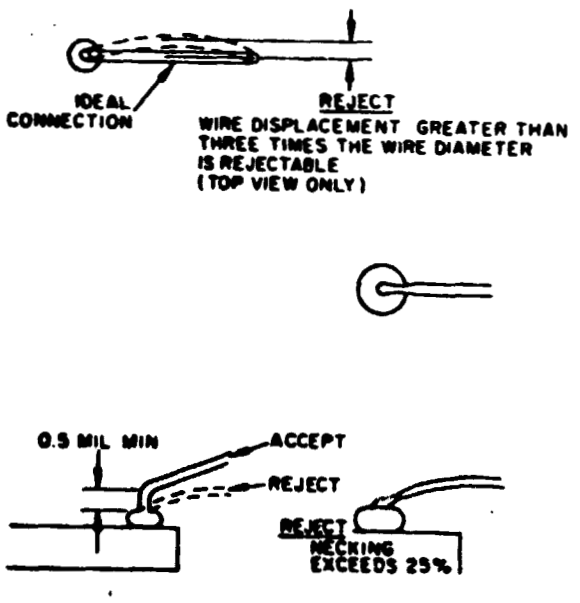


FIGURE C-15. LEAD CONFIGURATIONS.

EXAMPLE (NOT FOR PROCUREMENT)

NSL-A401,

DETAIL PROCUREMENT SPECIFICATION FOR

NASA SPECIAL LONG-LIFE (NSL) TRANSISTOR, TYPE NSL-401/1

FEBRUARY 1969

CONTENTS

NSL-A401/1

DETAIL PROCUREMENT SPECIFICATION FOR

NASA SPECIAL LONG-LIFE (NSL) TRANSISTOR, TYPE NSL-401/1

1. SCOPE

1.1 Applicability

This detail procurement specification is part of the system of Part Control Packages for controlling NASA Special Long-Life (NSL) parts, described in NASA CR-66742-1. This specification is detail section A of Part Control Package NSL-401/1, and defines the detail parts procurement requirements for transistors, type NSL-401/1. This specification and the general procurement specification for NSL transistors, NSL-A401, are mandatory whenever transistor type NSL-401/1 is specified.

1.2 Part Identification

This detail procurement specification covers a silicon, NPN transistor intended for use in low-level, low-noise amplifiers. Transistors procured under this specification shall be identified by the type designation NSL-401/1. The JEDEC part type which has the most similar electrical and mechanical characteristics is the 2N2484; however, this information is provided herein for reference purposes only, and the JEDEC part type should not be used instead of the NSL-401/1 for purposes other than for breadboards and early development models.

1.3 Part Manufacturer Identification

Transistors procured under this detail procurement specification shall be manufactured by, and obtained directly and only from:

Name:	National Semiconductor Corp.
Address:	P. O. Box 443
	Danbury, Connecticut 06813
Code Identification Number:	01295

1.4 Deviations

The requirements of 1.4 of NSL-A401 apply.

1.5 Revision Verification

The requirements of 1.5 of NSL-A401 apply.

1.6 Change Notification

The requirements of 1.6 of NSL-A401 apply.

2 APPLICABLE DOCUMENTS

2.1 Documents

The general procurement specification for NASA Special Long-Life (NSL) transistors, NSL-A401, forms a part of this specification. (The documents listed in 2.1 of NSL-A401 form a part of this document to the extent specified herein and within the limitations of 2.2 of NSL-A401.)

2.2 Conflicting Requirements

The requirements of 2.2 of NSL-A401 apply.

3. PRODUCT REQUIREMENTS

3.1 Electrical Characteristics

The electrical characteristics shall be in accordance with 3.1.1 and 3.1.2 below.

3.1.1 Maximum Ratings

The maximum ratings, at an ambient temperature of 25° ±3° C unless otherwise specified, shall be as shown in table I.

TABLE I.- MAXIMUM RATINGS

Storage temperature range	-65° to +200° C
Operating temperature range	-55° to +150° C
Junction temperature	+200° C
Collector-to-base voltage, emitter open	60 V
Collector-to-emitter voltage, base open	60 V
Emitter-to-base voltage, collector open	6.0 V
Collector power dissipation	0.36 W
Derate above 25° C ambient (in free air)	2.06 mW/° C

3.1.2 Electrical Requirements

The electrical requirements shall be as specified in table II.

3.2 External Physical Characteristics

The external physical characteristics of the transistors shall be as shown in figures 1 and 2. The general requirements of 3.2 of NSL-A401 also apply.

3.3 Internal Physical Characteristics

The internal physical characteristics of the transistors shall be as shown in figures 2 and 3. The general requirements of 3.3 of NSL-A401 also apply.

3.4 Environmental Compatibility

The requirements of 3.4 of NSL-A401 apply. In addition, the transistors shall be capable of meeting the following environmental requirement:

3.4.1 Radiation Resistance

The transistors shall be capable of withstanding a gamma radiation dose of not less than _____ rads (Si) without degradation of performance.

3.5 Manufacturing Controls

The requirements of 3.5 of NSL-A401 apply

3.6 Identification and Traceability

The requirements of 3.6 of NSL-A401 apply.

3.7 Product Assurance

The requirements of 3.7 of NSL-A401 apply.

4. TEST REQUIREMENTS

4.1 Controls Required Over Testing.

The requirements of 4.1 of NSL-A401 apply.

4.2 Test Methods and Criteria

The test methods and criteria specified in 4.2 of NSL-A401 apply. Tables I through IV and figures 1 through 3 herein apply as specified in 4.2 of NSL-A401.

4.3 Acceptance Test

The requirements of 4.3 of NSL-A401 apply. The burn-in test conditions, parameter drift measurements, acceptable limits, and drift criteria are provided in table III herein.

4.4 Qualification Test

The requirements of 4.4 of NSL-A401 apply. The qualification test conditions, electrical end-points, operation-life parameter drift measurements, and criteria are provided in table IV herein.

TABLE II.- ELECTRICAL REQUIREMENTS

Test	Test Method MIL-STD-750	Conditions	Limits at Temperature			Units
			T_A = -55° C	T_A = +25° C	T_A = +150° C	
Subgroup 1						
BV_{CEO}	3011 cond D	I_C = 10 mA 1/ I_B = 0		60 min		V
BV_{CBO}	3001 cond D	I_C = 10 µA I_E = 0		60 min		V
BV_{EBO}	3026 cond D	I_E = 10 µA I_C = 0		6.0 min		V
I_{CBO}	3036 cond D	V_{CB} = 45 V I_E = 0		10 max		nA
I_{CES}	3041 cond C	V_{CE} = 5 V V_{BE} = 0		5 max	10 max	nA
I_{CEO}	3041 cond D	V_{CE} = 5 V I_B = 0		2 max		nA
I_{EBO}	3061 cond D	V_{EB} = 6 V I_C = 0		2 max		nA
Subgroup 2						
h_{FE_1}	3076	V_{CE} = 5 V I_C = 1 µA		30 min		--
h_{FE_2}	3076	V_{CE} = 5 V I_C = 10 µA		200 min 500 max	35 min	--
h_{FE_3}	3076	V_{CE} = 5 V I_C = 100 µA		225 min		--
h_{FE_4}	3076	V_{CE} = 5 V I_C = 500 µA		250 min		--

1/ Pulsed: Pulse width ≤ 300 µsec, duty cycle ≤ 2%.

TABLE II.- ELECTRICAL REQUIREMENTS - Continued

Test	Test Method MIL-STD-750	Conditions	Limits at Temperature			Units
			T_A = -55° C	T_A = +25° C	T_A = +150° C	
Subgroup 2 (Continued)						
h_{FE_5}	3076	V_{CE} = 5 V I_C = 1 mA		250 min		--
h_{FE_6}	3076	V_{CE} = 5 V I_C = 10 mA 1/		800 min		--
$V_{CE(sat)}$	3071	I_C = 1.0 mA I_B = 0.1 mA		0.3 max		V
V_{BE}	3066 cond B	V_{CE} = 5 V I_C = 100 µA		0.5 min 0.7 max		V
Subgroup 3						
h_{oe}	3216	V_{CE} = 5 V I_C = 1.0 mA		0 min 40 max		µmho
h_{re}	3211	V_{CE} = 5 V I_C = 1.0 mA		0 min 8.0×10^{-4} max		
h_{ie}	3201	V_{CE} = 5 V I_C = 1 mA		3.5 K min 24 K max		-- ohm
h_{fe}	3206	V_{CE} = 5 V I_C = +1 mA f = 1 kHz		250 min 900 max		--
Subgroup 4						
$\lvert h_{fe} \rvert$	3306	V_{CE} = 5 V I_C = 500 µA f = 30 MHz		20 min 70 max		--
C_{obo}	3236	V_{CB} = 5 V I_E = 0 100 kHz≤f≤1 MHz		5.0 max		pf

TABLE II.- ELECTRICAL REQUIREMENTS - Continued

Test	Test Method MIL-STD-750	Conditions	Limits at Temperature			Units
			T_A = -55° C	T_A = +25° C	T_A = +150° C	
Subgroup 4 (Continued)						
C_{ibo}	3240	V_{EB} = 0.5 V I_C = 0 100 kHz≤f≤1 MHz		6.0 max		pf
NF_1	3246	f = 100 Hz V_{CE} = 5 V I_C = 10 μA R_g = 10 kilohms		7.5 max		db
NF_2	3246	f = 1 kHz V_{CE} = 5.0 V I_C = 10 μA R_g = 10 kilohms		3 max		db
NF_3	3246	f = 10 kHz V_{CE} = 5 V I_C = 10 μA R_g = 10 kilohms		2 max		db
NF_4	3246	V_{CE} = 5 V I_C = 10 μA R_g = 10 kilohms Power bandwidth of 15.7 kHz with 3 db points at 10 Hz and 10 kHz		3 max		db

TABLE III.- BURN-IN TEST CONDITIONS,
PARAMETER DRIFT MEASUREMENTS, AND CRITERIA

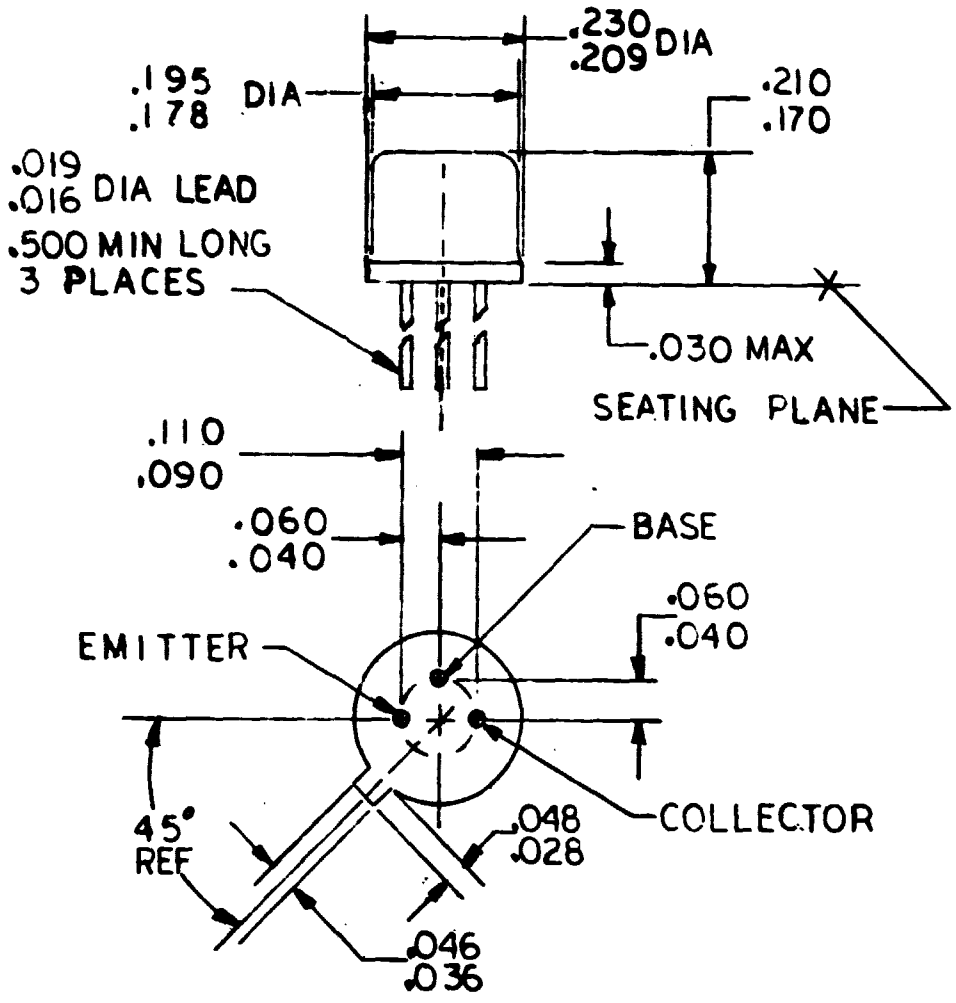
Test and Conditions	Test Method 1/	Acceptable Limits	Drift Criteria
Reverse-bias high temperature life (Not applicable)			
Burn-in: T_A = 25° ±3° C V_{CB} = 30 V P_T = 0.36 W	1026		
Parameter drift measurements:			
I_{CBO}	Table II herein	Table II herein	100% or 5 nA, whichever is greater
I_{EBO}			100% or 1 nA, whichever is greater
h_{FE_2}			±25%
$V_{CE(sat)}$			±50 mV
V_{BE}			±0.1 V
NF_2	Table II herein	Table II herein	±25%

1/ Applicable method of MIL-STD-750 (unless otherwise specified).

TABLE IV.- QUALIFICATION TEST CONDITIONS, ELECTRICAL END-POINTS, OPERATION-LIFE PARAMETER DRIFT MEASUREMENTS, AND CRITERIA

Test and Conditions	Test Method 1/	Acceptable Limits	Drift Criteria
Thermal resistance: V_2 = 30 V I_C = 1 mA T_2 = +125° ±3° C T_1 = +25° ±3° C	3132	486°C/W max	
Operation life: T_A = +25° ±3° C t = 2000 ±24 hours V_{CB} = 30 V P_T = 0.36 W	1026		
Electrical end-points and operation-life parameter drift measurements (at 25° ±3° C):			
I_{CBO}	Table II herein	Table II herein	Table III herein
I_{EBO}	↕	↕	↕
h_{FE_2}	↕	↕	↕
$V_{CE(sat)}$	↕	↕	↕
V_{BE}	↕	↕	↕
NF_2	Table II herein	Table II herein	Table III herein

1/ Applicable method of MIL-STD-750 (unless otherwise specified).



NOTE:

1. **JEDEC TO-18 PACKAGE**

FIGURE 1. EXTERNAL PHYSICAL CHARACTERISTICS

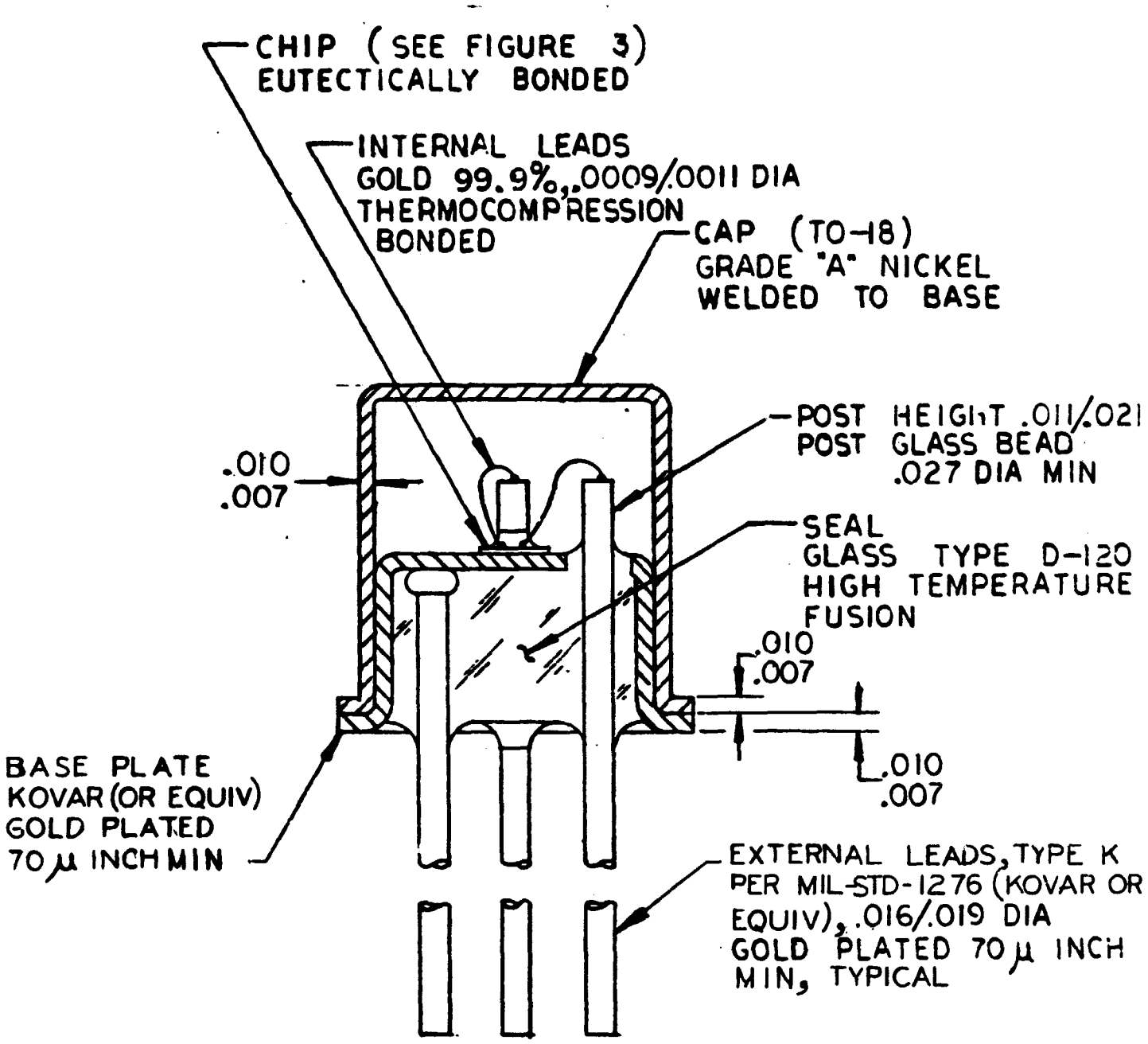
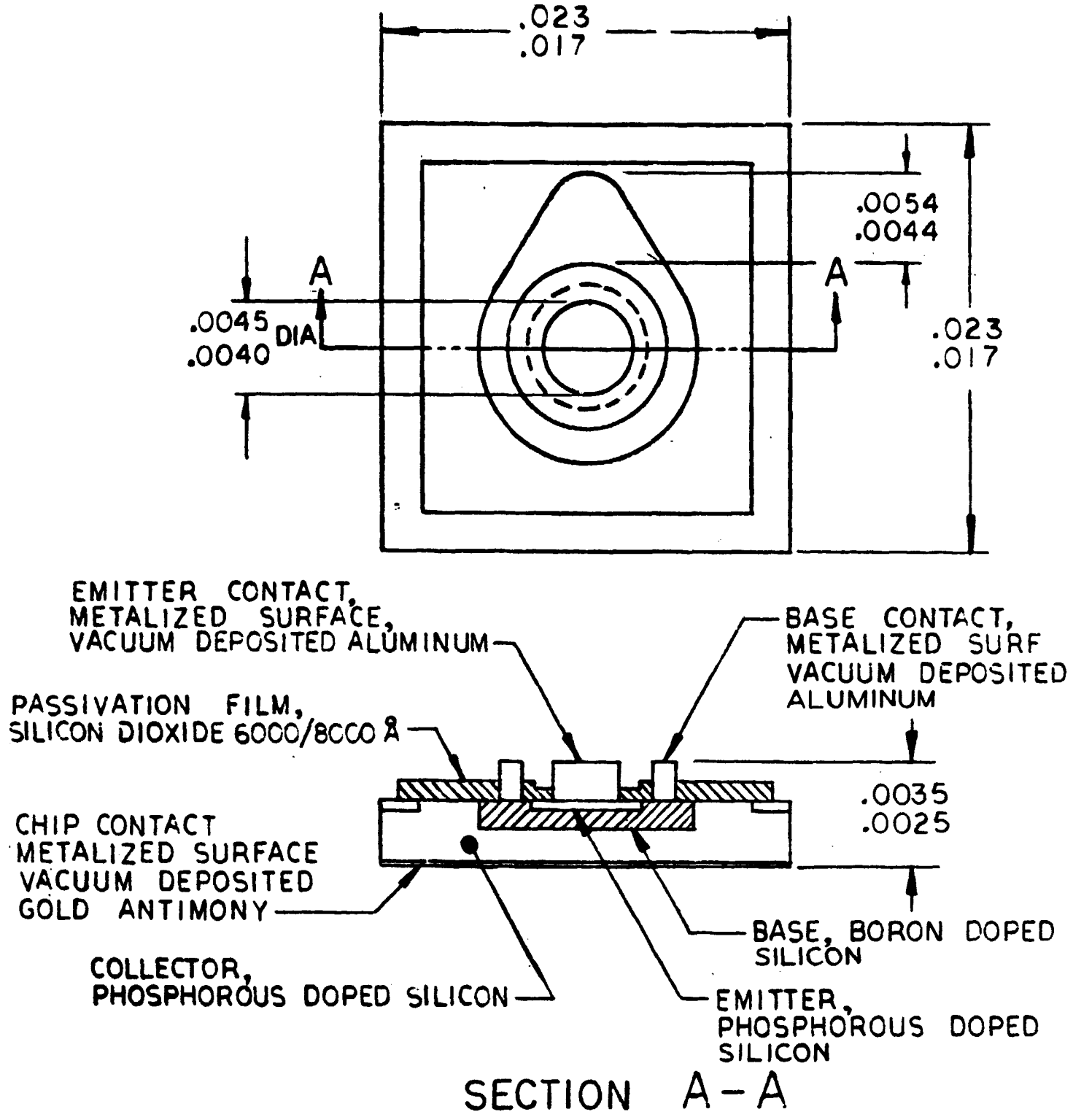


FIGURE 2. CROSS-SECTIONAL CHARACTERISTICS.



NOTE:

1. SEMICONDUCTOR PROCESS: PLANAR

FIGURE 3. CHARACTERISTICS OF SILICON CHIP

5. DOCUMENTATION REQUIREMENTS

5.1 Documentation Required with Delivery

The requirements of 5.1 of NSL-A401 apply.

5.2 Record Retention

The requirements of 5.2 of NSL-A401 apply.

6. PARTS DISPOSITION

6.1 Disposition of Parts

The requirements of 6.1 of NSL-A401 apply.

6.2 Packaging of Parts for Delivery

The requirements of 6.2 of NSL-A401 apply.

6.3 Delivery of Parts

The requirements of 6.3 of NSL-A401 apply.

7. ABBREVIATIONS, SYMBOLS, AND DEFINITIONS

The abbreviations, symbols, and definitions provided in NSL-A401 apply.

REVISION RECORD

REV	AUTHORITY	DESCRIPTION	RELEASE	
			DATE	APPROVAL

EXAMPLE

NSL-B401

GENERAL DESIGN APPLICATION SPECIFICATION FOR

NASA SPECIAL LONG-LIFE (NSL) TRANSISTORS

FEBRUARY 1969

CONTENTS

NSL-B401

GENERAL DESIGN APPLICATION SPECIFICATION FOR NASA SPECIAL LONG-LIFE (NSL) TRANSISTORS

1. SCOPE

1.1 Applicability

This specification is part of the system of Part Control Packages for controlling NASA Special Long-Life (NSL) parts, described in NASA CR-66742-1. This specification is general section B of Part Control Package NSL-401, and defines the general design application requirements for all NSL transistors. This specification and the applicable detail procurement specification, NSL-B401/____, are mandatory whenever NSL transistors are specified.

2. APPLICABLE DOCUMENTS

2.1 Documents

The following documents form a part of this specification to the extent specified herein. Unless otherwise specified herein, the issue in effect on the date of the part procurement contract shall apply.

SPECIFICATIONS

NASA

NSL-B401/____	Detail Design Application Specification for NASA Special Long-Life (NSL) Transistor

2.2 Conflicting Requirements

In the event of conflict between the requirements of this specification and any of the documents specified herein or in the applicable detail design application specification, the order of precedence shall be as follows:

a. The applicable NASA Special Long-Life (NSL) detail design application specification.

b. This general design application specification.

c. Specifications referenced herein or in the applicable detail design application specification.

3. DESIGN APPLICATION REQUIREMENTS

3.1 Design Limitations

3.1.1 Temperature

The most universal limitation to semiconductor performance is junction or die temperature. Normally, the temperature limit of a transistor is imposed by the die material. In many parts, other materials (such as metallization and passivation) and in encapsulated devices, however, the package material establishes the upper temperature limit of the device.

Above 200°C, changes in the diffused properties of silicon occur much more rapidly, and parts whose characteristics are extremely sensitive to changes in the impurity distribution may be derated from 200° to 175°C. Other parts may be rated at only 175°C because of the metallization system. Some systems (particularly gold on aluminum, or gold on silicon) are prone to deterioration over extended time at high temperatures. Large power transistors may have widely different temperatures across the die due to voids in the die-header bond, and for this reason may be rated at only 150°C. Many of these transistors also use varnishes over the die to aid in the control of leakage currents; varnishes may impose a limit of 150°C.

In addition to the establishment of an upper limit, operating temperature is a major factor in semiconductor reliability. Heat degrades bulk characteristics and has a degenerative run-away effect on junction characteristics. Localized hot spots resulting from impurity in materials and resultant localized high current densities frequently cause anomalies in performance. Material and process control during manufacture of a part can alleviate these problems but cannot remove the need for rigorous temperature control in final application.

3.1.2 Power Dissipation

The power dissipation capability of a transistor is dependent on the maximum allowable junction temperature, the thermal resistance from the junction to the exterior, and the external temperature. These, in turn, are dependent on several other factors, of which those relating to junction temperature have already been mentioned above. Thermal resistance depends on die size and thickness, die mounting material, die location, whether or not the collector is isolated, case material and size, and the characteristics of the heat sink, if any. Usually, values for thermal resistance (both from junction to case, and junction to air) will be found in the applicable detail design application specification.

3.1.3 Breakdown Voltage (Avalanche)

Avalanche breakdown voltage (as distinguished from secondary breakdown) is a function of the impurity doping level achieved in manufacturing the transistor die. Generally, high breakdown voltages are obtained by low doping levels, which also provide high bulk resistivity. For this reason, transistors with high collector-base breakdown voltages usually have relatively high saturation voltages.

The wide distribution of breakdown voltages obtained during manufacturing usually causes a manufacturer to offer several values of breakdown voltage in a family of similar parts. The part types described in the detail design application specification have been selected to provide the most useful breakdown voltage consistent with cost.

3.1.4 Secondary Breakdown and Safe Operating Area

Avalanche breakdown is produced at a transistor junction by raising the voltage across the junction until the current begins to flow. The knee of the curve is usually quite sharp, and the test is not destructive (as long as power is limited). When the voltage is reduced slightly, the current decreases nearly to zero (in better transistors), and the test may be performed again and again with no damage to the transistor.

Whether or not a junction (either diode or transistor) is in an avalanche breakdown condition depends only on the voltage across the junction. In contrast to avalanche breakdown, secondary breakdown occurs between the collector and emitter in transistors, and its occurrence depends on the collector-emitter voltage, collector current, duration of collector voltage and current application, and bias condition of the base-emitter junction. It is a destructive condition, usually resulting in a collector-emitter short. Rather than being a voltage-induced phenomenon, it is an energy-induced condition and occurs because extremely high temperatures are generated in small localized areas of the die. It is not a simple power-induced failure because it depends on uneven heating of the die and occurs in a span of time much too short to allow heating of the entire die.

The secondary breakdown capabilities of a transistor depend not only on the diffused properties of the die, but also on the emitter efficiency (which is related to the amount of emitter periphery), and the thermal time constant and thermal capacity of the die.

3.1.5 Current

The current carrying capability of transistors depends primarily on emitter area and die size, but may be limited by the internal lead wires to the die. At higher voltages it is also subject to both power limitations and secondary breakdown limitations.

3.2 Derating Procedures

There are two types of derating applied to transistors in circuit and system design:

a. Power derating, which must be performed in order to avoid damage to the parts, and

b. Reliability derating, which should be performed in high reliability systems and non-maintainable systems or circuits.

3.2.1 Power Derating

Each transistor is rated in the detail design application specification for a maximum junction temperature. To avoid exceeding this temperature, the information given in the derating section of the detail design application specification should be used. The power to be dissipated in the device and either the case or ambient temperature must be known.

When a heat sink is used, the case temperature can usually be determined reliably by measurement. When a heat sink is not used, the ambient temperature should be determined, and the appropriate derating curve should be used.

3.2.1.1 Conventional Maximum Use Levels

The conventional derating approach assumes that the thermal resistance, θ, from junction to the case/heat sink or to the ambient temperature, is a constant at all temperatures. This assumption produces a straight line for the Maximum Use Level Rating at which $T_J = T_{MAX}$ (see figure 1). This line runs between T_S (the temperature at which 100 percent of rating is allowable, usually 25°C) and T_{MAX} (at which the external temperature is equal to the maximum allowed for the junction and, therefore, zero added junction power dissipation is allowable). The portion of the solid line to the left of

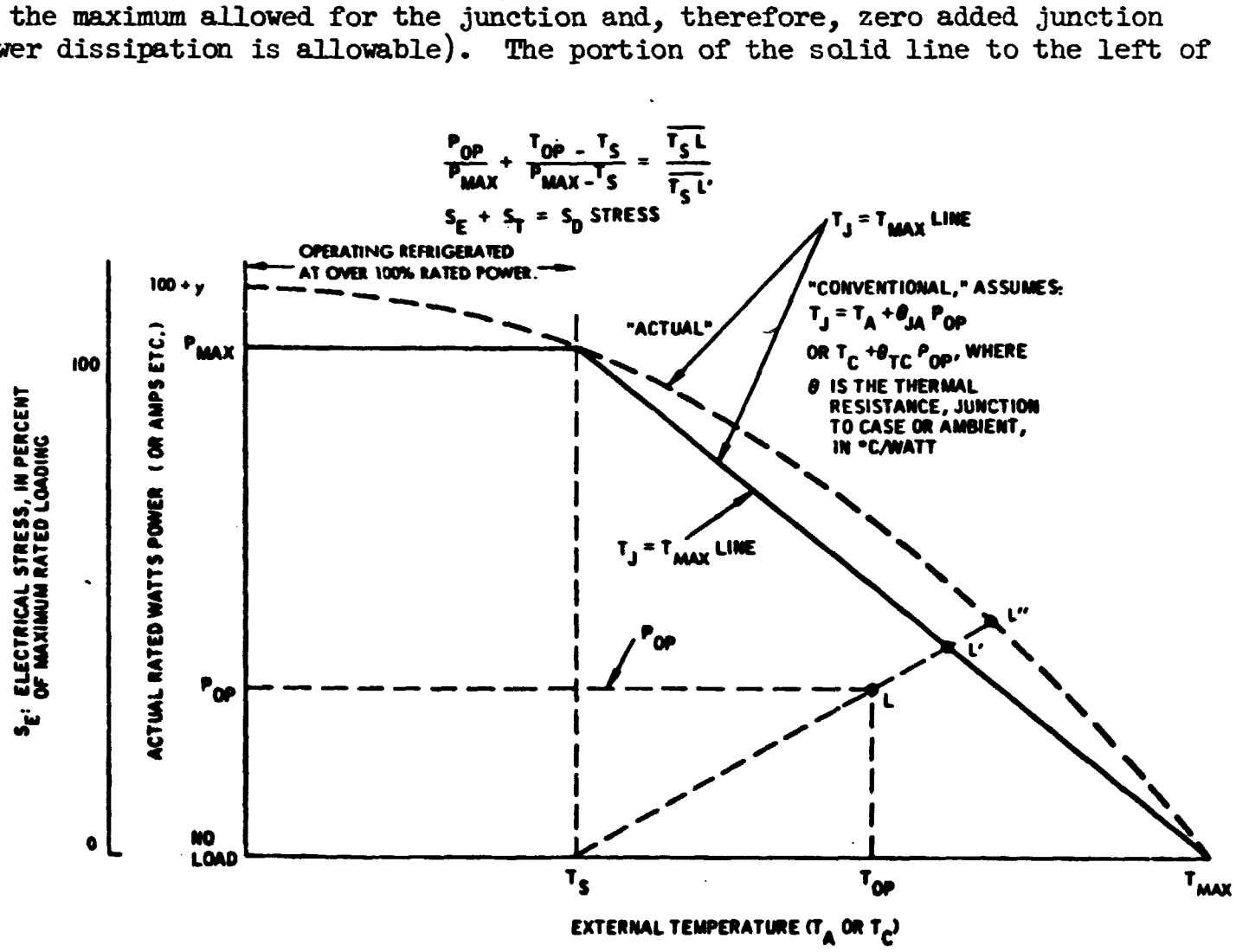


FIGURE 1. CONVENTIONAL MAXIMUM USE LEVELS.

T_S, also expresses the simplified assumption that 100 percent of rating cannot be exceeded. In reality, external refrigeration will allow operation at somewhat greater than 100 percent electrical rating without the T_J exceeding T_{MAX}, as implied by the extension of the dashed line (100 percent + y).

3.2.1.2 Actual Maximum Use Levels

Since the actual thermal resistance of the bulk semiconductor material is not precisely constant, the straight line assumption can lead to appreciable (though usually conservative) loading error. The actual line is shaped more like the curved dashed line in figure 1. On some devices, the part manufacturers recognize this by specifying more than the two points of 100 percent and zero percent rating. Figure 2 shows a rating chart which is typical of any power transistor. The actual use level point for 150° C (L_2) is 120 amps. The straight line would have given a point (L_2') of 80 amps, which would have wasted over 30 percent of the device capability, or caused a considerable reliability prediction error. The steeper the slope of the Use Level line, the greater the rating difference (caused by the nonlinearity of thermal conductivity).

3.2.2 Derating for Reliability

In addition to derating applied to maintain junction temperatures below the maximum, derating shall be applied to achieve an acceptable level of failure rate. There is a considerable difference in what constitutes an acceptable failure rate level between a redundant circuit which is required to operate only one hour in 24 and a nonredundant circuit which must operate continuously for one year.

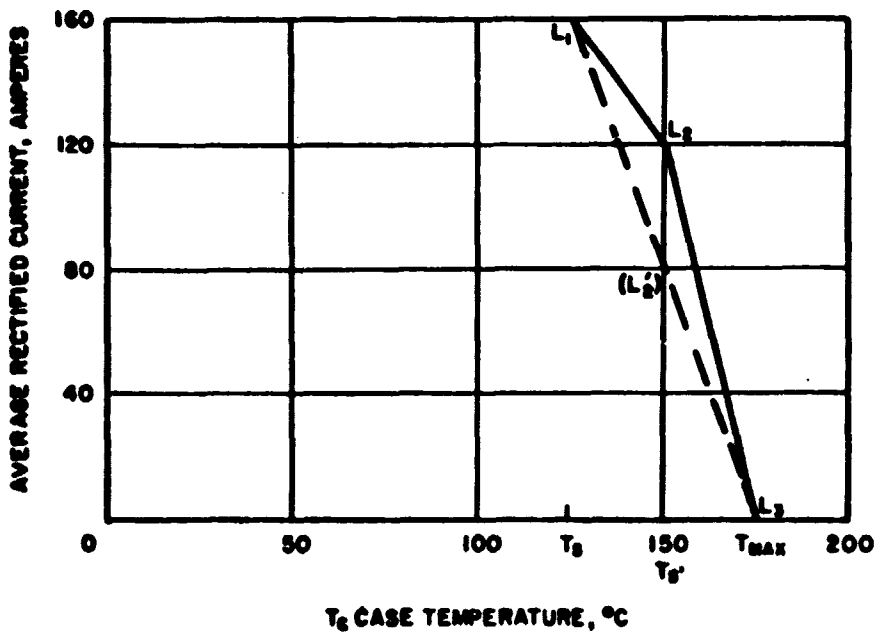


FIGURE 2. TYPICAL MULTIPOINT-RATING CURVE FOR SEMICONDUCTOR (SILICON) DEVICES.

Reliability (or failure rate) is a function of the stress level under which the part operates. The stress level has components of power/temperature stress, voltage stress, current stress, and mechanical stress. Operating temperature is the major factor.

3.2.2.1 Voltage Effects

In addition to the conventional electrical stress parameters of current or power, many semiconductor devices are reliability-sensitive to voltage stress. The degree of such sensitivity is expressed in prediction computation by the adjustment factor for secondary stress, π_{SS}.

3.2.2.2 Failure Mode Considerations

The nominal failure rates used herein for each part type express all typical failure modes which occur at a failure rate constant with time. It is assumed that design and control measures have been taken to eliminate conditions of poor quality and infant mortality.

3.2.2.3 Temperature and Power Ratings Terminology

This subsection clarifies the derivation and distinctions between a device's Electrical Stress Ratio (S_E), its Thermal Stress Ratio (S_T), and the Percent of Rating (S_D) which is used in "derating" to increase reliability.

Application of derating criteria requires a definition of uniform symbols for the terms used in power rating of transistors.

T_{MAX} is considered as the maximum permissible junction temperature (T_J). This temperature is often taken as 175°C for silicon devices. Since the junction temperature is difficult to measure directly, however, two other external "reference" temperatures are used:

a. T_C, the case temperature is easiest to determine, and is frequently used as the reference temperature.

b. T_A, the ambient temperature, may also be stipulated as the reference temperature.

Whether curves are referenced to T_C or T_A, there is no difference in their reliability or derating calculations, provided the device is mounted accordingly and the temperature information is properly used.

This means that power ratings referred to T_C cannot be used unless the device is mounted on a heat sink. In this instance the temperature of the heat sink is assumed as T_C, providing good thermal contact is maintained between the device and heat sink.

T_A assumes still air, unless otherwise stated. When the part manufacturer's power ratings used are based on T_A, then the results are conservative if the device is used with a heat sink (or with moving air) at the specified temperature.

The notations used herein, therefore, are:

T_J	Junction temperature
T_{MAX}	Maximum junction temperature allowable (from a deta. . part procurement specification)
T_C	Case temperature
T_A	Ambient temperature
T_{OP}	External operating temperature (case or ambient), whichever is specified for the specific part or instance.
T_S	Standard temperature (which is the external reference temperature at which P_{MAX} is specified (usually 25°C)[1/]
P_{MAX}	Maximum rated power at T_S, as specified in the detail part procurement specification.
P_{OP}	Actual operating power, in a specific instance
S_E	Electrical stress ratio (operating/maximum rated), without consideration of other environments; can be watts, amps, etc.; assumes $T_{OP} = T_S = 25°C$.
S_T	Thermal stress ratio ($T_{(J)}$ actual/$T_{(J)}$ MAX), assuming S_E = 0 percent.
S_D	Stress ratio for derating purposes; percent of rating; the sum of electrical and thermal stress rating percents.
S_{SS}	Stress ratio for secondary electrical stress; for transistors, voltage is used, and $S_{SS} = \frac{\text{Operating } V_{CE}}{\text{Rated } V_{CE}}$

3.2.2.4 Stress Ratios (Electrical and Thermal)

Semiconductor base failure rates, λ_b, are commonly related to the junction temperature. This junction temperature consists of the heat rise within the device (caused by power dissipated in the junction) plus

---

[1/] Unless otherwise noted, all values given herein are referred to $T_S = 25°C$. A $T_S \neq +25°C$ requires computation of "adjusted" stress ratios.

the case temperature. In turn, the case temperature is related to the ambient air or to the attached heat sink temperature.

Usually each device is given two rating points; one for maximum permissible junction temperature, and the other for the maximum case or ambient temperature at which 100 percent of the rated load can be dissipated without causing the sum of ambient (or case) plus internal temperature rise to exceed the specified maximum junction temperature. As the ambient (or case) temperature rises above the T_S value, the internal temperature rise and power load must be decreased if the combined temperature is not to exceed the maximum junction temperature. These points are illustrated in figure 1.

For semiconductor devices, the Electrical Stress Ratio (S_E) is used in calculating the rise of the junction temperature above the external reference temperature, T_A or T_C. It is expressed as:

$$S_E = \frac{P_{OP}}{P_{MAX}}$$

where

P_{OP} = Operating power level

P_{MAX} = Rated maximum power at standard temperature, $T_S = 25^{\circ}C$, unless otherwise specified

There is a corresponding Thermal Stress Ratio:

$$S_T = \frac{T_{OP} - T_S}{T_{MAX} - T_S}$$

However, the reliability computation curves for λ_b in subsequent sections have been simplified to use only the electrical stress ratio (S_E) and the T_C or T_A external temperatures, so that thermal stress ratio (S_T) is of interest only as a part of the derating procedures. Junction temperature (T_J) is not used in computations, except when it corresponds to a specific maximum junction temperature (T_{MAX}).

3.2.2.5 Electrical Stress (More Than One Device Per Case)

The $S_E = P_{OP}/P_{MAX}$ expression applies to the usual condition of a single device per case. For the more complex arrangements, additional symbols must be defined (the word "side" as used below also means individual device or section of the total assembly in the case):

S_E = Electrical stress ratio of the side being evaluated

P_1 = Power dissipation in an individual side being evaluated

$P_2 \ldots P_n$ = Power dissipated in the other (second, etc.) side(s) of the device

P_S = Maximum dissipation rating of one side of the assembly, with the other side(s) not operating; "one side rating "

N = Number of devices in the case

P_T = Total maximum rating of both sides (or all devices) operating; "both side rating"

Specifications for multiple devices in one case usually give a maximum rating for each device, and a total dissipation rating which is significantly less than the sum of individual ratings. For example, the dual transistor 2N2060 has a P_S of 0.5 watt and a P_T of 0.6 watt at 25°C ambient.

The following expressions now apply:

a. Dual devices in a single case (equally rated, unequally loaded):

$$\text{Stress Ratio, } S_E = \frac{P_1}{P_S} + P_2 \frac{2P_S - P_T}{P_T \times P_S}$$

b. Dual devices in a single case (equally rated, equally loaded):

$$S_E = \frac{2P_1}{P_T}$$

c. Three or more devices in a single case (all equally rated, unequally loaded):

$$\text{Stress Ratio, } S_E = \frac{P_1}{P_S} + (P_2 + P_4 \cdots P_N) \frac{NP_S - P_T}{P_T \times P_S}$$

d. Three or more devices (equally rated and equally loaded):

$$S_E = \frac{NP_1}{P_T}$$

3.2.2.6 Derating Versus Percent of Rating

Confusion is often caused by using the term "derating," in a numerical sense, when actually it refers to a general practice of operating below some maximum level. If a part is operated at 40 percent of rating, it should not be stated as "derated 60 percent", but as "operated at a percent of rating of 40 percent". "Percent derating" is not a valid numerical term.

Since the major environment degrading reliability is heat, it is normal to "derate" by decreasing the junction temperature. Assuming that temperature of the heat sink, etc., is fixed, derating is done and evaluated through a reduction of power.

3.3 Reliability

3.3.1 Reliability Assurance Tests

The control of high reliability part procurement specifications are provided by the Part Control Packages. The procurement specification includes quality assurance provisions and pre-usage conditioning requirements to assure compliance with the system duration and environmental requirements. These include extreme temperature cycling, acceleration, mechanical shock, and hermeticity testing for space service.

3.3.2 Reliability Assurance

The Part Control Packages require extended burn-in of parts (for 500 hours) and degradation analysis in selected instances. As a cost improvement, all destructive group B lot testing, which is extremely expensive when small numbers of parts are purchased, has been eliminated in favor of more extensive 100% stress screening and 100% inspection (such as internal visual and radiographic inspections).

3.3.3 Reliability Prediction Rationale and Derivation

This subsection outlines the general mathematical reasoning on which the reliability factors are based. It is quite possible, however, to estimate the reliability of a transistor from the charts and tables in 3.4 herein without a study of this subsection.

It is assumed that the device failure rate (λ_s) is composed of additive (λ) factors which have a mutual interaction with several product (π) factors, and also of one or more other additive (λ) factors. In the case of transistors, this expression is:

$$\lambda_s = \lambda_b \left(\pi_E \cdot \pi_A \cdot \pi_R \cdot \pi_{SS} \cdot \pi_C\right) \quad \Sigma_E$$

These factors are detailed in the explanation of their usage in 3.4 herein. The derivation of this expression is a special case of the general model (see table I for values of constants):

$$\lambda_b = Ae \left(\frac{(T + 273 + \theta_{RJ}S}{N_T}\right)^G e\left(\frac{T + 273 + \theta_{RJ}S}{T_O}\right)^P$$

Where A = Failure rate scaling factor.

N_T, T_O, G, and P = Curve-shaping factors for a given part type.

θ_{RJ} = Thermal resistance, in $^{\circ}C$ or $^{\circ}K$ per multiples of unit rating, from reference (ambient or heat sink as applicable) to device junction.

T = Ambient operating temperature in $^{\circ}C$.

$$S = \text{Electrical stress ratio} = \frac{\text{operating power level}}{\text{rated max power at standard temperature}}$$

For a more exact determination of the electrical stress ratio, see 3.2 herein.

TABLE I. - CONSTANTS IN MATHEMATICAL MODEL

Constants	Silicon,NPN Transistors	Silicon,PNP Transistors	FET and MOSFET	Unijunction Transistors
A	0.027	0.085	0.075	7.81
T_O	448	448	448	448
N_T	-1052	-1324	-1162	-1779
G	-1.0	-1.0	-1.0	-1.0
θ_{J-A}	150°C/W rating	150°C/W rating	150°C/W rating	150°C/W rating
P	10.5	14.2	13.8	13.8

3.4 Failure Rate Computation

This section describes the computation of the failure rate of a transistor in a particular application and contains the necessary charts and graphs for such a computation. The computation is based on the model below.

3.4.1 General Mathematical Model

The failure rate for semiconductor devices (after screening of gross quality defects) is generally assumed to be constant with time for many thousands of hours. This failure rate can be modeled as follows:

$$\lambda_s = \lambda_b (\pi_E \pi_A \pi_R \pi_{SS} \pi_C) + \Sigma_E \text{ (percent/1000 hours)}$$

where:

λ_s = Failure rate of a semiconductor device

λ_b = Basic failure rate (a function of electrical stress and operating temperature)

π_E = Use environment adjustment factor

Σ_E = Use environment additive failure rate term

π_A = Application factor (linear, switching, detector)

π_R = Factor for expressing the rated power (watts)

π_{SS} = Secondary electrical (voltage) stress ratio

π_C = Complexity factor

Note that some of the parameters in the above model do not apply, or have a value of 1, for some part types. These details are explained in the following sections on specific part types.

3.4.2 Transistor Family Types

The transistors covered by prediction techniques in this section have been divided into basic families with generally similar reliability characteristics as shown in table II, below. Further breakdown relating to construction, usage, etc., is provided for in the π and Σ factors detailed for each part type.

TABLE II. - TRANSISTOR FAMILY GROUPS

Family Group	Transistor Type	Applicable Factors
I	Silicon, NPN Silicon, PNP	π_E π_A π_R π_{SS} π_C Σ_E
II	FET, Silicon, P Channel FET, Silicon, N Channel MOSFET, Silicon, P Channel MOSFET, Silicon, N Channel	π_E π_A π_C Σ_E
III	Unijunction	π_E and Σ_E

3.4.3 Group I Transistors

3.4.3.1 General

The applicable prediction model for group I transistors is:

$$\lambda_s = \lambda_b (\pi_E) (\pi_A) (\pi_R) (\pi_{SS}) (\pi_C) + \Sigma_E \text{ (percent/1000 hours)}$$

where:

λ_s = Transistor failure rate (percent/1000 hours)

λ_b = Base portion of the failure rate, derived from figures 3 through 6, and based on S_E (electrical stress ratio) and T (temperature). The environmental adjustment products (π) and additive factors (Σ), respectively, can be obtained from tables III through VII.

3.4.3.2 π_E, Use Environment Factor

The use environmental factor expresses the general surroundings and caliber of maintenance that the part will experience. It is proportional to the electrical or internally imposed stresses in the device. See table III for values.

TABLE III. - π_E AND Σ_E, BASED ON ENVIRONMENTAL SERVICE CONDITION FOR GROUP I TRANSISTORS

Environment	Symbol	π_E	Σ_E
Ground, Fixed	G_f	4.75	0.0010
Space Flight	S_f	1.6	0.0005
Satellite, Launch	S_l	40.0	0.0210

3.4.3.3 Σ_E, Use Environment Additive Term

In contrast to the use environment factor, Σ_E represents the hazard of failure due to externally imposed environmental stresses. In the broad sense these stresses are interpreted as not only shock, vibration, cold, etc., but also the human effect (the technician with the soldering iron, etc.). Since these hazards exist irrespective of electrical stresses, this is considered an independent Σ_E or additive factor, rather than an interacting product factor such as π_E. See table III for values.

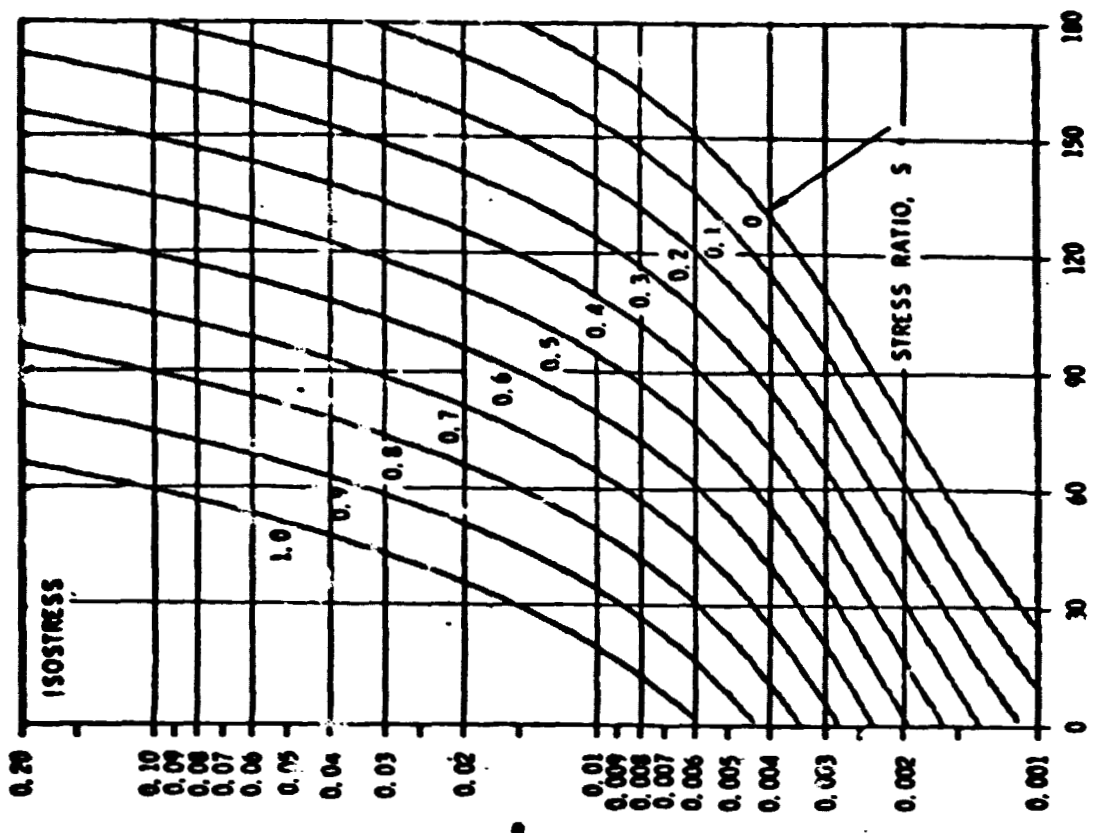


FIGURE 4. DETERMINATION OF FAILURE RATE, λ_b, AS RELATED TO STRESS RATIO, T, FOR GROUP I, Si, PNP TRANSISTORS

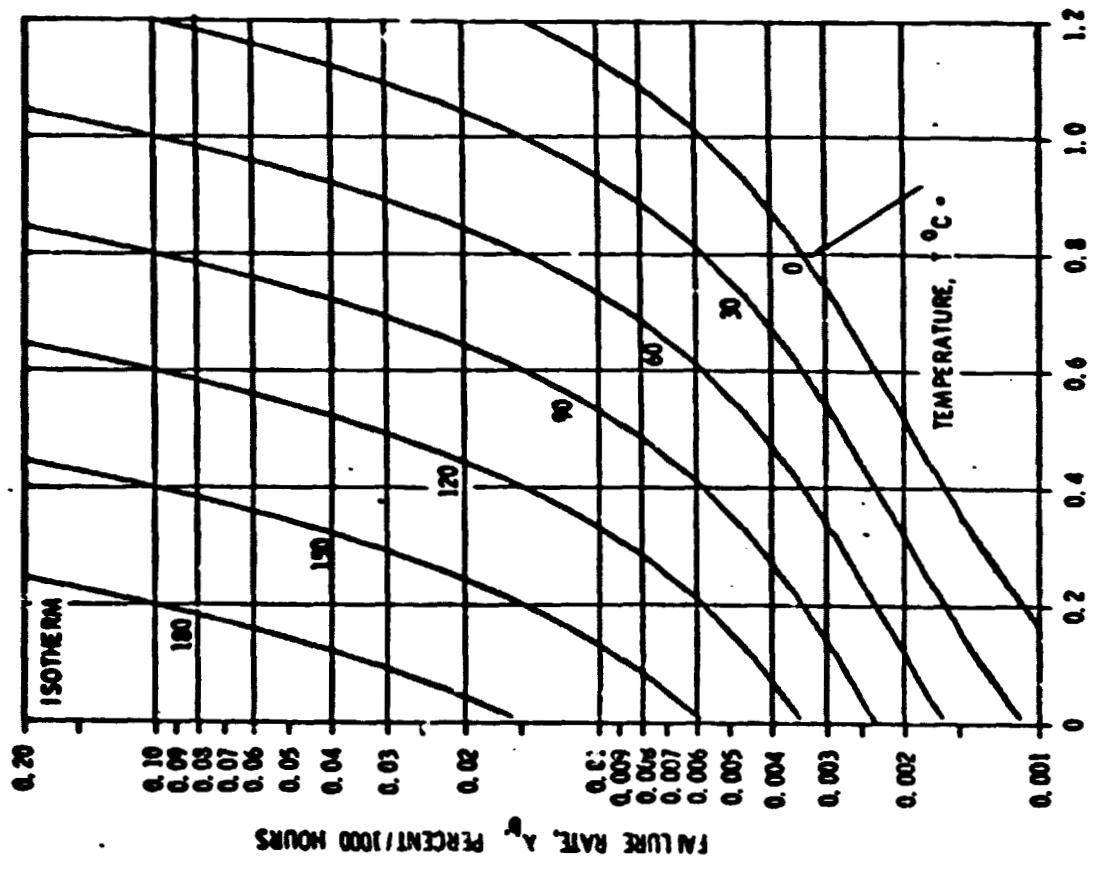


FIGURE 3. DETERMINATION OF FAILURE RATE, λ_b, AS RELATED TO STRESS RATIO, S, FOR GROUP I, Si, PNP TRANSISTORS

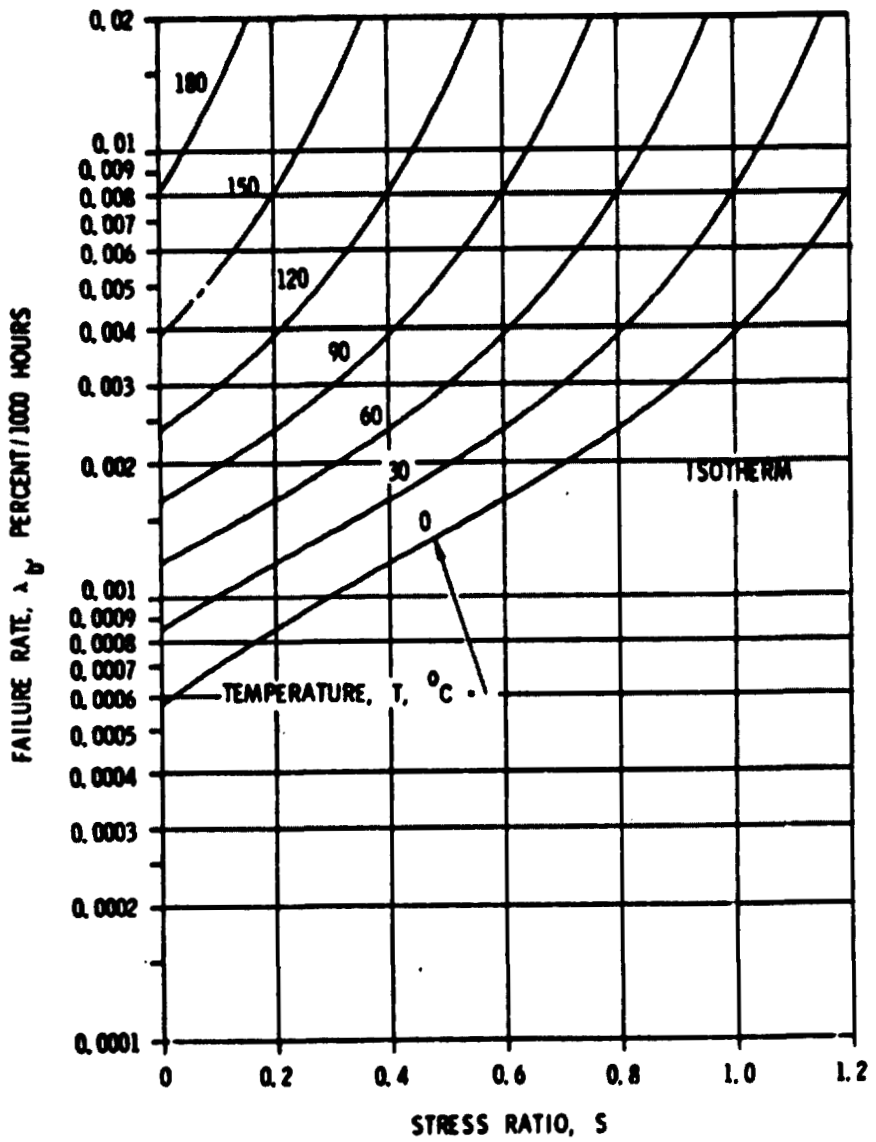


FIGURE 5. DETERMINATION OF FAILURE RATE, λ_b, AS RELATED TO STRESS RATIO, S, FOR GROUP I, Si, NPN TRANSISTORS

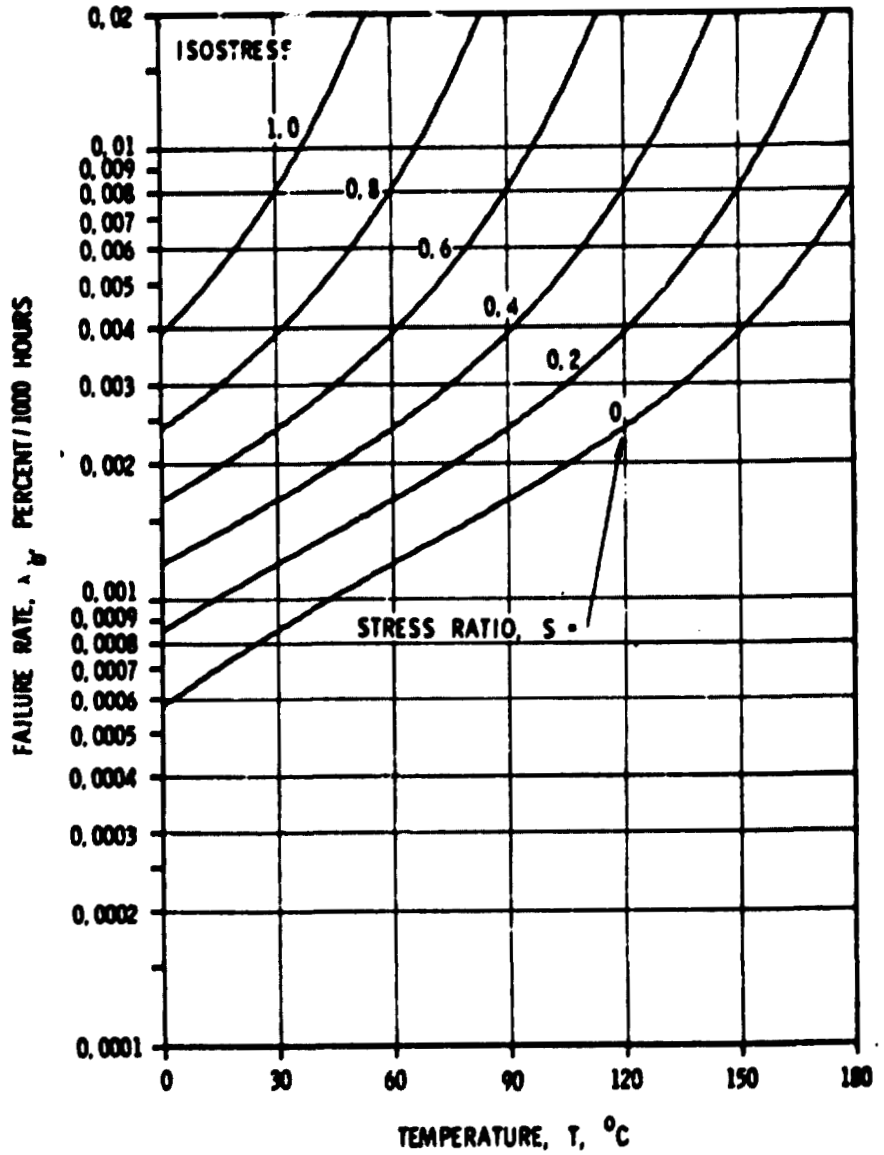


FIGURE 6. DETERMINATION OF FAILURE RATE, λ_b, AS RELATED TO TEMPERATURE, T, FOR GROUP I, Si, NPN TRANSISTORS

3.4.3.4 π_A, Application Factor

The application factor expresses the criticality of output demanded of the device. The identical part, behaving in identical fashion, could be reliable (satisfactory) in a simple digital/switching application, but has a much higher probability of degrading out of tolerance in a linear or more critical operation. See table IV for values.

TABLE IV. - APPLICATION FACTOR, π_A, FOR GROUP I TRANSISTORS

Application	π_A
Linear (AC)	1.0
Linear (DC)	2.0
Low Noise (Audio)	1.5
High Frequency (RF)	3.0
Low Noise (RF)	4.0
Logic Switching	0.5

3.4.3.5 π_R, Electrical Rating Factor

There is a reliability hazard inherent in the size or power rating of the device, irrespective of whether it is operated at a high or low stress ratio percentage of this rating. This hazard is expressed by π_R, which varies with the power (wattage) rating of the device. See table V for values.

TABLE V. - RATING FACTOR, π_R, FOR GROUP I TRANSISTORS

Power Rating (watts)	π_R
0 to 100 mW	1.0
> 100 to 500 mW	1.0
> 0.5 to 1.0	1.0
> 1.0 to 5	1.5
> 5.0 to 20	2.0
> 20	2.5

3.4.3.6 π_{SS}, Secondary Electrical Stress Factor

The factor π_{SS} deals with internal electrical stresses, and relates to S_{SS} (the stress ratio for a second significant parameter -- in the case of transistors, voltage). It is determined as OPERATING V_{CE}/RATED V_{CE} x 100. See table VI for values.

TABLE VI. - VOLTAGE STRESS FACTOR, π_{SS}, FOR GROUP I TRANSISTORS

S_S (percent)[1/]	π_{SS}
100	3.0
90	2.25
80	1.65
70	1.2
60	1.0
50	0.75
40	0.48
30	0.36
20	0.30
10	0.30
0	0.30

[1/] Voltage stress, $S_S = \frac{\text{Operating } V_{CE}}{\text{Rated } V_{CE}} \times 100$

3.4.3.7 π_C, Complexity Factor

The complexity factor expresses the construction complexity hazard of multiple devices, and each transistor in a case is subject to π_C as well as the other factors in the λ_s equation.

If only one transistor in a case is to be used in the circuit, the other factors can be neglected and π_C becomes 1.0 and does not influence the expression. See table VII for values.

TABLE VII. - COMPLEXITY FACTOR, π_C, FOR GROUP I TRANSISTORS

Complexity[1/]	π_C
Single Transistor	1.0
Dual (Unmatched)	0.7
Dual (Matched)	1.2
Darlington	0.8
Dual Emitter	1.1
Multiple Emitter	1.2
Complementary Pair	0.7

[1/] Each transistor in a case must be treated individually for the complexity factor. Its failure rate, λ_b, is determined by its application, modified by the other π factors and then multiplied by this complexity factor. If only one transistor of a pair is involved, it is treated as an independent item, and $\pi_C = 1.0$.

3.4.4 Group II (FET) Devices

3.4.4.1 General

The prediction model for FET devices is:

$$\lambda_s = \left[\lambda_b (\pi_E)(\pi_A)(\pi_C)\right] + \Sigma_E \text{ (percent/1000 hours)}$$

where λ_s is the FET device failure rate (percent/1000 hours) and π_E, π_A, π_C, and Σ_E are modifiers of λ_b as explained in 3.3.3 herein for transistors. The specific figures and tables applying for Group II devices are as follows:

λ_b: See figures 7 and 8

Σ_E and π_E: See table VIII

π_A: See table IX

π_C: See table X

TABLE VIII.- π_E AND Σ_E, BASED ON ENVIRONMENTAL SERVICE CONDITION FOR GROUP II FIELD EFFECT TRANSISTORS

Environment	Symbol	π_E	Σ_E
Ground, Fixed	G_f	14.0	0.015
Space Flight	S_f	4.5	0.008
Satellite, Launch	S_l	60.0	0.045

TABLE IX.- APPLICATION FACTOR, π_A, FOR GROUP II FIELD EFFECT TRANSISTORS

Application	A
Linear (AC)	1.0
Linear (DC)	2.0
Logic Switch	0.5
Low Noise (Audio)	1.5
High Frequency (RF)	3.0
Low Noise (RF)	4.0

TABLE X.- COMPLEXITY FACTOR, π_C, FOR GROUP II, FIELD EFFECT TRANSISTORS

Complexity 1/	π_C
Single device	1.0
Dual (unmatched)	0.7
Dual (matched)	1.2
Complementary pair	0.7
Tetrad	1.1

1/ See footnote, table VII.

3.4.5 Group III (Unijunction Devices)

3.4.5.1 General

The prediction model for unijunction devices is:

$$\lambda_S = \lambda_b (\pi_E) + \Sigma_E \text{ (percent/1000 hours)}$$

where λ_S is the unijunction device failure rate (percent/1000 hours), and π_E and Σ_E are modifiers of λ_b as specified in 3.3.3 herein for transistors. The specific figures and tables applying for Group III devices are as follows:

λ_b: See figures 9 and 10

π_E: See table XI

Σ_E: See table XI

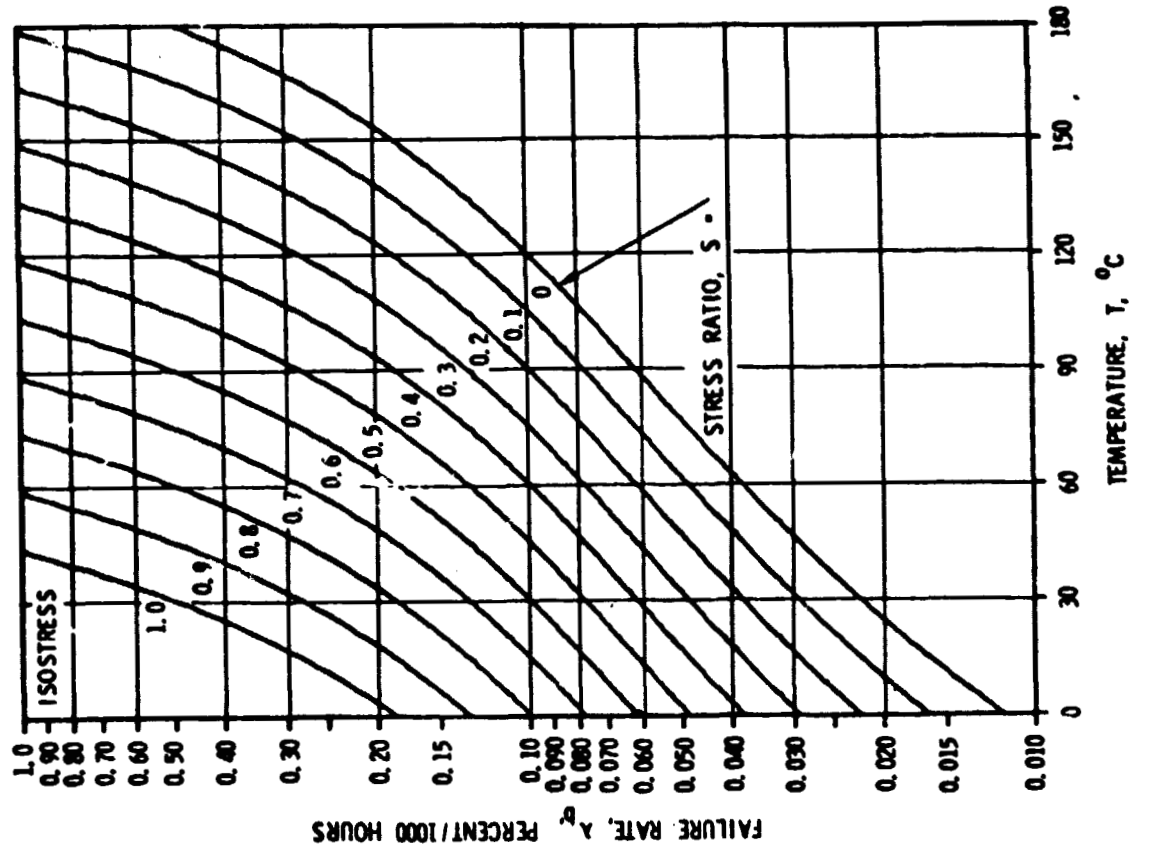


FIGURE 8. DETERMINATION OF FAILURE RATE, λ_b, AS RELATED TO TEMPERATURE, T, FOR GROUP II FIELD EFFECT TRANSISTORS

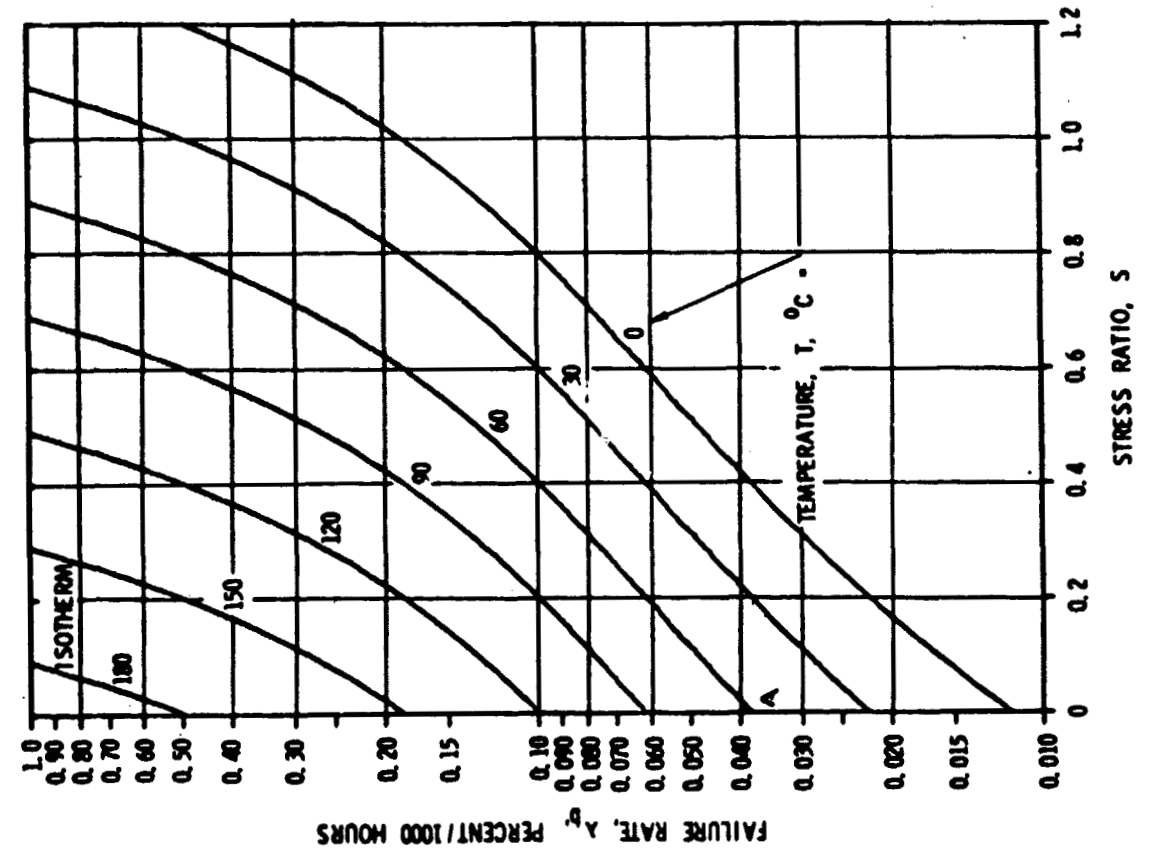


FIGURE 7. DETERMINATION OF FAILURE RATE, λ_b, AS RELATED TO STRESS RATIO, S, FOR GROUP II FIELD EFFECT TRANSISTORS

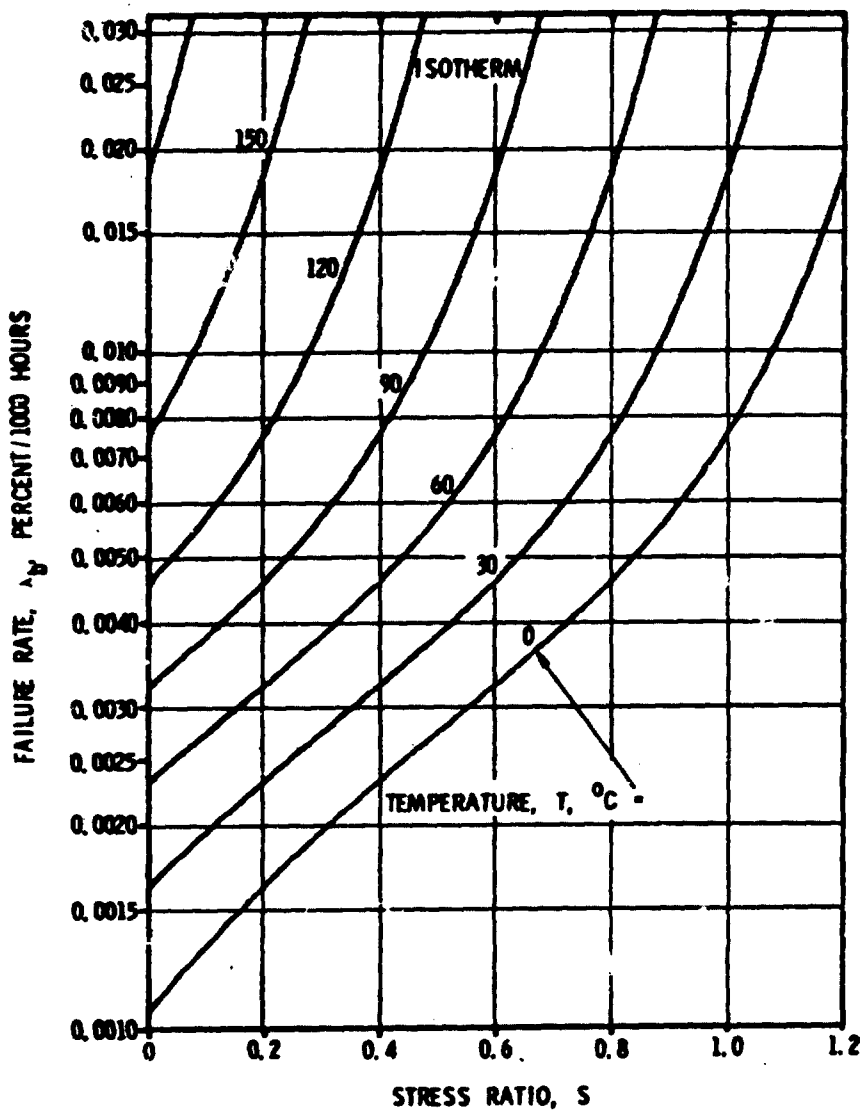


FIGURE 9. DETERMINATION OF FAILURE RATE, λ_b, AS RELATED TO STRESS RATIO, S, FOR GROUP III UNIJUNCTION TRANSISTORS

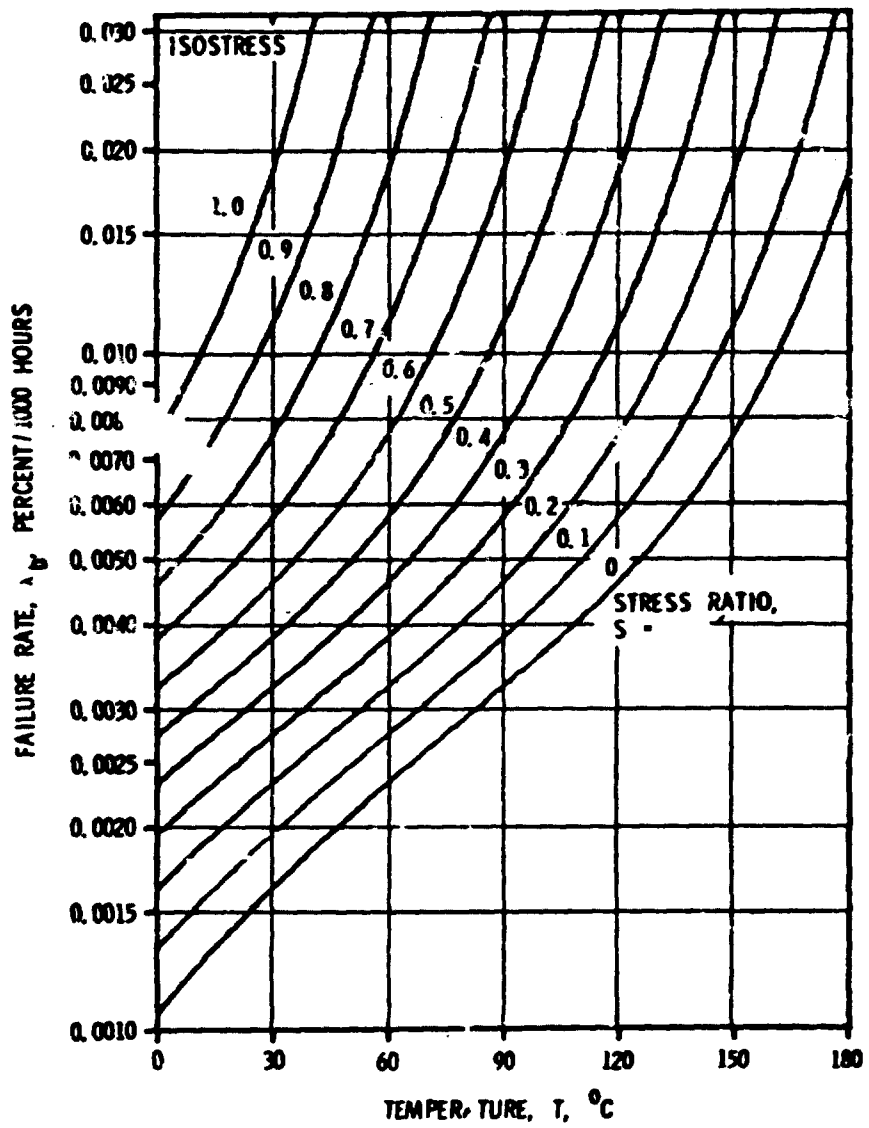


FIGURE 10. DETERMINATION OF FAILURE RATE, λ_b, AS RELATED TO TEMPERATURE, T, FOR GROUP III UNIJUNCTION TRANSISTORS

TABLE XI.- π_E AND Σ_E, BASED ON ENVIRONMENTAL SERVICE CONDITION FOR GROUP III, UNIJUNCTION TRANSISTORS

Environment	Symbol	π_E	Σ_E
Ground, Fixed	G_f	6.7	0.085
Space Flight	S_f	2.5	0.009
Ground, Mobile	G_m	22.5	0.090
Satellite, Launch	S_l	37.0	0.090

3.4.5 Summary and Examples

3.4.6.1 Summary

To compute the failure rate of a transistor which belongs to one of the three families covered (transistors, unijunctions, FETs), the applicable formula listed in tables XII, XIII, or XIV below should be used. The values of the factors, as directed in tables XII, XIII, and XIV, should be determined before performing the computation. An example is given at the end of the tables.

TABLE XII.- PREDICTION PROCEDURE FOR TRANSISTORS (GROUP I)

Part failure rate model (λ_p)

$$\lambda_p = \lambda_b \left(\pi_E \times \pi_A \times \pi_R \times \pi_{SS} \times \pi_C \right) + \Sigma_E \text{ (percent/1000 hours)}$$

where the factors are shown in the following tables and figures:

λ_b: See figures 3 thru 6

π_E: See table III

π_A: See table IV

π_R: See table V

π_{SS}: See table VI

π_C: See table VII

Σ_E: See table III

TABLE XIII.- PREDICTION PROCEDURE FOR FIELD EFFECT TRANSISTORS (GROUP II)

Part failure rate model (λ_p)

$$\lambda_p = \lambda_b \left(\pi_E \times \pi_A \times \pi_C\right) + \Sigma_E \text{ (percent/1000 hrs)}$$

where the factors are shown in the following tables and figures:

λ_b: See figures 7 and 8

π_E: See table VIII

π_A: See table IX

π_C: See table X

Σ_E: See table VIII

TABLE XIV.- PREDICTION PROCEDURE FOR UNIJUNCTION TRANSISTORS (GROUP III)

Part failure rate model (λ_p)

$$\lambda_p = \lambda_b \left(\pi_E\right) + \Sigma_E \text{ (percent/1000 hrs)}$$

where the factors are shown in the following tables and figures:

λ_b: See figures 9 and 10

π_E: See table XI

Σ_E: See table XI

3.4.6.2 Example: Determining the Failure Rate of a Transistor

Given: A silicon, NPN, general-purpose transistor is operating in a linear (ac) mode at 0.4 of its rated maximum power. It will be used in a ground-fixed service environment, at 30° C ambient temperature, operating at 60 percent of maximum voltage, and rated at 500 mW.

Find: The failure rate of the transistor.

Step 1. To derive the base failure rate, λ_b, the electrical stress ratio must first be calculated, in the following manner: Stress ratio = operating power (P_{op})/rated maximum power (P_{max}); for this example, S = 0.4.

Step 2. The values of the electrical stress ratio (0.4) and the ambient operating temperature (30° C) are inserted into figures 5 or 6, to arrive at the base failure rate, λ_b, of 0.0016 percent/1000 hours.

Step 3. From table III, the value of π_E is 4.75 and Σ_E is 0.0010 for a ground-fixed service environment.

Step 4. From table IV, the value of π_A is 1.0 for a linear (ac) application.

Step 5. From table V, the value of π_R is 1.0 for a transistor rated at 500 mW.

Step 6. To derive the π_{SS} term, the voltage stress must first be computed, in the following manner:

Voltage stress (S_{SS}) = operating V_{CE}/rated V_{CE} x 100
= 60 percent (given)

For an S_{SS} of 60 percent, the value of π_{SS} (from table VI) is 1.0.

Step 7. From table VII, the value of π_C for a single transistor is 1.0.

Step 8. To compute the total failure rate (λ_p), the λ_b terms and π terms are multiplied and then added to the Σ_E term, as shown in the model:

$$\lambda_p = \lambda_b (\pi_E \times \pi_A \times \pi_R \times \pi_{SS} \times \pi_C) + \Sigma_E$$

$$= 0.0016 (4.75 \times 1.0 \times 1.0 \times 1.0 \times 1.0) + 0.0010$$

$$= 0.0086 \text{ percent/1000 hours.}$$

4. ABBREVIATIONS, SYMBOLS, AND DEFINITIONS

Abbreviations and symbols are defined in the applicable paragraph of this specification.

REVISION RECORD

REV	AUTHORITY	DESCRIPTION	RELEASE	
			DATE	APPROVAL

CONTENTS

NSL-B401/1

DETAIL DESIGN APPLICATION SPECIFICATION FOR

NASA SPECIAL LONG-LIFE (NSL) TRANSISTOR, TYPE NSL-401/1

1. SCOPE

1.1 Applicability

This specification is part of the system of Part Control Packages for controlling NASA Special Long-Life (NSL) parts, described in NASA CR-66742-1. This specification is detail section B of Part Control Package NSL-401, and defines the detail design application requirements for a silicon, NPN transistor intended for use in low-level, low-noise amplifiers. This transistor is similar to JEDEC type 2N2484.

2. APPLICABLE DOCUMENTS

2.1 Documents

The following documents form a part of this specification to the extent specified herein. Unless otherwise specified herein, the issue in effect on the date of the part procurement contract shall apply.

STANDARDS

Military

MIL-STD-202	Test Methods for Electronic and Electrical Component Parts
MIL-STD-1276	Leads, Weldable, for Electronic Component Parts

SPECIFICATIONS

Military

MIL-S-19500	Semiconductor Devices, General Specification for

NASA

NSL-B401	General Design Application Specification for NASA Special Long-Life (NSL) Transistors

(The documents listed in 2.1 of NSL-B401 form a part of this document to the extent specified herein and within the limitations of 2.2 of NSL-B401.)

2.2 Conflicting Requirements

The requirements of 2.2 of NSL-B401 apply.

3. DESIGN APPLICATION REQUIREMENTS

3.1 Design Limitations

3.1.1 Maximum Ratings

Unless otherwise specified, the maximum ratings at an ambient temperature of 25° ± 3°C shall be as shown in table I herein.

TABLE I. - MAXIMUM RATINGS

Storage temperature range	-65° to +200° C
Operating temperature range	-55° to +150° C
Lead soldering temperature	300° C
Collector-to-base voltage, emitter open	60 V
Collector-to-emitter voltage, base open	60 V
Emitter-to-base voltage, collector open	6 V
Collector current	50 mA
Power dissipation, free air (25° C amb)	0.36 W
Derate above 25° C	2.06 mW/°C
Power dissipation, heat sink (25° C case)	1.2 W
Derate above 25° C	6.85 mW/°C

3.1.2 Electrical Characteristics

The electrical characteristics shall be as specified in table II and figure 1 herein.

3.1.3 External Physical Characteristics

The external physical characteristics shall be as specified in figure 2 herein.

TABLE II. - ELECTRICAL CHARACTERISTICS

Parameter	Min	Typ	Max	Conditions 1/
h_{FE}		430	800	I_C = 10 mA, V_{CE} = 5.0 V
h_{FE}	250	450		I_C = 1 mA, V_{CE} = 5.0 V
h_{FE}	200	430		I_C = 500 µA, V_{CE} = 5.0 V
h_{FE}	175	375		I_C = 100 µA, V_{CE} = 5.0 V
h_{FE}	100	290	500	I_C = 10 µA, V_{CE} = 5.0 V
h_{FE}	30	200		I_C = 1 µA, V_{CE} = 5.0 V
BV_{CBO}	60 V			I_C = 10 µA
BV_{CEO} (sus)	60 V			I_C = 10 mA pulsed
BV_{EBO}	6 V			I_E = 10 µA
V_{BE} (on)	0.5 V	0.57 V	0.7 V	I_C = 100 µA, V_{CE} = 5.0 V
V_{CE} (sat)		0.2 V	0.3 V	I_C = 10 mA, I_B = 0.1 mA
I_{CBC}		0.1 nA	10 nA	V_{CB} = 45 V
I_{CEO}		0.1 nA	2.0 nA	V_{CE} = 5.0 V
I_{CBO}		0.2 µA	10 µA	V_{CB} = 45 V, T_A = 150° C
NF		1.8 db	7.5 db	I_C = 10 µA, V_{CE} = 5V, f = 100 Hz
NF		1.8 db	3.0 db	I_C = 10 µA, V_{CE} = 5V, f = 1 kHz
NF		0.6 db	2.0 db	I_C = 10 µA, V_{CE} = 5V, f = 10 kHz
NF		2.0 db	3.0 db	I_C = 10 µA, V_{CE} = 5V, f = 15.7 kHz
$\lvert h_{fe} \rvert$	3.0	4.0		V_{CE} = 5.0 V, I_C = 50 µA, f = 5.0 MHz
$\lvert h_{fe} \rvert$	2.0	2.6	7.0	V_{CE} = 5.0 V, I_C = 500 µA, f = 30 MHz

1/ At T_A = 25°C, unless otherwise specified.

TABLE II. - ELECTRICAL CHARACTERISTICS (continued)

Parameter	Min	Typ	Max	Conditions 1/
h_{fe}	50	400	900	V_{CE} = 5.0 V, I_C = 1.0 mA, f = 1.0 KHz
h_{ie}	3.5 KΩ	15 KΩ	24 KΩ	V_{CE} = 5.0 V, I_C = 1.0 mA, f = 1.0 KHz
h_{oe}		15 μmho	40 μmho	V_{CE} = 5.0 V, I_C = 1.0 mA, f = 1.0 KHz
h_{re}		425 x 10^{-6}	800 x 10^{-6}	V_{CE} = 5.0 V, I_C = 1.0 mA, f = 1.0 KHz
C_{obo}		3.5 pf	5.0 pf	V_{CB} = 5.0 V, I_E = 0, 0.1 ≤ f ≤ 1 MHz

1/ At T_A = 25° C, unless otherwise specified.

3.1.4 Recommended Usage

The NSL-401/1 transistor is a low-noise, low-power device with high gain over a wide range of collector current. It should find extensive usage as the first stage in small-signal amplifiers, or the first of several stages in extremely low-noise amplifiers. Because of its high current gain, the device will also find applications as a reference amplifier, and its usage may allow a reduction in parts in amplifiers having several stages.

As a low-noise amplifier, this device should be operated at low collector-emitter voltages and low collector current levels. To obtain the lowest noise figures, care should be exercised in design to provide the proper source impedance. (Refer to figure 1 herein for the best low-noise performance.)

3.1.5 Application Review

3.1.5.1 Power

Under no conditions of operation shall the junction temperature be allowed to exceed 200°C (refer to the power derating

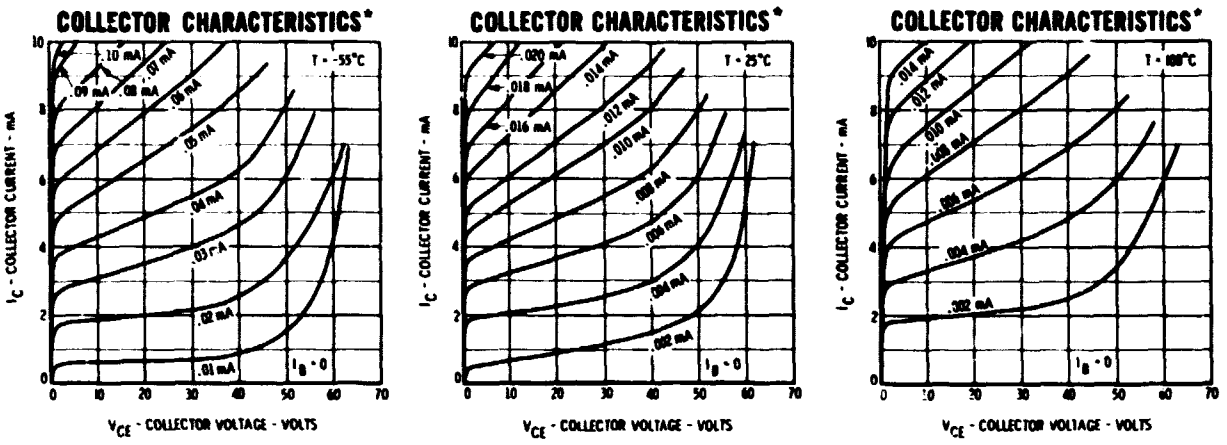
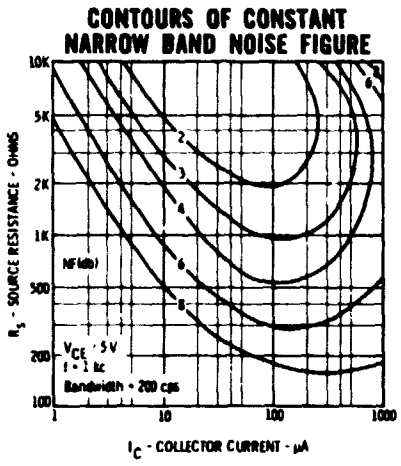
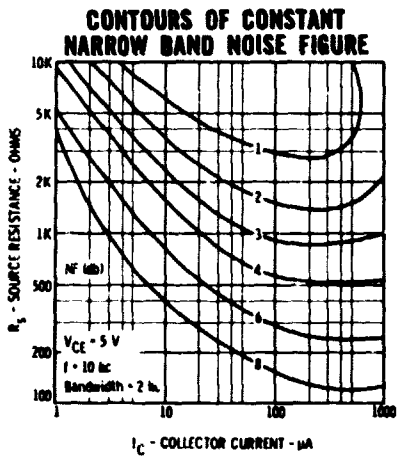
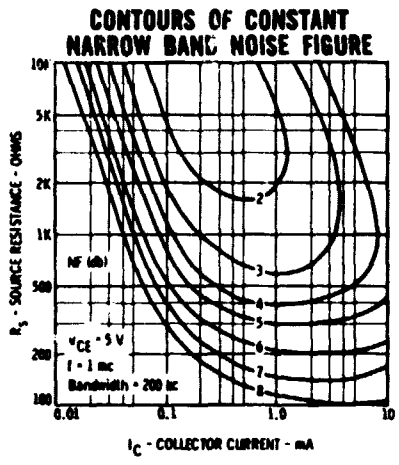
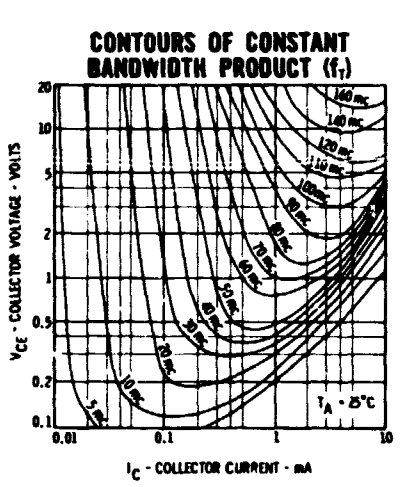


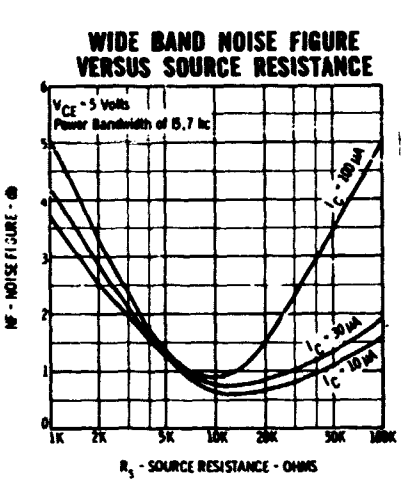
FIGURE 1. TYPICAL PARAMETER CURVES.

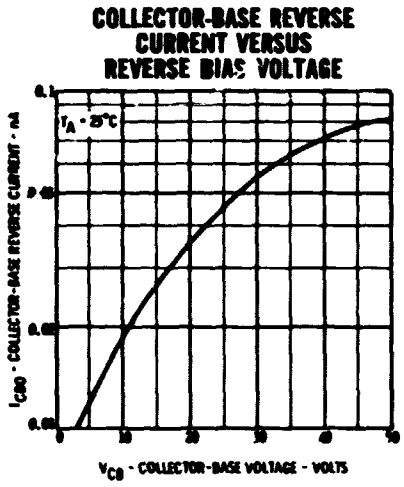




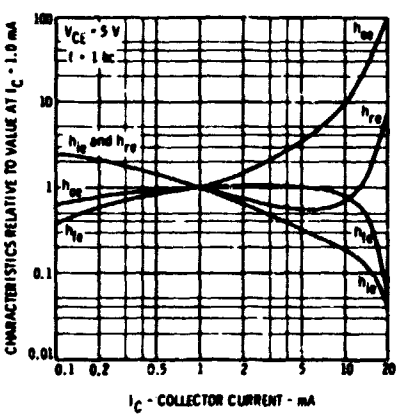


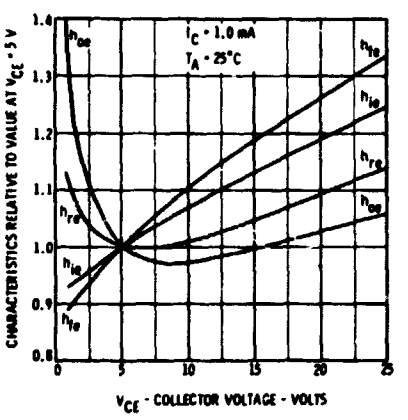






COMMON EMITTER CHARACTERISTICS





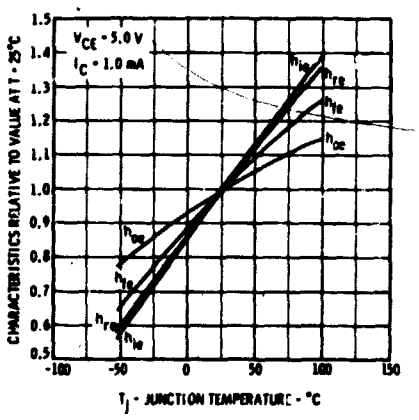
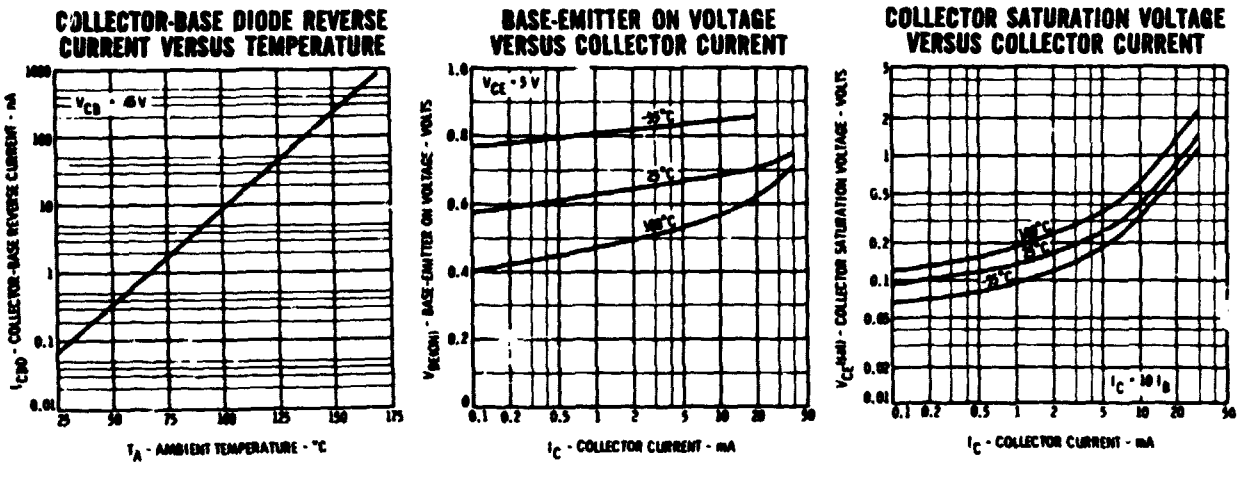


FIGURE 1.--Continued



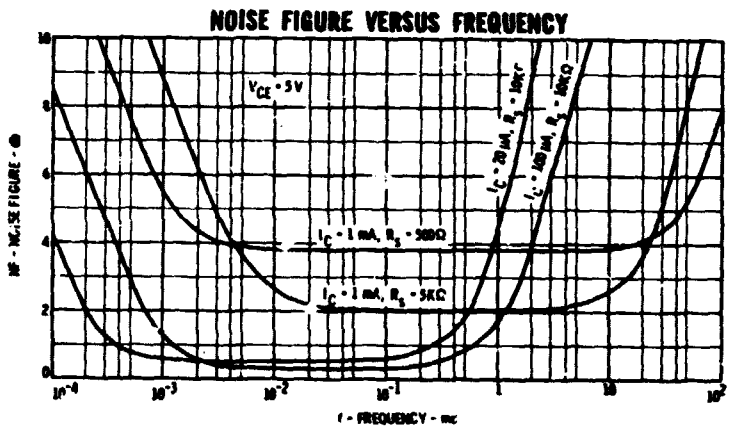
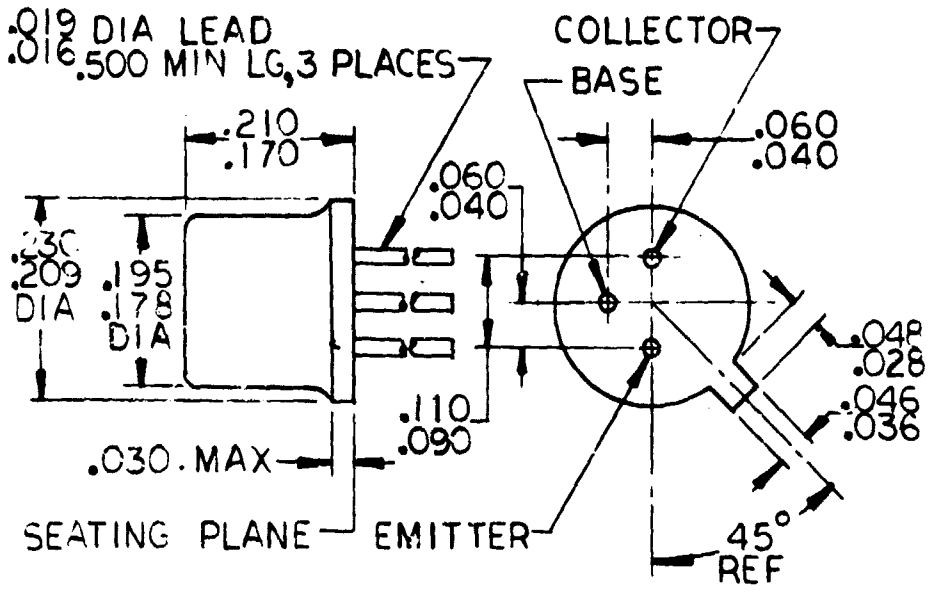


FIGURE 1.--Concluded.



NOTES:

1. Leads: MIL-STD-1276, Type K
2. Collector connected to case
3. Weight: 0.43 gm
4. Case: Hermetically sealed

FIGURE 2. EXTERNAL PHYSICAL CHARACTERISTICS.

requirements, 3.2.1 herein.) Average power dissipation shall be in accordance with the Reliability Derating Information, 3.3 herein, to realize failure rates consistent with system requirements.

3.1.5.2 Voltage

Maximum allowable voltages for this part (V_{CBO} = V_{CEO} = 60 V, V_{EBO} = 6 V) are listed in table I, Maximum Ratings. These values shall be reduced at least 15% to allow for changes with age. Further reduction increases reliability considerably. (Refer to table VI of the general design application specification, MCL-B401.)

3.1.5.3 Current

This device shall be used in applications where the maximum current is less than 20 mA. The maximum rating, 50 mA, is conservative.

3.1.5.4 Temperature

The maximum allowable storage ard junction temperature is 200°C. Exposure to temperatures above 200°C may cause permanent damage to the transistor die. Temperatures below -65°C may cause excessive thermal stress to be developed in the metal and glass package. The device shall not be subjected to temperatures below -65°C.

3.1.5.5 Vibration, Shock, and Acceleration

The device will withstand, without degradation, vibration levels of 20 G at frequencies from 10 to 2,000 Hz, acceleration levels of 30,000 G, and shock levels of 1,500 G.

3.1.5.6 Atmospheric Conditions

The device is hermetically sealed, and altitude operation is unlimited. It will meet the moisture resistance and salt spray requirements of MIL-STD-202, methods 106 and 101, respectively.

3.1.5.7 Radiation

The device is not hardened to radiation.

3.1.5.8 Worst Case Analysis

The worst case values of current gain, leakage currents, and small-signal parameters shall be analyzed in the design review.

3.2 Derating Procedures

The requirements of 3.2 of NSL-B401 apply.

3.2.1 Power Derating

Power derating shall be as specified in table III and figure 3 herein.

3.3 Reliability

The requirements of 3.3 of NSL-B401 apply.

3.4 Failure Rate Computation

To determine the failure rate for parts covered by this specification, the failure rate model listed below should be used, with reference to the general design application specification, NSL-B401, as noted.

TABLE III. - POWER DERATING

Maximum allowable junction temperature	T_J max	200°C
Thermal resistance, junction-to-case	θ_{JC}	146°C/W
Thermal resistance, junction-to-air	θ_{JA}	486°C/W
Maximum power dissipation at 25°C case temperature	P_T	1.2 W
For case temperatures above 25°C (when using a heat sink), derate		6.9 mW/°C
Maximum power dissipation at 25°C ambient temperature	P_T	0.36 W
For ambient temperatures above 25°C (without a heat sink), derate		2.1 mW/°C

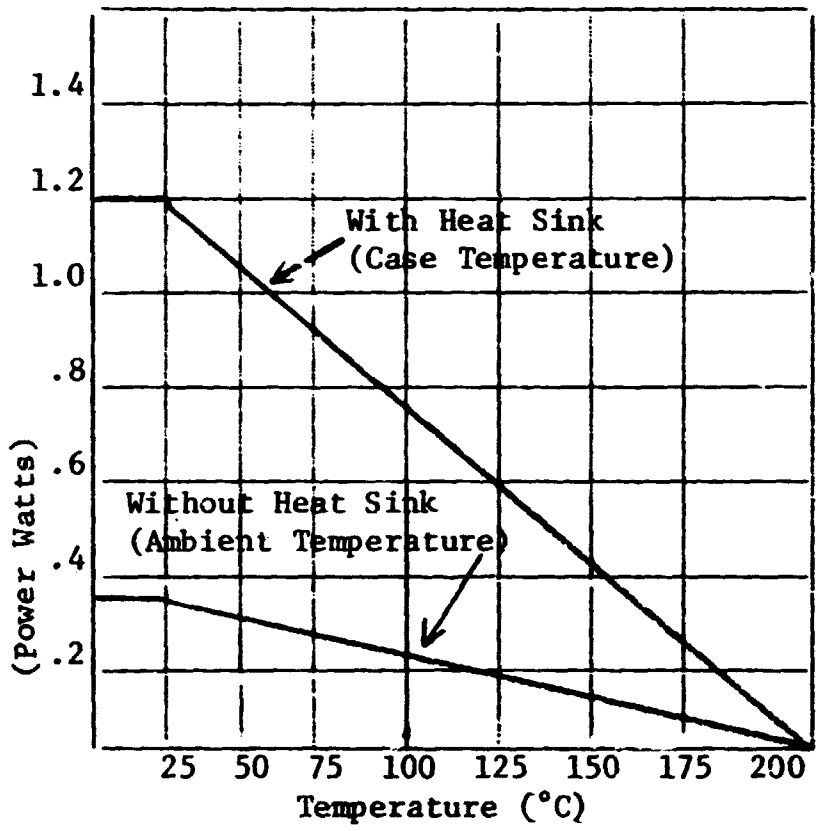


FIGURE 3. POWER DERATING.

The catastrophic failure rate, λ_S, in percent per 1000 hours, is computed as:

$$\lambda_S = \left[\lambda_b\ (\pi_E)\ (\pi_A)\ (\pi_R)\ (\lambda_{SS})\ (\pi_C)\right] + \Sigma_E$$

TABLE IV. - COMPUTATION OF FAILURE RATE FOR TYPE NSL-401/1 TRANSISTOR

Parameter	Description	Determine Value from NSL-B401
λ_B	Base failure rate	Figure 5 or 6
π_E	Environmental factor	Table III
π_A	Application factor	Table IV
π_R	Rating factor	$\pi_R = 1.0$
π_{SS}	Secondary stress factor	Table VI
π_C	Complexity factor	$\pi_C = 1.0$
Σ_E	Environmental additive term	Table III

4. ABBREVIATIONS, SYMBOLS, AND DEFINITIONS

The abbreviations, symbols, and definitions provided in NSL-B401 apply. Additional abbreviations, symbols, and definitions used herein are defined in MIL-S-19500.

REVISION RECORD

REV	AUTHORITY	DESCRIPTION	RELEASE	
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EXAMPLE

NSL-C401

GENERAL PART AND MANUFACTURER SELECTION AND CONTROL SPECIFICATION FOR NASA SPECIAL LONG-LIFE (NSL) TRANSISTORS

FEBRUARY 1969

CONTENTS

NSL-C401

GENERAL PART AND MANUFACTURER SELECTION AND CONTROL SPECIFICATION FOR NASA SPECIAL LONG-LIFE (NSL) TRANSISTORS

1. SCOPE

1.1 Applicability

This specification is part of the system of Part Control Packages for controlling NASA Special Long-Life (NSL) parts, described in NASA CR-66742-1. This specification is general section C of Part Control Package NSL-401, and defines the general requirements that a prime contractor shall observe for the selection and control of NSL parts. This specification and the applicable detail selection and control specification, NSL-C401/____, are mandatory whenever NSL transistors are specified.

2. APPLICABLE DOCUMENTS

2.1 Documents

The following documents form a part of this specification to the extent specified herein. Unless otherwise specified herein, the issue in effect on the date of the part procurement contract shall apply.

SPECIFICATIONS

NASA

NSL-C401/____	Detail Specification for Manufacturer Selection and Control
NSL-A401	General Procurement Specification for NASA Special Long-Life (NSL) Transistors
NSL-A401/____	Detail Procurement Specification for NASA Special Long-Life (NSL) Transistors

2.2 Conflicting Requirements

In the event of conflict between the requirements of this specification and any of the documents specified herein or in the applicable detail specification, the order of precedence shall be as follows:

a. The applicable NASA Special Long-Life (NSL) detail selection and control specification.

b. This general selection and control specification.

c. Specifications referenced herein or in the applicable detail selection and control specification.

3. METHODS AND REQUIREMENTS

3.1 General

The prime contractor shall select and control the qualification and procurement of NSL parts in accordance with the requirements of this specification and the applicable detail selection and control specification. The selection and control process shall consist of the following three phases:

Phase I. The prime contractor shall conduct a quality survey of the part manufacturer in accordance with the requirements and criteria of 3.2 of this specification and the applicable detail selection and control specification. Successful completion places the part manufacturer on the Manufacturer Eligibility List (MEL) and makes him eligible for a line certification survey as described in Phase II.

Phase II. The prime contractor shall conduct a line certification survey in accordance with the requirements and criteria of 3.3 of this specification and the applicable detail selection and control specification. Successful completion places the line on the Certification Line List (CLL), eligible to supply transistors to the specific NSL detail procurement specification for which the line is certified.

Phase III. The prime contractor shall, in accordance with the requirements and criteria of 3.4 of this specification and the applicable detail selection and control specification, negotiate and monitor the procurement of parts to the general procurement specification NSL-A401 and the applicable detail procurement specification. This action is contingent on the following:

a. The part manufacturer, required in the applicable detail procurement specification, is listed on the MEL.

b. The part manufacturer's line for producing the part is listed on the CLL.

c. The general procurement specification NSL-A401 and the applicable detail procurement specification are both approved by the prime contractor and the cognizant NASA installation.

Upon verifying the satisfactory completion of the requirements of NSL-A401 and the applicable detail procurement specification, the prime contractor shall approve the procurement lot as accepted and qualified NSL parts.

3.2 Part Manufacturer Qualification (Phase I)

3.2.1 Part Manufacturer Survey

A complete survey of the part manufacturer's shall be made. The part manufacturer shall provide adequate assurance of his capabilities to meet the requirements listed in this general specification.

3.2.1.1 Part Manufacturer Eligibility

All part manufacturers of transistors may have the opportunity to request, in writing, a part manufacturer survey for one or more particular transistors of interest to the NASA prime contractor. The right is reversed to consider part manufacturers for survey in order of current demand and usage. The NASA prime contractor shall respond with a questionnaire, as shown in appendix A herein, which the part manufacturer shall complete. Upon receipt of a satisfactorily completed questionnaire, the NASA prime contractor and the part manufacturer shall mutually agree to a time and place for the survey.

3.2.1.2 Resurvey Requirements

A part manufacturer survey will not need to be repeated as long as the part manufacturer produces and ships to the NASA prime contractors or subcontractors within a twelve-month period one or more lots of transistors in a satisfactory manner unless a major change from the findings of the last part manufacturer survey occurs. Examples of such major changes include a substantial change of ownership, simultaneous loss of several key personnel, or deterioration in delivery and quality record.

3.2.1.3 Survey Data

The part manufacturer shall provide the survey team with data that will be used for making a decision. This data shall include the following:

a. Organization chart that includes the key organizational blocks and delineates lines of authority and responsibility. The segment responsible to management for overall reliability shall be clearly identified and described. The organizational relationship between engineering, production, reliability, and quality assurance, procurement, and management shall be clearly indicated.

b. Short biographical sketches of all key personnel.

c. List of government contracts held and major purchase orders received, with a statement of performance (price, delivery, yield, and rejection rate).

d. Number of surveys made by NASA centers, prime contractors and subcontractors during previous 6- and 12-month periods.

e. Description of the failure analysis program, including failure defect analysis capabilities, failure mode detection, and corrective action programs.

f. Product-assurance-oriented training programs, covering all phases of activity involved in producing transistors.

g. Product assurance controls applied to subcontractors and vendors in connection with their supply of parts and materials, as applicable.

h. Manufacturing flow chart for all production operations that identify in sequence the materials, processes, and inspections used and that list the document number and revision of the documentation covering these materials, processes, and inspections.

i. Lot control plan for the traceability of materials and processes used throughout the manufacturing cycle, including part identification.

j. Manufacturing line or lines for which the manufacturer wishes to obtain approval.

k. List of transistor orders delivered to NASA, prime contractors, or to subcontractors within the past 6 months.

3.2.2 Criteria for Part Manufacturer Qualification

In order to meet the qualification requirements, the part manufacturer must complete the questionnaire of appendix A herein, supply the survey data of 3.2.2.3 herein, and demonstrate standardization practices, process controls, documentation and change procedures, subcontractor and part manufacturer control methods, inspection methods, and storage techniques to the survey team.

3.2.2.1 Standard zation of Design Practices and Processing Procedures

The part manufacturer shall maintain continuous standization and control of design practices and processing procedures, and shall formalize his results for use by his design, drafting, fabrication, and inspection personnel. The part manufacturer's product-assurance organization shall be responsible for reviewing these standards for adequacy in meeting product-assurance requirements of purchase orders, and for monitoring and assuring that they are being followed. The part manufacturer shall review the specifications of all his subcontractors for compatibility with the requirements of this specification, and all specifications shall be submitted for inspection by the survey team, upon request. Typical areas to be covered in this standardization system include:

a. Process specifications

b. Fabrication, assembly, and machining specifications

c. Drafting practice and drawing specifications

3.2.2.2 Process Control Charts

Design and process control shall be monitored by the part manufacturer through control charts on appropriate product and process variables, tolerances, and other control techniques, as necessary.

3.2.2.3 Process Control Documentation

The part manufacturer shall completely document with specifications and procedures the procurement of parts and materials, materials inspection, transistor manufacturing processes, and inspections used to control these processes. The documentation shall include internal procedures for the control and revisions of all documents. This documentation shall be available for review by the survey team.

3.2.2.4 Specification and Drawing Control

The part manufacturer shall adequately control the issue of new or revised process specifications, inspection procedures, and procurement specifications, and shall provide for the recall of obsolete issues. The specification control (or equivalent activity) shall know the location of all operational issues of specifications. Specification revisions (and new issues) shall require approval by the appropriate levels of production, engineering, and product-assurance management. Proprietary process or design specifications shall be handled in the same (or equivalent) formal manner as other specifications although they need not be made available to the survey team nor be given the same distribution as other specifications. However, they shall be identified on product-flow charts by title and number. Specification control (or equivalent activity) shall have a record of issue locations and revision history.

Internal process, inspection, and other specifications shall show the customer revision status when customer drawings or specifications, provided for contracts, are referenced. When changes to customer specifications are received, the impact on active products shall be evaluated by comparison with the prior customer documents; they shall therefore, be maintained in a controlled, known location.

3.2.2.5 Proprietary Processes and Procedures

Documents describing proprietary processes need not be made available to the qualifying activity; but upon the specific request of this activity, an official of the part manufacturer shall show the qualifying acitivity, that the proprietary operations are completely defined and that proper controls are specified.

3.2.2.6 Control of Procurement Sources

The part manufacturer shall exercise control over his sources of supply contractors to assure the quality and reliability of purchased parts materials, and shall maintain records of product performance of each sub-tier part manufacturer. Chemical analyses and physical tests necessary to verify that raw materials conform to design requirements shall be periodically conducted on samples randomly selected from raw material received. Test results shall be incorporated as part of the inspection records for the lot selected.

3.2.2.7 Part Manufacturer's Receiving Inspection

Receiving Inspection shall operate under prescribed procedures and maintain a formal record system. A formal method of handling rejected material shall be in evidence. There shall be a segregation of accepted material, rejected material, and parts being held prior to final disposition by Receiving Inspection. The above control procedures shall be implemented for such items as packages, semiconductor materials and other types of substrates, piece parts, solder preforms, wires, and pure chemicals.

3.2.2.8 Nonconforming Materials

The part manufacturer shall provide for the review, control, and disposition of nonconforming materials. Each nonconformance shall be reviewed, a disposition shall be made by personnel vested with this responsibility, and positive corrective action shall be taken to prevent recurrence of similar discrepancies. Pertinent drawings and documentation shall be changed or initiated, as necessary.

3.2.2.9 Measuring and Test Equipment

The part manufacturer shall provide and maintain measuring and testing devices necessary to assure that transistors conform to technical requirements. These device shall be calibrated at established periods against certified measurement standards which have known valid relationships to national standards to assure continued accuracy. The objective is to assure that inspection and test equipment is adjusted, replaced, or repaired before it becomes inaccurate. The calibration of measuring and testing equipment shall be in conformance with MIL-STD-750. The part manufacturer shall assure the use of only those subcontractors and sources of supply which depend on calibration systems that effectively control the accuracy of measuring and testing equipment.

3.2.2.10 Inventory Control

From the time of material receipt through processing and completion of the transistors, all materials, parts and finished products shall be handled and stored in such a way that the identity and quality of such items will be preserved. All materials shall be used on a first-in, first-out basis. Materials and parts shall be transferred and transported in containers or equipment and by methods that will adequately protect their quality and identity.

3.3 Line Certification (Phase II)

3.3.1 Line Survey

The part manufacturer's semiconductor line or lines to be used for the fabrication of the transistors of interest to the NASA prime contractor shall be surveyed. The part manufacturer shall allow the survey team to witness all line activities with the exception of proprietary processes and shall assist in completing the Line Certification Checklist (appendix B herein).

3.3.1.1 Time of Survey

A line survey shall not be made prior to the request for part manufacturer qualification. The line survey may be made during the same time as the part manufacturer quality survey, or at a time negotiated between the prime contractor and the part manufacturer after receipt by the prime contractor of a formal request for line certification.

3.3.1.2 Resurvey Requirements

While the line is listed on the CLL, a resurvey will not be required unless a major change is effected in the line. Examples of such changes include a major process change, major equipment change, or change in inspection philosophy or procedures.

3.3.1.3 Line Survey Data

The part manufacturer shall provide the survey team with data that will be used for making a decision. This data shall include the following:

a. Process Flow Chart

The part manufacturer shall present a process flow chart of a typical transistor within each family for which certification is requested. The chart shall show the sequence of fabrication and inspection with symbols to distinguish between each process. Inspection shall include any measurement, test, or visual inspection performed. The process flow chart shall show the following additional items:

- Specification number for each fabrication or inspection step with date of latest revision.
- Organization performing each process (production, Q.C., etc.).
- Points at which statistical control records are kept.

b. Route Ticket

The part manufacturer shall demonstrate the use of a route ticket for each lot. The ticket shall show, as a minimum, the following information:

- Lot identification
- Name of operation
- Date of each operation
- Loss, if any, at each operation
- Operator's name.

c. Process Control Chart

The part manufacturer shall show a process control chart that has been prepared and maintained during the manufacture of transistors. The process control chart shall contain, as a minimum, the following information for each process (as applicable):

- Lot identification
- Process dates
- Number of items inspected
- Number or percent defective
- Median values (from mechanical and electrical tests)
- Range of values.

d. Documentation

The part manufacturer shall demonstrate that documentation is available to operating personnel on the line at all times.

3.3.2 Criteria for Line Certification

In order to meet the line certification requirements, the part manufacturer shall supply the line survey data of 3.3.1.3 herein, demonstrate the processes from wafer preparation through package sealing, and demonstrate the quality control techniques such as screening and traceability. Proprietary processes need not be demonstrated, but should be disclosed by process specification title, number, and revision designation.

3.3.2.1 Wafer Preparation

The part manufacturer shall demonstrate his control of wafers by indicating his techniques for the measurement of:

a. Thickness

b. Flatness

c. Parallelism

d. Surface roughness

e. Crystal perfection

f. Surface orientation

g. Lifetime

h. Oxygen content

i. Conductivity

j. Resistivity.

A 100% visual inspection on wafers, just prior to passivation, shall be demonstrated.

3.3.2.2 Surface Passivation

The part manufacturer shall specify:

a. The type of layers formed on the substrate (SiO_2, Si_3N_4, etc.).

b. The methods used to form the layers on the substrate (simple oxidation, oxidation during diffusion, sputtering, etc.).

c. The purpose of the layer (masking, passivating, or dielectric).

For each type of layer, each method of formation used, and for each purpose, the part manufacturer shall specify the thickness of layer to be grown or deposited in the 500 to 15,000 Å range and shall demonstrate the method used to measure the thickness of each layer.

The part manufacturer shall demonstrate the method used during production for detecting and measuring the density (no./cm^2) and size diameter in microns, of pinholes and cracks in a typical passivating layer.

The part manufacturer shall demonstrate his procedure and equipment used to make a profile of each type of furnace (oxidation) that forms a passivating layer. The part manufacturer shall stipulate the frequency at which each furnace is profiled, the profiling tool (potentiometer) is calibrated, and the profile is monitored. A record, such as a strip chart, shall be maintained of the monitor readings. This record shall be easily interpreted and kept near the furnace.

The part manufacturer shall demonstrate procedures for corrective action in the event the temperature drifts out of tolerance.

At least one monitor wafer shall accompany each batch of wafers through the passivation step.

3.3.2. Photolithography

The part manufacturer shall identify each type of photoresist in use (as negative, positive, KPR, AX-11, etc.). A change in viscosity by varying the amount of thinner shall not constitute a different type. The part manufacturer shall demonstrate the procedure for receiving and storing each type of photoresist. Control methods for the viscosity, solid residue, line width or definition, and pinhole count of each type of photoresist shall be indicated. The areas in which photomasking and etching are to be performed, including minimum requirements for dust, humidity, temperature, and lighting conditions, shall be defined. The part manufacturer shall demonstrate the application of photoresist. Application parameters and techniquires that depend on the subsequent etching (e.g. oxide or aluminum), shall be specified. The following processes and criteria shall be described by the part manufacturer:

- Method of mounting the wafer
- Temperature of photoresist during application
- Time of rotation
- Speed of rotation
- Time and temperature for drying of photoresist
- Viscosity range of the photoresist.

When the photoresist is baked, temperature control procedures shall be defined. The part manufacturer shall demonstrate the photoresist inspection procedures. He shall demonstrate the control of the photoresist exposure and development processes, including inspection of the photoresist pattern for irregularities such as pinholes, scratches, poor definition, lifting, and misregistration. Post bake, etching, and photoresist removal along with the inspection criteria shall be defined by the part manufacturer. The control of masks and masking techniques shall be demonstrated by the part manufacturer.

3.3.2.4 Juction Formation

The part manufacturer shall demonstrate to the survey team the following tests:

- Profiling of a diffusion tube
- Temperature check of a diffusion tube
- Temperature check of an epitaxial furnace
- Flow control of gases in diffusion
- Flow control of gases in epitaxy
- Loading and unloading diffusion tube
- Load and unloading an epitaxy furnace
- Measurement of sheet resistivity and junction depth on an epitaxial layer
- Measurement of emitter and base junction depths on a diffused transistor.

3.3.2.5 Metallization

The part manufacturer shall indicate each type of metallization used in production for which he requests qualification (Al-Al, Al-Au, Al-Mo-Au, etc.). The part manufacturer shall demonstrate the controls and the metallizing process as specified below.

- Temperature of substrate, vacuum, and heat -- I^2R relationship on metal to be deposited
- Monitoring of metal thickness
- Temperature, time, and environment during alloying

- Time, temperature, and concentration of etching
- Removal of etchant.

The part manufacturer shall explain the corrective action taken if tolerances for each control are exceeded.

3.3.2.6 Die Sort Inspection

The part manufacturer shall demonstrate a typical die sort inspection, including production and quality control. The equipment and visual aids used as guidelines, route ticket records, and accepted and rejected criteria shall be defined.

3.3.2.7 Die Mounting

The part manufacturer shall indicate:

a. The types of die (Ge, Si, GaAs, etc.)

b. The bonding agent used (tin-lead solder, epoxy, glass, etc.)

c. The package mount material (metal, beryllia, sapphire, etc.)

d. The design used (bumps, preform, etc.).

The part manufacturer shall demonstrate the temperature control when heat is used in mounting the chip.

3.3.2.8 Wire Bonding

The part manufacturer shall identify each type of bonding used in current production, such as:

a. Kind of lead (wire, beam-lead, flip-chip, etc.)

b. Size of lead (3/4 mil, 1 mil, 1 1/2 mil diameter, 1 x 12 micron beam, etc.)

c. Material (Al, Au, Cr-Au, etc.)

d. Technique (thermocompression nailhead, thermocompression wedge, ultrasonic, etc.)

3.3.2.9 Pre-seal Visual Inspection

The part manufacturer shall demonstrate a typical pre-seal inspection with respect to:

a. Type of die (flip-chip, eutectic bonded, etc.)

b. Type of interconnection (Al-Al, Al-Au, etc.)

3.3.2.10 Sealing

The part manufacturer shall indicate:

a. The types of seals used in production (TO-5, TO-18, etc.)

b. The technique used (beam welding, resistance welding, furnace cycle with solder, hot-press with solder, epoxy cure, etc.).

The part manufacturer shall demonstrate controls over temperature, time, and vacuum during pre-seal bake, and over the maintenance of records. The part manufactuer shall demonstrate that heat applied to the transistor for sealing shall be controlled so that no significant mechanical or electrical degradation will result. A maximum time shall be established for each sealing temperature.

3.3.2.11 External Inspection

The part manufacturer shall identify his procedures, visual aids, route tickets, and records on transistors prior to packaging.

3.3.2.12 Quality Control

The part manufacturer shall demonstrate his quality control methods to ensure the production of reliable transistors. These methods shall include:

a. 100% screening procedures

b. Failure analysis methods

c. Traceability techniques

d. Feedback methods from quality stations to line operations.

3.4.5 Procurement Lot Acceptance

Upon verifying the satisfactory completion of the performance requirements in the general and applicable detail parts procurement specifications by the part manufacturer, the prime contractor shall approve the procurement lot as accepted and qualified NSL parts and shall add the detail part procurement specification number to the Mandatory Parts List (MPL).

3.4 Part Procurement and Qualification (Phase III)

3.4.1 Part Procurement

The prime contractor shall negotiate the price and delivery of the procurement lot with the part manufacturer.

3.4.1.1 Procurement Lot

The procurement lot shall be adequate to provide the entire quantity of the specific NSL part required by all contractors throughout the program, for flight, testing, spares and contingency. The intent shall be to secure the reliability and cost effectiveness achievable with single (large) lot procurement and lot qualification.

3.4.2 Part Fabrication

The prime contractor shall monitor the part fabrication to the product requirements specified in the general procurement specification NSL-A401 and the applicable detail procurement specification NSL-A401/____.

3.4.3 Acceptance Test

The prime contractor shall monitor the acceptance test in accordance with the general procurement specification NSL-A401 and the applicable detail procurement specification NSL-A401/____.

3.4.4 Qualification Test

The prime contractor shall monitor the qualification test in accordance with the general procurement specification NSL-A401 and the applicable detail procurement specification NSL-A401/____.

4. REVOCATION AND REINSTATEMENT REQUIREMENTS

4.1 Loss of Part Manufactuer Qualification Status

Loss of the part manufacturer qualification status may result from the following:

a. Failure to comply with the quality survey requirements specified herein when producing, testing, stocking, and documenting parts to the applicable specifications.

b. Failure to maintain line certification for at least one manufacturing line.

4.2 Loss of Line Certification

Loss of line certification by the part manufacturer may result from the following:

a. Failure to produce transistors on the certified line(s) at least once annually.

b. Failure to comply with the Change Notification requirements of the NASA NSL-A401 general procurement specification.

c. Failure to maintain part qualification for one or more transistors from that line.

d. Changes in conditions, such as fire or relocation.

4.3 Loss of Part Qualification

Loss of part qualification by the part manufacturer may result from the following:

a. Violation of any conditions listed in sections 4.1 and 4.2.

b. Failure to comply with the Change Notification requirements of the NASA NSL-A401 general specification specification.

c. Failure to comply with the data and report-submission requirements.

d. Failure to maintain an acceptable delivery schedule.

e. Violation of the product-assurance provisions of the applicable specifications.

4.4 Reinstatement of Qualification Status of Part Manufacturer Line or Part Qualification

Part manufacturers who have lost qualification to supply transistors to the procurement specification may have qualification reinstated after all surveys, tests, studies, and measurements of the original qualification have been reviewed and, if necessary, repeated to the extent specified by the original qualifying activity.

5. DOCUMENTATION REQUIREMENTS

5.1 Part Manufacturer Eligibility Documentation

The documentation required in 3.2.1.3 herein and the completed Part Manufacturer Questionnaire (appendix A) shall be submitted by the part manufacturer to the prime contractor before the part manufacturer survey of 3.2.1 is initiated.

5.2 Line Certification Documentation

The line survey data required in 3.3.1.3 herein shall be submitted by the part manufacturer to the prime contractor before the part manufacturer survey of 3.2.1 is initiated.

5.3 Part Qualification Documentation

The Qualification Test Report required in 5.1.4 of the NASA general procurement specification NSL-A401 shall be submitted by the part manufacturer to the prime contractor after the completion of the qualification test.

6. SURVEY TEAM REQUIREMENTS

6.1 Composition of Survey Team

The survey team shall consist of NASA and its prime contractor personnel, who are experienced in company organization, modern manufacturing methods, and quality assurance procedures.

6.2 Survey Cost

The prime contractor shall stand the expense of the salaries, travel, and incidentals of the survey team; the part manufacturer shall stand the expense of receiving and conferring with the survey team at the transistor facility mutually agreed upon.

6.3 Line Certification Checklist

The survey team shall complete the Line Certification Checklist (appendix B) during the survey specified in 3.3.1 herein.

6.4 Survey Report

The survey team shall summarize its findings in a report and transmit a copy to the part manufacturer's management.

7. ABBREVIATIONS, SYMBOLS, AND DEFINITIONS

7.1 Abbreviations

7.1.1 CLL Certified Line List

7.1.2 MEL Manufacturer Eligibility List

7.1.3 MPL Mandatory Parts List

7.1.4 NSL NASA Special Long-Life

7.2 Symbols

Not applicable

7.3 Definitions

Not applicable

REVISION RECORD

REV	AUTHORITY	DESCRIPTION	RELEASE	
			DATE	APPROVAL

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APPENDIX A

PART MANUFACTURER QUESTIONNAIRE

1. HISTORY

1.1 Company _____

Division _____

Address _____

City and State _____

Phone _____

Person to Contact _____

1.2 Fabrication Activation Date for Transistors _____

1.3 Device Types to be Qualified _____

_____

_____

1.4 Fabrication Activation Date for Each Type _____

_____

_____

1.5 Total Number of Employees _____

Quality Assurance (QA) _____

Production _____

Engineering _____

1.6 Plant Area _____ Square Feet

1.7 Manufacturing Area _____ Square Feet

1.8 Types of Transistors Manufactured _____

_____

_____

_____

1.9 Government Service Inspection: Resident _____ Itinerant _____

1.10 Facilities Available for:

a. Continuous Production _____

b. Pilot Production _____

c. R & D, Limited Production _____

2. MANAGEMENT

2.1 Name and Title of Key Personnel _____

_____

_____

_____

2.2 Does Reliability have authority from management equal to that of Engineering and Production? Does this mean a direct responsibility for reliability of products in the line? _____

_____

_____

2.3 Does the QA Manager have direct authority for implementing quality policy and action in the line?

2.4 Is there a regular, summarized, quality reporting system to management? Does action correction in the line result?

3. QUALITY ASSURANCE (QA)

3.1 To whom does the QA Manager report?

3.2 Do commitments to corrective action by QA Management have staff influence or direct authority in the line? Which act prevails?

3.3 What is the QA/Reliability relationship?

3.4 What is the ratio of QA inspectors to direct production employees?

		Yes	No
3.5	Are procedures for identification and positive control of rejected or accepted material described?	___	___
3.6	Is there a system for:		
	a. In-process failure analysis?	___	___
	b. End-item failure?	___	___
	c. Reporting?	___	___
3.7	Are correction requests and replies documented at:		
	a. In-process Inspection?	___	___
	b. Final Inspection?	___	___
3.8	Are written inspection procedures located and used in the areas of:		
	a. Receiving Inspection?	___	___
	b. In-process Inspection?	___	___
	c. Batch Processing?	___	
	d. Final Test?	___	___
3.9	Does QA perform first piece or set-up inspection?	___	___
	Does QA audit this inspection during the run?	___	___
	Are calibrations or equipment maintained and current?	___	___
3.10	Does QA provide for review of purchasing documents to assure inclusion of pertinent quality data prior to release for procurement?	___	___
		___	___
3.11	Do current specification revisions show on flow records?	___	___

4. EQUIPMENT CALIBRATION

4.1	Is there an effective calibration record control system?	___	___
4.2	Are decals in use for physical equipment identification (to indicate that the units have been calibrated when the next calibration is due) and the calibrator's identification?	___	___
4.3	Are adjustments on calibrated equipment required to be sealed and tamper-proof?	___	___
4.4	Do the part manufacturer's procedures provide for the removal from service of any equipment that has not been maintained or calibrated in accordance with established schedules?	___	___

	Yes	No
4.5 Does the part manufacturer have current certification of equipment on file reflecting standards calibration (date, traceability to National Bureau of Standards (NBS), and calibrator)?		
a. Mechanical standards?	___	___
b. Electrical standards?	___	___
4.6 Is new specialized test equipment for acceptance purposes "proved" on products by QA before release for use?	___	___
5. DRAWING AND CHANGE CONTROL		
5.1 Does the part manufacturer's system provide for a documented change control which will guarantee that the required drawing is available at the point of manufacture and inspection?	___	___
5.2 Does the part manufacturer's drawing and change control system guarantee the removal of obsolete documentation from the manufacturing and inspection areas?	___	___
5.3 Does the QA review all drawings and changes thereto before they become effective?	___	___
5.4 Does the part manufacturer have a procedure to control temporary changes, deviations, or waivers?	___	___
6. RELIABILITY		
6.1 Are failures (types of causes or failures) in the line accumulated, analyzed, and reported to action addressees?	___	___
6.2 Are corrections as to parts or process changes resulting from failure analysis, coordinated with the customer, QA, or Reliability?	___	___
6.3 Does Reliability have the right of approval on test specifications, data tabulation, and part or process changes?	___	___
6.4 Is a failure analysis laboratory, or equivalent, available?	___	___
6.5 Does Reliability have access to all pertinent transistor development and production data for analysis?	___	___

	Yes	No
6.6 Is reliability data available on transistors from line or lines for which the part manufacturer will seek approval?	___	___
7. INCOMING INSPECTION		
7.1 Are materials received in a controlled area that would prevent removal prior to inspection?	___	___
7.2 Do supervisors review test reports received from vendors?		
7.3 Are accepted materials adequately identified? Is acceptance evidenced on documents?	___	___
7.4 Are rejected materials adequately identified and segregated?	___	___
7.5 Are the shelf life and cure dates of materials properly identified and controlled?	___	___
7.6 Do records indicate that units, lots, or split lots are traceable to applicable documents (specification, revision letter, and inspection record)?	___	___
7.7 Are materials stored in a controlled area under the charge of an authorized custodian?	___	___
7.8 Is the original quality acceptance identification maintained through the storage period?	___	___
7.9 Are physical and chemical tests performed on raw materials?	___	___
Are such tests performed in-house?	___	___
Are such tests performed out-of-house?	___	___
8. IN-PROCESS INSPECTION		
8.1 Are traveler documents used for the sequence and control of all operations and processes?	___	___
8.2 Do traveler documents reference inspection procedures?	___	___
8.3 Are first-piece or set-up inspections performed by QA?	___	___
Are there patrol inspections during the run?	___	___

		Yes	No
8.4	Is there a specified material review procedure?	___	___
8.5	Are Corrective Action Requests written?	___	___
8.6	Are rejects from manufacture analyzed and modes summarized and reported?	___	___
8.7	Are military sampling plans used?	___	___
9.	MANUFACTURING CONTROL		
9.1	Are traveler documents which show the sequence of processes available?	___	___
9.2	Are documents which describe in-process manufacturing controls and procedures available?	___	___
9.3	Are control charts for batch processes used and kept current?	___	___
9.4	Are standards for the handling, cleanliness, and care of materials, parts and equipment specified?	___	___
9.5	Does QA have authority to stop product flow when out-of-control conditions exist?	___	___
9.6	Are elemental parameter distributions, such as for base voltage, gain, and resistivity, recorded at key process steps?	___	___
10.	FINAL TEST		
10.1	Do Final Test personnel (QA) have written inspection and test procedures for product classes on the line?	___	___
10.2	Do procedures provide for material review and disposition of nonconforming devices?	___	___
10.3	Do inspectors use assigned stamps to indicate inspection status on parts and accompanying documents?	___	___
10.4	Are Corrective Action Requests written?	___	___
10.5	Are rejected devices identified and segregated in a controlled area?	___	___
10.6	Are device failure experiences analyzed?	___	___

		Yes	No
10.7	Is a testing laboratory, or equivalent, maintained by QA for:		
	a. Electrical tests?	___	___
	b. Mechanical tests?	___	___
	c. Chemical tests?	___	___
10.8	Are statistical controls on device parameter distributions maintained?	___	___
	Are they reported to QA or Reliability?	___	___
10.9	Is an environmental test facility maintained for:		
	a. Temperature (high, low, cycle)	___	___
	b. Shock (mechanical, thermal)	___	___
	c. Acceleration	___	___
	d. Vibration (fixed, variable)	___	___
	e. Moisture resistance	___	___
	f. Altitude	___	___
	g. X-ray	___	___
	h. Hermeticity		
	(1) Fine leak rate	___	___
	(2) Gross leak rate	___	___
	i. Lead fatigue	___	___
	j. Life (operating)	___	___
10.10	Is automatic equipment used for electrically testing transistors?	___	___
	Does it have variables reading capability?	___	___
	Does it have attributes reading (go, no-go) capability?	___	___
	Can it be used for dc and ac tests?	___	___

11. FACILITIES

11.1	Does thepart manufacturer have his own mask-making facility?	___	___
11.2	Are mask-making operations performed in an ultra-clean room?	___	___
11.3	Are photoengraving (photoresist exposure operations performed in an ultra-clean room?	___	___

If answers to 11.1 or 11.2 above are "yes", what are the clean room specifications? _____

_____

11.4	Are particle counts taken and recorded regularly?	___	___

		Yes	No
11.5	Are clean room disciplines and procedures as to clothing, access, eating, materials allowed, cosmetics, etc. described?	___	___
11.6	Are unfinished and finished products of the area suitably protected to maintain their level of cleanliness?	___	___
11.7	Does QA audit compliance with procedures and standards?	___	___

12. SHIPPING

12.1	Does the part manufacturer have written procedures that control the transistors?	___	___
12.2	Are materials designated for shipment properly identified, handled, and protected?	___	___
12.3	Do copies of customer purchase orders and evidence of inspection acceptance accompany material to shipping (from Final Test)?	___	___
12.4	Do shipping documents reflect inspection status or evidence of inspection, identification, and similar shipping requirements?	___	___

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APPENDIX B

LINE CERTIFICATION CHECKLIST

1. HISTORY

1.1 Company _____

Division _____

Address _____

City and State _____

Phone _____

Person to Contact _____

1.2 Activation Date for Fabrication of Line. _____

_____

1.3 Device Types Fabricated on Line _____

_____

_____

1.4 Activation Date for Fabrication of Each Transistor Type _____

_____

_____

_____

2. FABRICATION METHODS AND MATERIALS

2.1 What traceability techniques are used? _____

_____

_____

2.2 Wafer Preparation

2.2.1 Which of the following tests are performed on the wafer?

	Yes	No
a. Thickness	___	___
b. Flatness	___	___
c. Parallelism	___	___
d. Surface roughness	___	___
e. Crystal perfection	___	___
f. Surface orientation	___	___
g. Lifetime	___	___
h. Oxygen content	___	___
i. Conductivity	___	___
j. Resistivity	___	___

2.3 Surface Passivation

2.3.1 What types of layers are formed? _____

_____

2.3.2 What methods are used? _____

_____

2.3.3 What is the purpose of each layer? _____

_____

2.3.4 What is the thickness of each layer? _____

_____

2.3.5 How often is each furnace profiled? _____

_____

2.3.6 How often is the profiling equipment calibrated? _____

_____

2.3.7 How often is the profile monitored? _____

_____

2.4 Photolithography

2.4.1 What type of photoresist is used? _____

_____

2.4.2 What is method of mounting the wafer? _____

_____

2.4.3 What is temperature of photoresist during application? _____

_____

2.4.4 What are the time and speed of rotation? _____

_____

2.4.5 What are the time and temperature of drying for the photoresist?_____

_____

2.4.6 What is the viscosity range of the photoresist? _____

_____

2.5 Junction Formation

2.5.1 How often is the diffusion tube profiled? _____

_____

2.5.2 How often is the temperature of the diffusion tube checked?

_____

_____

2.5.3 How often is the temperature of the epitaxial furnace checked?

_____

_____

2.5.4 Are the sheet resistivity and junction depth measured on an epitaxial layer? _____

_____

2.5.5 Are emitter and base junction depths measured on a diffused transistor?_____

_____

2.6 Metallization

2.6.1 What metallization system is used? _____

_____

2.6.2 What are the temperatures of the substrate and vacuum? What is the heat relationship on the metal to be deposited?

2.6.3 How is the metal thickness monitored? _____

2.6.4 What are the temperature, time, and environmental conditions during alloying? _____

2.6.5 What are the temperature, time, and concentration of etching?

2.6.6 How is the etchant removed? _____

2.6.7 Is back-surface metallization used? What is the method? _____

2.7 Die Mounting

2.7.1 What is the type of die? _____

2.7.2 What bonding agent is used? _____

_____

2.7.3 What package mount material is used? _____

_____

2.7.4 What is the design of the package mount? _____

_____

2.7.5 What forming gas is required? _____

_____

2.7.6 What is the work stage temperature, if applicable? _____

_____

2.8 Wire Bonding

2.8.1 What kind (physical) of lead is used? _____

_____

2.8.2 What size is the wire? _____

_____

2.8.3 What wire material is used? _____

_____

2.8.4 What bonding technique is used? _____

_____

2.8.5 What is the work stage temperature, if applicable? _____

_____

2.9 Sealing

2.9.1 What type of seal is used? _____

_____

2.9.2 What sealing technique is used? _____

_____

2.9.3 What is the atmosphere during sealing? _____

_____

2.10 Scribing

2.10.1 What is the method of scribing? _____

_____

2.10.2 What is the method of weakening? _____

_____

2.10.3 What is the effect of scribing on traceability? _____

_____

2.11 Cleaning

2.11.1 What is the method of cleaning? _____

_____

2.11.2 When is cleaning performed? _____

_____

2.11.3 What cleaning solutions are used? _____

_____ _____

2.11.4 How often are solutions changed? _____

_____

EXAMPLE

NSL-C401/1

DETAIL PART AND MANUFACTURER SELECTION AND CONTROL SPECIFICATION FOR

NASA SPECIAL LONG-LIFE (NSL TRANSISTOR, TYPE NSL-401/1)

FEBRUARY 1969

(THIS SPECIFICATION IS NOT APPLICABLE

TO TRANSISTOR NSL-401/1)

EXAMPLE

NSL-D401

GENERAL PART INSPECTION, HANDLING, AND STORAGE SPECIFICATION FOR

N . SPECIAL LONG-LIFE (NSL) TRANSISTORS

FEBRUARY 1969

CONTENTS

NSL-D401

GENERAL PART INSPECTION; HANDLING, AND STORAGE SPECIFICATION FOR NASA SPECIAL LONG-LIFE (NSL) TRANSISTORS

1. SCOPE

1.1 Applicability

This specification is part of the system of Part Control Packages for controlling NASA Special Long-Life (NSL) parts, described in NASA CR-66742-1. This specification is general section D of Part Control Package NSL-401, and defines the general part inspection, handling, and storage requirements for all NSL transistors. This specification and the applicable detail part inspection, handling, and storage specification, NSL-D401/____, are mandatory whenever NSL transistors are specified.

2. APPLICABLE DOCUMENTS

2.1 Documents

The following documents form a part of this specification to the extent specified herein. Unless otherwise specified herein, the issue in effect on the date of the part procurement contract shall apply.

STANDARDS

Military

MIL-STD-750	Test Methods for Semiconductor Devices

SPECIFICATIONS

Military

MIL-S-19500	Semiconductor Devices, General Specification for

NASA

NSL-D401/____	Detail Part Inspection, Handling, and Storage Specification for NASA Special Long-Life (NSL) Transistors

2.2 Conflicting Requirements

In the event of conflict between the requirements of this specification and any of the documents specified herein or in the applicable detail part inspection, handling, and storage specification, the order of precedence shall be as follows:

a. The applicable NASA Special Long-Life (NSL) detail part inspection, handling, and storage specification.

b. This general part inspection, handling, and storage specification.

c. Specification referenced herein or in the applicable detail part inspection, handling, and storage specification.

3. REQUIREMENTS

3.1 General

The procuring facility shall inspect, handle, and store all transistors in accordance with this specification, the applicable detail specification and the prime contractor's Parts Program Plan.

3.2 Storage and Handling

3.2.1 General

Improper handling and storage of parts can have a deleterious effect on the reliability and performance of the fabricated equipment. Therefore, the following requirements are established to cover the handling and storage of parts during the interval from their receipt until the parts lose their individual identity on assembly into modules, boards, or other equipment increments.

The general requirements to be used in the establishement of the handling and storage system shall be as follows:

a. Control of environment, such as temperature, humidity, contamination and pressure.

b. Procedure and facilities to segregate parts.

c. Housekeeping practices, including provisions for the routine disposal of used packaging materials.

d. Control measures to limit personnel access to parts being subjected to the receiving inspection cycle and parts that are placed in project stores.

e. Facilities for the interim storage of parts, such as adequate space and shelving, including protective cushioning material on the shelves.

f. Use of an integrated system of containers to separate and protect individual parts.

g. Grounding of all equipment prior to insertion of the part for electrical test.

h. Where applicable, keeping parts in metal shields until they are inserted in the equipment or removed for test.

i. Where applicable, keeping parts in carriers or other protective packages during test.

j. Enclosure of parts in individual packages at the earliest possible time after receiving inspection is completed.

k. Storage of metal oxide field effect parts with all leads shorted.

l. Minimizing mechanical shock or vibration as parts are transported from place to place.

m. Careful placement of packages or parts on shelves or benches (at no time shall they be thrown or dropped on a hard surface).

n. Use of transportation equipment that prevents packages from being accidentally dropped or dislodged in transit.

o. Providing bench surfaces on which materials are handled during operations such as test, assembly and inspection, with adequate cushioning and sills to prevent damage to parts from inadvertent rough handling.

p. Electrically grounding all accessible metal surfaces in work area.

q. Use of grounded wrist straps by all personnel when handling metal-oxide-silicon field effect parts.

r. Treating smocks worn by personnel during any phase of the process of inspection, assembly, or test, with an anti-static compound.

s. Precautions in storing or testing parts in substantial fields of X-rays, neutrons, or other energy particles.

t. Re-examination and retest as specified in the applicable detail specification, NSL-D401/____, at receiving inspection on a 100 percent inspection level, of all parts that are mishandled.

3.2.2 Procedures and Inspections

Procedures and instructions for the implementation of the handling and storage system shall cover at least the following:

a. Inspection requirements for packaging in accordance with the procurement specifications, including package-handling marking.

b. Precautionary measures necessary when handling sensitive or critical parts, including unpackaging techniques.

c. Identification and marking instructions for parts and individual containers to assure continued identity of part.

d. Instructions for preparing items for protective packaging to prevent handling and corrosion damage while in interim storage, awaiting other operations, or transport to shipping.

e. Procedure to establish a periodic inspection of the stores operations by the quality control group, including visual inspection of parts for determining acceptability of the parts condition.

3.3 Inspection Requirements

3.3.1 Pre-test Requirement

Receiving inspection shall assure that the parts are on the NASA Program's Mandatory Parts List (MPL). They shall also assure that parts have been inspected by the part manufacturer in accordance with the applicable procurement specifications and the required documentation has been submitted.

3.3.2 Material and Data

Receiving inspection shall assure that inspection and test equipment, specifications and instructions will be available to perform necessary test and examinations on receipt of the parts being purchased.

3.3.3 External Physical Characteristics

Receiving inspection shall perform external visual inspection as specified in the applicable detail specification.

3.3.4 Construction Analysis

Receiving inspection shall perform a construction analysis inspection as specified in the applicable detail specification.

3.3.5 Electrical Tests

Receiving inspection shall perform electrical tests as specified in the applicable detail specification.

3.3.6 Inspection, Measuring, and Test Equipment

3.3.6.1 Equipment Requirements

The user shall provide for the selection, evaluation, approval, maintenance, and control of all inspection standards, gages, measuring, and test equipment necessary to determine conformance with specifications and drawings. The requirements of this specification include production tools and equipment incorporating an inspection, measurement, or test function. All equipment shall be used in an environment and in a manner to ensure continued measurements of the required accuracy.

3.3.6.2 Calibration

The calibration of measuring and testing equipment shall be in accordance with MIL-STD-750.

3.3.7 Part Failure

Failure of any NSL transistors for any cause whatsoever shall be reported to the NASA prime contractor on the NSL Part Failure Report, appendix A herein.

3.3.8 Material Review Board

All discrepant parts and the effected lots shall be reviewed for disposition by the Material Review Board. All catastrophic failures shall have a failure analysis performed before disposition of the parts.

3.3.9 Part Separation

Receiving inspection shall assure that physical separation of the purchase parts shall be maintained. This shall provide, as a minimum, separation of:

a. Parts awaiting inspection or test results,

b. Conforming parts, and

c. Rejected parts.

The integrity of lots awaiting inspection and test results shall be maintained.

3.3.10 Inspection Records

Records shall be maintained attesting the parts' conformance to the requirements herein.

3.3.11 Inspection Stamps

3.3.11.1 Stamp Requirements

The user shall establish and maintain an inspection stamp control system which includes, but is not limited to, the following:

a. Stamps, decals, or seals shall be designed to identify parts that have undergone inspection or test. Parts which have been rejected need not be stamped, but the reject or withhold stamp shall be applied to the hold tag or other documentation, as appropriate.

b. Each stamp shall be traceable to the individual responsible for its use, and records shall be maintained to identify individuals with specific inspection stamps.

c. Stamps indicating that inspections have been performed shall be applied only to documentation.

d. Stamps shall be applied to tags, cards, or labels attached to individual parts as practical.

e. Stamp design shall not resemble Government inspection stamps.

3.4 Project Stores

A project stores area shall be selected and designated as a storage area for parts which have completed the receiving inspection cycle but which have not as yet been issued to the manufacturing activity. The following minimum requirements are established covering the treatment of parts during this interval.

a. Flight and non-flight parts shall be stored in separate areas within Project Stores and marked accordingly.

b. A Release Order (appendix B herein) is required for withdrawal of flight parts and shall be signed by Project Product Effectiveness management.

c. Only authorized personnel designated by Project Effectiveness management may withdraw parts from Project Stores.

d. Project Stores shall prepare kits from flight stock as requested on a Kit Requisition form, appendix C herein. During kit assembly, Quality Control enters the part number, serial number, and receiving lot number of the parts issued.

e. When a kit requisition is not involved, Project Stores shall issue parts:

(1) To complete a unit requiring selected part (completion of kit requirements).

(2) To replace a damaged or failed part, a Part Replacement Requisition (PRR), appendix D herein, shall be used only for "flight" parts.

f. Parts forwarded from Receiving Inspection for special testing shall be returned to Receiving Inspection after test for transfer to Project Stores. A Request for Inspection/Test form, appendix E herein, shall accompany the parts and shall be retained with the test data history.

g. There shall be limited personnel access to the Project Stores area.

3.5 Fabrication Controls

3.5.1 Fabrication Instructions

The manufacturing activity shall provide detailed work instructions to the product personnel for proper handling and installation of parts. These instructions shall reflect the assembly elements, the work stations, and the skill levels of persons involved.

3.5.2 Material Control

Articles undergoing fabrication shall be identified on records traceable to the individual parts.

3.5.3 Quality Control

Provisions shall be made for the establishment of Quality Control stations and procedures in the production and assembly areas.

3.5.3.1 Control of Cleanliness of Fabrication Area

Parts shall be handled, assembled, and processed under controlled cleanliness conditions. Special procedures to maintain such cleanliness shall be included or referenced on applicable process documents.

3.5.3.2 Process Control

The user shall maintain a defect-prevention program for the control of bonding, welding, and other processes where uniform high quality cannot be assured by inspection solely by examination of completed assemblies and subassemblies.

3.5.3.3 Process Control Procedures

Process control procedures shall supplement applicable process specifications to provide detailed methods. These procedures shall document the preparation and fabrication conditions to be maintained during each phase of the process.

3.5.3.4 Process Environments

Where processes must be conducted in special environment, such as under vacuum or inert gases, the process controls shall include means of maintaining the required environments and means of indicating or measuring the environments maintained.

3.5.3.5 Process Certification

The user shall provide for the certification of machine, equipment, and procedures used in process operations.

3.5.3.6 Personnel Certification

The user shall establish a system for personnel certification covering assembly, welding, soldering, and other processes requiring special skills.

3.5.4 Joining Techniques

Work instructions and process standards shall be developed and used which cover soldering and welding techniques. Part lead materials and finishes shall be consistent with the joining processes.

3.5.5 Containers and Kits

a. The user shall have a system of collecting, storing, and issuing kits of parts needed for fabrication. In addition to facilitating the assembly process, these kits are also intended to provide physical and environmental protection of their contents.

b. Individual containers should nest in larger trays or tote boxes that accommodate an entire kit or parts for one assembly in an orderly arrangement and provide mechanical security. If possible, the parts should be arranged for withdrawal in the order in which they are placed in the assembly.

c. The tray, containing a complete kit of parts for one assembly, should be delivered to the work station. As the assembly is completed, the individual containers should be returned to stores for re-use and the tray should become the container for the completed assembly. The completed assembly should be transported in the tray to the stockroom for storage until required in the next higher assembly.

d. Parts shall be protected from contact by bare hands; gloved fingers, tweezers, etc., shall be used.

e. Parts supplied to the assembler should preferably be ready for assembly without further preparation. Lead cutting is permissible if proper tools and instructions are supplied. Shear-type cutting tools (not pinch type) shall be used. Bending moments shall not be transmitted to the body of a part.

3.6 Traceability

A traceability system shall be established that obtains, retains, and assigns codes in such a manner that each NSL part can be traced from its receipt through its subassembly level.

4. ABBREVIATIONS, SYMBOLS, AND DEFINITIONS

None

REVISION RECORD

REV	AUTHORITY	DESCRIPTION	RELEASE	
			DATE	APPROVAL

APPENDIX A

PART FAILURE REPORT FORM

NSL PART FAILURE REPORT NO. _____

PART NAME _____ MANUFACTURER _____

NSL PART NO. _____ PURCHASE ORDER NO. _____

FAILURE FIRST OBSERVED _____
(Rec. Insp., Subassembly Test, Final Test, etc.)

DETAILS OF FAILURE (BE SPECIFIC)

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APPENDIX B

RELEASE ORDER FORM

CREDIT ACCOUNT (FROM)	CHARGE (TO)										CONTROL NUMBER
	G. L. A.	CONT ERP	ACCOUNT DETAIL MAJ	MIN	OPER	WORK ORDER NO.	SOURCE CODE ACTY	DEPT	SEC	LOT OR E.C.A. NO.	SERIAL

DATE REQUESTED	DATE DUE	PROC CODE	USE CODE	B/M CODE	PART, NEXT ASSEMBLY, PROJECT OR TEST EQUIPMENT NUMBER BASIC	PART, NEXT ASSEMBLY, PROJECT OR TEST EQUIPMENT NUMBER DASH	TOOL SERIAL OR CODE BASIC	TOOL SERIAL OR CODE DASH

QUANTITY REQUESTED (WHOLE)	QUANTITY REQUESTED (DEC)	QUANTITY ISSUED (WHOLE)	QUANTITY ISSUED (DEC)	UNIT	CATALOG OR PART NUMBER	DESCRIPTION	UNIT PRICE $	UNIT PRICE ¢	UNIT	TOTAL COST $	TOTAL COST ¢
									TOTAL		

REASON FOR REQUEST:

STORES ISSUE STAMP

REQUESTED BY	DEPT.	DELIVER TO:			DEPT.
		BLDG.	RM. OR ST.	EXT.	CONT. CENTER
APPROVED BY	DEPT.				
MATERIAL CONTROL	GOVT. PROP. CONTROL			RECEIVED BY	DEPT.

RELEASE ORDER

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Sheet 15

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APPENDIX C

KIT REQUISITION FORM

KIT REQUISITION

PART NO. _____ S/N _____ KIT NO. _____

PROGRAM _____

INSP	DATE	PART NO.	DESCRIPTION	QTY REQ'D	QTY ISSUED	LOT #	SERIAL #	BACK ORDER REQ. NO.

DWG. REV. _____ CHG # _____

E.O.'S _____ _____ _____

APPROVAL _____

SHEET ___ OF ___.

APPENDIX D

PART REPLACEMENT REQUISITION FORM

CREDIT ACCOUNT (FROM)	CHARGE (TO)										CONTROL NUMBER
	G. L. A.	CONT EXP	ACCOUNT DETAIL MAJ	MIN	OPER	WORK ORDER NO.	SOURCE CODE ACCT	DEPT	SEC	LOT OR E.C.A. NO.	SERIAL

DATE REQUESTED	DATE DUE	PROC CODE	USE CODE	B/M CODE	PART, NEXT ASSEMBLY, PROJECT OR TEST EQUIPMENT NUMBER BASIC	DASH	TOOL SERIAL OR CODE BASIC	CASH

QUANTITY REQUESTED (WHOLE)	QUANTITY REQUESTED (DEC)	QUANTITY ISSUED (WHOLE)	QUANTITY ISSUED (DEC)	UNIT	CATALOG OR PART NUMBER	DESCRIPTION	UNIT PRICE $	UNIT PRICE ¢	UNIT	TOTAL COST $	TOTAL COST ¢

REASON FOR REQUEST:

TOTAL

REQUESTED BY ____ DEPT. ____

APPROVED BY ____ DEPT. ____

MATERIAL CONTROL	GOVT. PROP. CONTROL		

DELIVER TO: ____ DEPT. ____

BLDG.	RM. OR ST.	EXT.	CONT. CENTER

RECEIVED BY ____ DEPT. ____

STORES ISSUE STAMP

PART REPLACEMENT REQUISITION

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Sheet 19

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APPENDIX E

REQUEST FOR INSPECTION/TEST FORM

REQUEST FOR INSPECTION/TEST

DATE OF REQUEST: _____

To: _____ Dept. # _____
(Insp./Test, Lab., Dept., etc.)
Bldg. _____

From: _____ Dept. # _____
Bldg.: _____
By: _____

(For Use by originator of this Request)
Total Lot Quantity Received: _____
Vendor: _____
Form and Date Held By Originator Pending Return of Insp./Test Reports: _____

Inspect or Test Following Material to Applicable Drawing and/or Specification:

Part Name or Type Material

Drawing No.: _____

Specification No.: _____

(Cat. and Stock No.: _____

(Alloy _____ HEAT # _____

Quantity to be Inspected/Tested: _____

R.R.-R.M., Special Data or Instructions:

_____ Purchase Order/R.R. No. _____
Receiving Memorandum No. _____
Work Order No. _____

Action On Material Inspected/Tested:

_____ R.I.T.R. Initiated _____ No. _____
Insp./Test Entries Posted to Forms
_____ Held By Originator of Request.
_____ Material to be Re-Inspected/Tested.

REQUIRED INSPECTION OR TEST	QUANTITY Accepted	QUANTITY Rejected	SIGNATURE OF INSP. OR TESTER	COMMENTS—SPECIFY REASONS FOR NON-ACCEPTANCE
(1)				
(2)				
(3)				
(4)				
(5)				
(6)				
(7)				
(8)				

Quantity Inspected/Tested _____ Date Insp./Test Completed: _____

Sig. of Accepting Insp./Tested _____ Customer: _____

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Sheet 21

EXAMPLE

NSL-D401/1

DETAIL PART INSPECTION, HANDLING, AND STORAGE SPECIFICATION FOR

NASA SPECIAL LONG-LIFE (NSL) TRANSISTOR, TYPE NSL-401/1

FEBRUARY 1969

CONTENTS

NSL-D401/1

DETAIL PART INSPECTION, HANDLING, AND STORAGE SPECIFICATION FOR NASA SPECIAL LONG-LIFE (NSL) TRANSISTOR, TYPE NSL-401/1

1. SCOPE

1.1 Applicability

This specification is part of the system of Part Control Packages for controlling NASA Special Long-Life (NSL) parts, described in NASA CR-66742-1. This specification is detail section D of Part Control Package NSL-401, and defines the detail part inspection, handling, and storage requirements for transistors, type NSL-401/1.

2. APPLICABLE DOCUMENTS

2.1 Documents

The following documents form a part of this specification to the extent specified herein. Unless otherwise specified herein, the issue in effect on the date of the part procurement contract shall apply.

SPECIFICATIONS

NASA

NSL-D401	General Part Inspection, Handling, and Storage Specification for NASA Special Long-Life (NSL) Transistors

(The documents listed in 2.1 of NSL-D401 form a part of this document to the extent specified herein and within the limitations of 2.2 of NSL-D401.)

2.2 Conflicting Requirements

The requirements of 2.2 of NSL-D401 apply.

3. REQUIREMENTS

3.1 General

The requirements of 3.1 of NSL-D401 apply.

3.2 Storage and Handling

The requirements of 3.2 of NSL-D401 apply.

3.3 Inspection Requirements

3.3.1 Pre-test Requirements

The contractor shall verify that the inspection requirements of 3.3.1 of NSL-D401 and as specified below are met.

3.3.1.1 Source Verification

The part manufacturer shall be:

National Semiconductor Corp.
P. O. Box 443
Danbury, Connecticut 06813
Code Identification Number: 01295

Shipments received from other sources, including distributors, jobbers, other part manufacturers, or facilities different than that specified above, shall be rejected.

3.3.1.2 Data Package

All documentation shall be contained on 8-1/2 by 11 inch sheets or standard electronic accounting machine printout forms. The following items shall be included in the data package:

a. Certificate of Compliance

b. Fabrication Record Report

c. Acceptance Test Report

d. Qualification Test Report

3.3.3 External Physical Characteristics

The external physical characteristics of the transistor shall be as shown in figures 1 and 2 herein.

3.3.4 Internal Construction Analysis

Construction and materials shall be in accordance with figures 2 and 3 herein.

3.3.5 Electrical Characteristics

The electrical characteristics of the transistor shall be as specified in table I herein.

3.3.6 Acceptance Test

The acceptance test requirements shall be as specified in tables II, III, and IV herein.

3.4 Project Stores

The requirements of 3.4 of NSL-D401 apply.

3.5 Fabrication Controls

The requirements of 3.5 of NSL-D401 apply.

3.6 Traceability

The requirements of 3.6 of NSL-D401 apply.

4. ABBREVIATIONS, SYMBOLS, AND DEFINITIONS

The abbreviations, symbols, and definitions are defined in MIL-S-19500.

TABLE I.- ELECTRICAL REQUIREMENTS

Test	Test Method MIL-STD-750	Conditions	Limits at Temperature			Units
			T_A = -55° C	T_A = +25° C	T_A = +150° C	
Subgroup 1						
BV_{CEO}	3011 cond D	I_C = 10 mA 1/ I_B = 0		60 min		V
BV_{CBO}	3001 cond D	I_C = 10 µA I_E = 0		60 min		V
BV_{EBO}	3026 cond D	I_E = 10 µA I_C = 0		6.0 min		V
I_{CBO}	3036 cond D	V_{CB} = 45 V I_E = 0		10 max		
I_{CES}	3041 cond C	V_{CE} = 5 V V_{BE} = 0		5 max	10 max	nA
I_{CEO}	3041 cond D	V_{CE} = 5 V I_B = 0		2 max		nA
I_{EBO}	3061 cond D	V_{EB} = 6 V I_C = 0		2 max		nA
Subgroup 2						
h_{FE_1}	3076	V_{CE} = 5 V I_C = 1 µA		30 min		--
h_{FE_2}	3076	V_{CE} = 5 V I_C = 10 µA		200 min 500 max	35 min	--
h_{FE_3}	3076	V_{CE} = 5 V I_C = 100 µA		225 min		--
h_{FE_4}	3076	V_{CE} = 5 V I_C = 500 µA		250 min		--

1/ Pulsed: Pulse width ≤ 300 µsec, duty cycle ≤ 2%.

TABLE I.- ELECTRICAL REQUIREMENTS - Continued

Test	Test Method MIL-STD-750	Conditions	Limits at Temperature			Units
			T_A = -55° C	T_A = +25° C	T_A = +150° C	
Subgroup 2 (Continued)						
h_{FE_5}	3076	V_{CE} = 5 V I_C = 1 mA		250 min		--
h_{FE_6}	3076	V_{CE} = 5 V I_C = 10 mA 1/		800 min		--
$V_{CE(sat)}$	3071	I_C = 1.0 mA I_B = 0.1 mA		0.3 max		V
V_{BE}	3066 cond B	V_{CE} = 5 V I_C = 100 µA		0.5 min 0.7 max		V
Subgroup 3						
h_{oe}	3216	V_{CE} = 5 V I_C = 1.0 mA		0 min 40 max		µmho
h_{re}	3211	V_{CE} = 5 V I_C = 1.0 mA		0 min 8.0×10^{-4} max		
h_{ie}	3201	V_{CE} = 5 V I_C = 1 mA		3.5 K min 24 K max		-- ohm
h_{fe}	3206	V_{CE} = 5 V I_C = +1 mA f = 1 kHz		250 min 900 max		--
Subgroup 4						
$\|h_{fe}\|$	3306	V_{CE} = 5 V I_C = 500 µA f = 30 MHz		20 min 70 max		--
C_{obo}	3236	V_{CB} = 5 V I_E = 0 100 kHz≤f≤1 MHz		5.0 max		pf

TABLE I.- ELECTRICAL REQUIREMENTS - Continued

Test	Test Method MIL-STD-750	Conditions	Limits at Temperature			Units
			T_A = -55° C	T_A = +25° C	T_A = +150° C	
Subgroup 4 (Continued)						
C_{ibo}	3240	V_{EB} = 0.5 V I_C = 0 100 kHz≤f≤1 MHz		6.0 max		pf
NF_1	3246	f = 100 Hz V_{CE} = 5 V I_C = 10 μA R_g = 10 kilohms		7.5 max		db
NF_2	3246	f = 1 kHz V_{CE} = 5.0 V I_C = 10 μA R_g = 10 kilohms		3 max		db
NF_3	3246	f = 10 kHz V_{CE} = 5 V I_C = 10 μA R_g = 10 kilohms		2 max		db
NF_4	3246	V_{CE} = 5 V I_C = 10 μA R_g = 10 kilohms Power bandwidth of 15.7 kHz with 3 db points at 10 Hz and 10 kHz		3 max		db

TABLE II.- ACCEPTANCE REQUIREMENTS

Examination or Test	Reference	Sample Size	Max Allow Defects
External Physical Characteristics	MIL-STD-750, method 2066, and figures 1 and 2 herein	Table III	0
Electrical Characteristics			
Subgroup I	Table I herein	Table III	0
Subgroup II	Table I herein	Table III	0
Subgroup III	Table I herein	Table III	0
Subgroup IV	Table I herein	Table III	0
Internal Construction Analysis	MIL-STD-750, method 2071, and figures 2 and 3 herein	Table IV	1/

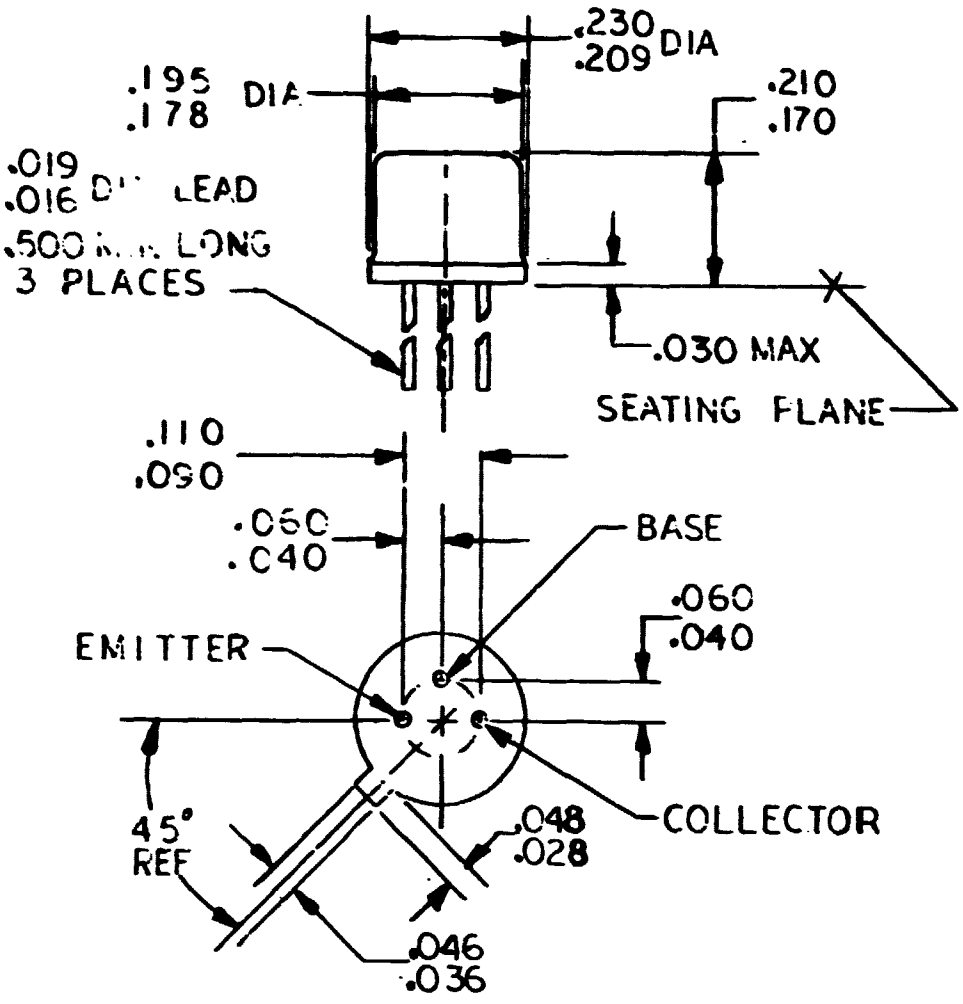
1/ Any deviation from the specified configuration shall be cause for rejection of the lot.

TABLE III.- SAMPLING TABLE FOR EXTERNAL PHYSICAL CHARACTERISTICS AND ELECTRICAL CHARACTERISTICS

Lot Size	Sample Size	Lot Size	Sample Size
2-15	2	1,201-3,200	50
16-25	3	3,201-10,000	80
26-90	5	10,001-35,000	125
91-150	8	35,001-150,000	200
151-280	13	150,001-500,000	315
281-500	20	500,001 and over	500
501-1,200	32		

TABLE IV.- SAMPLING TABLE FOR INTERNAL CONSTRUCTION ANALYSIS

Lot Size	Sample Size
1-99	0
100-999	2
1,000 and over	4



NOTE:

1. JEDEC TO-18 PACKAGE

FIGURE 1. EXTERNAL PHYSICAL CHARACTERISTICS

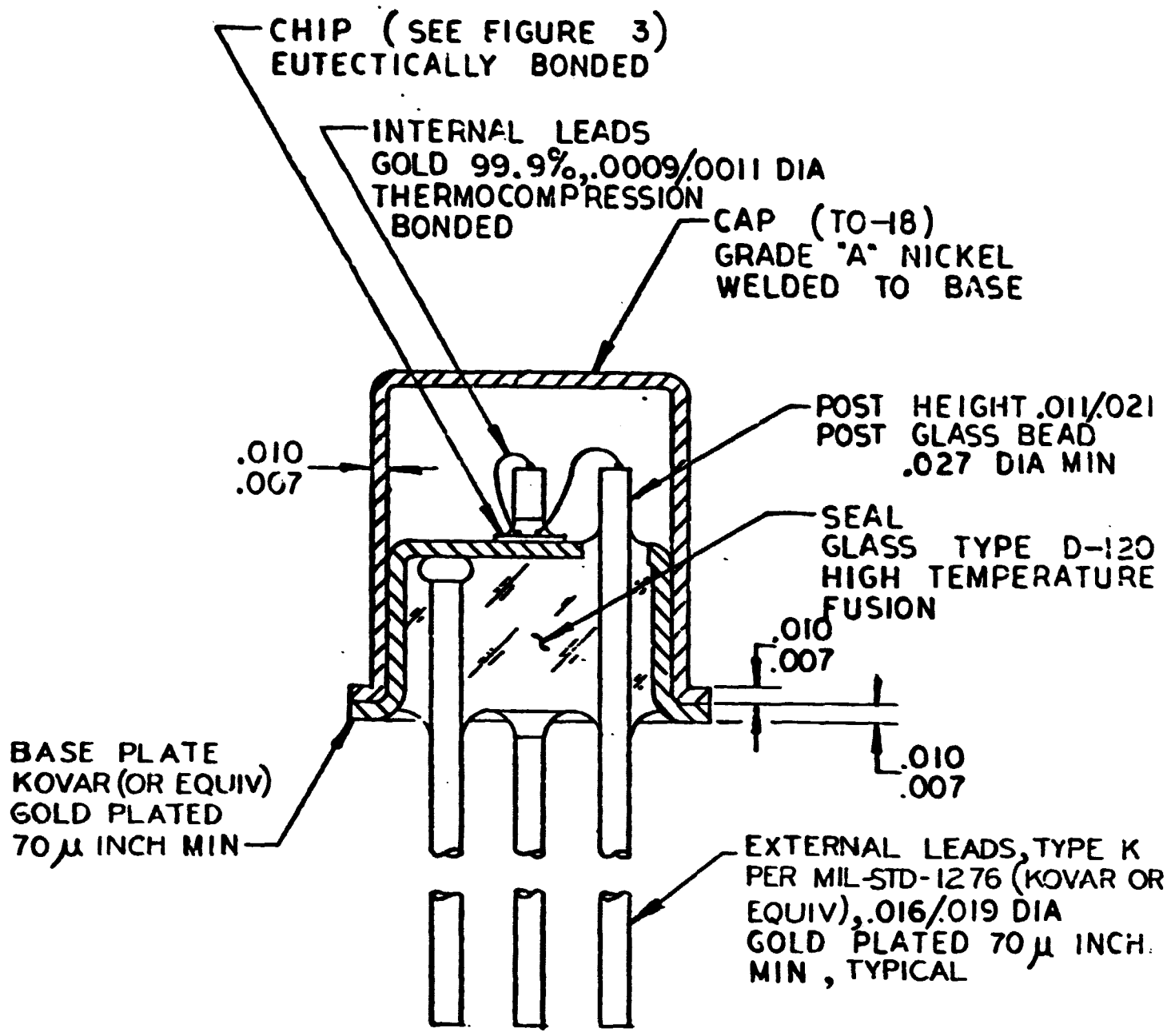
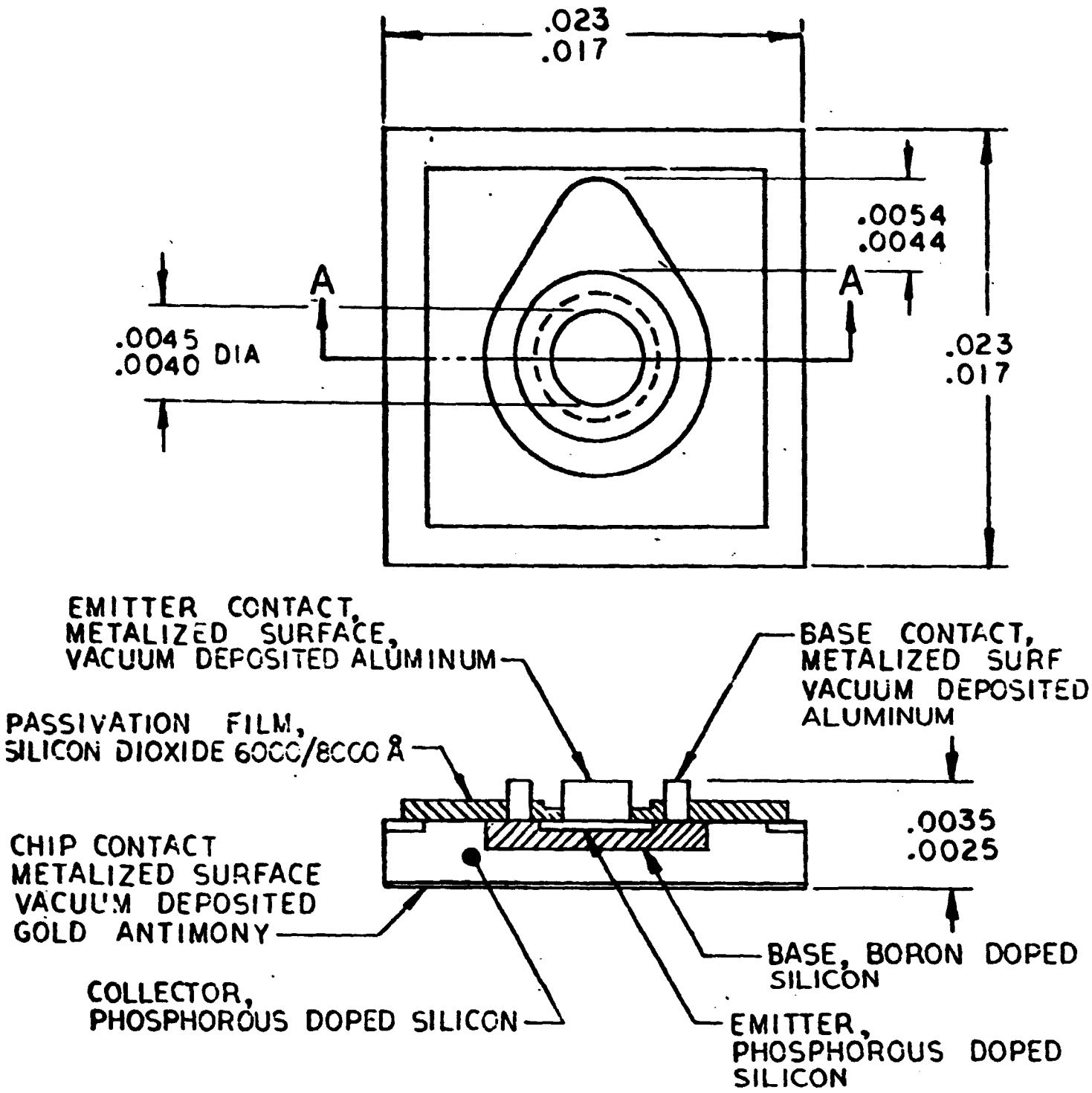


FIGURE 2. CROSS-SECTIONAL CHARACTERISTICS.



NOTE:

1. SEMICONDUCTOR PROCESS: PLANAR

FIGURE 3. CHARACTERISTICS OF SILICON CHIP

REVISION RECORD

REV	AUTHORITY	DESCRIPTION	RELEASE	
			DATE	APPROVAL

EXAMPLE

NSL-E401

GENERAL SUPPORTING DATA SPECIFICATION FOR

NASA SPECIAL LONG-LIFE (NSL) TRANSISTORS

FEBRUARY 1969

CONTENTS

NSL-E401

GENERAL SUPPORTING DATA SPECIFICATION FOR NASA SPECIAL LONG-LIFE (NSL) TRANSISTORS

1. SCOPE

1.1 Applicability

This specification is part of the system of Part Control Packages for controlling NASA Special Long-Life (NSL) parts, described in NASA CR-66742-1. This specification is general section E of Part Control Package NSL-401, and defines the general supporting data requirements for NSL transistors. This specification and the applicable detail supporting data specification, NSL-E401/____, are mandatory whenever NSL transistors are specified.

2. APPLICABLE DOCUMENTS

2.1 Documents

The following documents form a part of this specification to the extent specified herein. Unless otherwise specified herein, the issue in effect on the date of the part procurement contract shall apply.

SPECIFICATIONS

NASA

NSL-A401	General Procurement Specification for NASA Special Long-Life (NSL) Transistors
NSL-A401/____	Detail Procurement Specification for NASA Special Long-Life (NSL) Transistor, Type NSL-401/____
NSL-C401	General Part and Manufacturer Selection and Control Specification for NASA Special Long-Life (NSL) Transistors
NSL-E401/____	Detail Supporting Data Specification for NASA Special Long-Life (NSL) Transistor, Type NSL-401/____

2.2 Conflicting Requirements

In the event of conflict between the requirements of this specification and any of the documents specified herein or in the applicable detail supporting data specification, the order of precedence shall be as follows:

a. The applicable NASA Special Long-Life (NSL) detail supporting data specification.

b. This general supporting data specification.

c. Specifications referenced herein or in the applicable detail supporting data specification.

3. DATA REQUIREMENTS

3.1 General

A summary of supporting data shall be required by the prime contractor in five categories:

a. Part manufacturer survey documentation

b. Line certification survey documentation

c. Part qualification test data

d. Lot acceptance test data

e. Part history.

Data collected shall be summarized by the prime contractor for inclusion in this specification and the applicable detail supporting data specification updated as available.

3.2 Part Manufacturer Survey Documentation

The Part Manufacturer Questionnaire and the survey team report as required by NSL-C401 shall be included; also all supporting data for the survey shall be included in the part manufacturer survey documentation.

3.3 Line Certification Survey Documentation

The Line Certification Checklist and the survey team report as required by NSL-C401 shall be included; also all supporting data for the survey shall be included in the line certification survey documentation.

3.4 Part Qualification Test Data

The part manufacturer shall provide qualification test data as required by the general and detail procurement specifications, NSL-A401 and NSL-A401/____, respectively. A summary of the results of the qualification test shall be submitted to the Interagency Data Exchange Program (IDEP).

3.5 Lot Acceptance Test Data

The part manufacturer shall provide lot acceptance test data as required by the general and detail procurement specifications, NSL-A401 and NSL-A401/____, respectively.

3.6 Part History

The prime contractor shall maintain a history documentation required by NSL-A401, NS [illegible], and the applicable detail specifications. This shall include an identification of the part [illegible]cluding a part history of the part manufacturer and his processes), a list of all programs involving the use of each transistor (part usage), and a record of problems and alerts concerning the use of the particular transistor on high-reliability programs.

4. ABBREVIATIONS, SYMBOLS, AND DEFINITIONS

None

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REVISION RECORD

REV	AUTHORITY	DESCRIPTION	RELEASE	
			DATE	APPROVAL

EXAMPLE

NSL-E401/1

DETAIL SUPPORTING DATA SPECIFICATION FOR

NASA SPECIAL LONG-LIFE (NSL) TRANSISTOR, TYPE NSL-401/1

FEBRUARY 1969

CONTENTS

NSL E401/1

DETAIL SUPPORTING DATA SPECIFICATION FOR

NASA SPECIAL LONG-LIFE (NSL) TRANSISTOR, TYPE NSL-401/1

1. SCOPE

1.1 Applicability

This specification is part of the system of Part Control Packages for controlling NASA Special Long-Life (NSL) parts, described in NASA CR-66742-1. This specification is detail section E of Part Control Package NSL-401, and defines the detail supporting data requirements for NSL transistors, type NSL-401/1.

2. APPLICABLE DOCUMENTS

2.1 Documents

The following documents form a part of this specification to the extent specified herein. Unless otherwise specified herein, the issue in effect on the date of the part procurement contract shall apply.

SPECIFICATIONS

NASA

NSL-E401	General Supporting Data Specification for NASA Special Long-Life (NSL) Transistors

(The documents listed in 2.1 of NSL-E401 form a part of this document to the extent specified herein and within the limitations of 2.2 of NSL-E401.)

2.2 Conflicting Requirements

The requirements of 2.2 of NSL-E401 apply.

3. DETAIL REQUIREMENTS

3.1 General

The requirements of 3.1 of NSL-E401 apply.

3.2 Part Manufacturer Survey Documentation

a. Part Manufacturer Questionnaire (specified in NSL-C401)

b. Survey team report (specified in NSL-C401).

3.3 Line Certification Survey Documentation

a. Line Certification Checklist (specified in NSL-C401)

b. Survey team report (specified in NSL-C401).

3.4 Part Qualification Test Data

a. Electrical and Environmental tests (specified in NSL-A401 and NSL-A401/1)

b. Failure analysis -- if applicable (specified in NSL-A401 and NSL-A401/1)

c. IDEP input summary -- (submitted after completion of the above data).

3.5 Lot Acceptance Test Data

a. Physical, electrical, and environmental tests (specified in NSL-A401 and NSL-A401/1)

b. Failure analysis -- if applicable (specified in NSL-A401 and NSL-A401/1).

3.6 Part History

3.6.1 Part Identification

National Semiconductor Corp. part number NS1704 (JEDEC type 2N2484)

3.6.2 Part Usage

HS308 Program
National has 2N2920 on NASA Marshall APL and device is a matched pair of the same chip covered herein.

Military Qualification for the JAN and JAN TX2N929 and 930 per MIL-S-19500/253B (which is the same chip and package as the 2N2484)

Qualified for use on Apollo program by Autonetics (Autonetics I.I.D.472-0719-004)

Used on military and/or space programs by the following contractors.

Litton

Hughes

Lockheed

Barnes.

3.6.3 Problems and Alerts

National will be conducting qualification test in the near future on the 2N2484 per MIL-S-19500/376.

National 2N2484 was placed on high-reliability specification at Hughes Aircraft Company on 11/17/64.

4. ABBREVIATIONS, SYMBOLS, AND DEFINITIONS

None

REVISION RECORD

REV	AUTHORITY	DESCRIPTION	RELEASE	
			DATE	APPROVAL