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# CONCATENATED CODING FOR SPACE COMMUNICATIONS

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## ABSTRACT

A concatenated coding scheme is described which combines bi-orthogonal and parity coding. Results indicated that a substantial power gain of  $6\frac{1}{2}$  decibels over uncoded pulse-code-modulation is achieved. Experimental results indicate that this coding scheme will permit operation at signal-to-noise ratios of two decibels or greater.

Another important feature of this concatenated code is its simplicity of implementation. With presently available low-power microcircuits, the estimated total power consumption for the code generator is 100 milliwatts. The detection operation can be performed in real time.

# CONCATENATED CODING FOR DEEP SPACE COMMUNICATIONS

## INTRODUCTION

Concatenated coding concept links together in a series two or more coding schemes. The coding sequence is usually referred to as having an inner and outer coder. Together the two inner and outer coders are called a super coder (see Figure 1). In the system analyzed, the outer coder uses a parity code and the inner coder uses a bi-orthogonal coder. This technique combines an algebraic (parity) and probabilistic (bi-orthogonal) approach to coding to achieve very long codes (blocks) for which the probability of error decreases at a much higher rate than the system complexity. The concatenated coding technique analyzed has a substantial power gain of 6.5 db over uncoded pulse code modulation (PCM) for a probability of bit error of  $10^{-5}$ . This coding scheme will permit operation at signal-to-noise ratios (SNR) of 2 db or greater.

## ANALYSIS

The outer coder accepts serial uncoded PCM data and reformats it into groups of five bit data words. System performance is directly related to this data word length. Although the analysis assumed five bit data words, this word length can be greater. Greater word lengths would yield lower probability of bit error. Selection of the five bit data word length was a matter of convenience. These five bit data words are grouped into blocks of data to which a parity word is added by performing an odd parity count on each column of the block. There are  $K$  five bit words per block,  $(K-1)$  of these words are information and one five bit parity word. Figure 2 shows a pictorial example of a block of data with parity for  $K$  equal to seven.

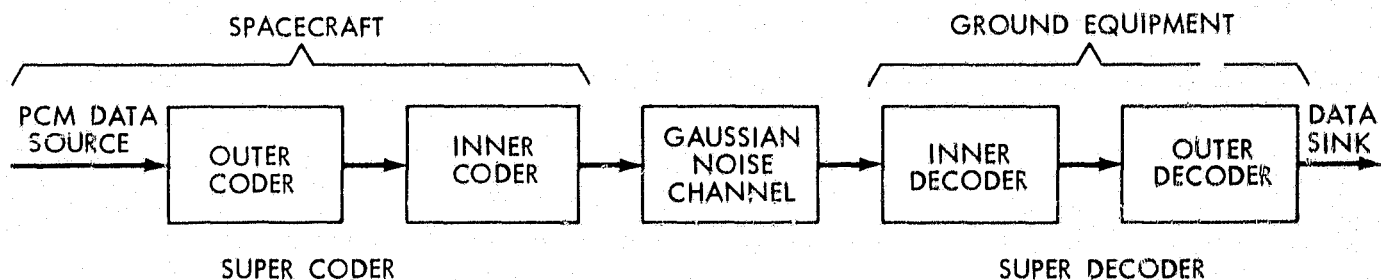


Figure 1. Concatenated Coding Concept

	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5
Data Word 1	1	0	0	0	1
2	1	1	0	1	1
3	0	0	1	0	1
4	0	0	0	1	0
5	1	1	0	1	0
6	0	1	1	1	0
Parity Word	0	0	1	1	0

Note: Parity word is odd parity count of bits in each column.

(a) Block of data and parity for K equal 7 and n equal 5.

	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5
Data Word 1	C	C	C	C	C
2	E	C	C	C	C
3	C	C	C	C	C
4	C	C	C	C	C
5	E	C	C	C	C
6	C	C	C	C	C
Parity Word	C	C	C	C	C

Key: Error (E)  
Correct (C)

(b) Block of data with undetected bit errors.

Figure 2. Pictorial Example of a Block of Data with Parity, and a Block of Data with Undetected Bit Errors in Column One

The inner coder accepts and transforms each five bit word, including the parity word, into a unique bi-orthogonal code word. It is this code which is transmitted through the assumed white Gaussian noise channel. The redundancy and parity bits added results in a bandwidth expansion of  $16K/5(K-1)$  more than the uncoded information. As K increases the required channel bandwidth approaches the bandwidth of the inner coder. For deep space communication, data rates are normally low and bandwidth expansion of this order should easily be passed by the channel.



At the receiving terminal, the noisy data first goes through an inner decoder and then through an outer decoder. The inner decoder uses correlation and a maximum likelihood detector to detect the 5 bit data words. Probability of word error ( $P_w(n)$ ) at the output of the inner decoder is

$$P_w(n) = 1 - \int_{-SNR^{1/2}}^{\infty} \frac{e^{-v^2/2}}{\sqrt{2\pi}} dv \left\{ \int_{-(V + SNR^{1/2})}^{(V + SNR^{1/2})} \frac{e^{-z^2/2}}{\sqrt{2\pi}} dz \right\}^{2^{n-1}-1} \quad [1]$$

where  $n$  is the number of information bits per word, and SNR is the signal to-noise ratio defined as signal energy per information bit per single-sided noise power density. The inner coder/decoder has been built with  $n$  equal to five, and its performance has been verified to give 3 db improvement over uncoded PCM (1). Also the performance of a bi-orthogonal code with  $n$  equal to eight has been verified to operate near the theoretical predictions (4)(5). The detected binary signal from the inner decoder, with errors, is wired to the outer decoder where a parity check is performed on each block of data. If parity does not check, the block is discarded. The remaining blocks, therefore, will have a higher probability of being correct. The undetected probability of bit errors was calculated using the remaining blocks.

The method used to determine the undetected probability of bit error consists of three steps:

1. A calculation is made to determine the discarded block error rate (DBR) as follows:

Let  $P(J)$  be defined as the probability that there will be  $J$  words in error out of a block of  $K$  words. And, let  $P(F/J)$  be defined as the conditional probability that parity will fail to detect an error has occurred, given that  $J$  words are in error. The probability that parity is successful in detecting that an error has occurred is:

$$P(S/J) = 1 - P(F/J)$$

An expression for the joint probability of having  $J$  words in error and having parity detect failure is given by:

$$P(S, J) = P(J) P(S/J)$$

Because the joint probabilities are mutually exclusive events, the discarded block rate is the summation of  $P(S, J)$  as  $J$  assumes values from 1 to  $K$ . In other words:

$$\text{DBR} = \sum_{J=1}^K P(J) P(S/J) \quad [2]$$

The first expression  $P(J)$  is obtained by applying the expression for the binomial distribution:

$$P(J) = \frac{K!}{J! (K-J)!} P_w(n)^J (1-P_w(n))^{K-J}$$

The second expression  $P(S/J)$  can be determined from the following equation:

$$P(F/J) = \sum_{i=1}^{J-1} \frac{(-1)^{i-1}}{(2^n - 1)^i} \quad \text{for } 2 \leq J \leq K$$

And:

$$P(F/J) = 0 \quad \text{for } J = 1$$

This expression assumes that each word error is equally probable.

A detailed derivation of these equations is given in the appendix.

2. The second step in determining the probability of bit error is to find the undetected block error rate  $P_B(K)$ . This is calculated by subtracting the discarded block rate from the total block errors received (TBR) and correcting for the drop in data quantity by dividing by  $(1-\text{DBR})$ . That is to say:

$$P_B(K) = \frac{\text{TBR} - \text{DBR}}{(1-\text{DBR})} \quad [3]$$

where:

$$\text{TBR} = 1 - (1 - P_w(n))^K$$

3. The third step is to determine the undetected bit error rate ( $P_e$ ) from the undetected block error rate:

$$P_e(K, n) = \left( \frac{2^n - 1}{2^n - 1} \right) \left[ \frac{\text{TBR} - \text{DBR}}{1 - \frac{2^n - 1}{2^n - 1} \text{DBR}} \right] \quad [4]$$

A derivation of this equation is given in the Appendix.

## RESULTS

Calculated results from equation (4) are plotted in Figures 3 and 4. When plotting the undetected probability of bit error, the additional bandwidth required by parity is compensated for by increasing the SNR by a factor of  $10 \log (K/K-1)$ . The plotted results are for block lengths of two, four and eight words and with five and eight information bits per word. Also shown on these plots, in parenthesis, is the percent data that was discarded. As an example, the undetected bit error rate at a SNR of 6 db with K equal four and n equal five is  $2 \times 10^{-7}$ . The quantity of data discarded is approximately 0.5 percent.

Another important objective of the study was to determine an optimum block length. This was achieved by plotting a family of curves for constant SNR. The results are shown in Figure 5. From this figure one observes that there is an increase in the undetected bit error rate for small values of K. This increase results from the extra power required to transmit parity. The results also show that for K equal two, parity will detect 97 percent of the errors, but the extra power required to transmit the parity word is increased by a factor of two. The slight increase in the undetected bit error rate for larger K's results from there being more combinations of errors which causes parity to fail. For SNR's between four and six db a block length of 10 appears to be optimum.

For comparison to other coding schemes, the concatenated code is shown with the convolution encoding with sequential decoding schemes developed by Lumb (2) and a GSFC experimental code, developed by Barnes (3), (see Figure 6).

## SYSTEM DESCRIPTION

The system described is based on a five bit per word bi-orthogonal system.

### Spacecraft

An important feature of the concatenated code is its simplicity of implementation. The spaceborne equipment requires just a few logic modules. The outer coder uses five flip-flops to store the data for five bit periods. Standard parity generating circuits require five flip-flops and ten gates. Power to operate this logic is approximately 60 milliwatts. The required timing signals are word rate and frame rate pulses. These are used to generate the block rate pulses which reset the parity generating circuits at the end of each block period. For ease of decommutation and parity generation, the frame length should consist of an

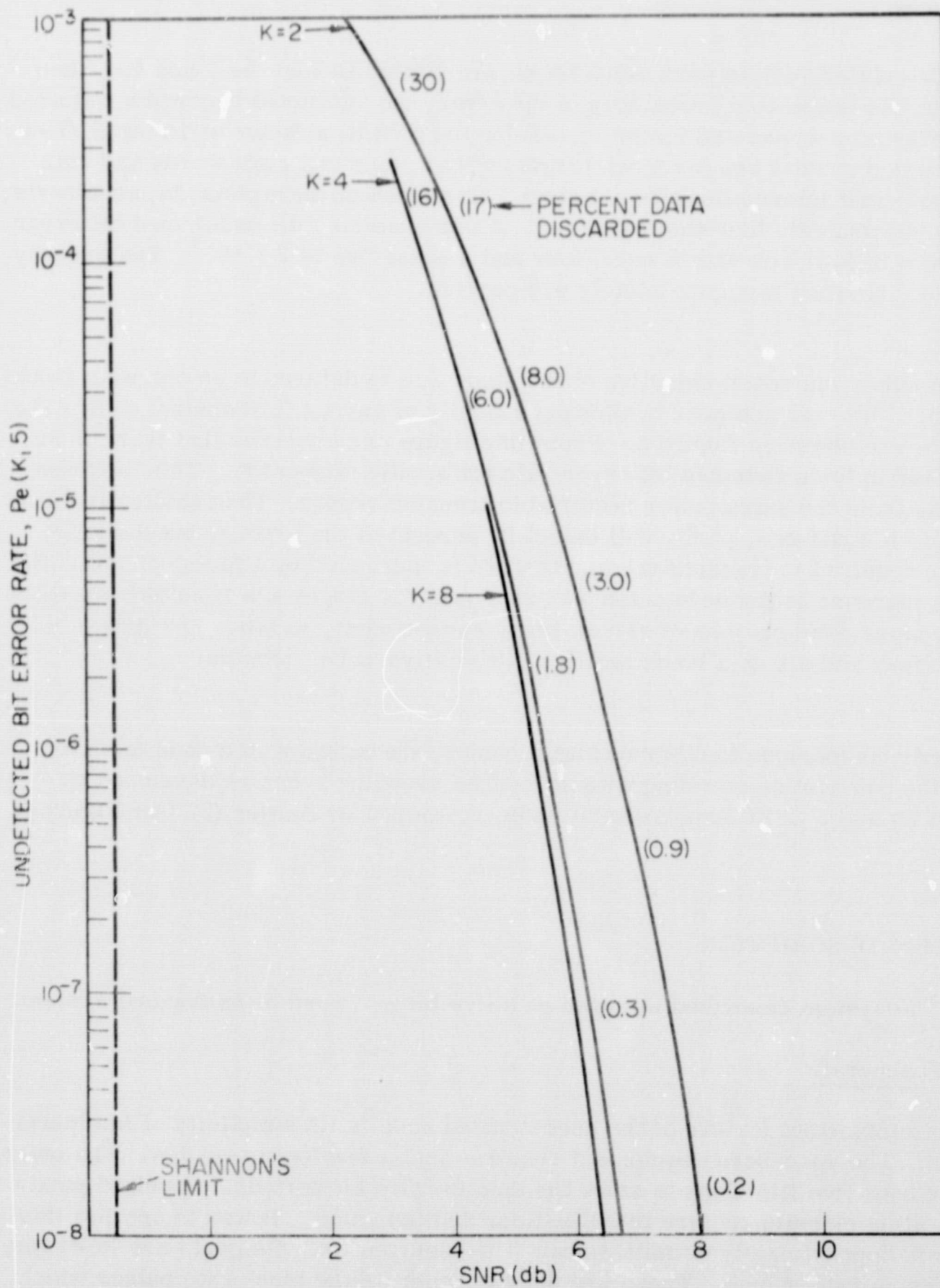


Figure 3. Undetected Probability of Bit Error Versus SNR for Block Lengths Two, Four and Eight with  $n$  Equal to Five

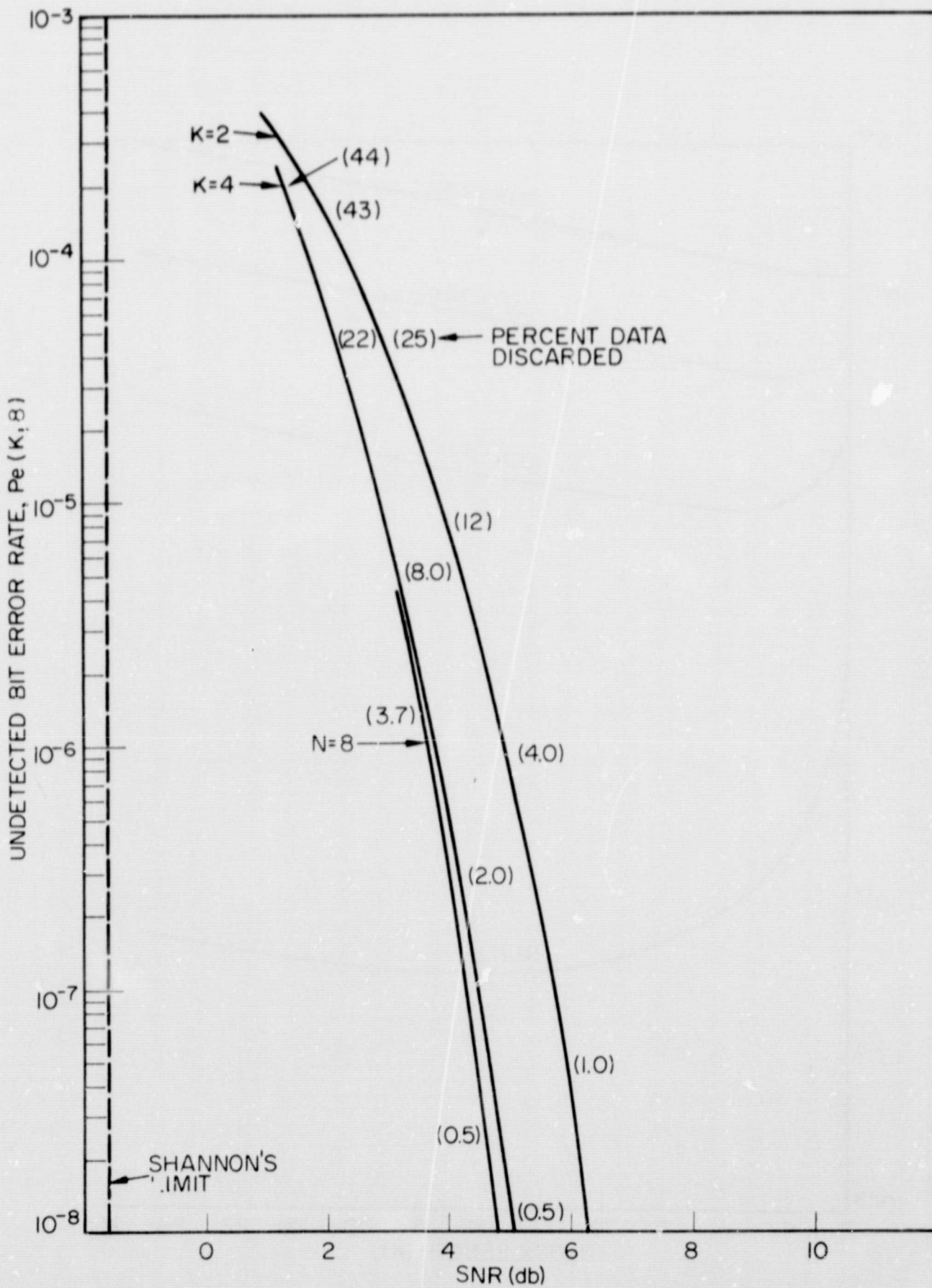


Figure 4. Undetected Probability of Bit Error Versus SNR for Block Lengths Two, Four and Eight with  $n$  Equal to Eight



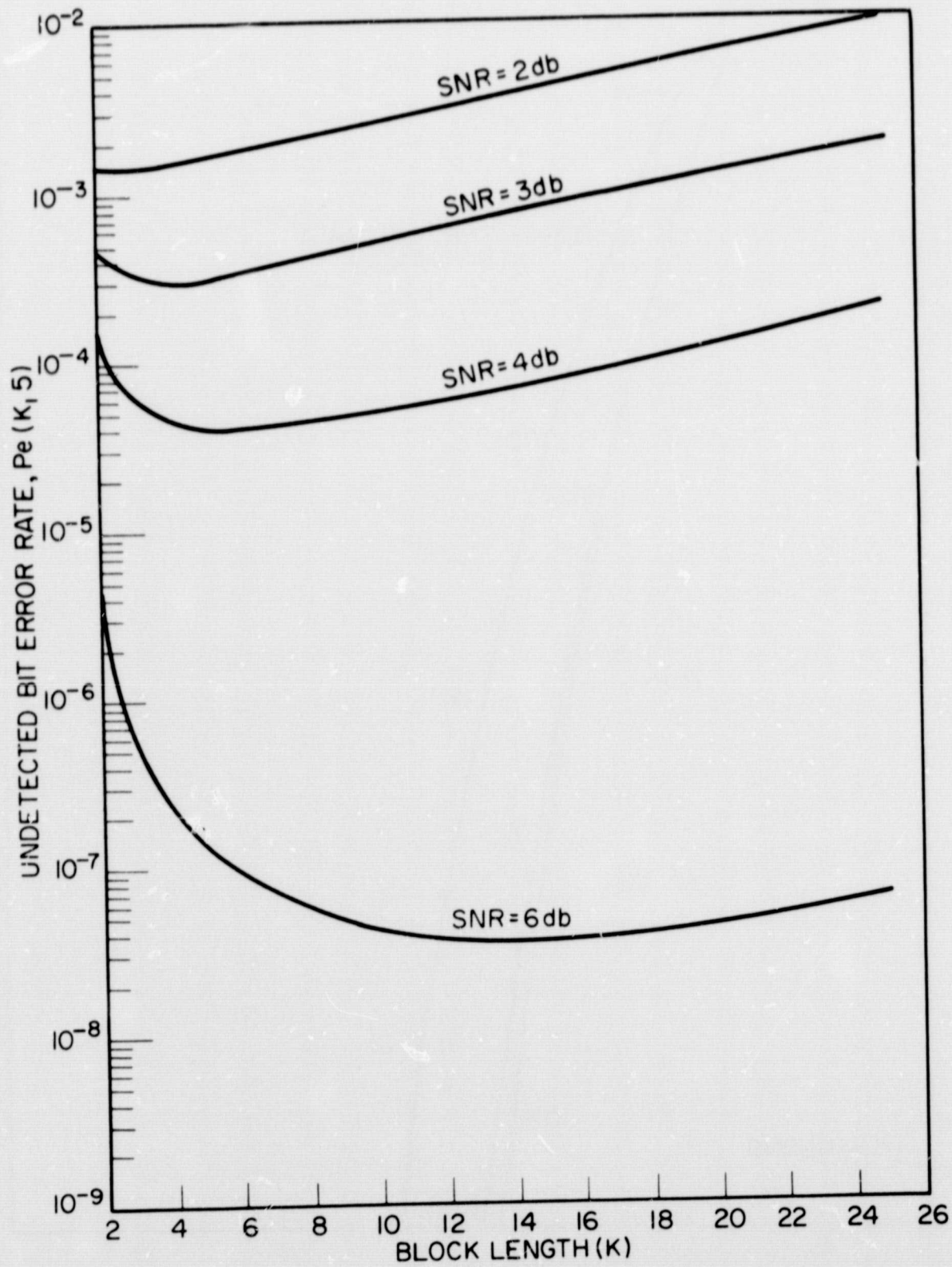


Figure 5. Undetected Probability of Bit Error Versus Block Length for SNR of Two, Four and Six Decibels with n Equal to Five

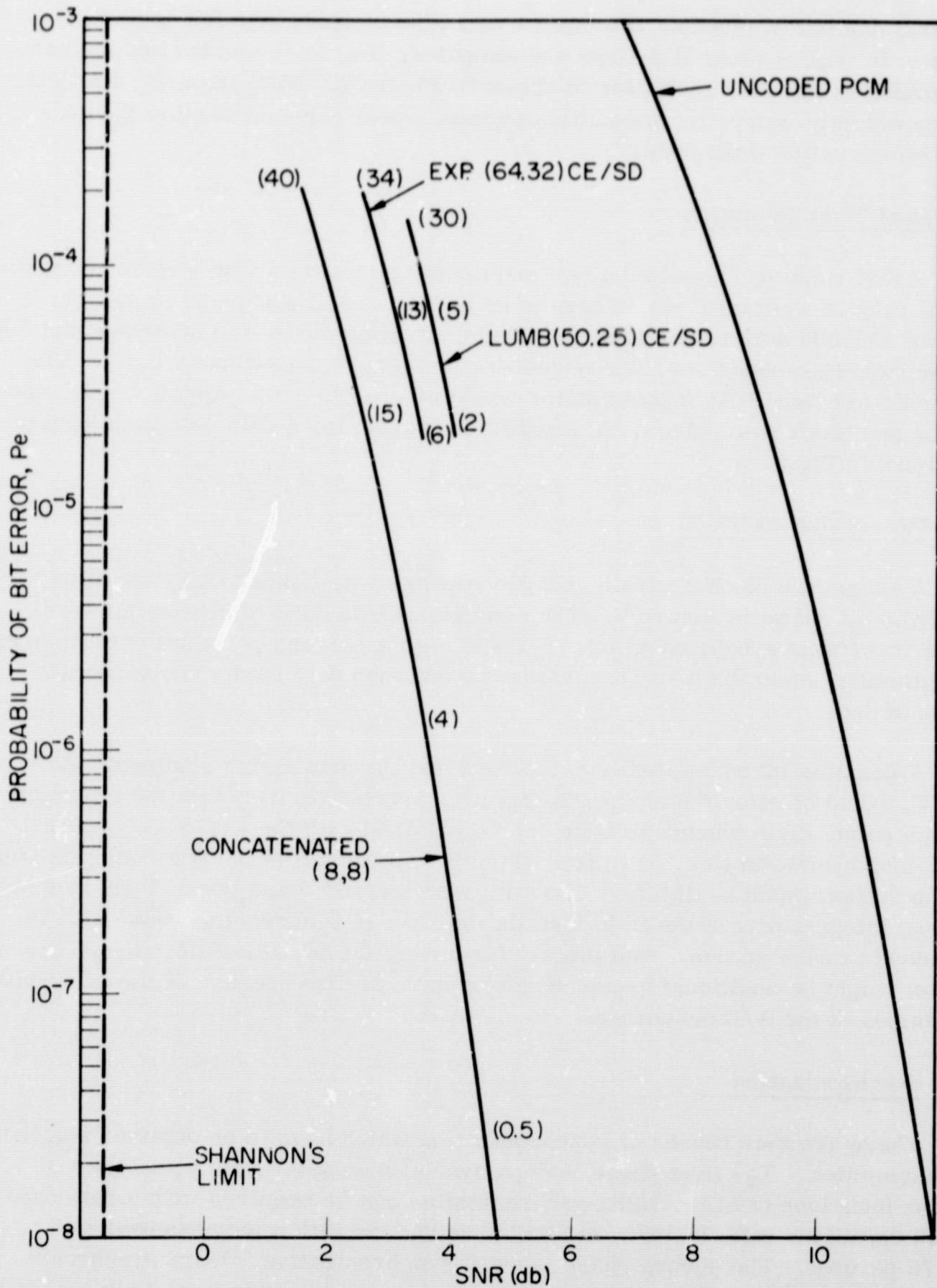


Figure 6. Comparison of Concatenated and Convolutional Encoding with Sequential Decoding Systems on the Basis of Probability of Bit Error and SNR

integral number of blocks. The inner coder also consists of a few logic elements. It requires four flip-flops and ten gates. The logic and timing diagrams pertaining to the code generator is shown in Figure 7. With presently available low-power microcircuits, the estimated total power consumption for the code generators is 100 milliwatts.

### Real Time Detection

If real time decommutation is a requirement at a receiving station, an additional rack of equipment would have to be added to each station at an estimated cost of \$35,000 dollars per station. This rack would house the bi-orthogonal decoder, word synchronizer, parity decoder and block generating circuits. The station's existing PCM decommutator would be used to obtain frame synchronization and block rate pulses. A schematic diagram for a data detection system is shown in Figure 8.

### Processing At GSFC

A schematic block diagram of a processing system using GSFC computer facilities is shown in Figure 9. The computer would have to determine word, block and frame synchronization. It would also use cross correlation techniques to optimally detect the bi-orthogonal codes and then do a parity check on each block of data.

A possible interface, between the field and the processing equipment at GSFC, would be after the analog-to-digital converter (A/D). With the interface at this point, digit synchronization can be obtained with the narrowest phase-lock-loop bandwidth (i. e., no jitter added by tape recorders). The recorded signal at the station would be digital. The digit matched filter and phase-lock-loop are now an integral part of the field installation. An A/D converter would have to be added to each station. One penalty for having the interface after the A/D converter might be additional use of magnetic tape storage because of the bandwidth expansion of the A/D converter.

### Synchronization

There are four phases of synchronization which have to be obtained before data detection. The first phase is digit synchronization. This phase uses a phase-lock-loop (PLL). Digit synchronization can be acquired with a data bandwidth expansion ratio of 16/5, at SNR of +2 db, and with a loop bandwidth of  $\pm 0.75$  percent. The second phase is word synchronization. Word synchronization can be achieved by using a self synchronizing bi-orthogonal code set which does not require additional bandwidth. Using this technique, word synchronization was acquired at SNR of +2db. Word synchronization threshold was



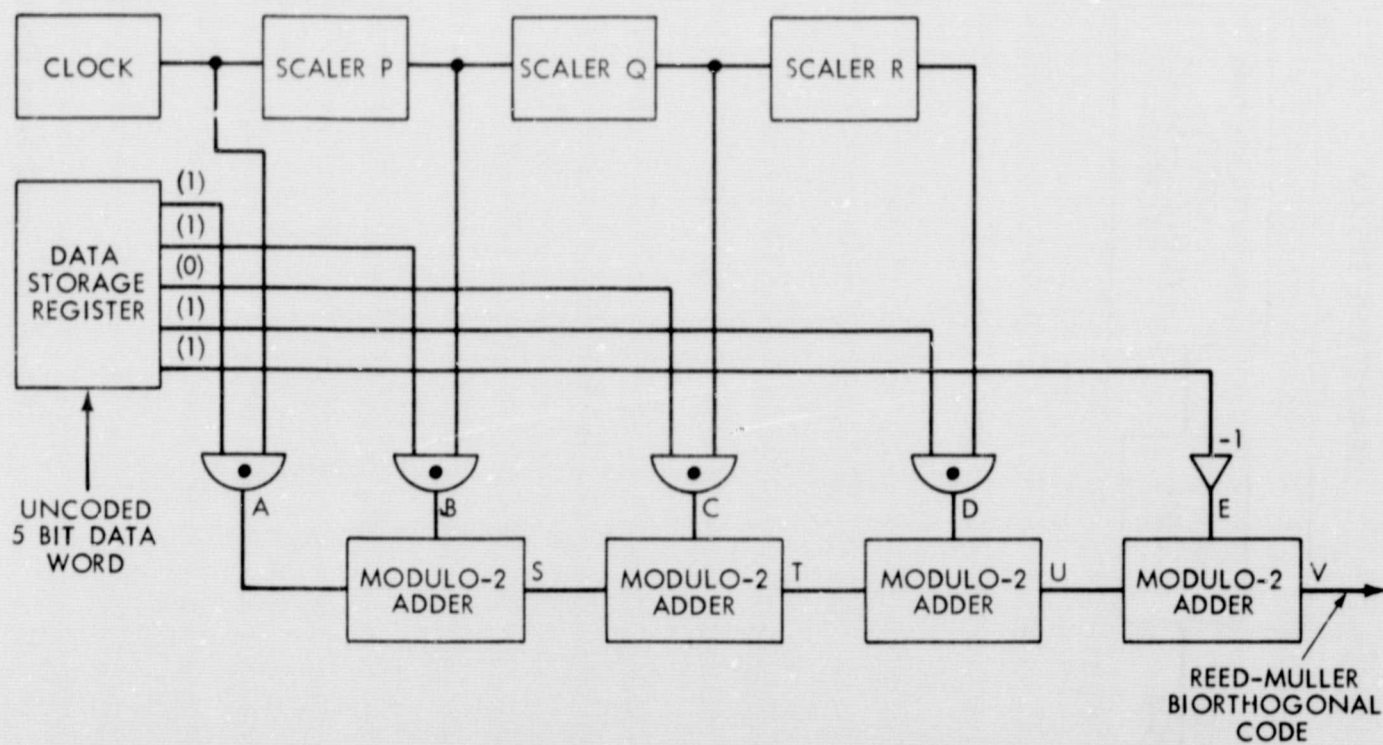
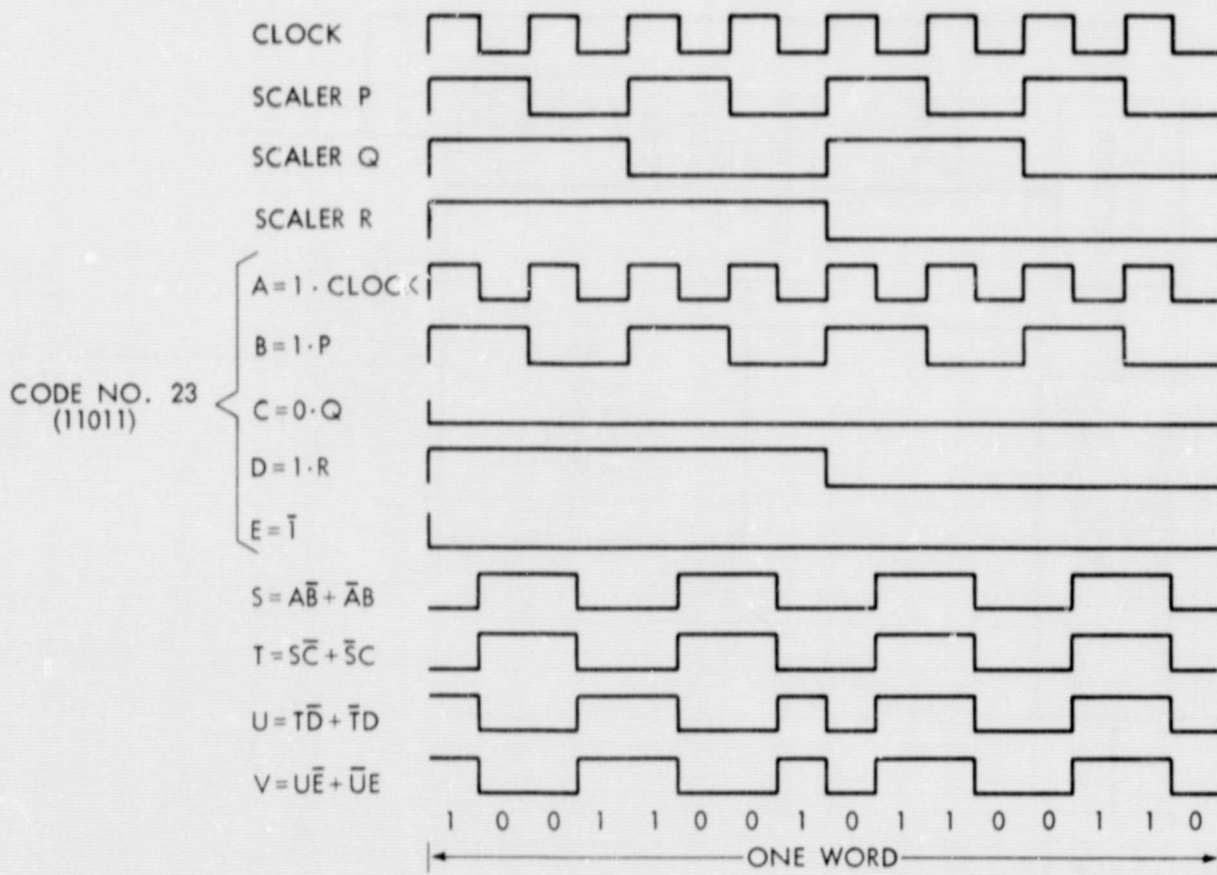


Figure 7. Logic and Timing Diagrams of Bi-Orthogonal Code Generator

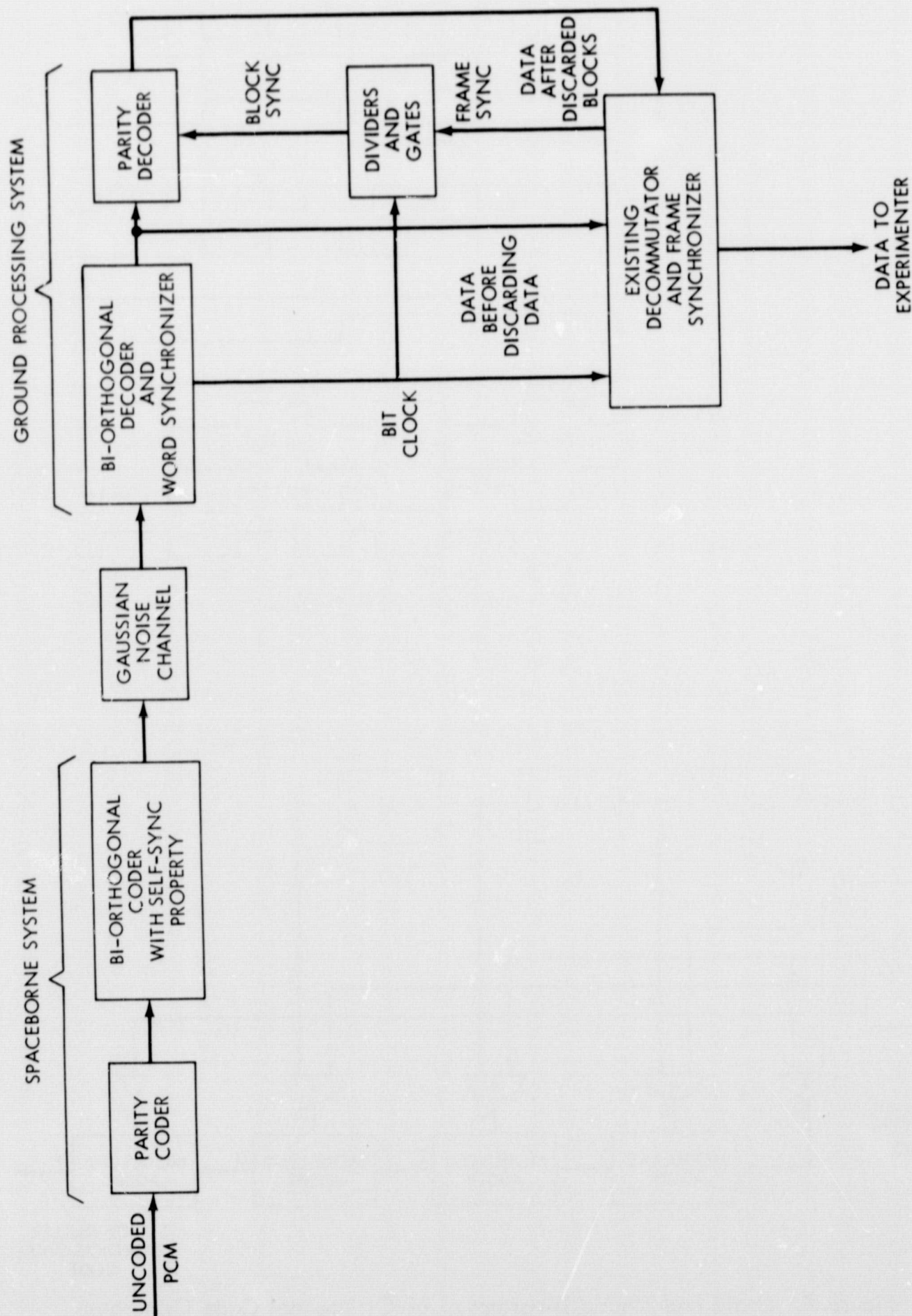


Figure 8. Real Time Detection Scheme Using Existing Decommutator



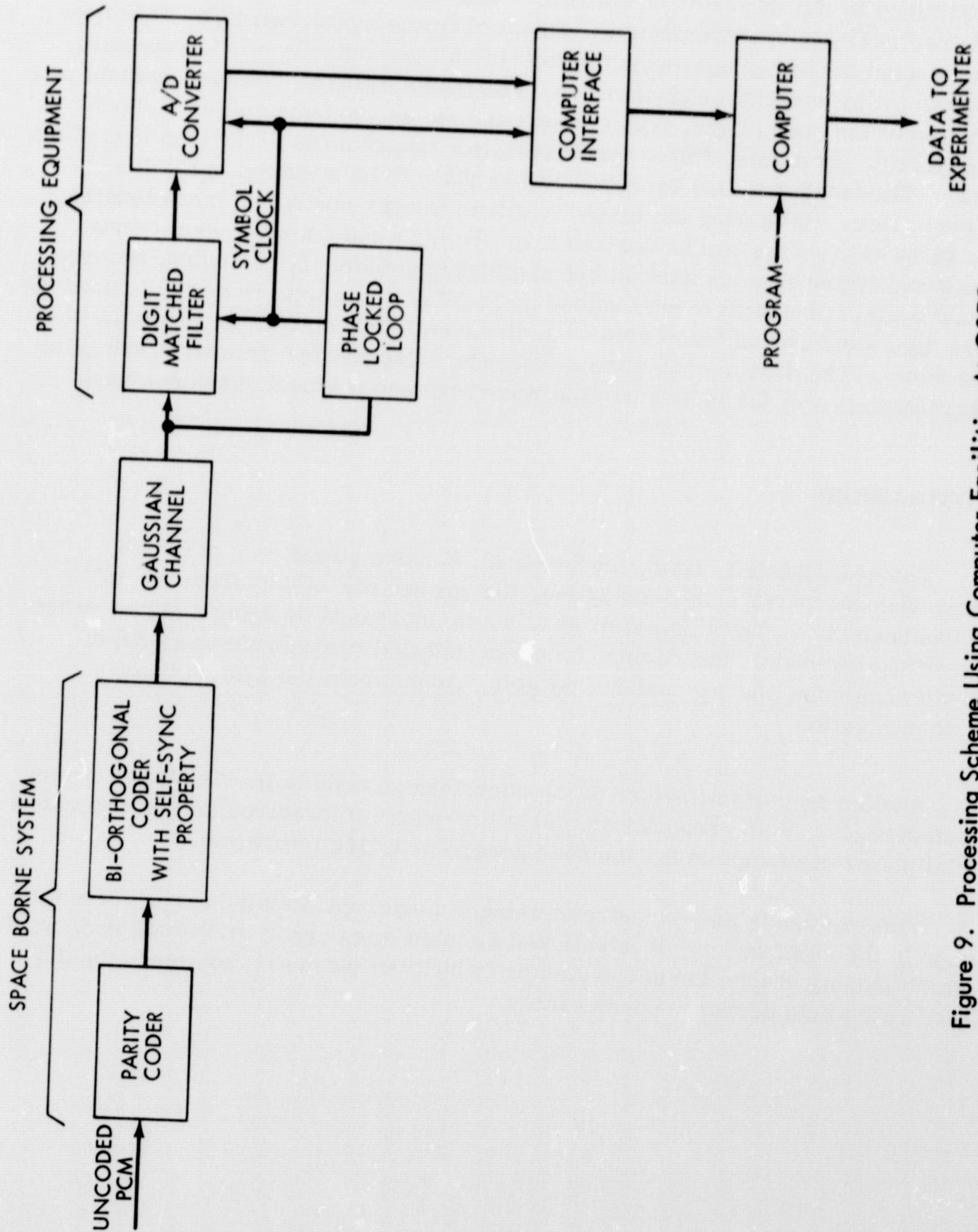


Figure 9. Processing Scheme Using Computer Facilities At GSFC

determined by the threshold of the PLL. The third synchronization phase to be obtained is frame synchronization. Standard frame synchronization techniques can be used for this phase, which is to transmit periodically a unique pattern, and use cross correlation to detect it. The frame synchronization threshold is a function of the code length, frame length and the desired acquisition and hold philosophy. As a rule, frame synchronization threshold is lower than that of the PLL. The fourth and last synchronization phase to be acquired is block synchronization. By making the frame length an integer number of block lengths, the block rate pulses can be derived from the digit and frame clocks. Thus, block and frame synchronization are acquired together. In summary, the combined system threshold is determined by the PLL. If a tape recorder is used before digit synchronization is achieved, the system threshold would increase considerably. The degree of threshold increase is largely determined by the jitter characteristics of the individual tape recorders and playback machines used.

## CONCLUSIONS

The concatenated coding technique (8, 8) has a power gain of 6.5 db over uncoded pulse code modulation, for probability of bit error of  $10^{-5}$ . It has been shown that this power gain can be increased by using a higher order bi-orthogonal code. The coding technique analyzed can operate to a SNR of +2 db when using the n equal five system. At this SNR the system loses synchronization.

Another important feature of the concatenated code is its simplicity of implementation. With presently available low-power microcircuits, the estimated total power consumption for the code generator is 100 milliwatts.

Future studies may investigate using a more sophisticated error correcting code in the outer coder. It is believed a single word error correcting code would not noticeably change the undetected probability of bit error; however, the discard rate would decrease considerably.

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1. Miller, W., et al., "Self-Synchronizing Bi-Orthogonal Coded PCM Telemetry System." NASA Technical Report R-292, September 1968.
2. Lumb, D. R., and L. B. Hoffman, "An Efficient Coding System For Deep Space Probes with Specific Application to Pioneer Missions." NASA TN D-4105.
3. Barnes, W. P., "A Simulation of Convolutional Encoding with Sequential Decoding with Application to IMP-I and AIMP-H, J Data Processing." NASA X-563-60-65.
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APPENDIX  
CONDITIONAL PROBABILITY P(F/J)

The conditional probability that parity can detect an error given that there are J words in a block that are in error, is arrived at in the following manner. When one word is in error (i.e. J equals one), there are  $2^n$  possible codes, one of which is the correct code. Since we are given that there is an error, there are  $(2^n - 1)$  possible erroneous codes. The conditional probability that parity will fail given that one word is in error is:

$$P(F/1) = 0/(2^n - 1) = 0.$$

When J equals two, there are  $(2^n - 1)^2$  different error patterns. Of these there is a total  $(2^n - 1)$  code combination that will cause parity to fail. In this analysis, each possible code failure is assumed to be equally probable. This assumption is good for orthogonal codes; for bi-orthogonal codes there are  $(2^n - 2)$  codes that are equally probable. However, the complement code has a smaller chance of being detected since its normal correlation is in the negative direction. See Figure 2 (b) for an illustrated code combination that caused parity to fail. Hence, the conditional probability that parity will fail given that two words are in error is:

$$P(F/2) = \frac{(2^n - 1)}{(2^n - 1)^2} = \frac{1}{(2^n - 1)}$$

For J equals three, there are a total of  $(2^n - 1)^3$  error patterns. Of these there are  $(2^n - 1)^2$  words, where compensating pairs of column errors will cause parity to fail. When the third bit of the column is considered, the total number of compensating pairs of column errors are reduced by a factor of  $(2^n - 1)$ . From this, given that three words are in error, the conditional probability that parity will fail to detect an error is:

$$P(F/3) = \frac{(2^n - 1)^2 - (2^n - 1)}{(2^n - 1)^3}$$

Which reduces to:

$$P(F/3) = \frac{1}{(2^n - 1)} - \frac{1}{(2^n - 1)^2}$$

Following the above procedure a general expression can be derived to determine the condition probability that parity will fail when it is given there are J words in error:

$$P(F/J) = \sum_{i=1}^{J-1} \frac{(-1)^{i-1}}{(2^n - 1)^i} \quad \text{for } 2 \leq J \leq K$$

And:

$$P(F/1) = 0 \quad \text{for } J = 1$$

This equation was verified analytically by a computer which was programmed to search through all code combinations and to determine the total number of times parity failed for various J values from two to six.

#### BIT ERROR PROBABILITY

If the inner coder uses an orthogonal code the word errors are equally probable, and the conditional probability that a given bit is in error when an n-bit word is detected incorrectly is  $2^{n-1}/(2^n - 1)$ , (1). When the inner coder uses a biorthogonal code the complement code causes the bit error derivation to be somewhat complicated. However, the probability of selecting the complement code to the transmitted code is much less than selecting a code orthogonal to it, since the Hamming distance for the complement code is twice that of the orthogonal codes. The biorthogonal code is used in the following analysis, and each possible code failure is assumed to be equally probable.

The probability of bit error is derived by subtracting the discarded bit rate, DER, from the total bit error rate before discarding known errors, TER, and correcting for the drop in data quantity by dividing by  $(1 - DER)$ . That is:

$$P_e(K, n) = \frac{TER - DER}{1 - DER}$$

Assuming word errors are independent, the probability of word error before discarding words is:

$$TBR = 1 - (1 - P_w(n))^K,$$

where K is the number of n-bit words per block. From this expression, TER can be derived by multiplying this probability of word error by the conditional

probability that a given bit is in error when an n-bit word is detected incorrectly. This is written as:

$$\text{TER} = (2^{n-1}/(2^n - 1)) \text{TBR}$$

Similarly, an expression for the probability of discarded bit error can be written as:

$$\text{DER} = (2^{n-1}/(2^n - 1)) \text{DBR}$$

When substituting these terms into the original equation the following equation results:

$$P_e(K, n) = (2^{n-1}/(2^n - 1)) \cdot \frac{\text{TBR} - \text{DBR}}{1 - (2^{n-1}/(2^n - 1)) \text{DBR}}$$

#### REFERENCE

1. Viterbi, A. J., "On Coded Phase-Coherent Communications," IRE Transactions on Space Electronics and Telemetry, March 1961.