X-711-69-91
PREPRINT



# THE IMP-I COMPUTER EXPERIMENT

RODGER A. CLIFF
STEPHEN PAULL

MARCH 1969


GODDARD SPACE FLIGHT CENTER
GREENBELT, MARYLAND

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ILLUSTRATIONS

# THE IMP-I COMPUTER EXPERIMENT

Rodger A. Cliff and Stephen Paull
NASA/Goddard Space Flight Center
Greenbelt, Maryland 20771

## ABSTRACT

The SDP-3 Computer was designed to serve as the core of the data system of a small unmanned spacecraft. It is a 16-bit serial machine with 4096 words of memory. The computer will be flown as an engineering experiment on IMP-I. In this application it will handle control and data compression for 4 scientific experiments. Interface between the computer and the experiments is accomplished by experiment interface packages which are located within the experiment package. These experiment packages are supplied to the experiment builder by the computer builder. The experiment interface packages are constructed from a line of standard interface modules, which in turn are built of the same IC's used in the SDP-3. An adaptive format consisting of data tagged with identification and word count is used for data transmission.

## GENERAL DESCRIPTION

The IMP-I computer experiment is being performed in anticipation of future advanced IMP-type spacecraft which may use a computer as the core of the spaceborne data system.

### Objectives of the Experiment:

The foremost advantage of a stored-program computer is its flexibility; the same hardware may be used to perform many different functions by changing the program. A related advantage is that comparatively simple hardware coupled with sophisticated software can accomplish tasks which would usually require much more complex hardware. In addition, time-shared operation of a computer can allow it to replace several different conventional hard-wired systems.

Disadvantages of a central time-shared computer include possible penalties in power drain and reliability. Within the present state of the art, the chief power hog in a spacecraft computer is the core memory. When operating at full speed, the IMP-I computer will draw about 10 watts. Three-fourths of this power (7.5w) goes to the memory. Hopefully future advances in magnetic, semiconductor LSI, and other, memories will alleviate this problem. In the meantime we must make reasonable trade-offs between how much we ask the computer to do and how much power it takes to do it. The reliability of a central computer may in principle be made arbitrarily high by appropriate redundancy techniques. The problem is one of cost, both in components and power drain. Another approach is to back up a powerful central computer with a hard-wired system of minimum complexity and low, but non-zero, capability.

We have had considerable experience with hard-wired data systems for small scientific spacecraft, but no comparable experience with computerized data systems. Consequently, we are flying a computerized data system on IMP-I (launch will probably be in mid 1970) as an engineering experiment. This will give us the experience we lack. We will then be able to make more meaningful comparisons between hard-wired, computerized, and hybrid data systems.

Typical problem areas in which we intend to gain experience are:
1) Interface with scientific experiments (hardware, software, and experimenter acceptance).
2) Time-shared real-time operation of a small computer.
3) Remote reprogramming of a computer in flight.
4) Verification of hardware and software operation (both prelaunch and post in-flight reprogramming).
5) Programmed experiment control.
6) In-flight data processing and buffering.
7) Variable format data transmission.
8) Ground-based processing of data from a computerized spacecraft.

### The SDP-3 Computer:

We will use a computer called the SDP-3 (Spacecraft Data Processor) in the IMP-I computer experiment. It is a 16-bit, serial, single word instruction, single address machine. It has 16 levels of priority interrupt and two modes — user and monitor — in order to effectively handle time-shared processing. The memory consists of up to 256 pages of 256 words each. A 16-page memory (4K words) will be flown on IMP-I. Interpage write access is prohibited in the user mode.

The SDP-3 features one level of indirect addressing and one hardware index register. Arithmetic is done in

two's-complement fixed-point format. There is a shift-left-and-normalize instruction, but other floating-point operations and multiplication and division must be provided by software.

Each SDP-3 instruction takes 64 bit times; this simplifies the control hardware. At the end of an arithmetic operation the result may either be put in the AC (in which case the second operand is restored in the memory) or the result may be stored in the memory location formerly occupied by the second operand (in which case the first operand remains unaltered in the AC).

The format of an instruction word is:

CCCCCC F T LLLLLLLL.

The 6-bit operation code CCCCCC allows 64 instructions of which 54 are being used. The flag bit, F, specifies indirect addressing if it is on and the tag bit, T, specifies indexing if it is on. Addresses within a page are specified by the 8-bit line number LLLLLLLL.

There is a continuously-running real-time clock which may be armed under program control to cause an interrupt at some selected time in the future. Also, the current value of the clock may be stored in the memory to mark the time of occurrence of some particular event. If there is a power outage, the computer marks its place and automatically restarts when power is restored. There are 32 binary control outputs which may be used to control experiments, the telemetry system, and the multiplexor which commutates the data from the experiments into the computer.

The SDP-3 (excluding the memory electronics) will consist of about 600 Fairchild LPDT$\mu$L circuits with an operating power dissipation of about 2.5 watts. Average dissipation will be even less because whenever the computer is idle, it enters a dormant low-power mode in which only the priority interrupt circuitry is energized. The volume is estimated to be of the order of 200 cubic inches and the weight about 4 pounds. The memory requires another 200 cubic inches and 4 pounds and draws about 7.5 watts at full speed.

The hardware of the SDP-3 computer is packaged in four separate boxes. The memory, including core stack, core access circuits, address register and storage buffer register, is one of these boxes. It is called MSU for convenience. The CPU box contains the accumulator and extension, index register and location counter, arithmetic hardware, and timing and control circuitry. The priority interrupt circuitry, real-time clock, and control registers are housed in the RTU (Real Time Unit). Interface circuitry for connecting the scientific experiments to the SDP-3 is contained in the EIU (Experiment Interface Unit). The MSU and CPU boxes are standard for all applications and represent a minimum configuration of the SDP-3. The RTU box is added for time-shared or real-time (or both) operation. The EIU is a "semi-custom" unit. Its design may be changed to adapt the SDP-3 to various spacecraft data systems. It would normally not be redesigned during a series of missions in a particular type of spacecraft, even though the experiments on each specific mission were different.

Computer Experiment Configuration:

Figure 1 is a block diagram of the IMP-I computer experiment. It shows 4 scientific experiments connected to the RTU and EIU of the SDP-3. The exact nature of this connection is discussed in the section of this paper "INTERFACE WITH SCIENTIFIC EXPERIMENTS."

Data is output from the SDP-3 computer by the output channel. This data is usually fed to the telemetry encoder of the normal spacecraft data system. To the encoder, the computerized data system looks just like any other experiment. The encoder time-division multiplexes the data from the SDP-3 with that of the other experiments. The data then passes through the switch shown in Figure 1 to the modulator and transmitter. Modulated RF from the transmitter passes through a diplexer to the spacecraft antenna and is transmitted to the earth.

The telemetry encoder has two rates which are selectable by ground command. When it is running at the low rate (400 data bits per second), it accepts 25 bits per second from the SDP-3. When it is running at the high rate (1600 bits per second), it accepts 100 bits per second from the SDP-3. Whenever extremely high output data rates from the SDP-3 are desired (for instance for a memory dump during checkout) the output channel may be connected directly to the modulator and transmitter. This is accomplished by ground command of the switch in the input of the modulator and transmitter. The output channel will then drive the modulator and transmitter at either 800 bits per second or 3200 bits per second. In this case the rate is selected by the SDP-3 program.

Either new programs or modifications of existing programs may be loaded into the SDP-3 via the command receiver and the SDP-3 input channel. Each command sent from the ground consists of a memory address followed by the word to be stored at that address. When the entire command has been decoded, checked for transmission error, and accepted, it is loaded into the memory on a cycle-steal basis. The maximum memory loading rate is about 2 words per second.

## INTERFACE WITH SCIENTIFIC EXPERIMENTS

The SDP-3 computer has, in its present configuration, the capability of servicing up to 8 scientific experiments. The block diagram of Figure 1 shows the overall interface scheme. An Experiment Interface Package (EIP) is installed as a part of the instrumentation electronics of each experiment being served by the computer.

Each EIP consists of from 10 to 16 Standard Interface Modules (SIM).

There are 9 different kinds of SIM:
1) Transfer Register, 8-Bit
2) Counter-Control Module
3) Command Memory, 6-Bit
4) Trigger Logic Module
5) Counter, 8-Bit
6) Counter, 7-Bit with Latch
7) Power Switch
8) Data Gates, 4 Channel
9) Parallel Extender Gates

The SIM in each EIP are interconnected in such a manner that they meet the operating requirements of the particular experiment. Because each experiment has a unique set of requirements, a unique interconnection configuration is necessary in each EIP.

SIM's are made of the same integrated circuit family as the SDP-3 itself; therefore, the EIP's are effectively electrical extensions of the SDP-3. Care has been taken in the design to minimize the number of wires between the SDP-3 and the experiments. As a result, no more than 7 wires are required to connect the SDP-3 to any one of the EIP's. The actual interface between the SDP-3 and the experiment (the EIP to experiment interface) usually requires many more interconnecting wires. Since this interface is between the built-in EIP and the other experiment electronics, no interconnecting cables are involved.

Both parallel and serial transfer of information are used between the SDP-3 computer and the experiments:
1) The storage buffer register has parallel access to the computer memory.
2) The transfer register in an EIP has parallel access to the experiment instrumentation electronics.
3) Direct connections between the RTU and each EIP provide parallel transfer of a limited number of control signals from the computer to the experiments and priority interrupt service requests from the experiment to the computer.
4) Information exchange between the storage buffer register and the transfer register of an EIP is a serial shifting operation through the serial selection gates in the EIU. This route serves only one experiment at a time.

General Interface System Design:

The parts of the SDP-3 which are active in communicating with an EIP are shown in Figure 2. Priority interrupt service requests from the EIP are fed directly to the priority interrupt circuitry of the RTU. Bits of the CA register in the RTU are used to address the appropriate set of experiment selection gates in the EIU. These gates route clock pulses and execute pulses to the selected EIP. They also connect the storage buffer register in the MSU to the selected EIP.

Figure 3 illustrates the operation of a typical EIP. There are 25 connections between the EIP and the rest of the experiment electronics. These include:
a) Command control lines which may be set by the computer to control experiment circuits.
b) 16 input lines for experiment data which is to be transferred to the computer memory.
c) A data ready trigger which is generated by the experiment electronics to initiate a transfer of data into the computer.
d) 2 reset lines which reset the experiment electronics at the end of a data transfer operation.

Exchange of information between an experiment and the computer may be initiated by either the experiment or the computer. Figure 4 is a timing diagram which illustrates these two different modes of operation.

The upper portion of Figure 4 illustrates operation initiated by circuits in the experiment electronics. A ready trigger from the experiment circuits to the trigger logic module turns on the priority interrupt latch P, and initiates the operation of monostable pulse generators D, L, R, and e. The pulse D is used to clear the transfer register and also provides a delay to allow gating circuits and accumulators to stabilize before data transfer takes place. The pulse L activates the parallel data gates and loads the experiment data word into the transfer register. The pulse R is available for resetting circuits in the experiment, and the pulse e is available to disable data input gates during the time of data transfer into the EIP. The data word is serially shifted from the transfer register into the storage buffer register by sixteen clock pulses when the computer responds to the priority interrupt service request with a machine instruction XMIN (Exchange Memory and Input, No execute pulses). The sixteen clock pulses also are used to reset the priority interrupt latch P.

The lower portion of Figure 4 shows timing of EIP operation during computer-initiated instructions XMIB (Exchange Memory and Input, execute pulses Before clock pulses) and XMIA (execute pulses After clock pulses). In both of these instructions, the counter-control module in the EIP decodes the four execute pulses and furnishes four control pulses on separate wires:
1) T, a transfer pulse to shift the contents of the first six bits of the transfer register into the command memory module.
2) C, a clear pulse to clear the transfer register to all zeros.
3) L, a load pulse to activate the parallel data input gates.
4) R, a reset pulse.

When the computer executes an XMIB instruction, these control pulses precede the sixteen clock pulses, and are used to transfer a data word into the transfer register. When the computer executes an XMIA instruction, the control pulses follow the sixteen clock pulses and are

used to transfer a command word from the transfer register into the command memory module.

Experiment Interface Packages:

The SDP-3 computer interfaces with 4 experiments on the IMP-I spacecraft:
1) University of California cosmic ray experiment.
2) University of Chicago cosmic ray experiment.
3) Goddard Space Flight Center plasma experiment.
4) University of Minnesota fluctuating electric and magnetic fields experiment.

University of California EIP: The University of California experiment transfers two kinds of data into the computer:
1) Pulse height analyzer random event data in the form of a six-bit word for each event.
2) Lost events data in the form of a sixteen-bit word obtained at regular intervals from an accumulator in the EIP.

Transfer of a six-bit pulse height analyzer data word into the computer is initiated by a "data ready" trigger fed from the experiment circuits to the trigger logic module in the EIP. This results in the following action:
1) A priority interrupt signal P2 is sent to the computer RTU.
2) Trigger logic pulse D clears the transfer register and counter-control module.
3) Trigger logic pulse L loads the six-bit data word into the first six stages of the transfer register.

The computer subsequently responds to the priority interrupt with an XMIN input-output instruction. This shifts the data word from the transfer register into the storage buffer register and turns off the priority interrupt latch.

The experiment circuitry furnishes an "end of cycle" trigger whenever the lost events count in the accumulator is to be transferred into the computer. This turns on the priority interrupt P1 which is fed to the computer RTU. The computer subsequently responds to the priority interrupt with an XMIB input-output instruction. The execute pulses preceding the sixteen clock pulses are used to transfer the contents of the accumulator into the transfer register:
1) The pulse C clears the transfer register.
2) The pulse L loads the contents of the accumulator into the transfer register.
3) The pulse R resets the accumulator.
The sixteen clock pulses shift the data word from the transfer register into the storage buffer register. This action also resets the priority interrupt P1.

University of Chicago EIP: Random event data from two pulse height analyzers is transferred from this experiment into the computer as a single sixteen-bit word:
1) Bits 1 through 7: pulse height analyzer number 1.
2) Bits 8 through 14: pulse height analyzer number 2.
3) Bits 15 and 16: identification bits.

The experiment has two interface operation modes:
Mode 1) The experiment sends only those events to the computer which are also being sent to the telemetry encoder.
Mode 2) Experiment events are sent to the computer as fast as the events occur, limited only by the availability of input-output service from the computer.

Operation of the EIP is the same for either mode of interfacing operation. The computer determines which mode is to be used and transmits this information to the EIP by means of the mode control bit from the RTU.

Two power supply control switches in the EIP are normally off when the experiment is not interfacing with the computer. Whenever data is to be processed by the computer, a control bit from the computer RTU turns on switch SW-2. This powers two accumulators for pulse height analyzer data and the trigger logic module. SW-1, which powers the remaining EIP modules, is turned on only during input-output information exchange between the computer and the EIP.

Each pulse height analyzer event that is sent to the accumulators is preceded by a preset-clear pulse to set the accumulators to zero. Transfer of the contents of the accumulators to the computer is initiated by a data ready trigger which is fed from the experiment electronics to the trigger logic module in the EIP. This turns on the priority interrupt latch which is fed directly to the computer priority interrupt service request line, and also initiates 3 trigger logic monostable signals:
1) The pulse e inhibits the accumulator input gates during the time the data is being transferred into the transfer register.
2) The pulse D clears the transfer register and counter-control module.
3) The pulse L loads the contents of the counters into the transfer register stages 1 through 14, and the two identification bits into stages 15 and 16.

The computer subsequently responds to the priority interrupt service request with an XMIA input-output instruction. The sixteen clock pulses shift the data word from the transfer register into the storage buffer register. The last execute pulse R following the clock pulse burst resets the priority interrupt latch.

GSFC Plasma Experiment EIP: Event rate information from this experiment is transferred into the computer memory at regular spacecraft spin sector intervals. Sector trigger pulses are fed from the computer RTU directly to the trigger logic module in the EIP. Each trigger pulse initiates the following action:
1) Power supply latch P turns on the power to the transfer register and parallel data gate modules.
2) Trigger logic pulse e disables the input gate to the rate data accumulator during the parallel transfer of accumulator contents into the transfer register.
3) Trigger logic pulse D clears the transfer register and counter-control module, and also provides a delay to allow the accumulator stages to stabilize.

4) Trigger logic pulse L loads the contents of the accumulator into the transfer register.
5) Trigger logic pulse R resets the accumulator.

The computer subsequently executes an XMIA input-output instruction which shifts the data word from the transfer register into the storage buffer register. A command word is simultaneously shifted from the storage buffer register into the transfer register, and the execute pulse T, which follows the sixteen clock pulses, transfers the command word into the command memory module. The output from this module furnishes six bits for control of experiment circuits. The execute pulse R resets the power supply control latch P to OFF.

University of Minnesota EIP: A mode control bit fed from the computer Real-Time Unit directly to the University of Minnesota EIP sets the experiment into either the survey mode or the measurement mode. While the experiment is in the survey mode, the computer samples the output of wide-band detecting circuits in the experiment at programmed time intervals. In this sampling operation, the computer transfers 16-bit data words from the experiment electronics into the computer memory with the I/O instruction XMIA.

When wide-band data gathered during survey mode operation indicates that significant measurements can be made in specified narrow-band frequency ranges, the computer changes the mode control bit to the measurement mode. In this mode, the operating frequency of narrow-band detecting circuits is placed under control of the computer. The computer sets the initial operating frequency by shifting a command word from the storage buffer register into the transfer register in the EIP, and then transferring this command word into the command memory module.

Each measurement made by the narrow-band detecting circuits in the experiment appears in the form of a 16-bit data word at the parallel input gates. This word is loaded into the transfer register by means of the trigger logic module monostable pulses, and is subsequently shifted into the computer storage buffer register when the computer executes an XMIA instruction. This serial shifting simultaneously places a new command word in the transfer register. The execute pulses following the 16 clock pulses transfer this command word into the command memory module to set the experiment operating frequency for the next measurement. Input-output operation for the measurement mode continues until the computer program restores the experiment to the survey mode.

To minimize power drain in the EIP, a computer-controlled power supply switch turns off power to the transfer register and parallel data input gates except during an input-output information exchange between the computer and the experiment.

Summary of EIP Characteristics: Table 1 compares the salient features of the 4 EIP's. There are no great differences in dimensions, mass, or number of parts. The operating and standby power drains are a reflection of the requirements of the various experiments and of the importance attached to power saving by the various experimenters. Notice that placing the EIP's in the experiments reduces the number of wires which must run through the wiring harness from the experiments to the computer from 66 to 25.

Table 1
EIP Characteristics

| | U. Cal. | U. Chic. | GSFC | U. Minn. |
|---|---|---|---|---|
| Dimensions: (inches) | | | | |
| L | 4.000 | 4.000 | 4.000 | 4.000 |
| W | 4.125 | 3.407 | 3.700 | 2.775 |
| H | .987 | .987 | .987 | .987 |
| Approx. Mass (grams) | 135 | 116 | 128 | 100 |
| Number of IC's | 68 | 59 | 66 | 50 |
| Discrete Parts: | | | | |
| R | 0 | 6 | 6 | 2 |
| C | 2 | 3 | 3 | 2 |
| Transistor | 0 | 4 | 4 | 2 |
| Power Drain: (milliwatts) | | | | |
| Standby | 263 | 89 | 115 | 0 |
| Operating | 263 | 204 | 230 | 156 |
| Number of Wires: | | | | |
| EIP to Exp. | 11 | 9 | 15 | 31 |
| EIP to SDP-3 | 6 | 6 | 6 | 7 |

There are also other advantages in placing the EIP's in the experiments. The EIP to SDP-3 interfaces are nearly identical. This will facilitate experiment interchangeability in future spacecraft. Furthermore, it is the responsibility of the experimenter to assure himself that the experiment to EIP interface operates properly. We know a-priori that the EIP and the SDP-3 are compatible. Therefore when a number of experiments are mated with the SDP-3 we can at least expect a minimum of hardware interface difficulties. In addition the weight, volume, and power dissipation of the various EIP's are charged to the experiments which they service. This is only fair in view of the EIP's function.

## VARIABLE DATA FORMAT

It is necessary to use a variable data format in order to fully realize the potential of a computerized data system. The variable format allows data from a temporarily very active experiment to replace data from a temporarily inactive experiment. It allows data which was stored

during periods of intense experiment activity to be transmitted later during quiescent periods. In short, the variable data format extends the flexibility provided by a stored-program computer into one more facet of the data system.

Structure of a Frame:

Data from the SDP-3, no matter where in the standard telemetry format it may be assigned, is stripped out of the other data and all strung together into one continuous bit stream. This bit stream is what would be received if the SDP-3 were driving the modulator and transmitter directly. The format of this data is determined by the SDP-3 software. We have chosen to make the frame length a constant 2048 bits (exactly half a page of memory). The first 32 bits of each frame are a frame sync pattern. Figure 5 shows how from 16 to 254 variable-length messages are packed into each frame.

Structure of a Message:

Each message consists of from 1 to 16 16-bit words. The first 4 bits of a message are identification indicating that the message is from one of 15 sources or is fill. The second 4 bits of a message are a word count which specifies the total number of words in the message. The remainder of the message is data from the specified source. The percentage of non-data bits in a message varies from 50% for one-word messages to 3% for 16-word messages. Relatively long messages will be used whenever it is feasible.

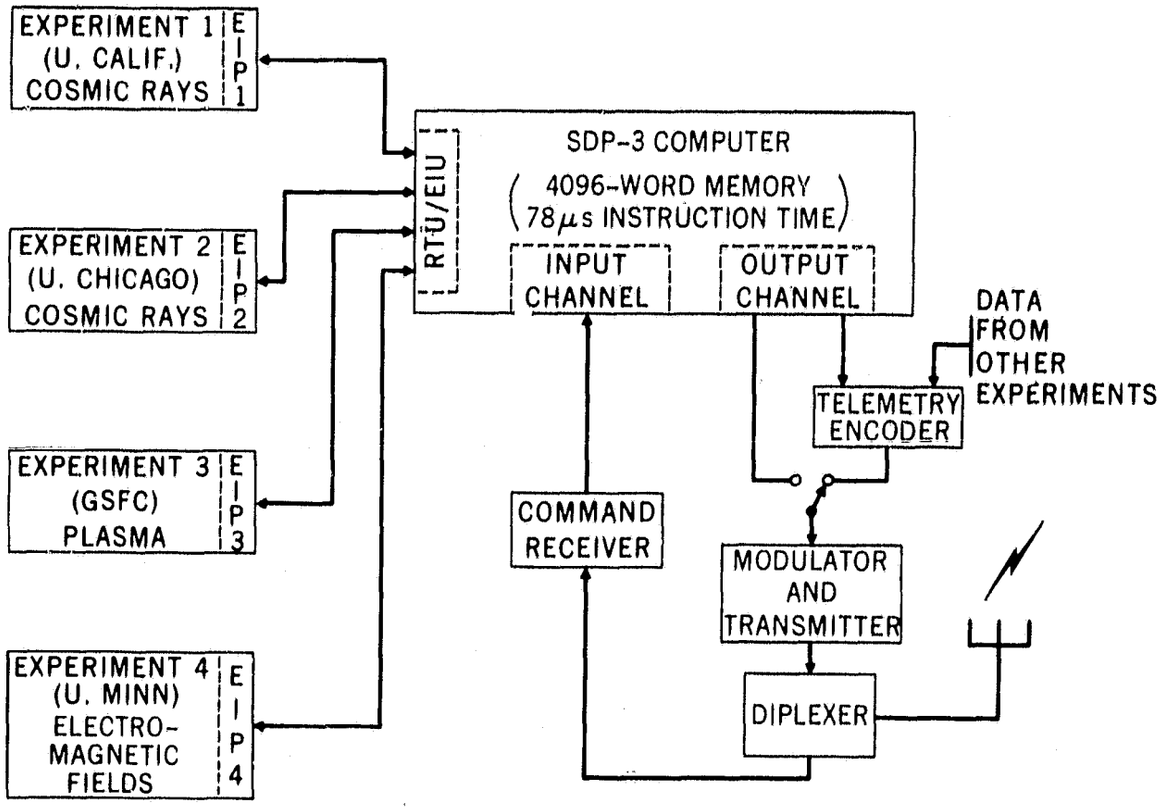



Figure 1. The IMP-I Computer Experiment

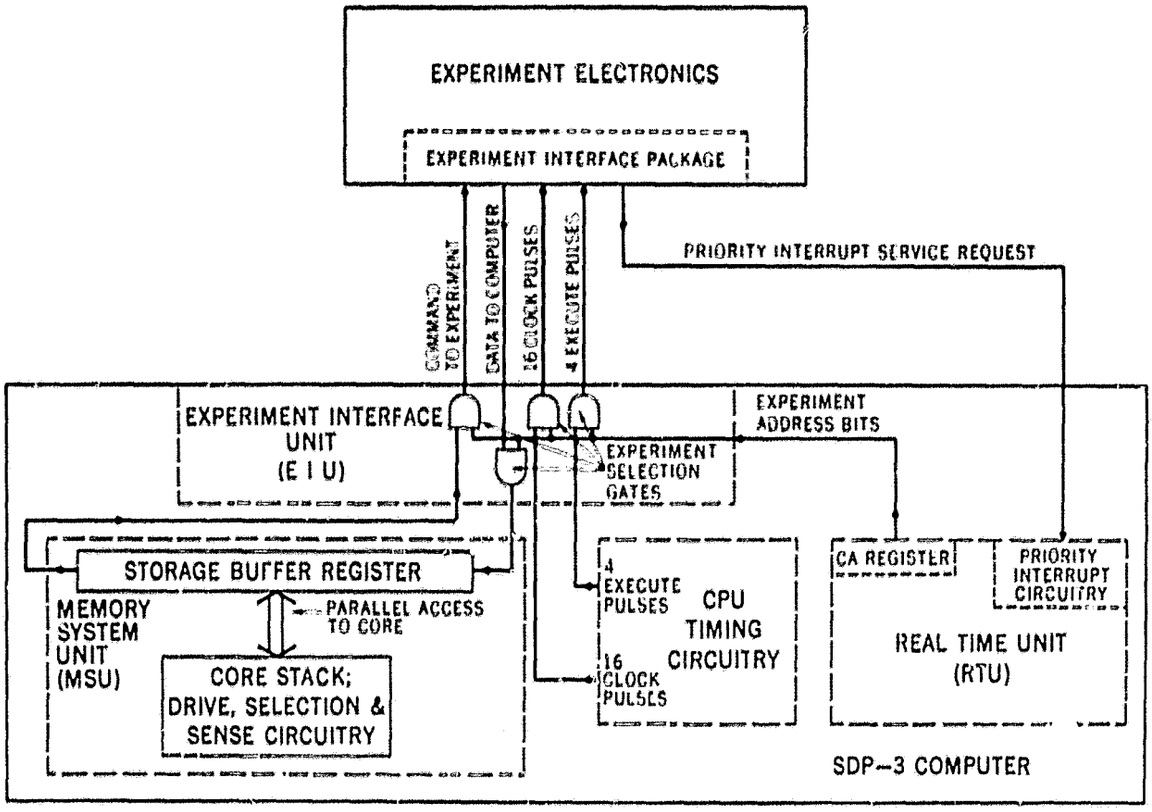



Figure 2. SDP-3 Computer Showing Typical Interface with Experiment Electronics

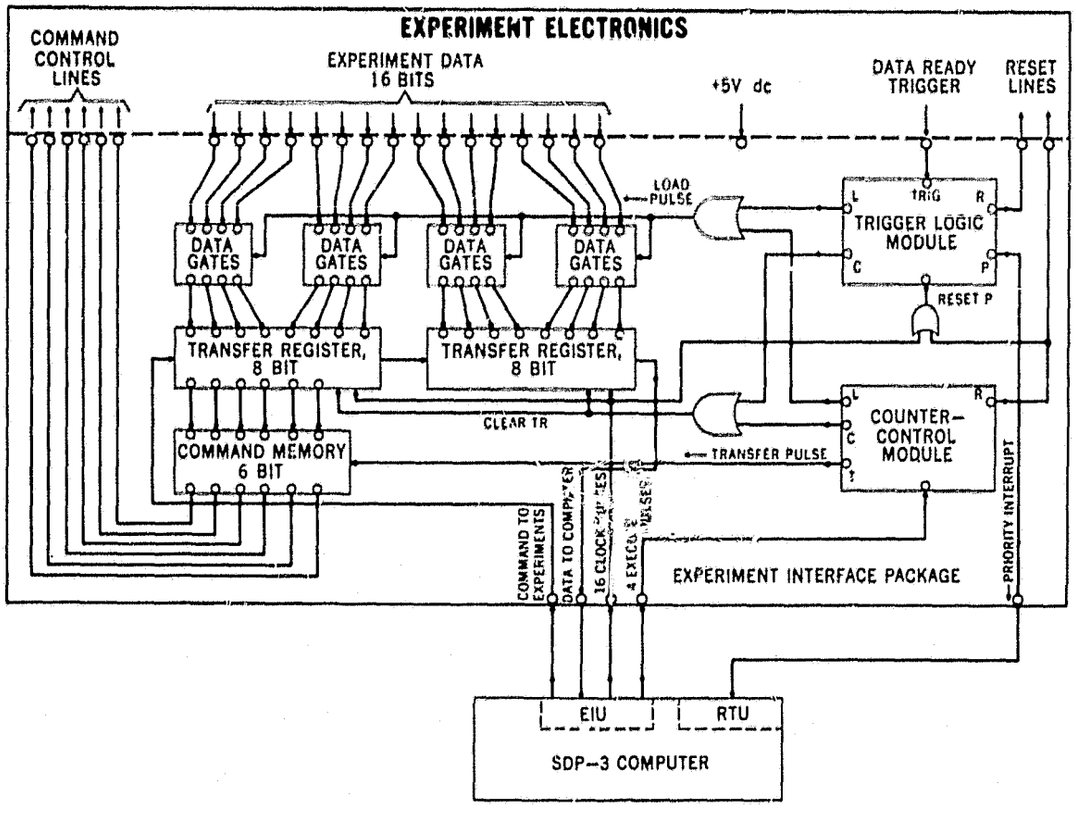



Figure 3. Typical Experiment Interface Package

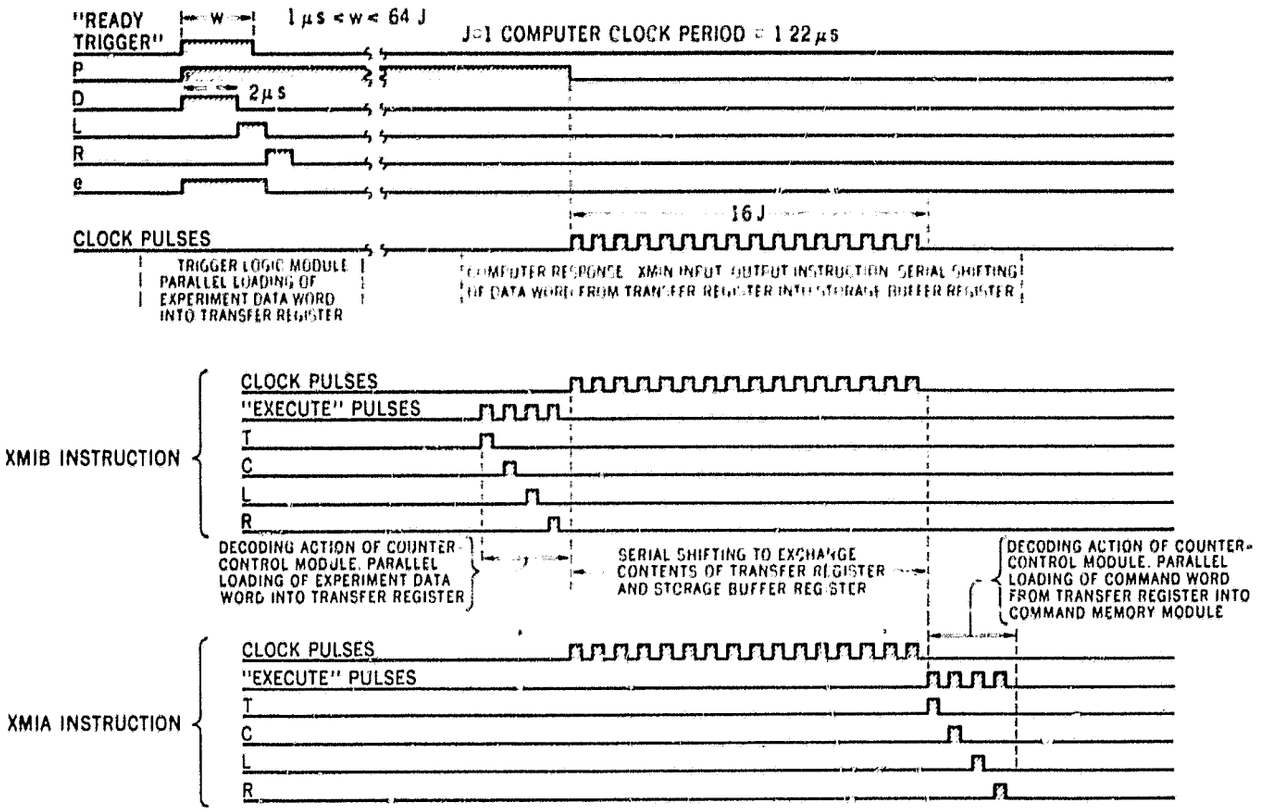
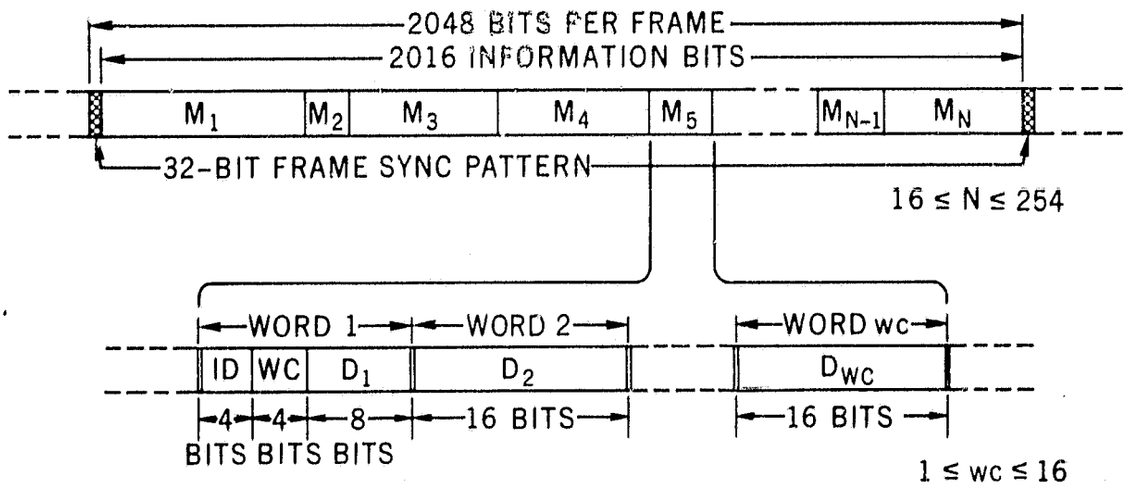



Figure 4. Timing Diagram for Information Exchange Between SDP-3 Computer and Experiments




| ID | MESSAGE TYPE |
|---|---|
| 0 | FILL |
| 1 | EXPERIMENT 1 (U. CALIF.) |
| 2 | " 2 (U. CHICAGO) |
| 3 | " 3 (GSFC) |
| 4 | " 4 (U. MINN.) |
| ⋮ | ⋮ |
| 14 | COMPUTER EXPERIMENT |
| 15 | REAL-TIME DECOM. AND PRINTOUT |

Figure 5. Variable Format for Data Transmission