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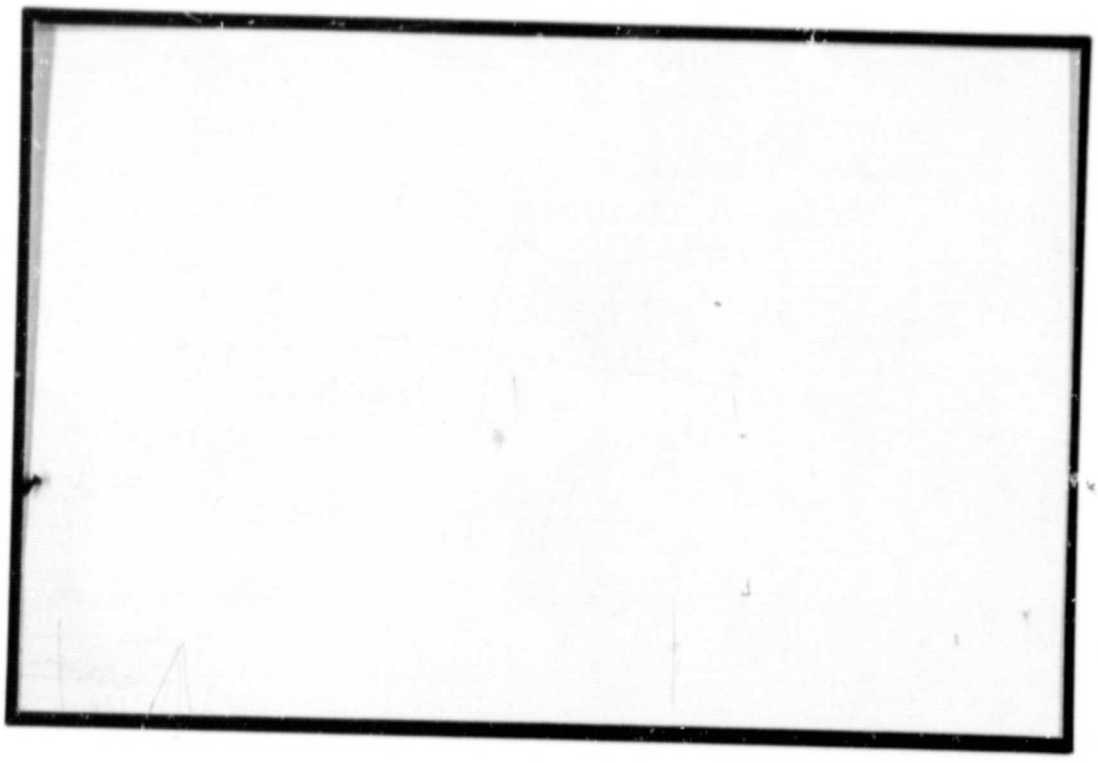

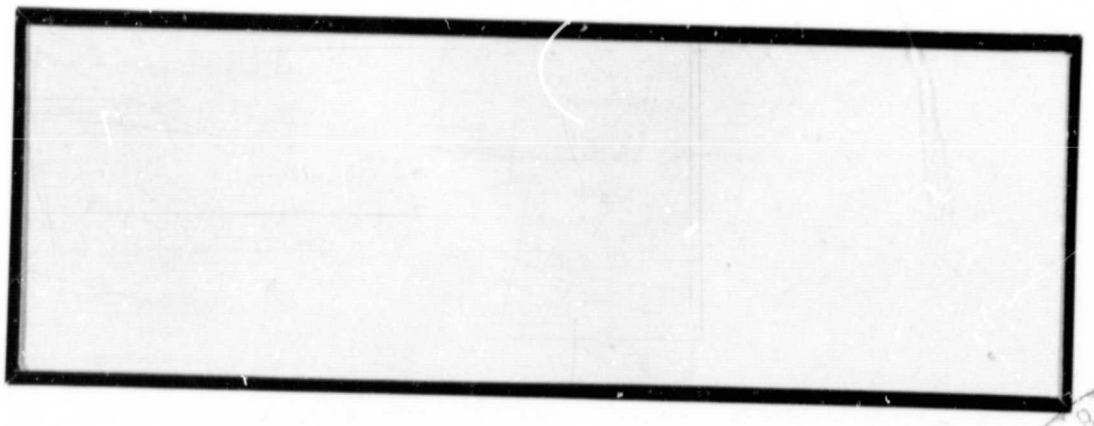

ENGINEERING EXPERIMENT STATION

A

A CLASS-D, D-C AMPLIFIER WITH ISOLATED OUTPUT

Prepared by

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FOREWORD

This is a technical report of a study conducted by the Electrical Engineering Department, Auburn University, toward fulfillment of Contract NAS8-11344. This report represents a summary of the research conducted to date on the use of transformer-coupled output circuits in class-D amplifiers.

ABSTRACT

This report is concerned with the development and design of a transformer-coupled output circuit for use with a class-D amplifier. With the transformer-coupled output circuit, both a-c and bipolar d-c output signals may be produced. The output circuit requires but a single d-c power source.

The theory of class-D amplification is presented. The mode of operation of class-D amplifiers which have been previously developed is explained. The significant advantages and disadvantages of this type of amplifier are discussed. It is shown that the use of a transformer-coupled output circuit presents certain advantages for class-D amplification.

The theory describing the operation of the transformer-coupled output circuit is presented. The design equations for the output-circuit transformer are developed for the general case. Equations yielding the maximum values of certain circuit parameters are also developed to serve as criteria in component selection. Factors to be considered in the selection of a core for the output-circuit transformer are also discussed.

An experimental, transformer-coupled output circuit was designed and constructed. The circuit was operated with a pulse-width modulator and driver circuit to form a class-D amplifier. Several tests were made

of both the a-c and d-c performance of the amplifier. The results of the tests are presented.

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A CLASS-D, D-C AMPLIFIER WITH ISOLATED OUTPUT

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I. INTRODUCTION

Class-D amplification is a broad term which may be used to describe methods of amplification which utilize switching-mode techniques. In simplest terms, the process of class-D amplification is a four-step sequence of events: (1) the input signal is sampled; (2) the information obtained is made to modulate a pulse signal; (3) the modulated pulse signal is amplified using switching-mode techniques; and, (4) the amplified pulses are demodulated to recover the information contained in the input signal.

The principal advantage of class-D amplification is the high efficiency which may be attained. In previous studies for example, class-D, d-c amplifiers have been designed and tested which were 80% to 90% efficient up to several hundred watts power output. Since the active devices in the power stages are operated in the saturated mode, thermal drift is insignificant. Saturated operation also makes it possible to reduce quiescent power consumption to levels as low as one-quarter watt.[1]

The principal disadvantage of the class-D amplifier is the complexity of the circuit required. Also some distortion is introduced by the modulation and demodulation of the pulse signal. Both negative feedback

and filtering techniques may be used to reduce distortion, when proper care is taken to assure stability.

A block diagram of a pulse-width-modulated, class-D, d-c amplifier, using negative feedback, is shown in Figure 1. In the input stage, an input signal is compared with the feedback signal. The resulting error signal is amplified to provide a control voltage, which is applied to the modulator. A positive control voltage causes the "P" channel to produce a negative output voltage, while the "N" channel responds to a negative control voltage and produces a positive output voltage. Such an arrangement makes it possible to amplify an a-c input signal, as well as a bipolar d-c input signal (a d-c signal of either polarity).

The pulse-width modulator produces a train of constant-amplitude pulses with width proportional to the magnitude of the control voltage. The pulses occur at a fixed rate, the switching frequency. The pulse-width-modulated signal is amplified in the driver and applied to the output stage. Each channel of the output stage is essentially a power switch which connects a power supply to the filter for the duration of each pulse. The filter demodulates the pulse signal, providing an analog output signal.

Although output circuits which operate in a somewhat similar manner have been used to obtain the high efficiencies referred to earlier, they possess several disadvantages. An obvious disadvantage is the need for two separate power supplies as shown in Figure 1. Furthermore, each power supply must be able to supply the maximum power requirement at full output. It may also be noted that, due to the direct-coupled nature of the circuit, the maximum output voltage cannot be greater than the supply voltage.

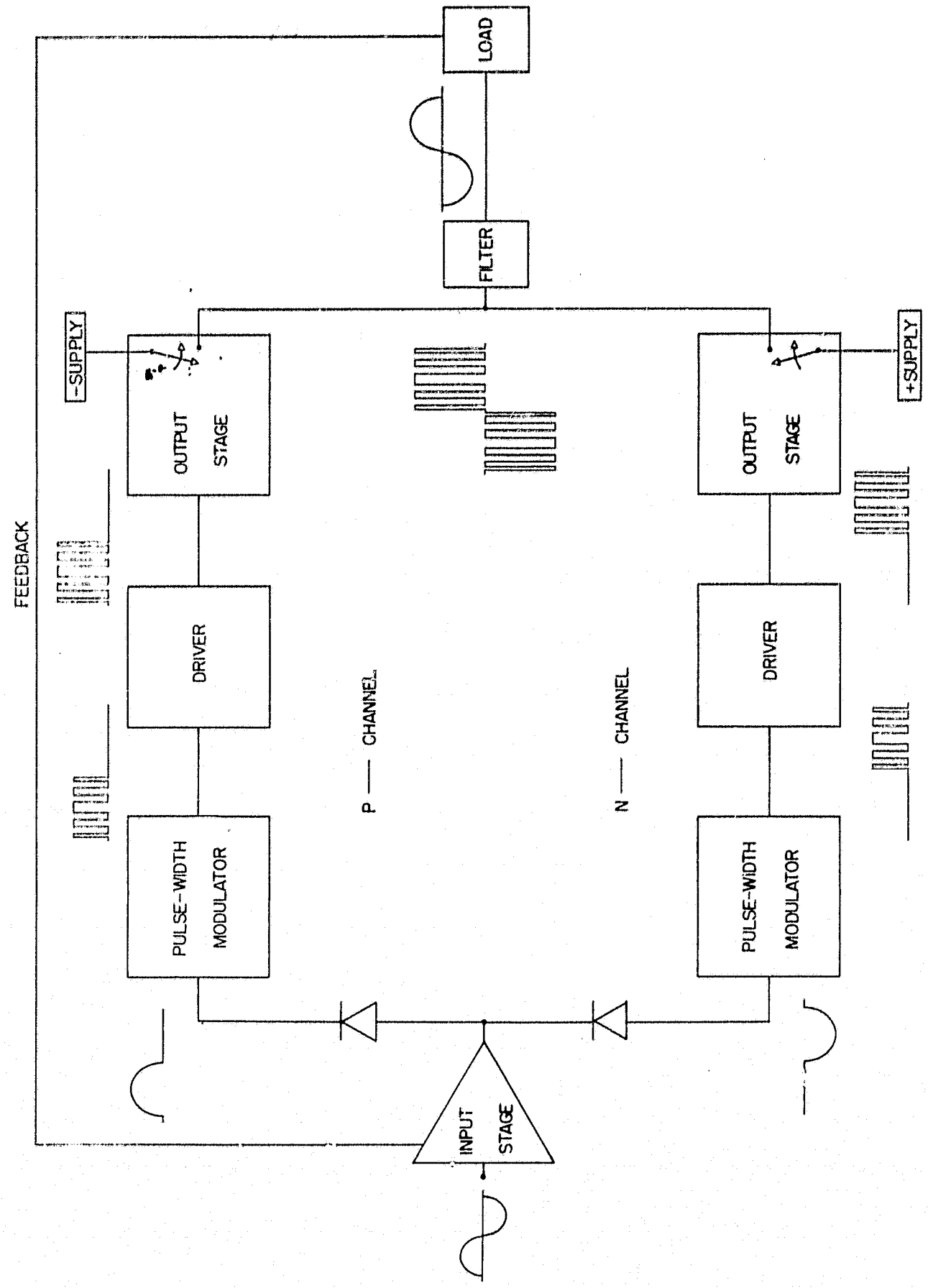


Fig. 1.--A block diagram of a pulse-width-modulated, class-D, d-c amplifier.

In order to avert these disadvantages, a transformer-coupled output circuit was developed for use in class-D amplifiers. This research is concerned with the design of such a circuit. Particular attention is paid to the design of the output-circuit transformers.

II. GENERAL DESIGN CONSIDERATIONS

The schematic diagram of the transformer-coupled output circuit is shown in Figure 2. The circuit is divided into two almost identical circuits, the N-channel and the P-channel. In the complete amplifier, the P-channel responds to positive inputs and produces negative output voltages, while the N-channel responds to negative inputs and produces positive output voltages. Since the two channels are similar, only the N-channel will be discussed in detail. All results are equally applicable to both channels.

The circuit of Figure 2 functions in the following manner. Assume that the N-channel is operating, that the pulse-width-modulated driving signal (a train of constant-amplitude, positive pulses) has remained unchanged for several cycles, and that the time constant of the filter capacitor, C_{41}, and load, R_L, is large enough that the output voltage, e_o, approximates some positive, d-c level. The waveforms associated with the operation of the circuit are shown in Figure 3. At $t = 0$, a pulse from the driver drives Q_{42}, one of the output transistors, into saturation. Since the voltage drop across Q_{42} is now quite small, almost the entire supply voltage is applied across the primary (P) of T_{42}. The connection of diode D_{42} and the phasing of the transformer secondary (S) is such that current will not flow in the secondary while Q_{42} remains saturated and current flows in the primary. During this time Q_{44}, one of the clamping transistors, is reverse-biased by

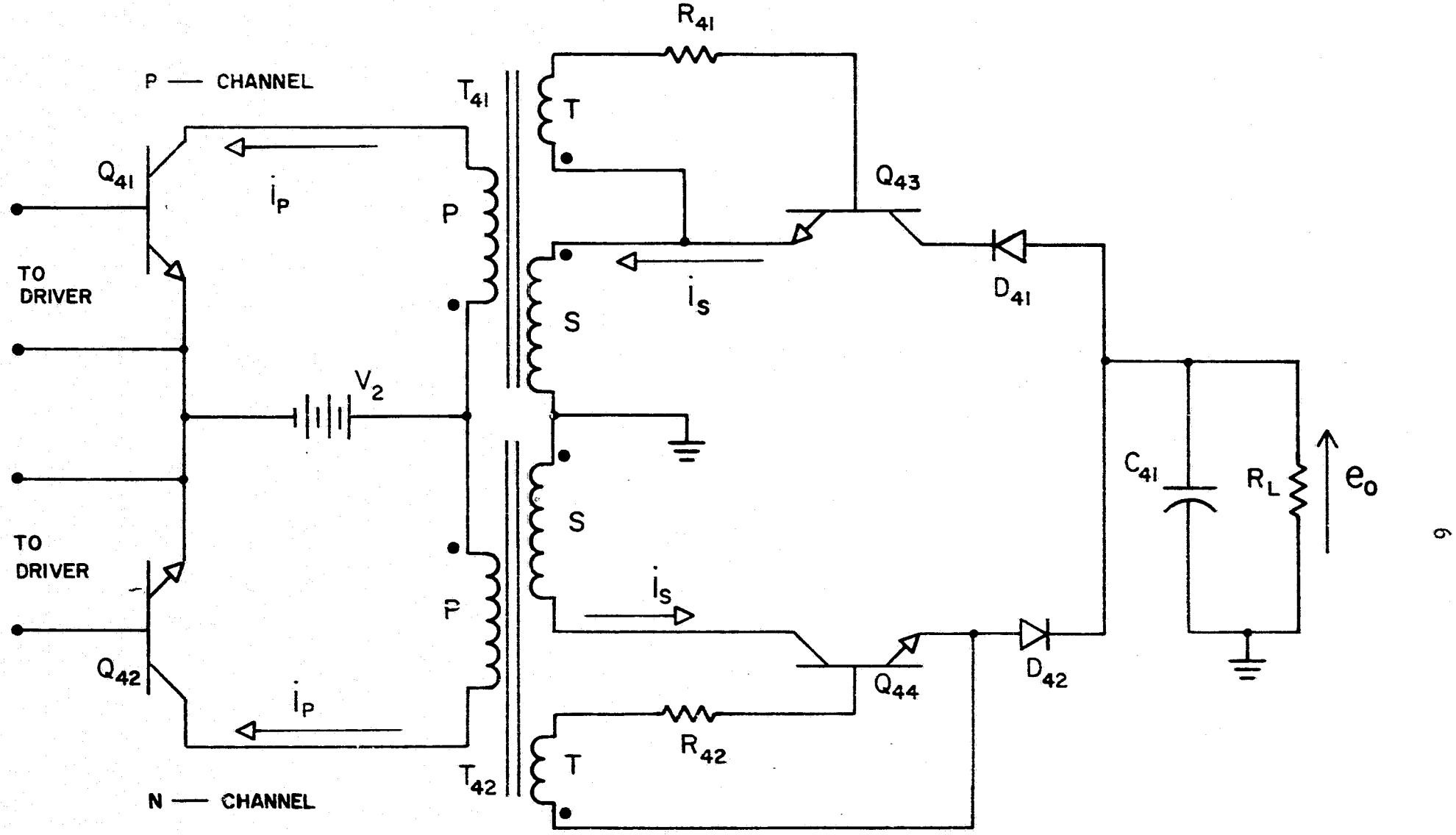
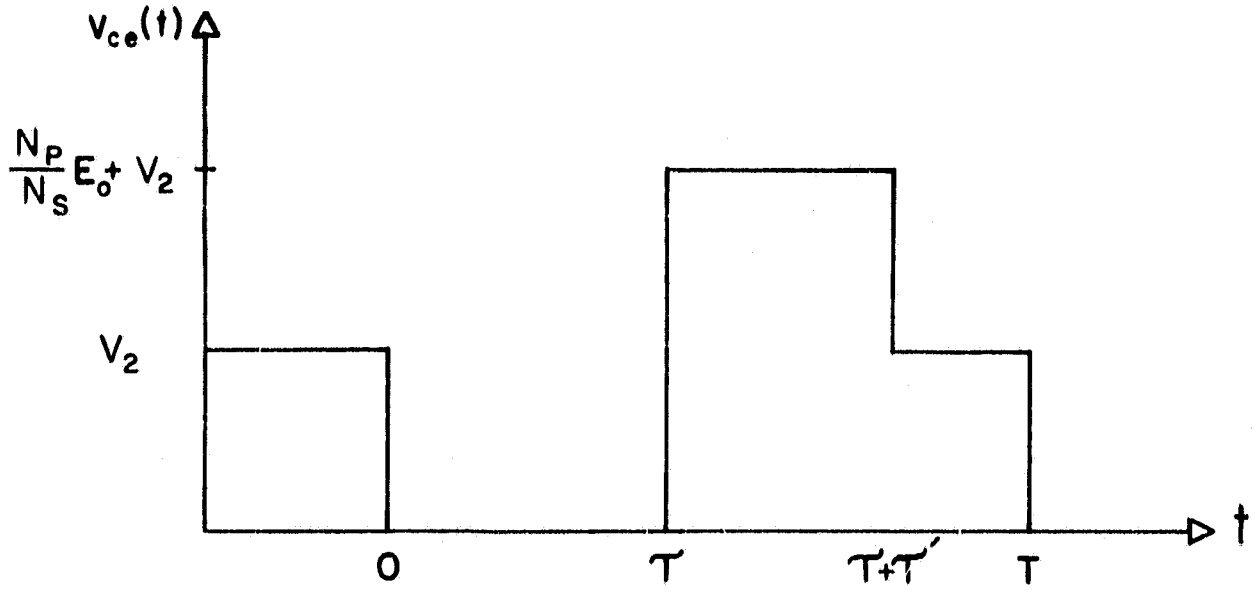
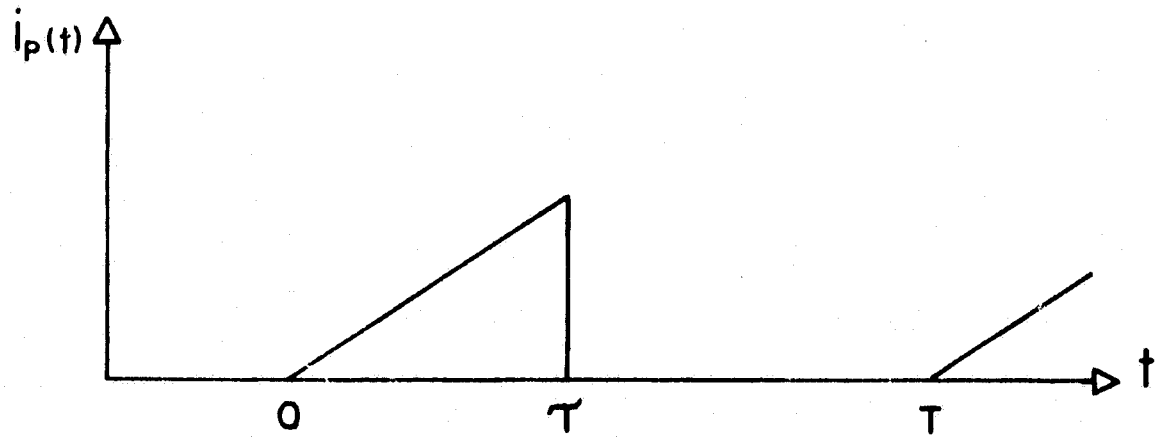


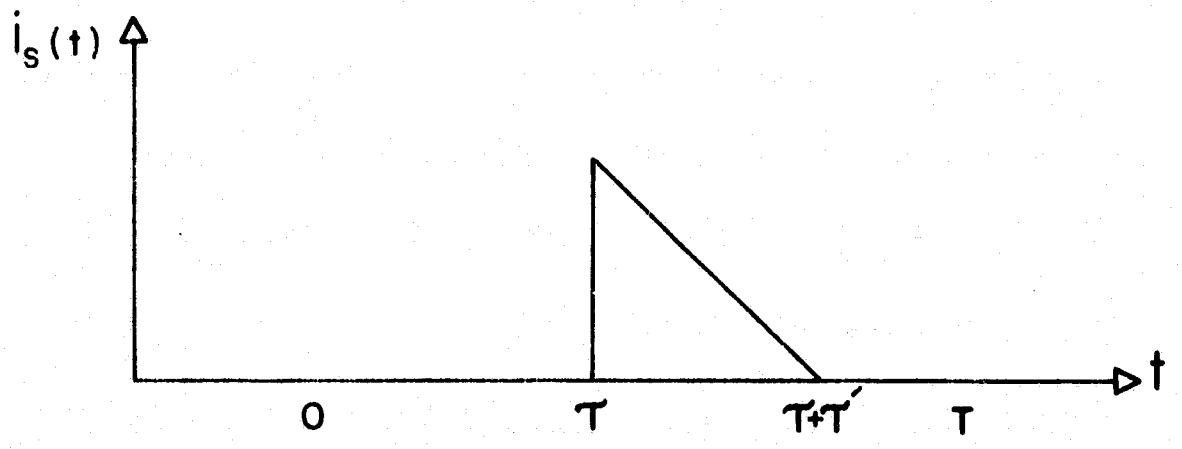
Fig. 2.--Schematic diagram of the transformer-coupled output circuit.



(a)



(b)



(c)

Fig. 3.--Waveforms associated with the output circuit: (a) the collector-emitter voltage of the output transistor; (b) the primary current; and (c) the secondary current.

the voltage of the tertiary winding (T). Assuming that the current in all of the transformer windings is initially zero, the primary current waveform describes a ramp as shown in Figure 3(b). As current flows in the primary winding, energy is stored in the core of the transformer, as current flow may not occur at this time in either the secondary or tertiary winding

At $t = \tau$, Q_{42} is driven to cut-off by the driver signal. As current flow ceases in Q_{42}, the voltage across the primary reverses polarity in response to the change in current. At the same moment, the secondary and tertiary winding voltage polarities also reverse, driving Q_{44} on and forward-biasing D_{42}. As the magnetic field begins to collapse, current flows in the secondary, removing the stored energy from the core of T_{42}. The secondary current waveform is a ramp of negative slope, as shown in Figure 3(c).

During this sequence of events, the role of Q_{43}, the other clamping transistor, is to prevent the positive output voltage from being short-circuited by D_{41} and the secondary of T_{41}. If an output voltage of only one polarity is desired, then just one channel of the output circuit is required, and the tertiary winding and the clamping transistor may be omitted.

A somewhat different mode of operation is also possible if the current waveforms become trapezoidal in shape. This mode of operation is explained and discussed in Appendix A.

The design of the output-circuit transformer will now be considered. In order to simplify the development of the design equations, certain assumptions will be made. First, all the losses in the circuit will be

taken into account by assuming an output circuit efficiency, η_o. Therefore, voltage drops, such as the saturation value of v_{ce} and the forward-biased diode voltage, and energy losses, such as those associated with leakage inductance and core losses, will not be considered separately. Second, it will be assumed that the driver pulses have been of constant width for several cycles, and that the time constant of the filter capacitor and load is sufficiently large for the output voltage to approximate a d-c level, E_o. Third, since it is desired that the current waveforms be ramp functions, the currents in the transformer windings are assumed to be zero at the beginning of each cycle. A simplified schematic diagram of the N-channel of the output circuit is shown in Figure 4. Note that the tertiary winding and the associated transistor, Q_{44}, have been omitted for clarity.

When transistor Q_{42} is driven into saturation, the power supply, V_2, is essentially connected across the primary inductance, L_p, of the transformer. For zero initial conditions, the primary current is given by

$$i_p(t) = \frac{1}{L_p} \int_0^t V_2 \, dt \tag{1}$$

which, for the duration of the primary pulse, becomes

$$i_p(t) = \frac{V_2 t}{L_p} \quad 0 \leq t \leq \tau. \tag{2}$$

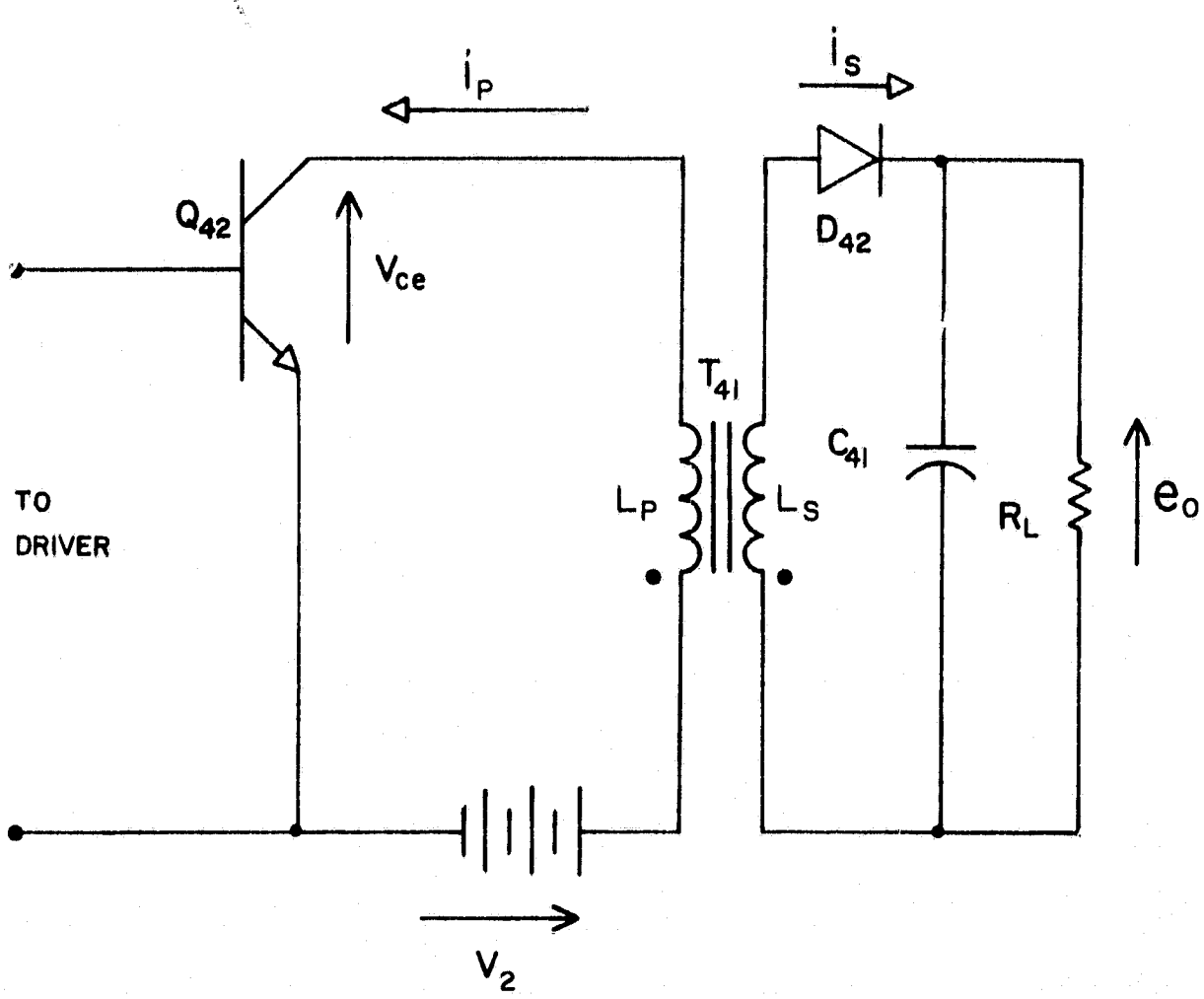


Fig. 4.--Simplified schematic diagram of the N-channel of the output circuit.

The time-averaged power input, P_2, is given by

$$P_2 = \frac{1}{T} \int_0^{\tau} V_2 \, i_p(t) \, dt \qquad (3)$$

where T is the period of the pulse-width modulated driving signal. The substitution of $i_p(t)$ from (2) in (3), yields the following solution for the primary inductance

$$L_p = \frac{(V_2 \, \tau)^2}{2 \, T \, P_2} \, . \qquad (4)$$

A similar development gives the required value of the secondary inductance as

$$L_S = \frac{(E_o \, \tau')^2}{2 \, T \, P_o} \qquad (5)$$

where τ' is the duration of the ramp of current in the secondary (the secondary current pulse-width, as shown in Figure 3(c)), and P_o is the required power output. The power output is related to the power input by the output-circuit efficiency as

$$P_o = \eta_o \, P_2 \qquad (6)$$

There are several criteria associated with the selection of some of the parameters in (4) and (5). The inverse of the period T, is the switching frequency, f_S. It has been shown that the switching

frequency should be at least five times the desired upper cutoff frequency of the amplifier in order that the distortion components, due to intermodulation between the signal and switching frequencies, will not have an amplitude which is greater than one per cent of the output signal.[2] Furthermore, a high switching frequency minimizes the size and weight of the driver transformers and simplifies the design and implementation of the output filter. However, switching losses in the output transistors may be expected to increase as the switching frequency is increased. Core losses may be reduced slightly by selecting a switching frequency which coincides with the peak in Q for the core selected for the output-circuit transformer. The procedure by which the switching frequency was selected for an experimental circuit is presented in Chapter III.

From a theoretical standpoint, the selection of τ and τ' is arbitrary. However, it is shown in Appendix B that power loss, due to the magnitude of the current peaks, may be minimized by selecting appropriate values for τ and τ' at maximum power output. These values are given by

$$\max \tau = T \left[\frac{\max E_o}{\max E_o + \eta_o V_2} \right] \tag{8}$$

and $$\max \tau' = T - \max \tau, \tag{9}$$

where $\max E_o$ is the maximum value of required output voltage.

The results of (8) and (9) apply at maximum power output. Therefore, when (8) and (9) are used in conjunction with (4), (5), and (6) in designing a transformer, the maximum values of output voltage, E_o,

power output, P_o, and power input, P_2, should be used.

The core material selected for the transformer should exhibit relatively low losses at the switching frequency. The selected core should give linear operation up to the predicted maximum level of magnetic field intensity. This maximum, in oersteds, is given by

$$\max H = \frac{0.4\,\pi\, N_p \max i_p}{m\ell} \tag{10}$$

where N_p is the number of turns in the primary, $m\ell$ is the mean magnetic path length in centimeters, and

$$\max i_p = \frac{V_2 \max \tau}{L_p} \tag{11}$$

is the maximum value of peak primary current. A similar calculation could also be made for the secondary but should yield approximately the same value for max H. If the maximum level of magnetic field intensity is too high, the permeability of the core will be reduced at peak current levels, resulting in non-linear operation. The value of magnetic field intensity at which the operation of the core becomes non-linear may be determined from data supplied by the manufacturer.

A schematic diagram of the complete N-channel of the output circuit is shown in Figure 5. The base drive circuit for Q_{44} must be designed such that power loss in Q_{44} is minimized.

The base drive circuit must be capable of driving Q_{44} into saturation for the largest peak value of current in the secondary, which is,

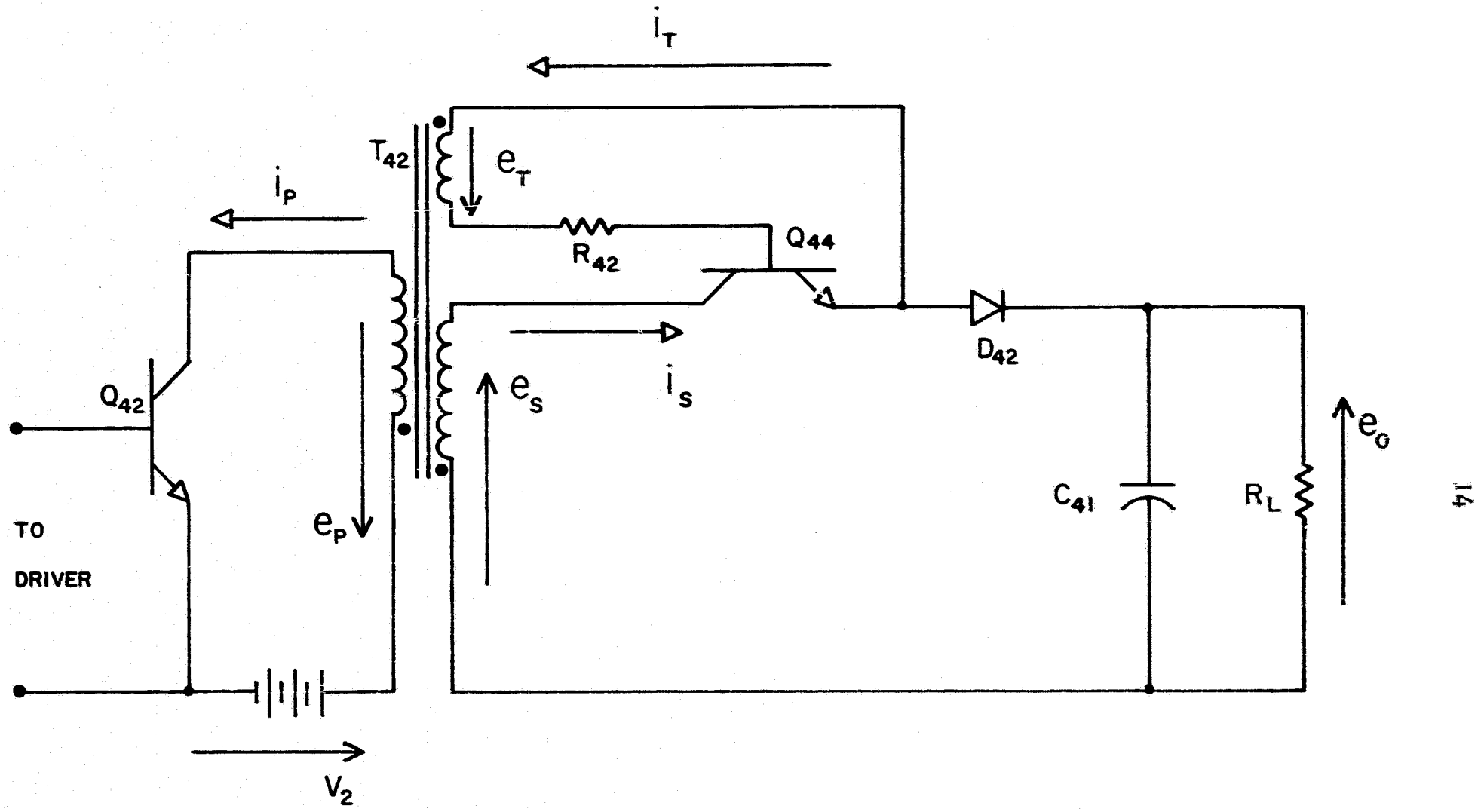


Fig. 5.--Schematic diagram of the N-channel of the output circuit.

$$\max i_S = \frac{(\max E_o)\ (\max \tau')}{L_S} \tag{12}$$

where max τ' is the largest value of τ'. When the required saturation values of base current, i_T, and base-emitter voltage, v_{be}, for Q_{44} have been determined at max i_S, the relationship between R_{42} and N_T, the turns in the tertiary winding, may be found from

$$R_{42}\ i_T + v_{be} = \frac{N_T}{N_S}\ (\max E_o) \tag{13}$$

where N_S is the number of turns in the secondary winding.

As the output voltage is decreased, the tertiary winding voltage e_T approaches the minimum value required to forward-bias Q_{44}. Typically this minimum value of e_T is approximately 0.6 volt. The value of e_o which results in this minimum value of e_T is approximately equal to e_S, the secondary winding voltage, and this value of e_S is given by

$$e_S = 0.6\ \frac{N_S}{N_T}\ . \tag{14}$$

When e_o becomes less than the value given in (14) for e_S, Q_{44} can no longer be driven to saturation. Therefore, the collector-emitter voltage, v_{ce}, of Q_{44} will increase until the sum of v_{ce} and e_o equals the value of e_S given by (14).

Since there will be increased power loss in Q_{44} when it is not operated in saturation, it is desirable that Q_{44} operate in the saturated mode to a relatively low value of output voltage. This is accomplished

by making N_T larger. However, a larger value of N_T results in a larger value of R_{42} in equation (13). As R_{42} is made larger, the power loss in it may become significant for high levels of base current. These considerations should be taken into account when a value of $e_o \approx e_S$ is chosen for use in (14) to determine N_T. With N_T determined from (14), R_{42} may then be determined by using (13).

A foreknowledge of certain maximum voltages and currents is required for the selection of circuit components. As before, only the N-channel, shown in Figure 5, will be discussed, since the results are applicable to both channels.

The maximum reverse value of v_{ce} for Q_{42} occurs when current is flowing in the secondary, and is

$$\text{max rev } v_{ce} = V_2 + (\text{max } E_o) \quad \frac{N_P}{N_S} \; . \tag{15}$$

The maximum value of peak collector current in Q_{42} is given by (11), as max i_p.

The maximum value of reverse voltage from the collector of Q_{44} to the cathode of D_{42} occurs when current is flowing in the primary and is

$$\text{max rev } v_{cc} = \frac{N_S}{N_P} \; V_2 + \text{max } E_o \; . \tag{16}$$

The maximum value of peak current in Q_{44} and D_{42} is given by (12) as max i_S. The maximum reverse value of base-emitter voltage for Q_{44} is

$$\text{max rev } v_{be} = \frac{N_T}{N_P} \; V_2 \; . \tag{17}$$

This equation also places an upper limit on the value of N_T.

III. DESIGN AND TESTS

An experimental transformer-coupled output circuit was designed according to the design considerations set forth in Chapter II. The design specifications for the output circuit were: a maximum d-c power output of 80 watts; a 20-ohm load; a single, 28-volt d-c power supply; and a bandwidth from d.c. to 1 kHz. The design equations used are summarized in Table 1. The procedure which was used in the design of the output circuit will now be discussed.

Selection of the switching frequency and the core for the output transformers is a dual process based upon the consideration of several factors. If the highest signal frequency is to be 1 kHz., then the switching frequency, f_S, should be greater than 5 kHz. in order to obtain low intermodulation distortion due to the switching frequency.[2] For a trial design, the switching frequency was set at 6 kHz. The intervals τ and τ' were calculated from (8) and (9) in Table 1. Using an assumed output-circuit efficiency, η_o, of 80%, the required primary and secondary inductances were determined using (4), (5), and (6).

Powered-permalloy toroidal cores were selected as the type best suited for the output-circuit transformers, because cores of this type exhibit good coupling, and relatively low losses up to approximately 50 kHz. Among available cores of this type, those with an initial permeability of 60 were chosen for use, because these have the lowest a-c losses at a given frequency and flux density.[3]

TABLE 1

SUMMARY OF DESIGN EQUATIONS FROM CHAPTER II.

$$\max \tau = T \left[\frac{\max E_o}{\max E_o + \eta_o V_2} \right] \tag{8}$$

$$\max \tau' = T - \max \tau \tag{9}$$

$$\max P_2 = \frac{\max P_o}{\eta_o} \tag{6}$$

$$L_P = \frac{(V_2 \max \tau)^2}{2 T \max P_2} \tag{4}$$

$$L_S = \frac{(\max E_o \max \tau')^2}{2 T \max P_o} \tag{5}$$

$$\max i_P = \frac{V_2 \max \tau}{L_P} \tag{11}$$

$$\max H = \frac{0.4 \pi N_P \max i_P}{m\ell} \tag{10}$$

Selecting a satisfactory core size is a trial-and-error process. It was desired to use the smallest core which would be relatively efficient and give linear performance up to the predicted maximum value of magnetic field intensity, max H. According to the manufacturer's data, those cores with an initial permeability of 60 will perform linearly up to approximately 60 oersteds. Therefore, with max i_p determined from (11), values of max H were calculated, using (10), for cores of several different sizes. The smallest core having a value of max H less than 60 oersteds was a core having a cross-sectional area of 2.025 sq. cm. and a mean magnetic path length of 11.13 cm. (Magnetics Inc. catalog number 55439).

In general, the Q of an inductor wound on a particular core will increase with frequency up to a "breakoff" frequency, which depends upon the inductance. Beyond this frequency, the Q will decrease. In preliminary tests it was found that the output circuit was slightly more efficient when the switching frequency coincided with this peak in Q for a particular core. Since the selected core had a maximum Q at approximately 10 kHz., the switching frequency for the final design was increased to 10 kHz.

The design parameters were recalculated using the 10 kHz. switching frequency and the same assumed efficiency of 80%. Table 2 lists the specifications and calculated parameters for the final design of the experimental output circuit. The actual winding inductances of the completed transformers are given in parenthesis, because the calculated inductances could not be obtained with an integral number of turns. A satisfactory size for the tertiary winding was experimentally determined

TABLE 2

SPECIFICATIONS AND PARAMETERS FOR THE EXPERIMENTAL OUTPUT CIRCUIT

Specifications:	
max P_O	80 W
R_L	20 Ω
V_2	28 Vdc.
BW	d-c - 1 kHz.
Parameters:	
η_o	80% (assumed)
f_S	10 kHz
T	100 μS
max τ	64 μS
max τ'	36 μS
max P_2	100 W
L_P	160.5 μH (150 μH)
L_S	130 μH (125 μH)
max i_P	11.15 A.
max H	43.5 Oe.

to be three turns. The maximum values of the significant currents and voltages in the output circuit were calculated using (11), (12), (15), (16), and (17), from Chapter II. On the basis of these calculations, active devices with adequate current and voltage ratings were selected for use in the experimental output circuit. This concludes the design procedure for the output circuit.

The experimental transformer-coupled output circuit was operated using a driver circuit and a pulse-width modulator. Together these formed an open-loop, class-D amplifier. A schematic diagram of the amplifier is shown in Figure 6. A complete parts list is given in Table 3.

The design of the pulse-width modulator and the driver is described in Reference 1. However, a brief description of their operation will be given here. In the modulator, A_{21} functions as an oscillator and generate a triangular waveform across C_{21} at the switching frequency. The triangular waveform is summed with the input signal, which is called the control voltage, e_c. The resulting signal is applied to one input of both A_{22} and A_{23}, which function as comparators. A positive reference voltage is applied to the other input of A_{22}. When e_c causes the peaks of the triangular waveform to exceed this positive reference, a pulse is generated at the output of A_{22}, with a width proportional to e_c. A negative reference voltage is applied to the non-inverting input of A_{23}, and this comparator produces pulses when e_c is negative.

The driver transistors, Q_{31}, are driven into saturation by the pulses from the modulator, producing a driving pulse which is transformer-coupled to the output circuit. Driver transformers are used because

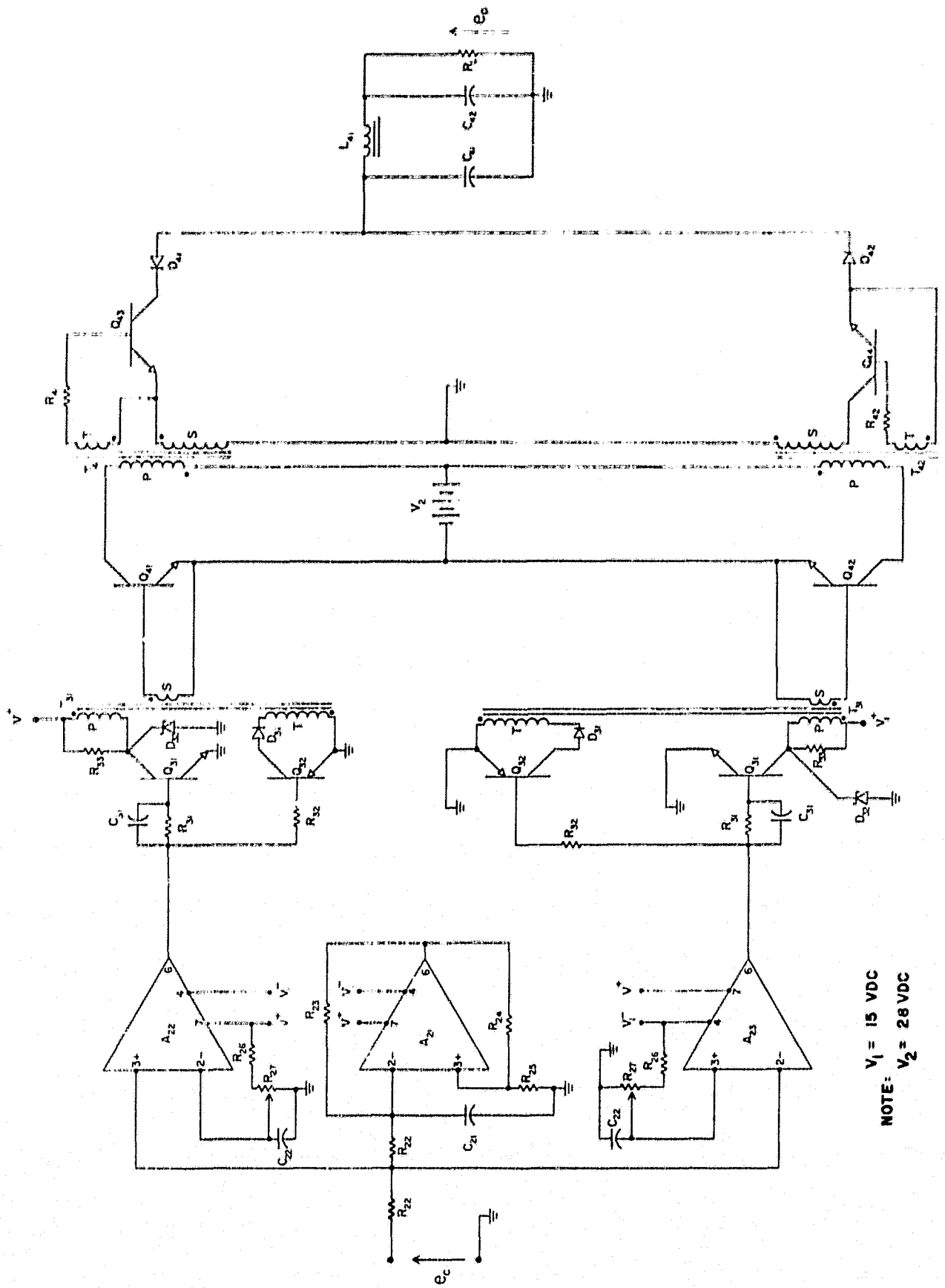


Fig. 6.--A schematic diagram of the experimental class-D, d-c amplifier with a transformer-coupled output circuit.

TABLE 3

CLASS-D AMPLIFIER PARTS LIST

Reference Symbol	Description
A_{21}	Linear integrated circuit, μA709 (Fairchild)
A_{22}	Same as A_{21}
A_{23}	Same as A_{21}
C_{21}	Fixed mica capacitor, 0.005 μF., 100 Vdc.
C_{22}	Fixed ceramic capacitor, 0.0047 μF., 100 Vdc.
C_{31}	Fixed ceramic capacitor, 680 pF., 100 Vdc.
C_{41}	Fixed polycarbonate capacitor, 5.0 μF., 100 Vdc.
C_{42}	Same as C_{41}
D_{31}	Diode, 1N3071
D_{32}	Zener diode, UZ5210 (Unitrode)
D_{41}	Diode, 1N3891
D_{42}	Same as D_{41}
L_{41}	Inductor, 4.0 mH.
Q_{31}	Transistor, 2N4862
Q_{32}	Transistor, 2N3485
Q_{41}	Transistor, 2N2814
Q_{42}	Same as Q_{41}
Q_{43}	Transistor, MHT 8304 (Solitron Devices, Inc.)
Q_{44}	Same as Q_{43}
R_{22}	Fixed resistor, 100kΩ, 5%, 1/4 watt
R_{23}	Fixed resistor, 15kΩ, 5%, 1/4 watt
R_{24}	Fixed resistor, 68kΩ, 5%, 1/4 watt
R_{25}	Fixed resistor, 34kΩ, 5%, 1/4 watt

TABLE 3—Continued

Reference Symbol	Description
R_{26}	Same as R_{22}
R_{27}	Potentiometer, 100kΩ, 5%, 1/4 watt
R_{31}	Fixed resistor, 4700Ω, 5%, 1/4 watt
R_{32}	Fixed resistor, 22kΩ, 5%, 1/4 watt
R_{33}	Fixed resistor, 10kΩ, 5%, 1/4 watt
R_{41}	Fixed resistor, 9.1Ω, 2 watt
R_{42}	Same as R_{41}
R_L	Fixed resistor, 20Ω, 10%, 100 watt
T_{31}	Transformer, core 55206 (Magnetics, Inc.) Primary(P), 818 turns, AWG no. 34 Secondary (S), 106 turns, AWG no. 26 Tertiary (T), 1000 turns, AWG no. 37
T_{41}	Transformer, core 55439 (Magnetics, Inc.) Primary (P), 34 turns, AWG no. 22, 4 windings in parallel Secondary (S), 31 turns, AWG no. 22, 4 windings in parallel Tertiary (T), 3 turns, AWG no. 22
T_{42}	Same as T_{41}

they have been found to improve the switching of the output-circuit transistors, Q_{41} and Q_{42}. Between pulses from the modulator, the "shorting" transistors, Q_{32}, are driven on. When a shorting transistor is on, the respective driver transformer appears as a short circuit to the base and emitter of the associated output transistor. This assures rapid turn-off of the output transistor which is necessary for efficient switching.

In the output circuit, the power supply V_2 is shown "floating", however either terminal may be grounded. It should be noted that a π-section, constant -k, low-pass filter was used at the output in place of the single capacitor shown previously. This filter was designed for a cutoff frequency of 1.6 kHz. In preliminary tests it was found that the π-section filter was more efficient at higher frequencies, and produced less distortion and ripple than the single-capacitor filter.

Several tests were made of both d-c and a-c performance. For d-c output voltages, the output circuit efficiency, output circuit linearity, and per-cent ripple were determined. For a-c output voltages, the output circuit efficiency, the gain, the phase, and the distortion of the test amplifier were determined.

Data was taken to determine the d-c efficiency of both channels of the output circuit. The data and the calculated output-circuit efficiencies are listed in Tables 4 and 5. Both the output voltage and current were measured in order to avoid errors due to changes in load resistance. A graph of the efficiency of each channel of the output circuit is shown in Figure 7. The efficiency of both channels

TABLE 4

DATA AND CALCULATED RESULTS FOR THE D-C EFFICIENCY TEST
OF THE N-CHANNEL

Supply Voltage Vdc	Supply Current Adc	Supply Power Watts	Output Voltage Vdc	Output Current Adc	Output Power Watts	Efficiency %
28.0	0.08	2.24	4.40	0.22	0.97	43.2
28.0	0.12	3.36	6.20	0.31	1.92	57.2
28.0	0.25	7.00	10.0	0.50	5.00	71.4
28.0	0.46	12.9	14.0	0.69	9.67	74.9
28.0	0.92	25.7	20.0	1.01	20.2	78.7
28.0	1.32	36.9	24.0	1.21	29.1	78.7
28.0	1.78	49.8	28.0	1.41	39.5	79.2
28.0	2.28	63.8	32.0	1.60	51.2	80.2
28.0	2.74	76.7	35.0	1.76	61.6	80.3
28.0	3.25	91.0	38.0	1.91	72.6	79.8
28.0	3.62	101.3	40.0	2.00	80.0	79.0

TABLE 5

DATA AND CALCULATED RESULTS FOR THE D-C EFFICIENCY TEST OF THE P-CHANNEL

Supply Voltage Vdc	Supply Current Adc	Supply Power Watts	Output Voltage Vdc	Output Current Adc	Output Power Watts	Efficiency %
28.0	0.07	1.96	-4.4	-0.22	0.97	49.5
28.0	0.10	2.80	-6.2	-0.31	1.92	68.7
28.0	0.23	6.44	-10.0	-0.50	5.00	77.7
28.0	0.44	12.3	-14.0	-0.70	9.80	79 6
28.0	0.92	25.7	-20.0	-1.01	20.2	78.6
28.0	1.33	37.2	-24.0	-1.21	29.1	78.2
28.0	1.78	49.8	-28.0	-1.41	39.5	79.3
28.0	2.29	64.1	-32.0	-1.61	51.6	80.4
28.0	2.73	76.4	-35.0	-1.75	61.3	80.2
28.0	3.23	90.4	-38.0	-1.90	72.2	79.8
28.0	3.61	101.0	-40.0	-2.00	80.0	79.2

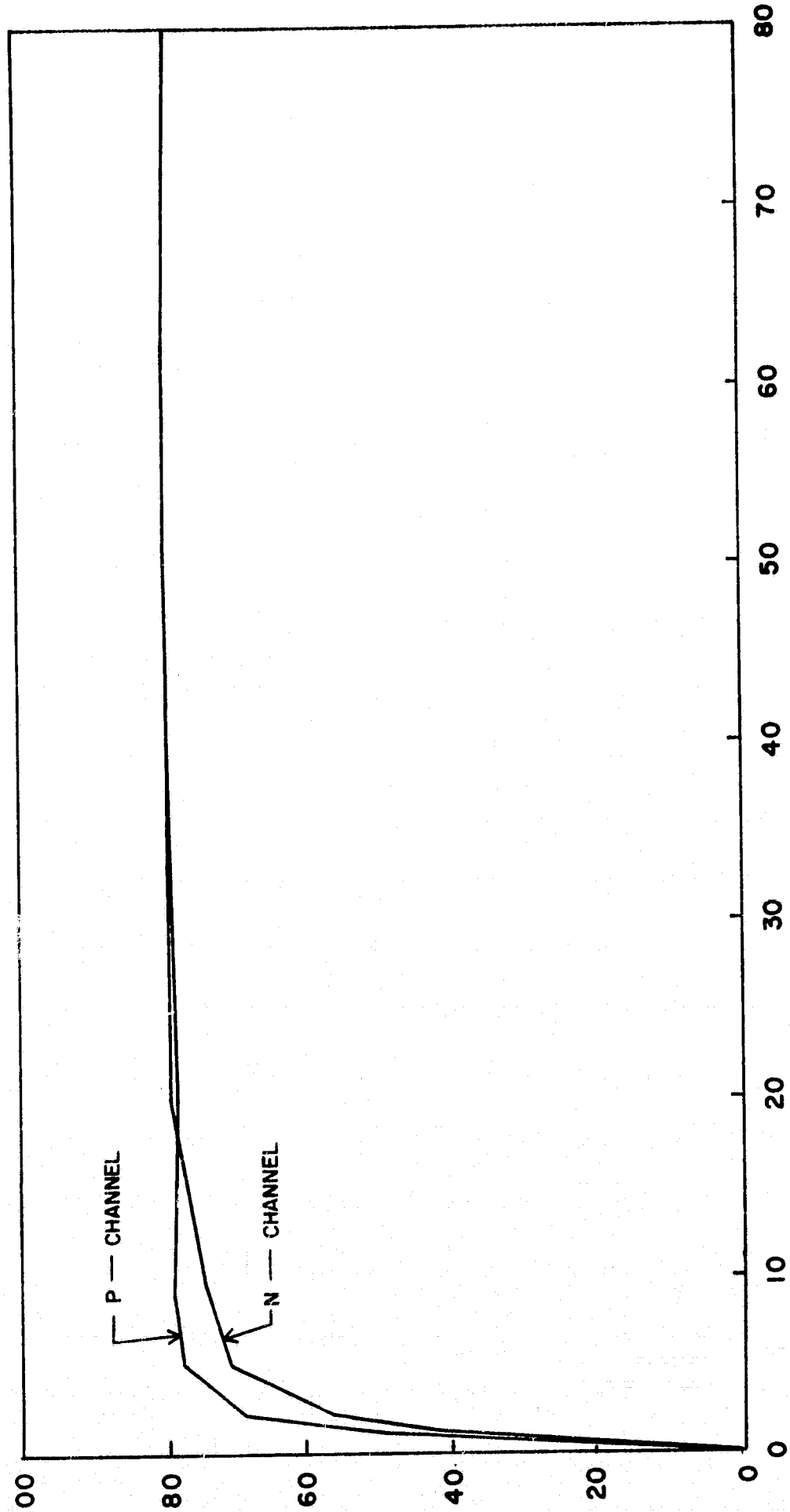


Fig. 7.--A graph showing the efficiency of each channel of the output circuit.

was approximately 80% over most of the output range.

The power consumption of the modulator and driver is not included in the data in Tables 4 and 5. With no signal input, the power consumption of the modulator and driver was approximately 0.6 watts. At 80 watts d-c power output, the power consumption was approximately 1.7 watts.

The data used to determine the linearity and the per-cent output ripple are listed in Table 6. In Figure 8 the d-c output voltage is plotted as a function of the width of the driver pulse-width in order to assess the linearity of the output circuit. A straight line was drawn from the origin to the last data point, for reference. The per-cent ripple is the ratio of the peak-to-peak ripple voltage to output voltage, expressed as a percentage. A graph of the per-cent ripple as a function of output voltage is shown in Figure 9. Since the ripple in both channels was nearly the same, the average value was plotted.

The per-cent distortion in the output signal was measured for several frequencies at six levels of power output. The data for this test is listed in Table 7. In Figure 10 the per-cent distortion is plotted as a function of frequency with power output as a parameter. The almost-uniform increase in distortion from 100 Hz. down to 50 Hz. was due to the signal generator.

The data and calculated results for the a-c efficiency test are listed in Table 8. For 20 watts power output and greater, the data was taken only up to the frequency where distortion approached 6%. The efficiency varied less than 2% over the range of frequencies listed at each power level. The values listed are mean values. It is significant that the a-c efficiency for the output circuit remained almost

TABLE 6

DATA FOR THE D-C LINEARITY AND RIPPLE TESTS

Output Voltage Vdc	N-Channel Driver Pulse-Width µs	N-Channel Output Ripple V-pp	P-Channel Driver Pulse-Width µs	P-Channel Output Ripple V-pp
2	.6	0.03	6	.03
5	9	0.05	9	.05
10	16	0.08	14	.08
15	24	0.14	22	.13
20	32	0.21	31	.20
25	40	0.28	39	.28
30	48	0.42	48	.40
35	56	0.56	56	.56
40	64	0.79	64	.78

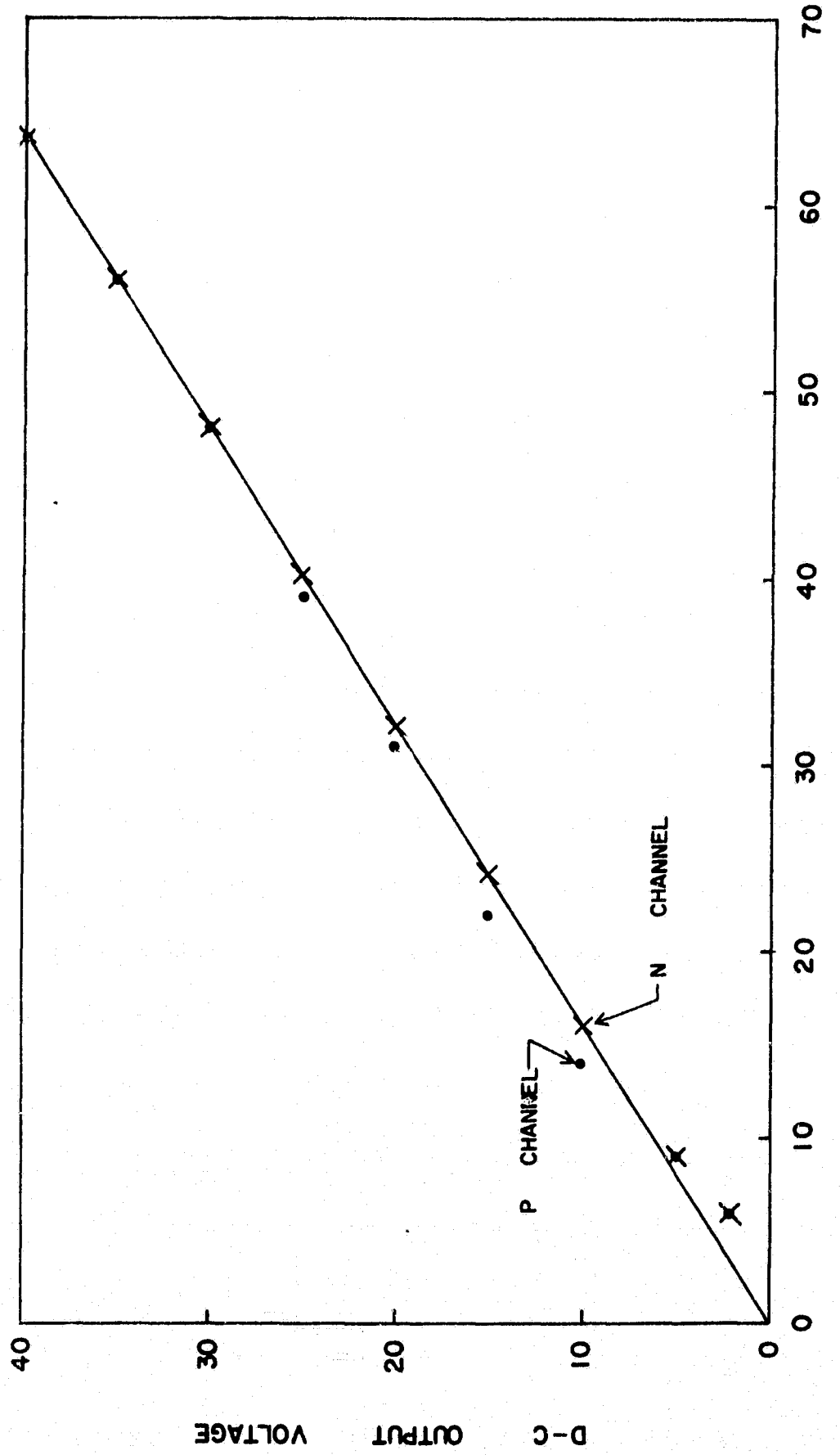


Fig. 8.--A graph showing the linearity of the output circuit.

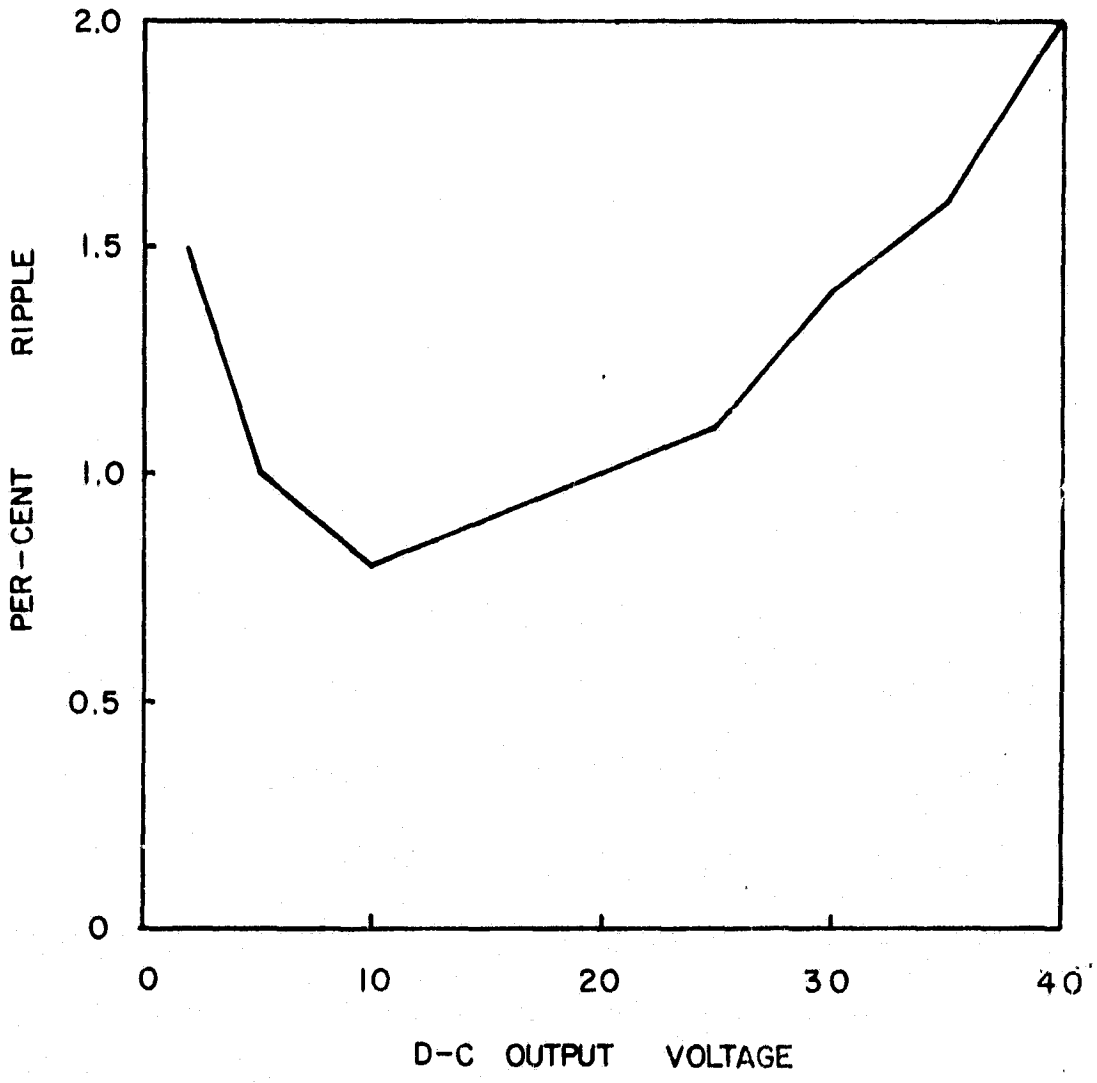


Fig. 9.--A graph showing the per-cent ripple as a function of output voltage.

TABLE 7

PER-CENT DISTORTION WITH CORRESPONDING
SIGNAL FREQUENCY AND OUTPUT POWER

Output Power Watts	SIGNAL FREQUENCY - Hertz					
	50	100	250	500	750	1000
5.0	5.4	5.2	5.3	4.5	1.8	1.9
10.0	5.2	4.9	4.8	4.3	3.2	3.0
14.5	4.8	4.4	4.3	4.5	4.7	4.4
20.0	4.4	4.0	3.9	5.1	6.9	6.2
30.0	4.1	3.7	3.8	5.8	10.0	—
40.0	3.9	3.6	3.9	6.3	11.4	—

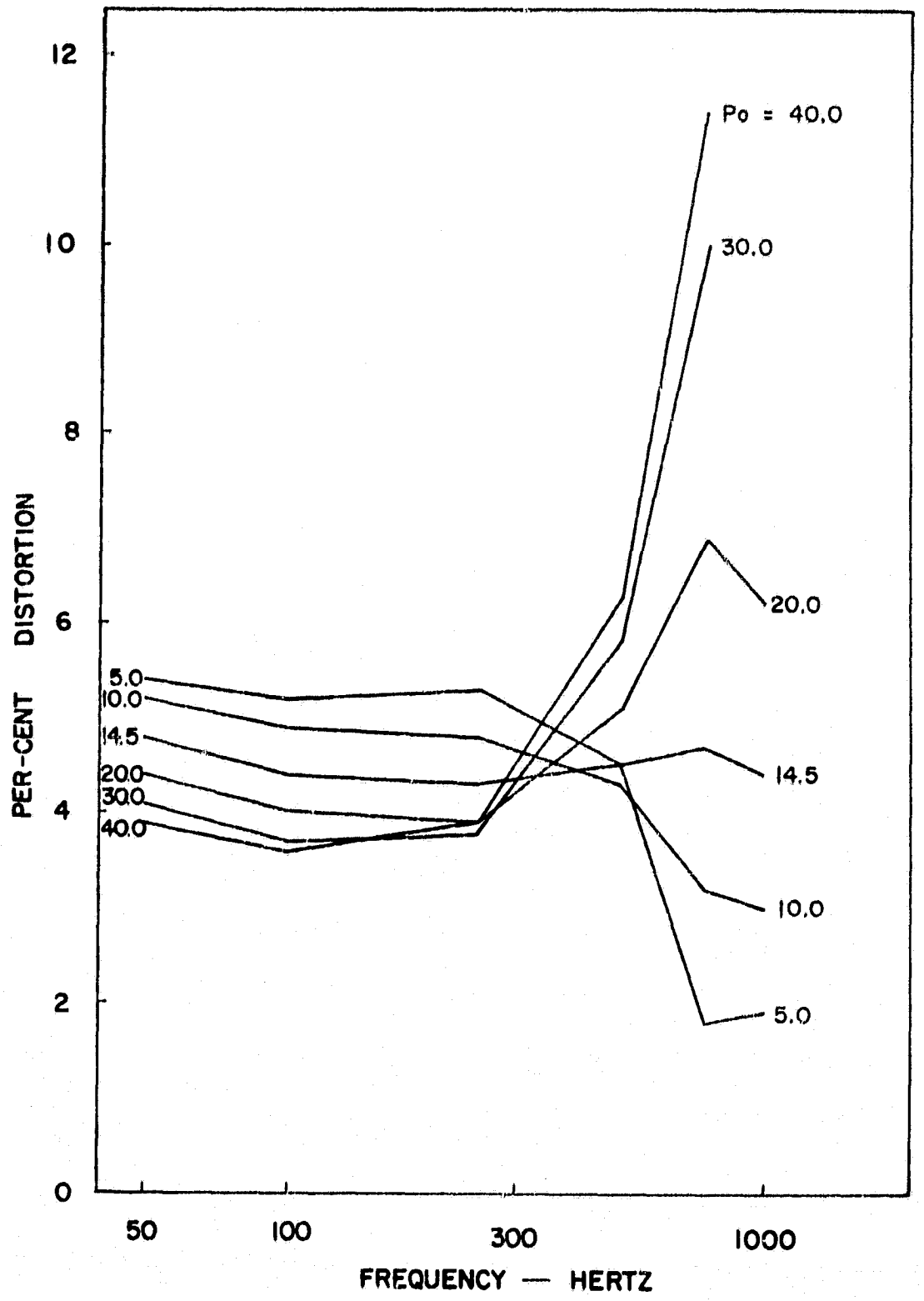


Fig. 10.--A graph showing the per-cent distortion as a function of signal frequency with power output as a parameter.

TABLE 8

DATA AND CALCULATED RESULTS FOR THE A-C EFFICIENCY TEST

Supply Voltage Vdc	Supply Current Adc	Supply Power Watts	Output Voltage V-RMS	Output Power Watts	Efficiency %	Frequency Range Hertz
28.0	0.24	6.7	10.0	5.0	74.4	50 - 1000
28.0	0.48	13.4	14.1	10.0	74.6	50 - 1000
28.0	0.93	26.0	20.0	20.0	76.9	50 - 610
28.0	1.40	39.2	24.5	30.0	76.5	50 - 510
28.0	1.90	53.2	28.3	40.0	75.2	50 - 460

constant in the vicinity of 75% over the ranges of power and frequency tabulated. At 40 watts a-c power output, the modulator and driver consumed approximately 1.2 watts.

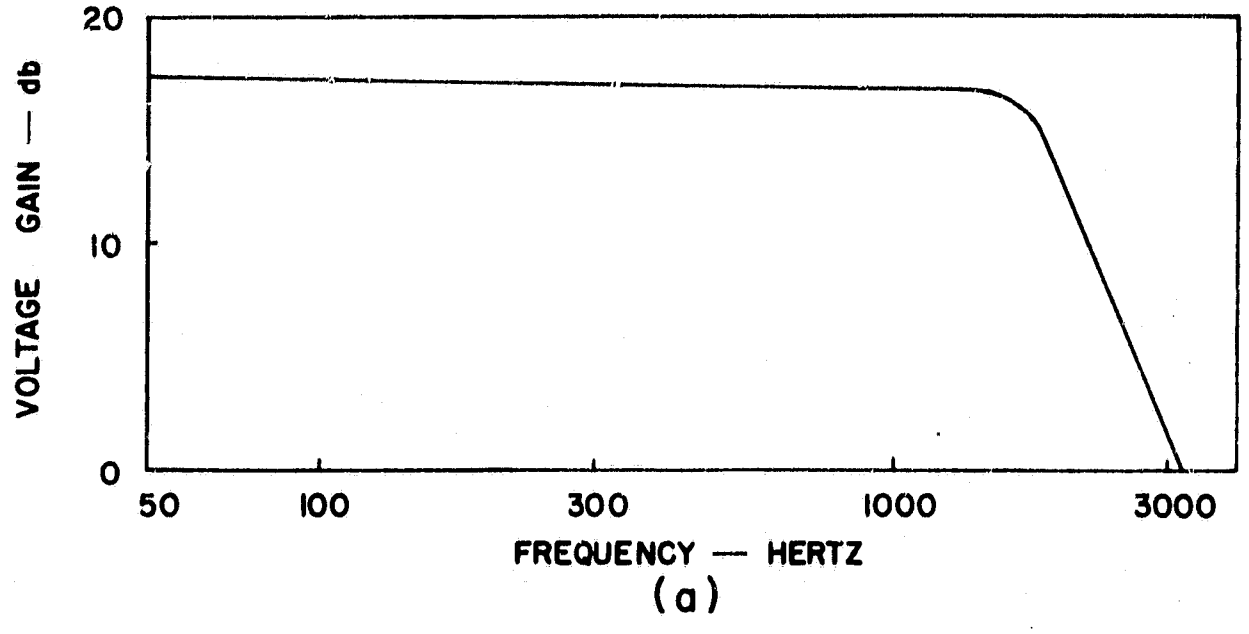
It may be noted that the maximum a-c power output is 40 watts, where for d-c the maximum is 80 watts. This is because the maximum d-c output voltage is equal to the peak value of the a-c output voltage.

The data for the determination of the gain and phase characteristics of the test amplifier are listed in Table 9. The gain and phase characteristics are plotted in Figure 11. It is significant that the gain of the test amplifier was almost constant at approximately 17 db up to the cutoff frequency of the output filter. A subsequent test of the output filter alone yielded a nearly-identical phase characteristic. Thus it would appear that little phase lag may be attributed to the circuitry ahead of the output filter.

TABLE 9

DATA FOR THE GAIN AND PHASE CHARACTERISTICS

Frequency Hertz	Input Voltage V-RMS	Output Voltage V-RMS	Voltage Gain db	Phase Angle Degrees
50	2.34	17.0	17.2	-7
100	2.34	17.0	17.2	-10
200	2.37	17.0	17.1	-17
300	2.37	17.0	17.1	-26
500	2.41	17.0	17.0	-42
700	2.42	17.0	16.9	-57
1000	2.43	17.0	16.9	-85
1500	2.44	17.0	16.8	-134
2000	2.29	10.0	12.8	-213
2500	2.37	5.0	6.5	——
3000	2.32	3.0	2.2	——
3200	2.32	2.3	0	——



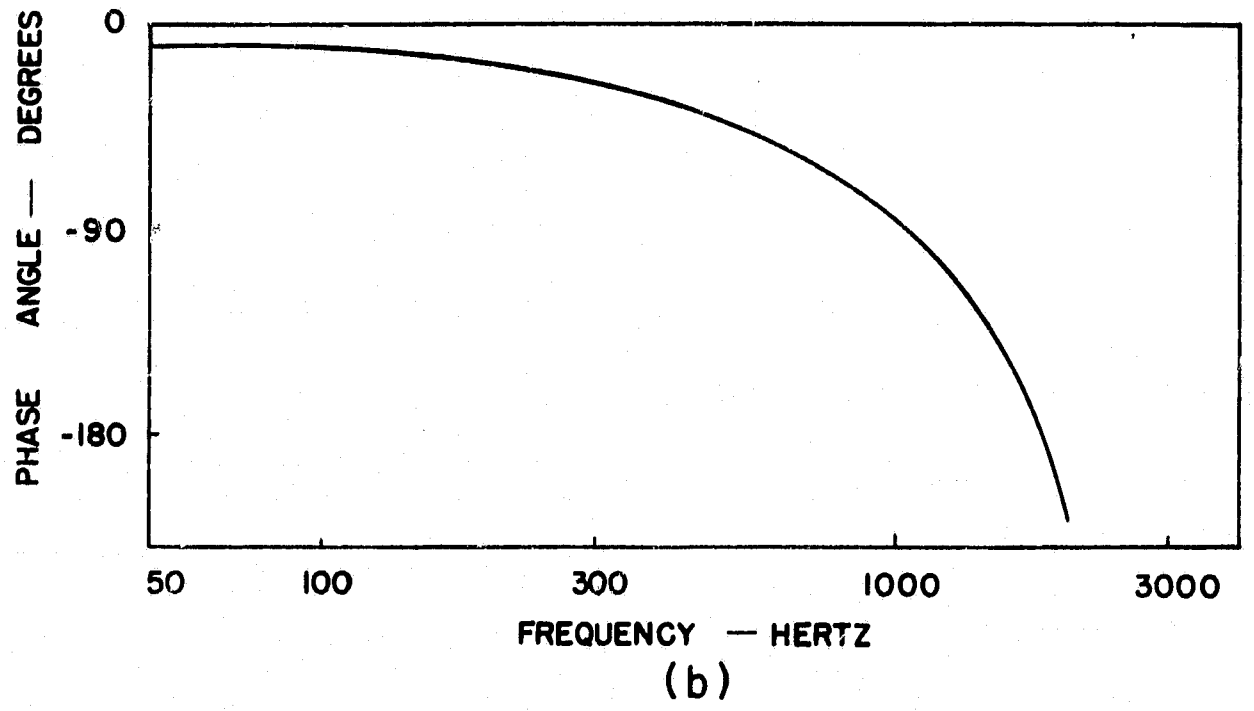


Fig. 11.--The gain characteristic (a), and phase characteristic (b) of the test amplifier.

IV. CONCLUSION

The test amplifier using the transformer-coupled output circuit exhibits several characteristics which are advantageous in a power amplifier. The output circuit tested produced bipolar output voltages from d-c to 1 kHz. while operating from a single d-c power supply. Furthermore, the power supply was completely isolated from the output and input circuitry, as a result of transformer coupling in the driver and output circuits. The distortion was acceptable for a high-power amplifier operated without feedback.

The efficiency of the test amplifier was relatively high. Although direct-coupled bipolar class-D amplifiers which were previously developed have a d-c efficiency of 90% these require two power supplies of opposite polarity, as discussed in Chapter I.[1] The class-D amplifier system utilizing a transformer-coupled output circuit has possible a greater overall efficiency than the forementioned direct-coupled class-D amplifier system since the active and quiescent losses of the required additional power supply have to be taken into account.

An interesting comparison in terms of a-c efficiency may be made between a class-B amplifier and the test amplifier. In Figure 12, the theoretical a-c efficiency of an ideal, push-pull output stage for a transistorized, 40-watt, class-B amplifier was plotted as a function of power output. Also plotted on the same graph is the actual a-c efficiency data for the transformer-coupled output circuit of the

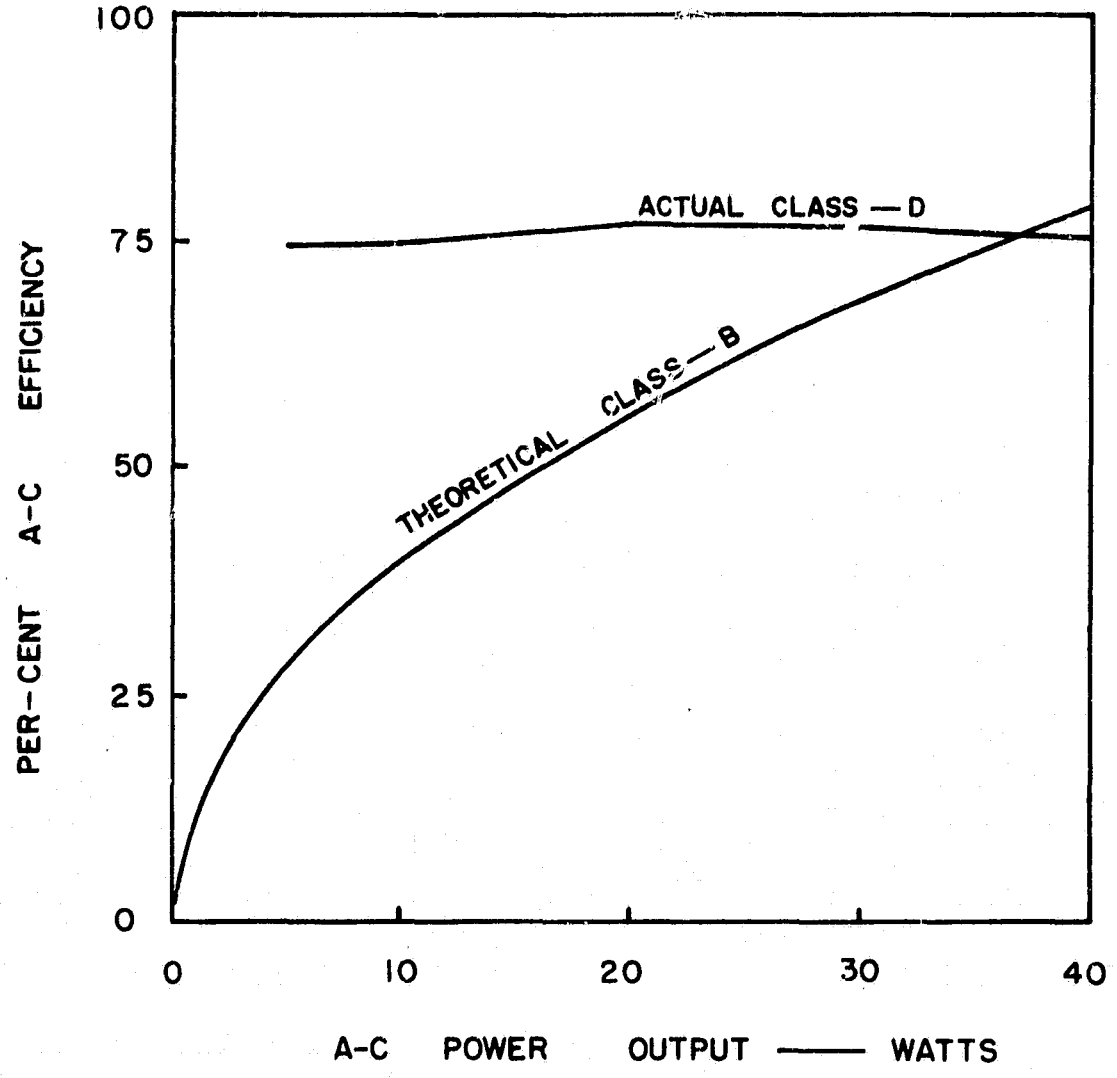


Fig. 12.--A graph showing the a-c efficiency of the test amplifier and the theoretical a-c efficiency of an ideal class-B amplifier.

test amplifier, as listed in Table 8. It may be shown that the maximum power loss for the ideal class-B amplifier is approximately 16 watts, at 16 watts power output. For the test amplifier, the greatest power loss was approximately 13 watts for the entire output circuit and filter. Thus the class-D output circuit would have slightly less heat dissipation.

An advantage, which is incidental to the use of the transformer-coupled output circuit, is the ability of the circuit to withstand a short-circuit at the output terminals. Because current may not flow simultaneously in both windings of the output transformer, current flow in the primary is unaffected by the short circuit. Current flow in the secondary is effectively limited by the limited amount of base current available from the tertiary winding of the output-circuit transformer. However, with the output shorted, all power must be dissipated in the secondary transistor (Q_{43} or Q_{44}), and in the filter inductor, if used.

Unfortunately, the output circuit as shown in Figure 6 will experience destructive failure if the load is removed. This will occur when a driving signal is applied because the output voltage across the filter capacitor will increase until some component (usually Q_{43} or Q_{44}) breaks down. This could be prevented by the inclusion of a protective circuit. Such a protective circuit could consist of a Zener diode which would conduct at some over-voltage and fire an SCR to short the output terminals.

From the results presented here it may be concluded that the use of a transformer-coupled output circuit adds to the advantages of class-

D power amplification. The transformer-coupled output circuit provides the usual advantages of isolation, as well as high efficiency with low quiescent losses. Class-D amplifiers using this type of output circuit are capable of high a-c and d-c power outputs while requiring only one power source.

REFERENCES

1. M. A. Honnell et al., The Analysis and Design of a Class-D Amplifier, Engineering Experiment Station, Auburn University, Auburn, Alabama, February, 1968.

2. E. C. Bell and T. Sargent, "Distortion and Power Output of Pulse Duration Modulated Amplifiers," Electronic Engineering, vol. 37, pp. 540-542, August, 1965.

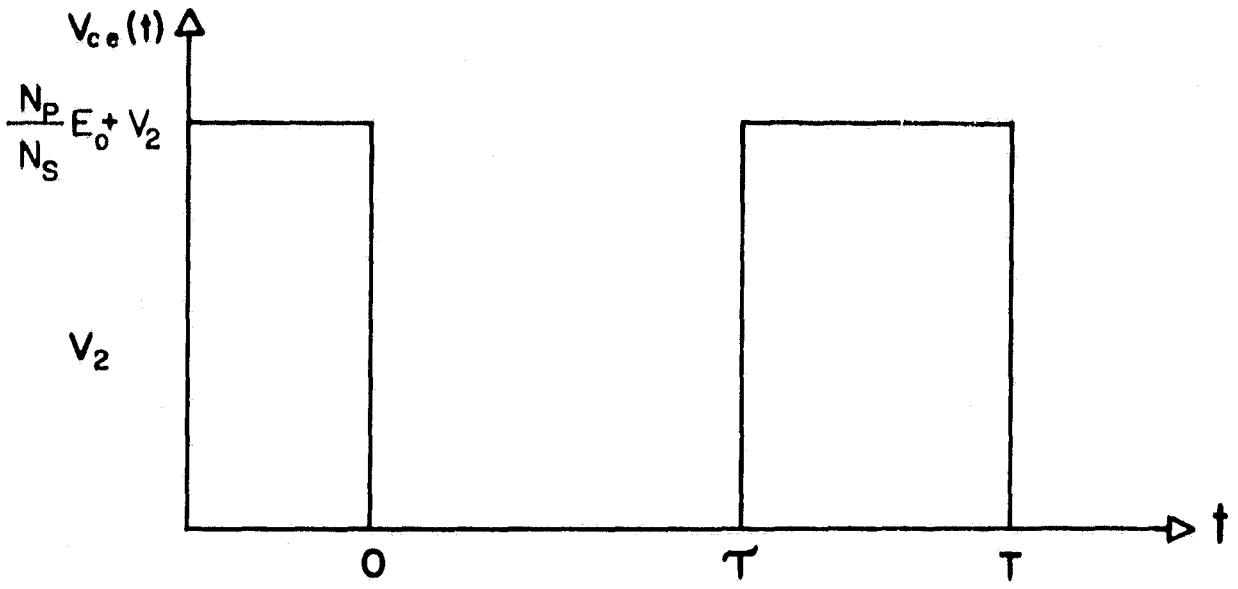
3. Permalloy Powder Cores, Data Catalog PC-303R, Magnetics Inc., Butler, Pa.

APPENDIX A

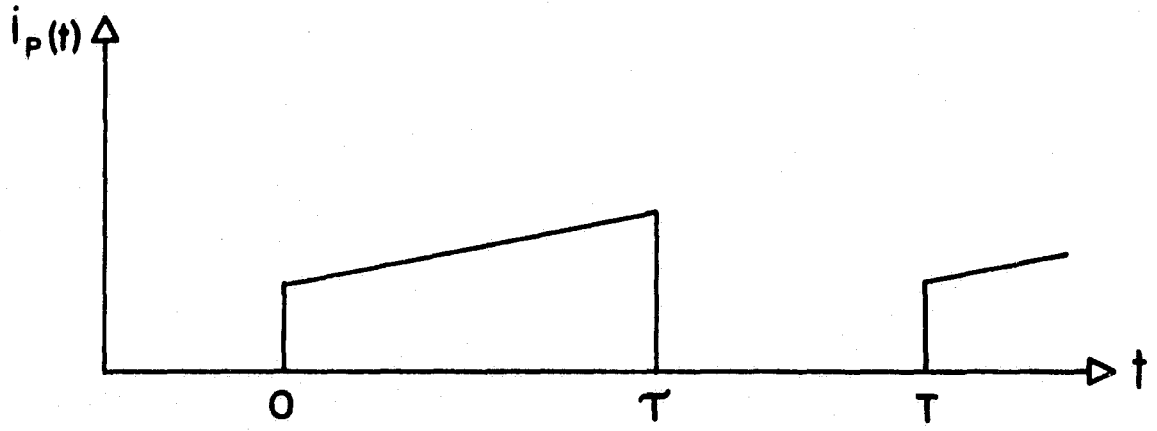
The output-circuit transformer may be made to operate in such a way as to produce trapezoidal current waveforms under certain conditions. If the transformer winding inductances are large enough, the current waveforms will be triangular, as shown in Figure 3, only for τ less than some certain value. For a pulse width greater than this, the current waveforms will become trapezoidal, as shown in Figure 13. The current waveforms have a finite level at $t = 0$ because not all of the energy is removed from the core at the end of each cycle. This is referred to as minor-loop operation because the hysteresis loop for the core does not return to zero magnetization during each cycle.

This mode of operation was investigated because it offers certain advantages in performance. In particular, the same average load current may be obtained while using a waveform having lower peak values. The reduced peak currents allow the use of a smaller transformer core at a given power level. The peak current rating of the active devices in the circuit may also be reduced.

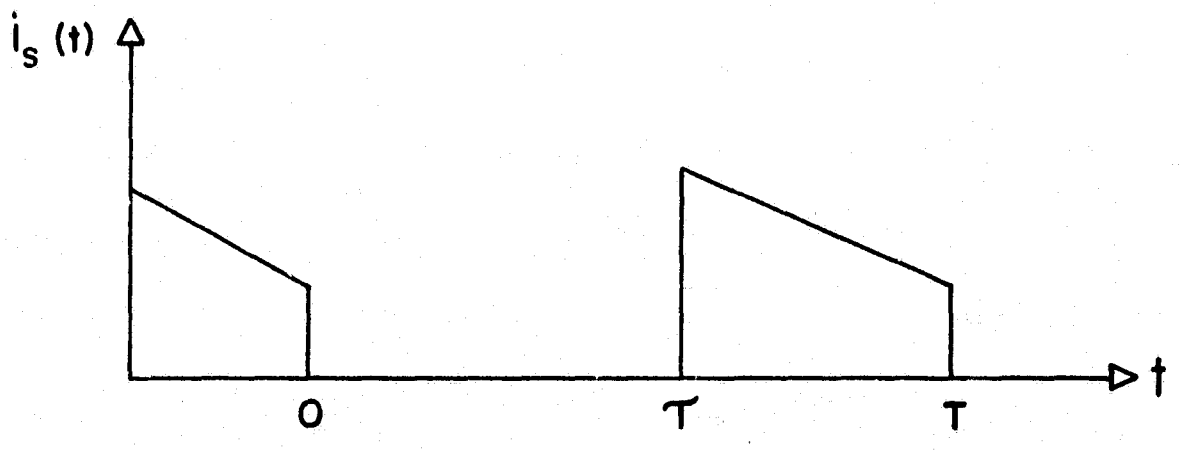
A significant disadvantage of this mode of operation is that the ratio of the output voltage to the driver pulse width is not constant when the current waveforms become trapezoidal in shape. When the current waveforms are ramp functions, the ratio remains approximately constant, resulting in linear operation. However, when the current waveforms become trapezoidal, the ratio begins to increase, and continues to



(a)



(b)



(c)

Fig. 13.--Output-circuit waveforms due to minor-loop operation of the transformer: (a) the collector-emitter voltage of the output transistor; (b) the primary current; and (c) the secondary current.

increase with increasing pulse width. This results in non-linear operation of the circuit.

APPENDIX B

Although both the primary pulse width, τ, and the secondary pulse width, τ', may be selected arbitrarily, it will be shown here that power loss may theoretically be minimized by selecting the proper values for these at maximum power output. The equation describing the ramp of current in Figure 14 is

$$i(t) = I_{pk} \frac{t}{\tau} \qquad 0 \leq t \leq \tau. \tag{B-1}$$

The time-averaged value of i(t) is

$$I = \frac{1}{T} \int_0^{\tau} I_{pk} \frac{t}{\tau} \, dt = \frac{I_{pk} \, \tau}{2 \, T} . \tag{B-2}$$

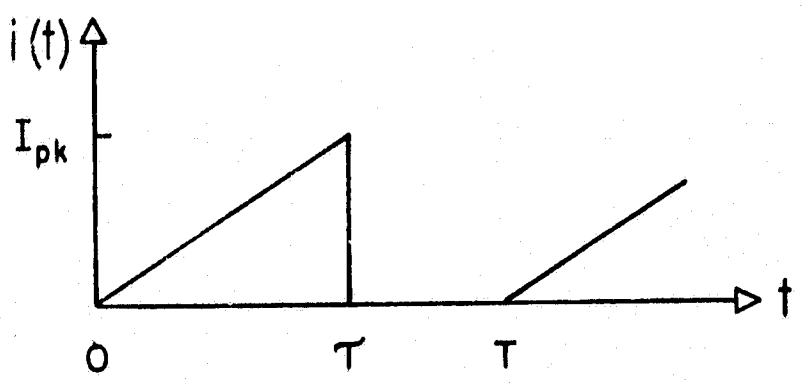


Fig. 14.--A current-ramp waveform.

For i(t) flowing through a resistance, R, the time-averaged power loss in R is

$$P = \frac{1}{T} \int_0^{\tau} i^2(t) R \, dt = \frac{R \, I_{pk}^2 \, \tau}{3T} \quad . \tag{B-3}$$

Solving (B-2) for τ and substituting the result for τ in (B-3) yields

$$P = \frac{2}{3} \, R \, I \, I_{pk} \quad . \tag{B-4}$$

Thus, if a certain average current I must be made to flow through R using a periodic current-ramp waveform, the power loss in R may be minimized by minimizing the peak value, I_{pk}.

Referring to Figure 3(b) and 3(c), define the peak values as

$$i_p(\tau) = I_p \tag{B-5}$$

$$i_s(\tau) = I_s, \tag{B-6}$$

the time-averaged supply current as

$$\text{avg}[i_p(t)] = I_2 = \frac{I_p \, \tau}{2 \, T} \quad , \tag{B-7}$$

and the time-averaged output current as

$$\text{avg}[i_s(t)] = I_o = \frac{I_s \, \tau'}{2 \, T} \tag{B-8}$$

At maximum power output, using anything less than the complete period T would require higher peak currents to maintain the same average currents. Therefore, to minimize losses, let

$$\max \tau + \max \tau' = T \qquad \text{(B-9)}$$

at maximum power output. Since the remainder of the equations in this Appendix are concerned only with conditions at maximum power output, the "max" notation will be dropped until the concluding equations.

In order to determine the fraction of T which should be alotted to τ and τ', assume all power loss in the primary circuit occurs in a series resistor R_p, and that all power loss in the secondary occurs in a series resistor R_S. It follows from (B-4) that the total power loss may be written

$$P_{LOSS} = \frac{2}{3} \left(R_p I_2 I_p + R_S I_o I_S\right). \qquad \text{(B-10)}$$

The substitution of the right side of (B-7) for I_2, the right side of (B-8) for I_o, and $T-\tau$ for τ' at maximum power output yields

$$P_{LOSS} = \frac{4T}{3} \left[\frac{R_p I_2^2}{\tau} + \frac{R_S I_o^2}{T - \tau} \right]. \qquad \text{(B-11)}$$

The power loss may be minimized by taking the derivative with respect to τ, and upon setting the derivative equal to zero, τ may be found as

$$\tau = \frac{\pm I_o I_2 T \sqrt{R_S R_p} - R_p I_2^2 T}{R_S I_o^2 - R_p I_2^2}. \qquad \text{(B-12)}$$

Since the average output current may be written as

$$I_o = \frac{E_o}{R_L} \qquad \text{(B-13)}$$

and the average supply current as

$$I_2 = \frac{E_o^2}{\eta_o V_2 R_L} \quad , \qquad \text{(B-14)}$$

the expression for τ given in (B-12) may be rewritten as

$$\tau = \left[\frac{\pm \eta_o V_2 E_o \sqrt{R_S R_P} - R_P E_o^2}{\eta_o^2 V_2^2 R_S - R_P E_o^2} \right] T \; . \qquad \text{(B-15)}$$

In many cases, reasonable design results may be obtained by assuming $R_S = R_P$. On the basis of this assumption, (B-15) becomes

$$\tau = \left[\frac{\pm \eta_o V_2 E_o - E_o^2}{\eta_o^2 V_2^2 - E_o^2} \right] T \; . \qquad \text{(B-16)}$$

Taking the positive sign, which yields positive values for τ, and returning to the "max" notation, (B-16) may be written as

$$\max \tau = \left[\frac{\max E_o}{\eta_o V_2 + \max E_o} \right] T \; . \qquad \text{(B-17)}$$

Experimental variation of max τ by up to 15% about the value given by

(B-17) has been found to result in little variation in efficiency. This would seem to imply that the assumption of $R_S = R_P$ was not critical.

An additional advantage is obtained from using (B-9) and (B-17) to determine values for τ and τ'. It follows from the preceding equations that for constant values of the average primary and secondary currents, that as τ is made larger, the peak primary current becomes smaller and the peak secondary current becomes larger. If τ is made smaller, the opposite occurs. However, when τ and τ' are selected according to (B-9) and (B-17), the peak currents are approximately equal (from the assumption that $R_P = R_S$) and at their joint minimum (a reduction in one current peak would result in an increase in the other).