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FINAL REPORT

SATURN INTEGRATED CIRCUIT RELIABILITY TEST PROGRAM

NATIONAL AERONAUTICS AND SPACE ADMINISTRATION
George C. Marshall Space Flight Center
Huntsville, Alabama

28 June 1966 - 1 July 1967

Prepared by
K. R. MacKenzie
M. R. Carpenter

On
Contract Number NAS8-18018

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MOTOROLA INC. Semiconductor Products Division

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SECTION I

1.0 INTRODUCTION

As monolithic silicon integrated circuits perform more functions per substrate area, it becomes imperative that studies be made defining integrated circuit reliability characteristics while these circuits are still using relatively simple construction techniques. This is particularly true for linear circuits in which a greater sensitivity to parameter changes within the circuit is suggested by engineering intuition. This program was proposed, in response to a request for quote issued by NASA's George C. Marshall Space Flight Center, Huntsville, Alabama, to explore the reliability of four types of linear circuits that have potential use in future NASA programs and thus achieve, by testing, a reliability figure of merit for each circuit.

The linear integrated circuit family now includes advanced circuit performance characteristics with the same potential reliability as found in digital integrated circuits and with a circuit cost not much greater than that of the discrete silicon transistor. Yet the use of circuits with unknown or unproven reliability, as attractive as their other features may be, should not be permitted in programs demanding highly reliable performance from all its parts until these circuits have been shown to merit consideration, either through extensive reliability testing or as a result of considerable field experience. Therefore, this program was undertaken in 1966 to study the reliability of two classifications of linear integrated circuits (the operational amplifier and the differential amplifier) made by different manufacturing processes (Table 1-I). Eight hundred test samples were selected. These samples were equally divided between the MC-1530F operational amplifier, the MC-1525G differential amplifier, the MC-1519G differential amplifier, all manufactured by Motorola, and

TABLE 1-I
COMPARISON OF TEST DEVICES

DEVICE TYPE	MC-1519G	MC-1525G	MC-1530F	SN-526A
TYPE OF AMPLIFIER	Differential	Differential	Operational	Operational
MANUFACTURING PROCESS	Monolithic PNP and Monolithic NPN with Thin Film Resistors	Monolithic with Diffused Resistors	Monolithic with Diffused Resistors	Monolithic with Diffused Resistors
TYPE OF PACKAGE	10-lead TO-5 Package	10-lead TO-5 Package	10-lead Alumina Flat Package (1/4" x 1/4")	10-lead Welded Flat Package (1/4" X 1/8")
LEAD WIRE	Gold	Gold	Aluminum	Gold
LEAD BOND TECHNIQUE	Stitch	Stitch	Stitch	Ball
METALLIZATION	Aluminum	Aluminum	Aluminum	Aluminum
MONOLITHIC CHIP	Epitaxial Diffused	Epitaxial Diffused	Epitaxial Diffused	Triple Diffused

the SN-526 operational-differential amplifier manufactured by Texas Instruments. Its goals were to complete a study that would design or evaluate screening tests and estimate their effectiveness, develop or define methods for linear circuit reliability analysis and stress evaluation, develop a method for predicting early failures, estimate the life expectancy of these circuits, and consider stresses associated with handling, testing and installation in equipment. This report summarized the results of this program.

1.1 GENERAL PROGRAM INTRODUCTION

1.1.1 Survey of Available Literature

A survey of existing reliability physics literature and semiconductor test reports was conducted to support the design phase of the test program. In this survey, 217 documents or articles were reviewed. Included in the data selected were previous studies and tests, publications, articles in professional journals, and presentations made at the various symposia conducted in the reliability engineering field. Section V discusses this survey in more detail. A listing of the reference material is in the Appendix.

At the conclusion of this data search, the failure mechanisms were categorized with respect to the region or area of the complete integrated circuit affected, e.g., bonds, interconnects, passivation, surface contamination, bulk defects, and other miscellaneous failure mechanisms. These dominant failure mechanisms and their applicable subdivisions were then used in the analysis of the manufacturing processes by which the different parts were constructed to design the specific details of the test program. The classifications of potential failures that Motorola selected for final reject classifications are summarized in the following paragraphs. A brief description of each failure mechanism is included under each reject classification. Table 1-II lists in outline form by major titles, each failure mechanism.

TABLE 1-II

DATA SURVEY FAILURE MECHANISM CLASSIFICATION

I. Intermetallic Compound Formation Failure Mechanisms

II. Wire Bond Failure Mechanisms

- a. Underbonding
- b. Overbonding
- c. Improper bond location

III. Improper Interconnections - Metallization Failure Mechanisms

- a. Metallization corrosion and decomposition
- b. Metallization alloying and diffusion
- c. Metallization creeping

IV. Passivation Failure Mechanisms

V. Surface Contamination Failure Mechanisms

- a. Ionic inversion
- b. Organic Material Contamination

VI. Bulk Failure Mechanisms

VII. Package Failure Mechanisms

VIII. Miscellaneous Failure Mechanisms

1.1.1.1 Intermetallic Compound Formation Failure Mechanism

This failure mechanism is generally associated with the by-product of joining two different metals subject to chemical reaction under highly stressed conditions. The specific mechanism that is applicable to this program, would be experienced when gold and aluminum junctions are exposed to accelerated temperatures. As is shown in numerous documentaries (noted sources in Appendix A), this mechanism is a function of temperature and reacts much more rapidly as the ambient temperature increases. The formation of gold-aluminum intermetallic compounds is generally considered to be nonexistent when the temperature does not exceed 150°C. In this program, three of the samples selected have gold leads and aluminum metallization and one of these three samples has posts where gold wires are bonded to aluminum surfaces It was expected that this mechanism would play a dominant role in these reliability evaluations, especially in the high temperature and temperature cycling tests. This mechanism usually occurs well above the manufacturers maximum ratings.

1.1.1.2 Wire Bonds Failure Mechanisms

Failures attributed to wire bonding from the lead wire to the bonding pads on the silicon die are generally the results of overbonding, underbonding, or improper location of the bond on the bonding pad. The open, intermittent, or high resistant bond failure attributed to overbonding is normally considered to be caused by an application of excessive pressure by the bonding tool on the lead in the wire bonding processes. This results in either a severing of the wire completely or a crimping of the wire enough to reduce its effective cross-sectional area for current transfer and/or its mechanical strength. Shorted circuits can also result from overbonding when excessive

temperatures occur, either at the die on the bonding too, which splatters the lead materials on the surface of the die. Under-bonding, however, may produce both open and intermittent bonds which are the natural result of insufficient pressure and/or temperature in the bonding operation. Improper bonding location may cause intermittent and shorted circuits. When bonds are formed too close to the edge of the interconnection, it is possible for a direct short to the silicon substrate material through pinholes and scratches in the oxide or improper passivation to occur. It is also possible, where a bond is made too close to the edge of the die, to find a bond shorted to the substrate material. There is also the potential intrametallization short when bonds are not located in their proper positions.

1.1.1.3 Improper Intraconnection Failure Mechanism

Two specific failure mechanisms are normally related to improper intraconnections. The first one is that of metallization and generally includes within its heading: decomposition of metal, corrosion of the metal, oxidation of the metal, improper deposition of the metal resulting from poor mask alignment, and lifting of the metal from the oxide surface. The second mechanism associated with improper intraconnections is that of metal diffusion and alloying which normally has been found to occur at stress conditions well above and in excess of maximum rated conditions for the integrated circuit. These circuit failures have been observed in past experimentation when the gold or aluminum metallization diffuses into junction or isolation regions or when aluminum alloys with the normal silicon dioxide (SiO_2) glass passivation at temperatures above 300°C. A third mechanism normally associated with poor design or overcurrent stressing, is that of metallization creeping where aluminum metal ions have been detected migrating to the positive polarized terminal when

the proper conditions exist in metal temperature and current density such that the aluminum becomes semiliquid, permitting more rapid motion of the aluminum ions. At Motorola, this formerly has been noted only in high current power step stress tests. Integrated circuits are normally designed with sufficient safeguard to guarantee long life under normal biased conditions.

1.1.1.4 Passivation Failure Mechanism

Insufficient or imperfect passivation has lead to failures resulting from a variety of factors. This classification includes pinholes and oxides, cracks and oxides, scratches and oxides, feathering of oxides, flaking of oxides, undercutting of oxides, and insufficient thickness of oxides.

1.1.1.5 Surface Contamination Failure Mechanism

Two types of surface conditions are generally associated with reliability of integrated circuits. The first mechanism is that of inversion of a surface region by a phenomenon referred to in technical literature as channelling and has been the subject of many articles in professional journals and presentations at the symposia. Channelling occurs when a bias voltage applied across a p-n junction causes mobile impurity ions (on the surface of the passivation, within the passivation, or at the interface between the passivation and the surface) to move to create a concentration of charges over the semiconductor material adjacent to the junction. This charge concentration causes a concentration of carriers of opposite polarity in the surface of the silicon adjacent to the junction, and when great enough, will invert p-type material to n-type material (or n-type material to p-type material). It has been shown that this condition is temperature-dependent (e.g., high ambient or junction temperature

accelerates the failure mechanism) and that the inversion of only a few monolayers at the semiconductor surface is necessary to create a channel of electrical significance. The second mechanism would be a more common mechanism related to organic materials or atmospheric contaminants being attracted to or left on the surface of the die. Device failures have been found to be caused by these organic materials left on die surfaces during processing of devices. These materials can cause device failures by providing a resistance short between silicon elements, by corroding vital areas of the integrated circuit and by many other potential mechanisms up to and including mechanical damage caused by microscopic particles left within the package after normal sealing.

1.1.1.6 Bulk Failure Mechanism

Bulk failure mechanisms are usually grouped to include cracks and scratches in dice with those defects which are inherent in the wafer or are induced during normal processing. One group of potential failures in this category may be associated with epitaxial layer imperfections, edge dislocations, isolated dislocations, twin boundaries, etch pits, stacking faults, and "stair-rod" dislocations associated with stacking faults. These failure mechanisms are found infrequently and usually are masked by the predomination of other mechanisms. Cracks in silicon die are found periodically in sample circuits. They may be caused primarily by overpressure applied during the die to header bonding operation, by mechanical stresses induced in the die as a result of changing thermal conditions, from impact shock and vibration felt by improper bonded die or the thermal mismatch of basic materials used in the construction of the integrated circuits. The latter instance is generally a function of circuit design and, when inadequate to withstand normal stresses, will usually be detected and corrected after the first series of thermal shock tests. Scratches in die may occur

during processing. Cracks or scratches occurring before passivation may result in failures that may be assigned to other mechanisms such as metal diffusion into silicon and pinholes in oxide.

1.1.1.7 Package Failure Mechanisms

Those failure mechanisms associated with package failures are generally reduced to the ability of a package to maintain a hermetic seal. Device failures have been found to be caused by faulty seals which permitted contaminants, particularly moisture, to react chemically with device materials. However, other mechanisms related to package reliability, such as ability of the package to withstand external corrosive environments, or the solderability of leads, are often included but are normally associated with quality assurance rather than reliability.

1.1.1.8 Die Bond Failure Mechanisms

The reliability of semiconductor devices has always been associated with the effects of temperatures. It is normally assumed that devices operating at higher junction temperatures are more liable to be affected by accelerated physical causes of failure than are the same devices operating at lower temperatures. For this reason, an improperly bonded die, characterized by voids under the die, may lead to thermal stresses that accelerate other failure mechanisms.

1.1.1.9 Miscellaneous Failure Mechanisms

Other mechanisms, such as improper masking, etching, misorientation of die, improper leads, and external surface condition, are being grouped under one singular heading for they generally do not contribute significantly to reliability stress failures. Improper masking or etching failures may normally be rejected during production electrical tests.

1.1.2 Summary of Test Program

The test program as finally decided upon is summarized in Table 1-III. Techniques found in the past to be significant for stressing the failure mechanisms reviewed in the data survey were utilized. These testing techniques emphasized operating and storage life and step stress testing. In addition, two environmental sequences were adapted from Mil-Std-19500 "MILITARY SPECIFICATION GENERAL SPECIFICATION FOR SEMICONDUCTOR DEVICES." Other tests performed included evaluation of the die surface temperatures, while under power, using a Barnes infrared interferometer; plus a repeat of two of the power temperature step stress tests making parameter measurements at high and low temperatures (-55° and +125°C). At the conclusion of the test program when all program tests were completed, Motorola added mechanical impact shock and mechanical vibration variable frequency. A quick synopsis of the goal of each major segment of the test program is shown in Table 1-III.

1.1.2.1 Operating Life Test

Three operating life tests were planned, one at 25°C and two at 125°C. The purpose for performing the 25°C test was to include a control test which would be invaluable if catastrophic effects were noted in one of the more highly accelerated tests. This test did become a very valuable tool for comparing relative parameter stability and the ability to withstand biased stress conditions at high temperatures for the MC-1525 and the MC-1519. The test sequences at 125°C were performed at two power levels, 100 and 300 mW, for the MC-1530, MC-1519, and SN-526. Because the incidence of failures had, in most past experiments, shown to be related mathematically in a logarithmic manner with the inverse of the absolute temperature, it was felt that two steps of different

TABLE 1-III
PROGRAM TEST PLAN

TEST STRESSES	DEVICE TYPES MC-1519G	MC-1525G	MC-1530F	SN-526A
	Number of Samples for Each Test			
OPERATING LIFE TESTS				
(1) Elevated Ambient	25	25	25	25
(2) Room Ambient	15	15	15	15
(3) Elevated Ambient Accelerated Power	25	25	25	25
STORAGE	15	15	15	15
STEP STRESS TESTS				
(5) Temperature	15	15	15	15
(6) Power (T_A = 25°C)	15	15	15	15
(7) Temperature - Power	15	15	15	15
(8) Temperature Cycling	15	15	15	15
MIL-S-19500 TEST SEQUENCES				
(9) Mechanical	25	25	25	25
(10) Thermal	25	25	25	25
SPECIAL STUDIES	10	10	10	10

junction temperatures would provide much more additional information than a single test at one level would have done. Had enough time existed to continue these tests indefinitely, a means of extrapolating these test results from the highly accelerated conditions used in this program to some normal system use conditions would have been possible. However, inasmuch as no failures were observed at 25°C, only inaccurate estimates can be made of the failure rate expected to be found at that stress condition.

At the time the program was proposed, it was assumed that if it were possible to achieve an inference (prediction) of the estimated failure rate expected to occur for each device after 8000 hours of operation at some typical use condition, then it would have to come from this portion of the test program utilizing either Arrhenius model of physical degradation or estimate of percent failure increase with respect to time. This part of the program combined thermal, voltage, and current stresses that should succeed in activating any and all known physical failure mechanisms reported in the previous section. All other test sequences have specific stress goals and either would not combine all variables into one test program or would be of such a nature that the information gathered from these test cells would not be used for long-term degradation predictions.

It was found for the MC-1525 that the only way one could effectively increase its junction temperature was by increasing the ambient temperature. This device was limited by its circuitry to approximately 100 milliwatts of power dissipation. Therefore, the temperature ambient for the MC-1525 at the "300-milliwatt stress level" was changed to 150°C with normal circuit power being dissipated.

1.1.2.2 Storage Life Test

A storage life test was included as a second control within the program. Past experience had shown that storage life tests have relatively little effect on integrated circuit performance characteristics. This test is required, however, to achieve a comparison of biased versus unbiased test results.

1.1.2.3 Environmental Stress Test Sequences

These test sequences are semiconductor standards which have been used in the industry during the past ten years. All solid state semiconductor devices, whose physical size is similar to those of the integrated circuits used in the test program, have been shown to be capable of passing each test in these sequences alone and as a sequence. Therefore, this test was performed to verify that each product was capable of withstanding these minimum environmental requirements. A mechanical and a thermal test sequence were included. The mechanical sequence included impact shock, vibration variable frequency, vibration fatigue, and a constant acceleration test. The thermal test sequence included solder heat, temperature cycling, thermal shock, and a moisture resistance test.

1.1.2.4 Step Stress Testing

Step stress testing is a technique for rapidly accelerating physical failure mechanisms utilizing the same samples until the maximum limit of the stresses has been reached or the maximum limit of the device has been reached. It has become accepted as a reliability tool not because its data is easily translatable to operational use phenomenon, but rather because it provides a quick and relatively inexpensive method of determining the basic failure mechanism for any

product and the maximum physical capabilities of the package and die system. Therefore, a series of step test sequences was conducted. They included a temperature step stress to determine the temperature limitation of each system; temperature-power step stress tests at 25° and 125°C to evaluate physical failures likely to occur as a direct result of temperature, bias, and high current density; and a temperature cycling step stress test was included to compare effects related to rapid temperature changes.

1.1.2.5 Nonprogram Test Sequences

Four test sequences were added after the program had been initiated and was underway. These test sequences included an analysis of the die bond structure using infrared techniques, a power temperature step stress test reading each test parameter at -55° and 125°C before resuming stressing, a mechanical impact shock step stress test, and a vibration variable frequency step stress test. These added tests supplied valuable information concerning the ability of the die to withstand mechanical shocks, the temperature differentials across the die surface during the power step stress test sequences, and the potential future use in programs of high temperature parameter measurements as a failure rate indicator.

1.1.2.6 Parameter Measurements

Parameter measurements were normally performed at room temperature ($T_A \approx 25°C$) before and after each step in this program. The parameters measured are listed in detail in Section 3.2 but included as a minimum; open loop or differential gain, input current drain, and input voltage differential were used wherever applicable for each circuit.

1.2 TEST PROGRAM SUMMARY

A summary of the test program results is shown in Tables 1-IV through 1-VII. However, to touch on only the highlights (more detail is included in Section 4), it is possible to conclude that all parts used in this program have attractive reliability features that make them potentially useful in a number of high reliability applications. The most reliable part tested was Motorola's operational amplifier, the MC-1530F. This part was not only the most reliable, as defined by the end-point criteria used in this program (see Section 3), but it was also the most stable. In no test did any of the MC-1530F test parameters (measured at room temperature) show any signs of constant degradation. It withstood ambient temperatures of 475°C and all thermal and shock tests it was subjected to. The next most successful part was the SN-526 operational amplifier manufactured by Texax Instruments. In some tests, its performance exceeded that of the MC-1530F; but it was more temperature sensitive and the input circuits did tend to degrade when subjected to the higher temperatures for long periods of time.

The MC-1525G exhibited the best circuit parameter stability for this program (excluding the MC-1530F), but did demonstrate a destructive phenomenon that restricted the use of the resistive network in its current control circuit. The MC-1519G performed poorest of all the circuits tested in this program. It appeared to be more susceptible to processing errors as well as process-related phenomena. For instance, the MC-1519G did show a higher susceptibility to the intermetallic compound formations at the Au-Al interfaces on its die and bonding posts. While all devices using gold wire interconnections and aluminum metallization on the die did exhibit this expected phenomenon, the MC-1519G did so most often, particularly on long-term storage tests at temperatures where the rate of reaction should have

TABLE 1-IV
PROGRAM SUMMARY REPORT - ALL DEVICES

Test Description	Test Duration	Accumulated Hours of Testing	Initial Sample Size	Number of Failures
Operating Life Tests				
T_A = 25°C P_d = 100 mW	3000 hours	121,875	60	0
T_A = 125°C P_d = 100 mW	3000 hours	278,561	100	6
T_A = 125°C P_d = 300 mW	3000 hours	255,624	100	15
Storage Life Test T_A = 150°C	3000 hours	177,500	60	3
Mechanical Test Sequence Impact Shock 1500g 1/2 ms Vibration Fatigue 20 g Vibration Variable Freq. Constant Acceleration 20,000 g	X	X	98	2
Thermal Test Sequence Solderability Temperature Cycling (-65° to +175°C) Thermal Shock Moisture Resistance	X	X	100	0

TABLE 1-V
PROGRAM SUMMARY REPORT
ALUMINUM WIRE SYSTEM (MC-1530F)

Temperature Step Stress Test		Power Step Stress Test				Temperature Cycling Step Stress ($-55^{o}C$ to T_h)	
		$T_A = 25^{o}C$ t = 48 hrs/step		$T_A = 125^{o}C$ t = 48 hrs/step			
Sample Size = 15		Sample Size = 15		Sample Size = 15		Sample Size = 15	
Test Cell ($T = {}^{o}C$)	Number of Failures	Test Cell (mW)	Number of Failures	Test Cell (mW)	Number of Failures	Test Cell ($T_h = {}^{o}C$)	Number of Failures
200	0	100	0	100	0	150	0
225	0	200	0	200	0	175	0
250	0	300	0	300	0	200	0
275	0	400	0	400	0	225	0
300	0	500	1 (1)	500	0	250	0
325	0	600	0	600	1 (2)	275	0
350	0	700	2 (2)	700	6 (2)	300	0
375	0	800	10 (2)	800	3 (2)	325	0
400	0						
425	0						
450	1						
475	0						

NOTES:

1. Test equipment error. Not discovered until too late to return device to lot.
2. Metal migration due to excessive current density at overstressed conditions.

TABLE 1-VI
PROGRAM SUMMARY REPORT
GOLD WIRE SYSTEMS (MC-1519G, MC-1525G, SN-526)

Temperature Step Stress Test		Power Step Stress Test				Temperature Cycling Step Stress ($-55^{o}C$ to T_h)	
		$T_A = 25^{o}C$ t = 48 hrs/step		$T_A = 125^{o}C$ t = 48 hrs/step			
Sample Size = 45		Sample Size = 30		Sample Size = 30		Sample Size = 45	
Test Cell ($T = {}^{o}C$)	Number of Failures	Test Cell (mW)	Number of Failures	Test Cell (mW)	Number of Failures	Test Cell ($T_h = {}^{o}C$)	Number of Failures
200	0	100	0	100	0	150	0
225	1	200	0	200	0	175	1
250	1	300	0	300	0	200	0
275	8	400	0	400	0	225	0
300	14	500	0	500	1	250	0
325	8	600	0	600	3	275	3
		700	1	700	3	300	13
		800	0	800	1		
		900	3	900	2		
		1000	0				

TABLE 1-VII
PROGRAM SUMMARY REPORT
GOLD WIRE SYSTEMS - MC-1525G

Power-Temperature Step Stress Test
T_A = 25°C
t = 48 hours/step
Sample Size = 30

Test Cell (T = °C)	Number of Failures
125	1
150	0
175	0
200	0
200	3

been substantially reduced. This factor may be attributed to the fact that this circuit is a hybrid circuit and, therefore, has more bonds. The MC-1519G also exhibited a greater susceptability to the surface inversion phenomenon (channelling) than did the other circuits, even though the MC-1530F and MC-1525G dice are made using the same integrated circuit die manufacturing process and did not exhibit similar channelling problems.

1.2.1 MC-1530F Results

No continuous degradation occurred for this circuit. The failures that did occur at the very highly accelerated stress levels were catastrophic in nature and resulted from metallization over-stresses or metal oxidation at the very high temperature. The power step stress failures are probably attributable to the method of test. On a single die, this power level is obtained by increasing the current drain in the output stages resulting in excessive current flows through critical metal regions. Motorola has performed considerable work in the metallization stressing and it is known that the rate of degradation of these circuits is both a function of current density and temperature. In these junction surface regions, the temperature exceeded 225°C and the current density approached critical proportions of 5×10^5 A/cm^2. Therefore, catastrophic metallization failures developed. It can be deduced therefore, that tests designed with power requirements greater than 400 milliwatts for circuits designed for milliwatt application are stressing the circuits beyond the physical limitation of the materials involved. In all, the MC-1530F did not demonstrate a single unreliable characteristic. All failures were generated as a result of overstressing each circuit beyond its physical limitations.

1.2.2 SN-526 Results

This circuit was less stable than that of the MC-1530F. Its input current did increase for each test that occurred at the ambient temperature of 125°C or higher. This may possibly be explained by recognizing that the SN-526 employs a Darlington input and that the temperature may be degrading the low-current gain by affecting the surface around the p-n junction regions. The effects of temperature related to surface concentrations of aluminum and oxygen ions and other forms of surface impurities have been the subject of many extensive investigations and it is probable that temperature is affecting the Darlington inputs in just this manner. Surface inversion did not appear to be taking place, for there was no input current recovery phenomona as a result of bake-out. In fact, this degradation took place during a storage life test. This change is accomplished within the first 1000 hours and very little degradation occurs after that. No devices degraded enough to have failed the limits originally selected.

Another failure mode was detected in the storage life test, the storage temperature step stress tests, and the temperature step stress test cells that is usually found in temperature tests when gold and aluminum metal interfaces occur. This failure mode is the occurrence of intermetallics commonly referred to as "purple plague" but also consisting of compounds other than Au_2Al. The rate of occurrence of these failures was not significantly different for either of the three devices using this interconnecting metal system. There appears to be little difference in the effects of temperature stresses on ball bonded leads and wedge bonded leads. The gold-aluminum intermetallics present, if not the principal cause of failure, were present in sufficient quantities to weaken the bonds so that subsequent stressing easily failed the circuit.

The SN-526 did the best in both power step stress tests as shown in Table 4-II. These circuits were best able to distribute the additional power requirements throughout their various elements. The MC-1530F concentrated the greatest share of its load throughout its output section; therefore, it is not unexpected that metallization wearout occurred at the 600- through 800-milliwatt stress levels. Yet the SN-526 was far superior to the MC-1530F in these power tests. The reason for this is not difficult to determine.

In any power stress test, the test sample is subjected to active region current density, metallization current density as well as the other temperature and voltage stresses. The SN-526 has an absolute value of 24 volts applied across the device as opposed to 12 volts for the MC-1530F. The total circuit current drain for the SN-526 at each stress step was only one-half that of the MC-1530F. Also, as the stresses increased, the twin output function of the SN-526 was utilized, thereby dividing the current density applied to each metal strip and active component still further. Finally, the SN-526 die had 4.5 times the surface area of the MC-1530F.

These factors resulted in less total current drain, less individual component current drain in that more components were available to accept the current loads, and more silicon dice to act as a heat conductor for that thermal energy generated at the die surface. This, then, should have resulted in lower hot spot temperatures, less stress and a greater likelihood of survival at these stresses.

1.2.3 MC-1519G Program Results

The MC-1519G differential amplifier is a hybrid circuit of excellent promise. However, in this program, certain weaknesses in processing were detected that make it mandatory that a tight visual inspection be implemented prior to accepting these parts for

applications requiring high reliability factors. This device produced the largest variation in the number of failure modes detected. Yet no failures occurred during operation at 25°C. Of the three failures detected at 125°C and at a power dissipation level of 100 milliwatts, one (at 125 hours) had a chopped (overbonded) lead bond which was the mechanism that led directly to the wire lifting from one of the interconnection islands. A second device (at 2000 hours) failed catastrophically and had a chopped bond as well as an excessive gold-aluminum reaction on the island region. The failure at 3000 hours was due to surface inversion or channelling.

Other failure modes were detected in other sequences. A list of the failure modes and where they occurred would be as follows:

(1) Chopped Bonds: This phenomenon was detected in the 100 milliwatt, 125°C operating life test, and in the shock step stress test which is described in a section entitled Additional Tests.

(2) Channelling: One failure at 3000 hours was detected in the 100 milliwatt-125°C life test; two such failures were found in the 300 milliwatt-125°C life test; one was found in the power step stress test at 25°C; and two at the power step stress test at 125°C.

(3) Aluminum-Gold Intermetallic Compounds: Their presence was observed in every MC-1519G test in this program that had the ambient temperature controlled at 125°C or higher.

(4) Broken Ceramic: The MC-1519G uses a ceramic disc to provide electrical isolation between the integrated circuit die and the dual-PNP transistor chip. After a mechanical impact shock test, this ceramic disc was found to be broken for one sample. However, this problem occurred only once and did not show up in the higher

stress levels of the centrifuge test or of the special impact shock test (10,000 G force) performed at the completion of the test program. It is assumed to be a random isolated event easily screened.

1.2.4 MC-1525G Program Results

The problems associated with the MC-1525G were the result of a peculiarity in the construction of the MC-1525G that permitted a catastrophic four-layer diode action to occur as a result of bias at temperature, the base current bias applied to terminals 3 and 9, plus the use of the lowest resistance (highest current) combination in current source emitter leg. While this results in an abnormally high number of failures in those cells combining an ambient temperature of 125°C with bias, no failures of this nature were generated when current limiting resistors were added to the bias circuits. No failures occurred because of parameter degradation. In fact, the MC-1525G stability features were better than that of all other test devices, except the MC-1530F.

A general summary of the results of this circuit's performance would show that:

(1) No failures or degradation occurred at the room temperature test condition.

(2) No failures, other than the NPNP action, occurred under the 100-milliwatt operational life test performed at 125°C.

(3) Three failures, other than that noted in point 2, did occur as a result of intermetallic chemical reaction of gold and aluminum in the 100-milliwatt, 150°C test--at which condition the average junction temperature was approximately 175°C, beyond the Motorola ratings of such a device.

(4) No failures of any kind were detected from storage at 150°C ambient temperature.

(5) Above and beyond the two problems noted above, no additional problems occurred on any of the other tests.

1.2.5 Special Infrared Studies

To support the other tasks of Saturn Linear Integrated Circuit Reliability Test Program, Motorola initiated a short study to determine the value of infrared radiometrics as a tool for the reliability evaluation of linear integrated circuits.

The primary area of interest in this study was the investigation of temperature gradients along the surface of the integrated circuit die while the device was operating under the electrical stress conditions used in the Saturn Reliability Test Program.

A Barnes Engineering Model RM2B infrared radiometric microscope was procured from Barnes Engineering Compnay. An infrared calibration source, Model RM121, specimen heater Model RM123 and Control Unit Model 23 TC121 were also procured. This equipment was procured on rental basis from Barnes Engineering. The RM2-B infrared radiometric microscope is equipped with a germanium immersed uncooled thermistor detector. The sensitive flake is 0.05 mm square. The optical gain of the immersion lens is 20. The optical pass band of the system extends from 1.8 to 22 microns. The microscope was delivered with a 36X objective lens which gave infrared spot size of approximately 0.0014 inch and 360X visual magnification. The integrated circuit chosen for the test vehicle in this study was the MC1530F.

1.2.6 Results of Study

The temperature readings made on devices tested indicated the mean temperature variations across the die shown in Table 1-VIII.

TABLE 1-VIII
OBSERVED TEMPERATURE GRADIENT WITH RESPECT TO DISSIPATION LEVEL
MC-1530F

Dissipation (mW)	Mean Die Temperature Differential (°C)	Mean Temperature at Center of Die (Sta. 39) (°C)
100	4	55
300	4	65
500	9	93
600	13	111
700	18	122
800	23	155.5

At dissipation levels above 300 milliwatts, the maximum temperature was observed at the common collector output transistor (as expected) and/or in the silicon isolation junction region. The minimum temperatures were observed in the regions of the input transistors. The observed temperature indicated that the major portion of the dissipation at the higher power levels was concentrated in the common collector output transistor, corroborating the results of the circuit analysis.

The mean temperatures at the center of the die were plotted as a function of the power dissipation as shown in Figure 1-1. The maximum and minimum temperature curves were plotted from the mean temperature differential data shown in Table 1-VIII. If thermal impedance is defined as the slope of the linear region of the temperature curve representing the center of the die, we find this 200°C/watt for the device operating in this configuration. This value of thermal impedance agrees closely with data obtained on the package from other sources.

Based on this study one must conclude that, from the standpoint of determining electrically induced thermal stress concentrations in integrated circuits, the usefulness of infrared radiometrics as a direct measurement tool is limited by the following factors:

(1) The emissivity of each target area must be determined precisely. This is at best a laborious process in a circuit of modest complexity.

(2) The sensitivity and resolution of the equipment must be such that small differences in temperature in adjacent areas can be detected. Since in general these areas will have different values of emissivity, the ability to determine the emissivity precisely is of paramount importance and in practice may be the limiting factor in determining equipment resolution.

As shown by this study, neglecting errors, the maximum temperature differential across the MC-1530F die was 4° at power levels of 100 and 300 milliwatts, even though under the 300-milliwatt test conditions the power density in the output section of the device is approximately five times greater than the power density in the input section.

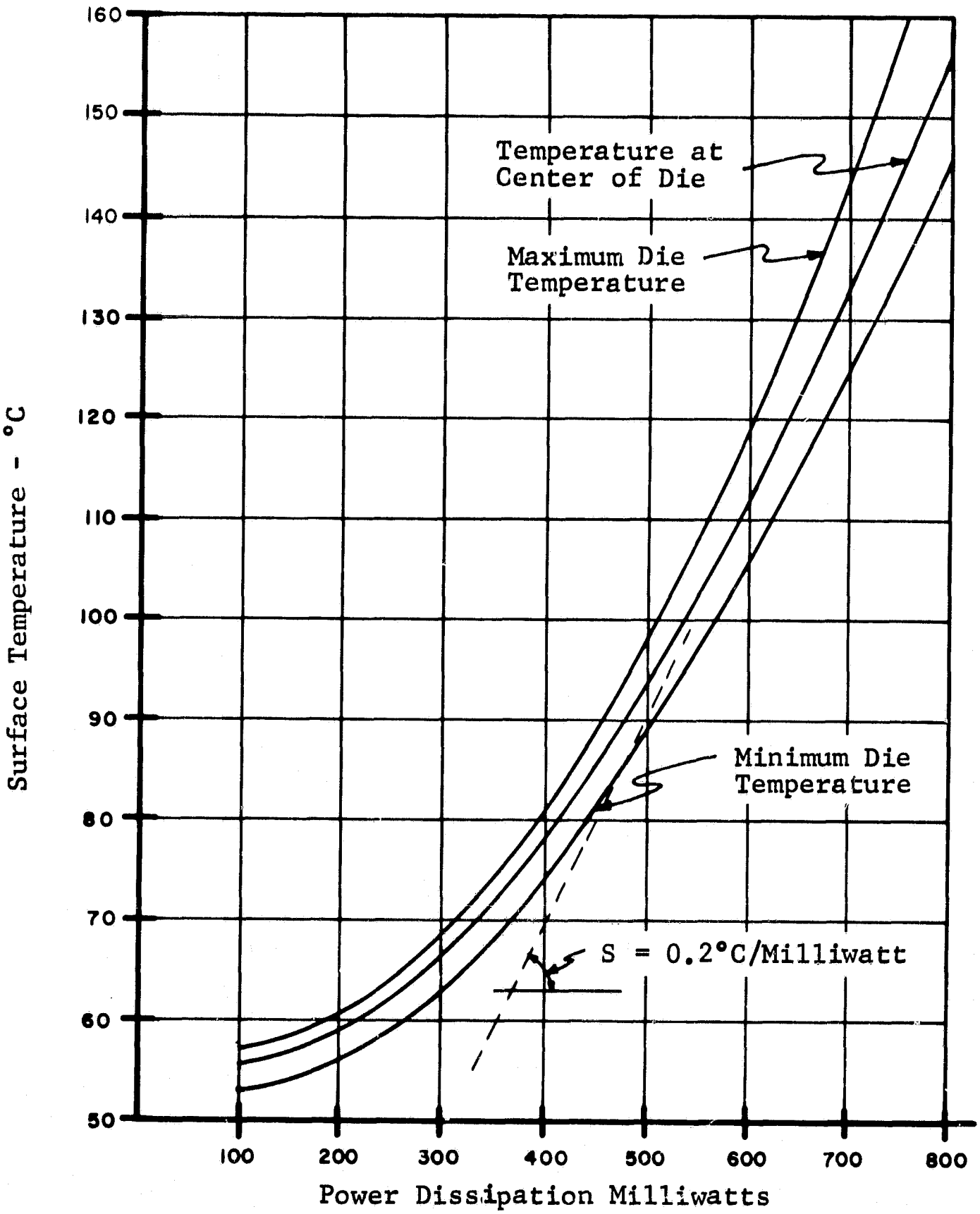


Figure 1-1. Surface Temperature vs Power Dissipation at T_A = 25°C for the MC1530F

(3) Procedures must be developed to facilitate rapid scanning, without loss in precision or resolution, to reduce the time spent in taking data.

1.2.7 Other Special Tests

1.2.7.1 Power Step Stress Test With High-Low Temperature Parameter Measurements

At a meeting which took place at the NASA Largely facility shortly after the contract was awarded, Motorola was asked to perform a special series of tests to determine whether or not potential life test failures would be more quickly detected by measuring high (T_A = 125°C) and low (T_A = -55°C) temperature parameters as well as those agreed upon at room temperature. It was decided that the answer to that question could best be determined by subjecting survivors of the mechanical stress sequence to a repeat of the power bias step stress tests except that the A_{VOL}, A_{dd}, I_{in}, and V_{io} parameters were tested at the temperature extremes. To this extent, six of the SN-526 and ten of the MC-1530F circuits were used. The test stressing technique was identical to that used in the power bias step stress test. The data does indicate that some circuits may fail faster if the high temperature measurements criteria are specified. These data, however, are not conclusive, and further effort should be expended in investigating this technique.

1.2.7.2 Accelerated Mechanical Step Stress Testing

Two special series of step stress tests were performed as a part of this test program to explore the physical limitations of these circuits and package combinations. A description of these test sequences and their results would show that:

(1) Ten samples of each type were subjected to 10 impact shocks of 3,000 G and 10,000 G (0.2-millisecond duration) each of the X_1, Y_1, and Z_1 stress axes. Parameter readings were made after the 3,000-G and 10,000-G steps. The SN-526, MC-1530F, and MC-1525G survived all stresses with no observed failures. Four MC-1519G's failed the 10,000-G step and subsequent failure analysis found this to be attributed to chopped bonds breaking after repeated stresses of these levels.

(2) Ten samples of each part were subjected to a vibration variable frequency step stress test, performed according to the method outlined in Mil-Std-750, Method 2056, except that the applied force was varied at each step from 30, 50, 70, 80, 90, and 100 G. The TO-5 circuits had package failures occurring at the 50-G step for the MC-1519G and at the 70-G step for the MC-1525G. This failure mechanism had been observed in other TO-5 packages tested in this manner and was explained as a function of a critical force frequency relationship that created a destructive resonant force in at least one package lead in four of the MC-1519G's TO-5 packages and five of the MC-1525G's.

No other failure mechanisms were detected. This failure mechanism was attributed to the package and has not been seen at the lower stress levels normally required to evaluate integrated circuit products.

1.3 OBSERVATIONS AND RECOMMENDATIONS

As a result of this test program, many observations have been made concerning the reliability of these linear circuits. In this section these observations will be analyzed.

1.3.1 Recommended Screening Procedure

The purpose of a reliability screening procedure is to improve the reliability of a given lot of devices by removing those units which have a high probability of failing prematurely with respect to the expected life of the part. The design of such a procedure required a thorough understanding of the mechanisms which lead to such early failure, the stresses which will accelerate these mechanisms, and an understanding of the random variables associated with the performance of the procedure.

The MC-1519G is a good example of the problems faced with designing good screens. It had a definite intermetallic problem because gold wire leads and the aluminum metallization were used. It also displayed evidences of surface inversion (channelling) on the monolithic chip. In addition, lead bonds opened when subjected to impact shocks of 10,000 G. To screen for surface inversion, a high voltage bias and a junction temperature as high as 175°C is desirable. Yet, if the device is subjected to 175°C for long periods of time, intermetallic compounds will form and reduce the bond strength. While decreasing the failure rate of the survivors for the channelling phenomenon, the lifetime of the device would also be reduced more drastically because of the intermetallic effects. Clearly, a trade-off must be exercised and a functional test with the ambient temperature restricted to 125°C is a suitable compromise; but the junction temperature must be considered when designing the burn-in screening test. This would appear to be enough of a problem by itself but to design an effective screen test for reducing the likelihood of a lead bond opening is not an easy task. The equipment used to generate an impact shock of 10,000 G for 0.2 millisecond requires that the circuit be mounted on a shock plate and dropped approximately 8 feet to the shock pad. The equipment is expensive

and the technique is slow and unsuitable for production work. Other approaches such as the use of "blow guns" are undesirable because of the uncontrolled nature of their applied stresses. They are applicable only to particular types of packages and they can cause damage to the package under test. In this program neither the temperature cycling step stress test nor the centrifuge test correlated with the impact shock test.

Another factor that must be taken into consideration when burn-in test circuits for operational amplifiers are designed is that these circuits are extremely sensitive to misapplication of voltages. For instance, when each catastrophic MC-1530F failure was analyzed, two were found to have open metallization in regions not biased or connected during the stress testing. The same effect was observed for SN-526 failures. This effect has also been observed on other reliability test programs for operational amplifiers. The cause of this susceptibility to overstress seen in operational amplifiers which may not be found in other amplifiers or digital circuitry is usually attributed to two factors. The first factor is uncontrolled high frequency oscillation found in devices that have extremely high f_T when sufficient feedback control is not used. The second factor is related to the nature of the output portion of the operational amplifier's circuit where transistors are used with no current limiting resistors in either the emitter or collector leads. This circuitry is normally able to prevent thermal and electrical runaway when the correct bias is applied to each terminal and the proper power supply sequence is used.

From this program a screening procedure consisting of the sequence shown in Figure 1-2 of these tests and examinations can be recommended.

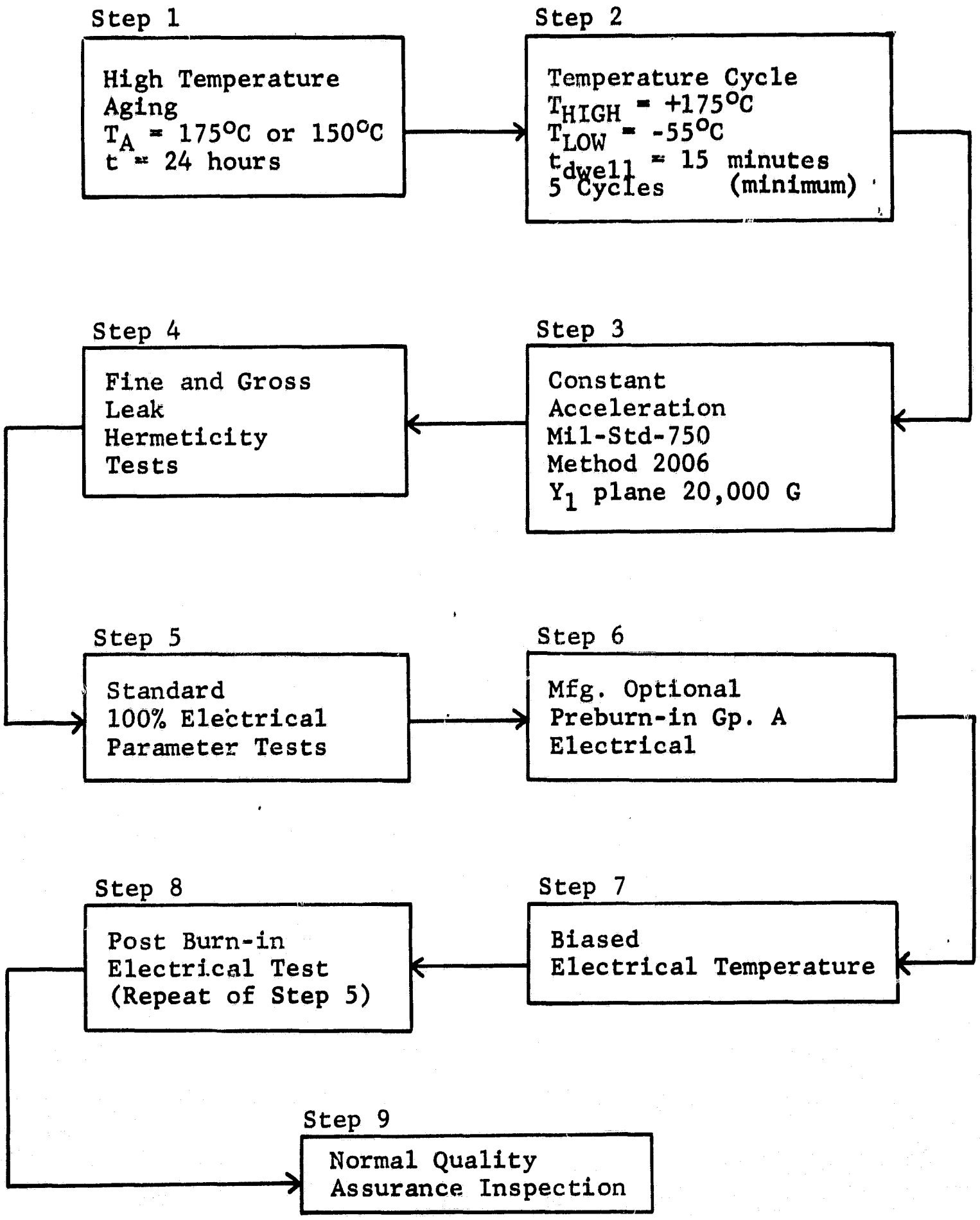


FIGURE 1-2. Recommended Reliability Screening Procedure

1.3.1.1 Fine and Gross Leak Test

Hermetic seal tests per Mil-Std-202, Method 112, Condition C, Procedure III, at a sensitivity of 10^{-6}, followed by a gross leak check such as defined under Mil-Std-202, Method 112, Condition A for metal packages or a penetrant dye test for all ceramic packages is recommended. The penetrant dye test has proven to be a more reliable indicator of seal integrity for ceramic packages than the tracer gas tests in these leak ranges if suspect devices are opened and examined microscopically. The all-ceramic package generally transmits sufficient light for this test to be nondestructive in that infusion of the marker dye along seal voids can be detected by observing the test specimen under proper lighting.

A recommended procedure for this penetrant dye test follows: In this test the devices are immersed in a penetrant dye (Magnaflux type SKL-HF or equivalent) and pressurized at 60 psig for 1 hour. After that period the devices are removed and subjected to a cascaded series of agitated acetone rinses to remove the dye from the surface and edges of the package. The package is then placed in front of a high intensity, point source, white illumination such that the translucent ceramic package is between the light source and the observer. Seal leakage is determined by a pinkish or red appearance of the package. Defective devices are removed at this point.

The penetrant die test can be used to confirm leaks indicated by other test methods on opaque packages by decapping the device and microscopically examining the interior of the package for traces of dye.

1.3.1.2 Burn-In

This test has been shown to be the most effective means of reliability screening for surface related phenomena. Time and dissipation levels must be negotiated for each individual device and product family. Factors which should be considered are normal operating voltage, dissipation level and system ambient temperature. Experience has shown that 250 hours at junction temperatures on the order of 150°C is sufficient to give effective screening against channelling, but whether channelling will be the dominant failure mechanism at use condition is undetermined.

1.3.2 8000 Hours Predicted Life Reliability

One of the requirements of this program was to predict the reliability of these circuits after 8000 hours of typical operation. This goal was not achieved for this requirement is actually beyond the scope of experiments of this nature. There are realistically only three ways to achieve this purpose. The first is to collect sufficient samples and test for 8000 hours at desired stress levels and collect data at that point from which the estimated failure rate could be calculated. However, there was insufficient time available during the duration of this program to permit this technique to be considered. A second approach would be to estimate the failure rate at many accelerated stress conditions from tests performed for shorter periods of time and then extrapolate this data to 8000 hours. Techniques of this sort normally assume a constant failure rate even though this fact is not generally true. This technique requires relatively large sample sizes, particularly at the lower stress levels, if the quality of the parts being accepted is relatively good. In this program the three life test samples (i.e., T_A = 25°C, 125°C and p_d = 300 mW T_A = 125°C)

did not have enough samples to properly estimate the failure rate for any circuit at 25°C or for either operational amplifier sample at the higher temperatures. No failures occurred in eight of the twelve test cells in which operational life tests were conducted more than 1000 hours. A third approach considered was to use any observeable parameter drift to predict 8000 hours failure rates. This approach is also laden with logical traps for one must assume repeatability within production lots and that observable degradation function of populative stability not device stability, thereby permitting the use of mathematical transformation of data when required for using statistical distributions and methods of prediction. This technique could not be applied because the stability of three of the parts was such that any observed parameter variation of degradation was less than the normal equipment variability further measurements.

The ideal technique that Motorola had planned to employ would have utilized the best features of methods two and three. However, inasmuch as an analysis of the data at the conclusion of the test program showed that the required characteristics were not present, no attempt is made to predict this factor for any test circuit in this program.

1.3.3 Recommendations for Future Effort

When the results of this program are examined in the light of the progress that the industry has achieved in the design and fabrication of more versatile and complex linear integrated circuits since the inception of this program, it becomes apparent that there are areas where additional effort could profitably be expended in future reliability programs. The following items are presented so that they may be given consideration in the planning of future reliability programs for linear integrated circuits.

1.3.3.1 PNP Transistors as Circuit Elements

A study of the reliability of linear integrated circuits using lateral PNP transistors and substrate PNP transistors in their circuitry was made. Many newer circuits are being designed to include the use of these components in the critical design stages. It is assumed that these circuits may differ somewhat in their reliability characteristics over the NPN circuits now tested. A program designed to explore PNP circuit reliability could be of value, if it studies the operational life characteristics of the device.

1.3.3.2. Functional Versus Nonfunctional Testing

One facet of the reliability variable not explored on this test program was the relative effectiveness of the functional test as opposed to the nonfunctional biased test. In past reliability analysis of digital gates, the data has shown that the static biased operating life test is as effective as the functional test. This postulate has not yet been verified for linear integrated circuits and the data available from other programs does tend to question its validity. In any event, a test program exploring in depth these questions would contribute significantly to the knowledge of linear integrated circuit reliability.

1.3.3.3 Reliability Prediction and Burn-In

This item should be incorporated into any program designed to explore the functional characteristics noted in item 2. It is a natural addition to any such program but to do such a program successfully, a very careful statistically designed program must be proposed that can be expected to show failures, the rate of change of failure rate, the nature of each failure, proportionality of these failures

when related to changes of stresses, and an analysis of parameter data that would show if reliability discriminates do exist for these circuits. Such a program would require a large number of samples of a single manufacturing process (in excess of 1000), enough preliminary distribution data to support the program design concept, and a smaller number of samples from other circuit electrical configurations, from other manufacturers and utilizing other manufacturing processes to determine the validity of the results of the major matrix. A properly designed program would place a high value on analysis or circuit functioning, electrical biasing techniques, electrical measurement techniques as well as the physical nature of device failures.

1.3.3.4 High Temperature Parameter Measurements

This subject was touched on only briefly in this program, but the data that was obtained shows that while the MC-1530F was the most stable when measured after being stabilized at room temperature, some circuits did exhibit variability and degradation when tested at the 125°C ambient temperature. The question "what does this mean?" was not explored in depth but should be in some future program.

1.3.3.5 Linear Circuits and Dielectric Isolation

Many circuits are being developed in dielectrically isolated integrated circuits. The future in this field does seem to be related quite closely to those applications requiring high radiation tolerance, but a knowledge of the general reliability characteristics of a dielectrically isolated linear integrated circuit would benefit all potential users of these circuits.

1.3.3.6 Study of Maximum Current

As the trend in integrated circuits is toward the smaller geometries, the more densely packed circuitry and the higher powered linear circuits, the mating of these elements is inevitable. Therefore, data must be gathered that can contribute toward evaluating the potential reliability of the circuit die itself. This could be accomplished by a physical study of the basic materials, the methods of processing the methods of interconnections, the limitations of active element geometries, as well as the reliability of the circuits.

1.3.3.7 Plastic Integrated Circuits

Within a very short period of time, plastic integrated circuits will be gaining acceptance in many military and space applications. Programs designed to explore the plastic systems currently in use would be instrumental in preparing the industry against the acceptance of the consensus of the popular clique for and against the use of plastic systems. An evaluation of this product must include a variety of plastic materials most likely to be used in the future, a variety of manufacturers and should include or evaluate the repeatability of each process.

SECTION II

2.0 TEST DEVICES

2.1 DESCRIPTION OF TEST DEVICES

Four different integrated circuit amplifiers were selected for this program. The three circuits manufactured by the Motorola Semiconductor Products Division were the MC-1519, MC-1525, and MC-1530. That manufactured by Texas Instruments, Inc. was the SN-526A. These circuits differ in performance characteristics, manufacturing processes and methods of packaging (Table 2-I). Other simplified characteristics are found in Table 2-II.

TABLE 2-I
COMPARISON OF TEST DEVICES

Device Type	Type of Amplifier	Manufacturing Process	Type of Package
MC-1519G	Differential	Monolithic PNP and Monolithic NPN with Thin Film Resistors	10-lead TO-5 Package
MC-1525G	Differential	Monolithic with Diffused Resistors	10-lead TO-5 Package
MC-1530F	Operational	Monolithic with Diffused Resistors	10-lead alumina Flat Package (1/4 in x 1/4 in)
SN-526A	Operational	Monolithic with Diffused Resistors	10-lead welded Flat Package (1/4 in x 1/8 in)

2.1.1 Differential Amplifier--MC-1519

The most important feature of a differential amplifier is its ability to amplify signals that are differential to its inputs, while rejecting signals which are common to its inputs. Common-mode signals not only are not amplified but are attenuated in a good

differential amplifier. A high impedance common to the emitters of the input transistors is necessary to obtain this characteristic. In the MC-1519, this high impedance is achieved by using a transistor operating in class A as a current source at this point (Figure 2-1). Design of this device permits its use in either the Common Emitter (CE) mode (Figure 2-2) or the Common Collector (CC) mode (Figure 2-3).

TABLE 2-II
DEVICE TYPICAL CHARACTERISTICS

Device	Lead Wire	Lead Bond Technique	Metallization	Monolithic Chip
MC-1519G	Gold	Stitch	Aluminum	Epitaxial Diffused
MC-1525G	Gold	Stitch	Aluminum	Epitaxial Diffused
MC-1530G	Aluminum	Stitch	Aluminum	Epitaxial Diffused
SN-526A	Gold	Ball	Aluminum	Triple Diffused

The MC-1519 is a monobrid circuit which has two dice housed in one package (Figure 2-4). One die is a compatible integrated circuit having three NPN transistors and two Nichrome thin film resistors (Figure 2-5a). The other die is a monolithic integrated circuit having two PNP transistors (Figure 2-5b). Interconnections between the die and the posts of the header are shown in Figure 2-4. The devices procured for this program are housed in the TO-5 package.

2.1.2 Differential Amplifier--MC-1525

Motorola's differential amplifier series, MC-1525 through MC-1528, are designed to provide system and circuit engineers with greater flexibility than was previously available in monolithic integrated circuitry. By using multiple biasing connections and compatible NPN-PNP amplifier cascades, a wide range of gain, impedance,

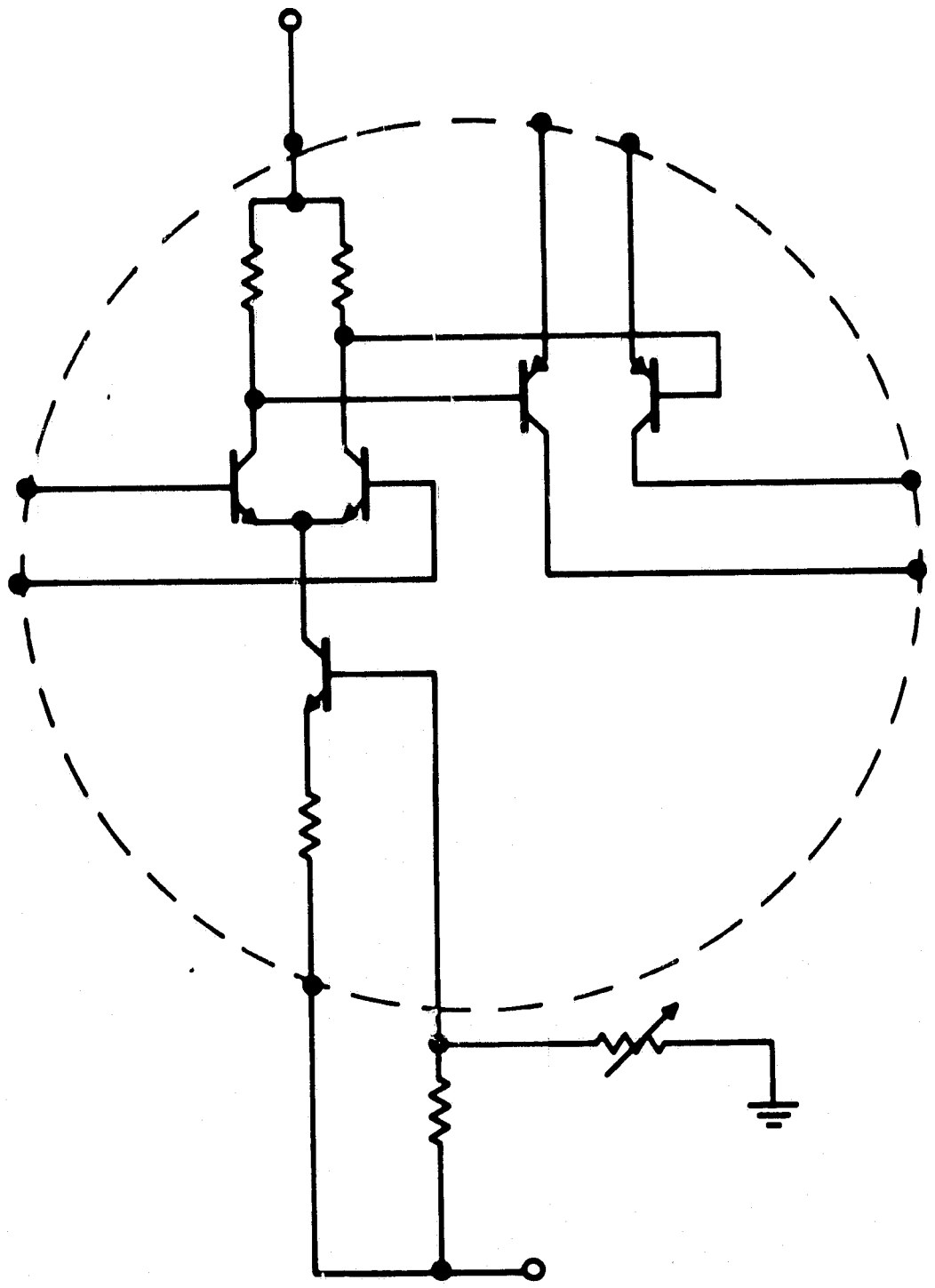


Figure 2-1. Schematic Diagram of MC-1519

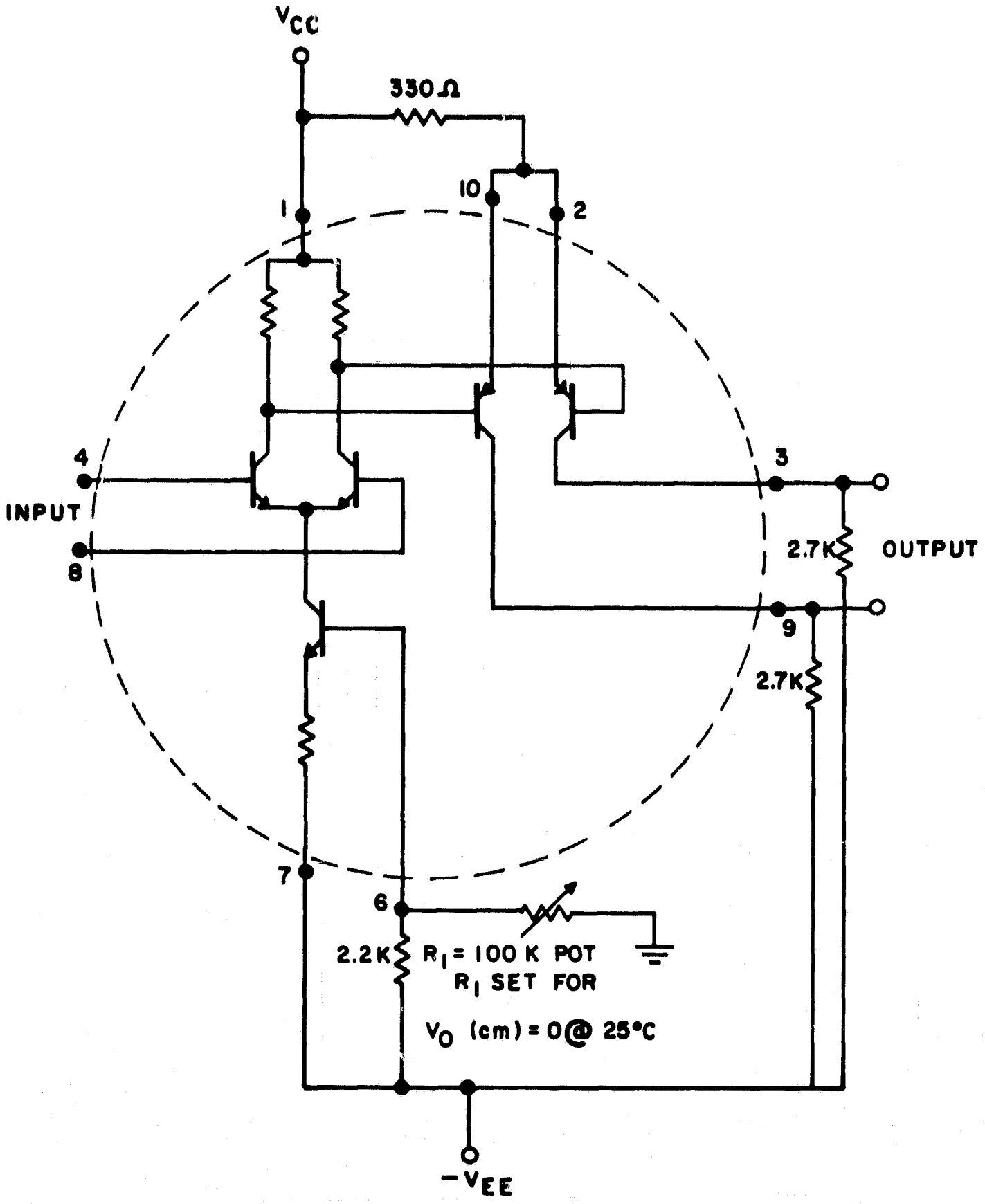


Figure 2-2. MC-1519 in Common Emitter (CE) Mode

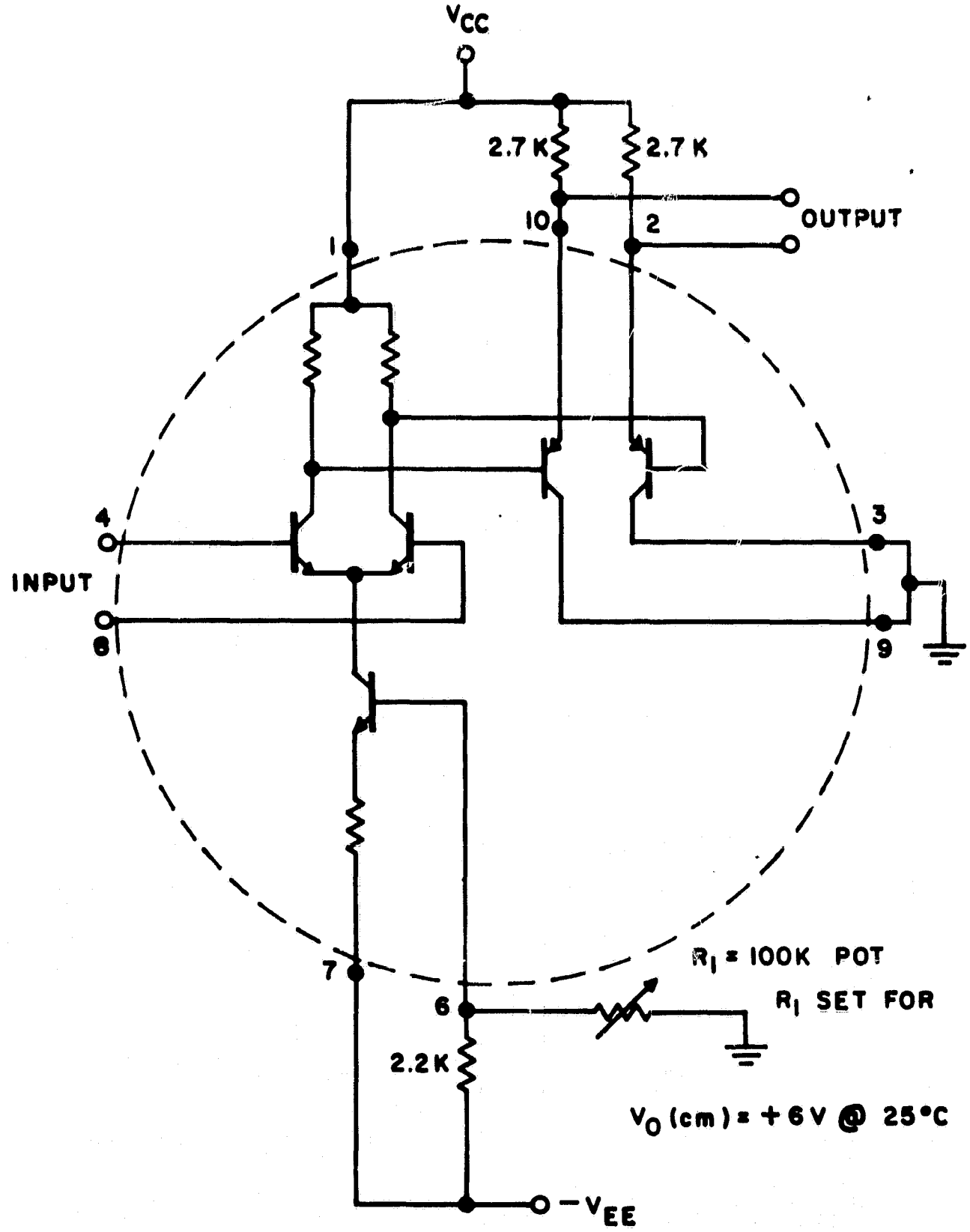


Figure 2-3. MC-1519 in Common Collector (CC) Mode

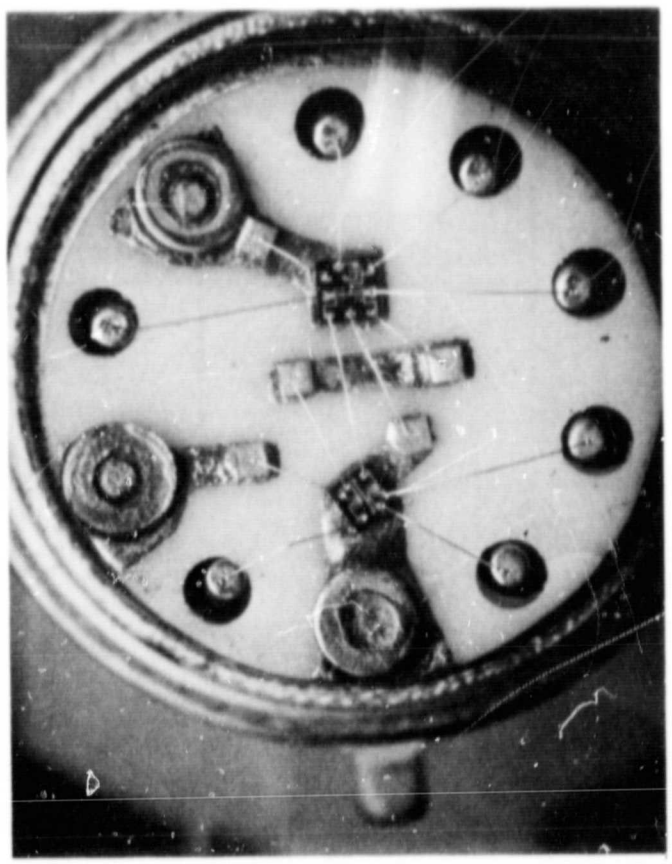
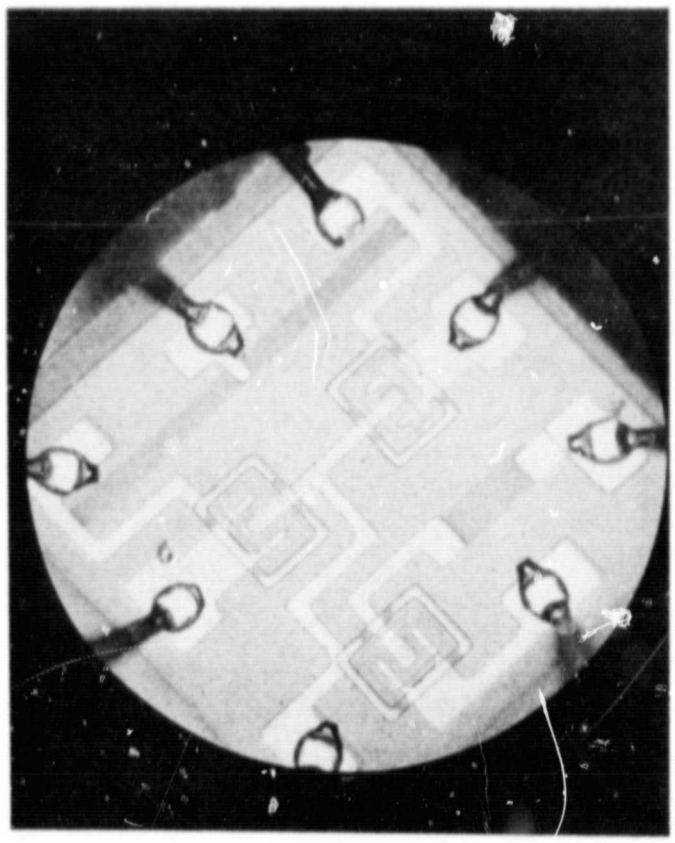
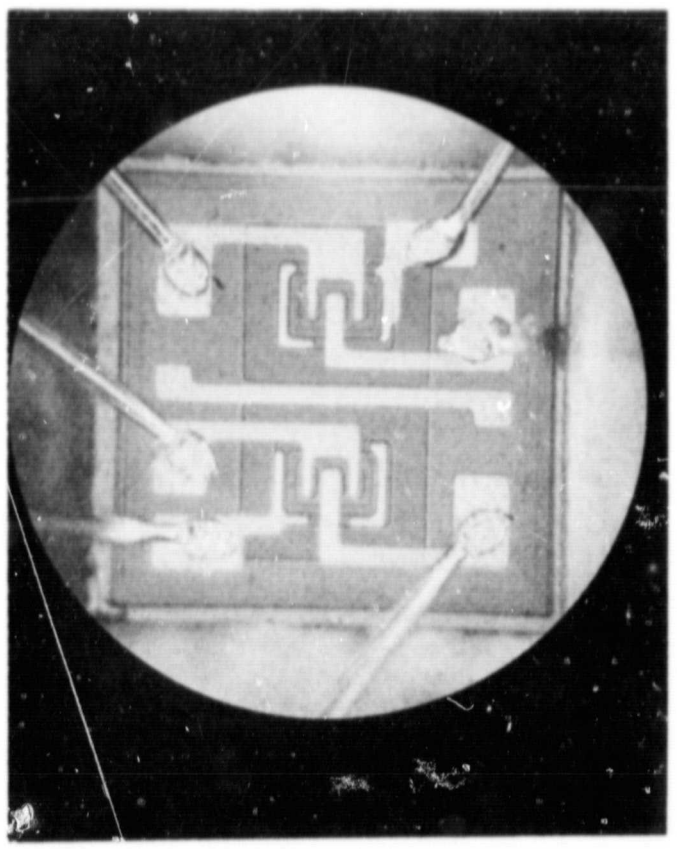


Figure 2-4. Photomicrograph of the MC-1519 Circuit



(a) Compatible Circuit Die



(b) Monolithic Circuit Die

Figure 2-5. Photomicrograph of the MC-1519 Dice

power supply voltage and current drain constraints may be satisfied. The circuits incorporate diode temperature compensation and are geometrically oriented for good tracking. The MC-1525 is the member of this series that has been selected. Like the MC-1519, this device employs an active current source at the emitters of the input transistors to meet the requirements for a good differential amplifier (Figure 2-6).

The four resistors in the emitter of the current source transistor may be connected in a variety of ways. The resultant effective resistances, (R_e), in conjunction with a given value of V_{EE} make provision for selection of a current level appropriate to the intended use of the device (Figure 2-7).

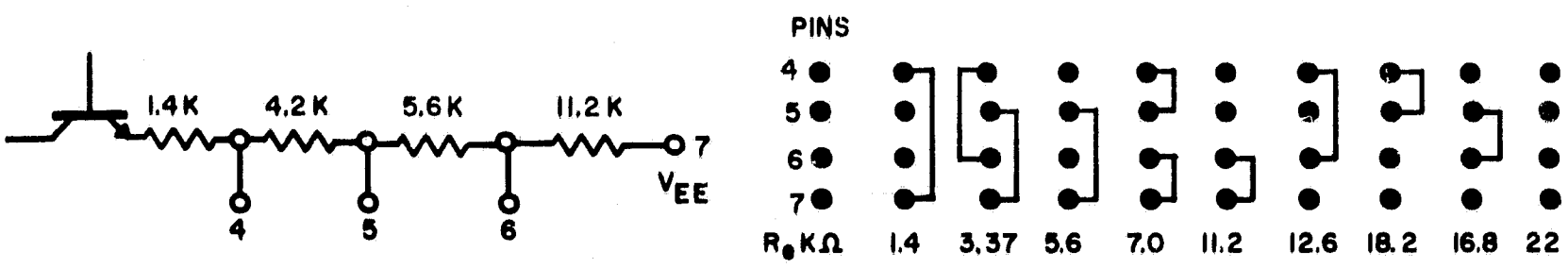


Figure 2-7. Effective Resistances in Current Source Emitter of MC-1525

The MC-1525 is a monolithic integrated circuit having diffused resistors (Figure 2-8). The devices procured for this program are housed in the 10-lead TO-5 package.

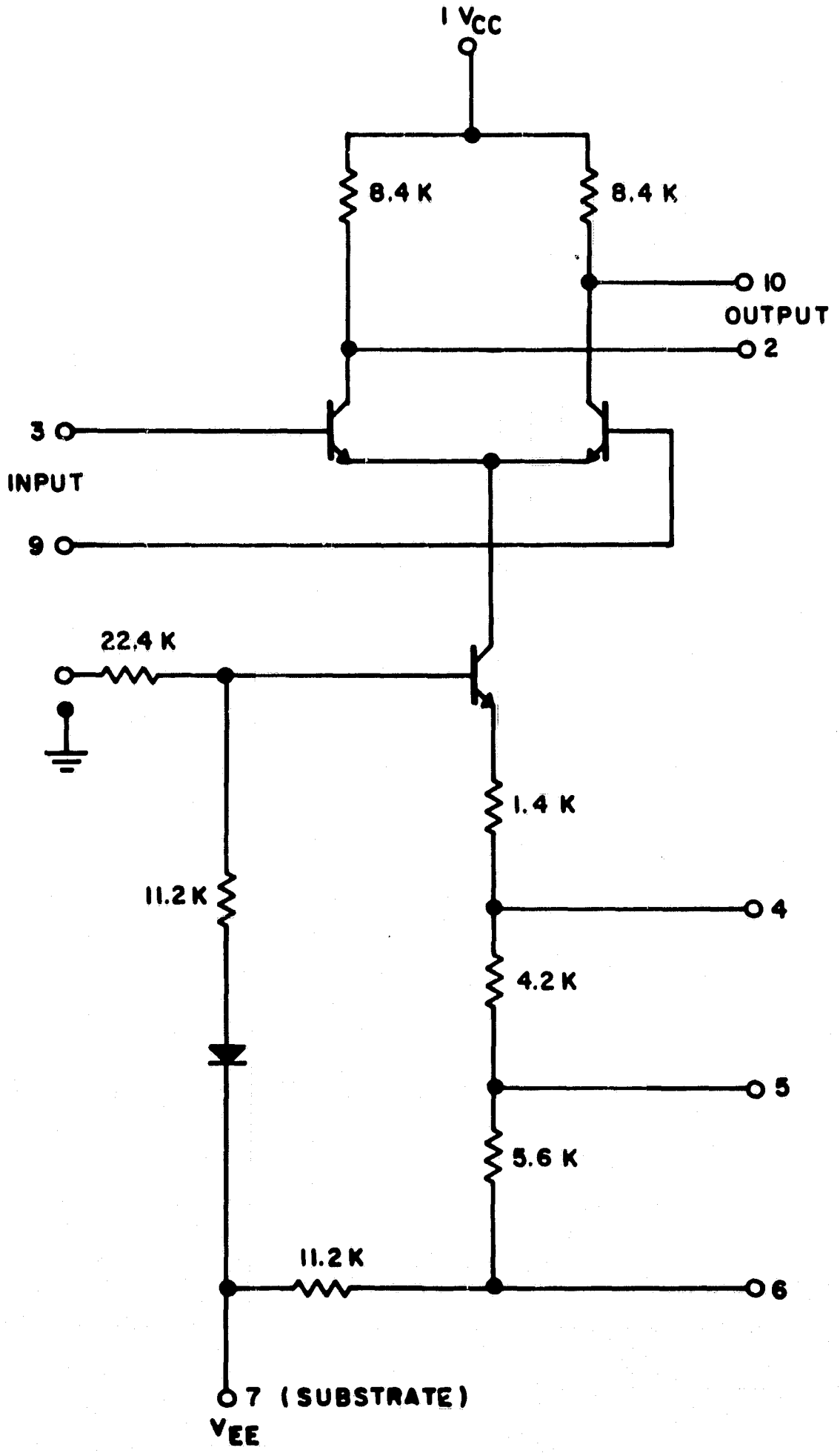


Figure 2-6. Schematic Diagram of MC-1525

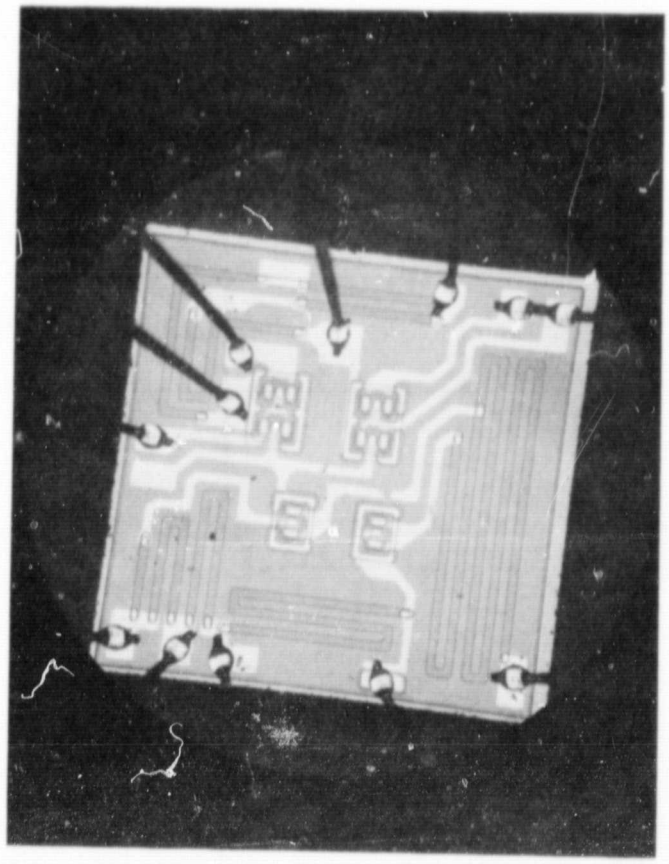


Figure 2-8. Photomicrograph of the MC-1525 Die

2.1.3 Operational Amplifier--MC-1530

Such advantages as low offset voltage and current, excellent temperature tracking, increased reliability, small size and reduced cost make the integrated circuit operational amplifier more attractive than many discrete operational amplifiers now in use. On the other hand, many discrete operational amplifiers are of such high quality that their performance cannot yet be duplicated in the state of the art of monolithic integrated circuit technology. For many operational amplifier applications, such as that of a summing amplifier, an integrator, a dc comparator or a transfer function simulator, the integrated circuit provides a reasonable compromise between desired performance and cost. Motorola's Operational Amplifiers, MC-1530 and MC-1531, are high performance, all-diffused integrated circuits, either of which may be fabricated from a single monolithic die by appropriate interconnections during manufacture. Like the MC-1525, the circuits incorporate diode temperature compensation. Additionally, variation of the output voltage with temperature is reduced to a minimum because critical dc voltage levels within the circuits are a function of resistor ratios and are not dependent on the absolute values of any resistor or the beta of any transistor in the circuit. The MC-1530 has been selected for this program (Figure 2-9).

The MC-1530 is a monolithic integrated circuit having diffused resistors (Figure 2-10). The devices procured for this program are housed in the 1/4-in x 1/4-in alumina flat package.

2.1.4 Operational Amplifier--SN526A

Texas Instruments' Amplifiers SN-525A and SN-526A are circuits either of which may be produced from a single "Master Slice" by appropriate interconnections during manufacture. The SN-526A has been selected for this program (Figure 2-11). It features

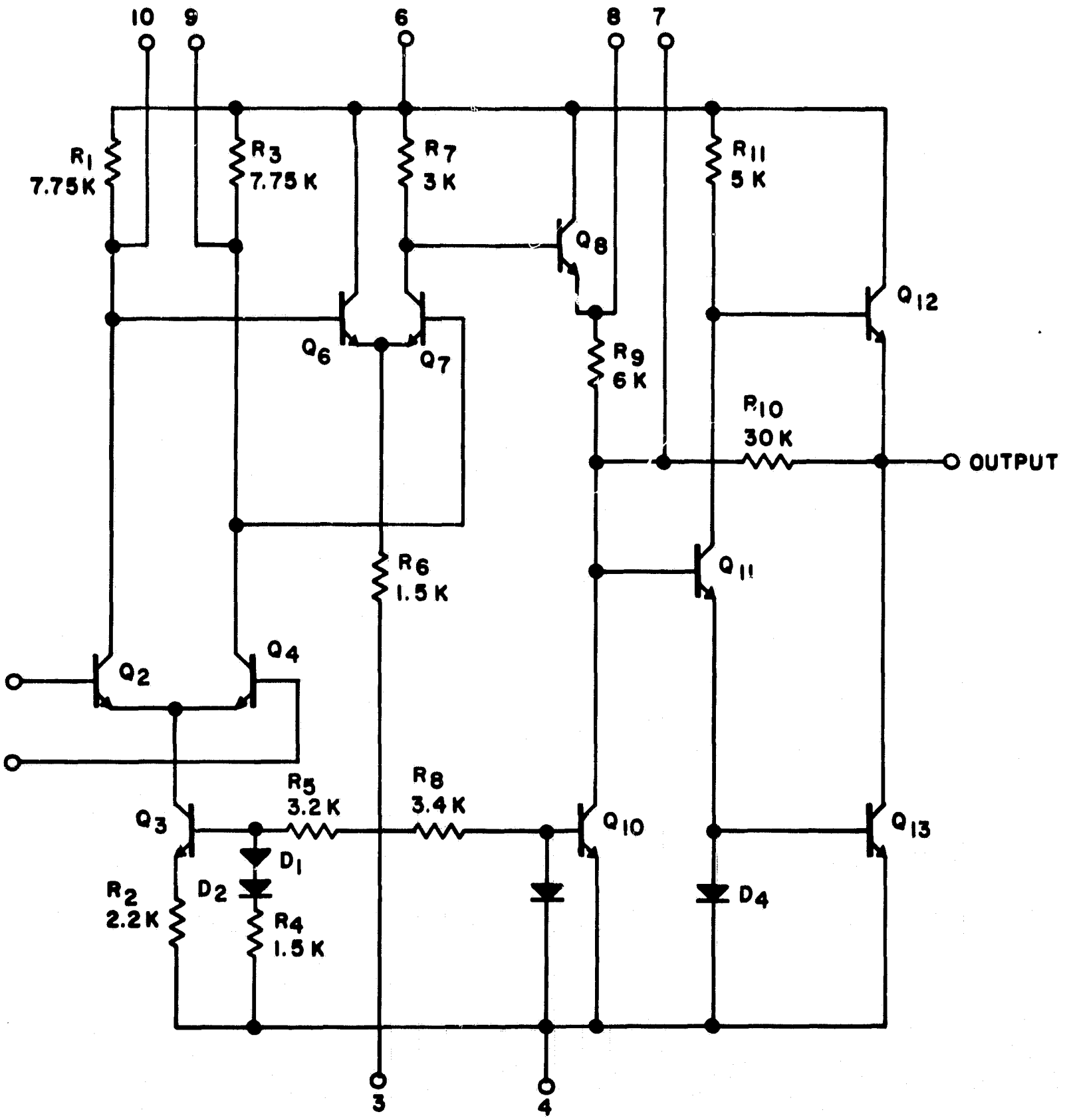


Figure 2-9. Schematic Diagram of MC-1530

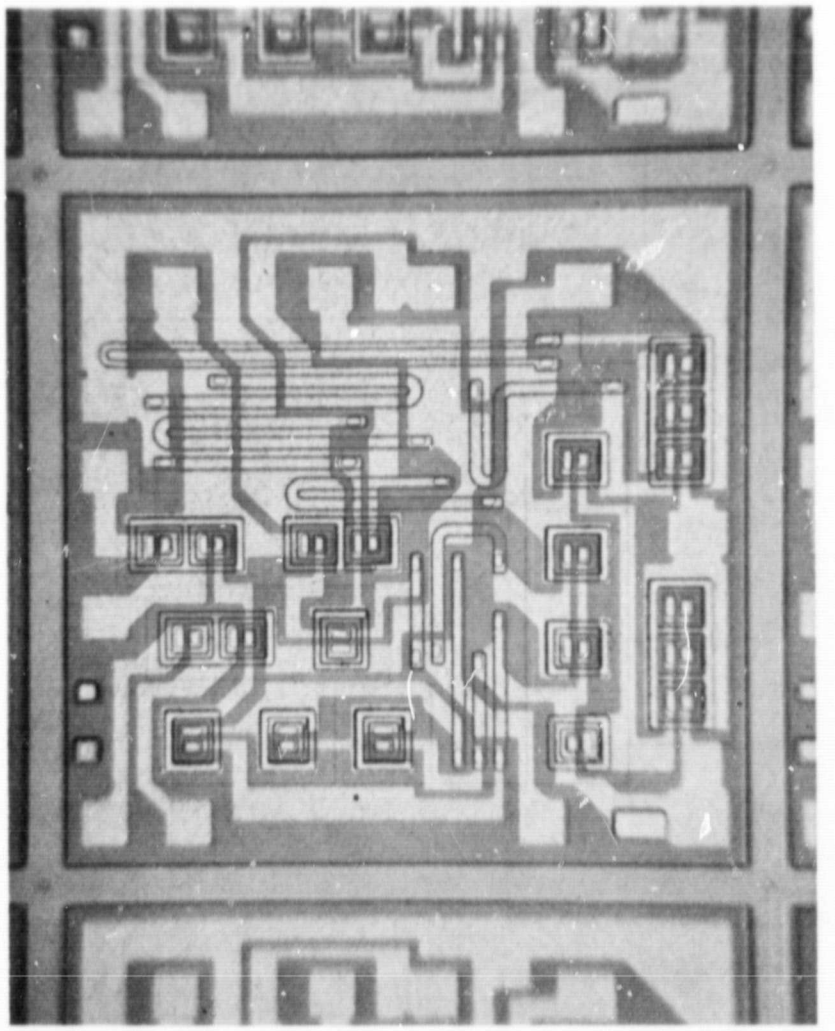


Figure 2-10. Photomicrograph of the MC-1530 Die

5035-4-6

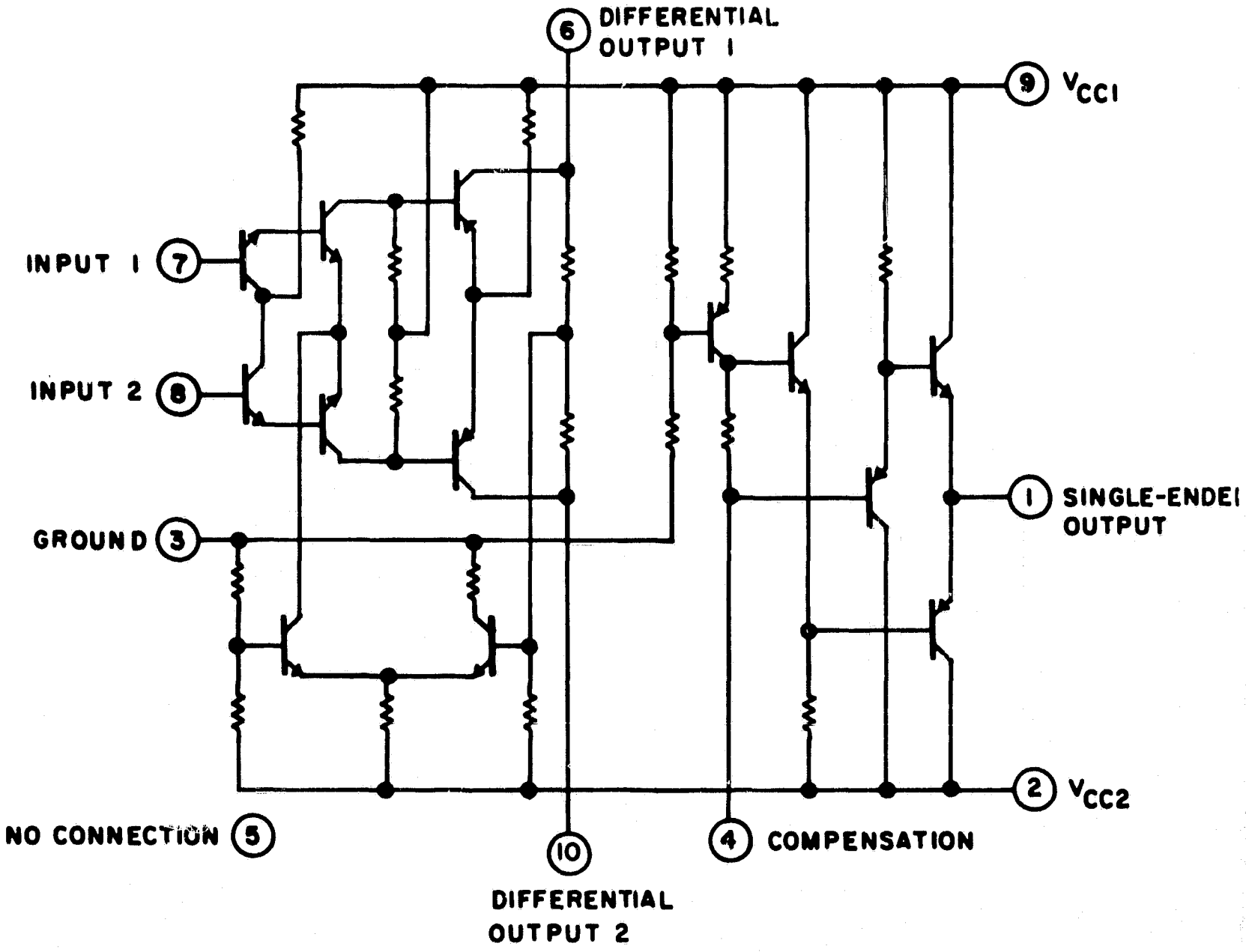


Figure 2-11. Schematic Diagram of SN-526A

Darlington high-impedance differential-input stages and a Class B output power amplifier. Differential amplifier outputs are also provided. These devices are packaged in a 1/4-in x 1/8-in welded package. Photographs of the welded package and the integrated circuit chip are shown in Figures 2-12 and 2-13.



Figure 2-12. SN-526A Package

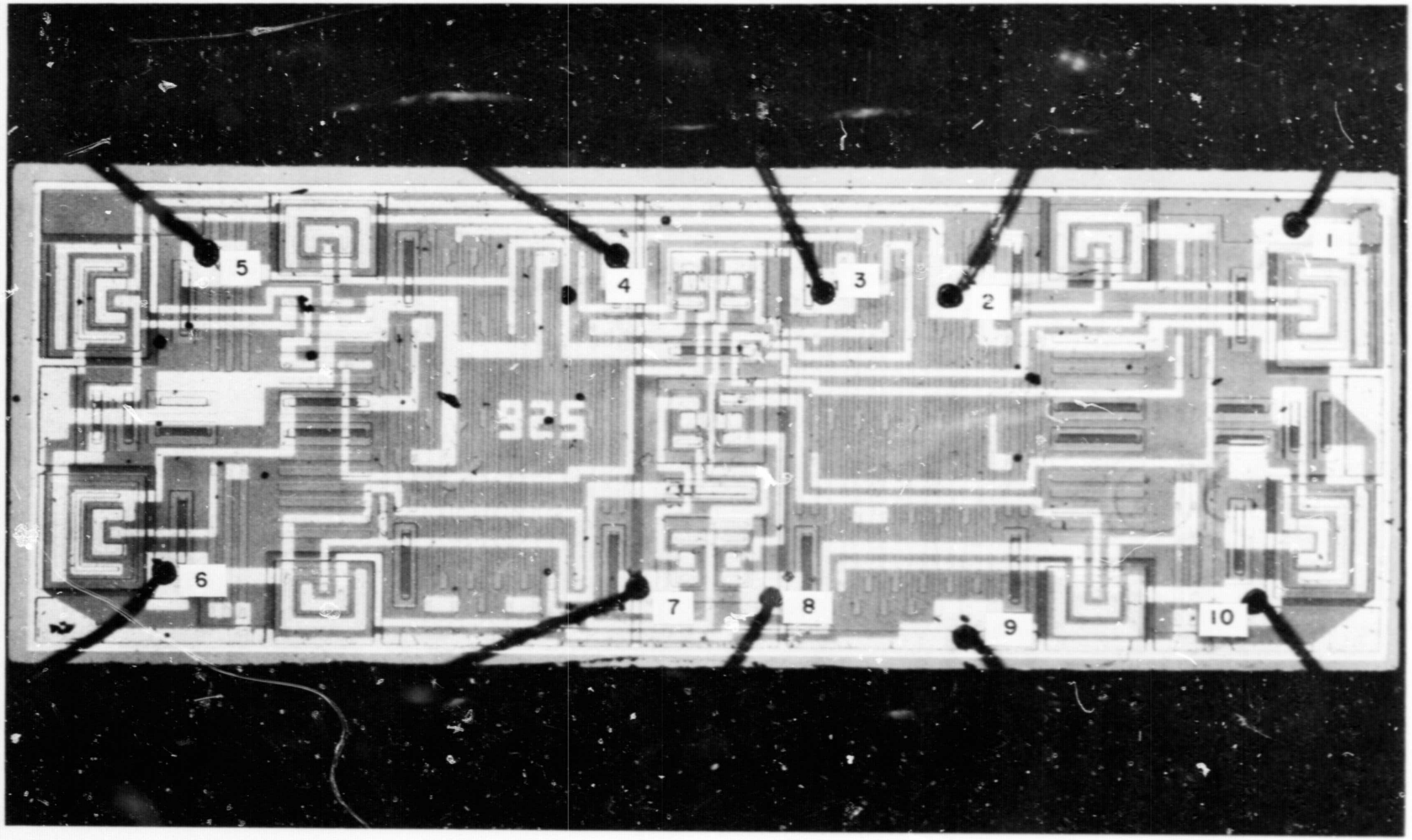


Figure 2-13. Integrated Circuit Die SN-526
Manufactured by Texas Instruments

6669-10-7

SECTION III

3.0 ELECTRICAL CHARACTERISTICS

The parameter characteristics of these integrated circuits are discussed in this section. As will be seen, the measurement definitions are similar for most circuits. The difference of importance are those techniques used to make the measurements. The discussion presented in this section will compare the parameters of each circuit separately, discussing their similarities using tabular and schematic presentations wherever necessary. Distribution analysis is also included to show the relative distributions for each device.

3.1 SPECIAL TEST METHOD REQUIREMENTS BY DEVICE

3.1.1 Differential Amplifier--MC-1519

Figure 3-1 shows the circuit configuration employed in measuring the electrical characteristics of the MC-1519 in the common emitter (CE) mode. This circuit is used in principle for fixing the circuit current for all measurements. An operational amplifier circuit was developed to provide and control the constant current flow through the input stage required in all test measurements. In the measuring circuits described herein, the amplifier symbol Δ is used to designate the circuit as shown in Figure 3-1 with the operational amplifier modification.

3.1.2 SN-526A, MC-1530, MC-1519

In describing the measuring circuits used for these circuits, the amplifier symbol Δ will be defined as the integrated circuit device under test. For those circuits and test requiring

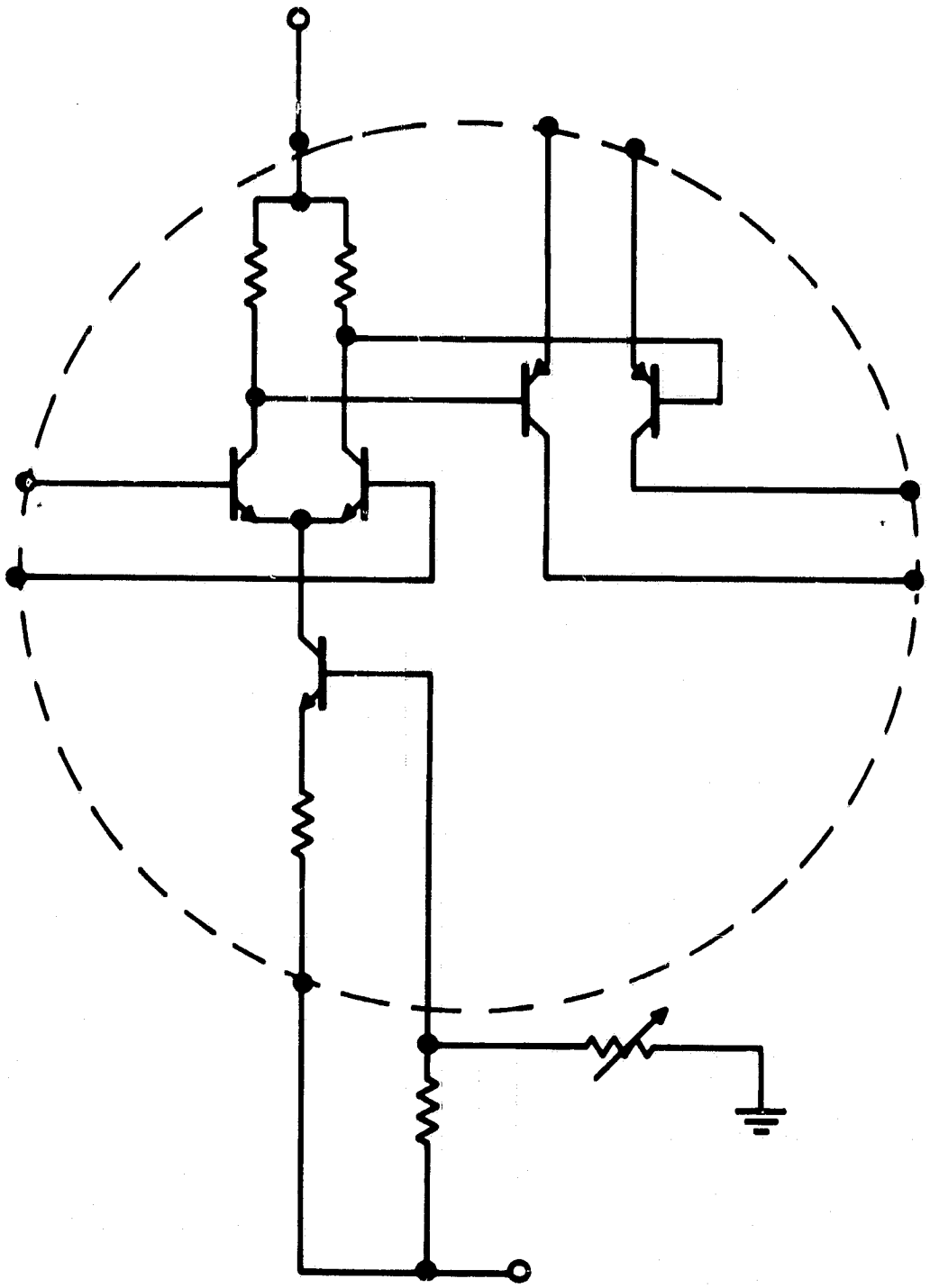


Figure 3-1. Schematic Diagram of MC-1519

roll off capacitors for stabilization, these items are not included in the description of the individual test method.

3.2 TEST MEASUREMENT TECHNIQUES

3.2.1 Input Offset Voltage (V_{io})

The input offset voltage is defined as the dc voltage which must be applied between the input terminals to obtain zero-differential-output voltage for double ended amplifiers, or zero-output voltage referenced to ground for single ended amplifiers. Without this voltage applied, the amplifier becomes unbalanced and the output voltage level will deviate from ground by an amount equal to the input offset voltage times circuit gain and with the opposite electrical polarity. Each amplifier used in this program has a two-sided input thereby requiring a measurement of the input offset voltage.

The technique used for setting V_{io} is essentially the same for all devices. In one device, the MC-1519, the voltage drop was measured across a resistor divider (1/1000) and divided by 1000 to obtain the actual V_{io}. For the other three circuits, the measurement was taken at the input terminals and read directly on a digital vacuum tube voltmeter. The equivalent circuit is as shown in Figure 3-2 for this measurement.

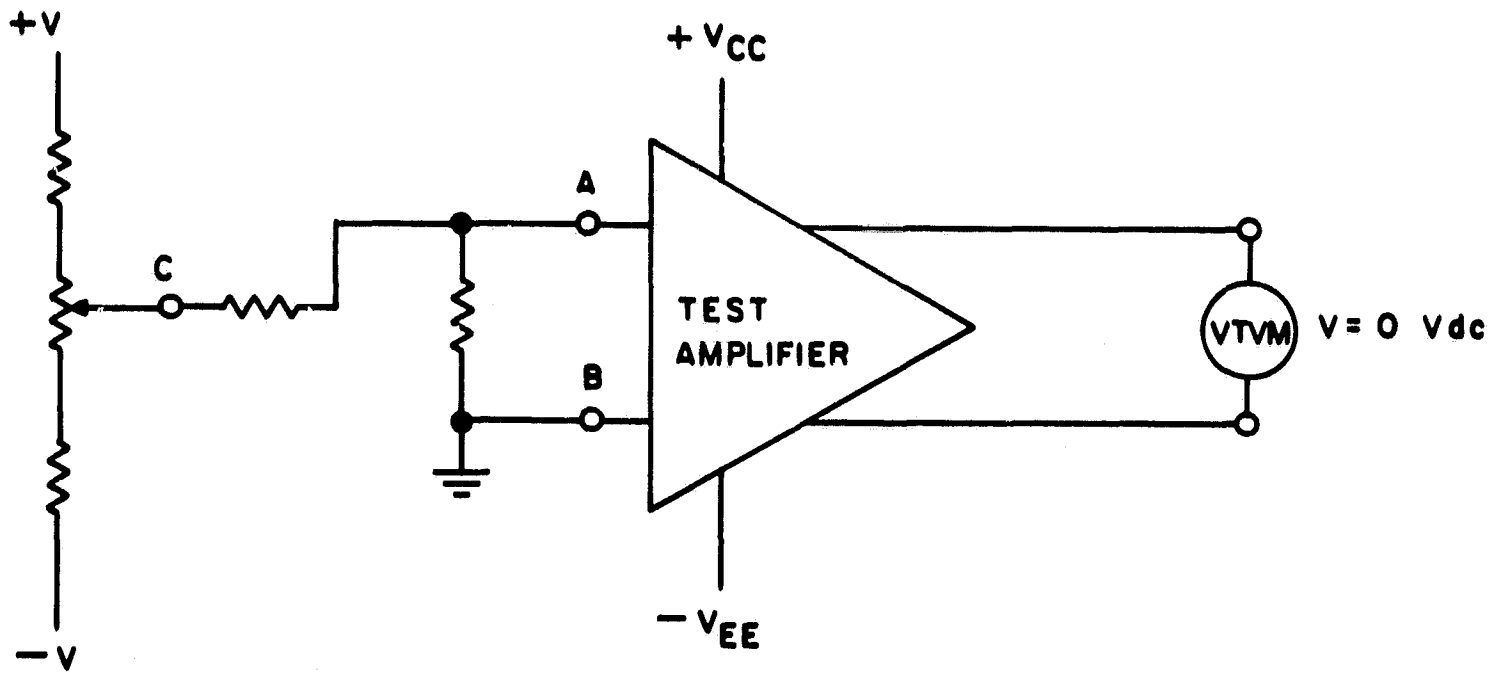


Figure 3-2. V_{io} Test Schematic

V_{io} is measured between points A and B for the MC-1530, MC-1525, and the SN-526A. It is measured between C and B, divided by 1000, for the MC-1519.

3.2.2 Input Current (I_i) and Input Offset Current (I_{io})

For the Motorola circuits, the input current is defined as that current measured at the input when the inputs were connected to the circuit ground through a 100-ohm resistance (see Figure 3-3).

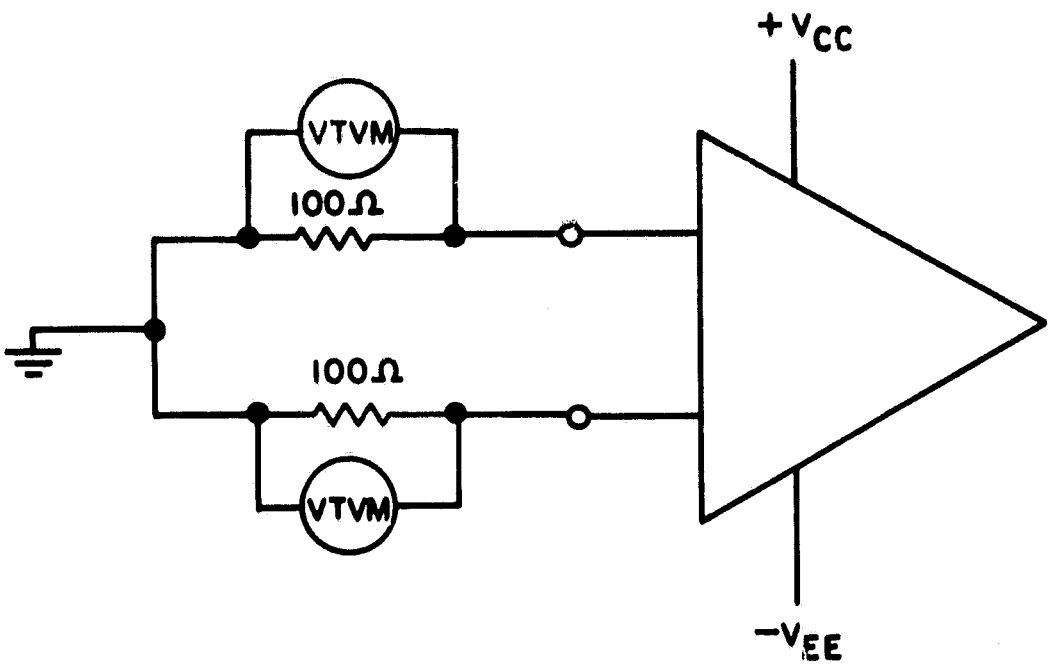


Figure 3-3. I_b and I_{io} Test Schematic

However, the data sheets for the SN-526A circuit calls for the measurement being made when $V_{in} = V_{io}$. To do that, the test method was modified to include the circuit shown for the V_{io} measurement with a current measurement being made in input as a voltage reading through a 10,000-ohm resistance.

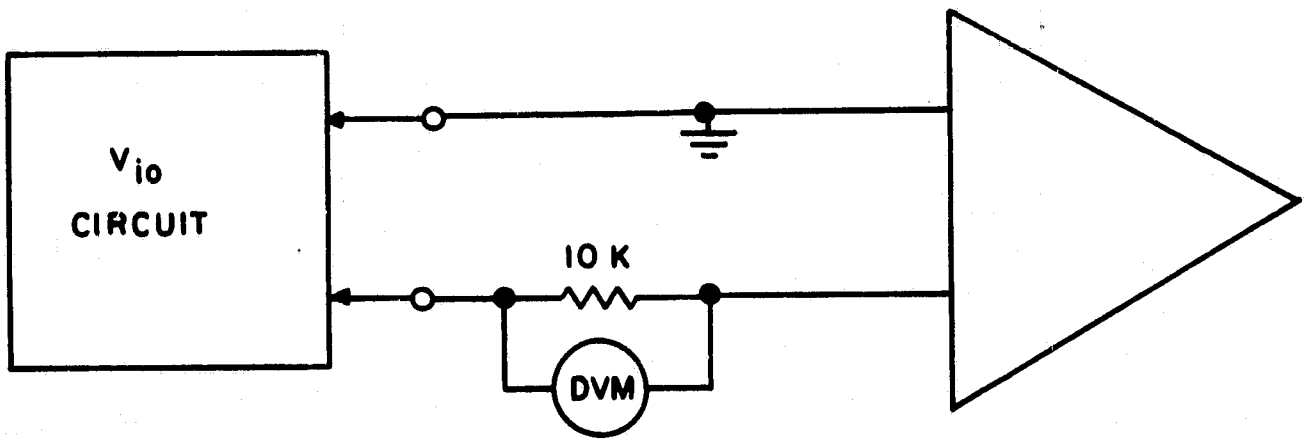


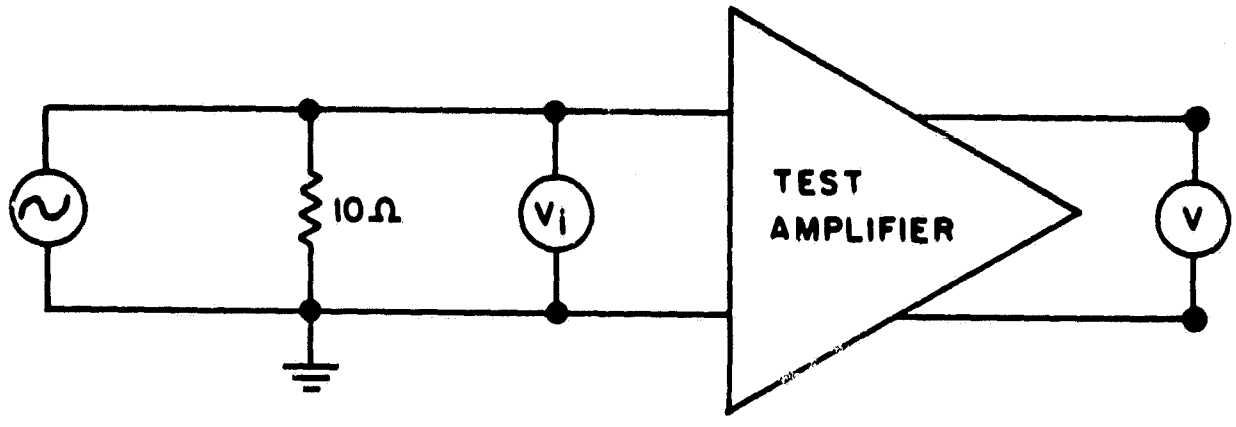
Figure 3-4. SN-526A I_i Test Schematic

Because of the very low input currents, typical values of 50 nAdc, and because the input offset voltage was adjusted at each measurement, the output remained balanced. In designing more rapid measurement techniques, it is assumed that the system designer would take advantage of the high gain operational characteristics of this style of amplifier and utilize a feedback resistor to set v_{io} at the level required to hold the output voltage at approximately 0 volts and then monitor the current in each input lead for the I_{in} measurement.

The differential input current (or input offset current - I_{io}) is defined as the difference in current values for each input and is a computed quantity obtained from the measured input currents. Its significance in this program is that it is a measure of the similarity of the input transistor characteristics and will become important if one of the two input circuits begins to degrade, if its degradation will show up as a function of input circuit.

3.2.3 Differential Voltage Gain (A_{dd})

This measurement is a measure of the circuit's ability to amplify differences in voltages applied to the two input terminals of the differential amplifier. As such, it does not apply to the single-ended MC-1530 and is used in the measurement of the SN-526A circuit only because that circuit offers both the single-ended and differential amplification characteristics in the same circuit. The measurement required first adjusting the input offset voltage (V_{io}) to the correct value and then applying a small alternating signal across the inputs and finally measuring the voltage difference at the output terminals under the predetermined load conditions. The differential gain is then defined as the ratio of the ouput signal to the input signal and can be converted to decibels if desired.



V_i = 1.0 mV rms
at 1 kHz - MC-1519, MC-1525
at 100 Hz - SN-526A

A_{dd} (ratio) = $\frac{V}{V_i}$

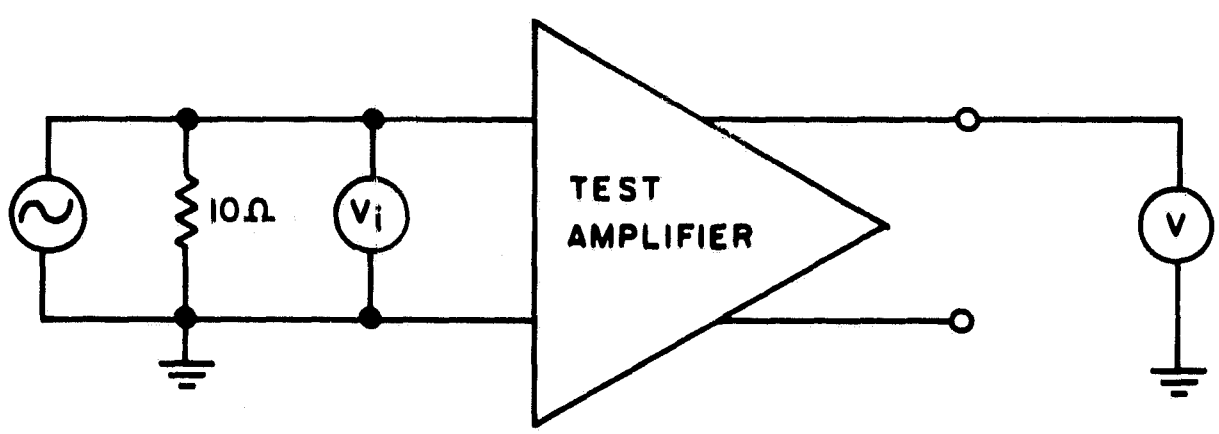
A_{dd} (dB) = 20 log $\frac{V}{V_i}$

Figure 3-5. Differential Voltage Gain Test Schematic

3.2.4 Single-Ended Voltage Gain (A_v, A_{Vol})

The procedure followed in this measurement is similar to that employed in the A_{dd} measurement (Paragraph 3.2.3) except that the output signal is now referenced to ground for one of the halves of the differential amplifier sections and the gain measurement pertains to that part of the amplifier (A_v). For the operational amplifier, it now becomes a measure of the open loop gain of the circuit (A_{Vol}). The significant variations in test procedure for these circuits are the input signal voltage and the oscillator frequency. The gain of the MC-1530 required that the input signal be reduced to 0.1 mV rms to permit undistorted sine waves at the output voltage. All other devices were measured with the input voltage equal to 1.0 mV rms. The Texas Instruments circuit (SN-526A) was measured at a frequency of 100 Hz because it was specified

to be done so. Motorola's circuits were tested at the frequency of 1000 Hz for the same reason. The circuit measurement technique is generally described as shown in Figure 3-6.



$$A_v \text{ (ratio)} = \frac{V}{V_i}$$

$$A_v \text{ (db)} = 20 \log \frac{V}{V_i}$$

Figure 3-6. Single-Ended Voltage Gain Test Schematic

3.2.5 Maximum Output Voltage Swing (V_o)

In this measurement, the input voltage was increased until the output voltage sine wave begins to become distorted. At this time, the peak-to-peak voltage is recorded. The significance of this measurement is probably found in its ability to detect leakage in the transistors in the output stages of the amplifier. However, this measurement was not considered a major parameter in this program. Again the oscillator frequency is set according to the published data sheet requirements of each vendor. The test circuit is identical with that used in measuring the single ended gain (A_v and A_{Vol}) except that the input signal is increased until the output distortion occurs.

3.2.6 Bandwidth (BW), Input Impedance (Z_{in}), and Common Mode Rejection (CM_{Rej})

These parameters are the ones which require considerable time for each parameter measurement, while being less significant as reliability study tests parameters. Therefore, they were made on those samples being life tested, both operational and storage, initially, at 1000 hours, and at each 1000 hour readout thereafter. The measurement techniques being used for some tests differ appreciably from those published in the applicable brochures. For instance, the ac input resistance measurement assumes the idealistic relationship that when $R_{in} = Z_{in}$, then V_o will be reduced by a factor of two resulting in a 6-dB drop in output signal. In each instance, however, it is necessary to adjust V_{io} to balance the output voltage (see Figure 3-7).

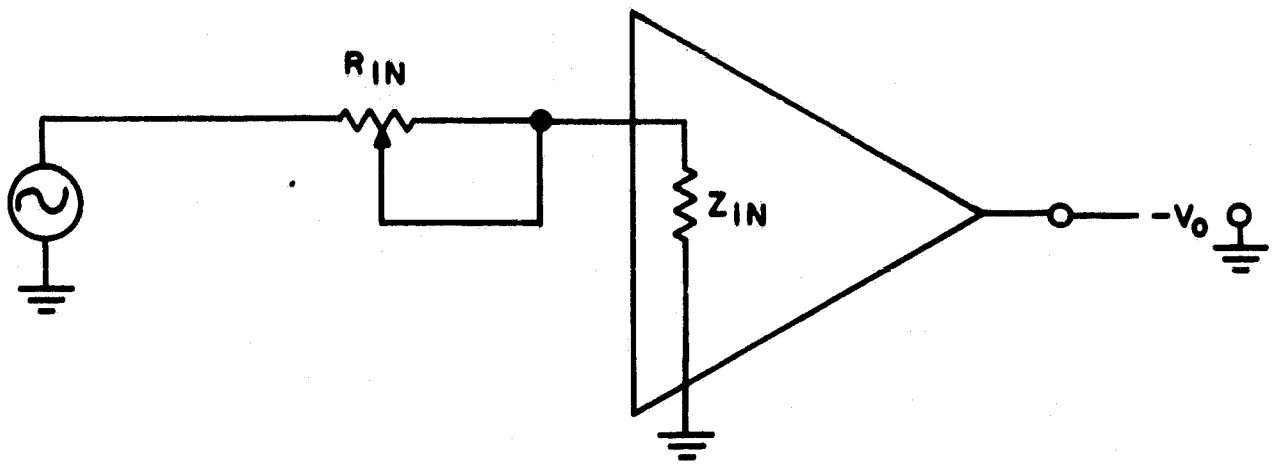


Figure 3-7. Input Impedance Test Schematic

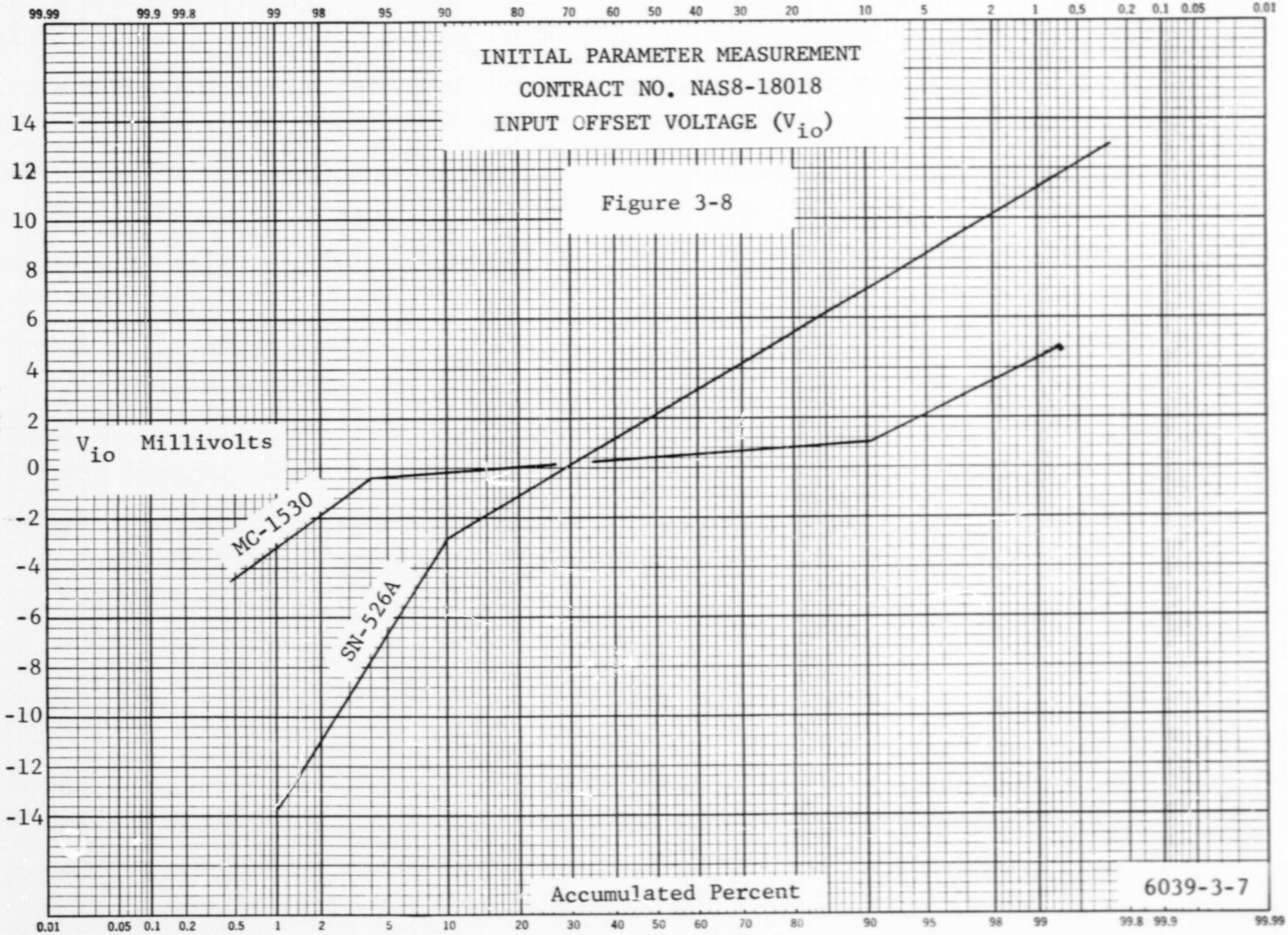
As is illustrated in Figures 3-9 and 3-10, the value of the dc input current is too large to permit such a simple circuit to be workable. When problems of this nature existed, modifications to procedures were incorporated that permitted the measurement to be made.

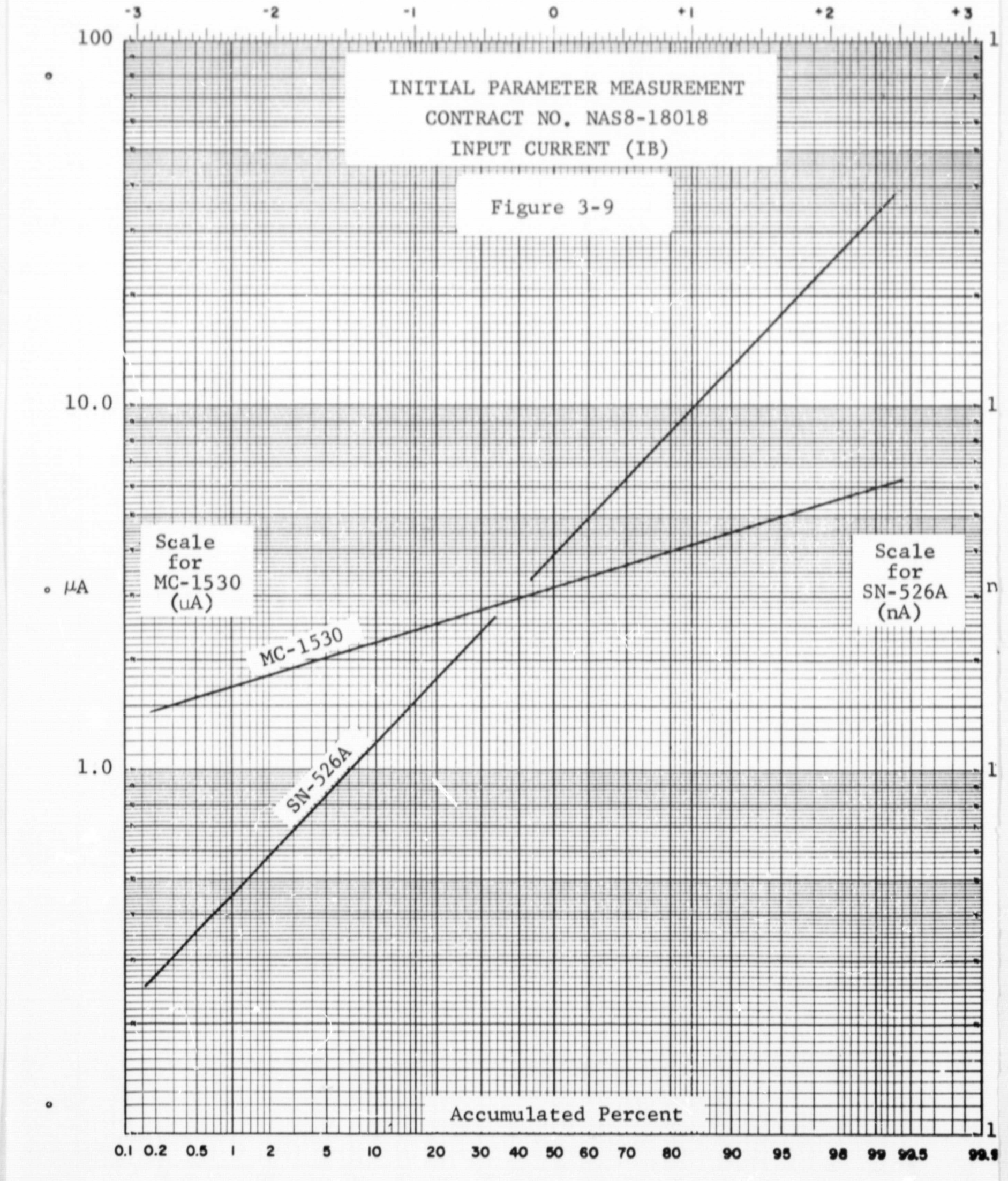
3.3 PROGRAM TEST PARAMETERS

A summary of the test parameters measured, their limits, and the actually recorded values are summarized in this section. The normal distribution graphs are representative of the total test sample. (See Figures 3-8 through 3-17.) The limits selected for the SN-526A have been arbitrarily selected by the test program personnel, based on distribution data shown here, for in none of the published documents available for this circuit is there a list of minimum or maximum limits. This is not a critical problem for the final data analysis includes an evaluation of parameter degradation as a result of applied stresses. All measurements recorded in this section were performed at room temperature (approximately 25°C).

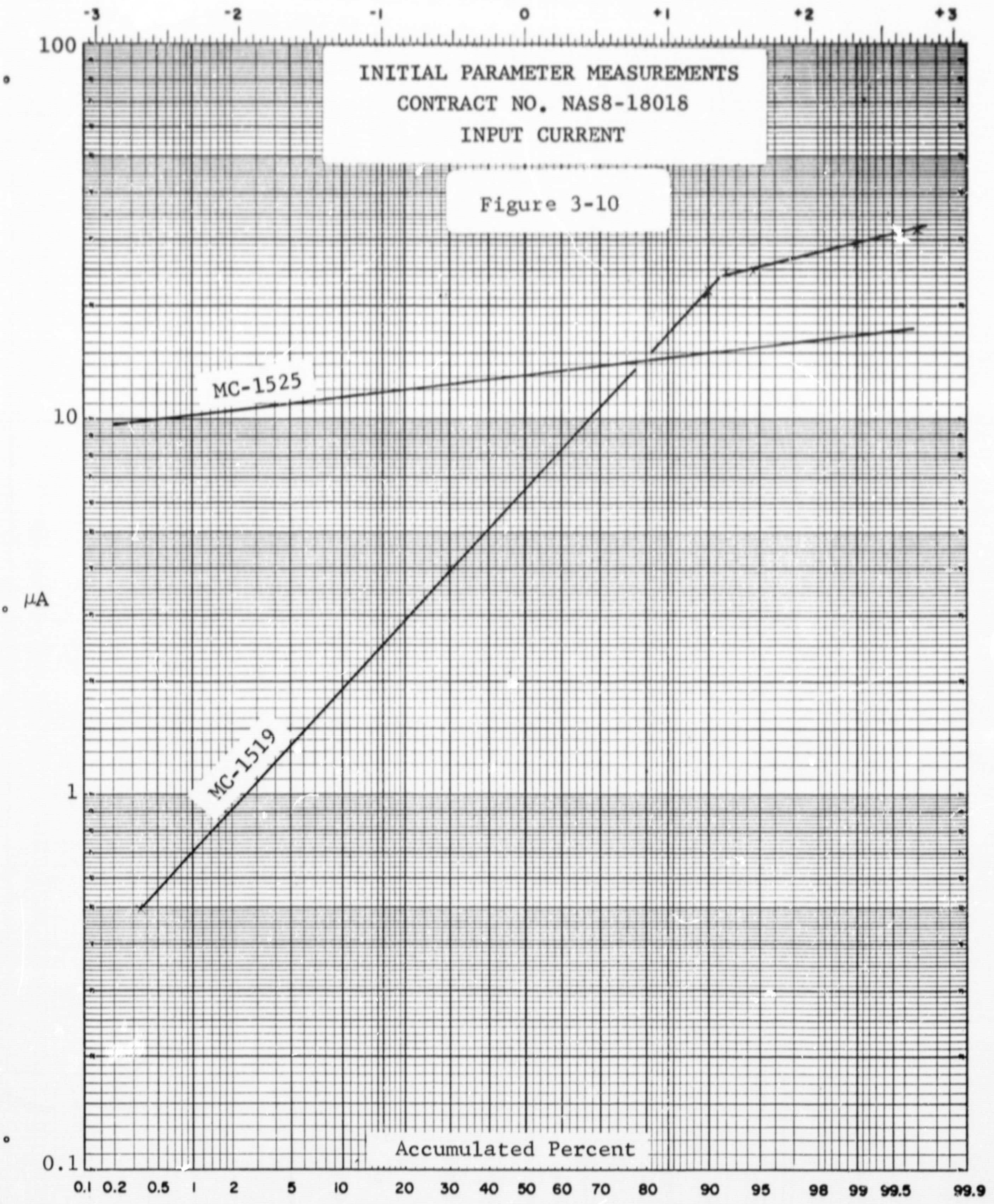
3.3.1 Table of Test Parameters

A list of the test parameters and their initial limits is found in Table 3-I. The endpoint limits are found in Tables 3-II, 3-III, 3-IV, and 3-V.


INITIAL PARAMETER MEASUREMENT
CONTRACT NO. NAS8-18018
INPUT OFFSET VOLTAGE (V_{io})
Figure 3-8
V_{io} Millivolts
MC-1530
SN-526A
Accumulated Percent
6039-3-7
99.99 99.9 99.8 99 98 95 90 80 70 60 50 40 30 20 10 5 2 1 0.5 0.2 0.1 0.05 0.01
0.01 0.05 0.1 0.2 0.5 1 2 5 10 20 30 40 50 60 70 80 90 95 98 99 99.8 99.9 99.99
14 12 10 8 6 4 2 0 -2 -4 -6 -8 -10 -12 -14


-3
-2
-1
0
+1
+2
+3
100
10.0
1.0
INITIAL PARAMETER MEASUREMENT
CONTRACT NO. NAS8-18018
INPUT CURRENT (IB)
Figure 3-9
Scale for MC-1530 (uA)
Scale for SN-526A (nA)
MC-1530
SN-526A
μA
Accumulated Percent
0.1 0.2 0.5 1 2 5 10 20 30 40 50 60 70 80 90 95 98 99 99.5

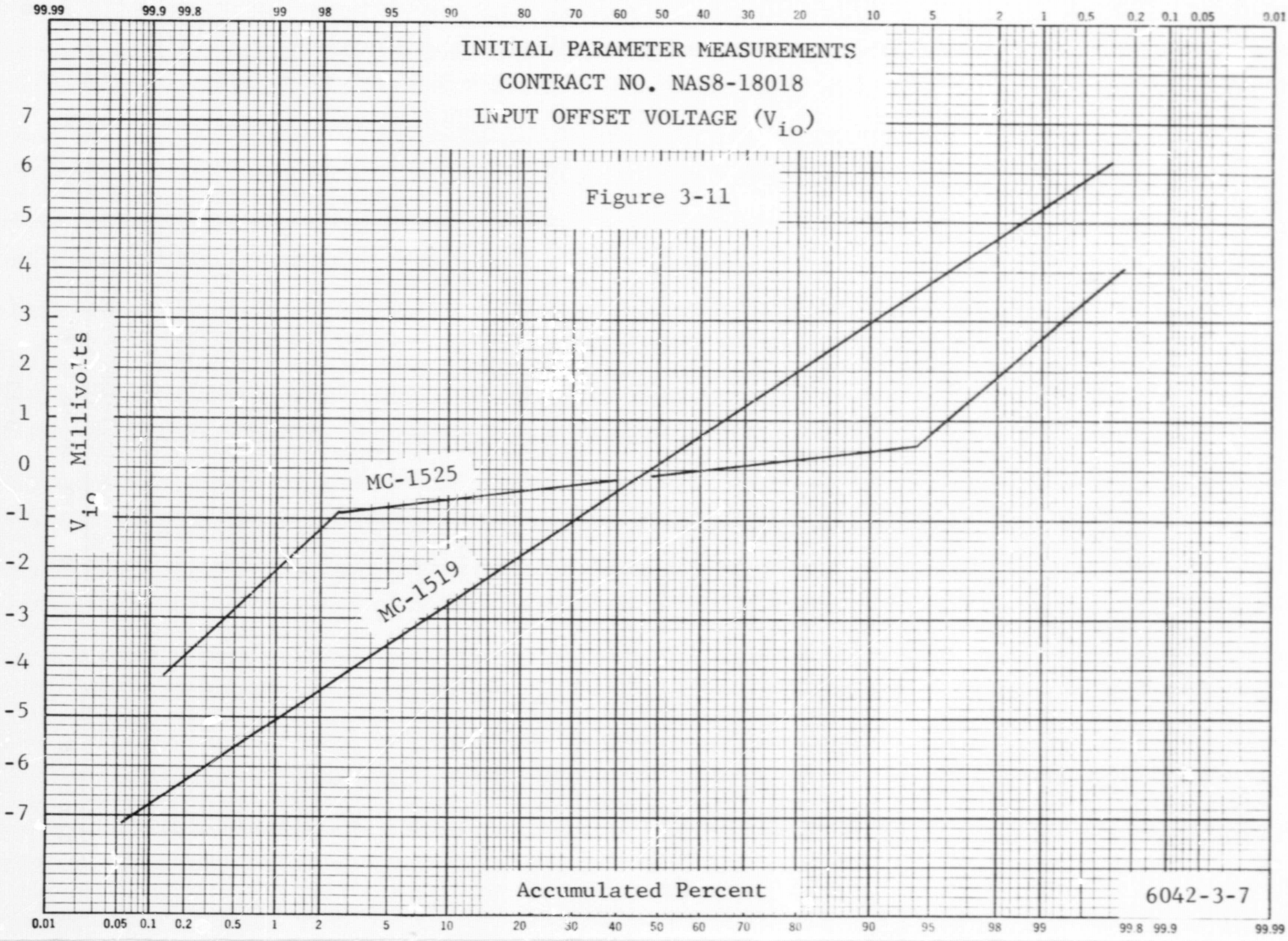
6040-3-7


-3
-2
-1
0
+1
+2
+3
100
10
1
0.1
μA
INITIAL PARAMETER MEASUREMENTS
CONTRACT NO. NAS8-18018
INPUT CURRENT
Figure 3-10
MC-1525
MC-1519
Accumulated Percent
0.1 0.2 0.5 1 2 5 10 20 30 40 50 60 70 80 90 95 98 99 99.5 99.9

6041-3-7

INITIAL PARAMETER MEASUREMENTS
CONTRACT NO. NAS8-18018
INPUT OFFSET VOLTAGE (V_{io})

Figure 3-11



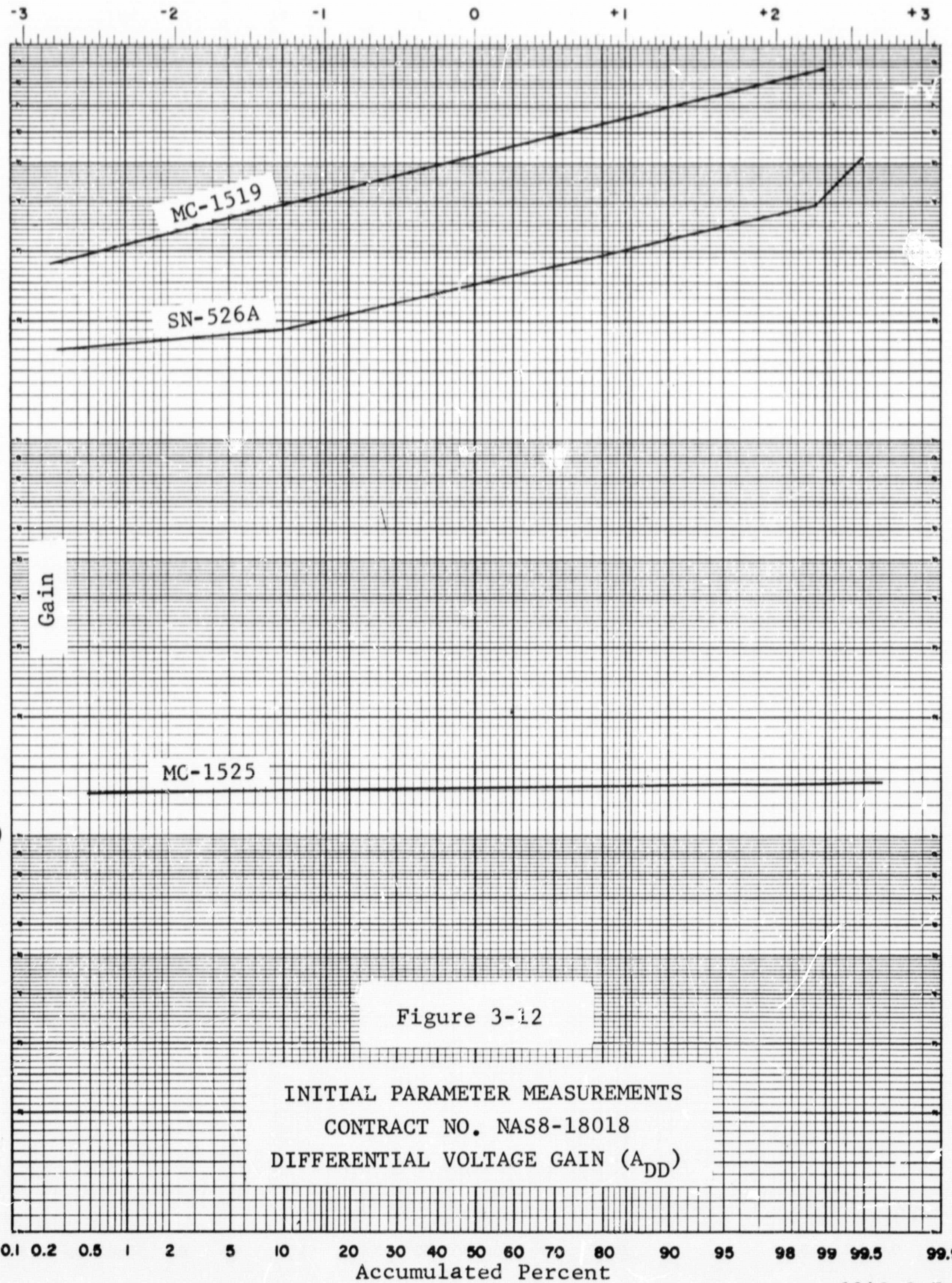


Figure 3-12

INITIAL PARAMETER MEASUREMENTS
CONTRACT NO. NAS8-18018
DIFFERENTIAL VOLTAGE GAIN (A_{DD})

6043-3-7

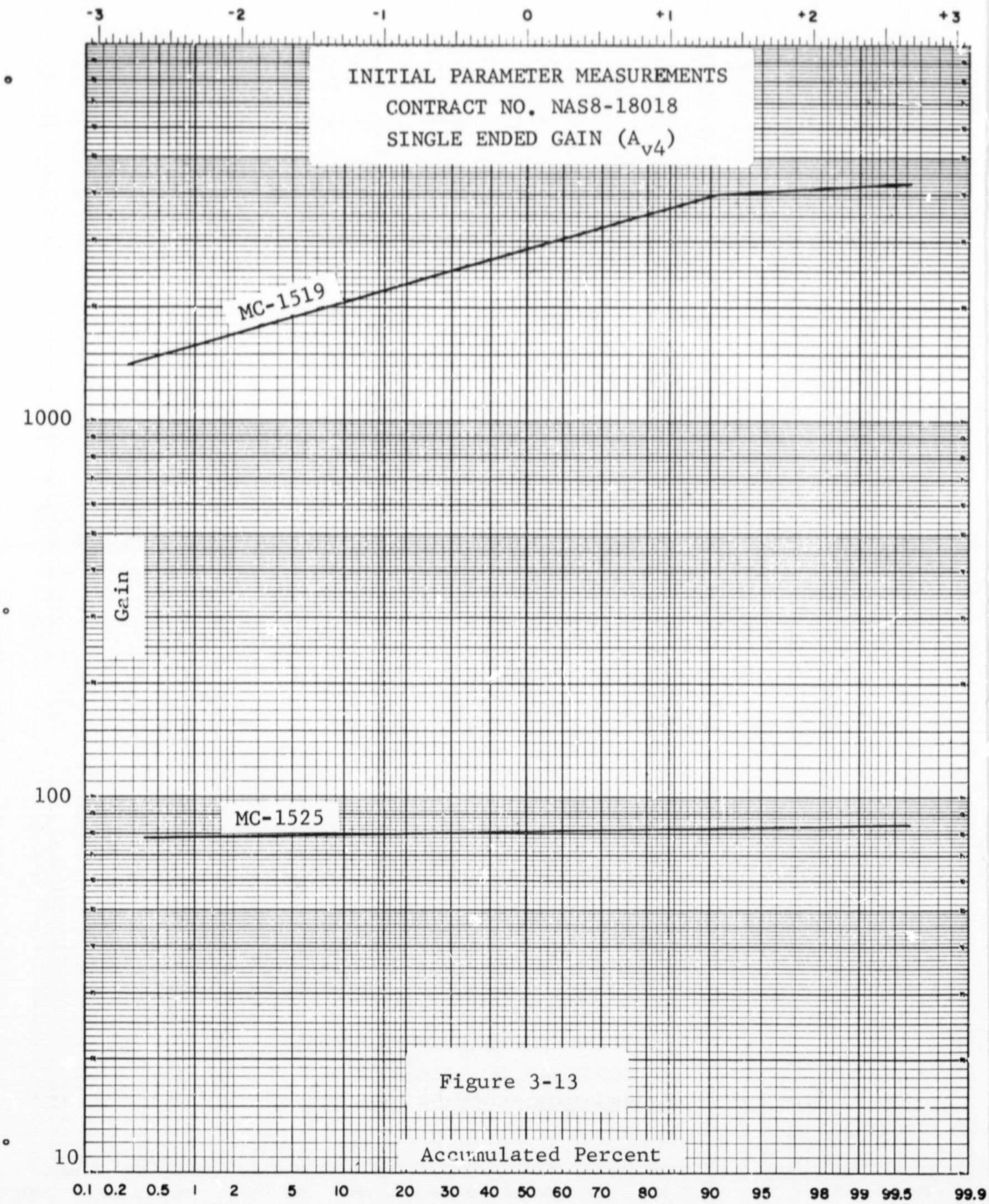
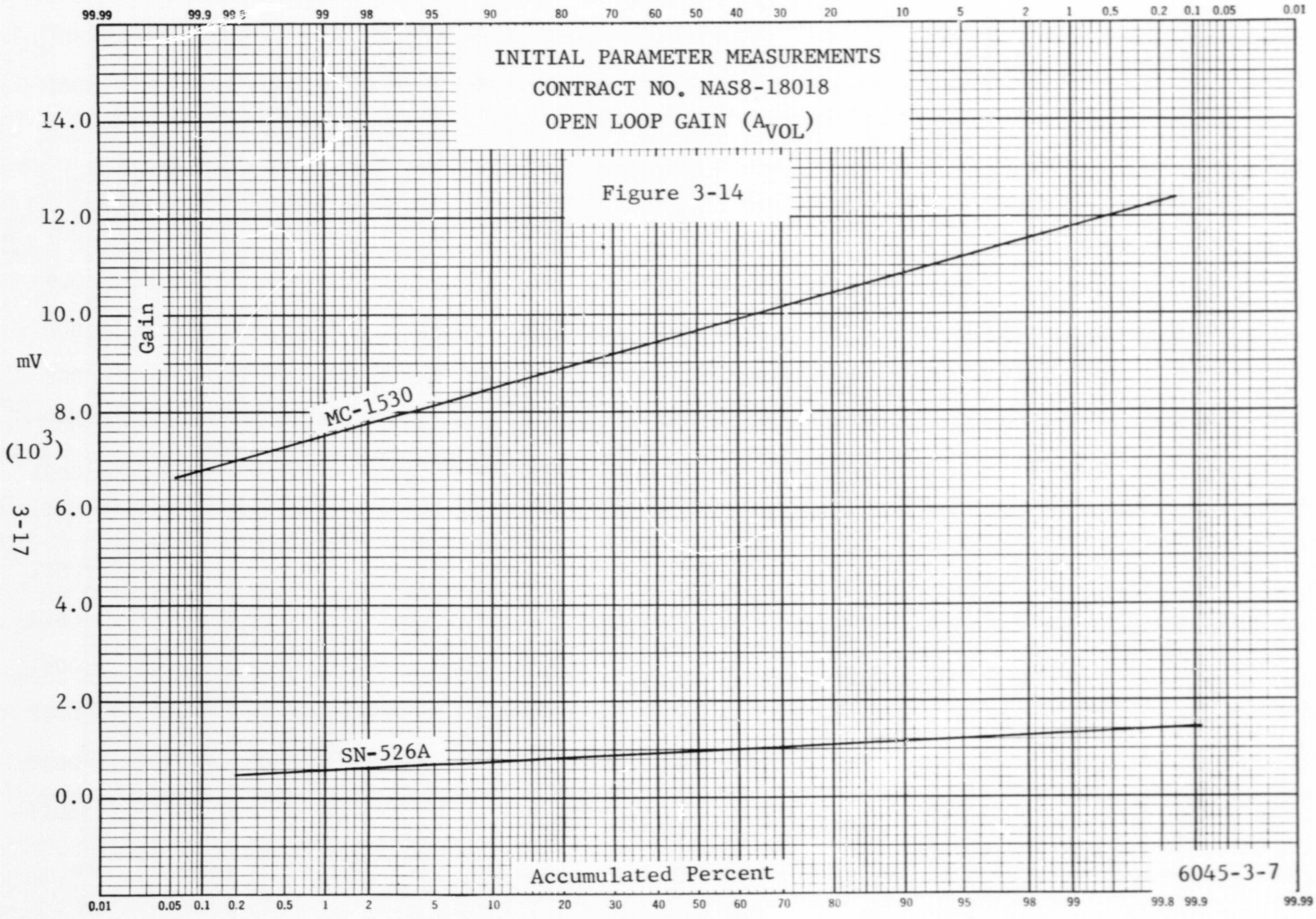


Figure 3-13

6044-3-7

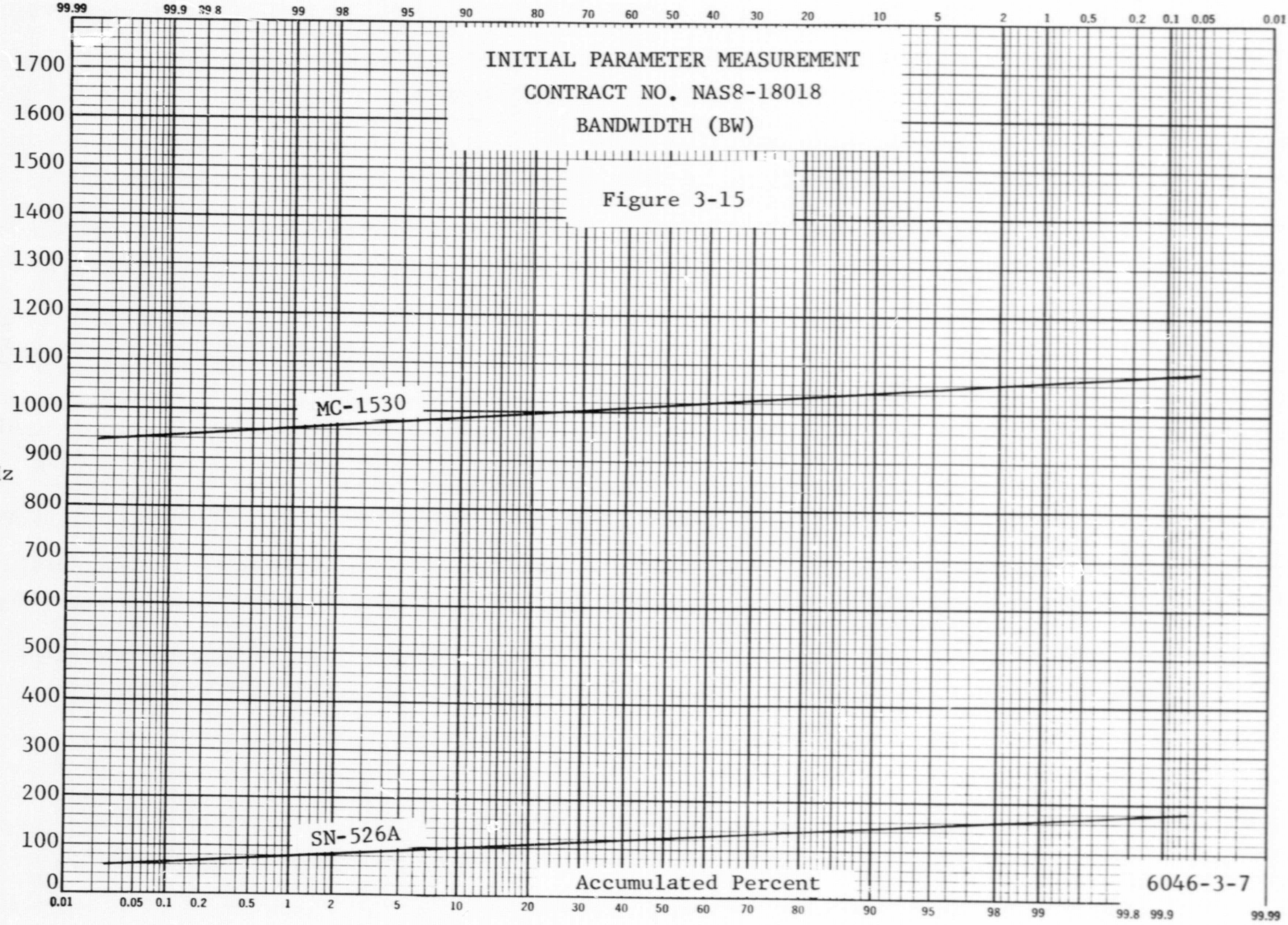
INITIAL PARAMETER MEASUREMENTS
CONTRACT NO. NAS8-18018
OPEN LOOP GAIN (A_{VOL})

Figure 3-14



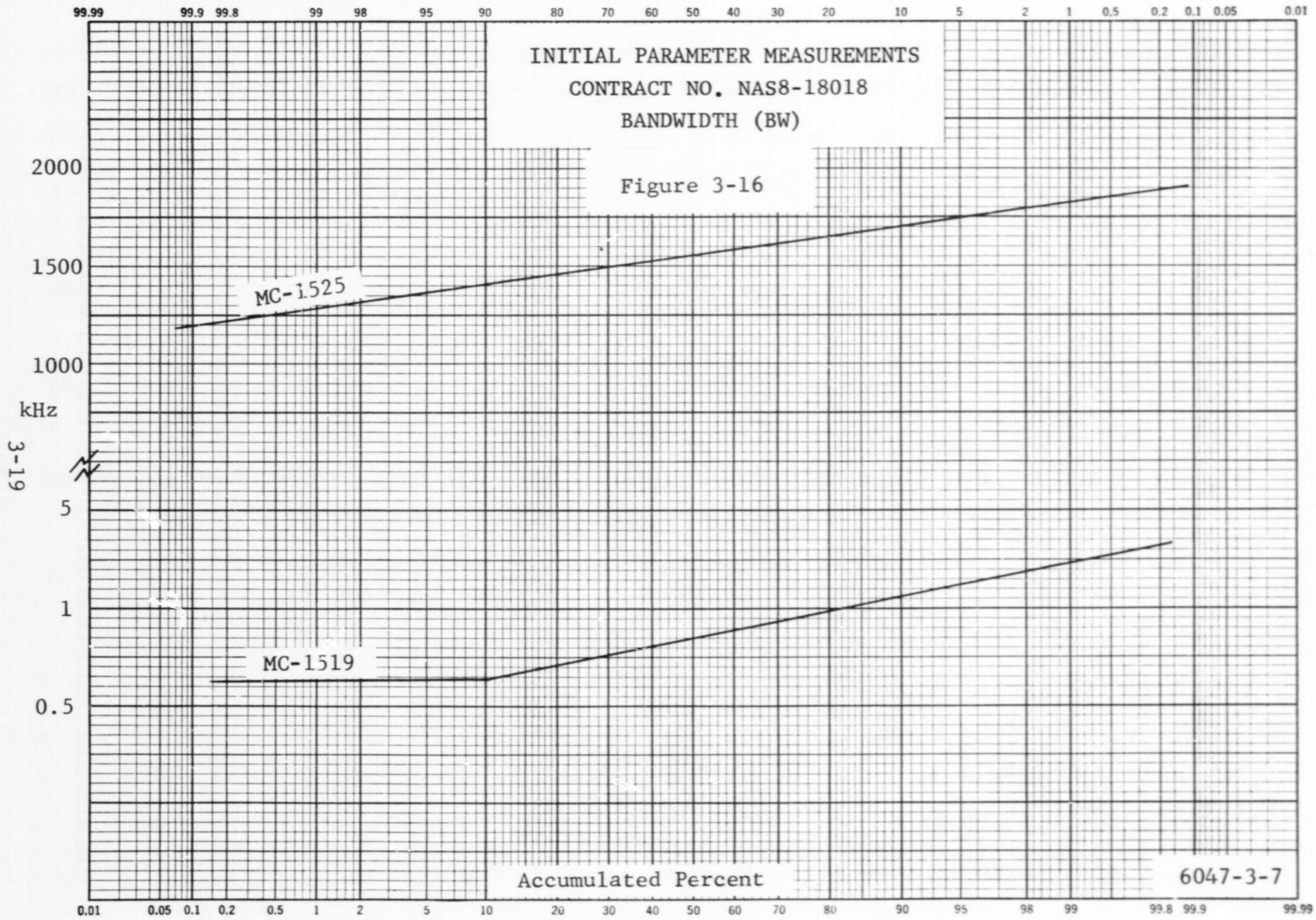
INITIAL PARAMETER MEASUREMENT
CONTRACT NO. NAS8-18018
BANDWIDTH (BW)

Figure 3-15



INITIAL PARAMETER MEASUREMENTS
CONTRACT NO. NAS8-18018
BANDWIDTH (BW)

Figure 3-16



INITIAL PARAMETER MEASUREMENT
CONTRACT NO. NAS8-18018
INPUT IMPEDANCE (Z_{in})

Figure 3-17

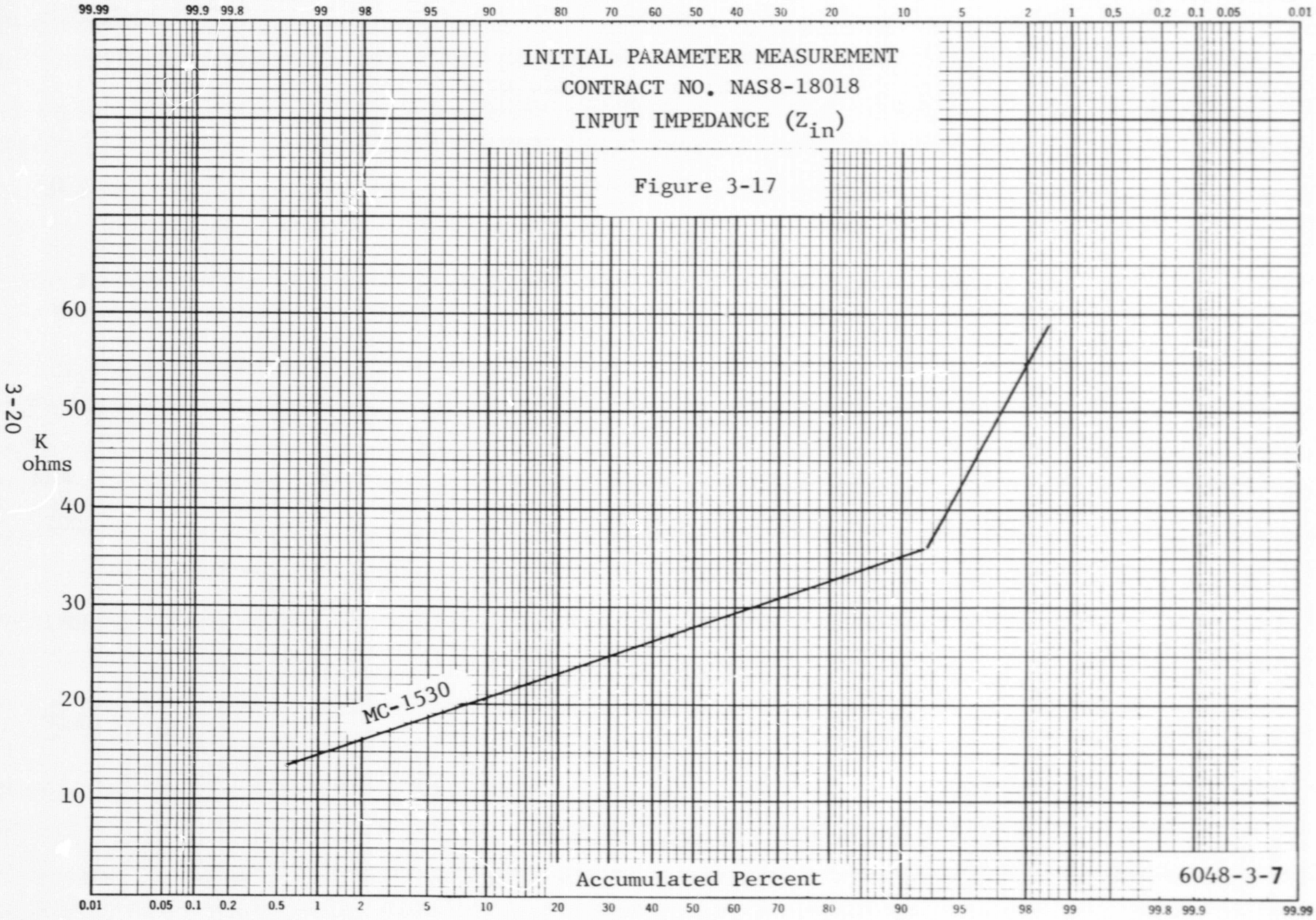


TABLE 3-I

INITIAL LIMITS OF TEST PARAMETERS

MC-1519		MC-1530		SN-526A		MC-1525	
Parameter	Initial Limits	Parameter	Initial Limits	Parameter	Initial Limits	Parameter	Initial Limits
A_{v4}	1.4-5.52 V	I_{B1}*	10 μA	I_{B7}*	0.5 μA Max	A_{dd}	120-160 V
V_{io8}	6.0 mV Max	I_{B2}*	10 μA	I_{B8}*	0.5 μA Max	$V_{o(CM)}$*	6.0-8.0 V
V_{io4}	6.0 mV Max	I_{io}*	2 μA	V_{io8}	±20 mV	V_o	7.0 V Min
V_o	12.0 V Min	V_{io}	5 mV Max	V_{io7}	±20 mV	V_{io}	5.0 mV Max
A_{dd}	2.8-11.03 V	V_o	9.0 V Min	A_{dd}	2.0-10.0 V	I_{io}*	4.0 μA Max
Z_{in}*	1.8 k ohm Min.	A_{VOL} at V_{in}=0.1mV	0.45-1.25 V	A_{VOL}	1.0-5.0 V	I_{in}*	20 μA Max
BN*	630 kHz Min	B_{WOL}*	1 MHz Min	BW*	50 kHz Min	CM_{Rej}*	80 dB Min
I_4*	0.7-70 μA	V_{ICM}*	2.0 V Min	V_o	9.0 V Min	BW*	1400 dB Min
I_8*	0.7-70 μA	Z_{in}*	10 k ohm Min	V_{OL}	5.0 V Min	Z_{in}*	2.0 k ohm Min
		CM_{Rej}*	70 dB Min	Z_{in}	10 M ohm Min		

*Study parameters. No decisions concerning failure of these circuits are made from these parameters.

TABLE 3-II

PRELIMINARY MC-1519 FAILURE CRITERIA

Parameters	Initial Limits	Final Limits		Units
		Degradation	Catastrophic	
A_{v4}	1.4 - 5.52	1.0 - 10.0	Inoperative	Volts
V_{io8}	6.0 Max	7.0 Max	10 Max	mV
V_{io4}	6.0 Max	7.0 Max	10 Max	mV
V_o	12.0 Min	10 Min	Inoperative	Volts
A_{dd}	2.8 - 11.03	2.0 - 20	Inoperative	Volts
Z_{in}*	1.8 Min	1.6 Min	Less than 0.5	k ohm
BW*	630 Min	Information Parameter		kHz
I_8*	0.7 - 70	0.5 - 100	0.1 - 300	μA
I_8*	0.7 - 70	0.5 - 100	0.1 - 300	μA
$V_{CM(out)}$*	Information Parameter			
$V_{CM(in)}$*	Information Parameter			

*Study parameters. No decisions concerning failure of these circuits are made from these parameters.

TABLE 3-III

PRELIMINARY MC-1530 FAILURE CRITERIA

Parameters	Initial Limits	Final Limits		Units
		Degradation	Catastrophic	
I_{B1}*	10 μA	±20 μA	±100 μA	μA
I_{B2}*	10 μA	±20 μA	±100 μA	μA
I_{io}*	2 μA	4 μA	20 μA	μA
V_{io}	5 mV Max	7 mV	50 mV	mV
V_o	9.0 Min	7.5 Min	2.0	Volts
A_{VOL} at V_{in} = 0.1 mV	0.45 - 1.25	0.20 - 3.2	Inoperative	Volts
B_{WOL}*	1 Min	Information Parameter		MHz
V_{ICM}*	2.0 Min	Information Parameter		Volts
Z_{in}*	10 Min	8 k ohms	1 k ohms	k ohm
C_{Mrej}*	70 Min	Information Parameter		dB
defined as $\frac{AVOL}{ACM}$ Computed = 20 log AVOL x 10^4 - 20 log $\frac{VICM}{2}$				

*Study parameters. No decisions concerning failure of these circuits are made from these parameters.

TABLE 3-IV

PRELIMINARY SN-526A FAILURE CRITERIA

Parameters	Initial Limits	Final Limits		Units
		Degradation	Catastrophic	
I_{B7}*	0.5 μA Max	2 μA Max	20 μA Max	μA
I_{B8}*	0.5 μA Max	2 μA Max	20 μA Max	μA
I_{io}*	Information Parameter			
V_{io8}	±20	±25	±50	mV
V_{io7}	±20	±25	±50	mV
A_{dd}	2.0 - 10.0	1.0 Min	Inoperative	Volt
A_{VOL}	1.0 - 5.0	0.28 Min	Inoperative	Volt
BW*	50 Min	Information Parameter		kHz
V_o	9.0 Min	7.5 Min	2.0 Min	Volt
V_{OL}	5.0 Min	3.5 Min	1 Min	Volt
Z_{in}	10 Min	8	1	M ohm
C_{Mrej}*	Information Parameter			

*Study parameters. No decisions concerning failure of these circuits are made from these parameters.

TABLE 3-V

PRELIMINARY MC-1525 FAILURE CRITERIA

Parameters	Initial Limits	Final Limits		Units
		Degradation	Catastrophic	
A_{dd}	120 - 160	80 - 200	10 Min.	Volt
A_v				Volt
$V_{o(CM)}$*	6.0 - 8.0	5.0 - 9.0	-5.0 - +11.5	Vdc
V_o	7.0 Min	3.5 Min	1.0 Min	Volt
V_{io}	5.0 Max	8.0 Max	50 Max	mVdc
I_{io}*	4.0 Max	10.0 Max	40 Max	μA
I_{in}*	20 Max	40 Max	100 Max	μA
CM_{Rej}*	80 Min	Information Parameter		dB
BW*	1400 Min	Information Parameter		kHz
Z_{in}*	2.0 Min	Information Parameter		k ohm

*Study parameters. No decisions concerning failure of these circuits are made from these parameters.

SECTION IV

4.0 TEST PROGRAM SUMMARY

A summary of the test program results on the operational amplifiers is shown in Tables 4-I and 4-II. However, to touch on only the highlights, it is possible to conclude that all parts used in this program have attractive reliability features that make them potentially useful in a number of high reliability applications. The most reliable part tested was Motorola's operational amplifier, the MC-1530F. This part was not only the most reliable, as defined by the end point criteria used in this program (see Section 3, Paragraph 3-23), but it was also the most stable. In no test did any of the MC-1530F test parameters show any signs of constant degradation. It withstood ambient temperatures of 475°C and all thermal and shock tests it was subjected to. The next most successful part was the SN-526 operational amplifier manufactured by Texas Instruments. In some tests, its performance exceeded that of the MC-1530F, but it was more temperature sensitive and the input circuits did tend to degrade when subjected to the higher temperatures for long periods if tune, Histograms for all parameters and all tests are being included for these two circuits.

While exhibiting more problems, the electrical characteristics of the differential amplifiers make them attractive circuits for further consideration. The MC-1525G exhibited the best circuit parameter stability for this program (excluding the MC-1530F), but did demonstrate a destructive phenomenon that restricts the use of the resistive network in its current control circuit. The MC-1519G performed poorest of all the circuits tested in this program. It appeared to be more susceptible to processing errors as well as process related phenomena. For instance, the MC-1519 did show a higher susceptibility to the intermetallic compound formations at the Au-Al interfaces on its die and bonding posts. While all

TABLE 4-I

PROGRAM SUMMARY REPORT

MC-1530F

Test Description	Test Duration (Hours)	Accumulated Hours of Testing (Hours)	Initial Sample Size	Summary of Test Data (No. Failures)
OPERATING LIFE TESTS				
T_A = 25°C pd = 100 mW	3000	44,500	15	0
T_A = 125°C pd = 100 mW	3000	72,500	25	0
T_A = 125°C pd = 300 mW	3000	72,750	25	0
Storage Life Test T_A = 150°C	3000	45,000	15	0
MECHANICAL TEST SEQUENCE Impact Shock 1500g ½ms Vibrative Fatigue 20g Vibration Variable Freq. Constant Acceleration 20,000g	X	X	25	0
THERMAL TEST SEQUENCE Solderability Temperature Cycling (-65°C to +175°C) Thermal Shock Moisture Resistance	X	X	25	0

TABLE 4-I (Cont'd.)

PROGRAM SUMMARY REPORT

MC-1530F

Temperature Step Stress Test		Power Step Stress Test				Temperature Cycling Step Stress (-55°C to T_h)	
		T_A = 25°C t = 48 hrs/step		T_A = 125°C t = 48 hrs/step			
Sample Size = 15		Sample Size = 15		Sample Size = 15		Sample Size = 15	
Test Cell (T = °C)	Number of Failures	Test Cell (mW)	Number of Failures	Test Cell (mW)	Number of Failures	Test Cell (T_h = °C)	Number of Failures
200	0	100	0	100	0	150	0
225	0	200	0	200	0	175	0
250	0	300	0	300	0	200	0
275	0	400	0	400	0	225	0
300	0	500	1 (1)	500	0	250	0
325	0	600	0	600	1 (2)	275	0
350	0	700	2 (2)	700	6 (2)	300	0
375	0	800	10 (2)	800	3 (2)	325	0
400	0						
425	0						
450	1						
475	0						

NOTES:

1. Test equipment error. Not discovered until too late to return device to lot.
2. Metal migration due to excessive current density at overstressed conditions.

TABLE 4-II

PROGRAM SUMMARY REPORT

SN-526

Test Description	Test Duration (Hours)	Accumulated Hours of Testing (Hours)	Initial Sample Size	Summary of Test Data (No. Failures)
OPERATING LIFE TESTS				
T_A = 25°C pd = 100 mW	2000	30,000	15	0
T_A = 125°C pd = 100 mW	3000	69,812	25	0
T_A = 125°C pd = 300 mW	3000	75,000	25	0
Storage Life Test T_A = 150°C	3000	44,500	15	1 (1) 3000 hrs.
MECHANICAL TEST SEQUENCE				
Impact Shock 1500g ½ms Vibrative Fatigue 20g Vibration Variable Freq. Constant Acceleration 20,000g	X	X	23	1 (2)
THERMAL TEST SEQUENCE				
Solderability Temperature Cycling (-65°C to +175°C) Thermal Shock Moisture Resistance	X	X	25	0

TABLE 4-II (Cont'd.)

PROGRAM SUMMARY REPORT

SN-526

Temperature Step Stress Test		Power Step Stress Test				Temperature Cycling Step Stress (-55°C to T_h)	
		T_A = 25°C t = 48 hrs/step		T_A = 125°C t = 48 hrs/step			
Sample Size = 15		Sample Size = 15		Sample Size = 15		Sample Size = 15	
Test Cell (T = °C)	Number of Failures	Test Cell (mW)	Number of Failures	Test Cell (mW)	Number of Failures	Test Cell (t_h = °C)	Number of Failures
200	0	100	0	100	0	150	0
225	1 (1)	200	0	200	0	175	1 (3)
250	0	300	0	300	0	200	0
275	3 (1)	400	0	400	0	225	0
300	4 (1)	500	0	500	0	250	0
325	2 (1)	600	0	600	3(1,4)	275	1 (1)
		700	1 (4)	700	1(1,4)	300	4 (1)
		800	0	800	0		
		900	0	900	2(1,4)		

NOTES:

1. Open wire bond at the die due to aluminum-gold intermetallic compound formation.
2. Bad bond, overbonded.
3. Test error - misinsertion in test socket.
4. Overstress tests.

devices using gold wire interconnections and aluminum metallization on the die did exhibit this expected phenomenon, the MC-1519G did so most often, particularly on long-term storage tests at temperatures where the rate of reaction should have been substantially reduced. This factor may be attributed to the fact that this circuit is a hybrid circuit and, therefore, has more bonds. The MC-1519G also exhibited a greater susceptability to the surface inversion phenomenon (channelling) than did the other circuits, even though the MC-1530F and MC-1525G dice are made using the same integrated circuit die manufacturing process and did not exhibit similar channelling problems.

In the following sections a discusssion of the vital details of this program is undertaken. It will place particular emphasis on such subjects as:

(1) The degradation characterisitcs of each circuits.
(2) Analysis of the power performance characteristic of each circuit.
(3) Analysis of the temperature performance characteristics for each circuit.
(4) The results of special tests performed at the conclusion of this test program. It will include a description and the results of a special mechanical step stress test, a special infrared study, and a special power biased temperature step stress performed to evaluate the validity of high and low temperature test measurements.
(5) A description of the failure analysis results obtained in this program.

4.1 MC-1530F RESULTS

No continuous degradation occurred for this circuit. Histrograms showing parameter values versus time on test are shown in Figures 4-1 through 4-10. The failures that did occur at the very highly accelerated stress levels were catastrophic in nature and resulted from metallization overstresses or metal oxidation at the very high temperature. The power step stress failures are probably in part attributable to the method of test. On a single die, this power level is obtained by increasing the current drain in the output stages resulting in excessive current flows through critical metal regions. Motorola has performed considerable work in the metallization stressing and it is known that the rate of degradation of these circuits is both a function of current density and temperature. In these junction surface regions, the temperature exceeded 225°C and the current density approached critical proportions of 5×10^5 A/cm^2. Therefore, catastrophic metallization failures developed. It can be deduced therefore, that tests designed with power requirements greater than 400 mW are stressing the circuits beyond the physical limitation of the materials involved. A picture of one such overstressed circuit is shown in Figure 4-11. In this unit, No. 171, it can be seen that the metal is opened in some points and appears to have bubbled and "creeped" in the other loops in the output half of the circuit. This metal fatigue is natural for these circuits under the overstress conditions used here. In all, the MC-1530F did not demonstrate a single unreliable characteristic. All failures were generated as a result of overstressing each circuit beyond its physical limitations.

4.2 SN-526 RESULTS

This circuit was less stable than that of the MC-1530F. A look at the data in Figure 4-12 shows that the SN526's input current did increase for each test that occurred at the ambient temperature of 125°C or higher. All characteristics of the MC-1530F remained

Figure 4-1. Operating Life Test, MC1530
T_A = 25°C, P_d = 100 mW
Sample Size = 15

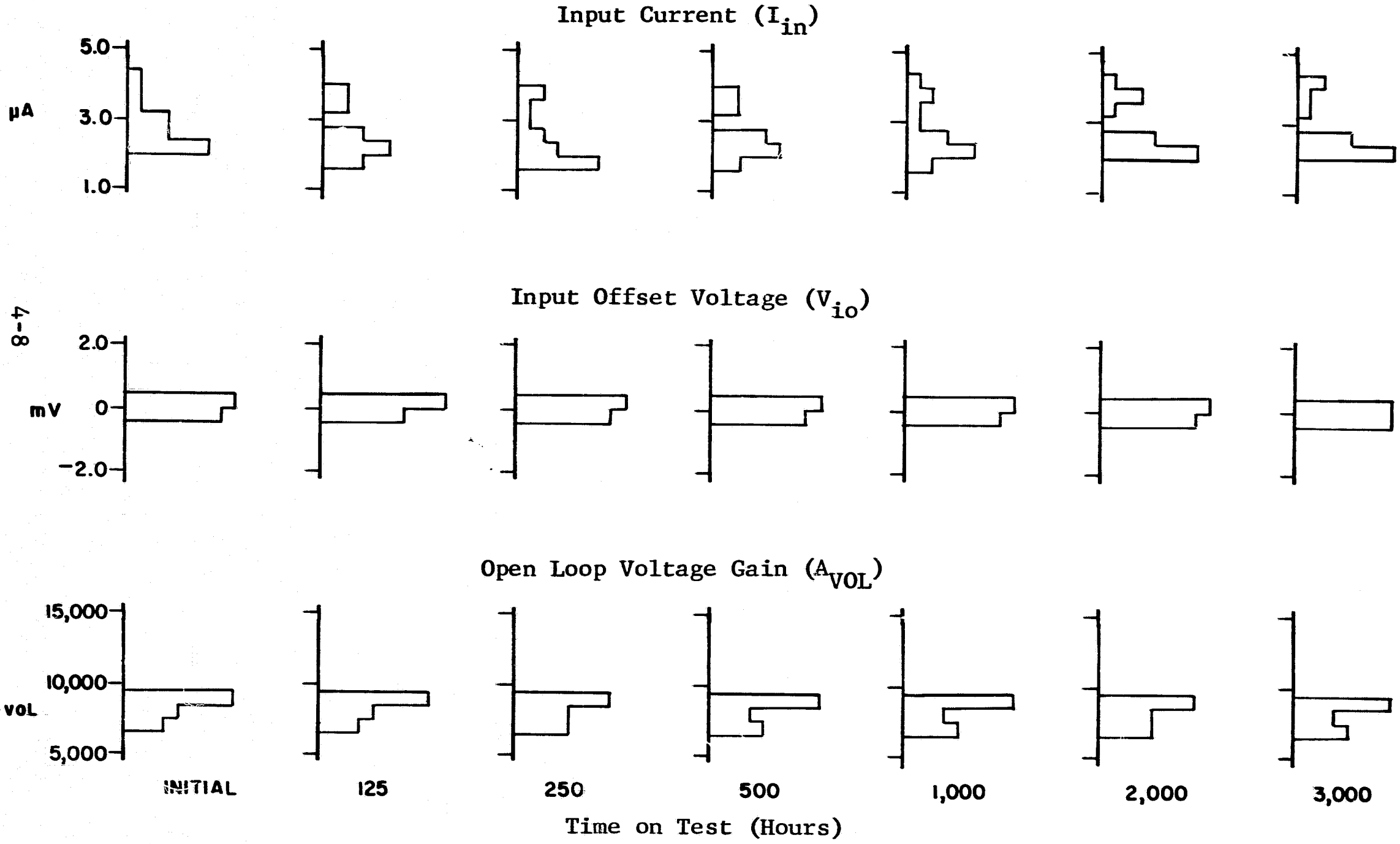
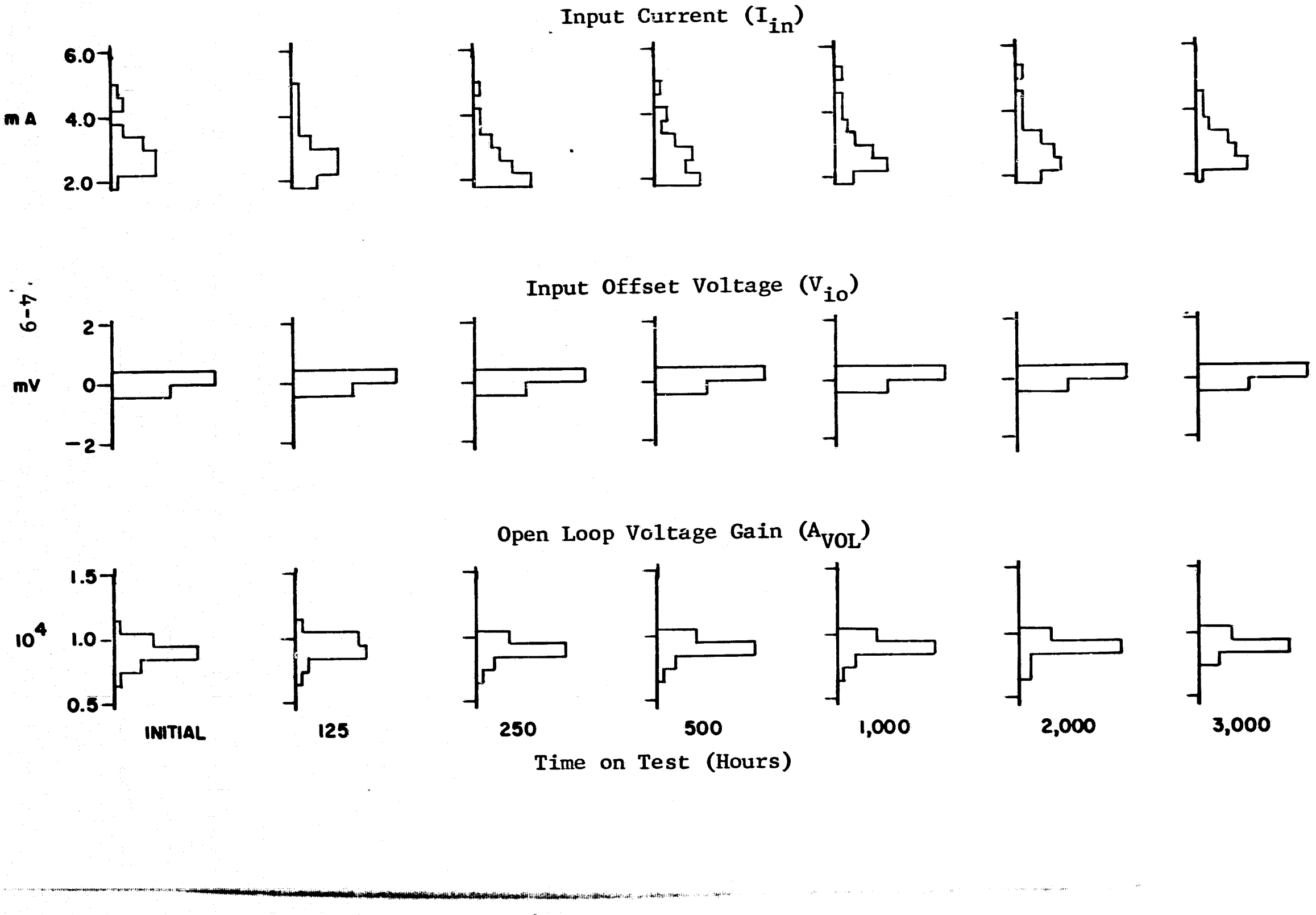


Figure 4-2. Operating Life Test, MC1530
$T_A = 125°C$
Sample Size = 25



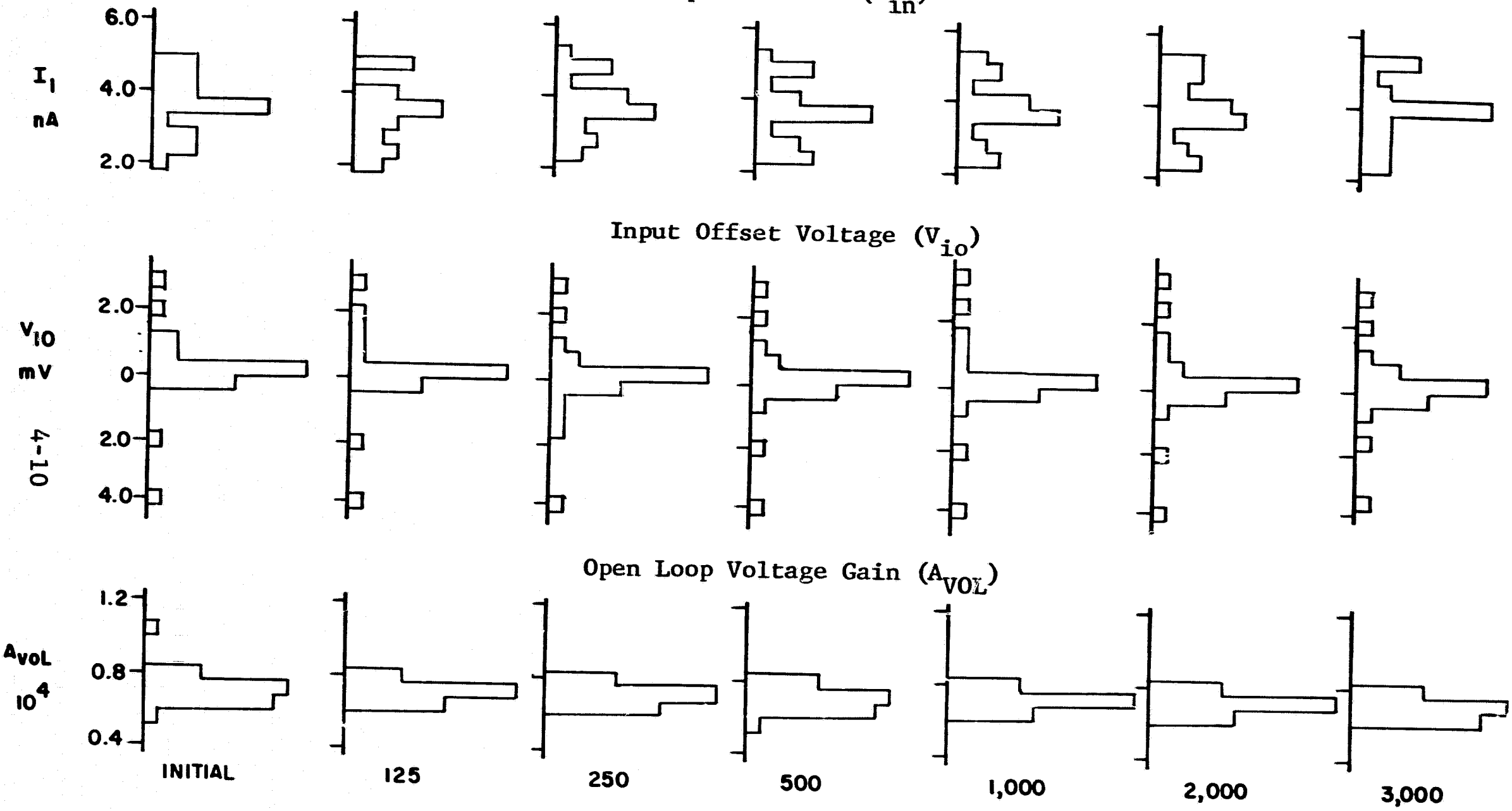


Figure 4-3. Operating Life Test, MC1530
T_A = 125°C, 300 mW
Sample Size = 25

Figure 4-4. Storage Life Test, MC1530
T_A = 150°C
Sample Size = 15

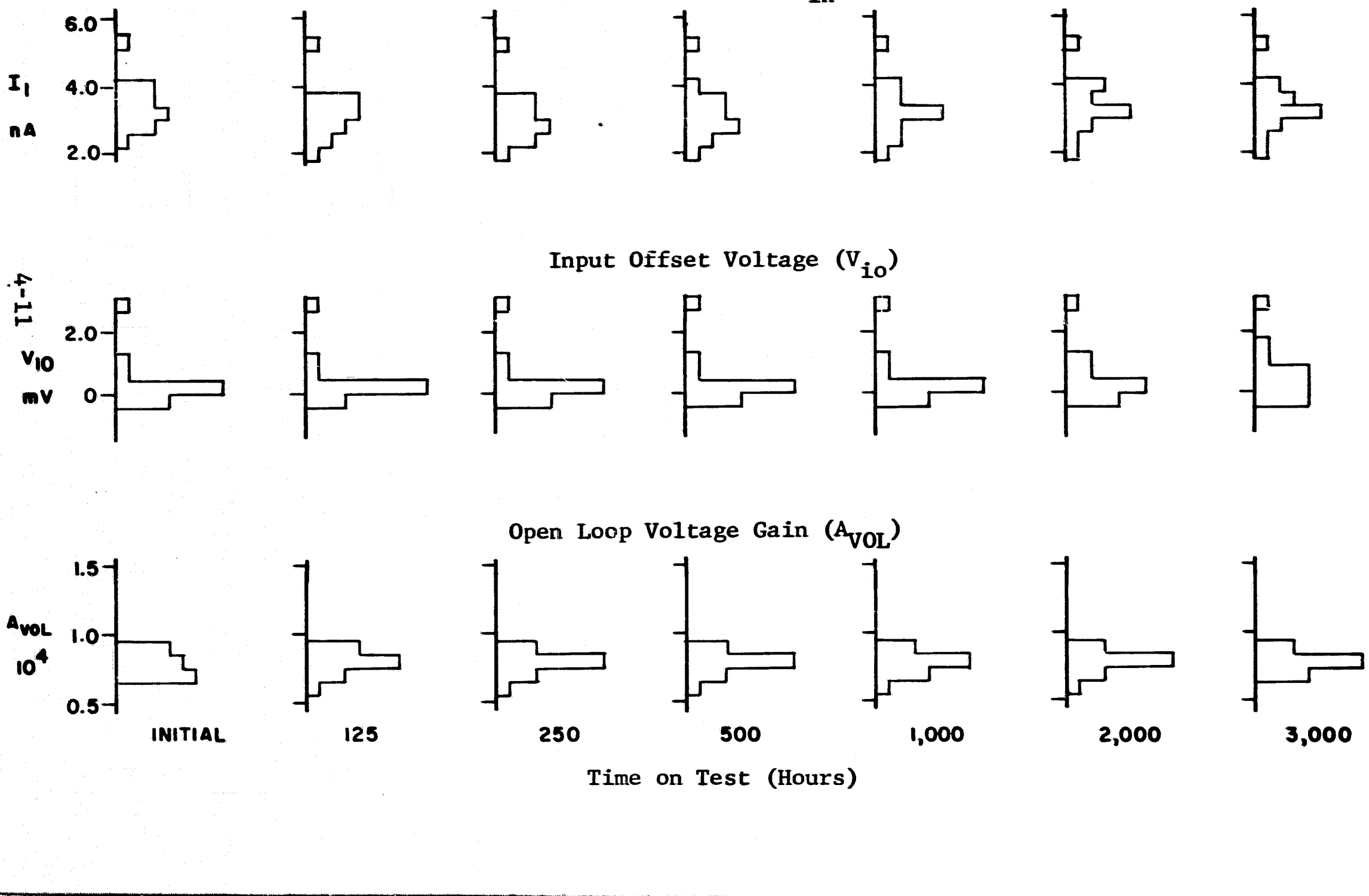


Figure 4-5. Temperature Step Stress Test, MC1530
Sample Size = 15

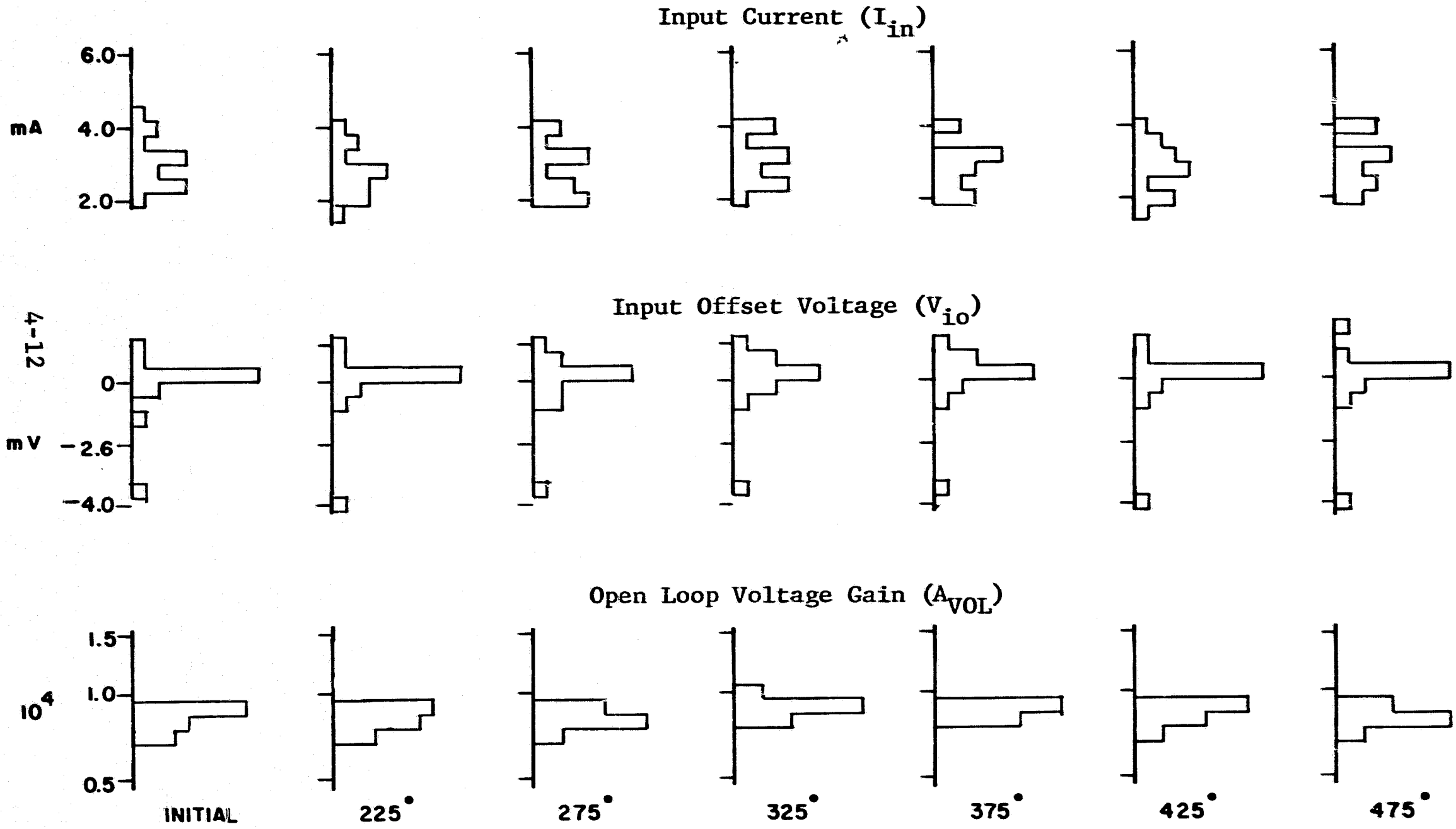


Figure 4-6. Power Step Stress Test, MC1530
T_A = 25°C
Sample Size = 15

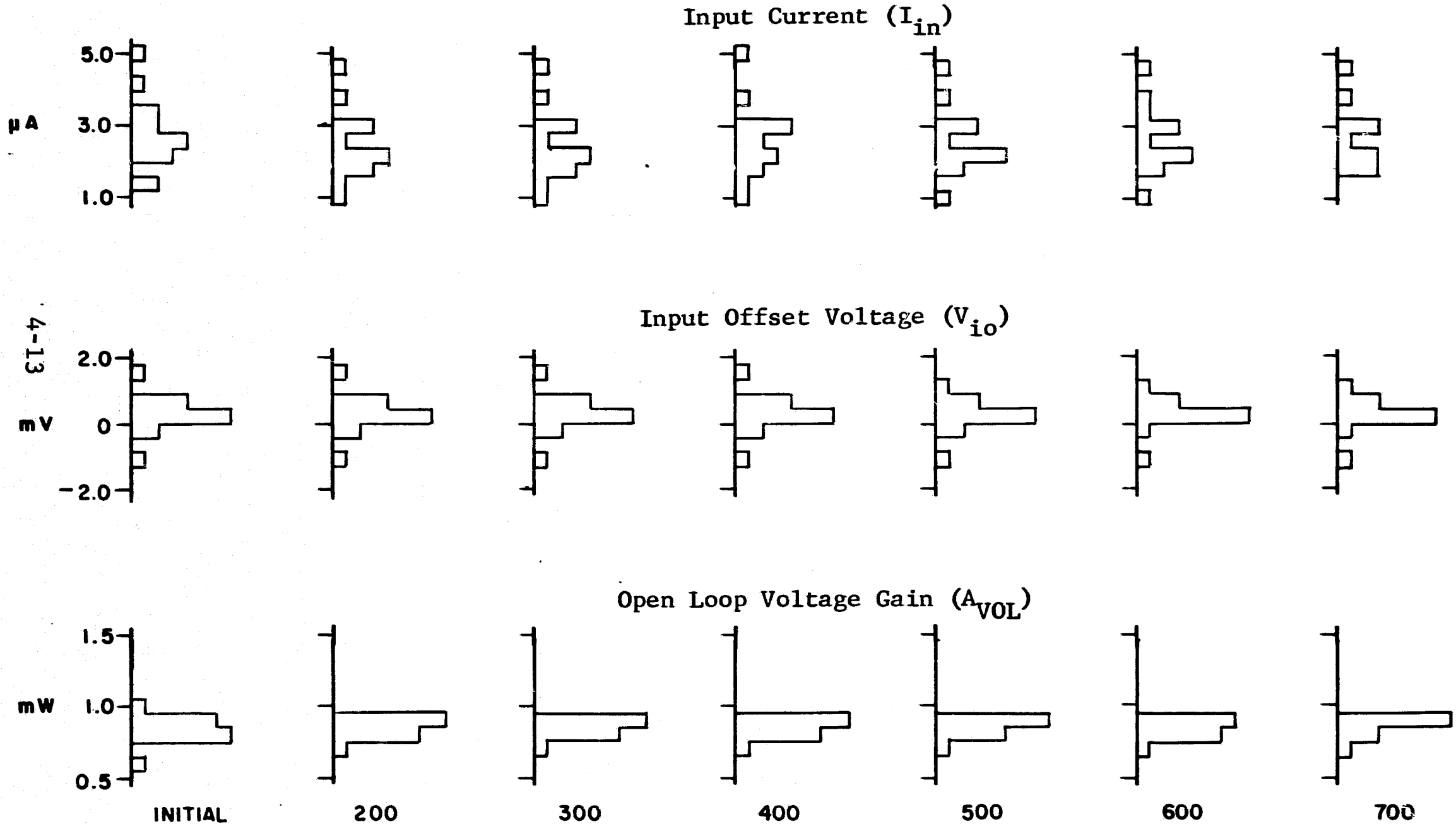


Figure 4-7. Power Step Stress Test, MC1530
T_A = 125°C
Sample Size = 15

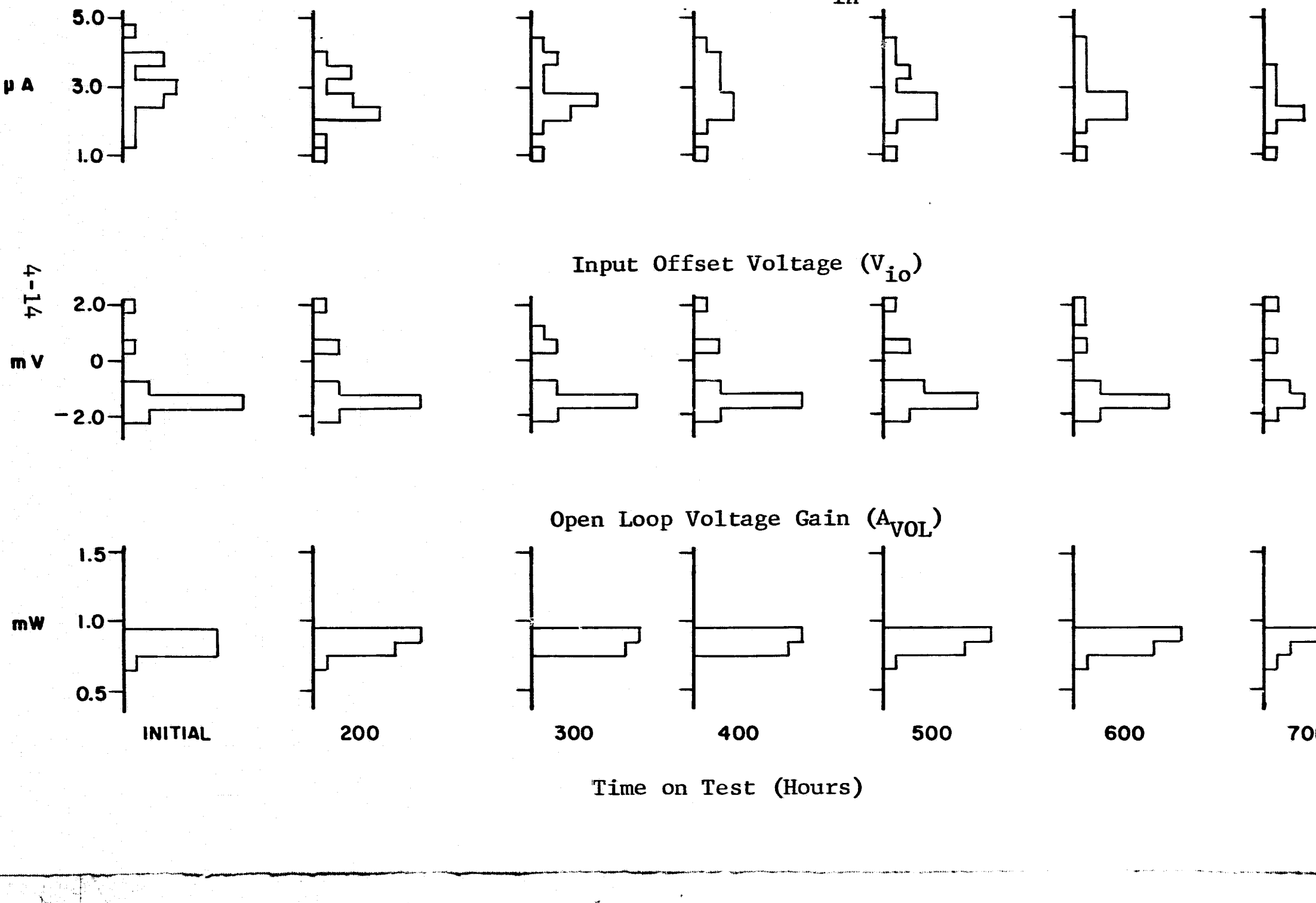


Figure 4-8. Temperature Cycling Test, MC1530
Sample Size = 15

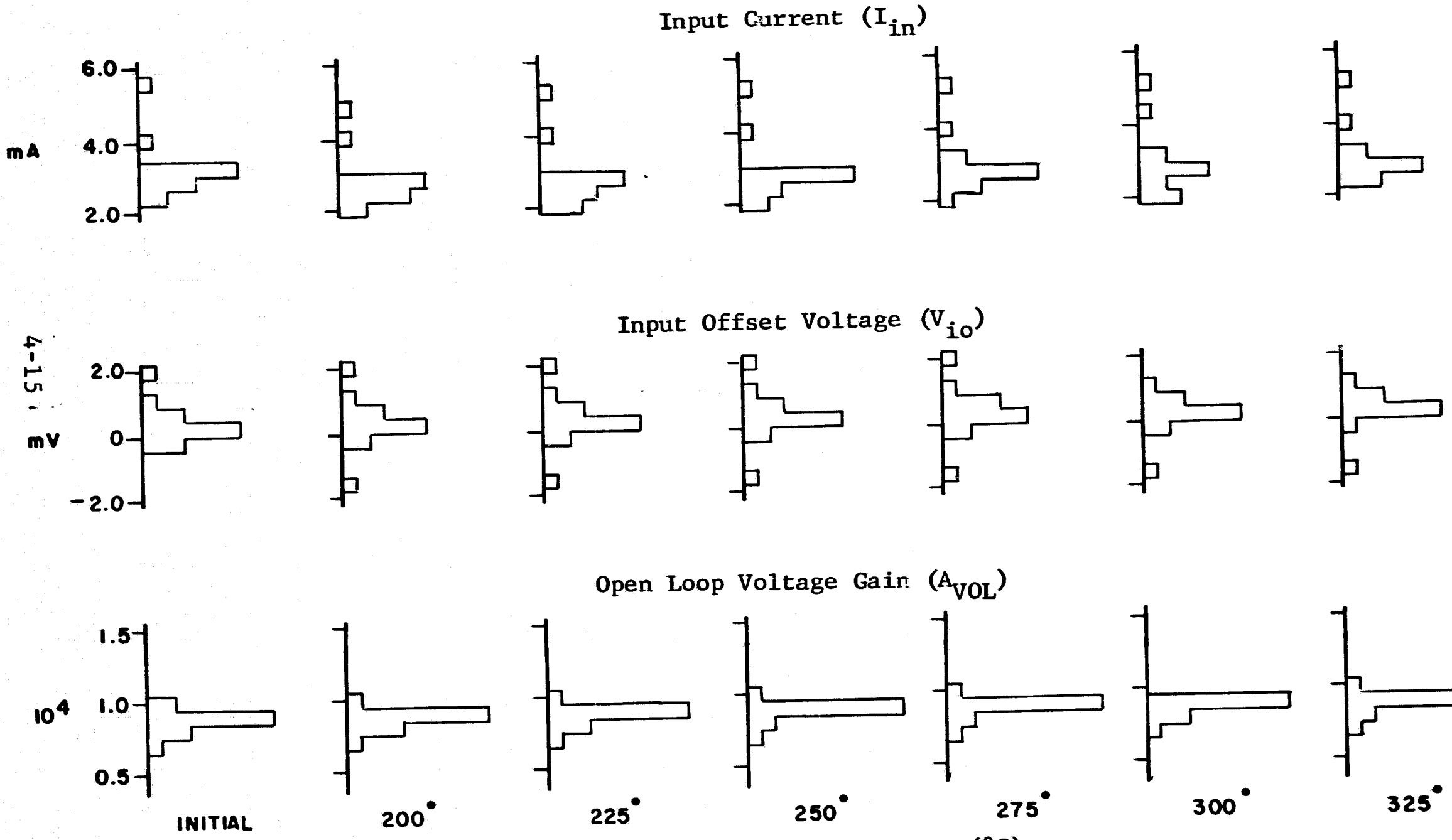


Figure 4-9. Mechanical Sequence, MC1530
Sample Size = 25

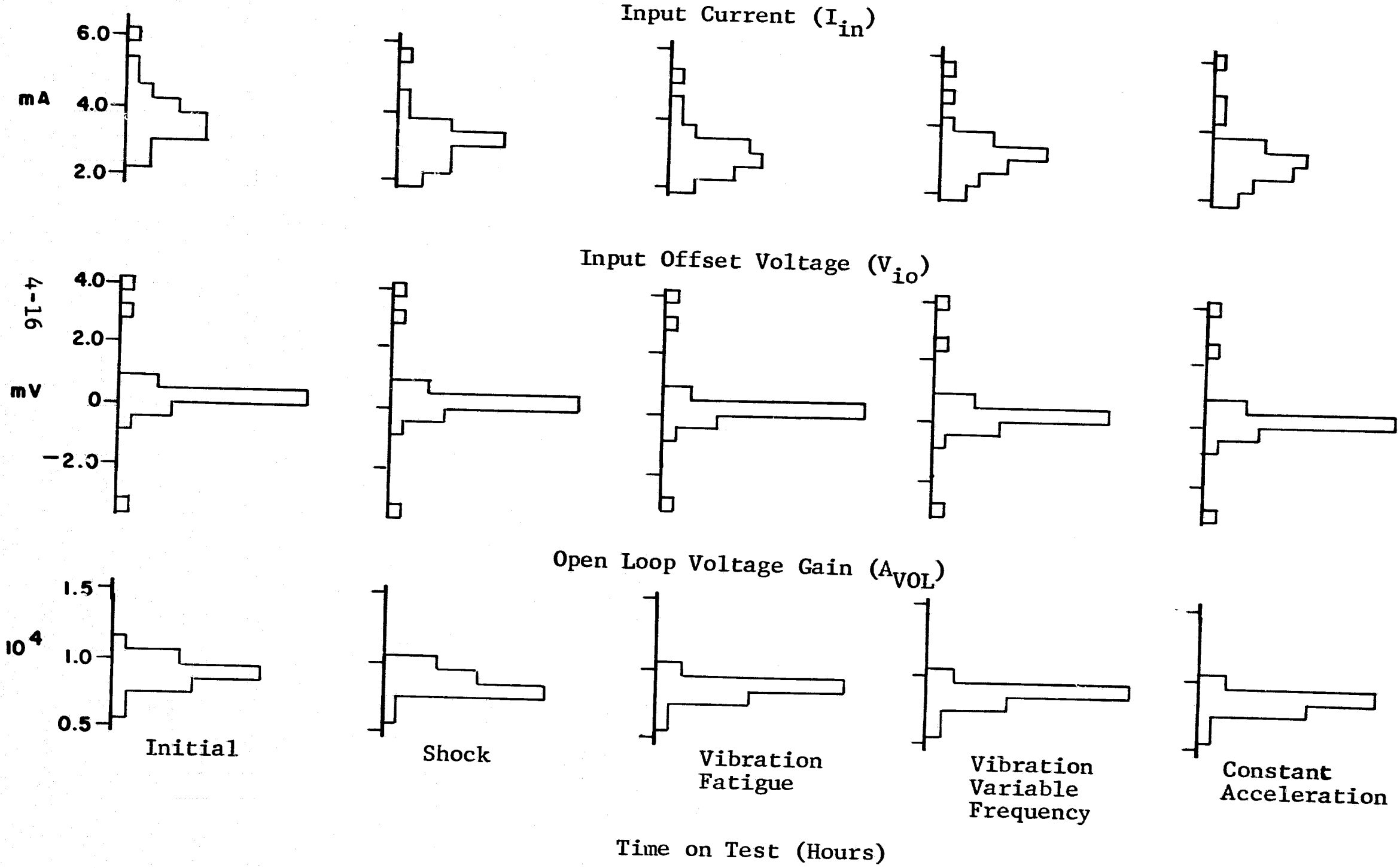
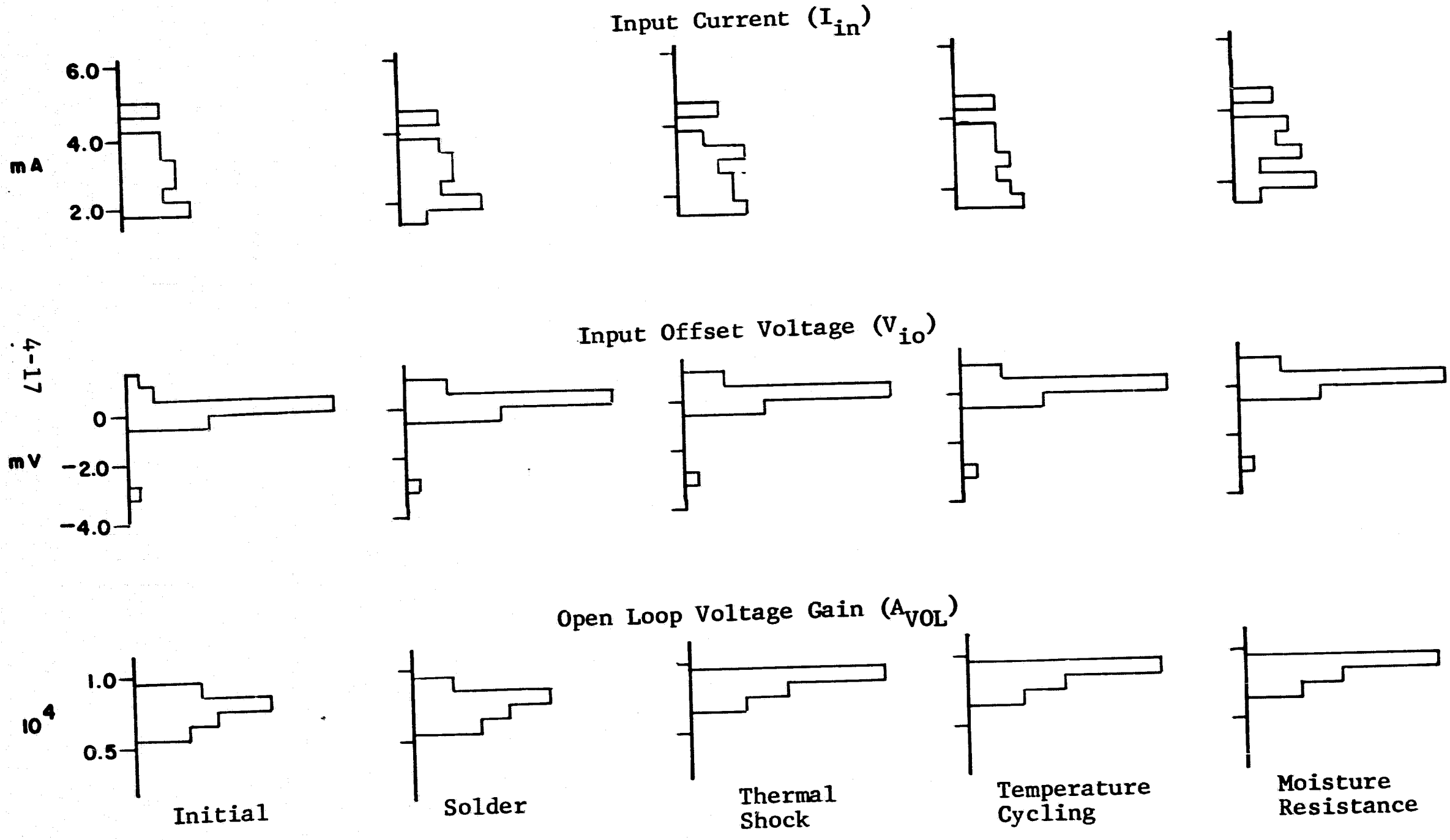


Figure 4-10. Thermal Sequence, MC1530
Sample Size = 25



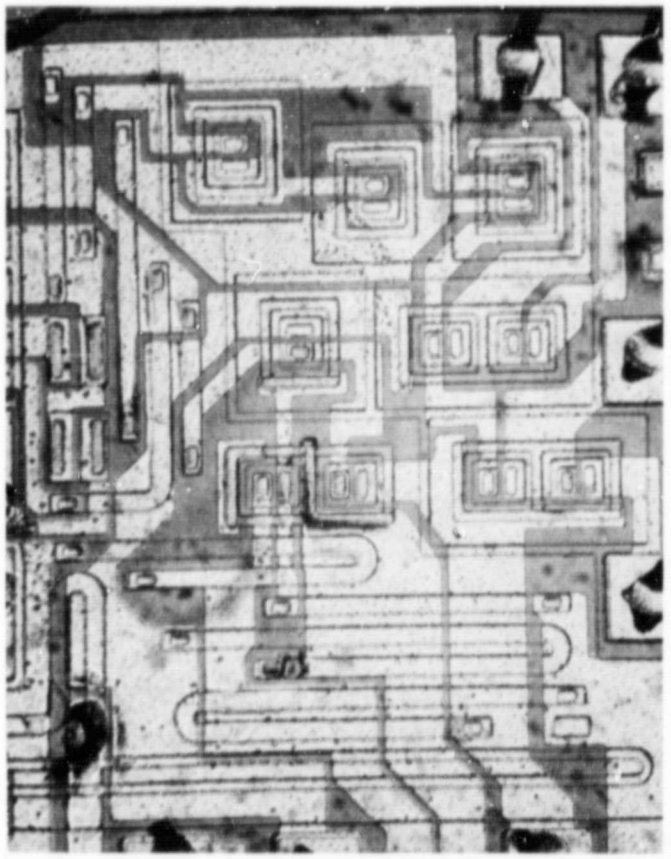


Figure 4-11. Unit No. 171--Failed at 800 mW Step Following Temperature Step Stress Test

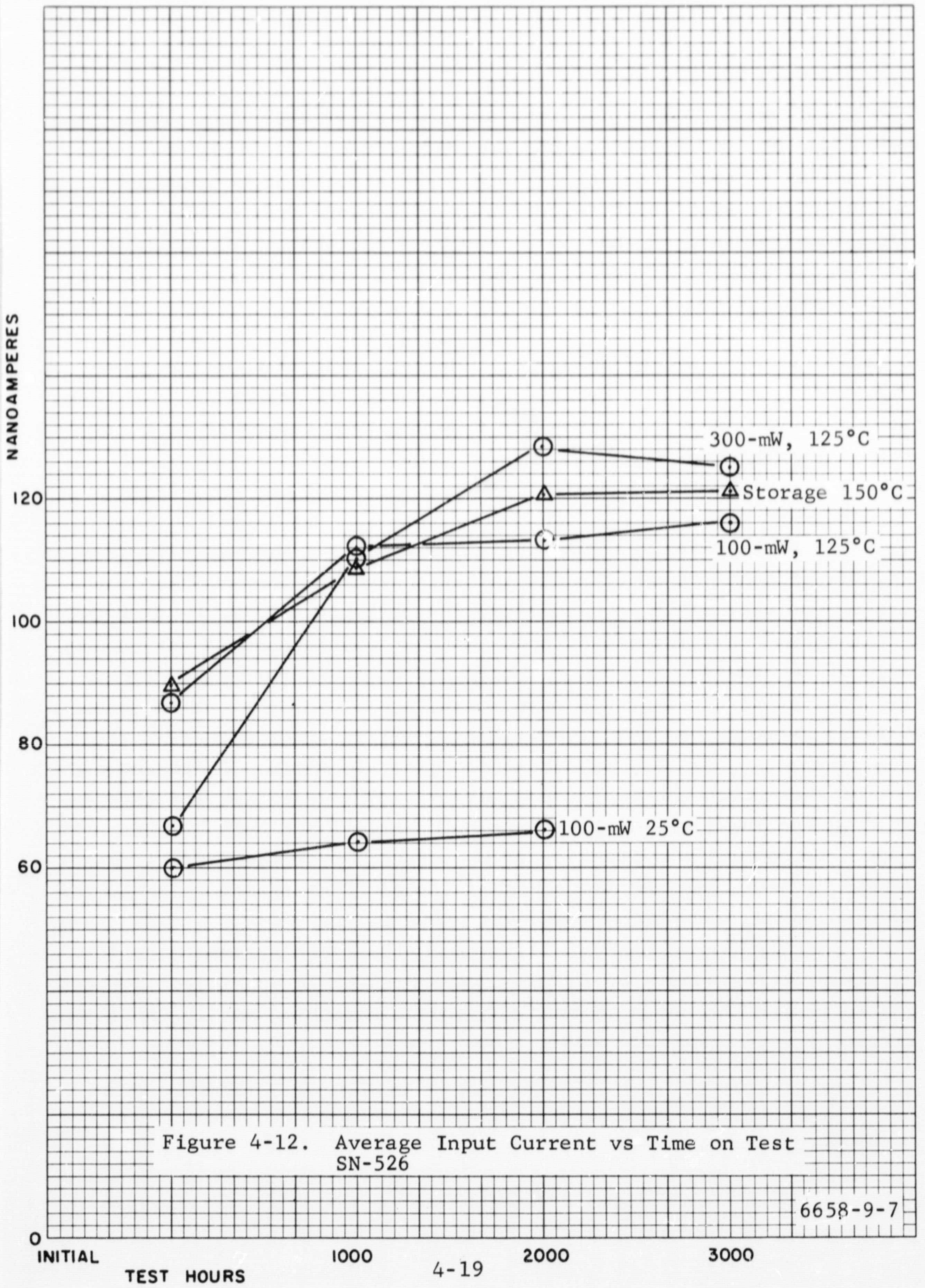


Figure 4-12. Average Input Current vs Time on Test SN-526

stable. This may possibly be explained by recognizing that the SN-526 employs a Darlington input and that the temperature may be degrading the low-current common emitter gain by affecting the surface around the p-n junction regions. The effects of temperature related to surface concentrations of aluminum and oxygen ions and other forms of surface impurities has been the subject of many extensive investigations and it is probably that temperature is affecting the Darlington inputs in just this manner. Surface inversion did not appear to be taking place, for there was no input current recovery phenomena as a result of bake-out. In fact, this degradation took place during a storage life test. This change is accomplished within the first 1000 hours and very little degradation occurs after that. No devices degraded enough to have failed the limits originally selected.

Another failure mode was detected in the storage life test, the storage temperature step stress tests, and the temperature step stress test cells that is usually found in temperature tests when gold and aluminum metal interfaces occur. This failure mode is the occurrence of intermetallics commonly referred to as "purple plague" but also consisting of compounds other than Au_2Al. The rate of occurrence of these failures was not significantly different for either of the three devices using this interconnecting metal system. A step stress plot of these three parts for the temperature step stress and the temperature cycling tests are found in Figures 4-13 and 4-14. There appears to be little difference in the effects of temperature stresses on ball bonded leads and wedge bonded leads. Pictures of three of the failures opened and photographed are shown in Figures 4-15, 4-16, and 4-17. Clearly the gold-aluminum intermetallics are present and, if not the principal cause of failure, were present in sufficient quantities to weaken the bonds so that subsequent stressing easily failed the circuit.

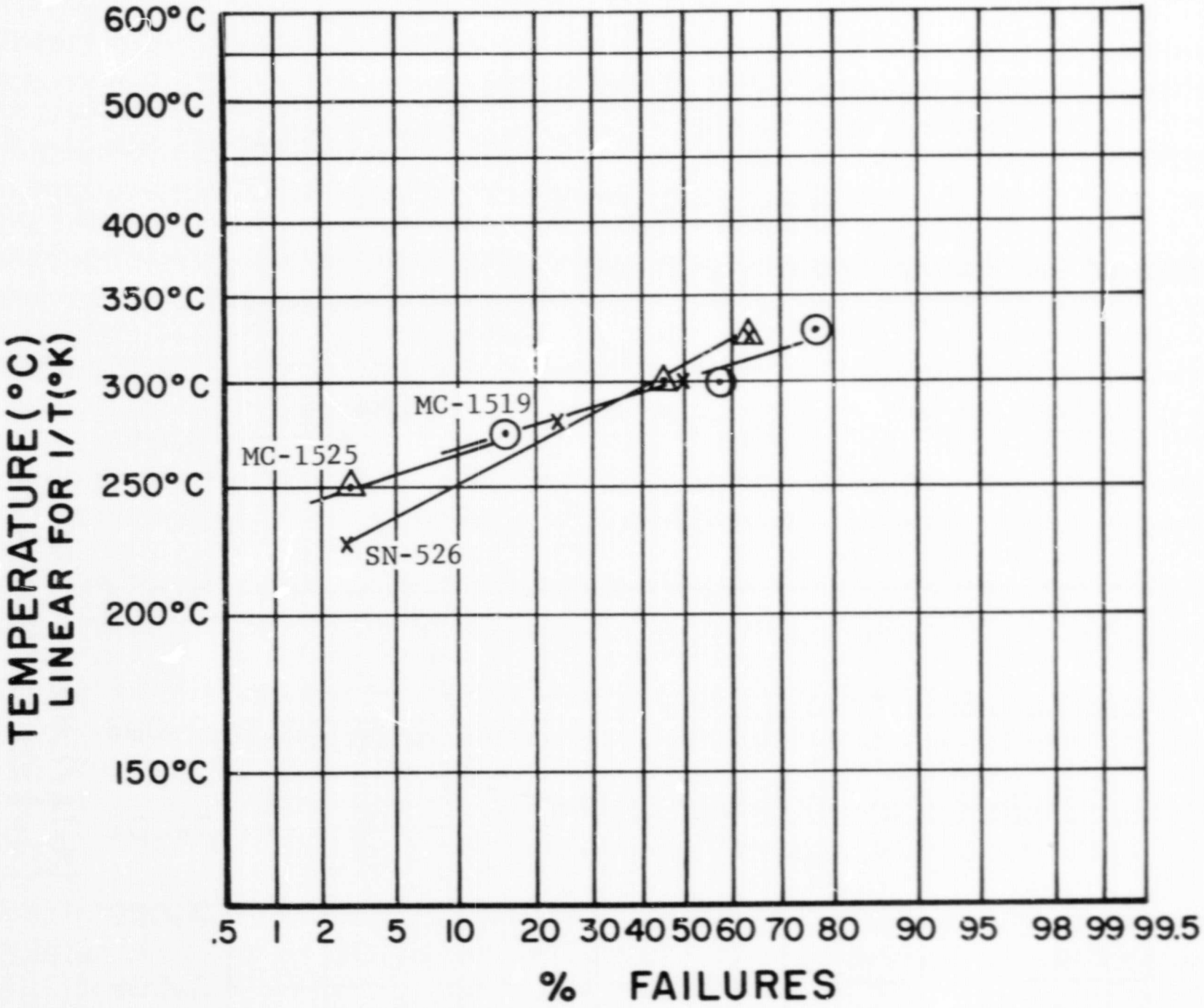


Figure 4-13. Temperature Step Stress Test
Sample Size is 15 Samples Each Type
Time on Test = 48 Hours

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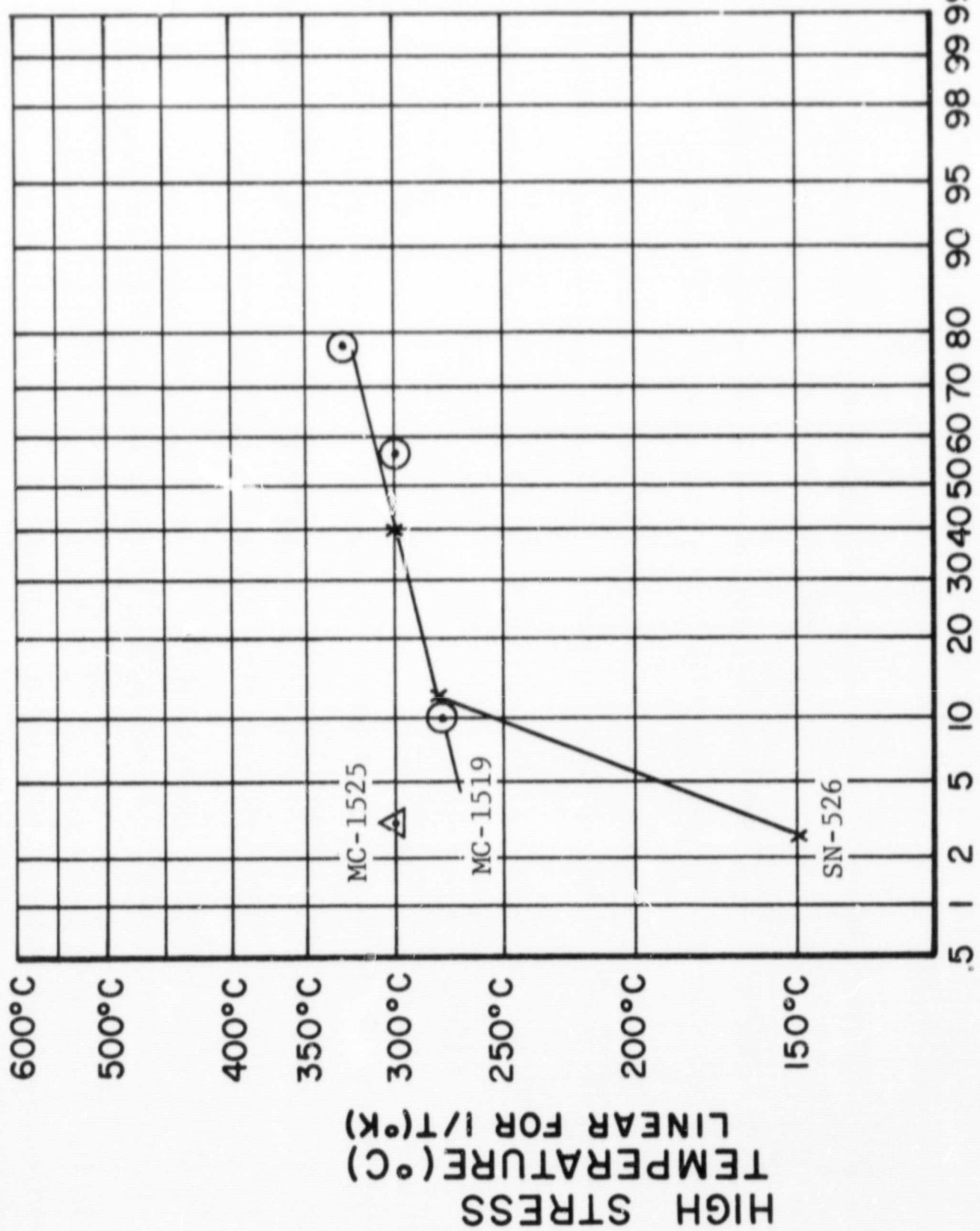
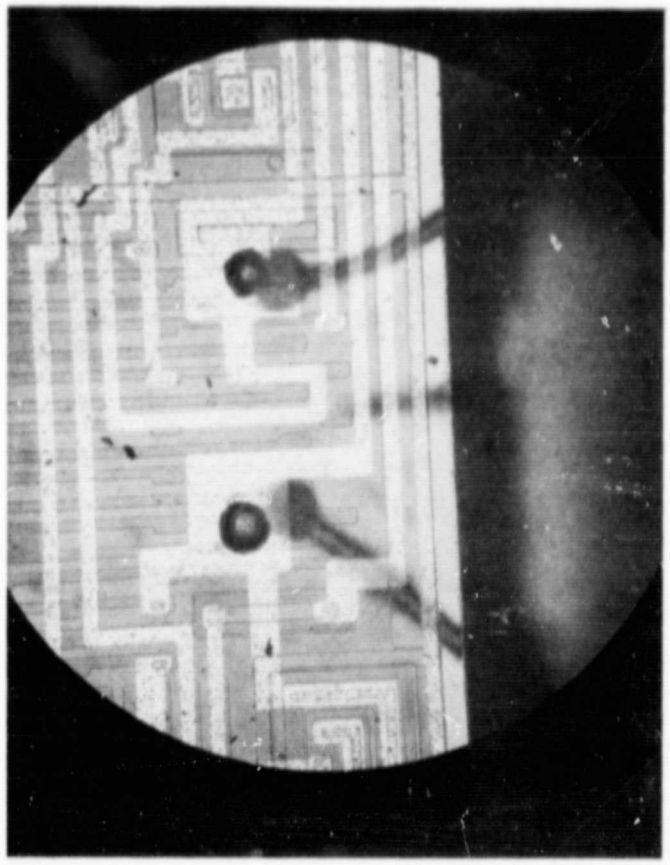


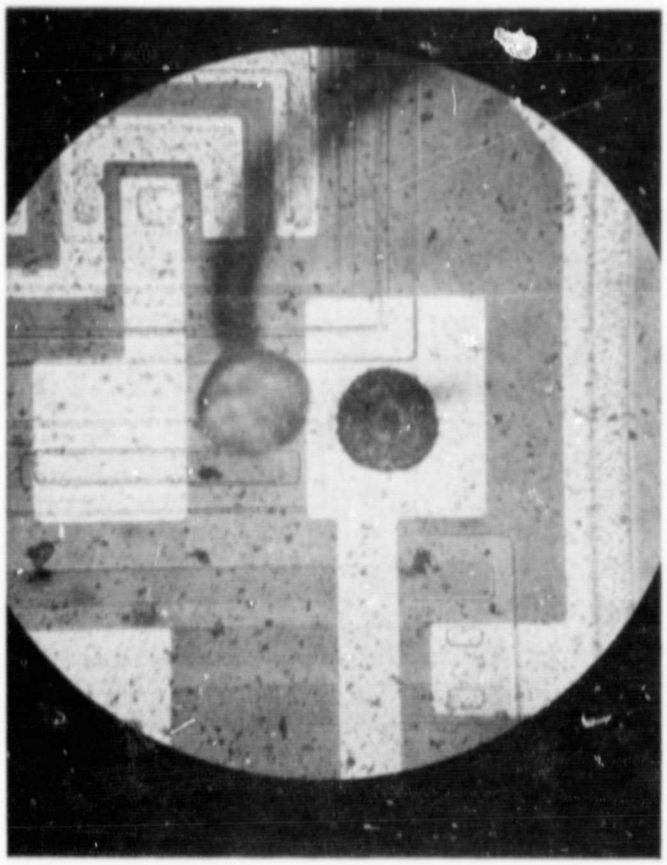
Figure 4-14. Temperature Cycling Step Stress Test
Sample Size is 15 for Each Device
Time on Test = 48 Hours

6660-9-7



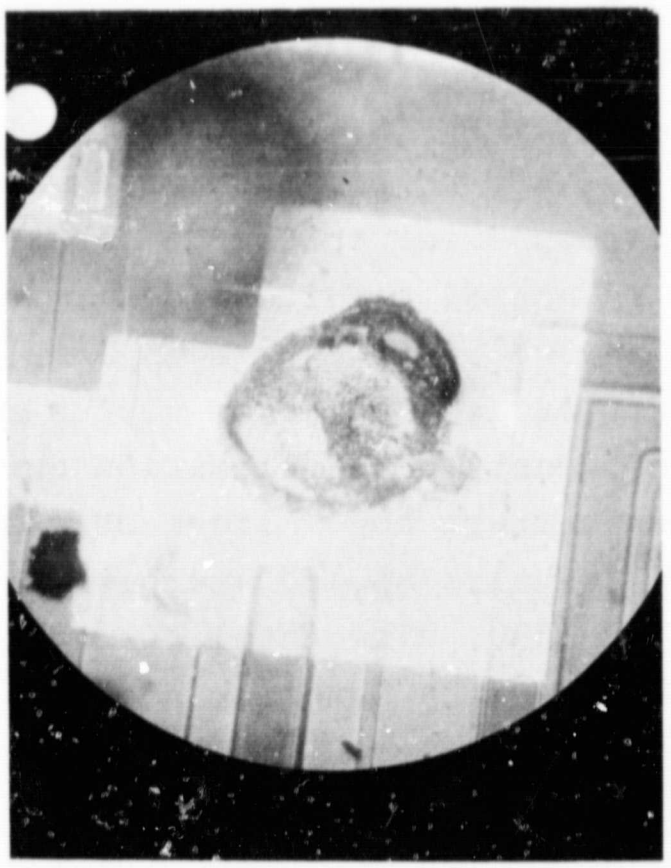
NOTE: The suspected cause of failure is assumed to open lead wire contact resulting from degradation at the wire bond-pad interface resulting from Au-Al intermetallic compounds.

Figure 4-15. Unit No. 67--Failed Temperature Cycling After +300°C Step



NOTE: The suspected cause of failure is assumed to be open lead wire contact resulting from degradation at the wire bond-pad interfac resulting from Au-Al intermetallic compounds.

Figure 4-16. Unit No. 9--Failed Temperature Cycling After +300°C Step



NOTE: The suspected cause of failure is assumed to be open lead wire contact resulting from degradation at the wire bond-pad interface resulting from Au-Al intermetallic compounds.

Figure 4-17. Unit No. 155--Failed 150°C Storage Life Test After 3000 Hours

The SN-526 did the best in both power step stress tests as shown in Table 4-II. These circuits were best able to distribute the additional power requirements throughout their various elements. The MC-1530 concentrated the greatest share of its load throughout its output section; therefore it is not unexpected that metallization wearout occurred at the 600 through 800 milliwatt stress levels. Yet the SN-526 was far superior to the MC-1530F in these power tests. The reason for this is not difficult to determine.

In any power stress test, the test sample is subjected to active region current density, metallization current density as well as the other temperature and voltage stresses. The SN-526 has an absolute value of 24 volts applied across the device as opposed to 12 volts for the MC-1530. The total circuit current drain for the SN-526 at each stress step was only one-half that of the MC-1530. Also as the stresses increased, the twin output function of the SN-526 was utilized, thereby dividing the current density applied to each metal strip and active component still further. Finally, the SN-526 die had 4.5 times the surface area of the MC-1530F.

This resulted in less total current drain, less individual current drain, more components to accept the current loads and more silicon dice to act as a heat sink for that thermal energy generated at the die surface. This, then, should have resulted in a cooler die, less stress and a greater likelihood of survival at these stresses.

Table 4-II summarized the results of the SN-526 test program using the limits found in Section 3.1 as its guide.

Figures 4-18 through 4-37 use histograms to show the parameter stability of the SN-526 on all tests.

OPERATING LIFE TEST
SN526
TA = 125°C Pd = 100 mW
Sample Size = 25

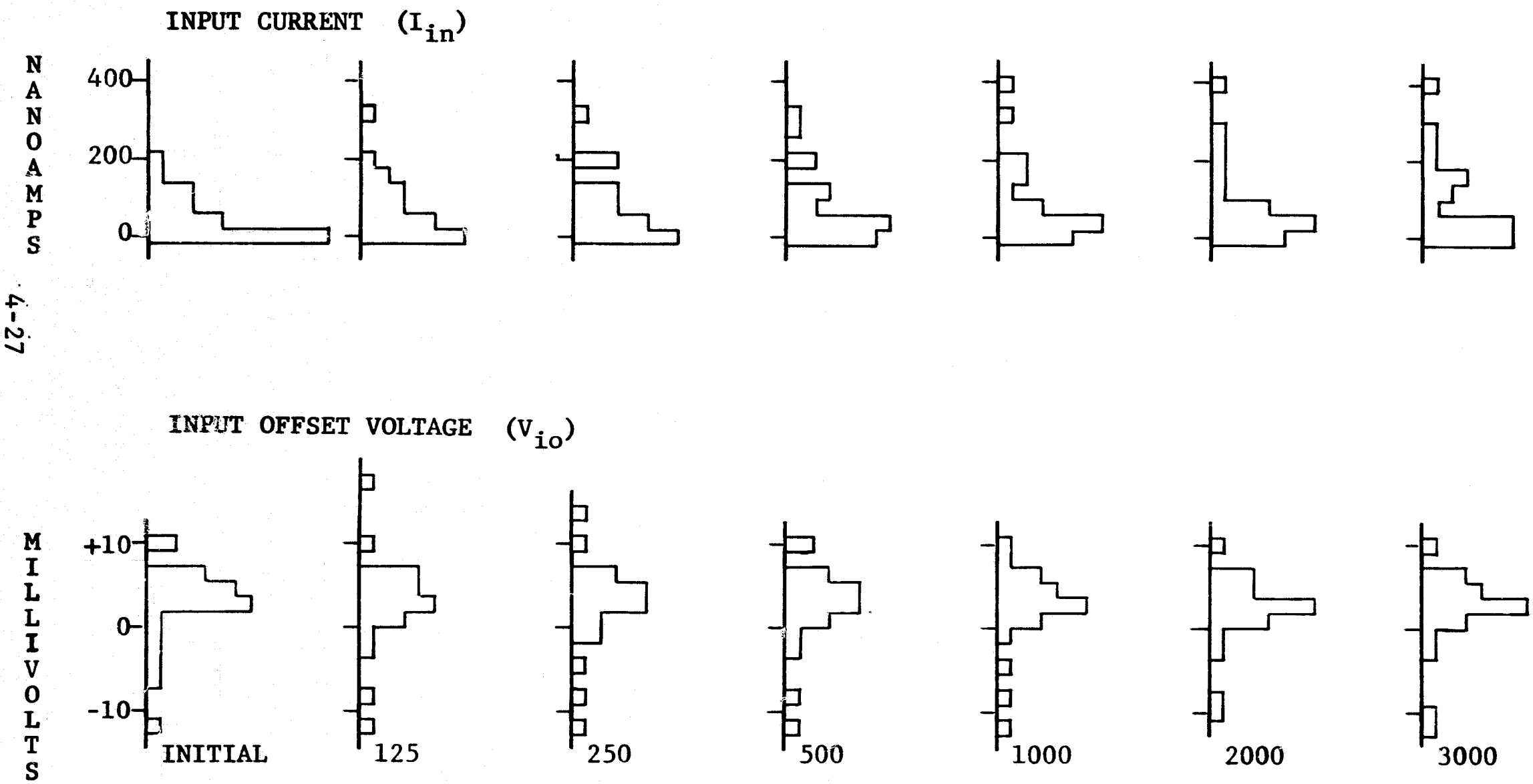
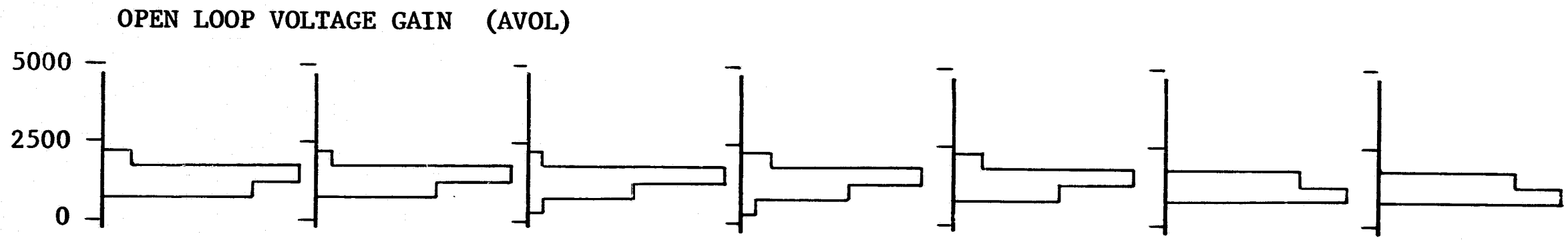
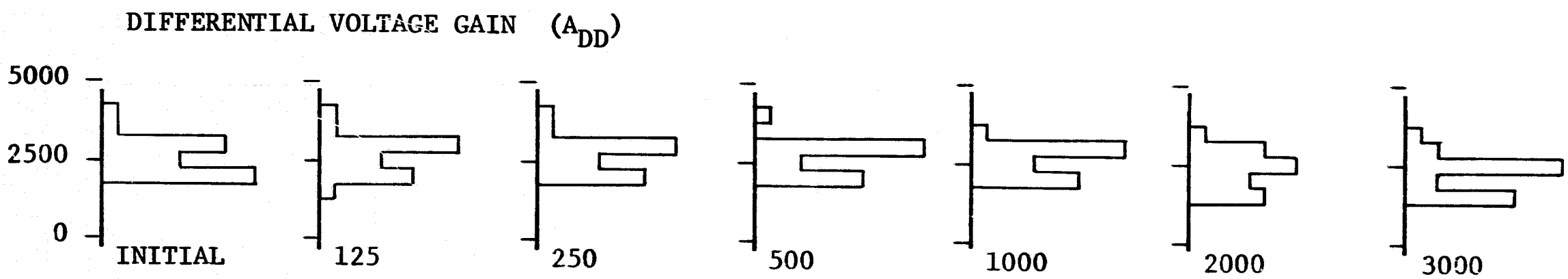


Figure 4-18

OPERATING LIFE TEST
SN526
TA = 125°C Pd = 100 mW
Sample Size = 25

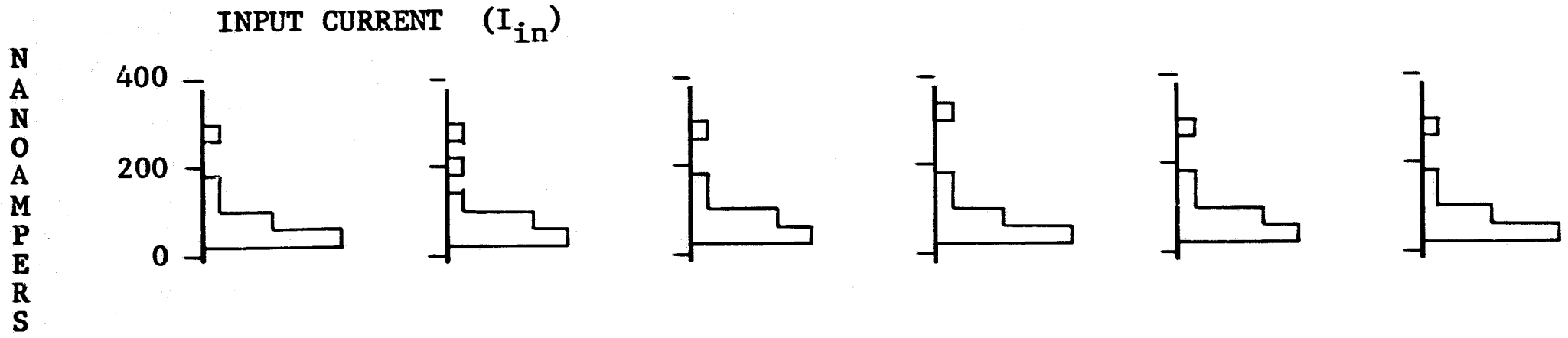


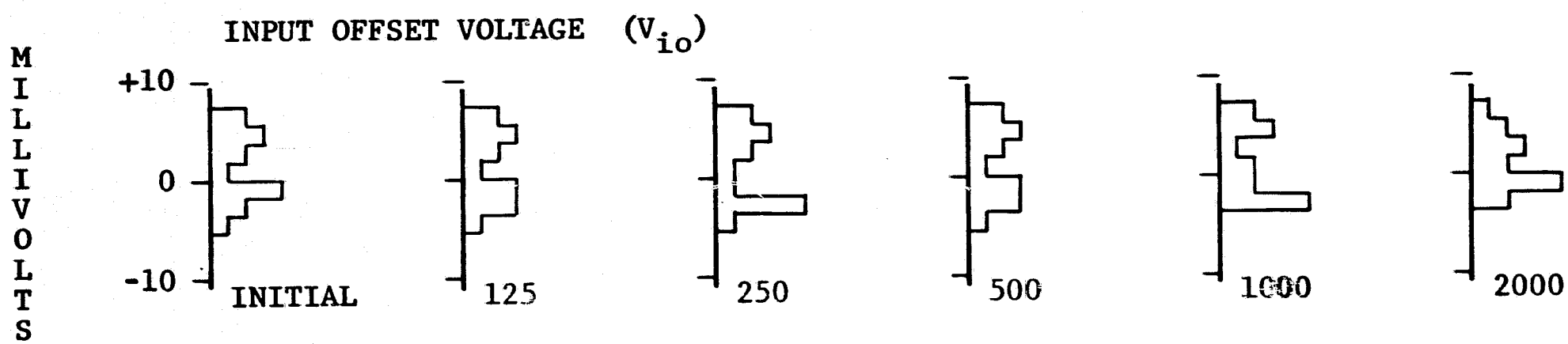


TIME ON TEST (HOURS)

Figure 4-19

OPERATING LIFE TEST
SN526
TA = 25°C Pd = 100 mW
Sample Size = 15





TIME ON TEST (HOURS)

Figure 4-20

OPERATING LIFE TEST
SN526
TA = 25°C Pd = 100 mW
Sample Size = 15

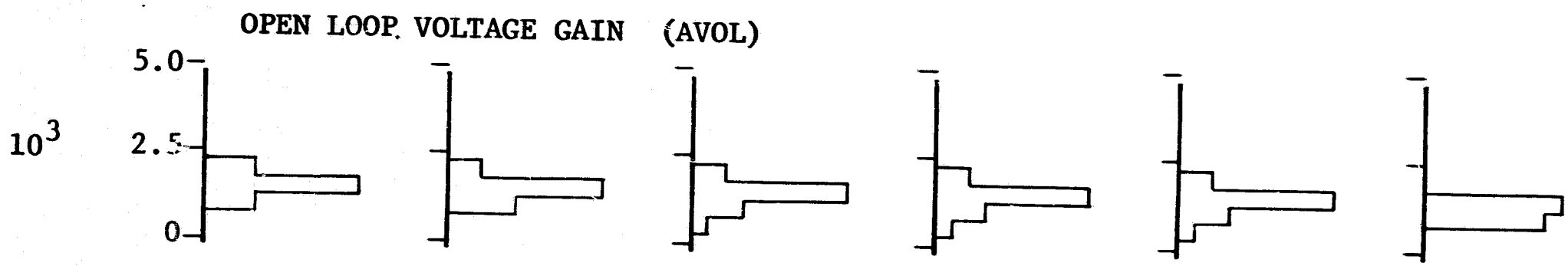


Figure 4-21

OPERATING LIFE TEST
SN526
TA = 125°C Pd = 300 mW
Sample Size = 25

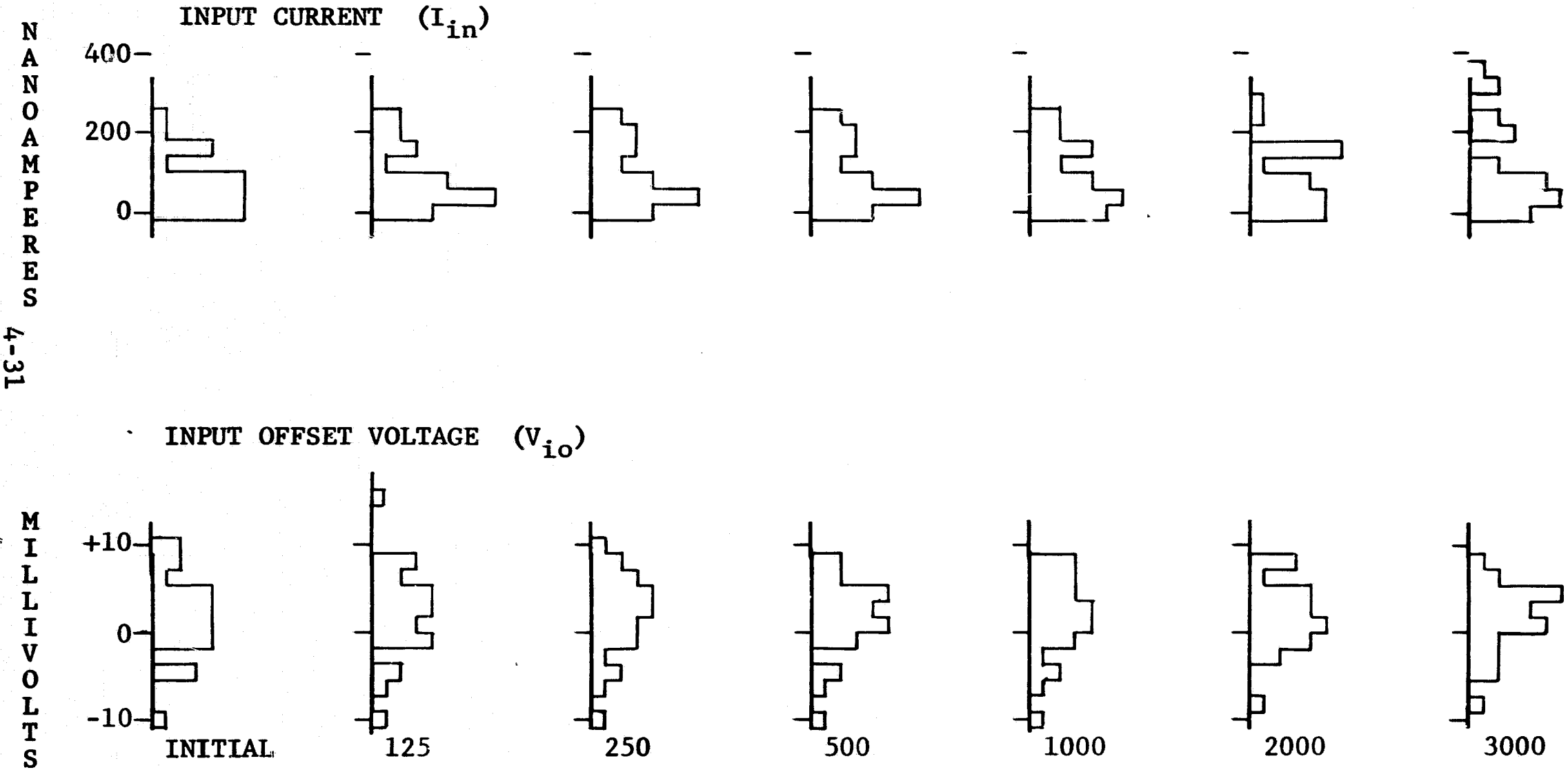
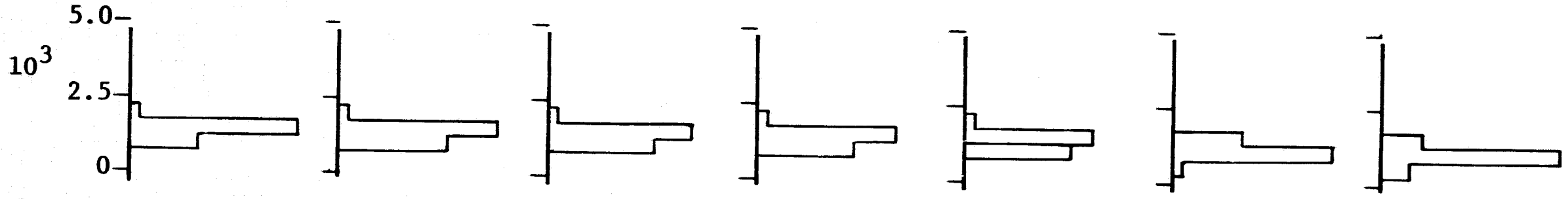


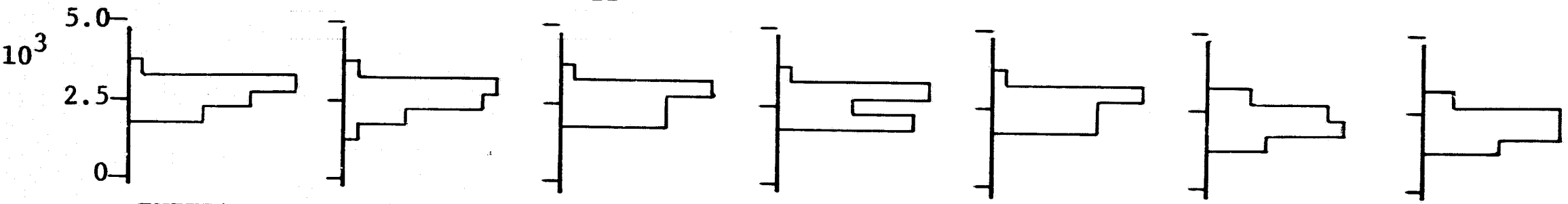
Figure 4-22

OPERATING LIFE TEST
SN526
TA = 125°C Pd = 300 mW
Sample Size = 25

OPEN LOOP VOLTAGE GAIN (AVOL)



DIFFERENTIAL VOLTAGE GAIN (A_{DD})



TIME ON TEST (HOURS)

Figure 4-23

STORAGE LIFE TEST
SN526
TA = 150°C
Sample Size = 15

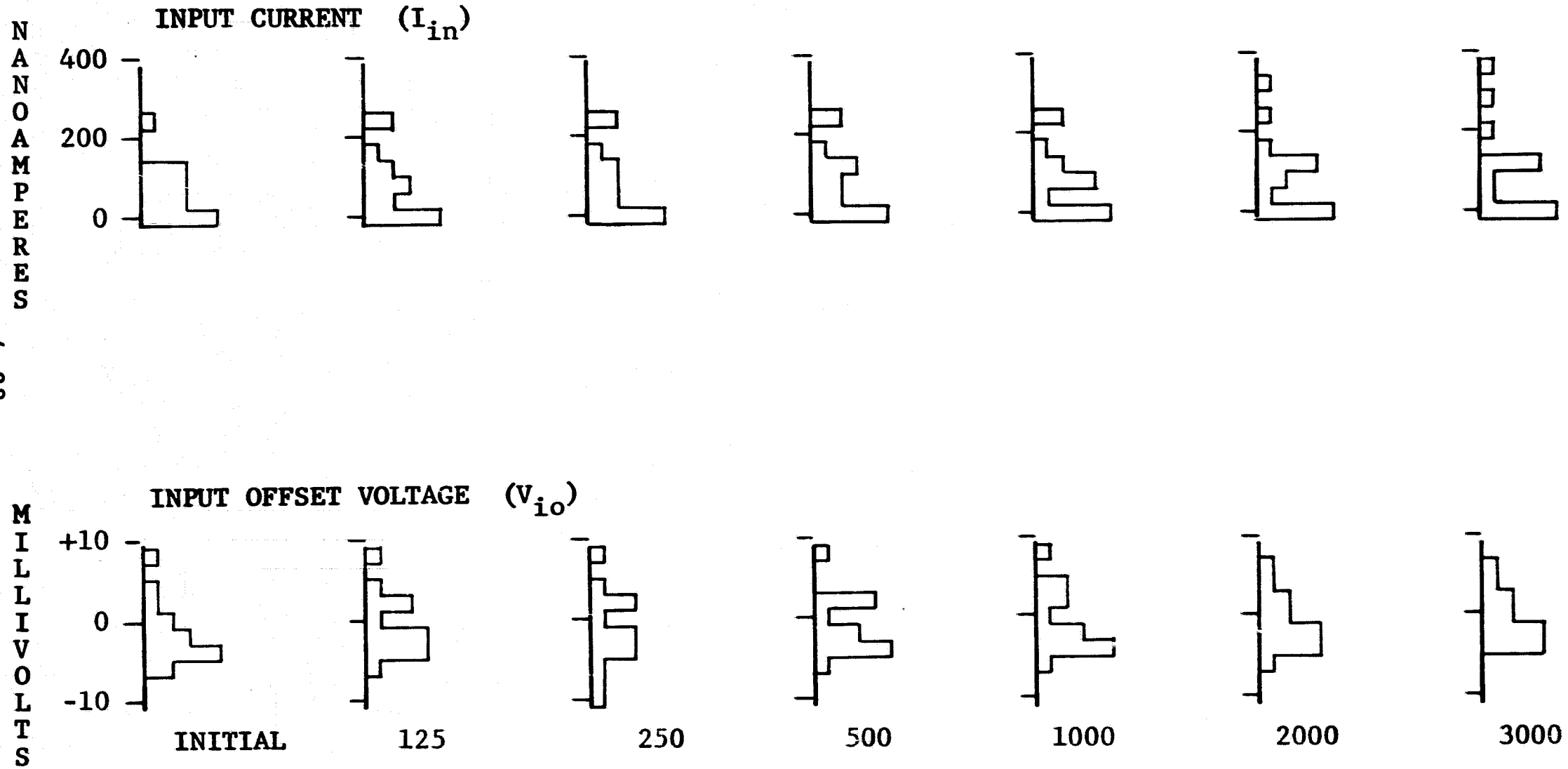
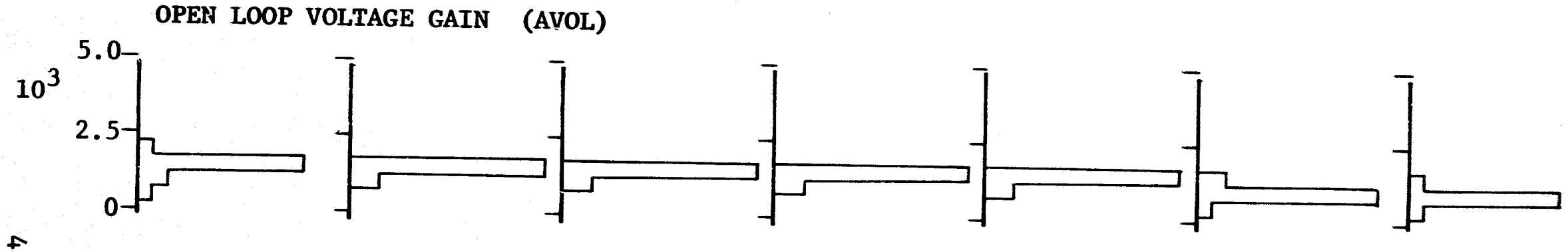


Figure 4-24

STORAGE LIFE TEST
SN526
TA = 150°C
Sample Size = 15



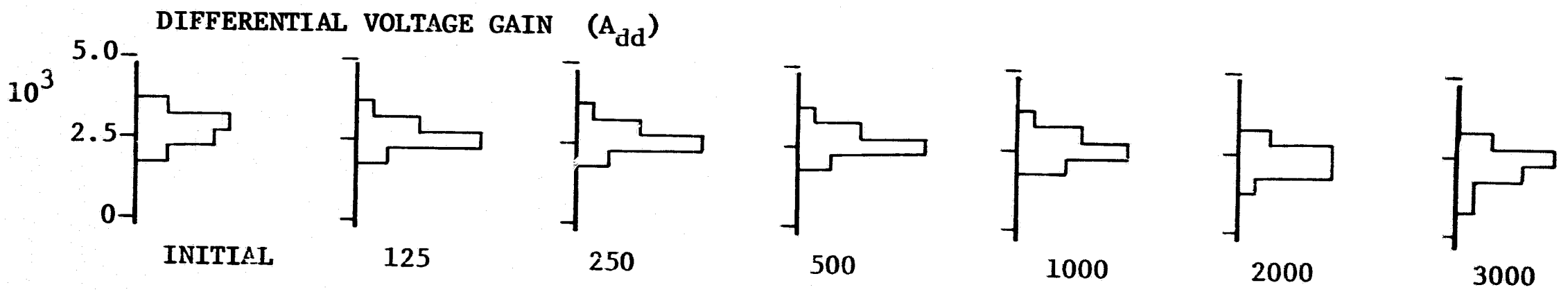


Figure 4-25

TEMPERATURE STEP STRESS TEST
SN526
Sample Size = 15

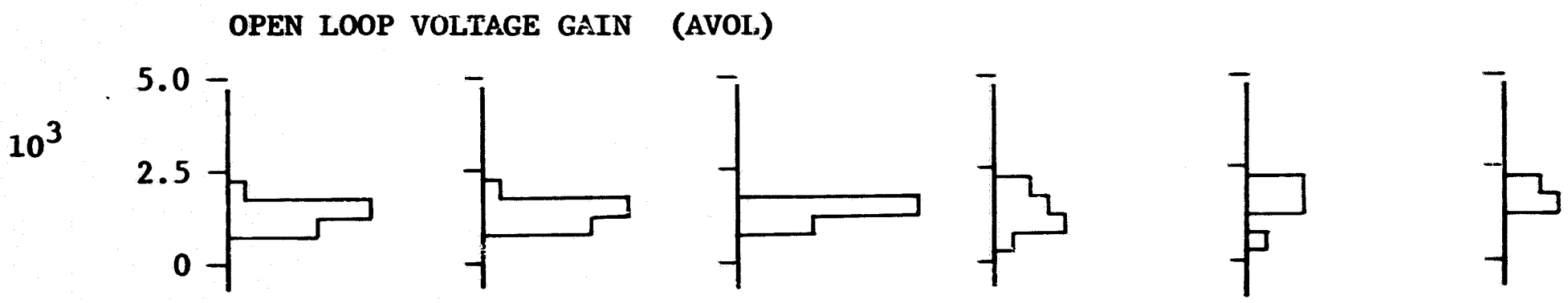


Figure 4-26

TEMPERATURE CYCLING TEST
SN526
Sample Size = 15

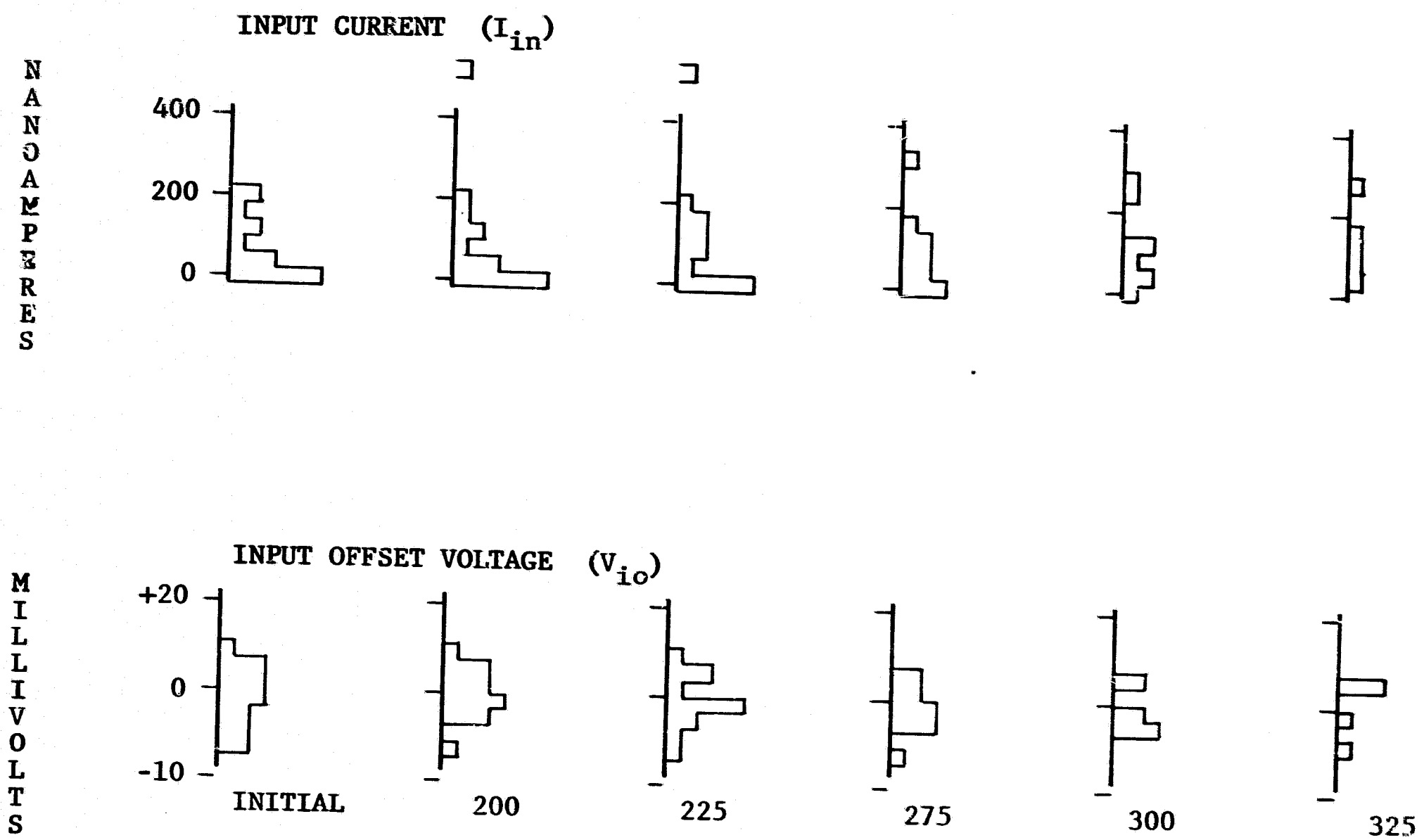


Figure 4-27

TEMPERATURE CYCLING TEST
SN526
Sample Size = 15

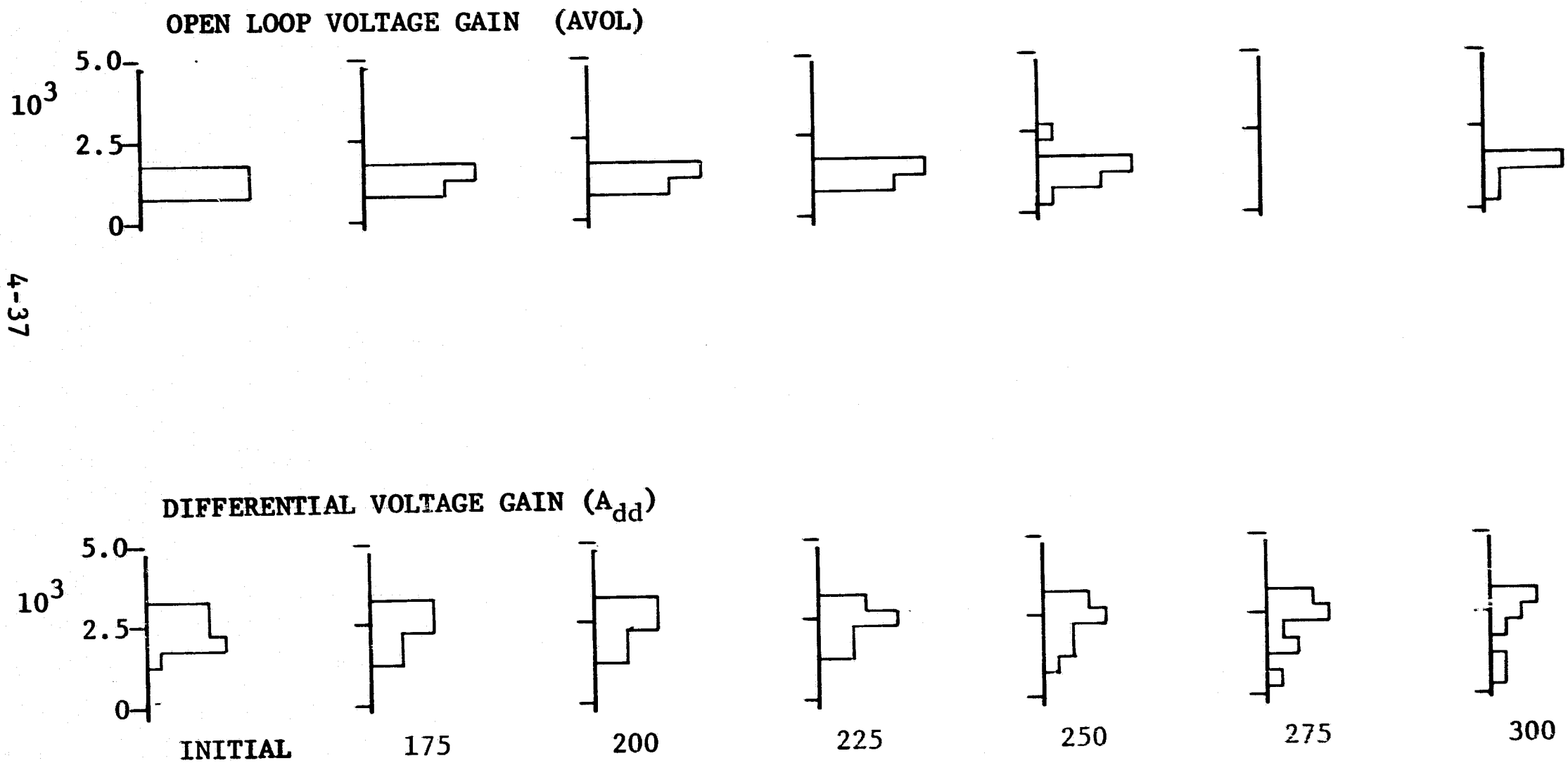


Figure 4-28

TEMPERATURE STEP STRESS TEST
SN526
Sample Size = 15

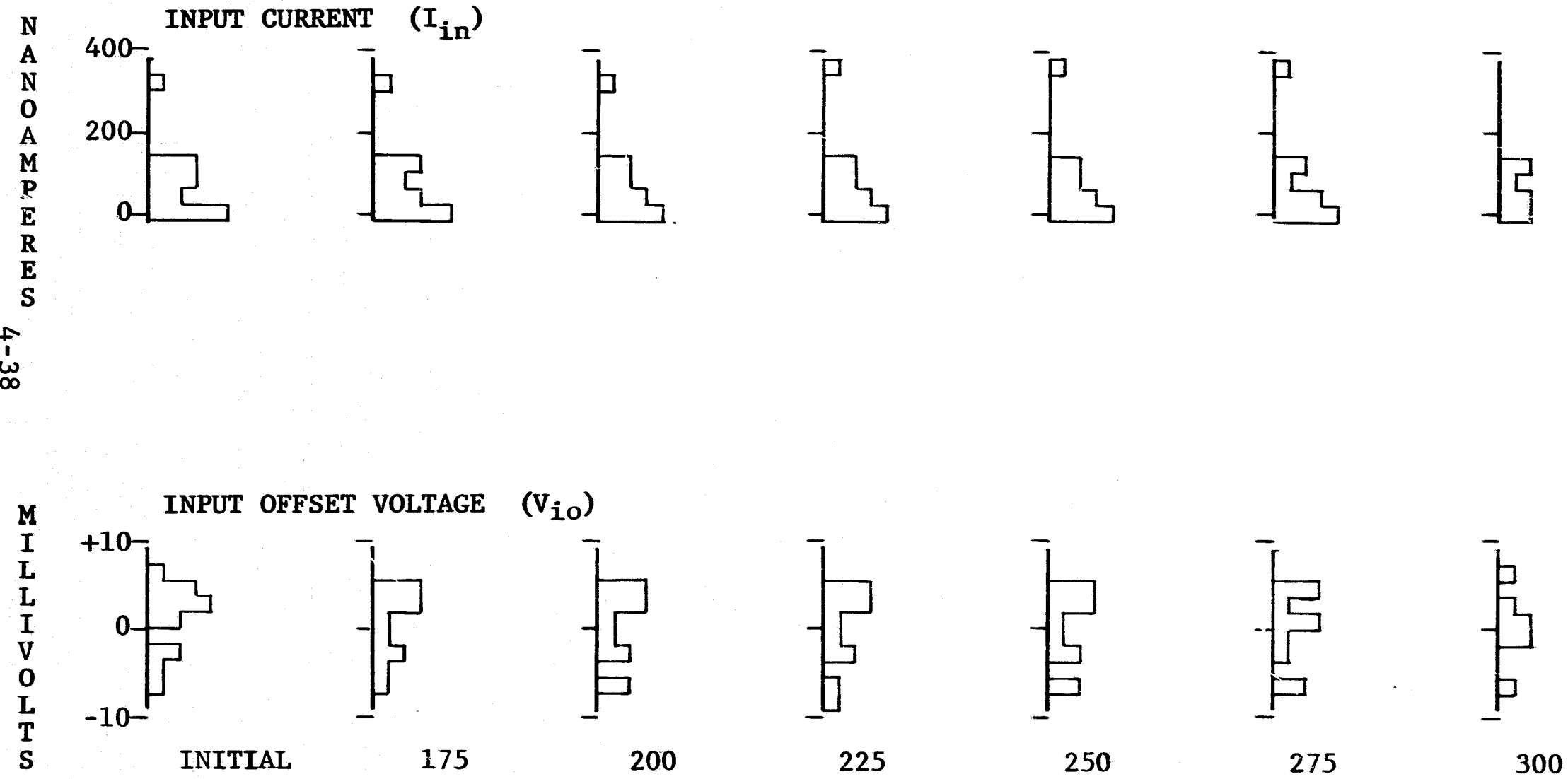


Figure 4-29

MECHANICAL SEQUENCE
SN526
Sample Size = 25

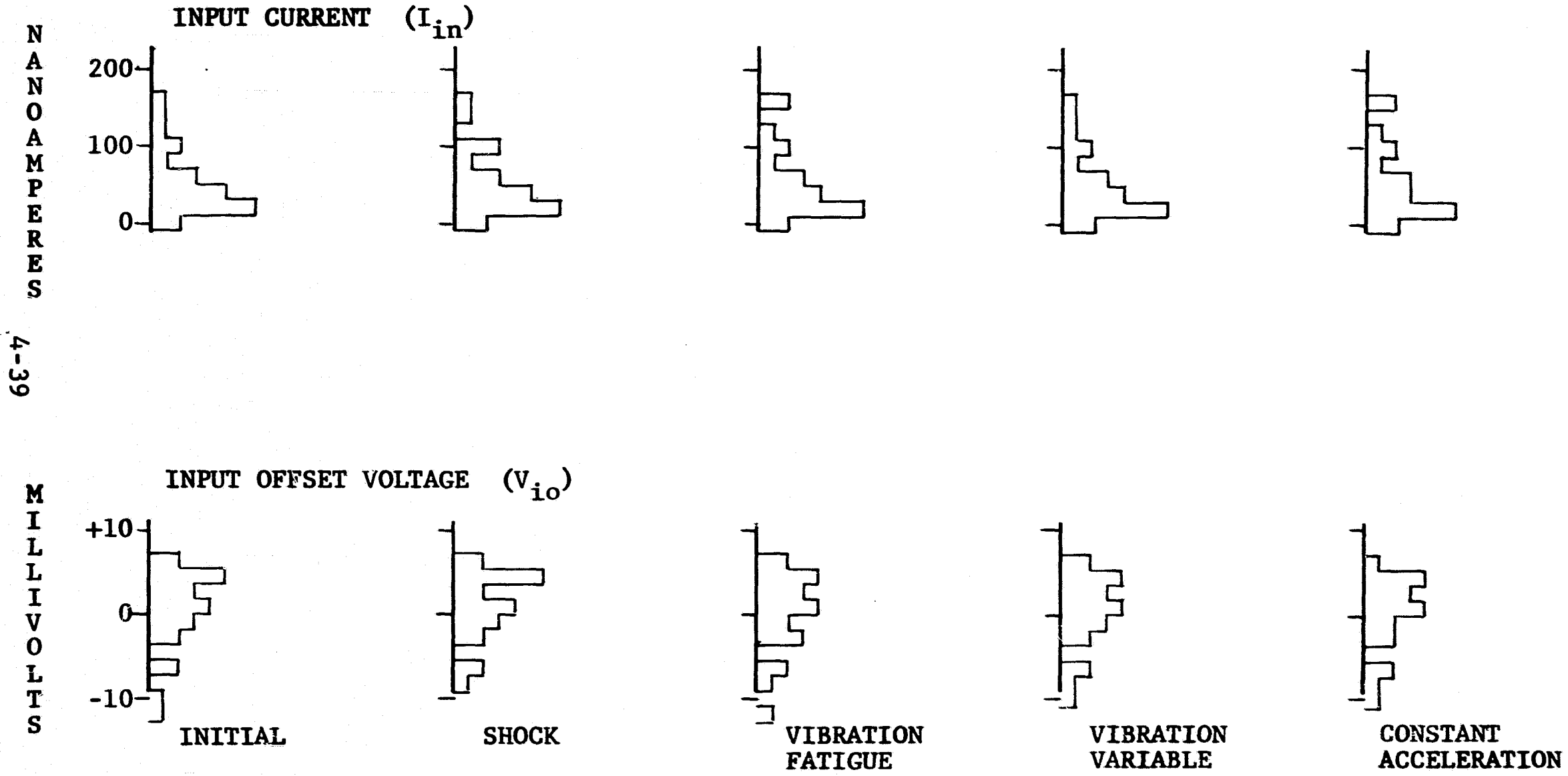
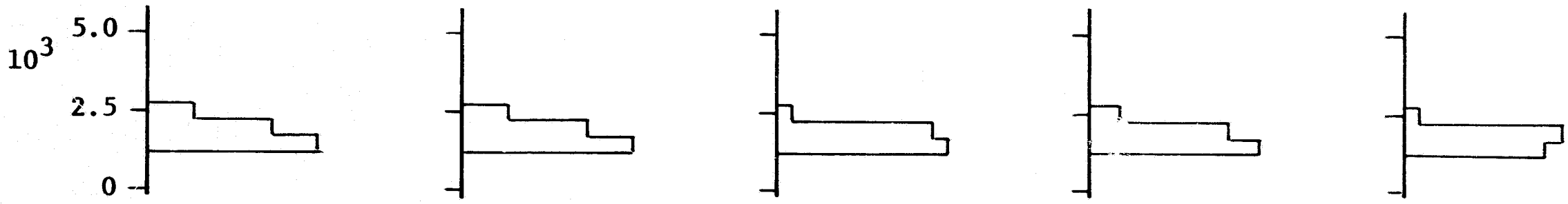


Figure 4-30

MECHANICAL SEQUENCE
SN526
Sample Size = 25

OPEN LOOP VOLTAGE GAIN (AVOL)



DIFFERENTIAL VOLTAGE GAIN (A_{dd})

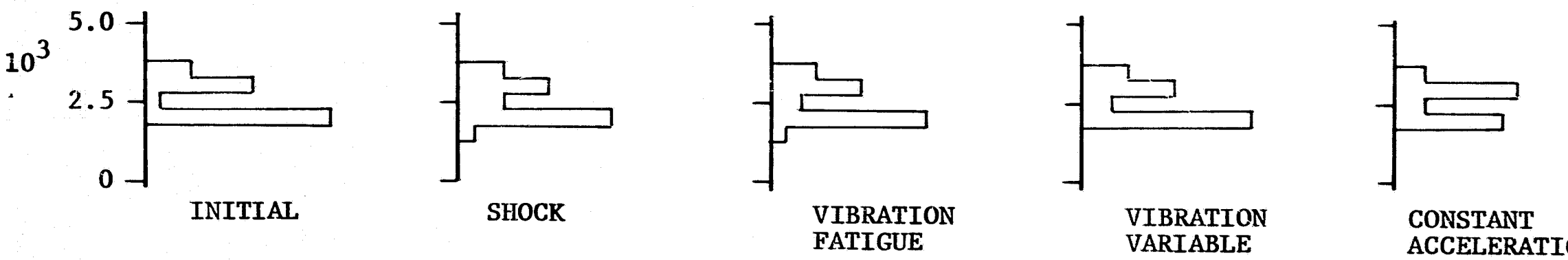


Figure 4-31

THERMAL SEQUENCE
SN526
Sample Size = 25

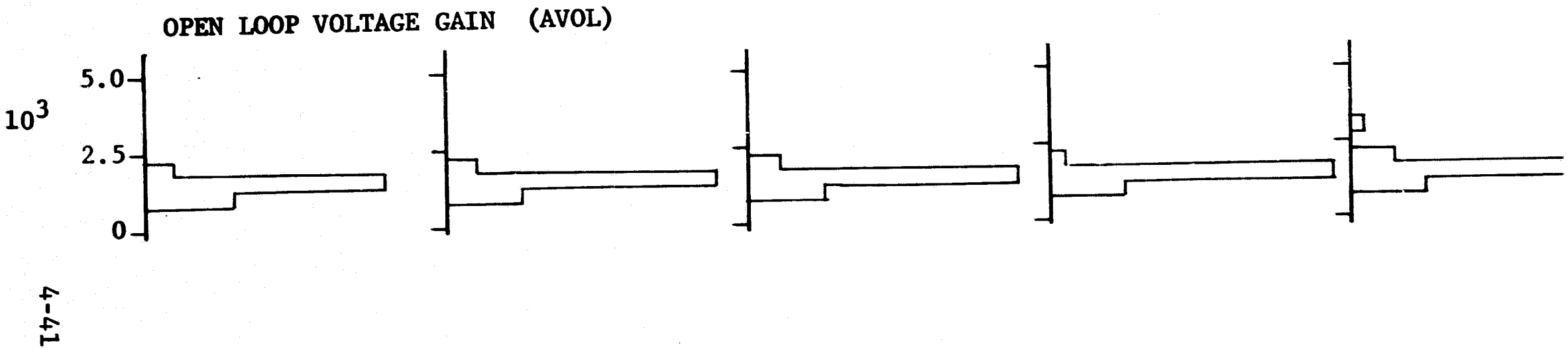


Figure 4-32

THERMAL SEQUENCE
SN526
Sample Size = 25

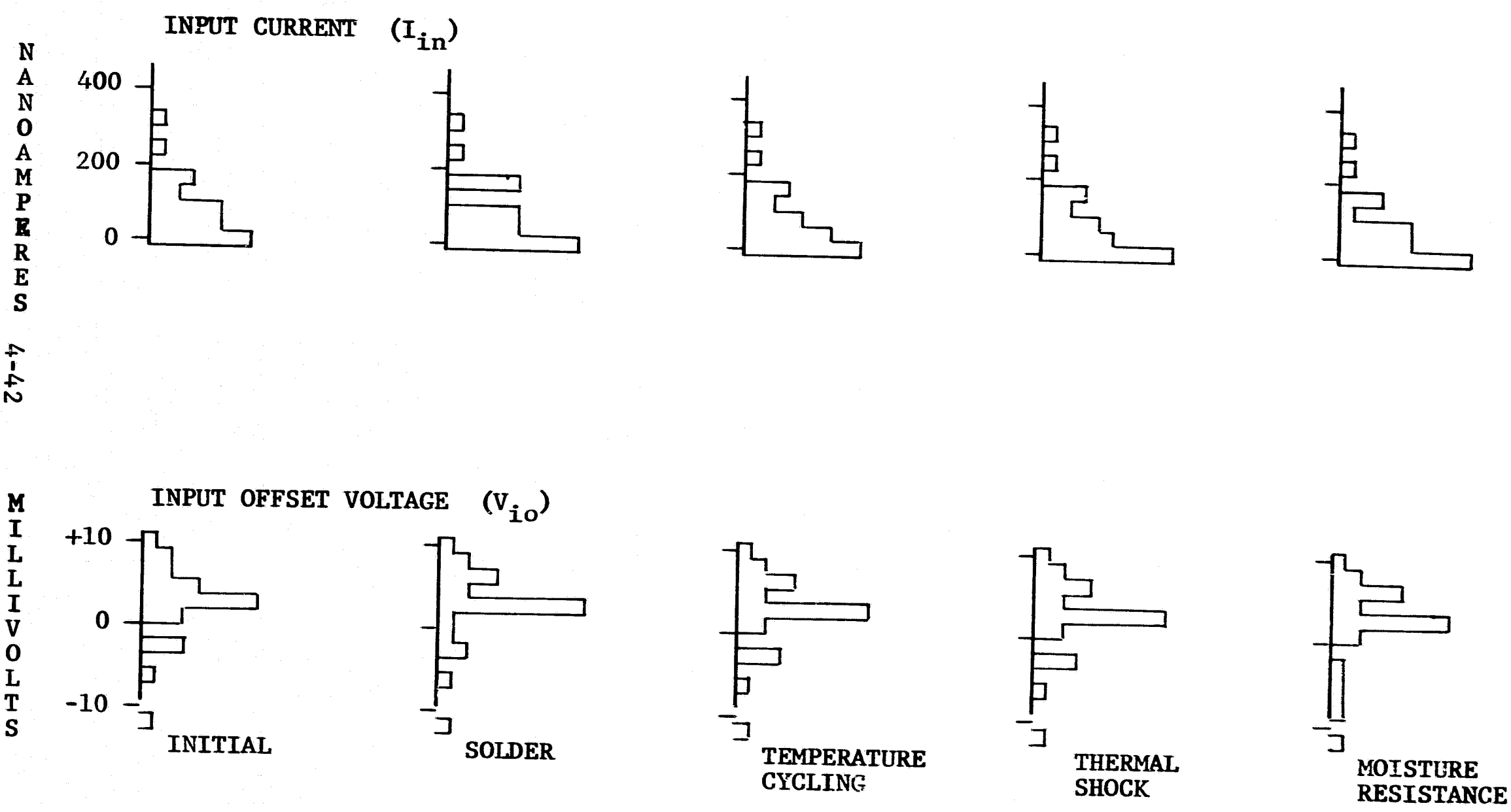


Figure 4-33

POWER STEP STRESS TEST
SN526
TA = 25°C
Sample Size = 15

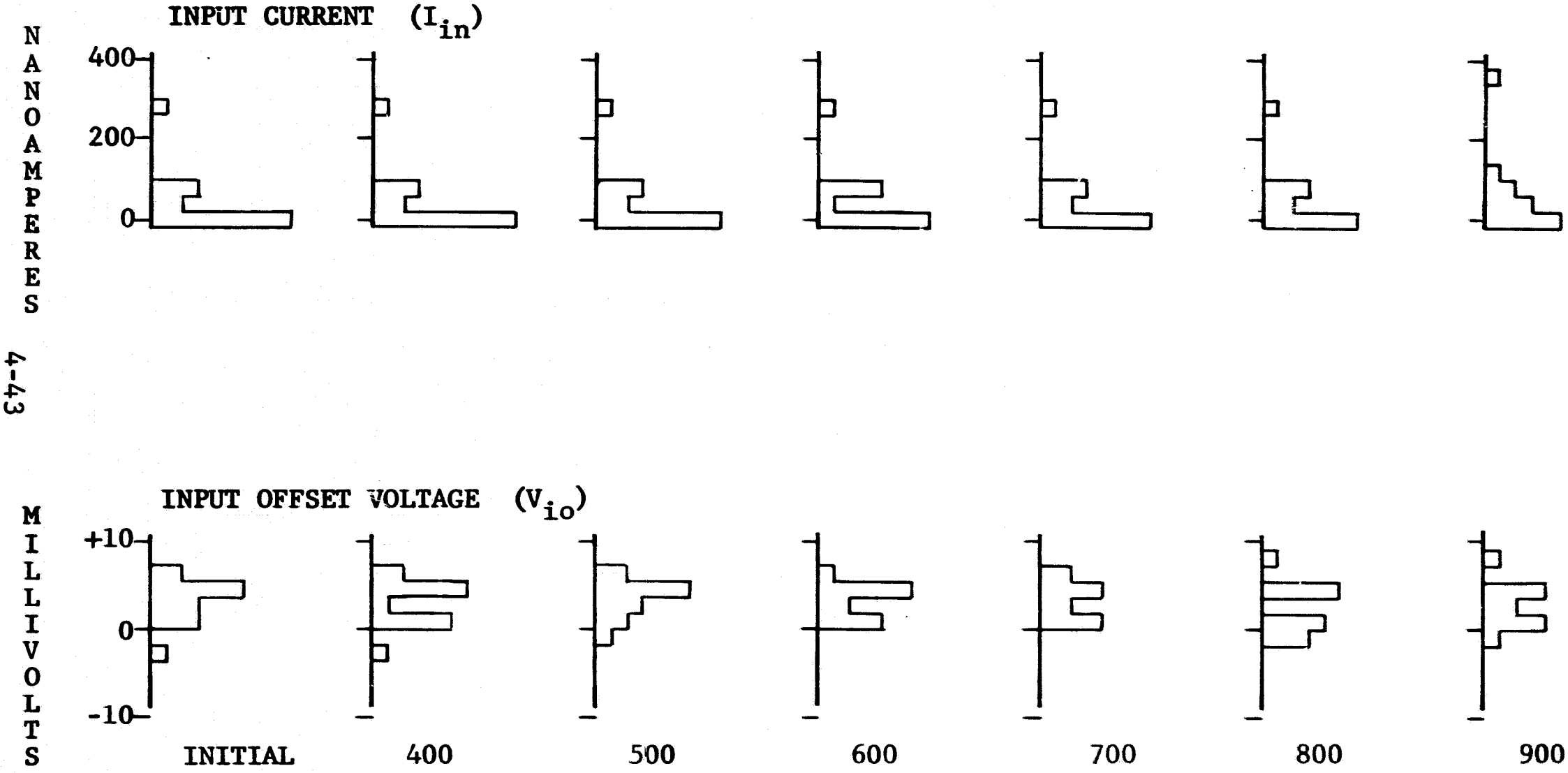
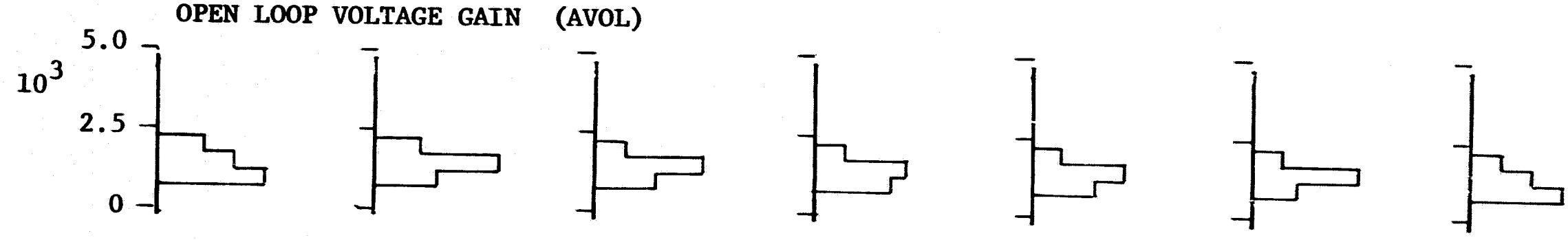


Figure 4-34

POWER STEP STRESS TEST
SN526
TA = 25°C
Sample Size = 15



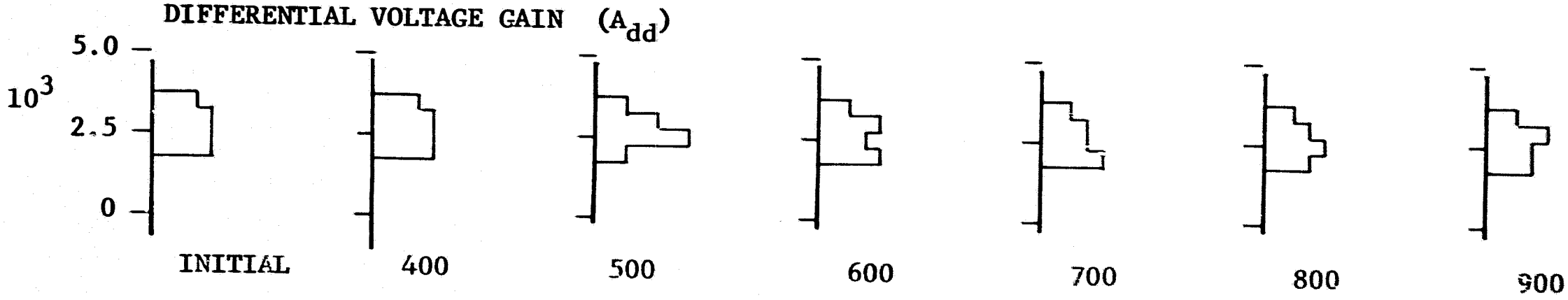


Figure 4-35

POWER STEP STRESS TEST
SN526
TA = 125°C
Sample Size = 15

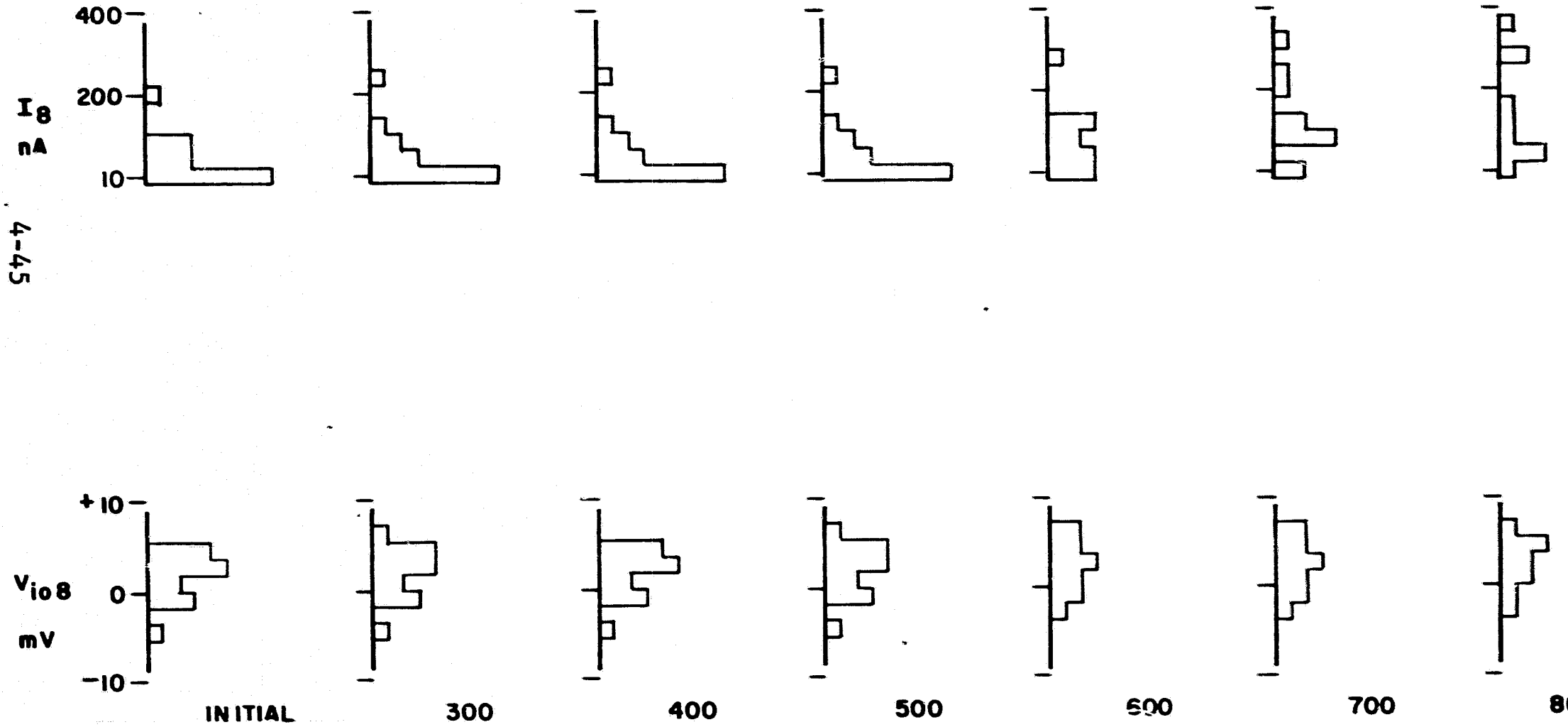


Figure 4-36

POWER STEP STRESS TEST
SN526
TA = 125°C
Sample Size = 15

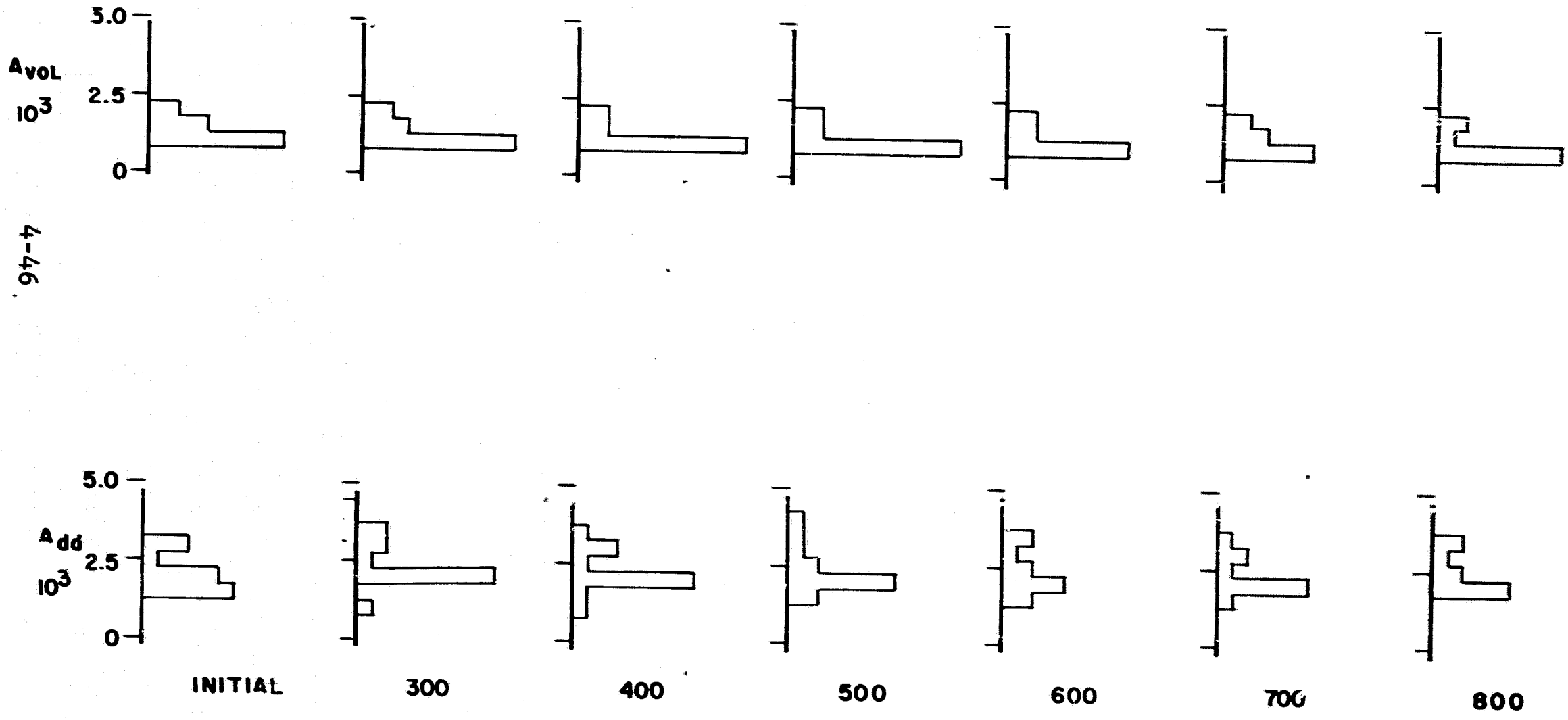


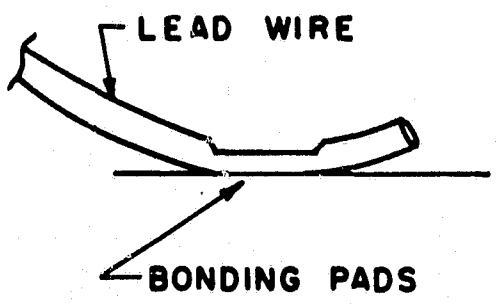
Figure 4-37

4.3 MC-1519 PROGRAM RESULTS

The MC-1519G differential amplifier is a hybrid circuit of excellent promise. However, in this program, certain weaknesses in processing were detected that make it mandatory that a tight visual inspection be implemented prior to accepting these parts for applications requiring high reliability features in its parts. The summary of test results is shown in Table 4-III. This device produced the largest variation in the number of failure modes detected. Yet no failures occurred during operation at 25°C. Of the three failures detected at 125°C and at a power dissipation level of 100 mW, one (at 125 hours) had a chopped (overbonded) lead bond which was the mechanism that led directly to the wire lifting from one of the interconnection islands. A second device (at 2000 hours) failed catastrophically and had a chopped bond as well as an excessive gold-aluminum reaction on the island region. The failure at 3000 hours was due to surface inversion or channelling.

Other failure modes were detected in other sequences. A list of the failure modes and where they occurred would be as follows:

(1) Chopped Bonds are defined as the overstressing of the bond by either applying too much pressure to the bond, thereby reducing the lateral thickness of the wire at the bond area, or by bonding with the wedge at an angle to the plane of the bond area resulting in the same reduction in lead strength. Diagrams of each are:



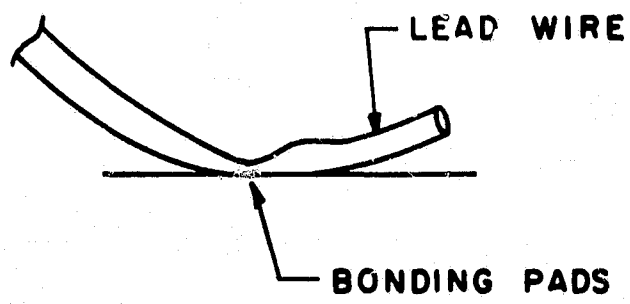


TABLE 4-III

PROGRAM SUMMARY REPORT - MC-1519

Test Description	Test Duration	Accumulated Hours of Testing	Initial Sample Size	Number of Failures
<u>Operating Life Tests</u> T_A = 25°C P_d = 100 mW	3000	42,375	15	0
T_A = 125°C P_d = 100 mW	3000	70,062	25	1 (1) 2 (2)
T_A = 125°C P_d = 300 mW	3000	69,562	25	2 (2)
Storage Life Test T_A = 150°C	3000	43,000	15	2 (1)
<u>Mechanical Test Sequence</u> Impact Shock 1500g ½ ms Vibrative Fatigue 20 g Vibration Variable Freq. Constant Acceleration 20,000 g	X	X	25	1 (3)
<u>Thermal Test Sequence</u> Solderability Temperature Cycling (-65° to +175°C) Thermal Shock Moisture Resistance	X	X	25	0

NOTES:

1. Open wire bond at interdie bonding island due to chopped, (overbonded) bond and accelerated aluminum gold intermetallic compound formation.
2. Inversion channel formation.

TABLE 4-III (Cont'd)

PROGRAM SUMMARY REPORT - MC-1519

Temperature Step Stress Test t = 48 hours/step		Power Step Stress Test T_A = 25°C t=48 hours/step		Power Step Stress Test T_A = 125°C t=48 hours/step		Temperature Cycling Step Stress (-55°C to T_h)	
Sample Size = 15		Sample Size=15		Sample Size=15		Sample Size = 15	
Test Cell (T = °C)	Number of Failures	Test Cell (mW)	Number of Failures	Test Cell (mW)	Number of Failures	Test Cell (T_h = °C)	Number of Failures
150	0	100	0	100	0	150	0
175	0	200	0	200	0	175	0
200	0	300	0	300	0	200	0
225	0	300	0	300	0	225	0
250	0	400	0	400	0	250	0
275	3 (4)	500	0	500	1 (2)	275	2 (4)
300	6 (4)	600	0	600	0	300	8 (4)
325	3 (4)	700	0	700	2 (2)	325	3 (4)
		800	0		1 (5)		
		900	3 (5)				
		1000					

NOTES (cont.):

3. Cracked ceramic substrate.
4. Gold-aluminum intermetallic compound formation at the die and at the interdie bonding islands.
5. Overstressed metallization.

A good bond would have no weak areas in it. This phenomenon was detected in the 100 mW, 125°C operating life test, and in the shock step stress test which is described in a section entitled, Additional Tests.

(2) Channelling is a phenomenon related to the inversion of surface regions of semiconductor devices by the application of a strong voltage field at a p-n junction region that may line up mobile ions at the surface, in the oxide, on the oxide, or in some other region. When sufficient ions of positive charge appear over a p region, the semiconductor region immediately below the surface at these points may become inverted (i.e., overdoped with electrons) changing the polarity at that point from positive to negative. The resulting leakage current will then provide additional current paths around the p-n junction. This phenomenon requires both voltage potential and thermal energy. Conversely, this phenomenon can be reversed by applying only thermal energy to the device thereby permitting the charge buildup to disperse. Since this phenomenon requires both the application of heat and voltage, it is not surprising that evidence of it was found only in the power-temperature sequence. One such failure at 3000 hours was detected in the 100 mW-125°C life test; two such failures were found in the 300 mW-125°C life test; one was found in the power step stress test at 25°C and two at the power step stress test at 125°C.

(3) Aluminum-Gold Intermetallic Compounds: The formulation of these compounds has been adequately documented. Their presence was observed in every test in this program that had the ambient temperature controlled at 125°C or higher.

(4) Broken Ceramic: The MC-1519 uses a ceramic disc to provide electrical isolation between the integrated circuit die and the dual-PNP transistor chip. After a mechanical impact shock test

this ceramic disc was found to be broken for one sample (see Figure 4-38). However, this problem occurred only once and did not show up in the higher stress levels of the centrifuge test or of the special impact shock test (10,000 G force) performed at the completion of the test program. It is assumed to be a random isolated event easily screened.

The degradation characteristics of the MC-1519G were generally acceptable. The plot of the two major variables in Figure 4-39 shows that some variation did occur that may be attributed to the device characteristics but that all shifting occurred well within specification limits and that the average value of the input circuit parameter improved as a function of testing.

4.4 MC-1525 PROGRAM RESULTS

The problems associated with the MC-1525 were the result of a peculiarity in the construction of the MC-1525 that permitted a catastrophic four-layer diode action to occur as a result of bias at temperature, the base current bias applied to terminals 3 and 9, plus the use of the lowest resistive combination in current source emitter leg. While this results in an abnormally high number of failures in those cells combining an ambient temperature at 125°C with bias, no failures of this nature were generated when current limiting resistors were added to the bias circuits. No failures occurred because of parameter degradation. In fact, the MC-1525 stability features were better than that of all other test devices, except the MC-1530.

A general summary of the results (Table 4-IV) of this circuit's performance would show that:

(1) No failures or degradation occurred at the room temperature test condition.

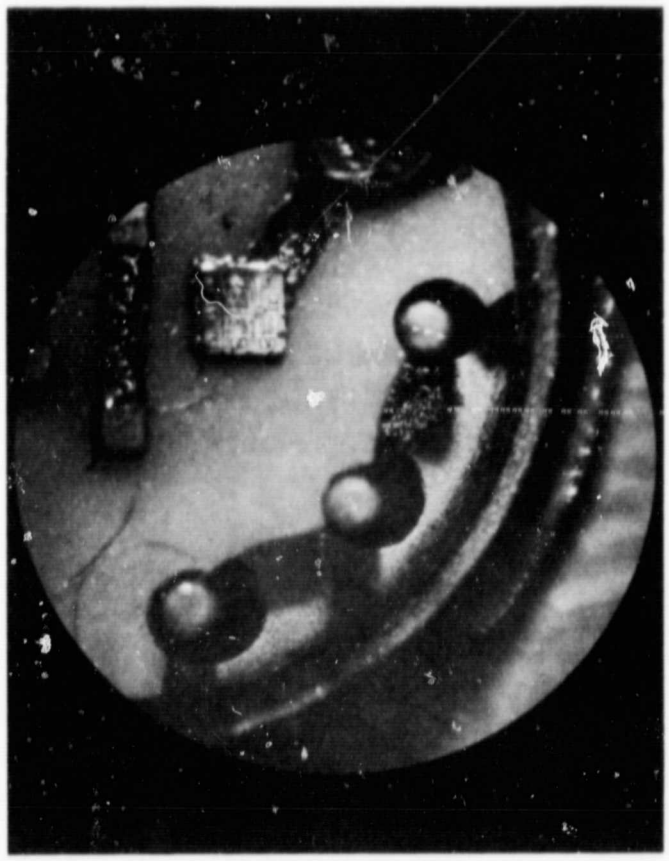


Figure 4-38. Unit No. 37--Ceramic Disc Broken as a Result of Mechanical Shock Test at 1500 G Shock Level ½ ms

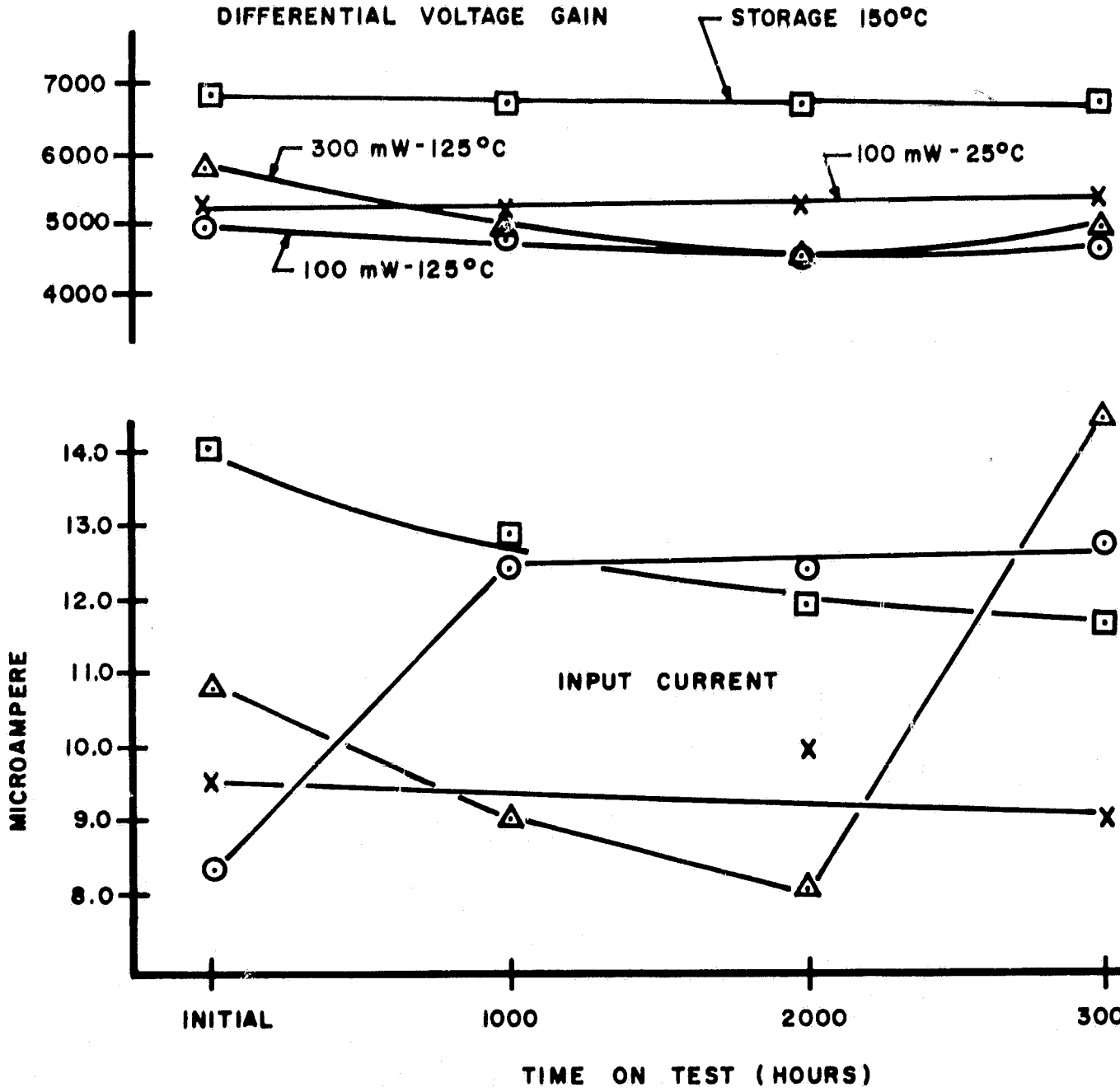


Figure 4-39. Plot of MC-1519 Parameter vs Time on Test

TABLE 4-IV

PROGRAM SUMMARY REPORT - MC-1525

Test Description	Test Duration	Accumulated Hours of Testing	Initial Sample Size	Number of Failures
<u>Operating Life Tests</u> T_A = 25°C P_d = 100 mW	3000	45,000	15	0
T_A = 125°C P_d = 100 mW	2000	66,187	25	3 (1)
T_A = 150°C P_d = 100 mW	2000	38,812	25	9 (1) 4 (2)
Storage Life Test T_A = 150°C	3000	45,000	15	0
<u>Mechanical Test Sequence</u> Impact Shock 1500 g ½ ms Vibrative Fatigue 20 g Vibration Variable Freq. Constant Acceleration 20,000 g	X	X	25	0
<u>Thermal Test Sequence</u> Solderability Temperature Cycling (-65° to +175°C) Thermal Shock Moisture Resistance	X	X	25	0

NOTES:

1. Open metal at V_{CC} - isolation region ohmic contact used by NPNP action to substrate. Physical capabilities of device exceeded.
2. Open wire bond at die due to aluminum-gold intermetallic compound formation.

TABLE 4-IV (Cont'd.)
PROGRAM SUMMARY REPORT - MC-1525

Temperature Step Stress Test t = 48 hours/step		Power-Temperature Step Stress Test T_A = 25°C t = 48 hours/step		Temperature Cycling Step Stress (-55°C to T_h)	
Sample Size = 15		Sample Size = 30		Sample Size = 15	
Test Cell (T = °C)	Number of Failures	Test Cell (T = °C)	Number of Failures	Test Cell (T_h = °C)	Number of Failures
150	0	125	1 (1)	150	0
175	0	150	0	175	0
200	0	175	0	200	0
225	0	200	0	225	0
250	1 (2)	200	3 (2)	250	0
275	2 (2)	225		275	0
300	4 (2)			300	1 (2)
325	3 (2)				

(2) No failures, other than the NPNP action, occurred under the 100-milliwatt operational life test performed at 125°C.

(3) Three failures, other than that noted in point 2, did occur as a result of intermetallic chemical reaction of gold and aluminum in the 100-milliwatt, 150°C test - at which condition the average junction temperature was approximately 175°C, beyond the Motorola ratings of such a device.

(4) No failures of any kind were detected from storage at 150°C ambient temperature.

(5) Above and beyond the two problems noted up to now, no additional problems occurred on any of the other tests.

4.5 SPECIAL INFRARED STUDIES

To support the other tasks of Saturn Linear Integrated Circuit Reliability Test Program, Motorola initiated a short study to determine the value of infrared radiometrics as a tool for the reliability evaluation of linear integrated circuits.

The primary area of interest in this study was the investigation of temperature gradients along the surface of the integrated circuit die while the device was operating under the electrical stress conditions used in the Saturn reliability test program.

A Barnes Engineering Model RM2B infrared radiometric microscope was procured from Barnes Engineering Company. An

infrared calibration source, Model RM121, specimen heater Model RM123 and Control Unit Model 23 TC121 were also procured. This equipment was procured on rental basis from Barnes Engineering at Motorola's expense. The RM2-B infrared radiometric microscope is equipped with a germanium immersed uncooled thermistor detector. The sensitive flake is 0.05 mm square. The optical gain of the immersion lens is 20. The optical pass hand of the system extends from 1.8 to 22 microns. The microscope was delivered with a 36X objective lens which gave infrared spot size of approximately 0.0014 inch and 360X visual magnification. The integrated circuit chosen for the test vehicle in this study was the MC-1530F.

4.5.1 Test Procedure

Five MC-1530F operational amplifiers we_e subjected to initial electrical parameter measurements. The units were then decapped, cleaned and examined microscopically. The emissivity of the die surfaces of these samples was determined by heating the sample to a known temperature (125°C) using the RM123 specimen heater, and then adjusting the system gain to achieve a reading of the known temperature. The gain control adjust on the RM-2B electronics unit is calibrated in units of emissivity. The emissivity of 40 target areas of each die was determined in this fashion. Figure 4-40, shows the location of the target areas with respect to the MC-1530 die. After the emissivity of the target points for each die was obtained, the devices were powered under the test conditions used in the Saturn Integrated Circuit Reliability Test Program. The surface temperature at each target was read, using the value of emissivity determined for that target, at levels of 100, 300, 500, 600, 700 and 800 milliwatts total dissipation.

During the powered phase of the experiment, a chimney was placed around the units under test to eliminate stray drafts.

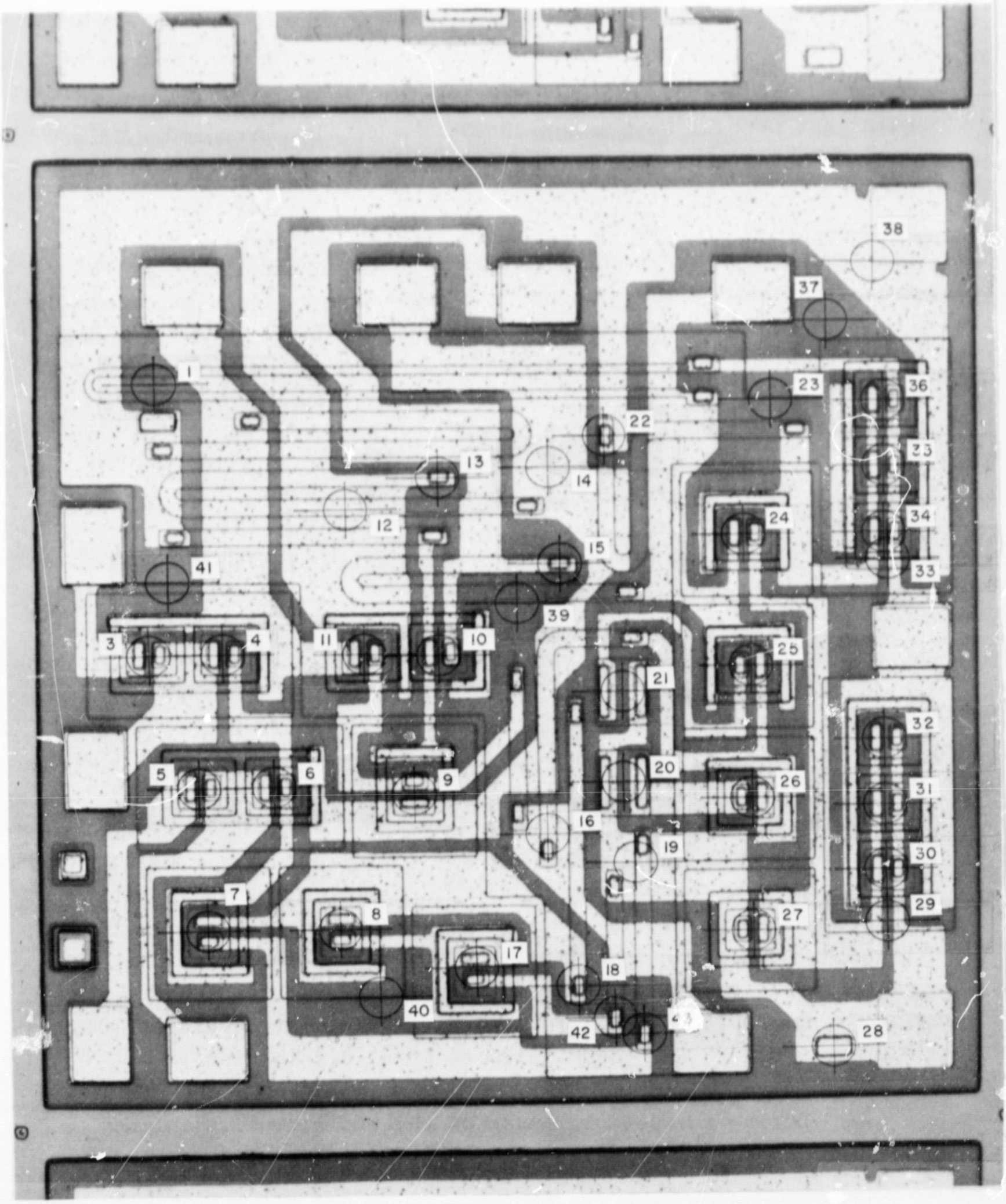


Figure 4-40. MC-1530F Target Areas--Emissivity Profile

4.5.2 Results of Study

The range of emissivities observed ranged from less than 0.20 to 0.85, the lower values being observed in predominately aluminum target areas. Considering the differences in emissivities obtained for each target area on all devices, it was found the maximum range in values of emissivity for a specific target was 0.18; the minimum was 0.03 and the average range of values from device to device was 0.07. The greatest variation occurred at predominately SiO_2 target areas indicating that some of the variation is due to positioning errors with respect to the surrounding low emissivity metallization. It was also noted that the inclusion of any foreign material, such as pyroceram particles greatly affected the value of emissivity. The variation of the emissivity of the transistor areas was on the order of 0.07 to 0.08 out of 0.45 average. This variation in emissivity would introduce errors in temperature readings which preclude the use of an average value of emissivity for each target area to be used in temperature measurements on many devices. The temperature readings made on devices tested indicated the mean temperature variations across the die shown in Table 4-V.

TABLE 4-V

OBSERVED TEMPERATURE GRADIENT WITH RESPECT TO DISSIPATION LEVEL

MC-1530F

Dissipation (mW)	Mean Die Temperature Differential (°C)	Mean Temperature at Center of Die (Sta. 39) (°C)
100	4	55
300	4	65
500	9	93
600	13	111
700	18	122
800	23	155.5

At dissipation levels above 300 mW the maximum temperature was observed at the common collector output transistor, (stations 34, 35, and 36) and/or in the silicon isolation junction region at station 37 (see Figure 4-40). The minimum temperatures were observed in the regions of the input transistors. The observed temperature indicated that the major portion of the dissipation at the higher power levels was concentrated in the common collector output transistor, corroborating the result of the circuit analysis.

The accuracy of the temperature indications depend, neglecting fixed system errors, on the determination of the emissivity of the target area setting that value of emissivity on the gain control (emissivity adjust) and the errors in focusing on the target point. The major source of error was in determining the emissivity setting to be used. The calibrated dial is graduated in units of tenths from 0.2 to 1.0; no interpolation scales were available. At best then, the probable error in reading and setting the emissivity control was ± 0.01 and may have been as great as ± 0.02 considering errors in returning to the same target area.

The emissivity of the transistor areas ranged from 0.40 to 0.55. This means that the error in the temperature readings for these areas could be in error by a factor on the order of ± 5 percent which means, for example, that the mean temperature difference on the surface of the die shown in Table 4-V for 800-mW level could have been as little as 8.4°C which is less than the expected variations in average die temperature at this power level due to variations in junction-to-air-thermal impedance caused by minor variations in die bonds and air flow around the package.

4.5.3 Conclusions

Based on this study one must conclude that from the standpoint of determining electrically induced thermal stress

concentrations in integrated circuits the usefulness of infrared radiometrics as a direct measurement tool is limited by the following factors:

(1) The emissivity of each target area must be determined precisely. This is at best a laborious process in a circuit of modest complexity.

(2) The sensitivity and resolution of the equipment must be such that small differences in temperature in adjacent areas can be detected. Since in general these areas will have different values of emissivity, the ability to determine the emissivity precisely is of paramount importance and in practice may be the limiting factor in determining equipment resolution.

As shown by this study, neglecting errors, the maximum temperature differential across the MC-1530 die was 4° at power levels of 100 mW and 300 mW, even though under the 300-mW test conditions the power density in the output section of the device was approximately five times greater than the power density in the input section.

(3) Procedures must be developed to facilitate rapid scanning, without loss in precision or resolution, to reduce the time spent in taking data.

Until these basic problems are resolved, the use of infrared radiometric microscopy as an everyday reliability tool is severely limited.

4.6 SPECIAL STUDY--POWER STEP STRESS TEST WITH HIGH-LOW TEMPERATURE PARAMETER MEASUREMENTS

At a meeting which took place at the NASA Langley facility, shortly after the contract was awarded, Motorola was asked to perform a special series of tests to determine whether or not potential life test failures would be more quickly detected by measuring high (T_A = 125°C) and low (T_A = -55°C) temperature parameters as well as those agreed upon at room temperature. It was decided that the answer to that question could best be determined by subjecting survivors of the mechanical stress sequence to a repeat of the power bias step stress tests except that the A_{VOL}, A_{dd}, I_{in}, and V_{io} parameters were tested at the temperature extremes. To this extent, six of the SN-526 and ten of the MC-1530F circuits were used. The test stressing technique was identical to that used in the power Bias Step Stress test except that the SN-526 test was cancelled after the 300-mW step and the MC-1530F was cancelled after the 500-mW step. The data does indicate that some circuits may fail faster if the high temperature measurements criteria are specified. Graphical presentations of this data are found in Figures 4-41 and 4-42.

4.7 SPECIAL STUDY--ACCELERATED MECHANICAL STEP STRESS TESTING

Two special series of step stress tests were performed as a part of this test program to explore the physical limitations of these circuits and package combinations. A description of these test sequences and their results is as follows:

4.7.1 Impact Shock Step Stress Test

Ten samples of each type were subjected to 10 impact shocks of 3000 G and 10,000 G (0.2-millisecond duration) each of the X_1, Y_1, and Z_1 stress axes. Parameter readings were made after the 3000-G and 10,000-G steps. The SN-526, MC-1530F and MC-1525G survived all stresses with no observed failures. Four MC-1519G's failed the

10,000-G step and subsequent failure analysis found this to be attributed to chopped bonds breaking after repeated stresses of these levels.

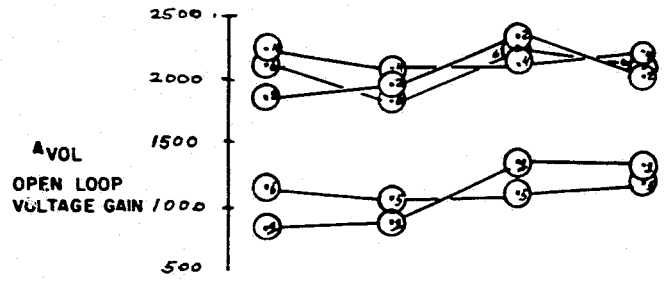
4.7.2 Vibration Variable Frequency Step Stress Test

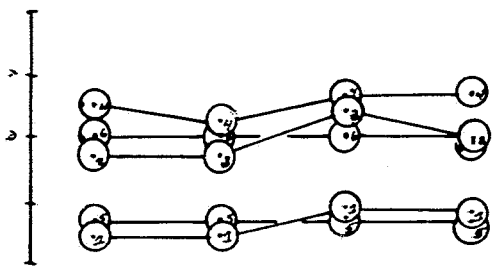
Ten samples of each part were subjected to a vibration variable frequency step stress test, performed according to the method outlined in MIL-STD-750, method 10 except that the applied force was varied at each step from 30, 50, 70, 80, 90, and 100 G. The TO-5 circuits had package failure occurring at the 50-G step for the MC-1519G and at the 70-G step for the MC-1525G. This failure mechanism had been observed in other TO-5 packages tested in this manner and was explained as a function of a critical force frequency relationship that created a destructive resonant force in at least one lead in four of the MC-1519G's and five of the MC-1525G's.

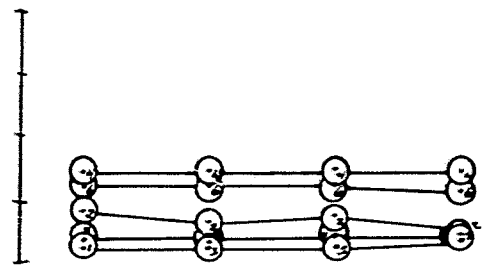
No other failure mechanisms were detected as related to the TO-5 internal system or for the flat package as a unit. This failure mechanism was attributed to the package and has not been seen at the lower stress levels normally required to evaluate integrated circuit products.

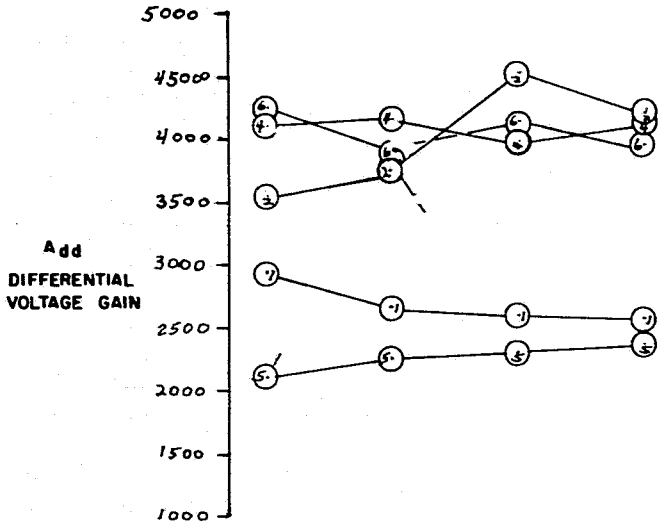
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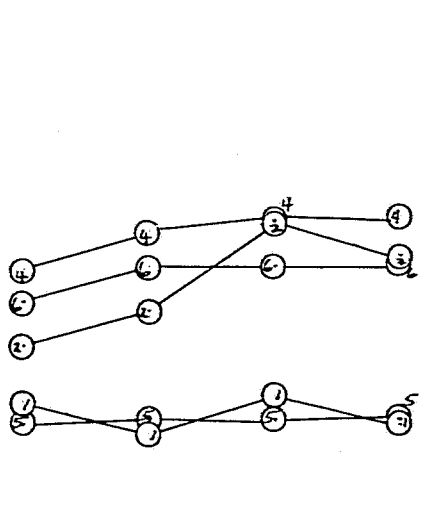
SN-526

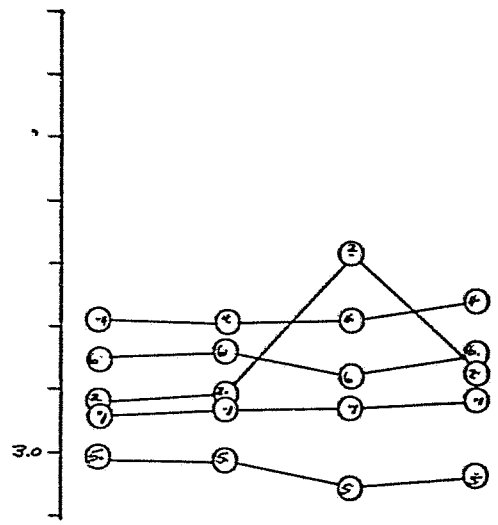

A_{VOL}
OPEN LOOP
VOLTAGE GAIN
2500
2000
1500
1000
500

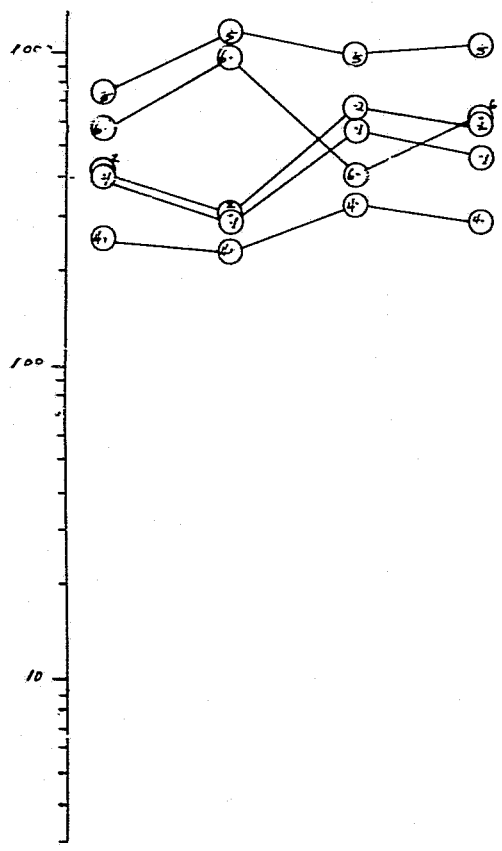


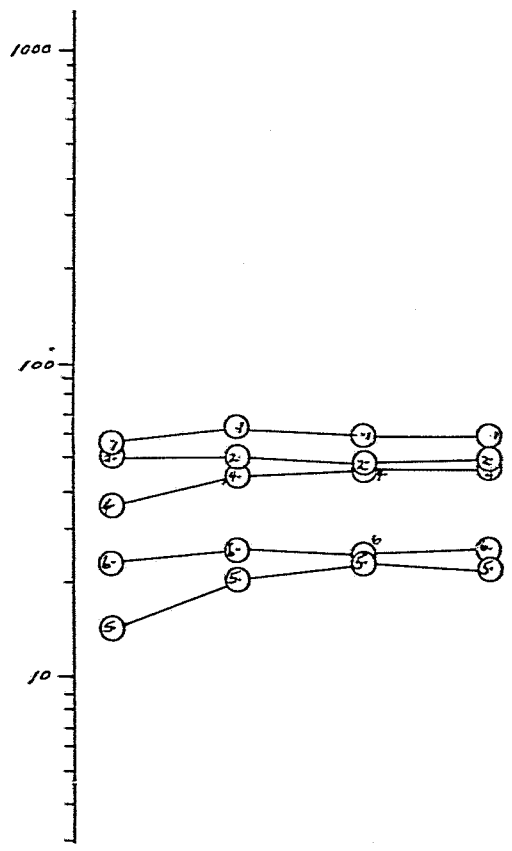


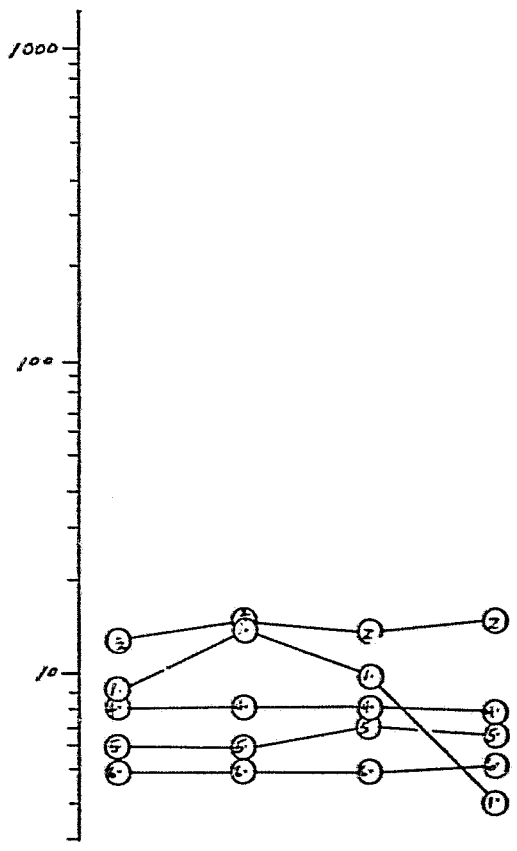

A_{dd}
DIFFERENTIAL
VOLTAGE GAIN
5000
4500
4000
3500
3000
2500
2000
1500
1000




3.0


I_B
mA
100
10


1000
100
10


1000
100
10

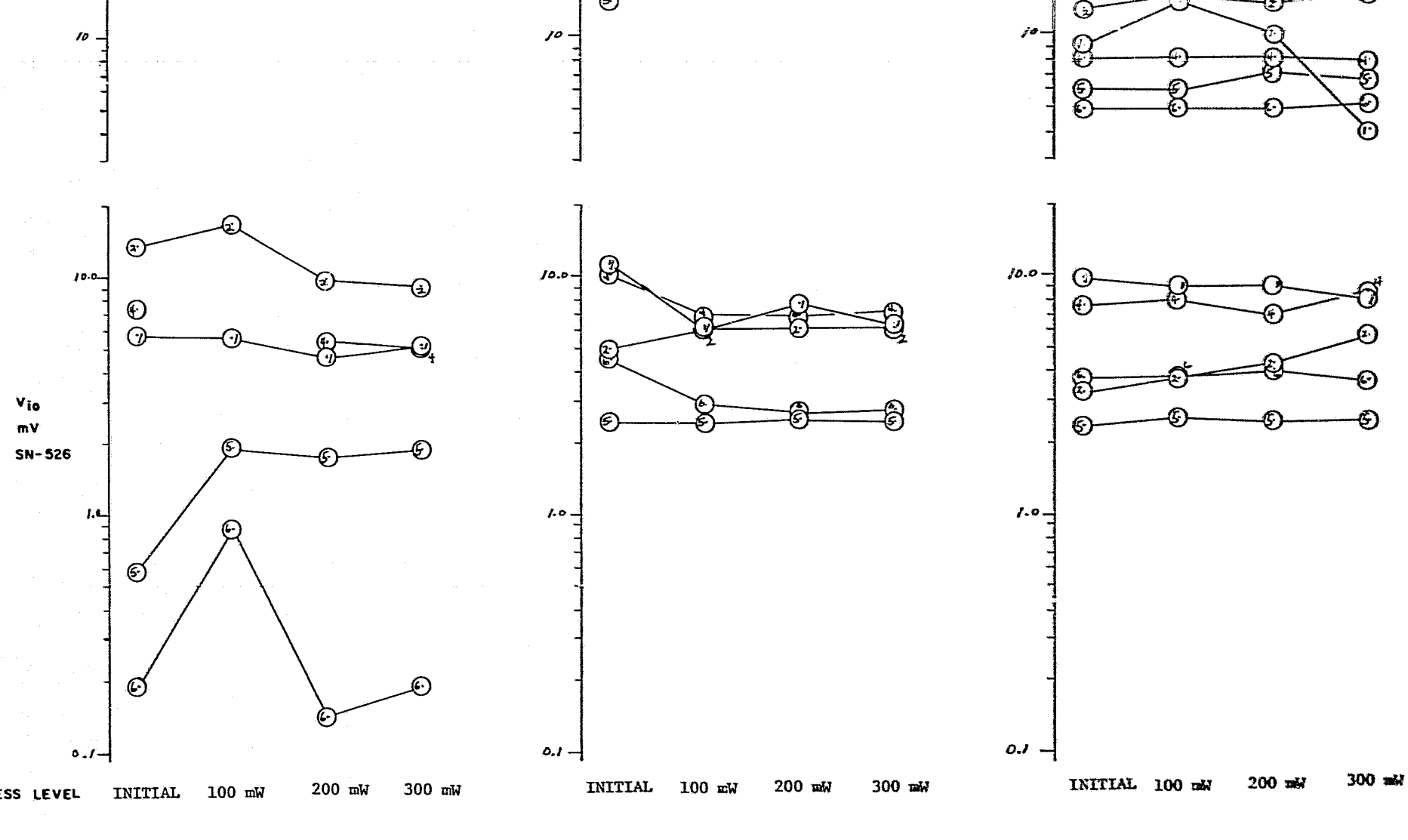
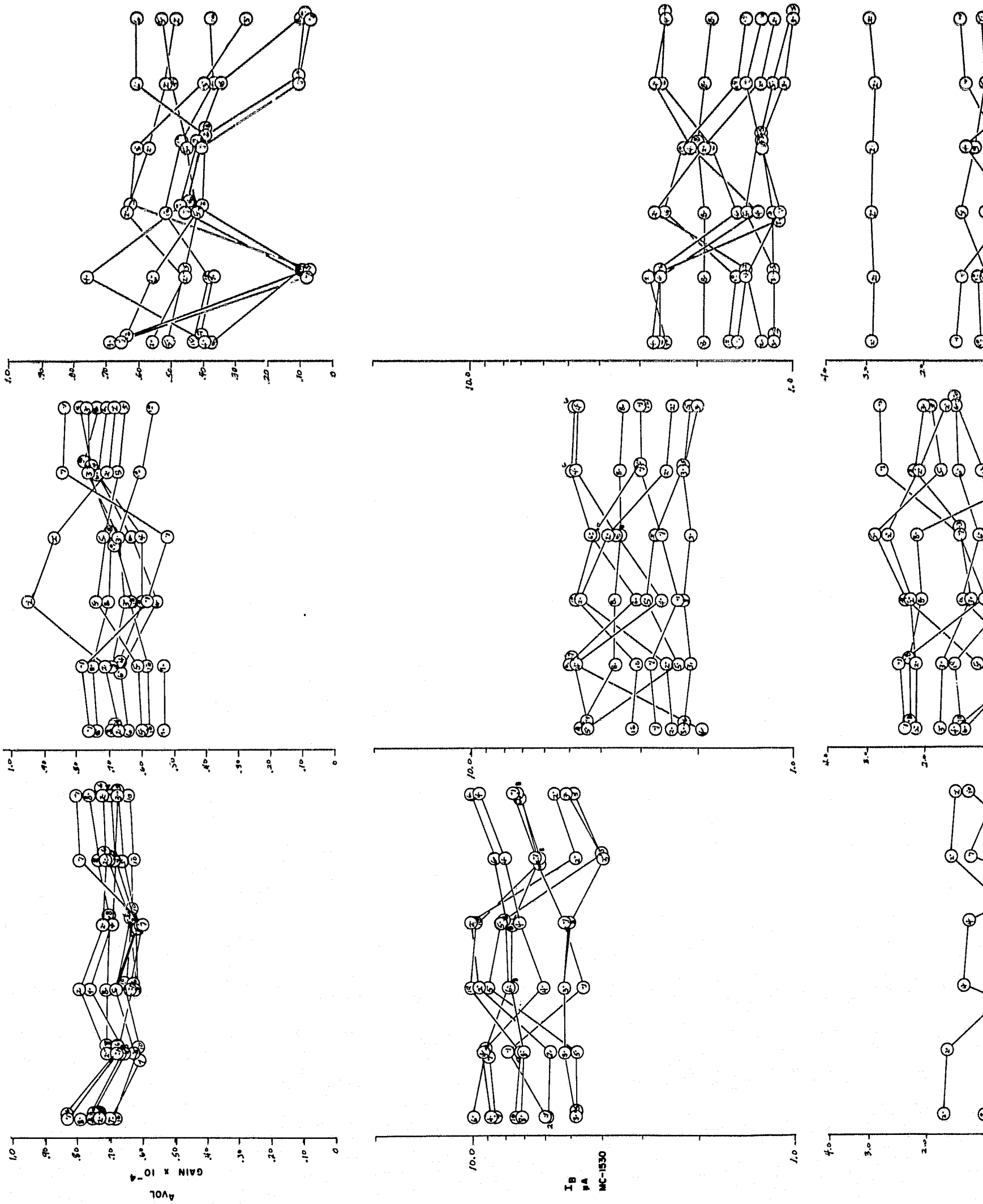


Figure 4-41. Plot of Special Power Temperature Step Stress Test Results for SN-526

6676-10-7



4-65 A

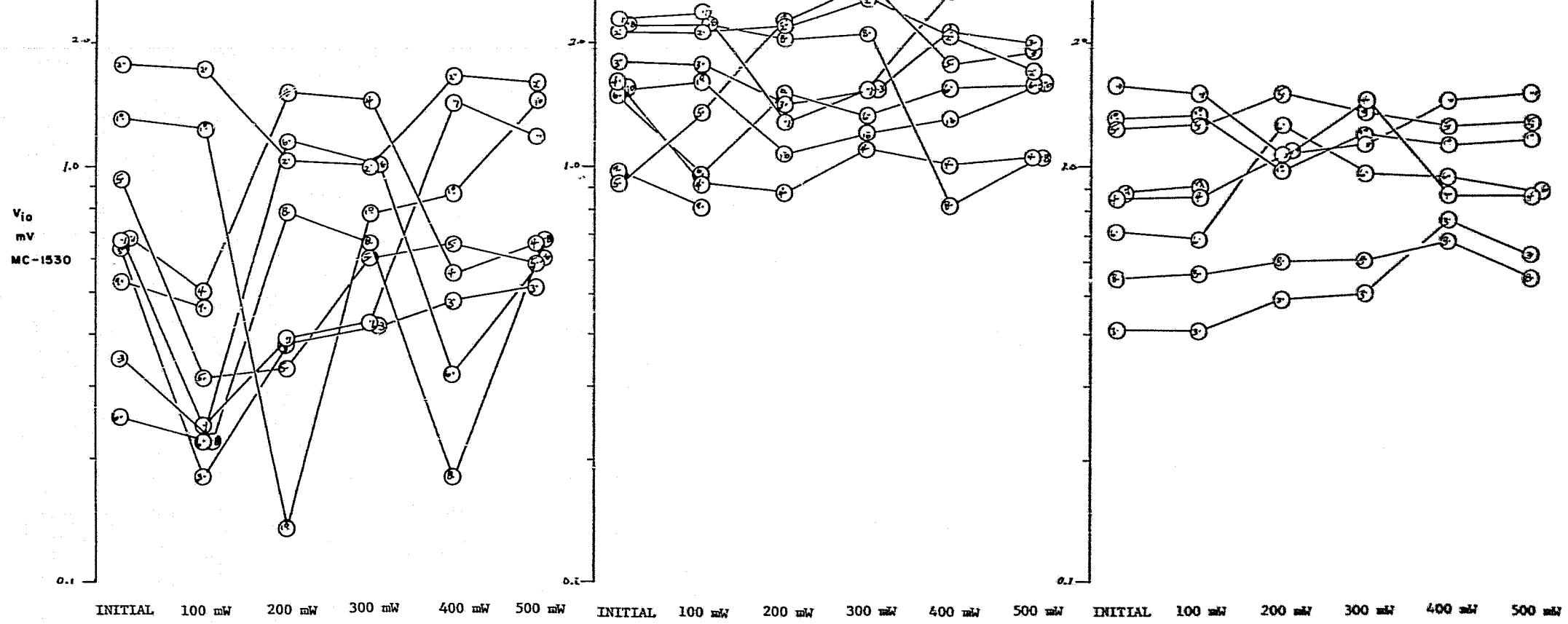


Figure 4-42. Plot of Special Power Temperature Step Stress Test Results for MC-1530F

6677-10-7

SECTION V

5.0 SUMMARY OF LITERATURE SURVEY

To support the design phase of the test program, a survey of existing reliability physics literature, including available semiconductor test reports was conducted. The purpose of this survey was to determine what failure modes and mechanisms have been significant in determining the failure rate of monolithic integrated circuits, and the environmental and electrical stress tests used to accelerate these mechanisms.

Two hundred and seventeen documents or articles were reviewed. These are listed in Appendix B. These documents were selected from reports of special studies and tests, articles in professional journals, and presentations made at the various symposia conducted in the reliability engineering field.

In studying the source materials, it was noted that wide differences in interpretation and usage of the terms "failure mode" and "failure mechanism" exist in the field of semiconductor technology. To avoid ambiguity and misunderstanding, the term "failure mechanism" as used in this report shall be defined as: The fundamental physical mechanisms that are responsible for the change causing the observed failure. These mechanisms are considered to be independent causes of failure.

The relative rates of incidence of the various failure mechanisms could not be established from a review of the literature because quantitative data were furnished in only a few reports. However, the results of the Autonetics studies and two other recent studies (references 105 and 135) have indicated that the prevalent causes of failure are imperfections of bonds, intraconnecting

metallization, and passivation and surface instabilities resulting from surface contamination, including inversion channelling.

The dominant failure mechanisms are categorized with respect to the region or area of the complete integrated circuit affected. These are bonds, interconnects, passivation, surface contamination, bulk defects, and other miscellaneous failure mechanisms.

5.1 FAILURE MECHANISMS ASSOCIATED WITH WIRE BONDS

Most wire bond failures are a result of either improper bonds (over- or underbonding) or reactions occurring between dissimilar metals at the bond.

Failures have also been attributed to such causes as improper bond location in relation to the bonding pad on the die or the post, improper routine or tensioning of the internal lead wires and broken lead wires.

These mechanisms will be discussed under the categories of intermetallic compound formation, improper bonding, and improper lead dress.

5.1.1 Intermetallic Compound Formation

Open and intermittent bonds were experienced in devices having gold-aluminum metallization when stored at 200° and 300°C. Initially, the failure mechanism was identified as gold diffusing into aluminum to form $AuAl_2$ (purple plague). Subsequently, the failure mechanism was identified as a ternary compound of Au-Al-Si (black death). More recently, the failure mechanism has been identified to be due to the formation of gold-rich Au-Al compounds in

the order AuAl, Au_2Al, Au_5Al_2, Au_4Al and gold (solid solution of aluminum in gold). Although not all authorities agree as to the specific failure mechanism involved, it has been established that gold diffuses into aluminum, that silicon present near the Au-Al interface apparently acts as a catalyst in the diffusion, and that it proceeds more rapidly at higher temperatures. The effects of this failure mechanism can be reduced by utilizing all-aluminum metallization or by using aluminum leads within the package to form the Au-Al bond on the TO-5 post or on the flat-package bonding pad. Most authorities agree that failure caused by Au-Al intermetallic compound formation are a function of the ratio of gold to aluminum at the bond as well as the area of the bond. Thus bond failures at temperatures in the 150° to 300°C range may occur in chopped bonds due to depletion of gold at the neck or heel of the bond. Underbonding will aggravate this mechanism due to reduced bond area and higher unit stress at the bond.

5.1.2 Improper Bonding

Open, intermittent, and high-resistance circuits may result from the application of excess pressure by the bonding tool on the lead in the wire bonding process, either severing the lead completely or crimping it sufficiently to reduce materially its effective cross-sectional area for current transfer. The short circuits can result from the application of excess temperature which splatters lead material on the surface of the die. As noted above, the reduction of the available gold as a result of overbonding gold wire to aluminum films renders the bond very sensitive to intermetallic compound formation.

Electrically open and intermittent bonds have been attributed to underbonding resulting from insufficient pressure and/or temperature at the time of bonding, which gives a decreased

bond area, through insufficient deformation of lead material or inclusion of large crystallites or particles of metallic oxides in the recrystallized or eutectic region of the bond.

Some intermittent open and short circuits were found to have been caused by bonds formed too close to the edge of the intraconnect or the die. In the former case, the failure mechanism was usually identified as one of the failure mechanisms of improper passivation; e.g., pinholes or scratches in the oxide. In the latter case, the bond was found to have shorted to the substrate material either directly or by a shunt across the oxide surface. This type of failure is rare. Generally this failure mechanism is effectively screened by production electrical parameter measurements.

5.1.3 Improper Lead Dress

Failures have also been attributed to improper lead routing, sagging leads due to excessive length, and broken leads due to excessive tension. Failures of this type may be classified as due to improper lead dress, and in general is a function of the wire bonding operation.

5.2 FAILURE MECHANISMS ASSOCIATED WITH INTRACONNECTING METALLIZATION

Failures of metallization which forms the intraconnecting network of the integrated circuit result from either a decrease in cross-sectional area of the conductor, which raises the resistance of the conductive path and/or causes localized overstress in the metal which causes the metal to fuse, or unwanted surface metal bridges which cause shorts between adjacent metal runs or circuit elements. These mechanisms may also include interactions with imperfect passivation though in general this class of defect is classified as due to improper passivation.

5.2.1 Improper or Damaged Metallization

Failure mechanisms which are associated with improper or damaged metallization include poor adhesion of the metal film, improper thickness of the metal, improper width of the metal, and cracks and scratches in the metal. The first three are normally caused by improper deposition and photoetching. Scratches are generally attributed to handling damage during subsequent assembly process steps. Other mechanisms in this category are decomposition, corrosion, and oxidation of the metal films though these are more often associated with thin film resistors. The deposited film may contain an abnormally high concentration of lattice defects which anneal out during the subsequent processing steps or under use conditions.

The effect of all of these failure mechanisms is to effectively reduce the effective cross-sectional area for current transfer. When the current density at any of these constrictions increases to a value sufficient to cause migration of the metal to occur, further decreasing of the cross-sectional area at that point, burn-out will result.

5 2.2 Metal Alloying and Diffusion

Circuit failures were experienced when the gold or aluminum metallization diffused into junction regions, isolation regions, or the substrate. Gold has been shown to migrate rapidly across silicon. Aluminum has been shown to migrate from the areas of metallization, particularly at the edges and at steps in the oxide, when devices were stored at 150° to 350°C for periods ranging from 2,500 to 11,000 hours. Aluminum has been shown to react with the oxide passivation to form an aluminum oxide and silicon at temperatures ranging from 250° to 560°C.

Aluminum may also diffuse along cracks or scratches in the oxide causing bridging or shorts between adjacent metal circuits.

These mechanisms generally result from excessive stress or are associated with poor passivation.

5.3 FAILURE MECHANISMS ASSOCIATED WITH SEMICONDUCTOR SURFACES

These failure mechanisms can be categorized into two basic groups, mechanical defects in the passivation and surface or passivation contamination.

5.3.1 Passivation Defects

The mechanisms attributed to passivation defects generally relate to improper formation of the passivation layers and, in general, are confined to those defects which can be detected usually. Such mechanisms include: pinholes in oxide, cracks in oxide, scratches in oxide, feathering of oxide, flaking of oxide, undercutting of oxide, and insufficient thickness of oxide, to include unpassivated areas. The partially passivated or unpassivated areas cause failure by providing a shunt for current flow or by permitting impurities and contaminants to diffuse into the surface of the die. The failure mechanisms of improper passivation are related to the other failure mechanisms which identify partially passivated or unpassivated areas, and include failure mechanisms associated with the interaction of the metallization.

5.3.2 Contamination of Surfaces and Passivation Layers

5.3.2.1 Inversion Channel Formation

Uncontrolled inversion channel formation is probably the dominant cause of failure in all silicon planar type products. The control of semiconductor surface states has been the subject of many research programs which have resulted in numerous articles in the literature. This phenomenon generally occurs as a result of temperature-bias testing. When the bias voltage applied across a p-n junction causes mobile impurity ions (on the surface of the passivation, within the passivation, or at the interface between the passivation and the surface) to move to create a concentration of charges over the semiconductor material adjacent to the junction. This charge concentration causes a concentration of carriers of opposite polarity in the surface of the silicon adjacent to the junction and when great enough, will invert p-type material to n-type material (or n-type material to p-type material). It has been shown that the inversion of only a few monolayers at the semiconductor surface is necessary to create a channel of electrical significance.

Susceptibility of a junction to channelling is proportional to the applied field, the resistivity of the surface layers of the n and p regions, and junction temperature. Formation of inversion channels is sharply accelerated at junction temperatures above 150°C.

Techniques which have been used to reduce the susceptibility of a device to the channelling mechanism include: modifying the passivation silicon to provide trapping centers for specific contaminating ionic species, controlling the surface potential with metal film electrodes, and confirming the formation of channels to a predetermined area by the use of low surface resistivity barriers ("guard rings").

Channelling is generally manifested by an increase in the leakage current of the affected junction and, in many instances of transistor failure, a decrease in current gain at low collector currents. The formation of inversion layer channels during combined temperature voltage stresses is a reversible reaction. Induced channels may be removed by storage at high temperatures (usually 200°C) for a short period of time.

5.3.2.2 Surface Contamination

Surface contamination as used herein refers to extraneous material left on the surface of the semiconductor material during the processing and assembly of the device. These contaminants include organics such as photoresist, metal particles adhering to the surface, and contaminants of a chemical nature which can cause corrosion or degradation of the metallization or passivation films. In general these are characterized by resistive shorts between circuit elements, across junctions, and between adjacent conductor paths. Open metallization can also occur as a result of corrosion or electrolytic action. These mechanisms have occurred during high temperature storage and operating life tests. They are irreversible.

5.4 BULK FAILURE MECHANISMS

Relatively few failures were found to have been caused by bulk defects. Devices made from wafers having bulk defects which are inherent in the wafer or are introduced during processing are normally rejected during production line electrical tests. Defects in this category may be associated with the epitaxial layer. Edge dislocations, isolated dislocations, twin boundaries, stacking faults and "stair-rod" dislocations associated with stacking faults were found to exist in the silicon wafer. There is little evidence

that these defects, in themselves, have a deleterious effect on the operation of semiconductor devices. However, it is established that such lattice imperfections yield nonuniform doping and provide nucleation centers for impurity precipitation. "Stair-rod" dislocations have been established as the most serious of these types of defects. The failure mechanism bulk defect, as used in this survey, categorizes many of those failures for which another failure mechanism cannot be found. As an example, if a transistor were to degrade under the temperature, voltage, and current conditions of its use and all other possible failure mechanisms (e.g., diffusion of metal into silicon, surface contamination, pinholes in oxide, etc.) were eliminated, bulk defects might have been the failure mechanism postulated as responsible for the failure. Included within this failure mechanism are failure modes caused by current concentration centers, unstable or improper resistors, and faulty capacitors, diodes, and transistors. The references also include failures reported as due to this mechanism for which failure analysis did not continue until a specific failure mechanism was identified. Failures which are in truth caused by bulk defects are generally detected during high temperature storage tests or, in the case of higher power integrated circuits, during high current switching tests.

5.5 PACKAGE FAILURE MECHANISMS

The categories of failure mechanisms listed under this heading are generally those which are attributed to a failure of the package or are attributable to the package fabrication processes including final sealing. Also included here are faulty die bonds which are a function of the mechanical assembly of the package.

5.5.1 Faulty Seals

Device failures were found to be caused by faulty seals which permitted contaminants, particularly moisture, to penetrate the package and react chemically with the device materials. The specific failure mechanisms listed under the general heading of faulty seal are: faulty cap-to-case seal, faulty preform-to-case seal, broken insulation around terminal, and faulty insulator-to-case seal. The faulty seals were found to be caused by poor wetting of the elements of the seal during assembly or breaking of insulation due to mechanical stresses created in the interface by differences in the thermal expansions of the elements of the seal. The failure of faulty seals can be accelerated by temperature cycling and can generally be detected by suitable leak rate testing.

5.5.2 Foreign Material Inside Package

The two predominant types of device failure experienced from foreign material inside the package were shorts caused by conducting material and mechanical damage caused by nonconducting materials during shock and vibration testing. This material is attributed to weld spatters or excessive pyroceram used during final seal of ceramic flat packages.

5.5.3 Voids in Die Bonds--Loose Die

Hot spots and thermal runaway were found frequently to be caused by voids under dice and loose dice because the heats generated in use were not dissipated through the die-to-header bond to the package. This failure mechanism results from poor wetting of the die and/or the header during assembly. Voids can sometimes be detected by radiographic depending on die bonding techniques. A sequence of thermal cycling followed by constant acceleration or mechanical shock has proven effective as a screen for this type of failure.

5.5.4 Misorientation of Die

Relatively few failures were found to have been caused by the misorientation of the die within the package, improper design layout, or improper marking of the pins of the device. In most cases, the devices having this failure mechanism are rejected during production line electrical tests or the failure has been classified as due to another failure mechanism such as misrouting of leads or improper lead tension.

5.5.5 Package Surface Contamination

External surface contamination was found to have caused electrically "good" dice to be classified as failures. Contamination on the package provided external leakage paths between terminals or between a terminal and the package. These contaminants may be present because of improper cleaning or handling or because of the use of improper materials.

5.6 MISCELLANEOUS FAILURE MECHANISMS

This category includes those mechanisms which cannot be logically classified under the previous categories. These mechanisms may or may not be related to a single process step. Improper masking, for example, is attributable to a specific process, while scratches on a die could occur at any step where the wafer or die is handled.

5.6.1 Improper Masking or Etching

Relatively few failures were found to have been caused by improper masking or etching. Devices made from wafers having imperfections due to these processing errors are normally rejected during

production line electrical tests. In most cases where these imperfections are not detected by production electrical tests, subsequent failure analysis usually defines a more specific failure mechanism such as undercutting of oxide, and improper thickness of oxide. These defects are, in general, contributory to such mechanisms as metallization problems and channelling.

5.6.2 Cracks or Scratches in Die

These mechanisms are generally attributed to handling damage, although in some cases improper die bonding techniques contribute to the problem. Cracks in silicon die are found to be caused primarily by overpressure applied during the die-to-header bonding operation or by mechanical stress induced in the dice by changing thermal conditions or shock and vibration in cases where the die was not thoroughly attached to the header throughout the interface. Scratches in dice were found to result during processing. Cracks or scratches occurring before passivation may result in failures from other failure mechanisms, such as metal diffusion into silicon and pinholes in oxide. Those occurring after passivation provide shunts for current flow or partially passivated or unpassivated paths by which impurities and contaminants within the package diffuse into the die, eventaully causing failure.

5.6.3 Etch Pits

Etch pits were found to cause failures when they provided areas contributing to improper passivation of the surface, and eventual diffusion into the die of the impurities and contaminants present within the package.

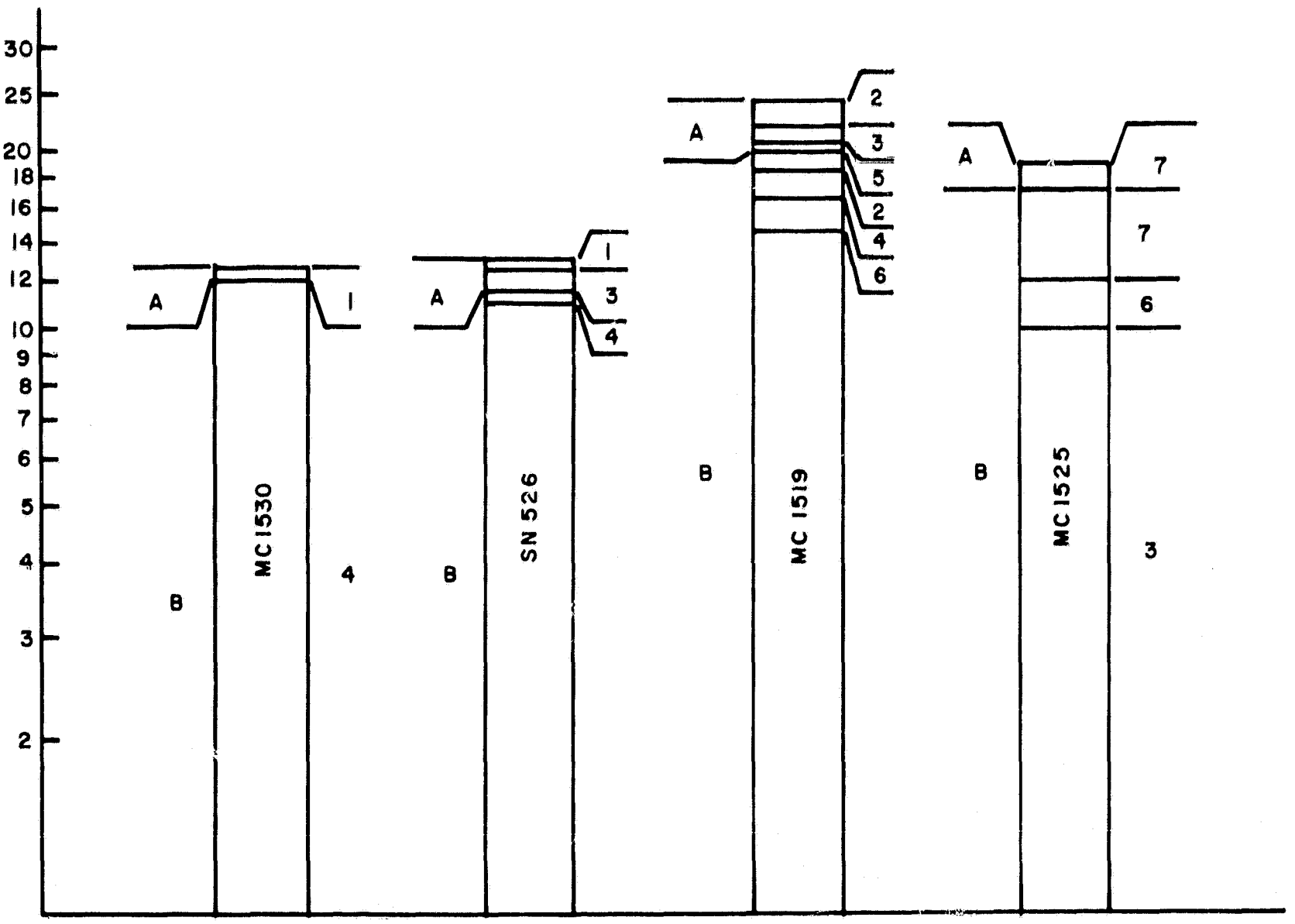
5.7 COMPARISON OF SURVEY AND TEST PROGRAM RESULTS

The results of the literature survey is further summarized in Table 5-I. The table also shows the results of the test program in terms of these mechanisms, showing the total number of failures attributable to each major grouping, i.e. lead bonds metallization, surfaces, bulk, package and miscellaneous mechanisms. These results clearly show that many of the failure mechanisms, which have historically had significance in causing integrated circuit failures, did not affect the devices tested to any extent which was detectable by this program. Most of the failures in this program involved either the metallization or the lead bonds, and occurred at greatly accelerating stress levels. The exception to this was the MC-1525, some of which exhibited an uncontrolled PNPN action at the maximum power level of the device, i.e., at the minimum emitter resistance in the current source transistor. This has been classified as a bulk failure mechanism although it is more of a design limitation rather than a failure mechanism, as such. Figure 5-1 shows the total percentage failure for each device type, and the contribution to the total by each failure mode. The graphs also show the proportion of failures which occurred during the normal stresses and those levels beyond the design ratings of the device. This figure shows, graphically, the excellent reliability characteristics of integrated circuit amplifiers.

TABLE 5-I

COMPARISON OF TEST PROGRAM AND LITERATURE SEARCH RESULTS

Failure Mechanism	Number of Failures Noted			
	MC-1530	SN-520	MC-1519	MC-1525
Wire Bond Failure Mechanisms (Total)	0	23	28	18
Intermetallic Compound	0	22	25	18
Overbonding	0	1	3	0
Underbonding	0	0	0	0
Mislocated Bond	0	0	0	0
Improper Lead Dress	0	0	0	0
Metallization Failure Mechanisms (Total)	23	1	4	0
Bad as Deposited or Etched	0	0	0	0
Damaged	0	0	0	0
Diffusion/Alloying	1	0	0	0
Excessive Current Density	22	1	4	0
Surface Failure Mechanisms (Total)	0	0	7	0
Passivation Defects	0	0	0	0
Inversion Channelling	0	0	7	0
Surface Contamination	0	0	0	0
Corrosion	0	0	0	0
Bulk Mechanisms (Total)	0	0	0	13
Package Failures (Total)	0	0	5	5
Faulty Seal	0	0	0	0
Foreign Material	0	0	0	0
Poor Die Bond	0	0	1	0
Misoriented Die	0	0	0	0
Package Surface Contamination	0	0	0	0
External Lead Failure	0	0	4	5
Misc. Mechanisms (Total)	1	1	0	0
Improper Mask	0	0	0	0
Improper Etch	0	0	0	0
Cracked Die	0	0	0	0
Etch Pits	0	0	0	0
Test Errors	1	1	0	0



TEST CONDITIONS:

A. Stress levels were within the manufacturers ratings for the device.

B. Stress levels were above manufacturers ratings for the device.

FAILURE MODES:

1. Test error
2. Channelling
3. Open bonds
4. Metallization failure
5. Die mount/bond failure
6. Package failure
7. Bulk failure mechanisms

Figure 5-1. Percent Defective Due to Each Major Failure Mode

APPENDIX A

LIFE TEST CIRCUITS

The purpose of operating life or burn-in tests is to accelerate those mechanisms which lead to premature failure of a device under normal operating stress or to provide an estimate of the life expectancy of devices during normal operation. Functional tests (i.e., operating the device in a fashion similar to which it will be used in a system) are the most attractive to most circuit designers. As integrated circuits become more complex, however, it is increasingly difficult to increase the electrical stress levels so that the basic mechanisms which cause failures will be accelerated without either violating the operational or functional design of the circuit, or introducing stress levels in the interior of the device which are so far removed from normal operation that correlation between the accelerated level and the normal operating stress level becomes obscure. Other techniques must, therefore, be developed considering not only the physical reactions or processes which lead to failure but the logistic factors of time and facility costs if economical procurement of high reliability linear integrated circuits is to become a reality. This means that burn-in or life testing techniques must be compatible with standard quality assurance procedures. Past experience with digital integrated circuits has indicated that, in a vast majority of cases, a combination of dc bias and temperature will accelerate most of the failure modes that are present. If we consider that the basic structure of linear integrated circuits and the processing techniques utilized in their fabrication are no different than those used in the production of digital integrated circuits, then it follows that the same mechanisms found in the digital circuit should also be present in the linear circuit. Relative frequency of occurrences may differ due to such differences as material resistivity, chip area, etc. In considering the foregoing factors, dc operational life tests were chosen for this program.

An analysis was made of each device at each stress level to determine the concentration of stress within the integrated circuit and is presented in this section.

ANALYSIS OF THE MC-1519 OPERATIONAL LIFE TEST CIRCUIT

The circuit selected for the MC-1519 at the 100- and 300-mW levels was a dc biased operational life test with controlled stresses applied to various regions in the devices. The basic technique utilized here fixes the stress levels by fixing the voltages at two different points in the circuit. The electrical schematics are shown in Figures A-1 and A-2. In these circuits each circuit element was identified by notations that aid in the analysis that follows. One of the significant features in this test design was that it encompasses a considerable degree of simplicity and duplicates, statically, the stresses that the elements of the circuit are expected to see under normal operational performance. The circuits shown in Figures A-1 and A-2 are quite similar to the basic electrical parameter test circuit required to perform differential gain, input offset voltage, and other electrical measurements. Differences occur only in the sense that the collector of the differential pair of PNP transistors is connected to pin 5 instead of the V_{EE} supply, permitting circuit power control by the transistor labeled Q_5 in the diagram. This permits a logical extension in high power levels beyond 300 mW for the power step stresses bias conditions by extending these collector leads to the V_{EE} supply.

As is noted in these circuit schematics, the bias levels are controlled by grounding the base input terminal of transistors Q_1 and Q_2 (pins 4 and 8) and by establishing the proper bias level at pin 6 to control the total current flow through R_3. These factors permit, with minor modifications, the adaptation of this circuit to a high volume screen burn-in requirement. If the voltage at pin 6 is fixed at a level determined to give x milliwatts of power, assuming

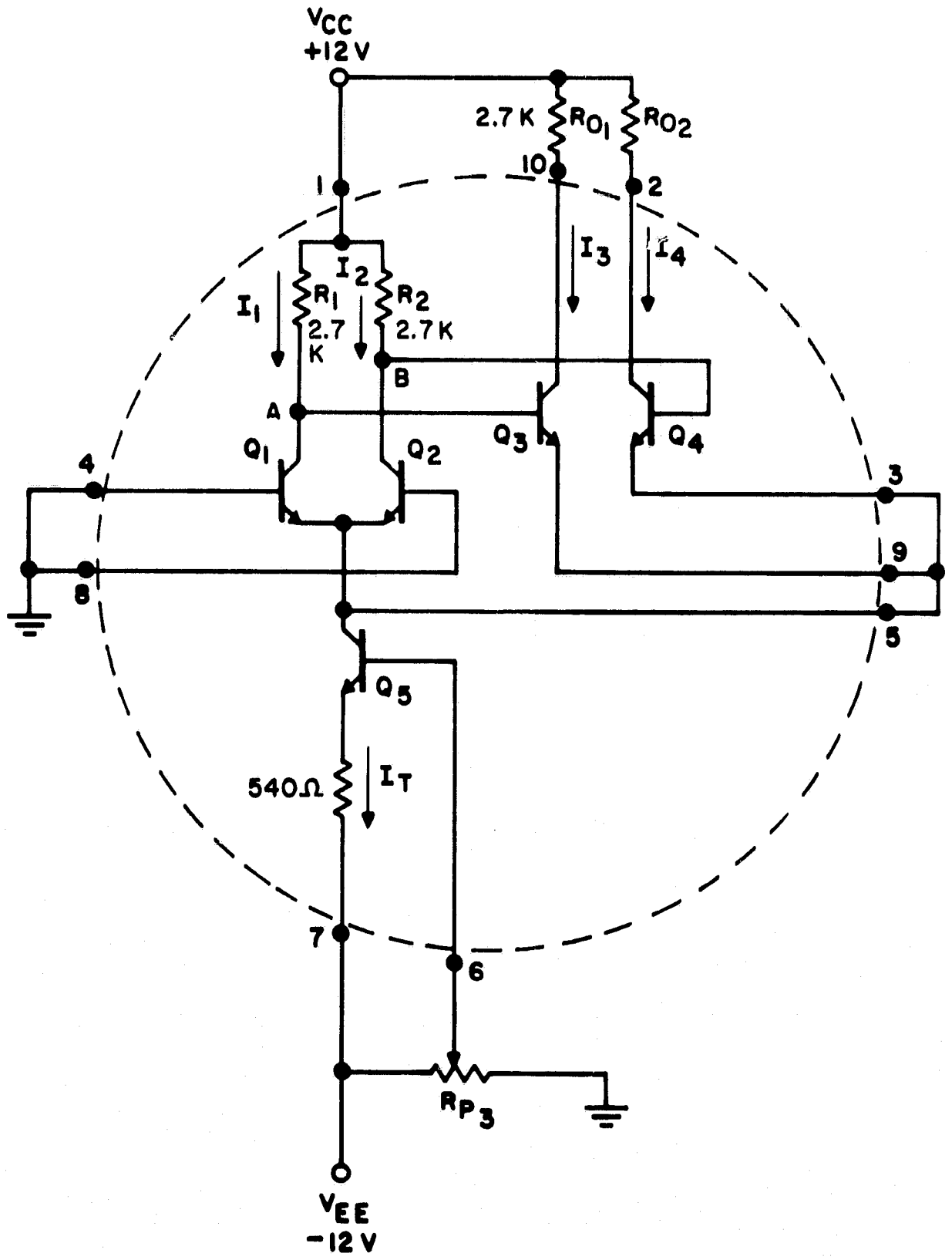


Figure A-1. 100-Milliwatt Life Test Circuit for MC-1519

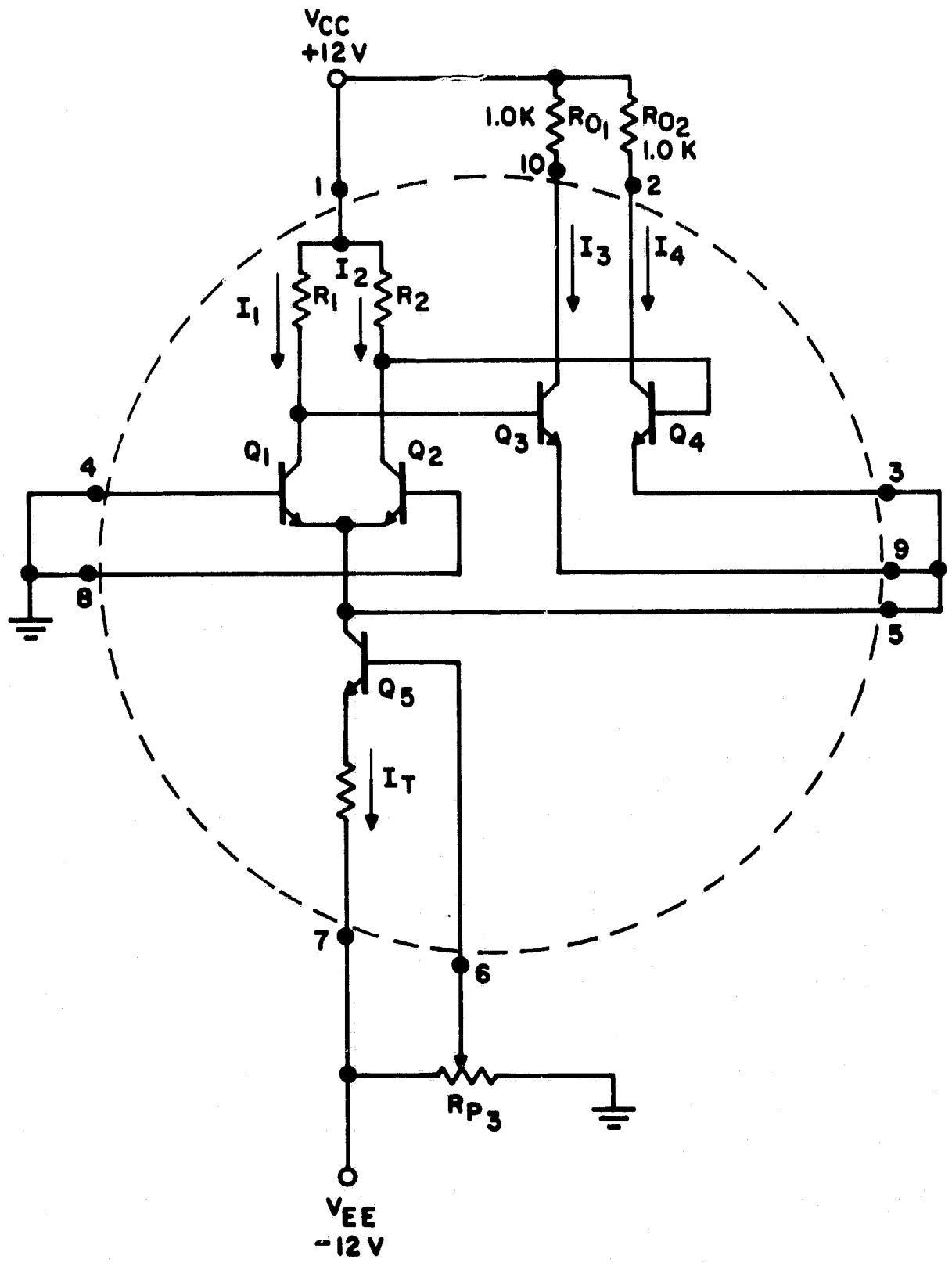


Figure A-2. 300-Milliwatt Life Test Circuit for MC-1519

an absolute value of R_3 equaling 540 ohms, than the total distribution of power in any population of devices subjected to this burn-in stress will then see power conditions proportional to the distribution of resistance values for these circuits. Normally, in the manufacture of integrated circuits, the diffused resistor tolerances are sought to be less than $\pm$20 percent. In this circuit, because its resistors are Nichrome deposited thin film, the distribution of power levels should be much better. However, this reliability study program will include a variable potentiometer in our network which will permit the final adjustment of the value of I_T for each circuit so that the total power of the circuit can be set at the exact level desired. A description of the circuit functions and a breakdown of the power dropped across each circuit component follows in the next two sections.

100-Milliwatt Life Test Circuit

The circuit for this test is shown in Figure A-1. The power dissipated in this circuit is equal to the total circuit current flow (i.e., through R_3) times the applied voltage (V_{CC} - V_{EE} = 24 volts) minus the power consumed in the external load resistors Ro_1 and Ro_2. It can be defined as follows:

$$Pd_T = Pd_{Ro} + Pd_c$$

where Pd_T is total circuit power consumption

Pd_{Ro} is power lost in the load resistors

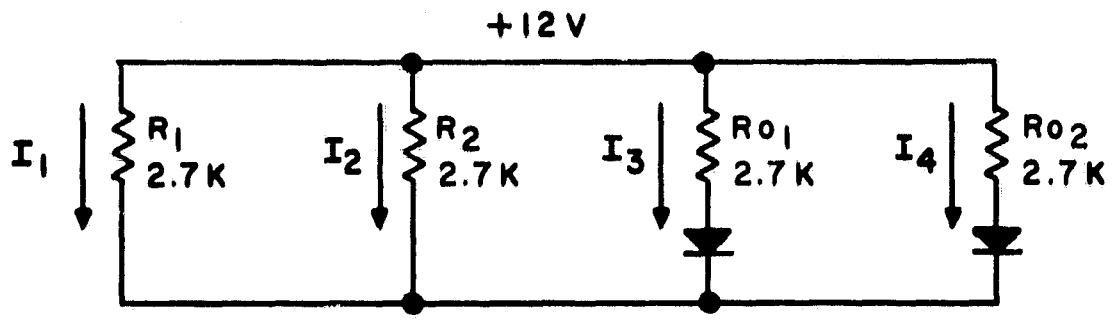
Pd_c is power used in MC-1519 circuit

V_{CC} = +12 Vdc

V_{EE} = -12 Vdc

$$Pd_T = I_T (V_{CC} - V_{EE}) = 24\ I_T$$

Considering the load circuits of R_1, R_2, Ro_1, and Ro_2 to be as follows and equal to I_T



then it is seen that the current drain in the output load resistors will equal R_1 or R_2 minus a factor equal to:

$$\frac{V_{BE}}{2.7\ k\Omega} = 0.27\ mA$$

Since $I_1 + I_2 + I_3 + I_4 \approx I_T$

then

$$I_T = 4I_3 + 0.54\ mA$$

and

$$I_3 = \frac{I_T - 0.54\ mA}{4} \qquad (1)$$

$$Pd_{Ro} = I_3^2\ Ro + I_4^2\ Ro = 2I_3^2\ Ro$$

$$Pd_{Ro} = \frac{Ro}{8}\ (I_T - 0.54\ mA)^2$$

Then

$$Pd_c = 24I_T - \frac{Ro}{8}\ (I_T - 0.54\ mA)^2 \qquad (2)$$

In this circuit it is necessary to set Pd_c and control I_C by raising and lowering the voltage drop at pin 6. If it is assumed that

$$R_3 = 540 \text{ ohms}$$

$$Pd_c = 100 \text{ milliwatts}$$

$$Ro = R_1 = R_2 = 2.7 \text{ k ohms}$$

Then equation (2) can be rearranged as follows:

$$\frac{Ro}{8} (I_T - 0.54 \text{ mA})^2 - 24 I_T + 100 = 0$$

$$I_T^2 - 2(0.54 \times 10^{-3})(I_T) + (0.54 \times 10^{-3})^2 - \frac{(24)8}{Ro} I_T + \frac{(0.1)8}{Ro} = 0$$

$$I_T^2 \left[- 2(0.54 \times 10^{-3}) + \frac{(24)8}{Ro} \right] I_T + (0.54 \times 10^{-3})^2 + \frac{(0.1)8}{Ro} = 0$$

$$I_T = \frac{\left[2(0.54 \times 10^{-3}) + \frac{(24)8}{Ro} \right]}{2} - \sqrt{\frac{\left[2(0.54 \times 10^{-3}) + \frac{(24)8}{Ro} \right]^2 - 4 \left[(0.29 \times 10^{-6} + \frac{(0.1)8}{Ro} \right]}{2}}$$

$$I_T = \frac{72.19 \times 10^{-3}}{2} - \sqrt{\frac{5.211 \times 10^{-3} - 1.186 \times 10^{-3}}{2}}$$

$$= \frac{72.14 \times 10^{-3}}{2} - \sqrt{\frac{4.025 \times 10^{-3}}{2}}$$

$$= \frac{72.19 - 63.44}{2} \times 10^{-3} = \frac{8.75 \times 10^{-3}}{2} \text{ Amperes}$$

$$I_T = 4.37 \text{ mA}$$

From equation (1):

$$I_3 = \frac{I_T - 0.54 \text{ mA}}{4} = \frac{3.83}{4} \text{ mA}$$

$$= 0.96 \text{ mA}$$

To calculate the theoretical value of the pin 6, it is only necessary to convert the equation from I_T in terms of V_6 (voltage at pin 6).

$$I_T = \frac{V_{EE} - (V_6 - 0.7 \text{ V})}{R_3} = \frac{V_{EE} - V_6 + 0.72 \text{ volt}}{540 \text{ ohms}}$$

$$V_6 = V_{EE} + 0.72 \text{ volt} + 540 \, I_T$$

$$= -12 \text{ V} + 0.72 \text{ V} + (540 \text{ ohms}) \, (4.37 \text{ mA})$$

$$= -11.28 + 2.36$$

$$= -8.92 \text{ volts}$$

In all these calculations, the voltage is referenced to the 0 voltage potential at pins 4 and 8 and that the forward voltage drop (base-emitter) V_{BE} is assumed to be 0.72 volt. Using the typical values for the circuit components and the calculated value of I_T, estimates of the power dissipated by each circuit element can be calculated. They are:

A. Resistor R_3

$$Pd_{R_3} = (I_T)^2 R_3 = (4.37)^2 \quad (0.54) \times 10^{-3} \text{ mW}$$

$$= 10.3 \text{ mW}$$

B. Transistor Q_5

$V_{CE} = V_6$ for all power levels

$$Pd_{Q_5} = V_{CE} \times I_T = V_6 \times I_T = (8.92 \text{ volts}) \ (4.37 \text{ mA})$$

$$= 38.98 \text{ mW}$$

C. Transistors Q_1 and Q_2

Neglecting the incremental increase in collector currents resulting from the base currents of transistors Q_3 and Q_4 because they will contribute less than 2 percent of the transistor currents for Q_1 and Q_2

$$V_{CE_{Q_1}} = V_{CC} - (2.7 \text{ k}\Omega)(0.96 \text{ mA} + 0.27 \text{ mA}) + 0.72 \text{ volt}$$

$$= 9.4 \text{ volts}$$

$$Pd_{Q_1} = Pd_{Q_2} = I_1 \times V_{CE_{Q_1}} = (1.23 \text{ mA})(9.4 \text{ V})$$

$$= 11.6 \text{ mW}$$

D. Transistors Q_3 and Q_4

Because the collector voltages of transistors Q_1 and Q_2 are clamped by the V_{BE} diodes of the PNP transistor, it then follows:

$$V_{CE_{Q_3}} = V_{CE_{Q_4}} = V_{CE_{Q_1}} + 0.72\ V = 10.1\ V$$

Then

$$Pd_{Q_4} = PD_{Q_3} = I_3 \times V_{CE_{Q_3}} = 10.1\ V \times 0.96\ mA$$

$$= 9.7\ mW$$

E. Resistors R_1 and R_2

$$I_1 = I_2 = 1.23\ mA$$

$$R_1 = R_2 = 2.7\ k\Omega$$

$$Pd_{R_1} = Pd_{R_2} = (1.23)^2(2.7) \times 10^{-3}$$

$$= 4.07\ mW$$

A summary of the power dissipation characteristics would be:

Transistor Q_1 = 11.6 mW
Transistor Q_2 = 11.6 mW
Transistor Q_3 = 9.7 mW
Transistor Q_4 = 9.7 mW
Transistor Q_5 = 39.0 mW

Resistor R_1 = 4.07 mW
Resistor R_2 = 4.07 mW
Resistor R_3 = 10.3 mW

In analyzing this 100-mW test setup, it is noted that all transistors are set at such a level that they have a minimum of 9.0 volts collector to emitter, that the monolithic chip with the Nichrome resistors is stressed with 80 percent of the power or 80.5 mW and that this factor is very nearly in proportion to the ratio of the cross-sectional areas of the two dice in question. This ratio is approximately equal to 3:1.

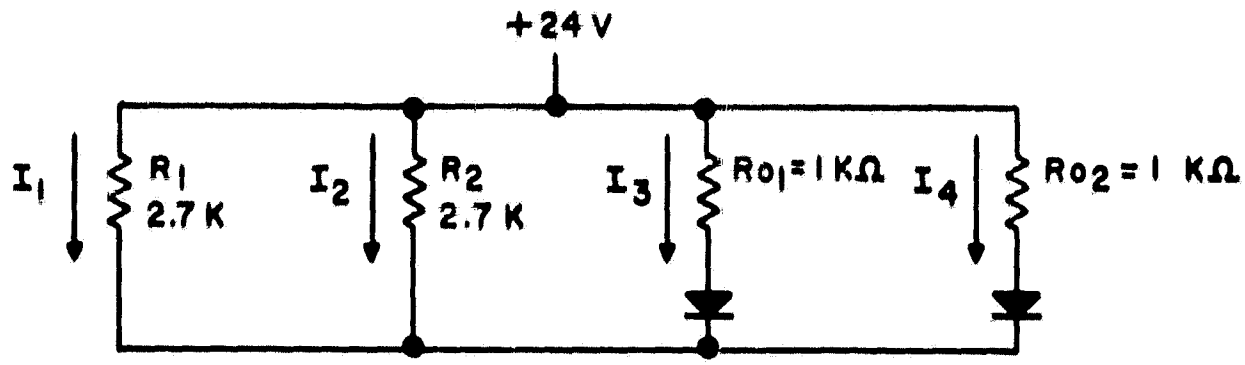
The analysis of the 300-mW stress test setup will further verify that by minor adjustment in load resistor values and voltages applied to pin 6 this technique can be utilized for a variety of stress levels.

300-Milliwatt Operating Life Test

The analogy for this circuit is similar to that used for the 100-mW life test circuit except that the external resistors have been decreased in value requiring the PNP transistors to take a larger share of the current load, thereby dissipating a large percentage of the power. For this circuit equation (1) has been modified to:

$$Pd_c = 24I_t - 2Ro \quad I_3^2 \qquad (3)$$

Unlike the 100-mW case where the resistances R_1, R_2, Ro_1, Ro_2 were equal to 2.7 k ohms, the simple dc analysis of power loss in the external load resistances requires a slightly different analysis. First, considering the load bridge to be:



and that

$$I_1 + I_2 + I_3 + I_4 + 2I_{B_{Q_1}} = I_T$$

ignoring the base current factors for pins 9 and 8 ($2\ I_{B_{Q_1}}$) because it should be less than 2 percent of the total current and assuming that $Ro_1 = Ro_2$ and that $R_1 = R_2$ the it follows that the voltage drop across each line is the same (call V_{c1}) then

$$I_T = \frac{V_{c1}}{R_1} + \frac{V_{c1}}{R_2} + \frac{V_{c1}}{Ro_1} - \frac{V_{BE}}{Ro_1} + \frac{V_{c1}}{Ro_2} - \frac{V_{BE}}{Ro_2}$$

$$I_T = V_{c1}\left(\frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{Ro_1} + \frac{1}{Ro_2}\right) - V_{BE}\left(\frac{1}{Ro_1} + \frac{1}{Ro_2}\right)$$

and since $Ro_1 = Ro_2 = 1\ k\Omega$

$$I_T + 2\left(\frac{0.72\ V}{1\ k}\right) = I_1 + I_2 + I_3 + I_4$$

In this equation

$$I_3' = I_3 + 0.72\ mA$$

$$I_4' = I_4 + 0.72\ mA$$

and have no physical analogy being used for aid in the mathematical

$$I_1 = \frac{V_{c1}}{2.7\ k\Omega} \text{ and } I_3' = \frac{V_{c1}}{1\ k\Omega}$$

$$V_{c1} = 2.7\ k\Omega\ I_1 = 1\ k\Omega\ I_3'$$

$$I_1 = \frac{1}{2.7}\ I_3'$$

$$I_1 = I_2,\ I_3 = I_4$$

$$I_T + 1.44\ mA = 2I_1 + 2I_3'$$

$$= \frac{2}{2.7}\ I_3' + 2I_3' = 2\left(1 + \frac{1}{2.7}\right)\ I_3$$

$$= \frac{7.4}{2.7}\ I_3'$$

then

$$I_3' = \frac{I_T + 1.44\ mA}{7.4}\ 2.7 \qquad (4)$$

$$I_3 = \frac{2.7}{7.4}\ (I_T + 1.44\ mA) - 0.72\ mA \qquad (5)$$

Now substituting equation 5 into equation 3

$$Pd_c = 24I_T - 2Ro\left[(I_T + 1.44 \times 10^{-3})\ \frac{2.7}{7.4} - 0.72 \times 10^{-3}\right]^2$$

and I_T becomes equal to

$$I_T = \frac{91.71 \times 10^{-3} - 38.78 \times 10^{-4}}{2}$$

$$= \frac{91.71 - 62.27}{2} = \frac{29.44}{2}$$

$$= 14.7 \text{ mA} \quad \text{for Ro} = 1 \text{ k}\Omega$$

$$Pd_c = 300 \text{ mW}$$

This results in:

$$V_6 = -3.33 \text{ volts}$$

$$I_1 = I_2 = 2.18$$

$$I_3 = I_4 = 5.16 \text{ mA}$$

This results in the following calculation of component dissipations:

Transistor Q_1 = 14.9 mW

Transistor Q_2 = 14.9 mW

Transistor Q_3 = 39.0 mW

Transistor Q_4 = 39.0 mW

Transistor Q_5 = 48.9 mW

Resistor R_1 = 12.6 mW

Resistor R_2 = 12.6 mW

Resistor R_3 = 116.7 mW

At this stress level, the relative percentage of power consumed by the PNP transistor chips has increased to approximately 30 percent of the total circuit power. Since this is in proportion to the relative cross-sectional areas of the two silicon dice, the assumption can be made that the average junction temperatures are nearly equal, a very important factor that must be considered whenever possible as the power levels are increased.

MC-1525 Life Test Analysis

It can be shown that any imbalance between the currents of the differential transistors, Q_1 and Q_3, has no effect as long as the sum of the currents remains constant. The circuit analysis may, therefore, be simplified by the use of a single equivalent stage in the collector of Q_2. Figure A-4 shows this equivalent circuit.

The circuit may be further simplified by the use of a Helmholtz-Thevinen equivalent circuit at the input to Q_2 with the parameters as shown in Figure A-5.

Solving for the currents in Q_2, we have:

$$V' = I_b R' + (B+1) I_b R_3 + V_{be}$$

$$V' = I_b [R' + (B+1) R_3] + V_{be}$$

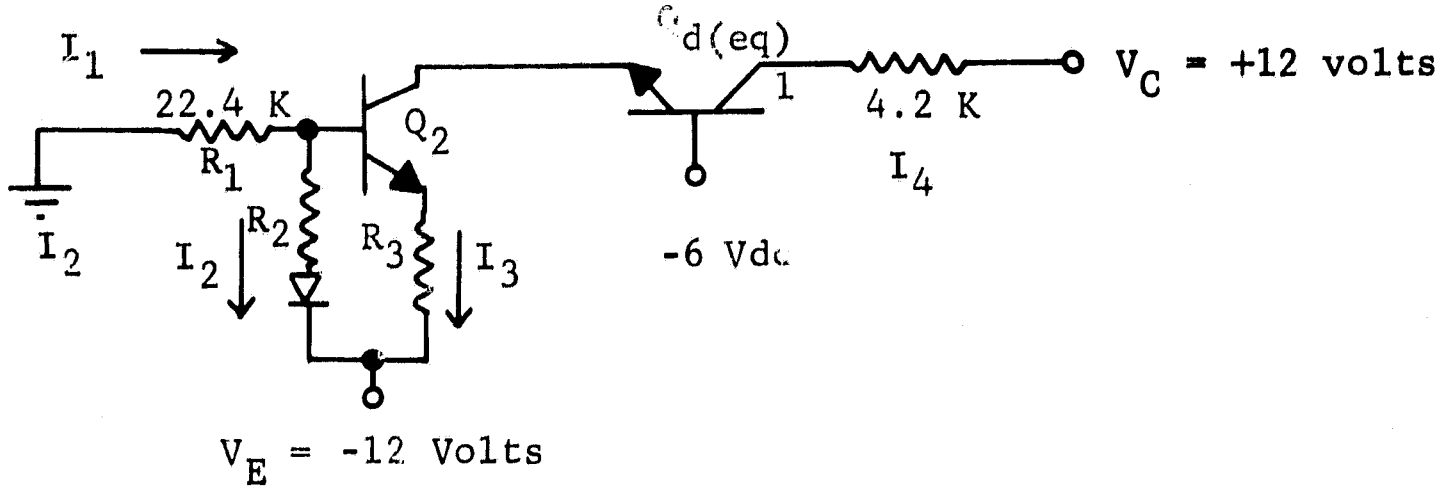


Figure A-3. MC-1525 Equivalent Circuit

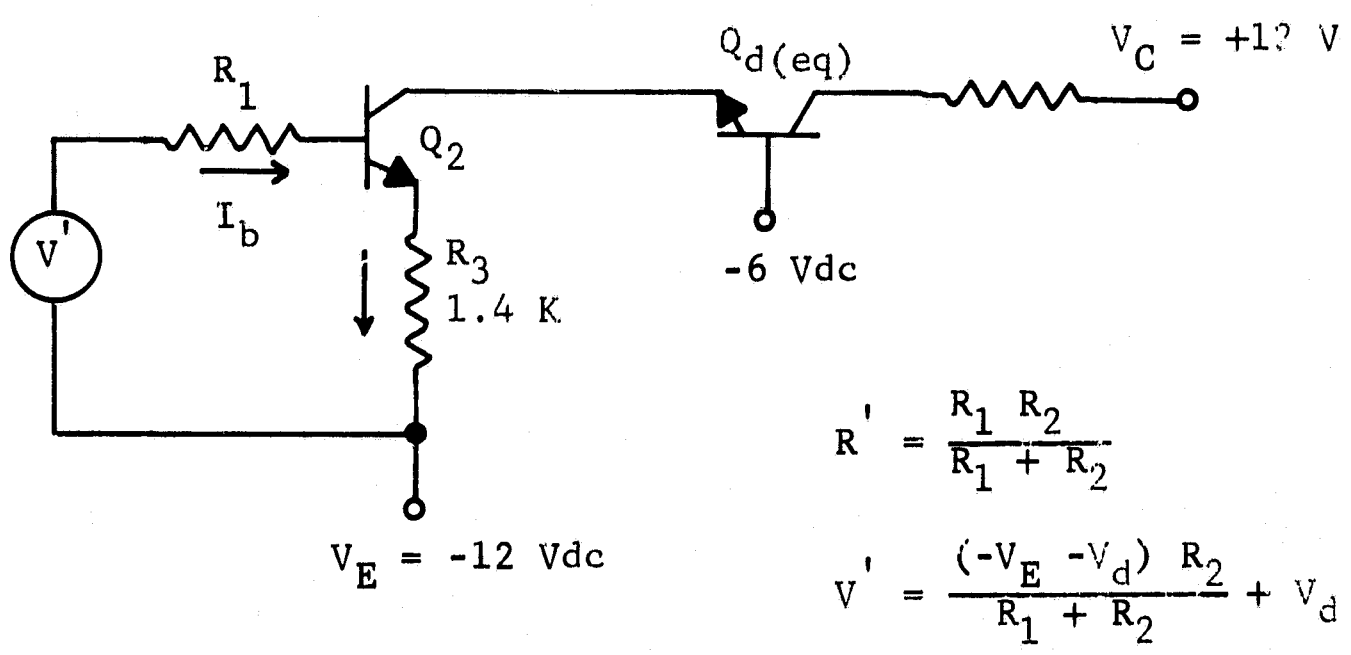


Figure A-4. MC-1525 Equivalent Circuit Using Equivalent Voltage Source in Base of Q_2

$$I_b = \frac{V' - V_{be}}{R' + (B + 1)\ R_3}$$

$$I_e = \frac{(B + 1)\ (V' - V_{be})}{R' + (B + 1)\ R_3}$$

$$I_c = I_e\ (Q_{eq}) = \frac{B\ (V' - V_{be})}{R' + (B + 1)\ R_3}$$

Evaluating the quantity $(V' - V_{be})$ assuming $V_d = V_{be} = 0.6$ volt

$$V' = \frac{(-V_{EE} - V_d)\ R_2}{R_1 + R_2} + V_d$$

$$V' = \frac{[-(-12) - 0.6]\ 11.2 \times 10^3}{(11.2 + 22.4)\ 10^3} + 0.6$$

$$V' = \frac{11.4}{3} + 0.6 = 3.8 + 0.6 = 4.4 \text{ volts}$$

$$V' - V_d = 3.8 \text{ volts}$$

The equivalent source resistance, neglecting the dynamic resistance of the diode, is

$$R' = \frac{R_1\ R_2}{R_1 + R_2} = \frac{11.2 \times 22.4}{11.2 + 22.4} \times 10^3 = \frac{22.4}{3}\ k\Omega$$

$$R' = 7.47\ k\Omega$$

Assuming a beta of 50 which corresponds to an $\alpha = 0.98$, then

$$I_b = \frac{3.8}{(7.47 + 51 \times 1.4) \times 10^3} = 48\ \mu A$$

$$V_{R_3} = (B + 1)\ I_b\ R_E = 51 \times 48 \times 10^{-6} \times 1.4 \times 10^3$$

$$V_{R_3} = 3.4 \text{ volts}$$

$$V_{e(Q_2)} = V_{R3} + V_{EE}$$

$$V_{E(Q_2)} = 3.4 + (-12) = -8.6 \text{ volts}$$

$$V_{C(Q_2)} = -6.6 \text{ volts}$$

$$V_{CE(Q_2)} = 2.0 \text{ volts}$$

$$I_{C(Q_2)} = BI_b = 50 \times 48 = 2.4 \text{ mA}$$

$$V_{R2} = V_{R3} + V_{be} - V_d = 3.4 \text{ volts}$$

$$I_2 = \frac{V_{R2}}{R_2} = \frac{3.4}{11.2} \times 10^{-3} = 0.30 \text{ mA}$$

$$I_{E(Q_{eq})} = I_{C(Q_2)} = 2.4 \text{ mA}$$

$$V_{e(Q_{eq})} = V_{bb} - V_{be} + -6.6 \text{ volts}$$

$$V_{C(Q_{eq})} = V_{cc} - \alpha I_e R_{(eq)}$$

$$V_{C(Q_{eq})} = 12 - 9.9 = 2.1 \text{ volts}$$

and

$$V_{ce(Q_{eq})} = 2.1 - (-6.6) = 8.7 \text{ volts}$$

Calculating the total power

$$P_T = V_{CC} I_{CC} + V_{EE} I_{EE} + V_{BB} I_{bb(eq)}$$

$$P_T = 12 \times 2.35 \times 10^{-3} + (+12)(0.3 + 2.45)10^{-3} + (-6)(+48)10^{-6}$$

$$P_T = 60.9 \text{ mW}$$

The power dissipation in each element in the device can now be evaluated

$$P_{R1} = (I_2 + I_b)^2 R_1 = (0.348 \times 10^{-6})^2 \times 22.4 \times 10^3$$

$$P_{R1} = 2.7 \text{ mW}$$

$$P_{R2} = I_2^2 \, R_2 = (0.3 \times 10^{-3})^2 \times 11.2 \times 10^3$$

$$P_{R2} = 1.0 \text{ mW}$$

$$P_R = I_3^2 \, R = [(B + 1) \, I_b]^2 \, R = [51 \times 48 \times 10^{-6}]^2 \, 1.4 \times 10^3$$

$$P_R = 8.4 \text{ mW}$$

Neglecting the $V_{be} \, I_b$ term

$$P_{Q2} = I_c \, V_{EE} = 2.0 \times 2.4 \times 10^{-3}$$

$$P_{Q2} = 4.8 \text{ mW}$$

Assuming $\alpha_{(Qeq)} = 1$

$$P_{R(eq)} = (I_{c(Qeq)}) \, R_{eq} = (2.35 \times 10^3)^2 \times 4.2 \times 10^3$$

$$P_{R(eq)} = 23.4 \text{ mW}$$

Assuming matched conditions on the differential transistors, Q_1 and Q, this power may be assumed to divide equally, so that one-half of the above power is dissipated in each resistor. The power dissipated in each resistor is then

$$P_{R_4} = P_{R_5} = 11.6 \text{ mW}$$

Using the value calculated for $V_{CE(Q_{eq})}$ and assuming a matched condition (0 offset), then

$$P_{Q1} = P_{Q3} = \frac{1}{2} \quad (V_{CE}\ I_C)$$

$$P_{Q1} = P_{Q3} = \frac{1}{2}\ (8.7 \times 2.35)$$

$$P_{Q1} = P_{Q3} = 20.4 \text{ mW}$$

$$P_{D1} = 0.6 \times 0.3 = 0.18 \text{ mW}$$

Approximately 58 percent of the power is being dissipated in the resistor network and approximately 14 percent is dissipated in each of the input transistors, Q_1 and Q_3, and 14 percent in the current source transistor, Q_2.

MC-1530 100-Milliwatt Test Circuit

The life test circuit for the 100-milliwatt test is shown in Figure A-6. In calculating the power dissipated in each circuit element, the external capacitance can be disregarded for its purpose is to suppress random oscillations that can occur if the circuit is not properly designed. Considering the input differential stage of the amplifier, we determine the voltages at different points in the circuit and thus estimate the power dissipated in the elements of that section of the device. If we assume that the input differential transistors are matched, the circuit may be redrawn as shown in Figure A-6 for the bias conditions shown in Figure A-7.

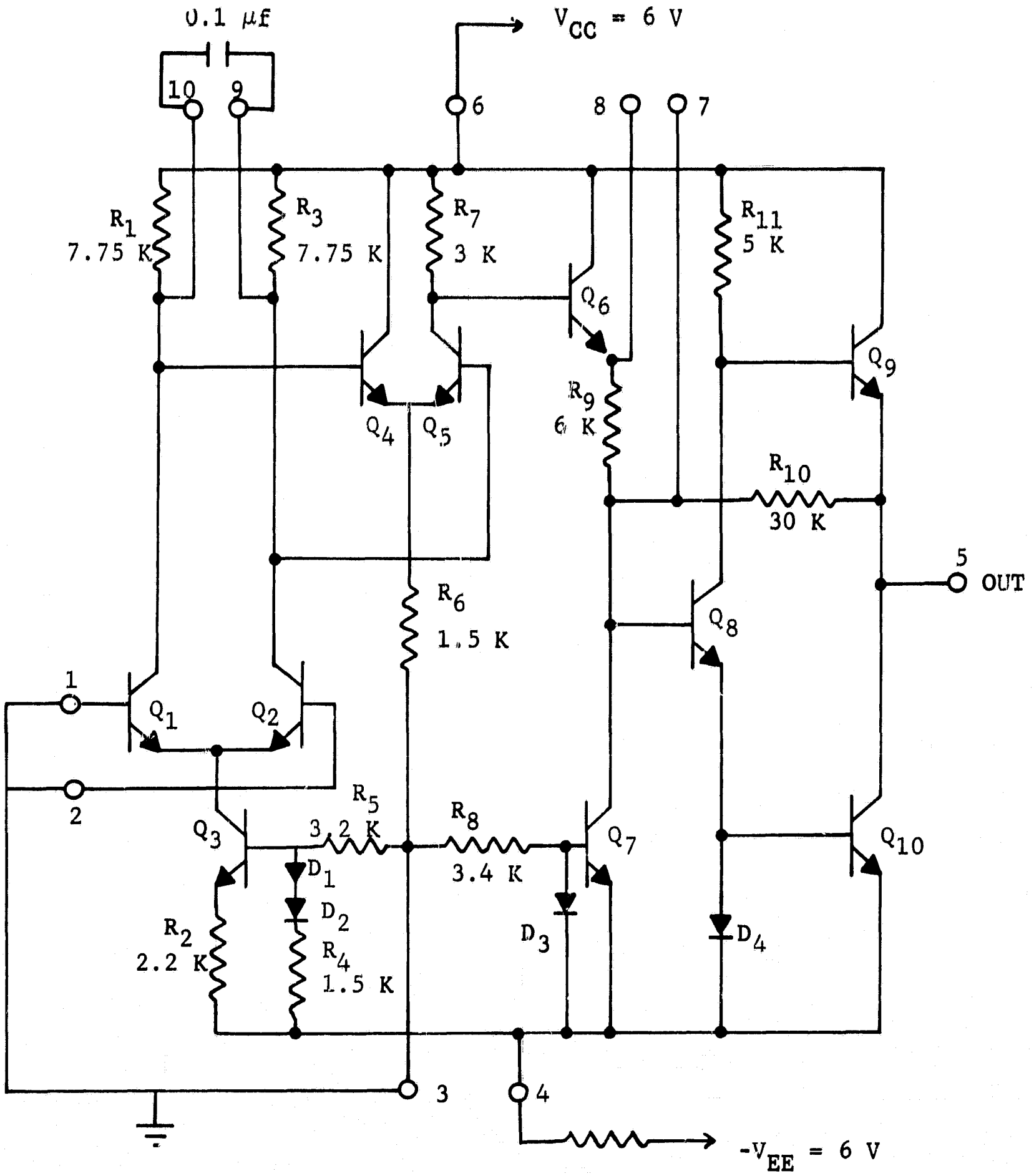


Figure A-5. MC-1530 Operating Life Test Circuit

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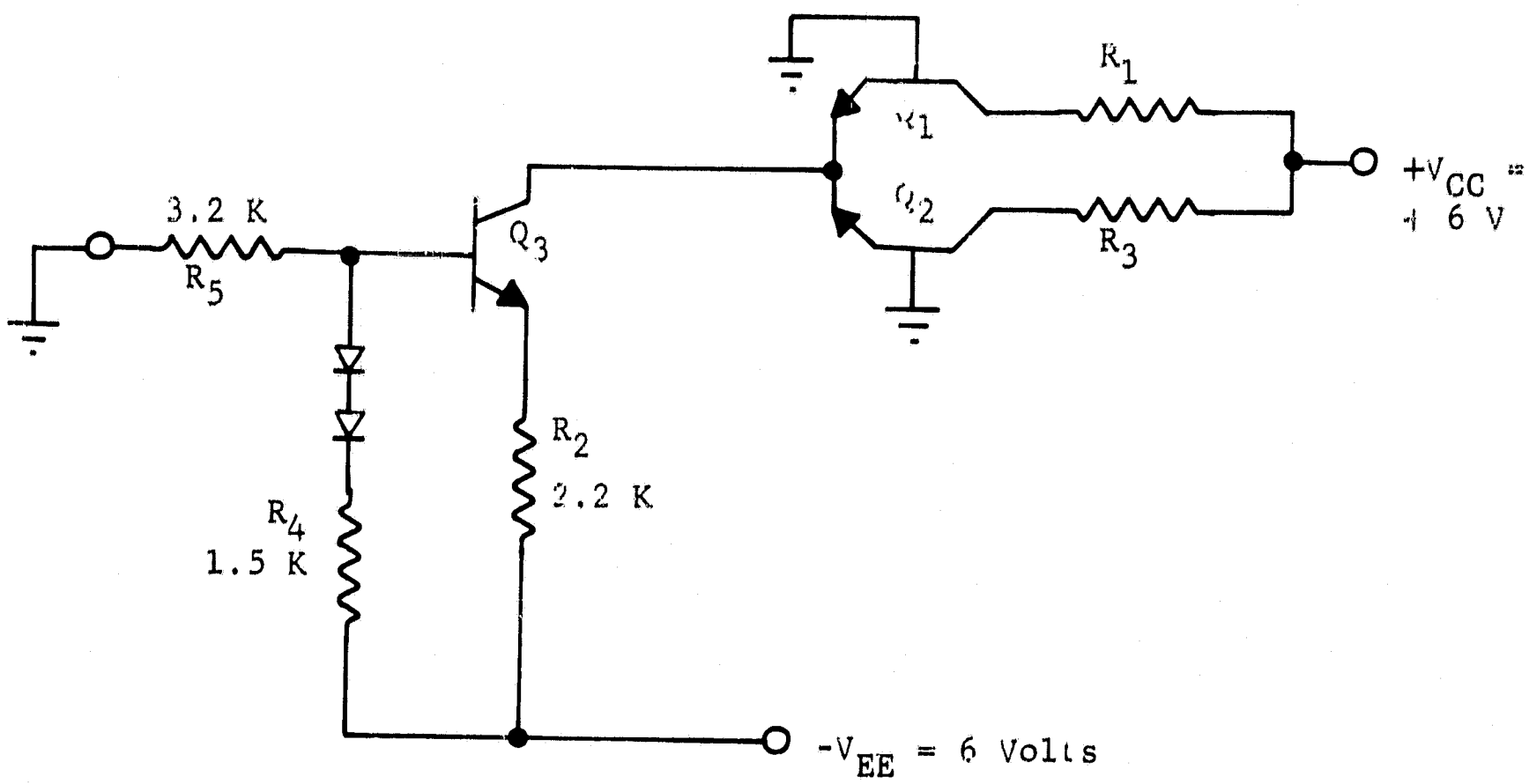


Figure A-6. MC-1530 Input Differential Amplifier Section

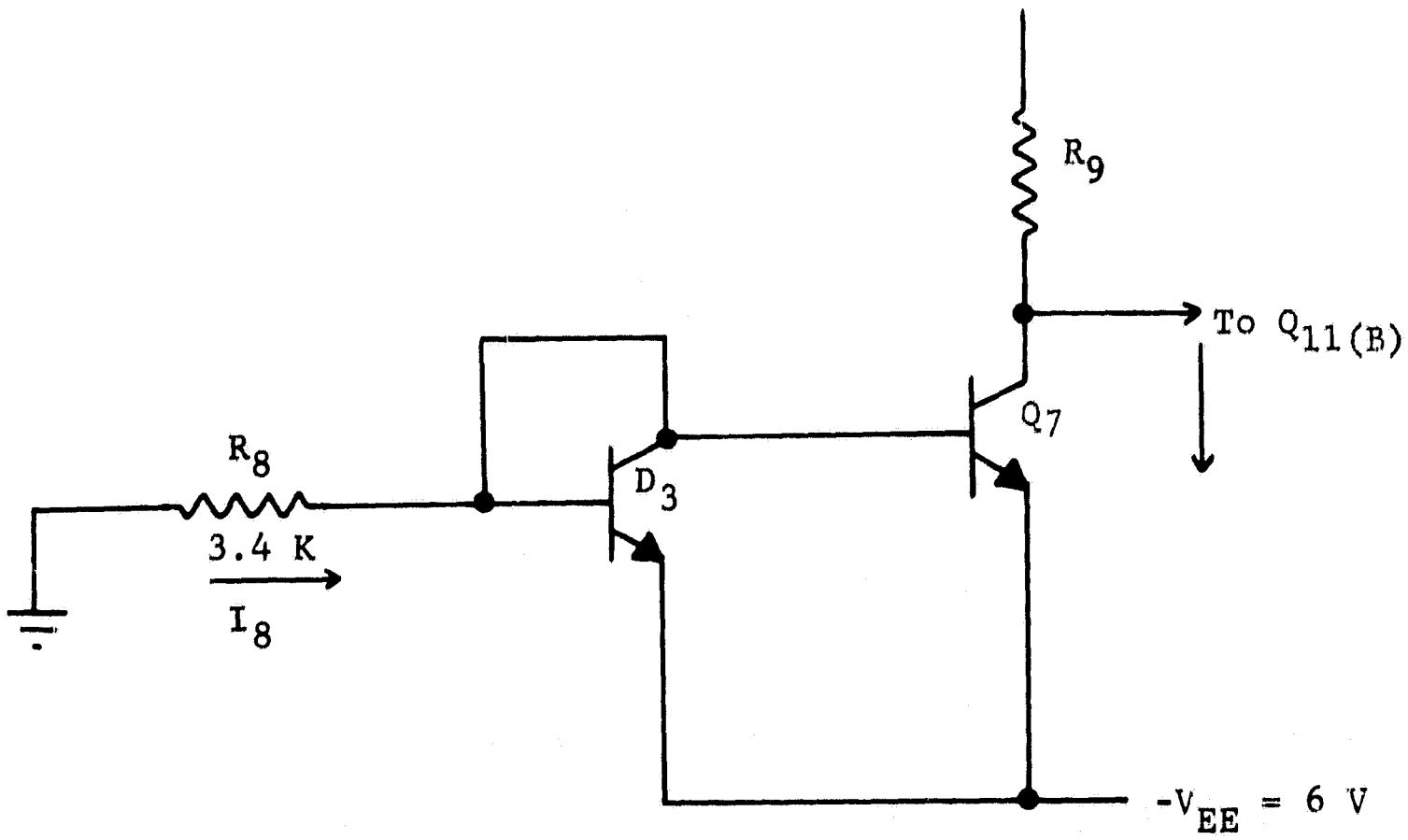


Figure A-7. MC-1530 Level Shifter Section

Assuming $\alpha = 1$ for both transistors, we may then calculate the voltage at the base of Q_3 and use the voltage to calculate the current through R_2, which is approximately equal to the collector current. Assuming $V_d = 0.7$ volt and $I_b \approx 0$.

$$V_{B\text{-}Q3} \approx \frac{[-6 + 2(0.7)\ R_5]}{(R_4 + R_5)} \approx -3.2\ V \qquad (6)$$

then

$$I_{R_2} \approx \frac{V_{EE} - (V_{B\text{-}Q3} - 0.7)}{R_2} \approx 1.0\ mA \qquad (7)$$

Then assuming that $I_{C\text{-}Q1} = I_{C\text{-}Q2} = 1/2\ I_{C\text{-}Q3}$ ($\alpha = 1$) and resistors R_1 and R_3 are matched, the voltage at the collectors of Q_1 and Q_2 can be determined neglecting the base currents of Q_4 and Q_5 by the equation.

$$V_{C\text{-}Q1} \approx V_{C\text{-}Q2} \approx V_{CC} - \frac{R_3}{2R_2} \left[V_{EE} + 0.7 - \frac{(V_{EE} + 1.4)\ R_5}{R_4 + R_5}\right] \qquad (8)$$

$$V_{C\text{-}Q2} \approx +2.2 \text{ volts}$$

This voltage also appears at the bases of Q_4 and Q_5. The voltage at the emitter of these transistors is then:

$$V_{E\text{-}Q4} = V_{E\text{-}Q5} \approx V_{B\text{-}Q4} - 0.7 \qquad (9)$$

$$V_{E\text{-}Q4} \approx 2.2 - 0.7 \approx 1.5 \text{ volts}$$

and

$$I_{R_6} \approx \frac{1.5 \text{ volts}}{1.5 \text{ K}} \approx 1 \text{ mA}$$

The voltage at the collector of Q_5 is then

$$V_{C\text{-}Q5} = V_{CC} - I_{C\text{-}Q5} R_7 \qquad (10)$$

assuming that transistors Q_4 and Q_5 are matched and $\alpha \approx 1$, then

$$V_{C\text{-}Q5} = V_{CC} - I_C R_7 \qquad (11)$$

$$V_{C\text{-}Q5} \approx 6 - (0.5 \times 3) \approx 4.5 \text{ volts}$$

and

$$V_{C\text{-}Q6} \approx 3.8 \text{ Vdc}$$

The meshes of the circuit consisting of R_8, D_3, and Q_7 may be analyzed in the following manner. The diode D_3 is formed as a transistor with the collector shorted to the base. The section is redrawn as shown in Figure A-8.

The current through the transistor connected as D_3 will be

$$I_{R_8} = \frac{-V_{EE} - V_{BE}}{R_8} \qquad (12)$$

$$I_{R_8} = \frac{6 - 0.7}{3.4 \text{ K}} = \frac{5.4}{3.4} = 1.58$$

If the transistors are identical, then the current in the emitter of Q_7 will be equal to the current of the emitter of the diode connected transistor D_3. Assuming further that $\alpha = 1$ then $I_{C\text{-}Q7} = I_{R_8}$ and the

collector of Q_7 behaves as a collector of a common base stage and may be represented as a current source equal to 1.58 mA.

The level shifting and output stages may then be redrawn as shown in Figure A-9. We can determine the voltage at the base of Q_8 as being two diode drops removed from $-V_{EE}$. Therefore:

$$I_{R_9} = \frac{V_{E\text{-}Q6} - V_{EE} - 1.4}{R_9} \qquad (13)$$

$$I_{R_9} \approx \frac{3.8 + 6 - 1.4}{6 \times 10^3} \approx 1.4 \text{ mA}$$

Summing the currents at the base of Q_8, neglecting the base current of Q_8, we have

$$I_{R_{10}} + I_{R_9} = I_{Q7} \qquad (14)$$

and

$$E_o = I_{R_{10}} R_{10} + V_{B\text{-}Q8} = \qquad (15)$$

$$I_{R_{10}} R_{10} + V_{EE} + 1.4 \text{ V}$$

Substituting equations 7, 8 and 9 into equation 10 and simplfying we have:

$$E_o \approx -V_{EE}\left(\frac{R_{10}}{R_8} - \frac{R_{10}}{R_9} - 1\right) - V_{E\text{-}Q6}\frac{R_{10}}{R_9} + 1.4\left(\frac{R_{10}}{R_9} - \frac{R_{10}}{2R_8} + 1\right) \qquad (16)$$

$$E_o \approx 6\left(\frac{30}{3.4} - \frac{30}{6} - 1\right) - 3.8\,\frac{30}{6} + 1.4\left(\frac{30}{6} - \frac{30}{6.8} + 1\right)$$

$$E_o \approx 0.16 \text{ volt}$$

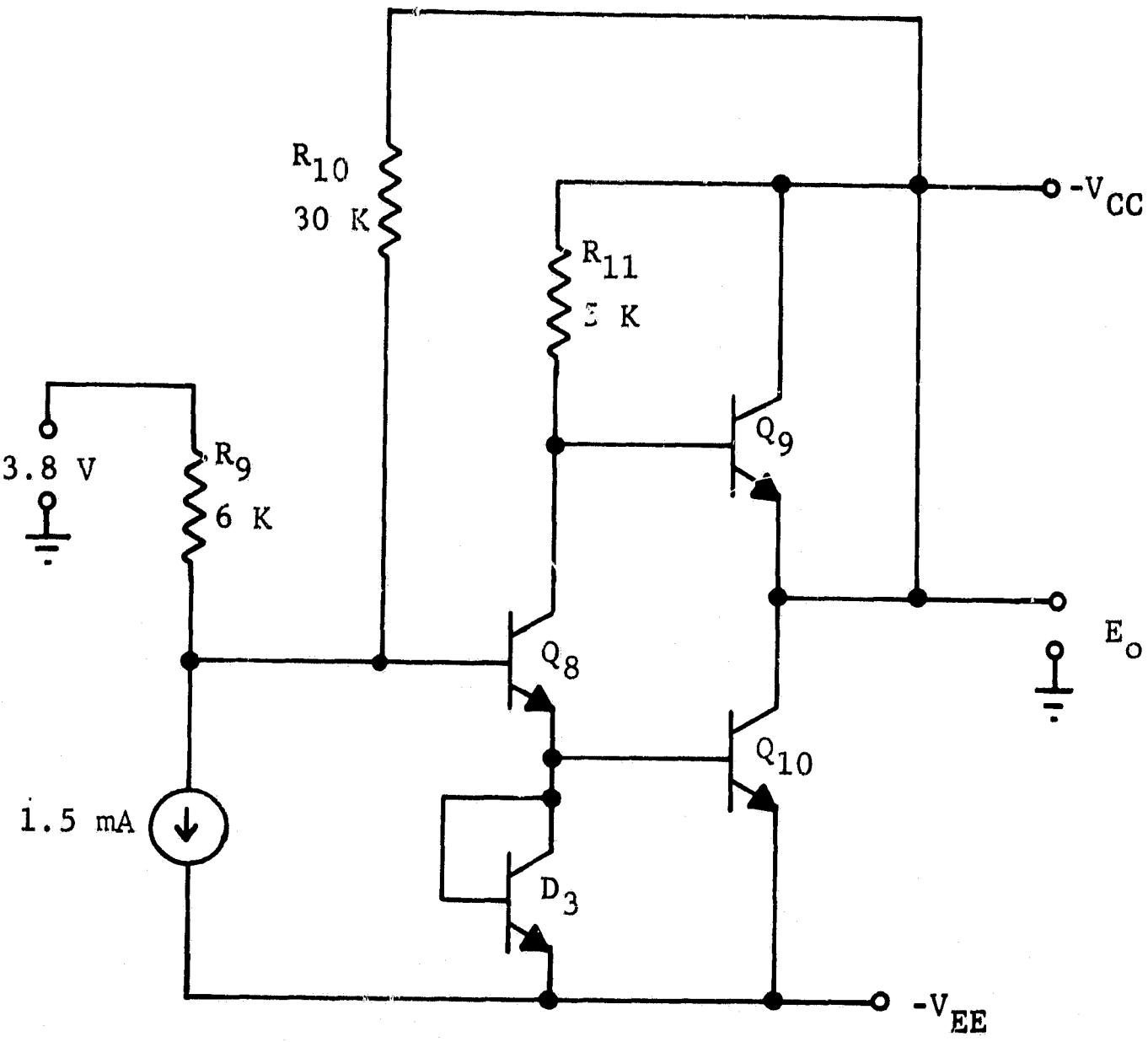


Figure A-8. MC-1530 Level Shifter and Output Amplifier Equivalent Network

This value is in error due to the approximation that $\alpha = 1$, as well as due to the round off of the value calculated for V_{E-Q6}. Were we to reflect this value of voltage back to the input, assuming typical gain, it would result in an offset of approximately -0.3 millivolt. This value is small considering the typical value of 1 millivolt given for this device.

Using the value of E_o calculated above then:

$$V_{C-Q6} = E_o + 0.7 = V_{C-Q6} \text{ volts}$$

$$I_{R_{11}} = \frac{V_{CC} - V_{C-Q6}}{R_{11}}$$

$$I_{R_{11}} = \frac{5.14}{5\ K} = 1.02\ mA$$

The combination of D_4 and Q_{10} is in the same form as D_3 and Q_7 except that the transistor Q_{10} is made up of three transistors connected in parallel, each of which is identical with the diode connected transistor. The emitter current of each, assuming identical characteristics, will be equal to the emitter current of D_4 and the total current which flows in Q_{10} will be approximately equal to three times the current which flows in D_4, which is approximately 1.38 mA, as calculated above. The current in the output transistors will be:

$$I_{C-Q10} \approx I_{C-Q9} \approx 3 \times 1.02$$

$$I_{C-Q9} \approx 3.06\ mA$$

Using the values of the currents and voltages that have been calculated for typical component values, the power dissipation in each component is tabulated below for the 100 milliwatt level.

P_{R1}	1.9 mW	P_{Q1}	1.5 mW	P_{D1}	0.8
P_{R2}	2.2 mW	P_{Q2}	1.7 mW	P_{D2}	0.8
P_{R3}	1.9 mW	P_{Q3}	1.5 mW	P_{D3}	2.2
P_{R4}	1.4 mW	P_{Q4}	2.3 mW		
P_{R5}	3.1 mW	P_{Q5}	1.5 mW		
P_{R6}	1.5 mW	P_{Q6}	3.1 mW		
P_{R7}	0.8 mW	P_{Q7}	2.2 mW		
P_{R8}	8.6 mW	P_{Q8}	6.2 mW		
P_{R9}	11.8 mW	P_{Q9}	17.9 mW		
P_{R10}	0.8 mW	P_{Q10}	18.9 mW		
P_{R11}	5.2 mW				
Total $P_R \approx$	39.2 mW	P Transistor $\approx$	56.8 mW	$P_D \approx$	3.8 mW

Total power = 99.8 milliwatts

MC-1530 - 300-Milliwatt Life Test

The test circuit used in the 300-milliwatt test is a modification of the 100-milliwatt test circuit. This modification consists of connecting a variable resistance between pin 7 and 8, which effectively varies the resistance of R_9. It has been empirically determined that the value of resistance used to produce 300 milliwatts does not cause significant loading on the input differential stage. The operation of Q_4 and Q_5, the second

differential pair, is also not appreciably affected. We can, therefore, represent the circuit operating at the 300-milliwatt level with the network shown in Figure A-10. The resistor R_k represents the parallel combination of R_9 and the external rheostat.

From Figure A-10 it is seen that the total power supplied by V_{CC} and V_{EE} must equal the sum of the power in the box representing the differential amplifier and the Q_7 current source, and that ΔI_{CC} and ΔI_{EE} differ by 0.5 mA. The power which must be dissipated in the output section is then:

$$300 - 33 = 267 \text{ mW}$$

by inspection $\Delta I_{EE} + 0.5 = \Delta I_{CC}$

and

$$\Delta I_{EE} = \frac{267 - 3.0}{12} = 22 \text{ mA}$$

The power dissipated in the shunt resistor must be considered. It was experimentally determined that the 300 milliwatts could be achieved with a nominal shunt resistance of 570 ohms and a current drain of approximately 30 milliamperes would yield the proper power dissipation. At these conditions the total power supplied per device is 360 milliwatts of which approximately 60 milliwatts is dissipated in the external resistor. The average voltage across R_k was determined to be 5.7 volts. The value R_k can be determined by

$$R_k = \frac{(R_{sh})(R_9)}{R_{sh} \quad R_9}$$

$$R_k = \frac{570 \times 6000}{6570} = 520 \text{ ohms}$$

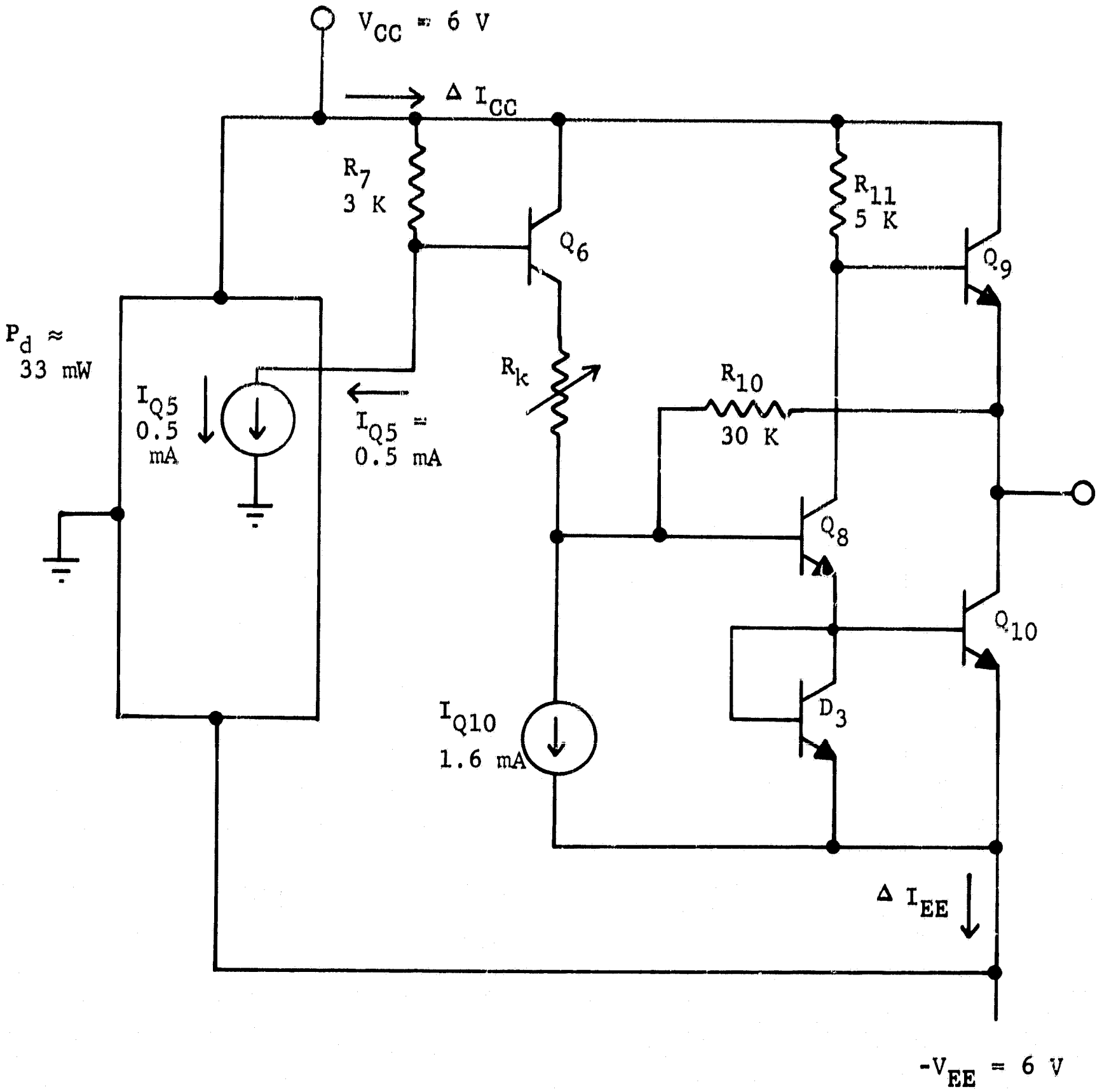


Figure A-9. MC-1530 - 300 Milliwatt Life Test Equivalent Circuit

adjusting ΔI_{EE} for the power in the shunt resistor, we have

$$\Delta I_{EE} = 22 + \frac{60}{12}$$

$$\Delta I_{EE} = 27 \text{ mA}$$

I_{Rk} can be determined by

$$I_{Rk} = \frac{V_{Rk}}{R_k}$$

$$I_{Rk} = \frac{5.7}{5.2} = 11.0 \text{ mA}$$

and

$$I_{b\text{-}Q8} = I_{Rk} - I_{Q7} - I_{R10}$$

neglecting I_{R10} which will be quite small:

$$I_{B\text{-}Q8} \approx 11.0 - 1.6 \approx 9.4 \text{ mA}$$

since the collector load resistance, R_{11}, is equal to 5k, Q_8 will be saturated as, for that matter, will be Q_{10}. The distribution of current between the output loop (Q_9 and Q_{10}) and the driver loop (R_{11}, Q_8, and D_3) will be determined by the difference between V_{SAT} of transistors Q_8 and Q_{10} and the difference between V_{BE}, Q_9, and V_{D3}. This renders the circuit indeterminate to piecewise linear analysis.

The emitter current in Q_8 is equal to the sum of the base and collector currents. The collector current in Q_8 can be determined by

$$I_{C\text{-}Q8} = \frac{V_{CC} - V_{EE} - (V_{D3} - V_{CESAT})}{R_{11}}$$

The offset voltage for this type of transistor will be on the order 0.1 volt and the value of R_{sc} will be approximately 75 ohms, at a level of 2 milliamperes. The value of V_{SAT} will be approximately 0.25 volt and we may assume that V_{D3} = 0.8 volt. Therefore

$$I_{C\text{-}Q8} \approx \frac{12 - 1.05}{5K} \approx 2.2 \text{ mA}$$

and

$$I_{E\text{-}Q8} \approx 11.6 \text{ mA}$$

Regardless of the division of currents between D_3 and Q_{10}, the sum of the currents at the emitter node of Q_{10} must be 27 mA; therefore

$$I_{C\text{-}Q10} = 27 - 11.6 - 1.6 = 13.8 \text{ mA}$$

The voltage at the emitter of Q_6 was found to average 1.2 volts; therefore:

$$V_{CE\text{-}Q6} = 6 - 1.2 = 4.8 \text{ volts}$$

and assuming $V_{BE} \approx 0.7$ volt

$$V_{R7} = 4.1 \text{ volts}$$

In the foregoing analysis, the current in R_{10} has been ignored as has the base current in Q_9.

The power in the critical elements may now be evaluated. Since Q_{10} is saturated, most of the power in the output loop will appear at Q_9. Power in the highly stressed components are

$$P_{Q9} \approx 13.8 \times 12.0 = 166 \text{ mW}$$

$$P_{Q6} \approx 4.8 \times 9.4 = 45 \text{ mW}$$

$$P_{R11} \approx 11 \times 2.2 = 24 \text{ mW}$$

The power dissipated in Q_8, Q_{10}, and D_3 will be approximately 15 milliwatts and the power in R_7, R_9, and the current generator, I_{Q10}, totals 13.2 milliwatts.

SN-526 LIFE TEST CIRCUITS

This section analyzes the stress applied to each identifiable component of the SN-526 operational amplifier while biased using the circuits selected for life testing. It does not stress each component on the die surface inasmuch as this die has more components than used for the circuit operation. This circuit is actually two circuits in one. It can be divided into two principal sections. The first section would include an input network - differential amplifier combination along with a current source that makes it possible to use this circuit as a differential amplifier. The second section is a push-pull output network that permits this circuit to be used as an operational amplifier. The purpose of the second section appears restricted to providing a voltage translation for operation around zero (ground) volts when two supplies are used to provide class B operations as an operational amplifier, and to provide a network capable of driving loads as low as 600 ohms. In actual performance, the gain of this amplifier is achieved in its differential input and the open loop voltage gain (A_{VOL}) characteristics are usually found to be less than one-half of the measured values of the differential voltage gain (A_{dd}).

100-Milliwatt Life Test Stress Analysis

The life test selected for the 100-milliwatt test consisted of applying normal biases to V_{CC} and V_{EE} and grounding input pins 7 and 8. In addition, a 0.01-μF capacitor was connected between pins 3 and 4 for stabilization purposes. The actual power level under test was a function of the basic operational characteristics of these circuits and was not adjusted to the planned 100 milliwatts. The forthcoming analysis concluded that typical power levels, at room temperature and based on Texas Instruments' data sheet resistor values, would be equal approximately to 130 milliwatts.

For the purposes of analysis, this circuit is divided into two sections. The schematic diagram found in Figure A-11 outlines the component identification system used in this analysis. The input network, differential amplifier, voltage divider and the input circuit source are redrawn as shown in Figure A-12. If one assumed the transistors Q_1 and Q_2 contribute little to the power consumption of the circuit and that Q_3 and Q_4, as well as Q_5 and Q_6, are well enough balanced to assume approximately equal shares of the current during this test, then the equivalent circuit drawn in Figure A-12 is adequate for this power distribution analysis.

The current will be controlled by the basic dc current and voltage relationships required between points A, D, and E because, in this circuit, we have essentially a single voltage network. A system of equations has been generated that permit these points to be analyzed by simultaneous equations, thereby permitting the calculation of each component's current load. This series of equations has used the value of 0.720 for the value of V_{BE}. It is also assumed tha $\alpha = 1.0$.

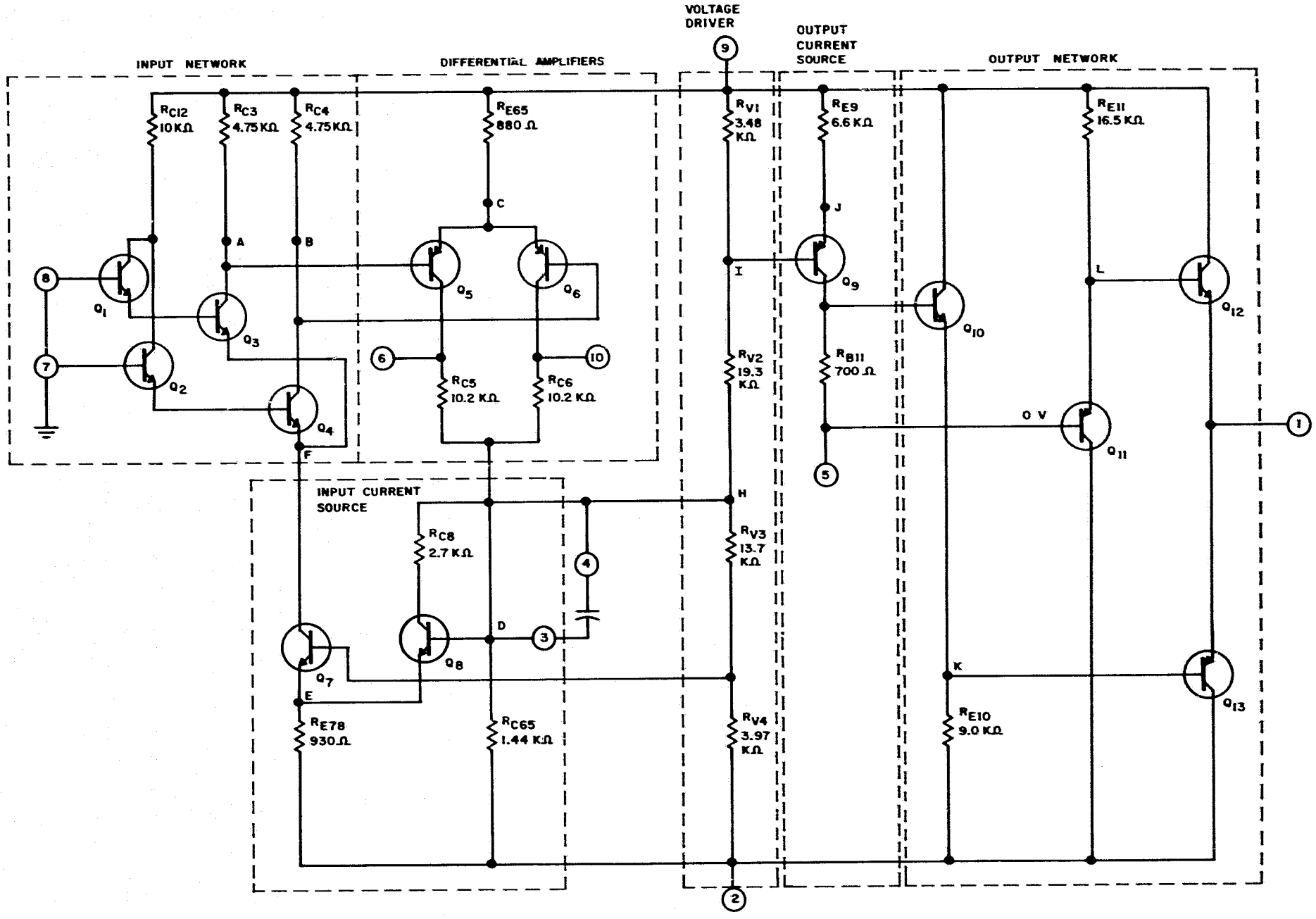


Figure A-10. SN-526, 100-mW Life Test

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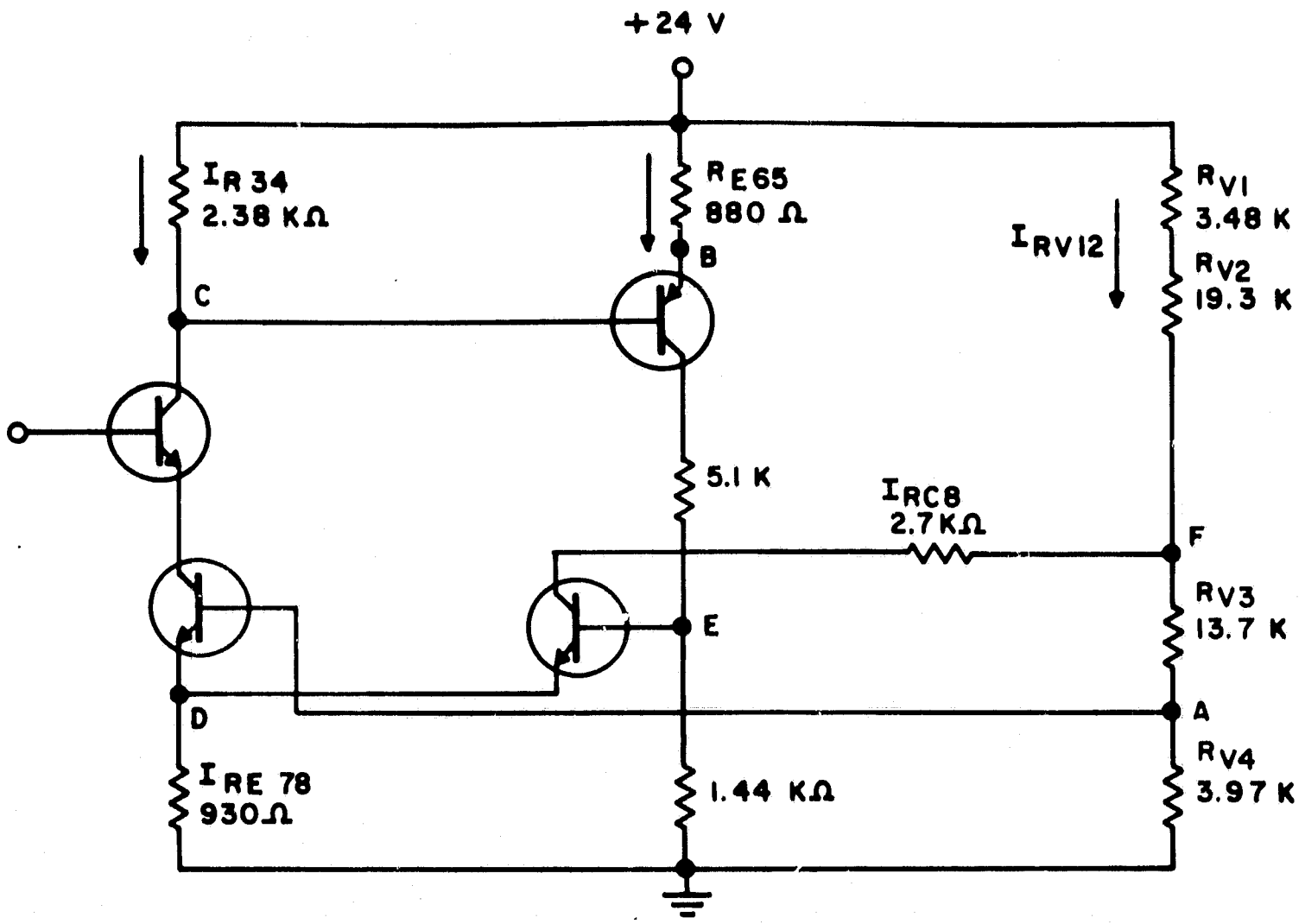


Figure A-11. Equivalent Power Test Circuit Input-Differential Amplifier Section of SN-526- 100 mW Operating Life Tes

With the circuit redrawn in this manner, we can now assume that:

$$I_{RE78} = I_{RC8} + I_{RC34} \tag{17}$$

Since:

$$I_{RC34} = \frac{I_{RE65} \times R_{E65} + V_{BE}}{R_{C34}}$$

then

$$I_{RC34} = \frac{0.88}{2.38} \; I_{RE65} + \frac{V_{BE}}{2.38} \; k\Omega$$

or

$$I_{RC34} = 0.370 \; I_{RE65} + 0.302 \tag{18}$$

substituting equation (18) into equation (17)

$$I_{RE78} = I_{RC8} + 0.370 \; I_{RE65} + 0.302 \tag{19}$$

and

$$I_{RC8} = I_{RE78} - 0.370 \; I_{RE65} - 0.302 \tag{20}$$

At the other end of the circuit it is likewise true that for the current source to function, R_{E78} must receive a part of its current from Q_8. To do this, the voltage at the base of Q_8 must be approximately equal to that of Q_7. This would require that the following condition exist.

$$I_{RE78} \times 0.93 \; k\Omega + V_{BE} = 1.44 \; k\Omega \times I_{RE65} \tag{21}$$

or

$$I_{RE78} = 1.548 \; I_{RE65} - 0.774 \tag{22}$$

Substituting equation (22) in equation (23)

$$I_{RC8} = (1.548 - 0.370)\ I_{RE65} - (0.302 + 0.774)$$

or

$$I_{RC8} = 1.178\ I_{RE65} - 1.076 \qquad (23)$$

Since I_{RC8} is being drawn for the voltage divider, the current flowing in R_{V12}(i.e., R_{V1}, R_{V2}) consists of that current due to I_{RC8} as well as that from the resistor network called I_R. Therefore, I_{RV12} can be represented as follows:

$$I_{RV12} = I_R + I_{RC8} \qquad (24)$$

The voltage at point G (the base of Q_7) is equal to

$$\frac{3.97k}{17.67k}\ (24 - I_{RV12} \times 22.78K) \text{ and } I_{RE78} \times 0.93k + V_{BE}$$

or

$$\frac{3.97k}{17.67k}\ (24v - I_{RV12} \times 22.78\ k\Omega) = I_{RE78} \times 0.93k + V_{BE} \qquad (25)$$

Since by definition

$$I_R = \frac{V_{d(RV3\ +\ RV4)}}{RV3\ +\ RV4}$$

or

$$I_R = \frac{24 - 22.78k\ (IR + IRC8)}{17.67k} = \frac{24 - I_{RV12} \times 22.78\ k\Omega}{17.67k}$$

which reduces to

$$I_{R(mA)} = 0.593 - 0.563\ I_{RC8} \qquad (26)$$

Combining equation (9) and (10), one obtains

$$I_{RE78} = 1.759\ mA - 2.404\ I_{RC8} \qquad (27)$$

Solving equation (27) for I_{RC8} gives:

$$I_{RC8} = -0.416 \quad I_{RE78} + 0.732 \text{ mA} \tag{28}$$

Comparing equation (20) and (28) gives an expression in I_{RE78} and I_{RE65} such that:

$$1.416 \; I_{RE78} - 0.37 \; I_{RE65} + 1.034 \text{ mA} = 0 \tag{29}$$

Solving equations (22) and (29) as a set of simultaneous equations it is found that

$$I_{RE65} = 1.169 \text{ mA}$$

From this other critical values are found to be equal to:

$$I_{RE78} = 1.036 \text{ mA}$$

$$I_{RC34} = 0.735 \text{ mA}$$

$$I_{RC8} = 0.301 \text{ mA}$$

$$I_{R} = 0.424 \text{ mA}$$

Using these figures, the approximate current-voltage relationship for the first half of this circuit can be derived and are found in Table A-I.

The output stage is designed for current amplification and to establish signal zero at pin 1 at ground potential. Since the output has been designed to operate class B, we, for the purposes of this analysis, will neglect the base current existing in the output transistors Q_{11} and Q_{13}. Neglecting the output transistors, the circuit can be redrawn as shown in Figure A-13. The 412.5k ohm

TABLE A-I

SUMMARY OF 100-MW LIFE TEST
FOR SN-526 POWER DISTRIBUTION

Circuit Element	Voltage (Volts)	Current (mA)	Power (mW)
Q_1	12.7	0.01	0.127
Q_2	12.7	0.01	0.127
Q_3	11.70	0.368	4.30
Q_4	11.70	0.368	4.30
Q_5	15.063	0.584	8.80
Q_6	15.063	0.584	8.80
Q_7	9.586	0.735	7.04
Q_8	7.320	0.301	2.203
Q_9	10.00	0.0292	2.431
Q_{10}	12.720	0.683	8.68
Q_{11}	12.720	1.253	15.60
Q_{12}	12.00	1.0	12
Q_{13}	12.00	1.0	12
R_{C12} = 10k ohms	0.20	0.020	0.004
R_{C3} = 4.75k ohms	1.74	0.368	0.640
R_{C4} = 4.75k ohms	1.74	0.368	0.640
R_{E78} = 930 ohms	0.974	1.036	0.997
R_{E65} = 880 ohms	1.03	1.169	1.200
R_{C5} = 10.2k ohms	5.95	0.584	3.490
R_{C6} = 10.2k ohms	5.95	0.584	3.49
R_{C8} = 2.7k ohms	0.814	0.301	0.245
R_{C65} = 1.44k ohms	1.68	1.169	1.963
R_{V1} = 3.48k ohms	2.00	0.575	1.150
R_{V2} = 19.3k ohms	11.10	0.575	6.38
R_{V3} = 13.k ohms	5.80	0.424	2.46
R_{V4} = 3.97k ohms	1.680	0.424	0.712
R_{E9} = 6.6k ohms	1.28	0.194	0.248
R_{B11} = 700 ohms		0.027	0.015
R_{E10} = 9.0k ohms	11.28	1.253	14.133
R_{E11} = 16.5k ohms	11.28	0.684	7.704
			129.8

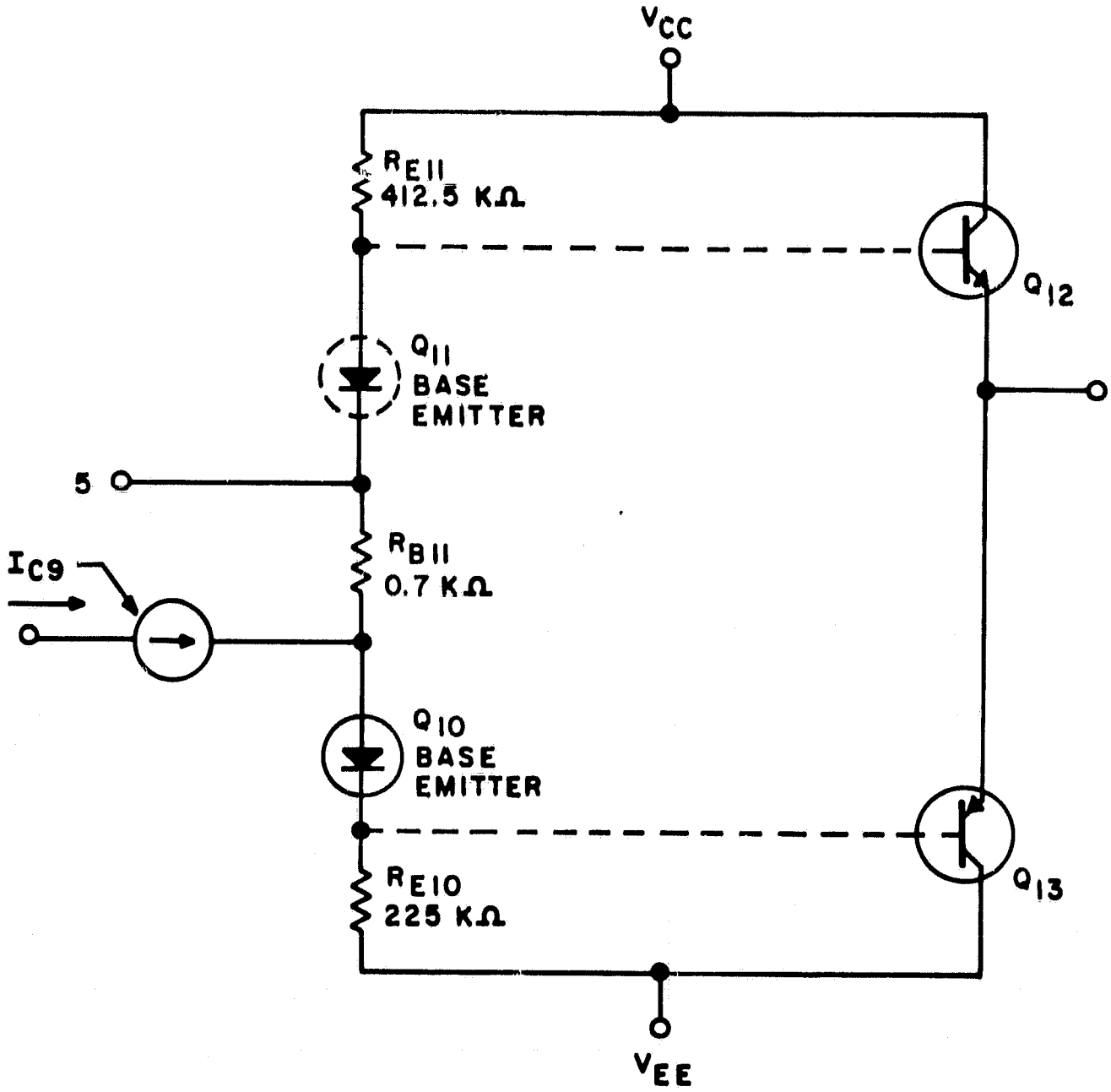


Figure A-12. Equivalent Circuit, Output Section SN-526A

resistor and the 225k-ohm resistor are the values of R_{E11} and R_{E10} referred to the base of transistors Q_{11} and Q_{10}, respectively, assuming a transistor beta of 25. The base emitter junctions can then be represented as diodes.

Neglecting the current supplied by the collector of Q_9, the voltage at the base of Q_{12} is seen to be -2.58 volts and at the base of Q_{13} the voltage is -4.05 volts. These voltages will be modified (made more positive) by the current supplied by Q_9.

Analysis of the structure of Q_9 showed that the base emitter of this transistor is shunted by a NP diode formed by low resistivity N diffusion into the base region of Q_9. This would produce a transistor of low α, the value of which would depend on the voltage and current levels applied. Therefore, the assumption of $\alpha \approx 1$ is NOT valid for this device.

If we assume that the output is approximately 0 volts, then the voltage at the base of Q_{12} will be +0.72 and the voltage at the base of Q_{13} will be approximately -0.72. Assuming 0 base current in both output transistors, it is seen that I_{RE10} is 1.253 mA and I_{RE11} is 0.684 mA.

Referring to the circuit shown in Figure A-13, the current which must be supplied by Q_9 to establish these voltages may be calculated.

With -0.72 volt at $R_{E10(eq)}$ it can be seen that there must be 0.0565 mA flowing in $R_{E10(eq)}$. The current flowing from the position supply, I_{RE11}, will be, under these conditions, 0.0273 mA. The current supplied by Q_9 will be, then, approximately 0.0292 mA.

It can be seen that the base emitter voltages Q_{12} and Q_{13} are at the threshold of base current flow. It is conceivable, therefore, that some emitter current is flowing in both transistors. Under the 100-mW life test condition, there is no external load on the output, because the geometry of Q_{10} and Q_{12} is identical with the geometry of Q_{11} and Q_{13}. Since they are effectively biased at equivalent impedance levels the current flowing in output transistors will be nearly equal to that which flows in Q_{10} and Q_{11}. If we, for convenience, assume that the current flowing is equal to 1 mA, then the power dissipated in each output transistor will be 12 mW and the total power dissipated by the circuit will be approximately 130 mW which is consistent with the published typical value for this device.

300-mW LIFE TEST ANALYSIS

The major difference between this test (shown in Figure A-14) and the 100-mW test is that the stresses applied to the circuits are not equally distributed as they were in the 100-milliwatt test. To obtain the overstress conditions and to stress the stability characteristics of the output section of the operational amplifier, it was decided to concentrate the major portion of the power stress on the output Class B amplifier section, with less concentration on the input-differential network. In this program, the evaluation is principally interested in the SN-526's characteristics as an operational amplifier. However, to obtain over 500 milliwatts of total circuit stress as required in the power step stress tests, it was necessary to also load the outputs of the differential amplifier.

For this test condition, the analysis can be simplified. If the input network and differential amplifier can be redrawn as shown in Figure A-15, then it is noted that the current values are controlled by the voltage level at Point A. Using this fact, it is then an easy task to compute the currents in this section. They are

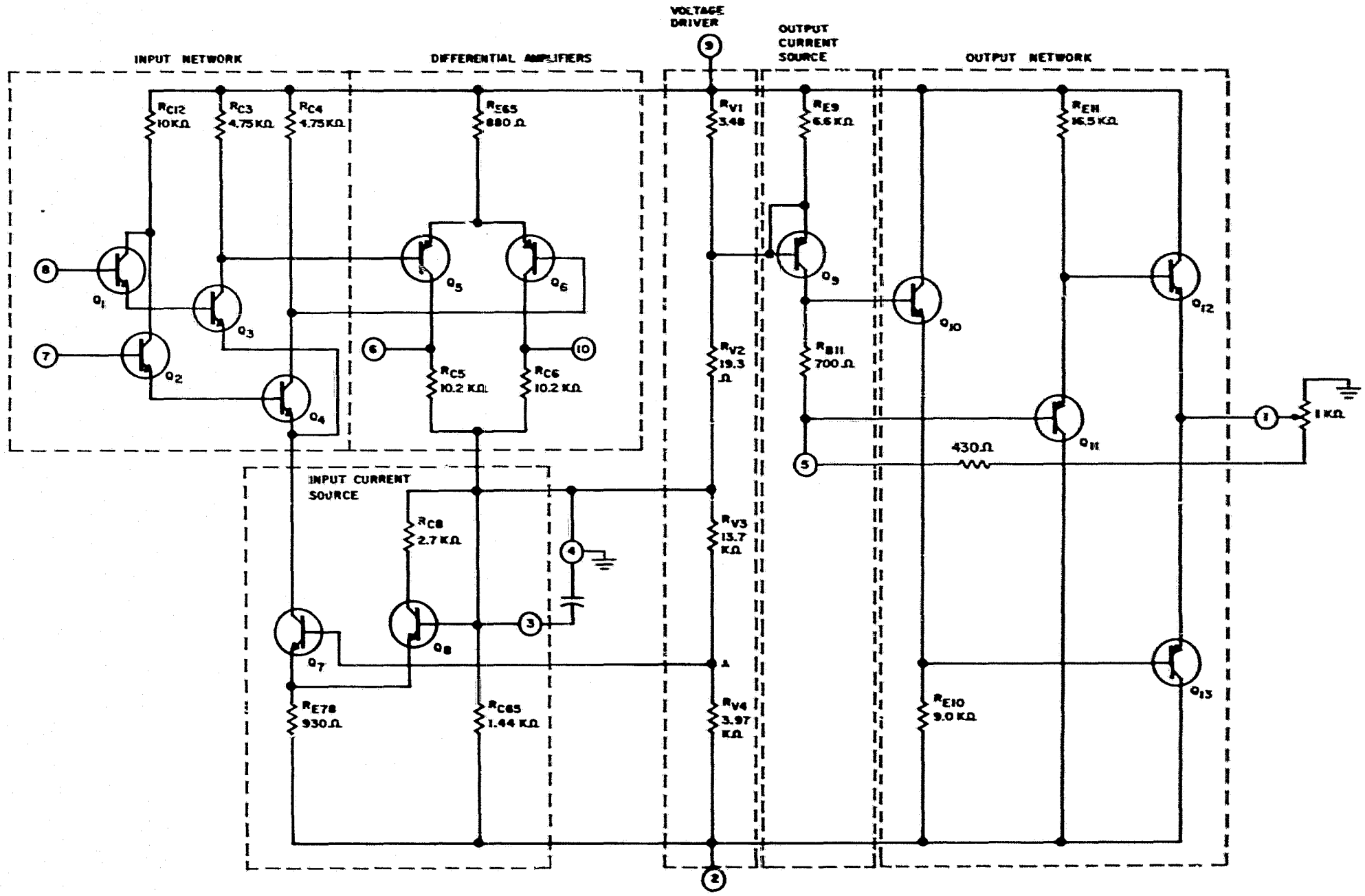


Figure A-13. SN-526, 300-mW Life Test Bias Conditions

6653-9-7

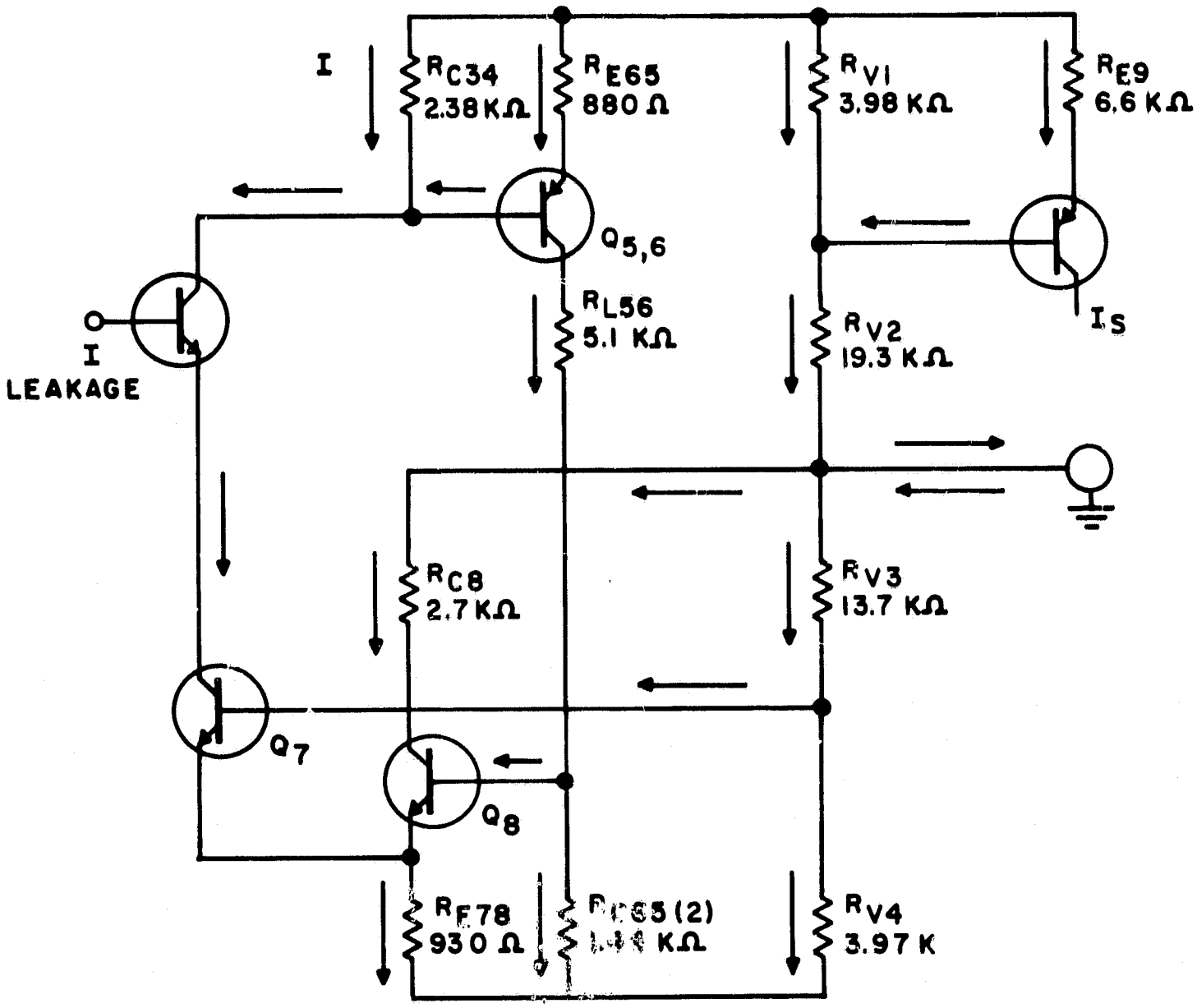


Figure A-14. Equivalent Power Test Circuit Input-Differential Amplifier Section of SN-526 - 300 mW Operating Life Test

summarized in Table A-II. Using the same basic analogy as in the 100-mW analysis to describe the output of the SN-526, Figure A-16, it is seen that the various load conditions do not appreciably change the power load carried by the majority of the components in this output section. Inasmuch as the potentiometer used to simulate a load was adjusted for each device, the estimated power load for Q_{12} was arrived at by subtracting the dissipation of the remainder of the circuit and receiving a normalized value of load for that one element.

TABLE A-II
SUMMARY OF 300-MILLIWATT LIFE TEST
FOR SN-526 POWER DISTRICUTION

Circuit Element	Voltage (Volts)	Current (mA)	Power (mW)
Q_3, Q_4 + Q_7	19.645	1.00	19.645
Q_5	13.416	0.938	12.584
Q_6	13.416	0.938	12.584
Q_8	6.972	1.129	7.871
Q_9	6.888	0.168	6.197
Q_{10}	15.12	0.80	12.096
Q_{11}			≈0
Q_{12}	8.72	14.774	128.831
Q_{13}	15.28	1.5	22.92
R_{C12} = 10k ohms			-
R_{C3} = 4.75k ohms	2.375	0.500	1.187
R_{C4} = 4.75k ohms	2.375	0.500	1.187
R_{E78} = 930	1.980	2.129	4.215
R_{E65} = 880	1.650	1.875	3.094
R_{C5} = 10.2k ohms	9.568	0.938	8.974
R_{C6} = 10.2k ohms	9.568	0.938	8.974
R_{C8} = 2.7k ohms	3.048	1.129	3.441
R_{C65} = 1.44k ohms	2.700	1.875	5.062
R_{V1} = 3.48k ohms	1.834	0.527	0.966
R_{V2} = 19.3k ohms	10.171	0.527	5.360
R_{V3} = 13.7k ohms	9.302	0.679	6.316
R_{V4} = 3.97k ohms	2.696	0.679	1.830
R_{E9} = 6.6k ohms	1.112	0.168	0.187
R_{B11} = 700k ohms		≈0	
R_{E10} = 9.0k ohms	14.40	1.586	22.648
R_{E11} = 16.5k ohms	8.00	0.485	3.880

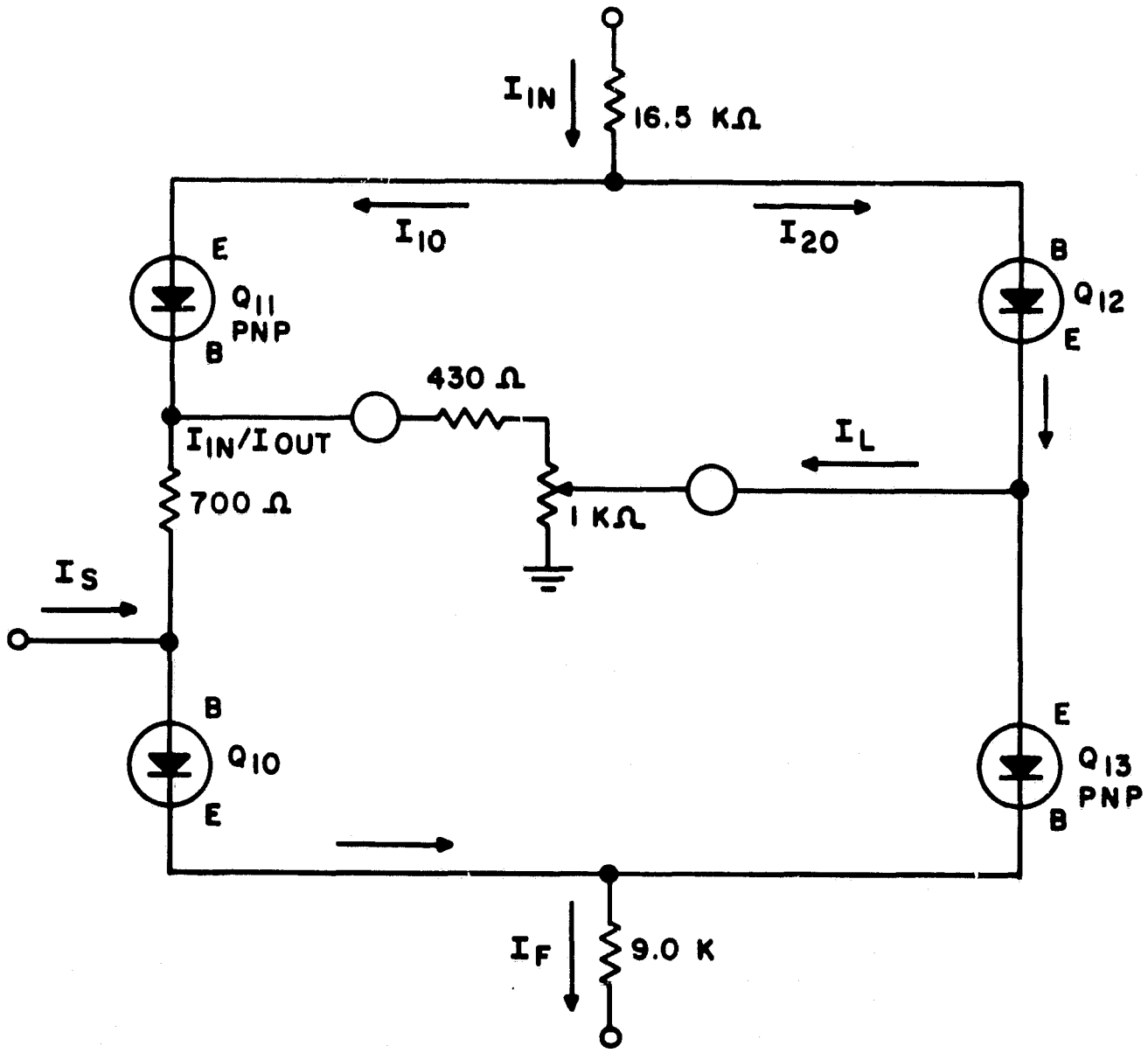


Figure A-15. Output Section of SN-526 Simplified With Load Conditions Added

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